



## 70V, 2.5mA Precision Protection APD Bias Dual-Gain Track/Hold Current Mirror

## General Description

The SY26501 develops a peak current mode-controlled boost regulator and a high-side driver with accurate current monitor to drive the optical modules. The device operates over a wide input voltage from 2.8V to 5.5V and is capable of generating up to 70V regulated output, a  $1\times/1.8\times$  dual-gain current mirror with a track and hold output buffer, which is unique to simplify the fiber module circuit design with a MCU with regular resolution ADC.

The SY26501 operates at a fixed 850kHz switching frequency that allows use of small external ceramic capacitors and inductor. The SY26501 features cycle-by-cycle current limit of boost switch, adjustable driver current limit, input UVLO and thermal protection.

The SY26501 is available in a thermally enhanced, QFN3×3-16 package. It operates over an ambient temperature range of -40°C to +85°C.

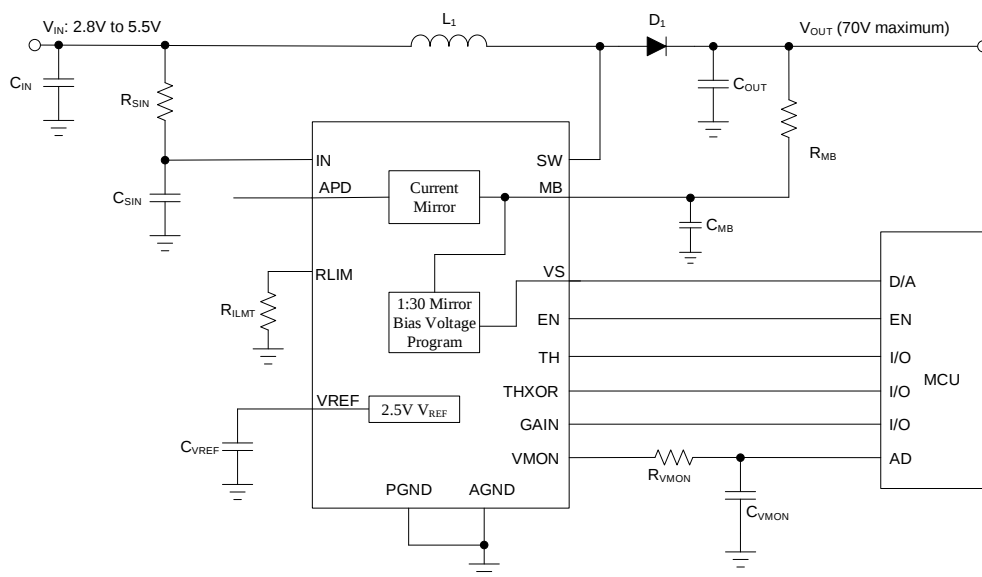
## Features

- Wide Input Range: 2.8V to 5.5V
- Wide Output Voltage Range from ( $V_{IN} + 5V$ ) to 70V
- 850kHz Switching Frequency
- Less Than 1 $\mu$ A Shutdown Current
- 1:30 Output Voltage Programming
- Adjustable Precision, Over-Current Protection
- Internal 1 $\times$ /1.8 $\times$  Dual-Gain Current Mirror
- Up to 2.5V Voltage Buffer for Full-Scale Output Current
- Input Voltage UVLO
- Over Temperature Protection
- Full Chain Circuit: Bias-Mirror-Track/Hold
- Compact Package: QFN3 $\times$ 3-16
- -40 $^{\circ}$ C to +85 $^{\circ}$ C Operating Temperature Range

## Applications

- Fiber Modules with APD Photon Sensor
- Laser Beam Finders (LIDA)

## Typical Applications



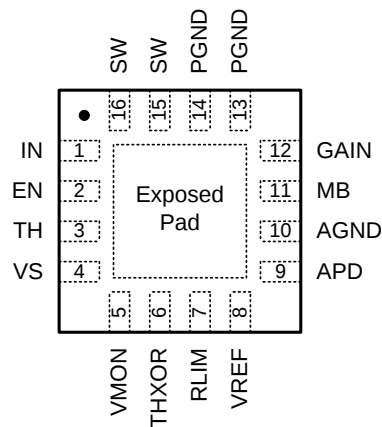
### Figure1. Schematic Diagram

## Ordering Information

| Ordering Part Number | Package Type                                 | Top Mark |
|----------------------|----------------------------------------------|----------|
| SY26501QDQ           | QFN3×3-16<br>RoHS Compliant and Halogen Free | DWBxyz   |

x=year code, y=week code, z= lot number code

## Pinout (top view)



| Pin         | Name  | Type | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------------|-------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1           | IN    | P    | IC power supply input. Bypass this pin to ground with at least a 1μF ceramic capacitor.                                                                                                                                                                                                                                                                                                                                                       |
| 2           | EN    | I    | Enable control input. Pull this pin high to turn on the IC.                                                                                                                                                                                                                                                                                                                                                                                   |
| 3           | TH    | I    | Track or Hold Input. Input high for tracking (when THXOR is logic low; check THXOR description for more detail), where the VMON follows the current output of the APD pin simultaneously; low for holding where the VMON outputs a snapshot of APD current captured right after the following edge of the signal applied on the TH pin, in which the APD current snapshot is converted into a voltage and is stored in an internal capacitor. |
| 4           | VS    | I    | Proportional input for programming the MB voltage with an increment gain of 1:30.                                                                                                                                                                                                                                                                                                                                                             |
| 5           | VMON  | O    | Current Monitoring Output. Its voltage is proportional to the current of the APD pin.                                                                                                                                                                                                                                                                                                                                                         |
| 6           | THXOR | I    | Logic input. The complementary logic level of THXOR and TH is set for tracking and holding. Pull this pin high to select input low of TH for tracking function, and input high of TH for holding function. Pull this pin Low to select input high of TH for tracking function, and input low of TH for holding function.                                                                                                                      |
| 7           | RLIM  | I    | Current-Limit Programming. Connect a resistor from RLIM to AGND to program the APD current-limit threshold.<br>$I_{APD\_MAX} (mA) = \frac{70}{R_{LIM} (k\Omega)}$                                                                                                                                                                                                                                                                             |
| 8           | VREF  | O    | Reference Voltage Output.                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 9           | APD   | O    | Output for Biasing the APD Device. The current out of this pin is sampled with a mirror circuit for current monitoring and over-current protection.                                                                                                                                                                                                                                                                                           |
| 10          | AGND  | G    | Signal Ground. Connect directly to the local ground plane. Connect AGND to PGND at a single point, typically near the return terminal of the output capacitor.                                                                                                                                                                                                                                                                                |
| 11          | MB    | I    | Mirror Bias Input. Connected to the boost stage output.                                                                                                                                                                                                                                                                                                                                                                                       |
| 12          | GAIN  | I    | 1×/1.8× Gain Selection Input. Input low to select 1× gain and high to select 1.8× gain; where the 1× gain has an equivalent conversion gain of 1.25kΩ and 2.25kΩ for 1.8× gain.                                                                                                                                                                                                                                                               |
| 13,14       | PGND  | G    | Power Ground. Connect the negative terminals of the input and output capacitors to PGND. Connect PGND externally to AGND at a single point, typically at the return terminal of the output capacitor.                                                                                                                                                                                                                                         |
| 15,16       | SW    | O    | Low End Boost Switch Output. Connect inductor to SW. Minimize the trace area at SW to reduce switching-noise emission.                                                                                                                                                                                                                                                                                                                        |
| Exposed Pad | GND   | G    | Exposed Pad. Connect to a large copper plane at the AGND and PGND potential to improve thermal dissipation. Do not use as the only ground connection.                                                                                                                                                                                                                                                                                         |

## Block Diagram

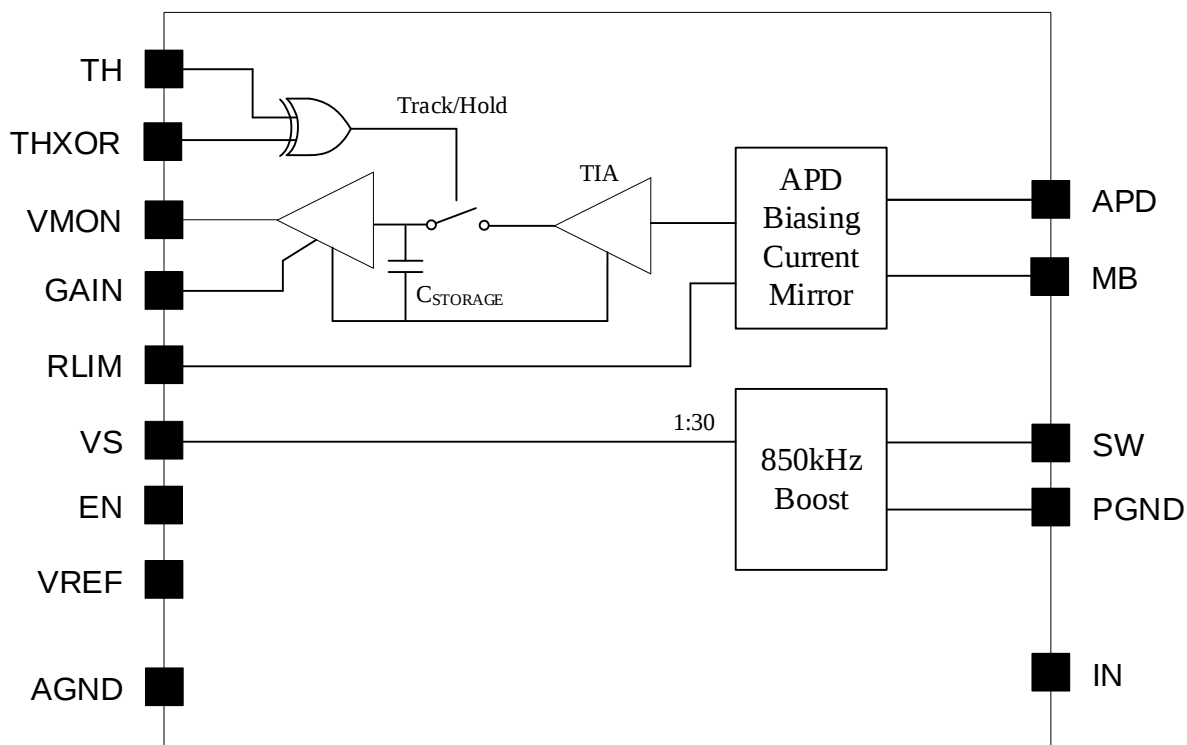


Figure2. Block Diagram

| Absolute Maximum Ratings (1)                  | Min  | Max          | Unit |
|-----------------------------------------------|------|--------------|------|
| IN, EN, VS, TH, THXOR, VMON, RLIM, VREF, GAIN | -0.3 | 6            | V    |
| SW, MB                                        | -0.3 | 76           |      |
| APD                                           | -0.3 | $V_{MB}+0.3$ |      |
| LX, 10ns Duration                             | -6   | 83           |      |
| LX, 50ns Duration                             | -3   | 80           |      |
| LX, 200ns Duration                            | -1   | 78           | °C   |
| Junction Temperature, Operating               | -40  | 150          |      |
| Lead Temperature (Soldering, 10 sec.)         |      | 260          |      |
| Storage Temperature                           | -65  | 150          |      |

| Thermal Information (2)                              | Typ | Unit |
|------------------------------------------------------|-----|------|
| $\theta_{JA}$ Junction-to-ambient Thermal Resistance | 37  | °C/W |
| $\theta_{JC}$ Junction-to-case Thermal Resistance    | 27  |      |
| $\theta_{JB}$ Junction-to-board Thermal Resistance   | 13  |      |
| $P_D$ Power Dissipation $T_A = 25^\circ\text{C}$     | 2.7 | W    |

| ESD Ratings               | Min  | Max | Unit |
|---------------------------|------|-----|------|
| HBM (Human Body Mode)     | -1.5 | 1.5 | kV   |
| CDM (Charged Device Mode) | -750 | 750 | V    |

| Recommended Operating Conditions (3) | Min | Max | Unit |
|--------------------------------------|-----|-----|------|
| IN                                   | 2.8 | 5.5 | V    |
| APD                                  | 10  | 70  |      |
| APD Current                          |     | <2  | mA   |
| Junction Temperature, Operating      | -40 | 125 | °C   |
| Ambient Temperature                  | -40 | 85  |      |

**Electrical Characteristics** ( $V_{IN} = 3.3V$ ,  $T_J = -40^{\circ}C$  to  $+85^{\circ}C$ . Typical values are at  $T_J = 25^{\circ}C$ , unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

| Parameter                                            | Symbol                | Test Conditions                                   | Min  | Typ  | Max  | Unit   |
|------------------------------------------------------|-----------------------|---------------------------------------------------|------|------|------|--------|
| Input Voltage Range                                  | V <sub>IN</sub>       |                                                   | 2.8  |      | 5.5  | V      |
| Efficiency (Note 5)                                  | η                     | V <sub>OUT</sub> =50V, 1mA loading                |      | 40   |      | %      |
| Input UVLO                                           | V <sub>UVLO</sub>     |                                                   | 2.3  | 2.5  | 2.7  | V      |
| Input UVLO Hysteresis                                | V <sub>UVLO,HYS</sub> |                                                   |      | 200  |      | mV     |
| Quiescent Current                                    | I <sub>Q</sub>        |                                                   |      | 500  | 700  | μA     |
| Shutdown Current                                     | I <sub>SHDN</sub>     | EN=Low                                            |      | 0.02 | 2    | μA     |
| Output Short Circuit Operation Current (Note 5)      | I <sub>SHRT</sub>     | V <sub>OUT</sub> =40V, R <sub>LIM</sub> =28kΩ     |      | 60   |      | mA     |
| Thermal Shutdown Temperature (Note 4)                | T <sub>SD</sub>       | Temperature rising                                |      | 160  |      | °C     |
| Thermal Shutdown Hysteresis (Note 4)                 | T <sub>HYS</sub>      |                                                   |      | 15   |      | °C     |
| LOGIC IO                                             |                       |                                                   |      |      |      |        |
| Logic High Level                                     | V <sub>HIGH</sub>     |                                                   | 1.1  |      |      | V      |
| Logic Low Level                                      | V <sub>LOW</sub>      |                                                   |      |      | 0.4  | V      |
| Input Low Sourcing                                   | I <sub>LB</sub>       | Bias to V <sub>LOW</sub>                          |      | 10   |      | nA     |
| BOOST AND APD BIASING                                |                       |                                                   |      |      |      |        |
| Boost FET RON                                        | R <sub>DS(ON)</sub>   |                                                   |      | 0.6  | 1    | Ω      |
| Switching Frequency                                  | f <sub>S</sub>        |                                                   | 680  | 850  | 1020 | kHz    |
| Maximum Duty Cycle (Note 4)                          | D <sub>MAX</sub>      |                                                   | 90   | 94   | 98   | %      |
| Output Voltage Accuracy                              | V <sub>MB,ACY</sub>   | V <sub>OUT</sub> =20V~60V, 1mA load               | -1.5 |      | 1.5  | %      |
| V <sub>VS</sub> to V <sub>MB</sub> Programming Ratio | VPR                   |                                                   |      | 30   |      | V/V    |
| Soft-Start Time                                      | t <sub>SS</sub>       | From EN ON, 60V output voltage, no load           |      | 2.5  |      | ms     |
| Boost FET Current Limit                              | I <sub>PEAK</sub>     |                                                   | 0.6  | 0.68 | 0.76 | A      |
| Switch Leakage Current                               |                       | V <sub>SW</sub> = 72V, T <sub>A</sub> = 25°C      |      | 0.01 | 0.1  | μA     |
| Mirror Voltage Drop                                  | V <sub>MD</sub>       | I <sub>APD</sub> = 100μA, V <sub>OUT</sub> = 70V  | 0.8  | 1    | 1.2  | V      |
|                                                      |                       | I <sub>APD</sub> = 2mA, V <sub>OUT</sub> = 70V    | 1.15 | 1.35 | 1.55 | V      |
| VREF PIN                                             |                       |                                                   |      |      |      |        |
| Internal Reference Voltage                           | V <sub>REF</sub>      |                                                   | 2.38 | 2.48 | 2.58 | V      |
| Load Regulation                                      |                       | From 0 to 1mA                                     | 0.3  | 0.6  | 0.9  | %      |
| Temperature Co-efficiency (Note 4)                   |                       |                                                   |      | 50   |      | ppm/°C |
| DRIVER AND CURRENT MONITOR                           |                       |                                                   |      |      |      |        |
| 1× Transfer Resistance                               | TR <sub>1×</sub>      | APD current to VMON transferring ratio, 1× gain   |      | 1.25 |      | kΩ     |
| 1.8× Transfer Resistance                             | TR <sub>1.8×</sub>    | APD current to VMON transferring ratio, 1.8× gain |      | 2.25 |      | kΩ     |
| Current Mirror Accuracy                              | I <sub>MIR, ACC</sub> | I <sub>APD</sub> = 3μA ~25μA (Note 4)             | -10  |      | 10   | %      |
|                                                      |                       | I <sub>APD</sub> = 25μA~2mA                       | -5   |      | 5    | %      |



## Electrical Characteristics ( $V_{IN} = 3.3V$ , $T_J = -40^{\circ}C$ to $+85^{\circ}C$ . Typical values are at $T_J = 25^{\circ}C$ , unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

| Parameter                   | Symbol       | Test Conditions                                                                          | Min | Typ | Max | Unit |
|-----------------------------|--------------|------------------------------------------------------------------------------------------|-----|-----|-----|------|
| Settle Time (Note 4)        | $t_{ST}$     | APD to VMON settle time, to 90% for rising and 10% for falling, to 1mA and to 10 $\mu$ A |     | 200 | 300 | ns   |
| TH Effective Delay (Note 4) | $t_{DELAY}$  | TH to track/hold and 1 $\times$ /8 $\times$ effective delay                              |     | 50  |     | ns   |
| Holding Droop (Note 4)      | $V_{DROOP}$  | Voltage droop measured in 10ms when holding 1V                                           |     | 3   |     | V/s  |
| $I_{LIM}$ Programming Error | $I_{LIMERR}$ | Test with $R_{LIM} = 28k\Omega$ for $I_{LIM} = 2.5mA$                                    | -15 |     | 15  | %    |
|                             |              | Test with $R_{LIM} = 47k\Omega$ for $I_{LIM} = 1.49mA$                                   | -15 |     | 15  | %    |

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

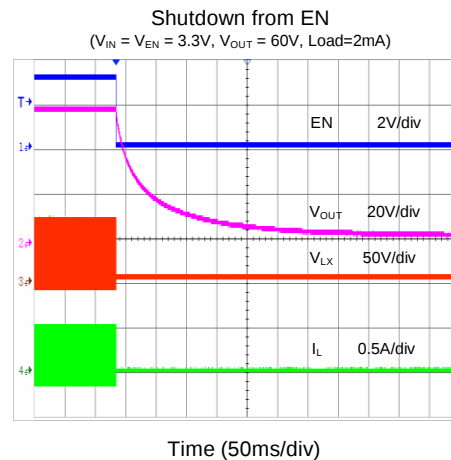
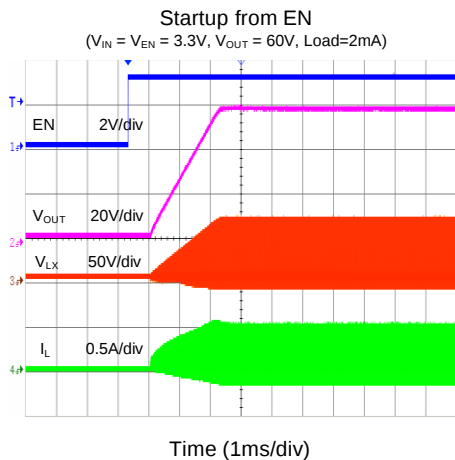
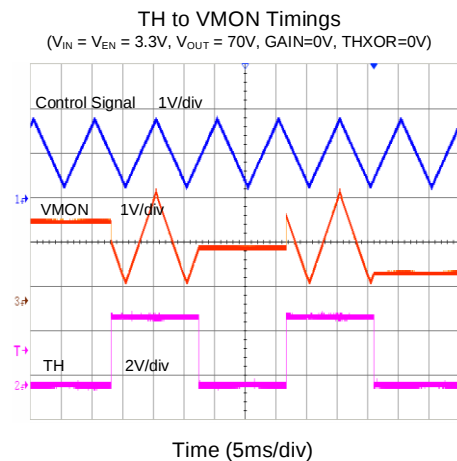
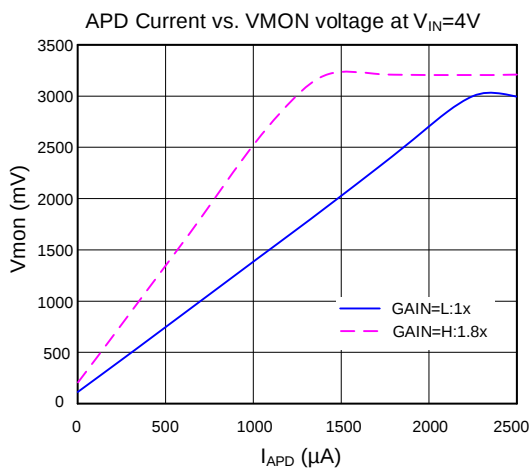
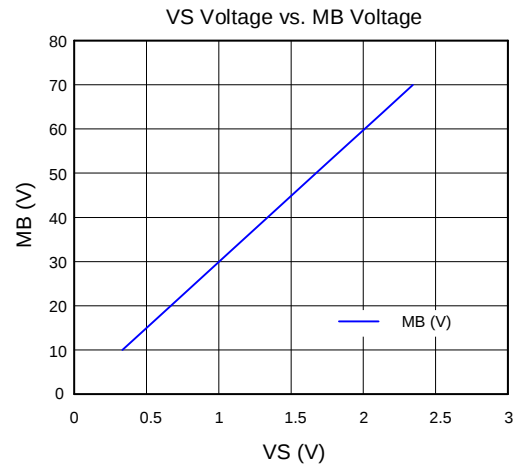
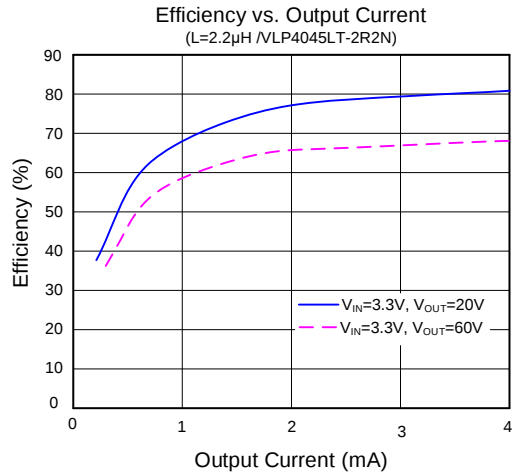
**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^{\circ}C$  on a low effective two-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

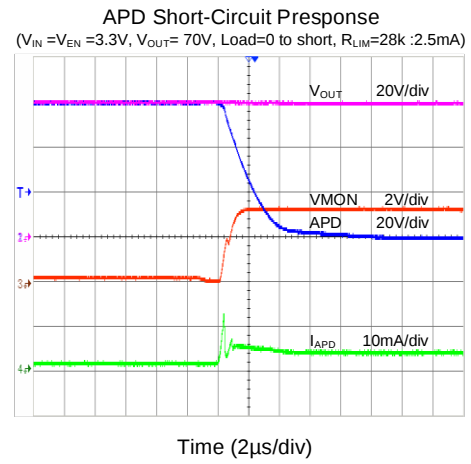
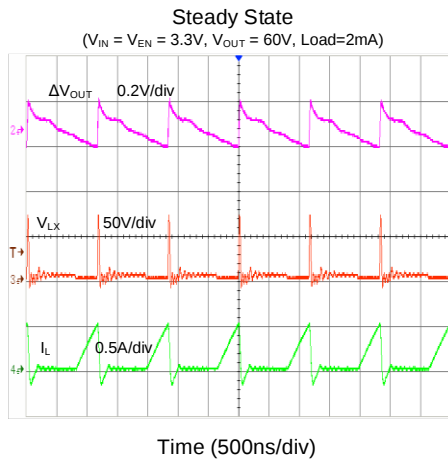
**Note 3:** The device is not guaranteed to function outside its operating conditions.

**Note 4:** Guaranteed by design.

**Note5:** Based on bench test data.

## Typical Performance Characteristics





## Applications Information

The SY26501 develops a peak current mode controlled Boost regulator and a high-side driver with accurate current monitor to drive the optical modules. The device operates over a wide input voltage from 2.8V to 5.5V and is capable of generating up to 70V regulated output, a 1×/1.8× dual-gain current mirror with a track and hold output buffer, which is unique to simplify the fiber module circuit design with a MCU with regular resolution ADC.

The SY26501 operates at a fixed 850kHz switching frequency that allows using small external ceramic capacitors and inductor.

### Enable and Disable:

When the EN pin is pulled to high voltage (>1.1V), the SY26501 is enabled. When the EN pin is pulled to low voltage (<0.4V), the SY26501 goes into shutdown mode. Less than 1μA input current is consumed in shutdown mode.

### Extending the Monitoring Range:

The GAIN pin input is for selecting 1×/1.8× gains for proper output levels, that extends the appreciated monitoring range by 1.8 times. The gain could be changed during tracking or holding, with less interference injection. As the fiber receiver monitors signal in very high dynamic range but less resolution, this circuit brings out a unique tradeoff between the resolution and dynamic range.

### Programming the Current Limit:

Connect a resistor from RLIM pin to AGND to program the current-limit threshold. The  $R_{LIM}$  for setting the current limit level is calculated with the following equation, and please refer to the Figure 3 for the typical  $I_{LIM}$  to  $R_{LIM}$  plot.

$$R_{LIM}(k\Omega) = \frac{70}{I_{APD\_MAX}(mA)}$$

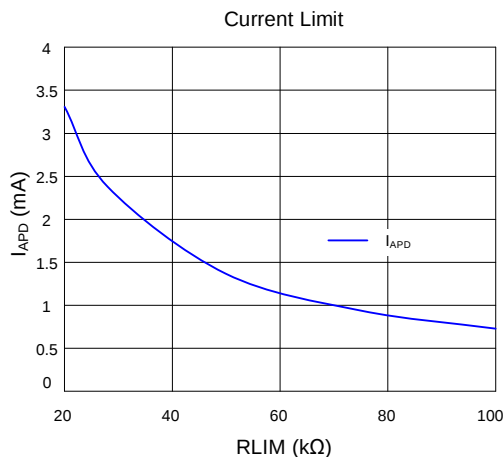


Figure 3. APD Current Limit vs.  $R_{LIM}$

### Ripple Filtering:

A simple RC filtering circuit could help in suppression of ripple applied at MB input, which then improving the modulation effect to the signal picked-up in the optical channel. Refer to the Figure 4. The recommended values of  $R_{MB}$  and  $C_{MB}$  are 100Ω and 0.1μF.

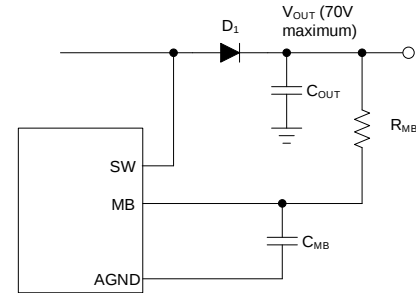


Figure 4. RC Filtering for Ripple Suppression

### VMON Parameter Setting:

The  $R_{VMON}$  and the  $C_{VMON}$  placed close to the ADC input are for ringing dump that occurs when the ADC input switch cuts for holding. These two components do not affect the transient, but induce interference to the measurement. Those components should also be evaluated on the final PCB. The recommended values of  $R_{VMON}$  and  $C_{VMON}$  are 510Ω and 100pF. Refer to the Figure 5.

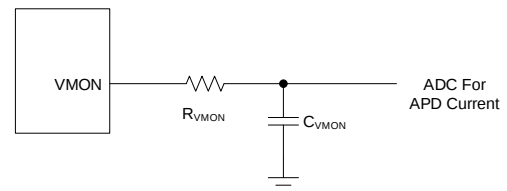


Figure 5. VMON Parameter

### Input Capacitor C<sub>IN</sub>:

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the  $V_{IN}$  and PGND pin. Care should be taken to minimize the loop area formed by  $C_{IN}$ ,  $V_{IN}$ , and the PGND pin. In this case a 10μF low ESR ceramic capacitor is recommended. The SIN capacitor must be close to the IN Pin and AGND pin to minimize the potential noise problem. Care should be taken to minimize the loop area formed by  $C_{SIN}$ , and IN/AGND pins. In this case a 100nF low ESR ceramic is recommended.

### Output Capacitor C<sub>OUT</sub>:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X7R ceramic capacitor 0.1μF capacitance.

## Rectifier Diode:

Because of high switching speed of the SY26501, a schottky diode with low forward voltage and fast switching speed is desirable for the application. The voltage rating of the diode must be higher than maximum ( $V_{OUT}-V_{IN}$ ) voltage. The diode's average and peak current rating should exceed the average output current and peak current. The recommended value of D is BAT46W.

## VREF Parameter Setting:

The 2.48V VREF is the reference voltage provided externally. Bypass this pin to ground with a 470nF ceramic capacitor.

## Inductor L:

A proper inductor must be connected between the  $V_{IN}$  and the SW pin for the SY26501 stable operation. 2.2 $\mu$ H inductor value is strongly recommended.

## Layout Design:

The layout design of SY26501 is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC:  $C_{IN}$ ,  $C_{SIN}$ ,  $C_{OUT}$ , L.

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2)  $C_{IN}$  must be close to pins IN and SGND. The loop area formed by  $C_{OUT}$  and PGND must be minimized.
- 3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.
- 4) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source, it is desirable to add a pull down 1M $\Omega$  resistor between the EN and SGND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

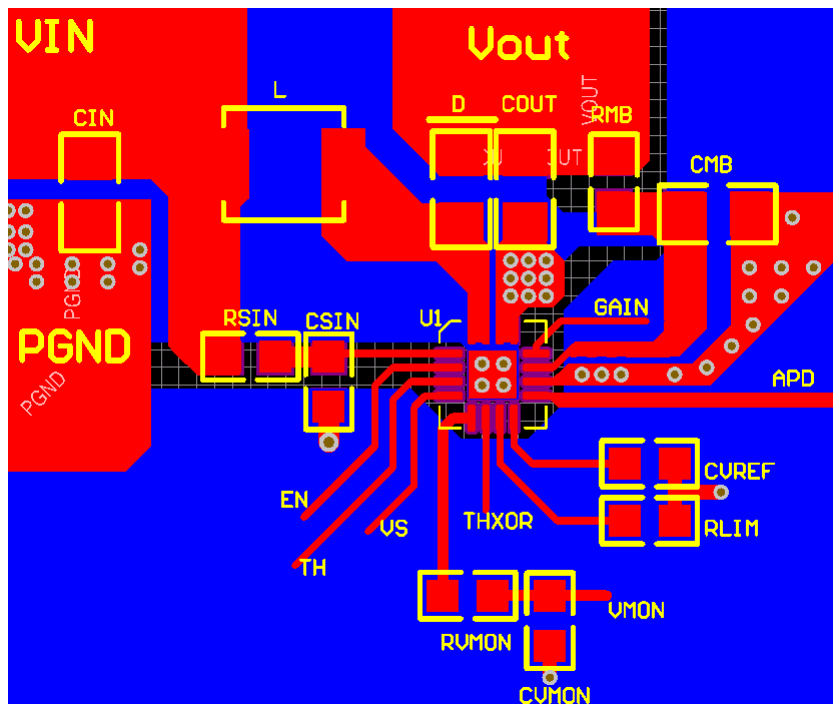
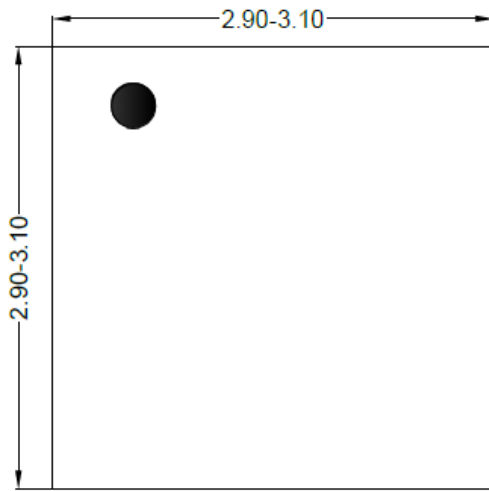
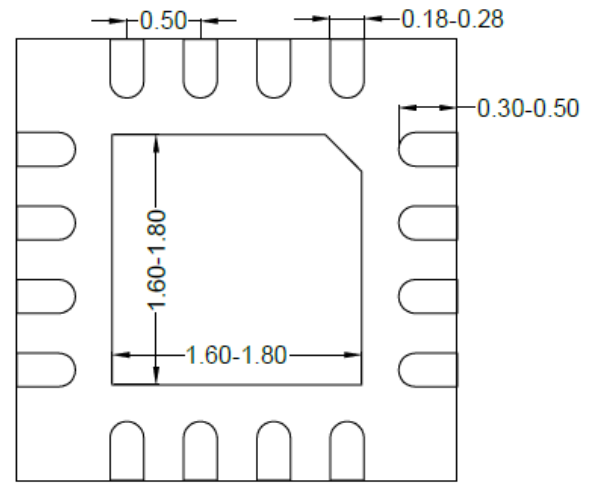


Figure6. PCB Layout Suggestion

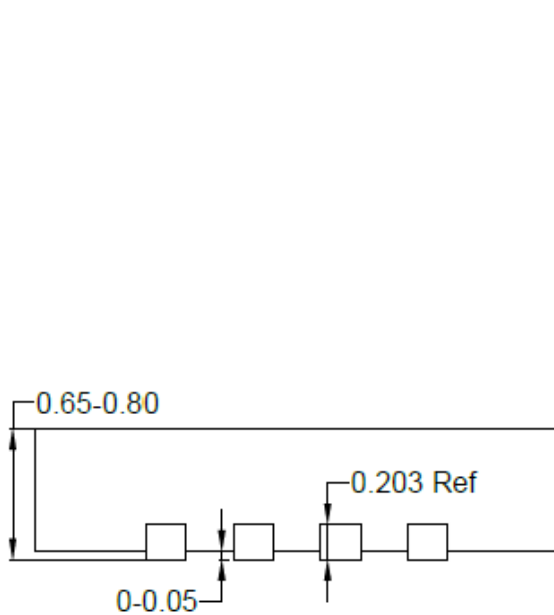
**QFN3×3-16 Package Outline Drawing**



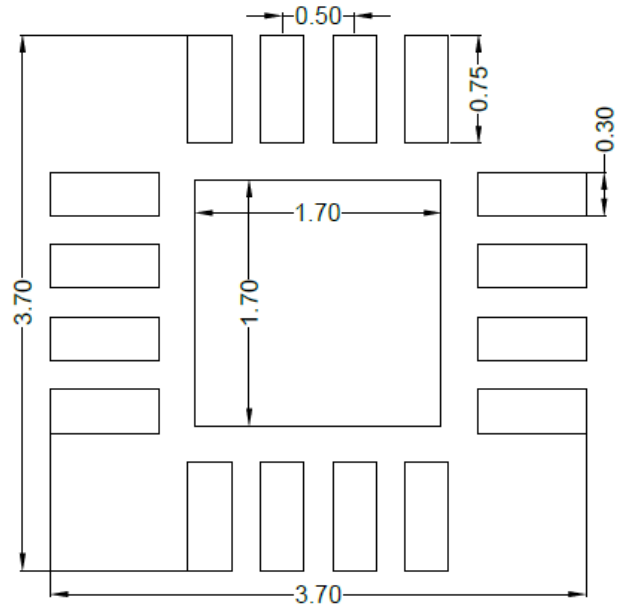
**Top View**



**Bottom View**



**Side View**

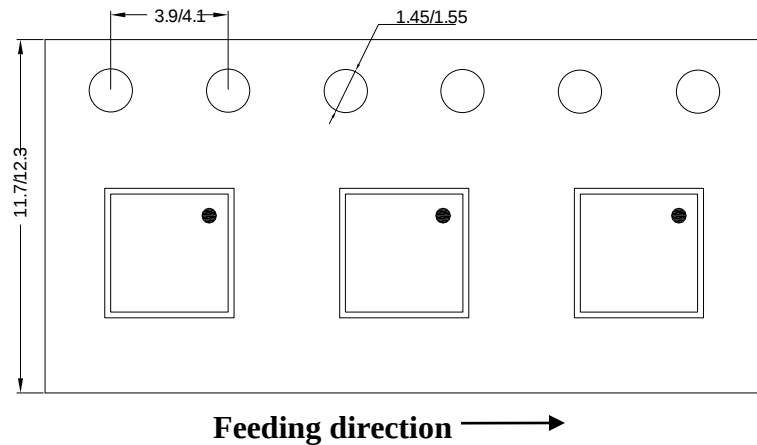


**PC B layout (Recommended)**

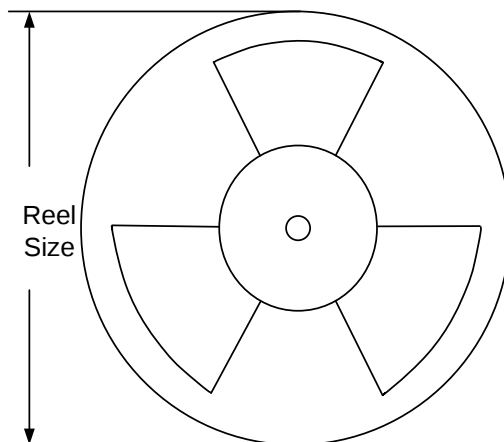
**Notes: All dimension in millimeter and exclude mold flash & metal burr.**

## Taping & Reel Specification

### 1. QFN3×3-16 Taping Orientation



### 2. Carrier Tape & Reel Specification for Packages



| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---------------|-----------------|------------------|------------------|--------------------|--------------------|--------------|
| QFN3×3        | 12              | 8                | 13"              | 400                | 400                | 5000         |

### 3. Others: NA



## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

| Date         | Revision     | Change          |
|--------------|--------------|-----------------|
| Apr.11, 2023 | Revision 0.9 | Initial Release |

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