SY21306

High Efficiency, 16V, 10A Synchronous Step Up Regulator

General Description

The SY21306 is a high efficiency, high power density synchronous boost regulator. The device uses adaptive constant off time and current mode control. The integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

The SY21306 provides selectable PFM/PWM light load operation mode. The device features cycle-by-cycle peak current limit. The low output voltage ripple, the small external inductor and the capacitor size are achieved at programmable pseudo-constant frequency.

The SY21306 is available in a compact QFN3×3-20 package.

Ordering Information

SY21306□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21306RAC	QFN3×3-20	--

Features

- Input Voltage Range: 2.8-16V
- Programmable Pseudo-constant Frequency: 300kHz-2MHz
- Low $R_{DS(ON)}$ for Internal Switch
  - ✓ Main FET: 10mΩ
  - ✓ Rectifier FET: 20mΩ
- PFM/PWM Selectable Light Load Operation Mode
- Internal Loop Compensation
- Programmable Peak Current Limit
- Internal Soft-start Time Limit the Inrush Current
- Input Voltage UVLO
- Over Temperature Protection
- Over Voltage Protection
- RoHS Compliant and Halogen Free
- Compact Package:QFN3×3-20

Applications

- Power Bank
- High Power AP
- E-cigarette
- Bluetooth Speaker

Typical Application

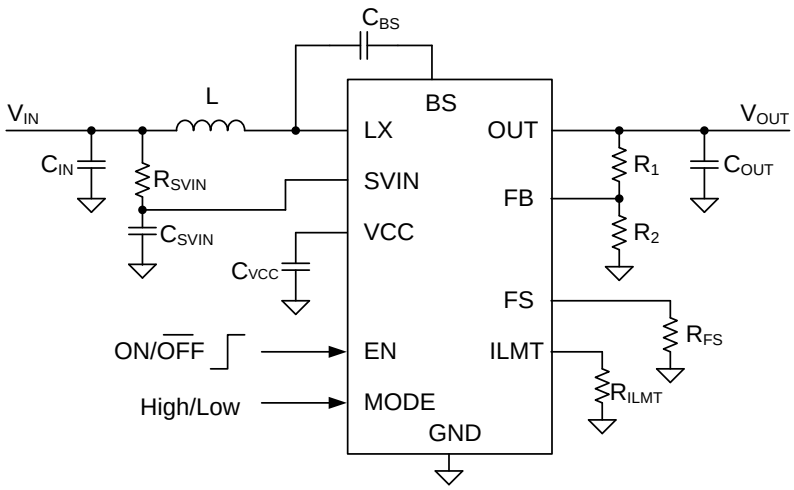

Figure1. Schematic Diagram

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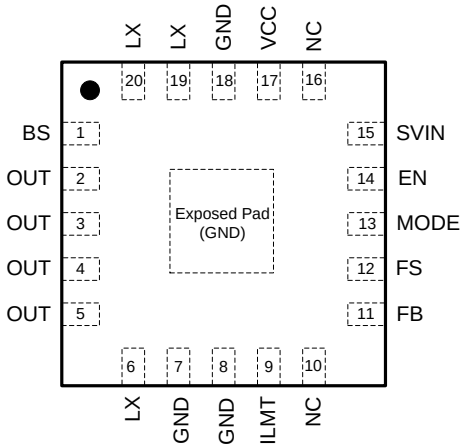
Pinout (top view)



(QFN3×3-20**)**

Top Mark: BMF*xyz* (device code: BMF, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
BS	1	Bootstrap pin. Supply rectifier FET's gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
OUT	2,3,4,5	The boost converter output pin.
LX	6,19,20	Inductor node. Connect an inductor from power input to the LX pin.
GND	7,8,18, EP	Ground pin of the IC.
ILMT	9	Switch peak current limit setting. Connect a resistor from this pin to GND. I_{LMT}(A)=1200/R_{ILMT}(kΩ)-2
NC	10,16	Not connected.
FB	11	Feedback pin. Connected to the center of the resistor voltage divider to program the output voltage: V_{OUT}=1V×(R_1/R_2+1)
FS	12	Switching frequency setting pin. Connect a resistor from this pin to ground to program the switching frequency. f_S(kHz) = 73565/R_{FS}(kΩ)+300
MODE	13	Operating mode selection under light load. Pull this pin low for PFM operation, and pull this pin high for PWM operation. Do not leave it floating.
EN	14	Enable control. Pull high to turn on the IC. Do not leave it floating.
SVIN	15	IC power supply input pin. Decouple this pin to the GND pin with a 1μF ceramic capacitor at least.
VCC	17	Output of the internal LDO regulator. Decouple this pin to the GND pin with a 1μF ceramic capacitor at least.

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Block Diagram

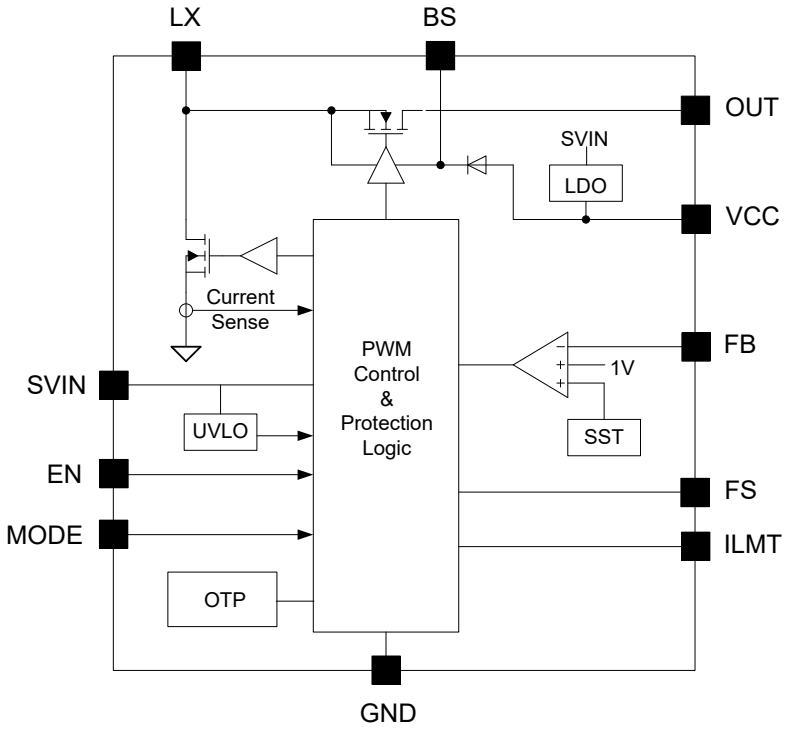

Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

SVIN, LX, OUT, ILMT, FS, MODE, EN ---------- -0.3V to 18V
FB, VCC ---------- -0.3V to 4V
BS-LX ---------- -0.3V to 4V
Dynamic LX Voltage in 10ns Duration ---------- -3.5V to 22V
Power Dissipation, P_D @ T_A = 25°C QFN3×3-20 ---------- 3.1W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 32°C/W
θ_{JC} ---------- 4°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

SVIN ---------- 2.8V to 16V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

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Electrical Characteristics

(V_{IN} =5V, V_{OUT}=12V, I_{OUT}=100mA, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{SVIN}		2.8		16	V
Quiescent Current	I_Q	FB=1.1 V		200	250	μA
Shutdown Current	I_{SHDN}	EN=0		1.5	3.5	μA
FB Leakage Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Main N-FET R_{ON}	$R_{DS(ON)_M}$			10		mΩ
Rectifier N-FET R_{ON}	$R_{DS(ON)_R}$			20		mΩ
Feedback Reference Voltage	V_{REF}		0.99	1	1.01	V
SVIN UVLO Rising Threshold	$V_{SVIN,UVLO}$				2.8	V
SVIN UVLO Hysteresis	$V_{SVIN,HYS}$			0.25		V
Output OVP Threshold	$V_{OUT,OVP}$		16	17	18	V
Main N-FET Current Limit	I_{LMT}	R_{ILMT}=100kΩ	8.5	10	11.5	A
Main N-FET Current Limit Program Range	$I_{LMT,RNG}$		2		10	A
ILMT Reference Voltage	V_{ILMT}			0.6		V
EN/MODE Input Voltage High	$V_{EN/MODE,H}$		1.2			V
EN/MODE Input Voltage Low	$V_{EN/MODE,L}$				0.4	V
Switching Frequency Program Range	$f_{SW,RNG}$		300		2000	kHz
Switching Frequency Accuracy	f_{SW}	R_{FS}=360kΩ	400	500	600	kHz
Minimum ON Time	$t_{ON,MIN}$			130		ns
Minimum OFF Time	$t_{OFF,MIN}$			120		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

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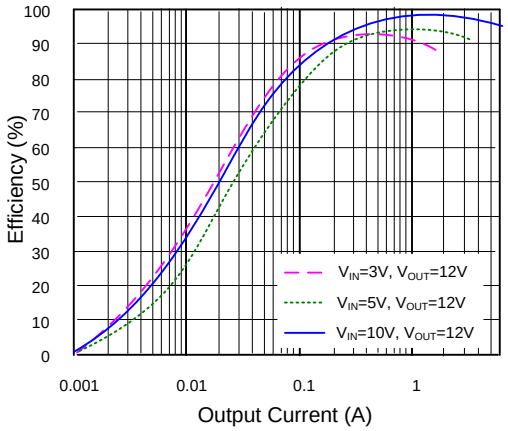
Typical Performance Characteristics

(f_{SW}=500kHz, T_A=25°C)

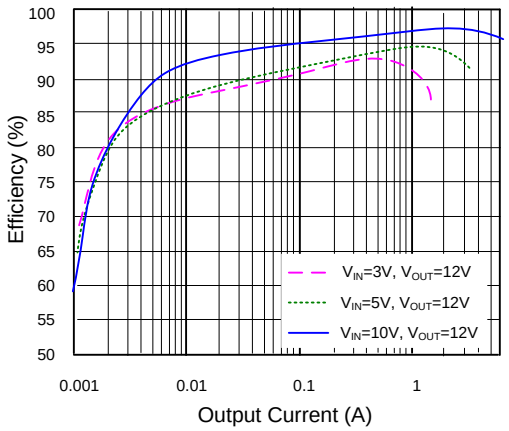
Efficiency vs. Load Current

Mode=high



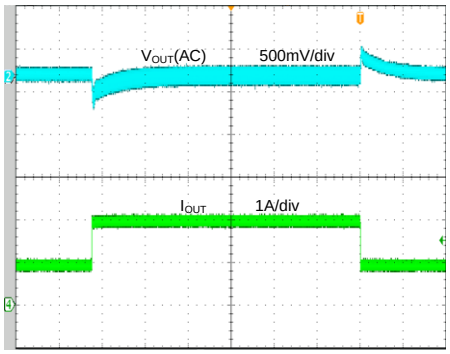
Efficiency vs. Load Current

Mode=low



Load Transient

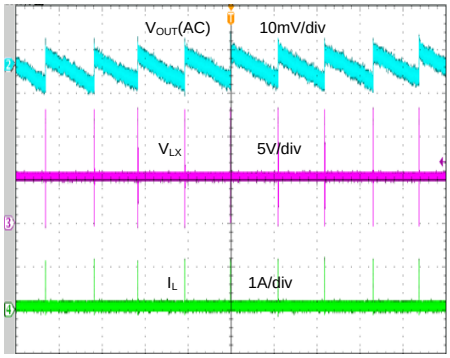
(V_{IN}=5V, V_{OUT}=12V, I_O=1 ~ 2A)



Time (200μs/div)

Output Ripple

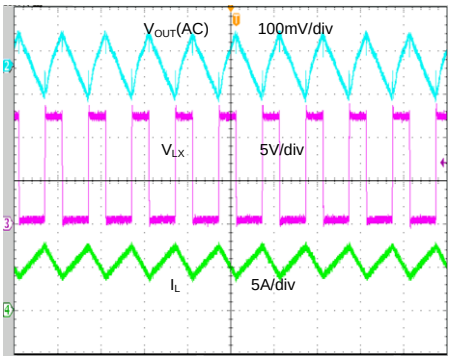
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



Time (800μs/div)

Output Ripple

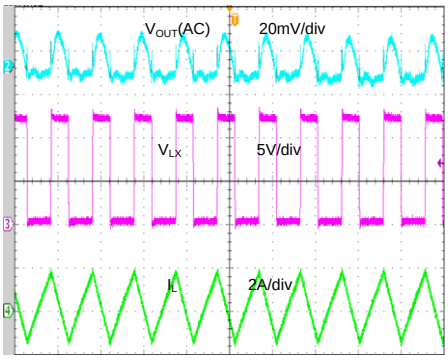
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (2μs/div)

Output Ripple

(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



Time (2μs/div)

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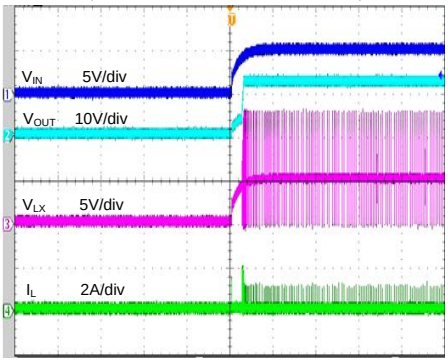
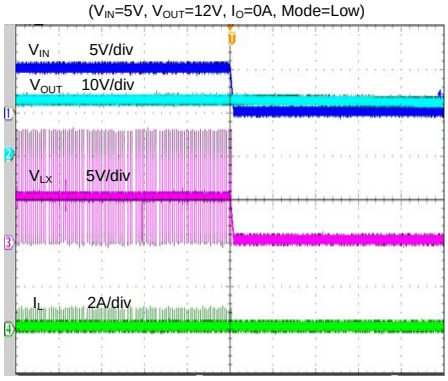
Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



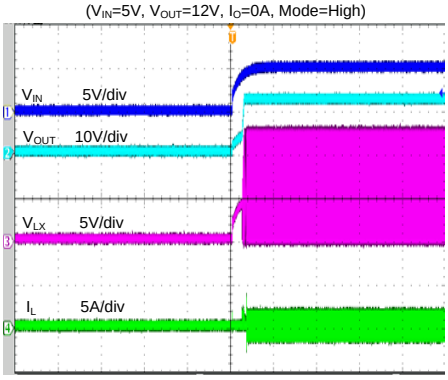
Time (20ms/div)

Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



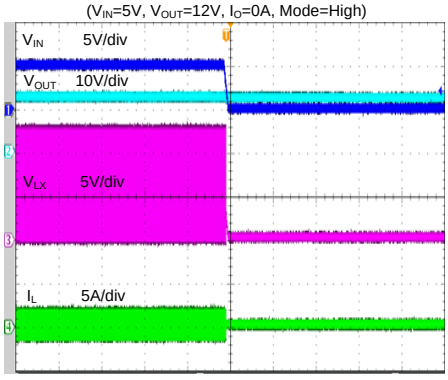
Time (20ms/div)

Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



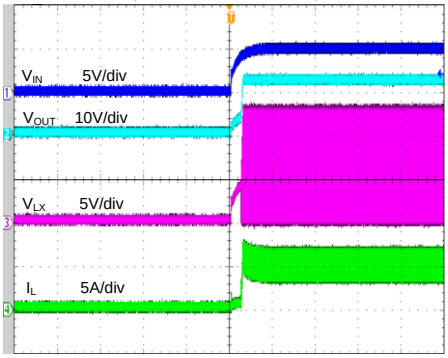
Time (20ms/div)

Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



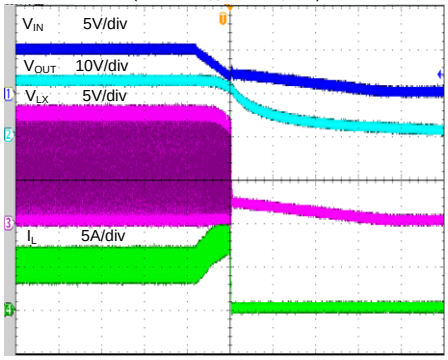
Time (10ms/div)

Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (20ms/div)

Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (200µs/div)

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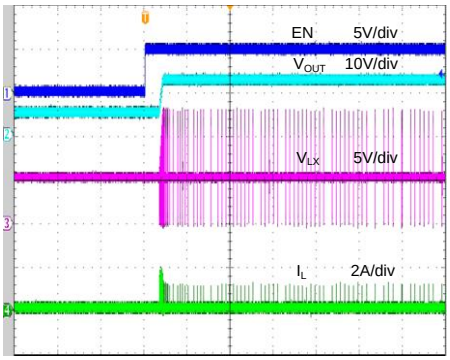
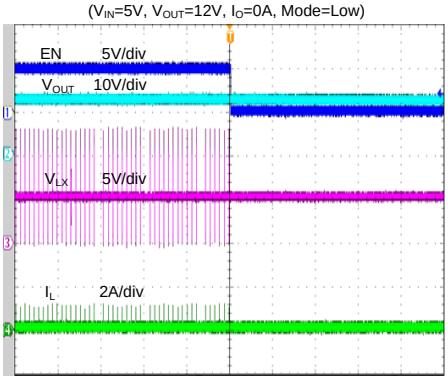
Startup from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



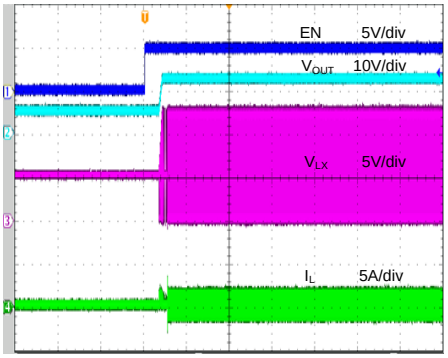
Time (10ms/div)

Shutdown from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



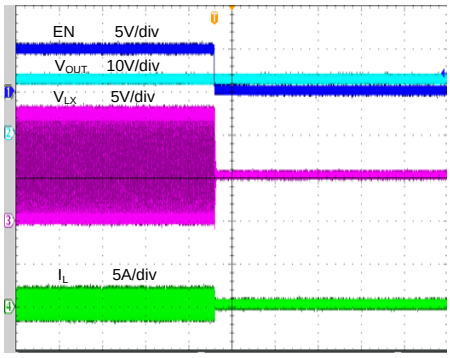
Time (10ms/div)

Startup from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



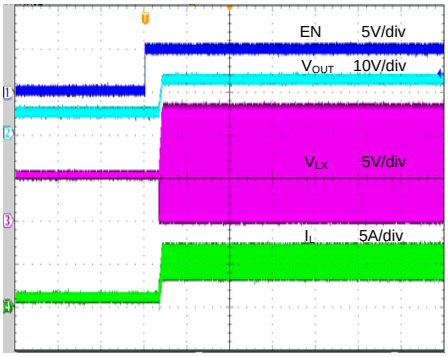
Time (10ms/div)

Shutdown from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



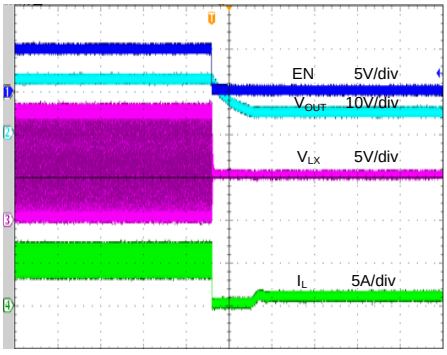
Time (10ms/div)

Startup from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (10ms/div)

Shutdown from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (200µs/div)

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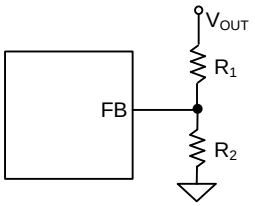
Applications Information

Because of the high integration in the SY21306, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the main FET current limit setting resistor R_{ILMT}, the switching frequency program resistor R_{FS}, the inductor L and the feedback resistors (R_1 and R_2) need to be selected for the targeted applications.

Feedback Resistor Divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value between 10k and 1M is recommended for both resistors. If R_1=200k is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{R_1}{V_{OUT} - 1}(\Omega)$$



Input Capacitor C_{IN}

The ripple current through the input capacitor is calculated as:

$$I_{CIN_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}(A)$$

To minimize the potential noise problem, place a typical X5R or a better grade ceramic capacitor really close to the VIN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, VIN, and the GND pin. In this case, a 10µF low ESR ceramic capacitor is recommended.

The SVIN capacitor must be close to the SVIN and GND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by C_{SVIN}, SVIN and the GND pin. In this case, a 1µF low ESR ceramic is recommended.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into account when selecting these capacitors. For the best performance, it is recommended to use X5R or a better grade ceramic capacitor with 25V rating and more than 44µF capacitors.

Boost Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT_MAX} \times 40\%}(H)$$

Where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

The SY21306 is less sensitive to the ripple current variations. Consequently, the final choice of the inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT_MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT_MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve good overall efficiency.

Switching Frequency

The switching frequency of the SY21306 in CCM can be programmed by adjusting the external resistor R_{FS} connected to the FS pin:

F_{SW} (kHz)= 73565/R_{FS}(kΩ) +300

Under PFM light load condition, the SY21306 will linearly fold back the frequency, thus minimize the output ripple.

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Enable Operation

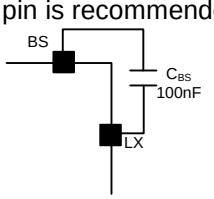
Pulling the EN pin low (<0.4V) will shut down the device. Driving the EN pin high (>1.2V) will turn on the IC again.

Light Load Operation Mode Selection

PFM or PWM light load operation is selected by the MODE pin. Pull MODE pin low (<0.4V) for PFM operation. Pull this pin high (>1.2V) for PWM operation.

External Bootstrap Capacitor

This capacitor provides the gate driver voltage for the internal rectifier. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.



Peak Current Limit Setting

The peak current limit can be programmed with a resistor R_{ILMT} connecting from the ILMT pin to ground: $I_{LIM}(A)=1200/R_{ILMT}(k\Omega)-2$

Layout Design

The layout design of the SY21306 is highly simplified. To achieve higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, C_{SVIN}, C_{VCC}, C_{OUT}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connected to the GND pin to achieve the better thermal performance and the noise immunity. If the board space allows, a designated ground plane layer will be highly recommended.

2) C_{SVIN} must be close to SVIN and GND pins. The loop area formed by C_{SVIN}, S_{VIN} and GND pins must be minimized.

3) C_{OUT} must be close to OUT and GND pins. The loop area formed by C_{OUT}, OUT and GND pins must be minimized.

4) The PCB copper area associated with the LX pin must be minimized to improve the noise immunity.

5) The components R_1 and R_2 and the trace connected to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB pin.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the SVIN pin is connected directly to a power source such as a Li-Ion battery, it will be desirable to add a pull down 1MΩ resistor across the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

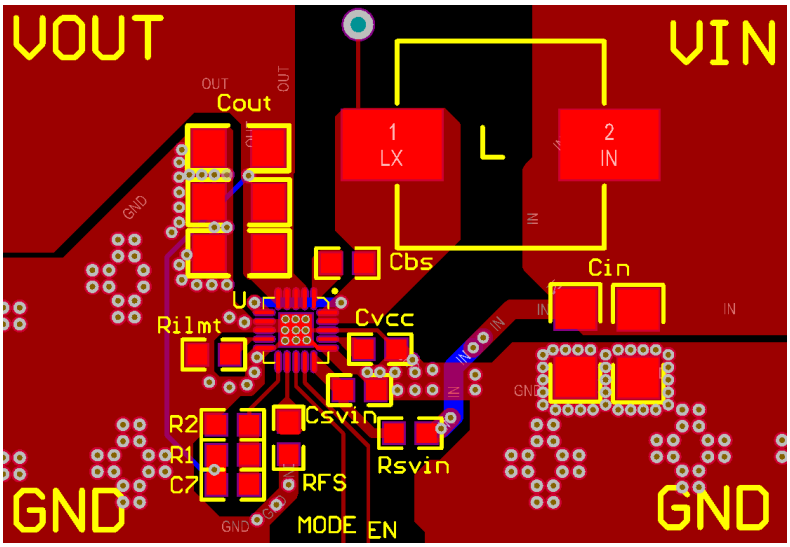


Figure3. PCB Layout Suggestion

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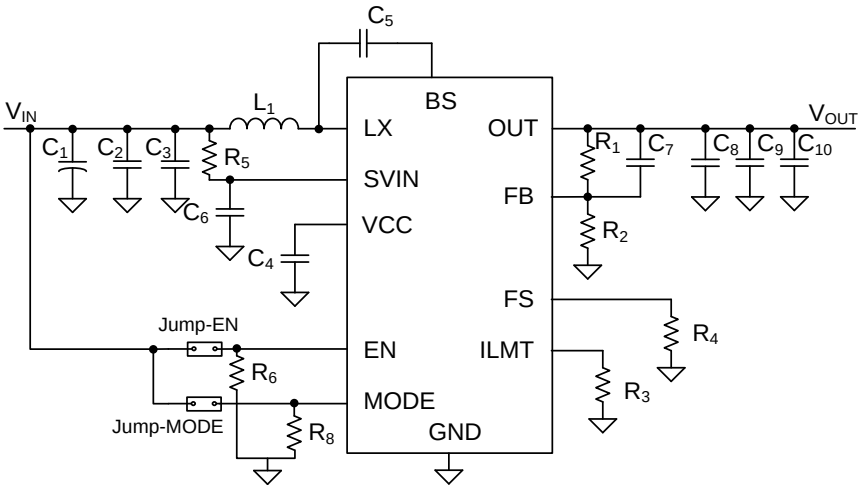
Schematic



BOM List

Designator	Description	Part Number	Manufacturer
C1	100µF/25V, Electrolytic Capacitor		
C2, C3	10µF/25V,1206	C3216X5R1E106KT	TDK
C4	2.2µF/16V,0603	C3216X7R1E225K	TDK
C5	100nF/50V,0603	C1608X7R1H104K	TDK
C6	4.7µF/25V,0603	C1608X5R1E475M	TDK
C8,C9,C10	22µF/16V,1206	C3216X5R1C226M	TDK
L1	2.2µH/18A	PCMB104T-2R2MS	CYNTEC
R1	110k , 1%,0603		
R2	10k , 1%, 0603		
R3	100k , 1%, 0603		
R4	300k		
R5	10ohm, 1%, 0603		
R6,R8	1MΩ, 1%, 0603		

Recommended Component Selection

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	L1(µH)
12	110	10	2.2
9	80.6	10	1.5
5	80.6	20	0.68

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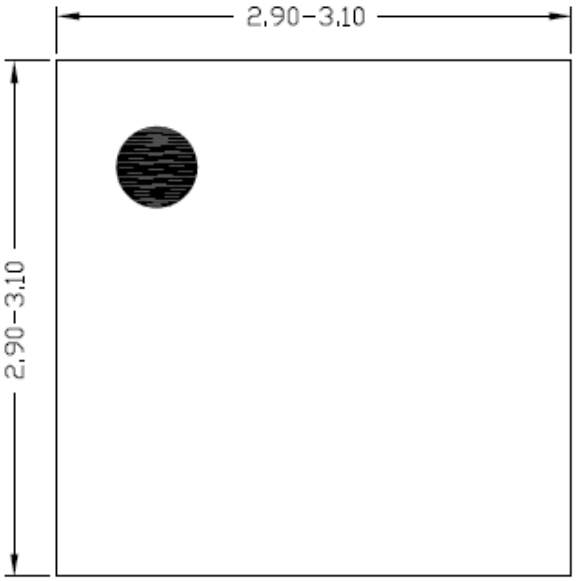
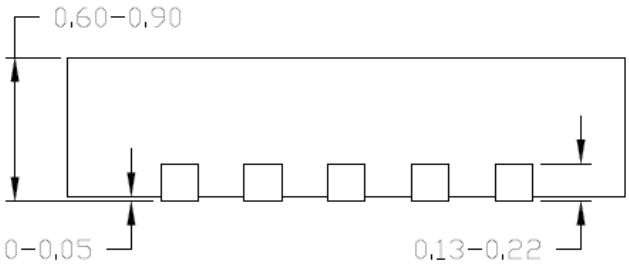
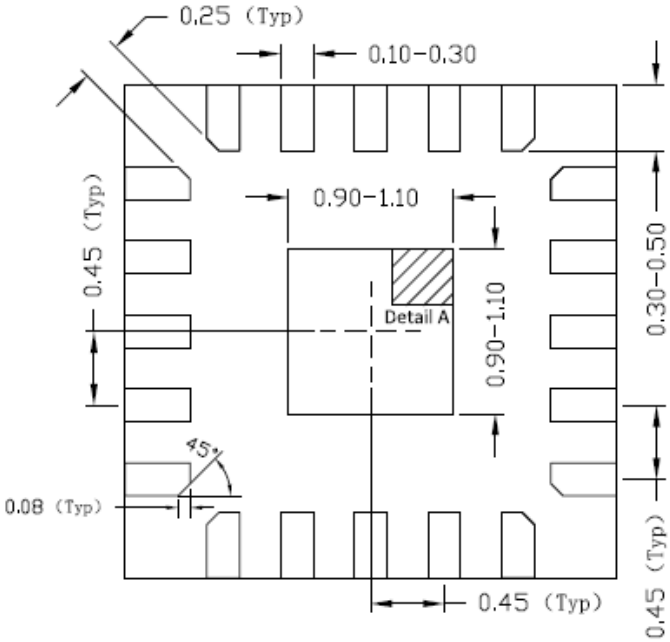
QFN3×3-20 Package Outline



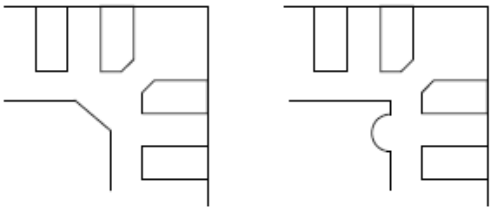
Top view



Side view



Bottom view



Detail A
Pin1 Identifier: two options

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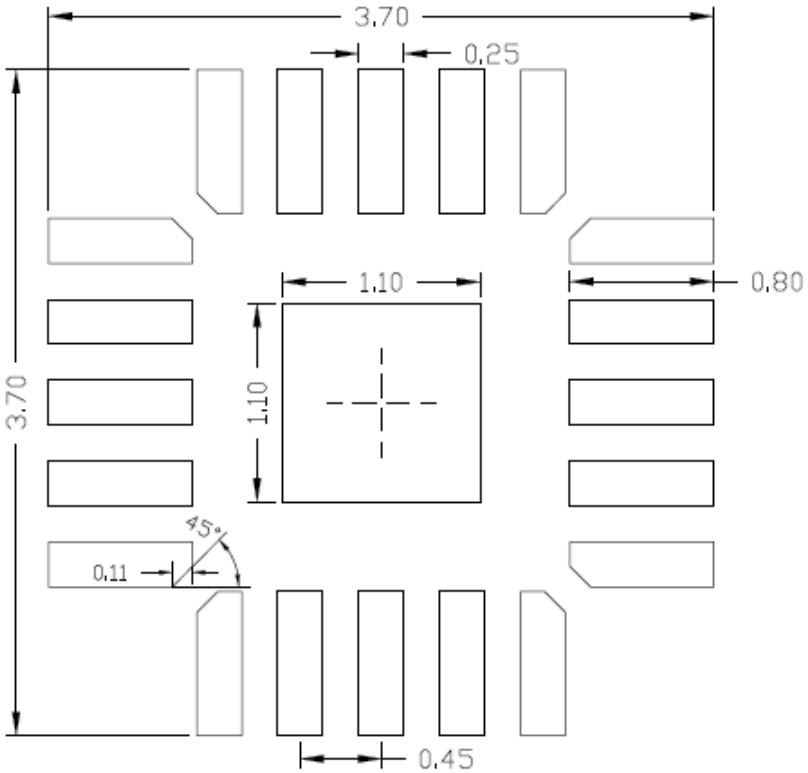

Recommended PCB layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

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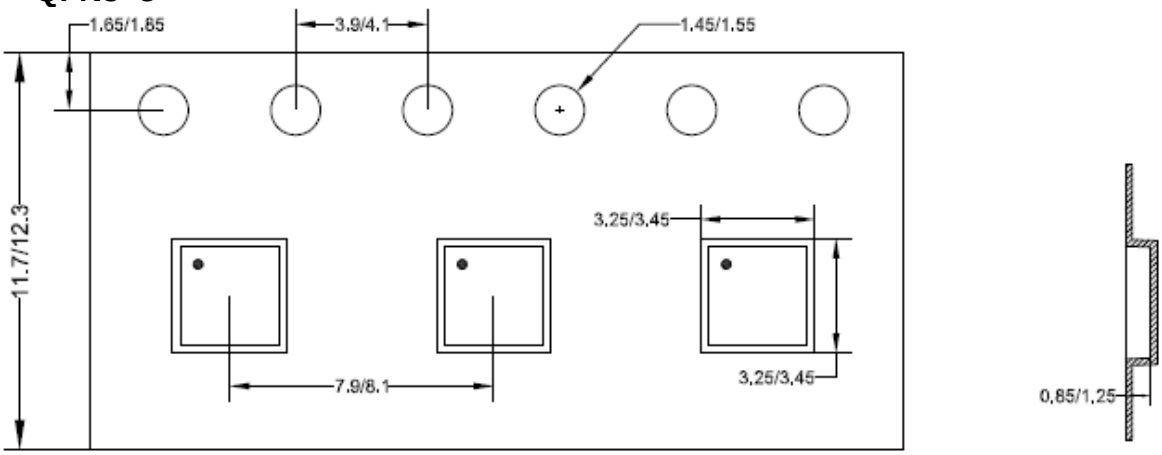
Taping & Reel Specification

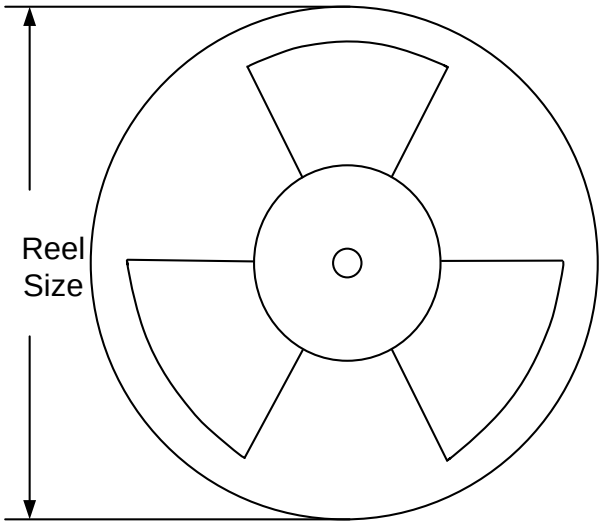
1. Taping orientation

QFN3×3



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.02,2024	Revision 1.0	Language improvements for clarity.
June 30, 2020	Revision 0.9B	Update the pin description of the MODE pin.
Feb. 22, 2019	Revision 0.9A	Update the formula of saturation current of the inductor in page 8
Sep.04, 2018	Revision 0.9	Initial Release

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