

0.85V Minimum Input and 5.5V Maximum Output High Efficiency 0.6A Valley Current Synchronous Boost

General Description

The SY20492D is a high efficient, synchronous, step-up Boost converter designed for one-cell Li-Ion or Li-polymer, or a two to three-cell alkaline Ni-Cd or Ni-MH battery powered applications. It can convert down to 0.85V input voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch.

The SY20492D can disconnect the output from input during the shutdown mode. When input voltage exceeds the regulated output voltage, the SY20492D enters bypass mode automatically.

Features

- 0.85V Minimum Input Voltage
- Adjustable Output Voltage from 1.8V to 5.5V
- Min 0.6A Valley Current Limit
- 5 μ A Typical Quiescent Current
- Load Disconnect During Shutdown
- Low $R_{DS(ON)}$ (Main Switch/Synchronous Switch) at 3.3V Output: 100/170m Ω
- Output OVP
- RoHS Compliant and Halogen Free
- Auto Bypass Mode When $V_{IN} \geq V_{OUT}$
- Compact Package SOT23-6

Ordering Information

SY20492□(□□)□
 └─ Temperature Code
 └─ Package Code
 └─ Optional Spec Code

Ordering Number	Package type	Note
SY20492DABC	SOT23-6	----

Applications

- All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment

Typical Applications

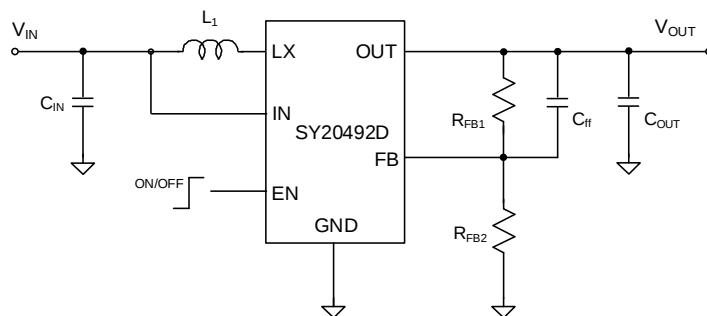


Figure 1. Schematic Diagram

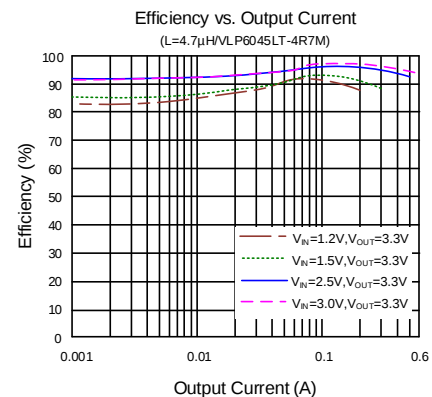
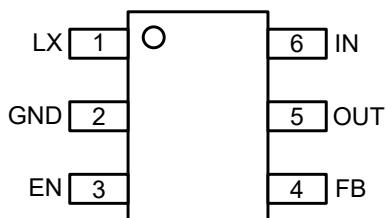


Figure 2. Efficiency vs. Output Current

Pinout (top view)



(SOT23-6)

Top mark: **N4xyz for SY20492DABC** (Device code: N4, x=*year code*, y=*week code*, z= *lot number code*)

Pin Name	Pin Number	Pin Description
LX	1	Inductor node. Connect an inductor between the IN pin and the LX pin.
GND	2	Ground pin.
EN	3	Enable pin. Pull high to turn on. Do not leave it floating.
FB	4	Feedback pin. Connect a resistor R_{FB1} between OUT and FB, and a resistor R_{FB2} between FB and GND to program the output voltage. $V_{OUT}=0.5V \times (R_{FB1}/R_{FB2}+1)$.
OUT	5	Output pin. Decouple this pin to the GND pin with a minimum of 10 μ F ceramic capacitor.
IN	6	Input pin.

Block Diagram

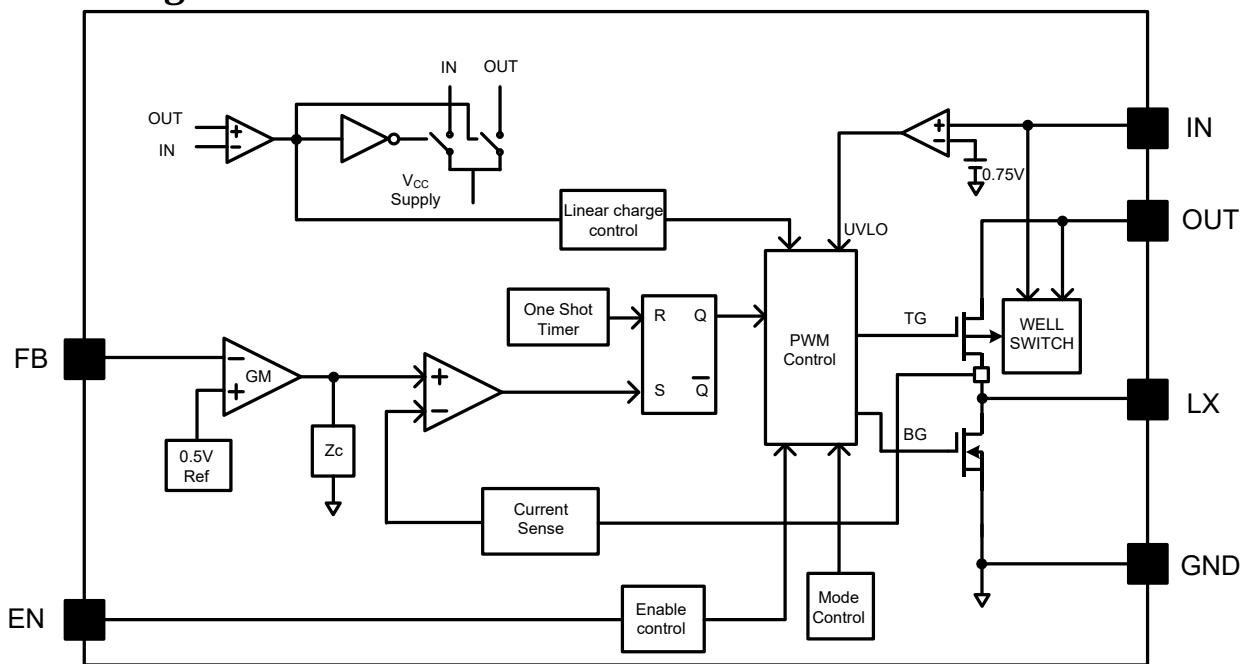


Figure3. Block Diagram



SILERGY

SY20492D

Absolute Maximum Ratings (Note 1)

FB, IN, OUT, EN ----- -0.3V to 6.0V

LX ----- -0.3V^{(*)1} to 6.0V^{(*)2}

Power Dissipation, P_D@ T_A=25°C SOT23-6----- 1W

Package Thermal Resistance (Note 2)

θ_{JA} ----- 100°C/W

θ_{JC} ----- 30°C/W

Junction Temperature Range ----- -40°C to 150°C

Lead Temperature (Soldering, 10 sec.) ----- 260°C

Storage Temperature Range ----- -65°C to 150°C

(*)1 LX Voltage tested down to -3V< 20ns

(*)2 LX Voltage tested up to +7V< 20ns

Recommended Operating Conditions (Note 3)

IN ----- 0.85V to 5.5V

OUT----- 1.8V to 5.5V

Junction Temperature Range ----- -40°C to 125°C

Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

($V_{IN}=2.4V$, $V_{OUT}=3.3V$, $I_{OUT}=300mA$, $T_A = 25^{\circ}C$, unless otherwise specified)

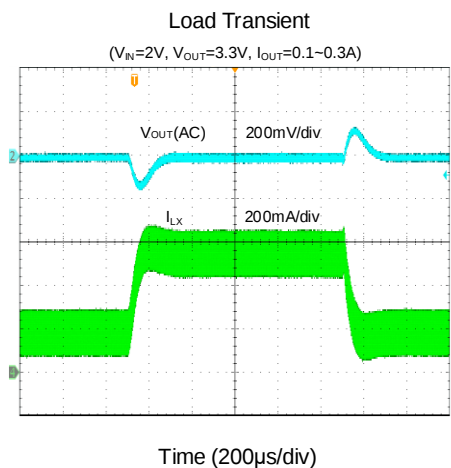
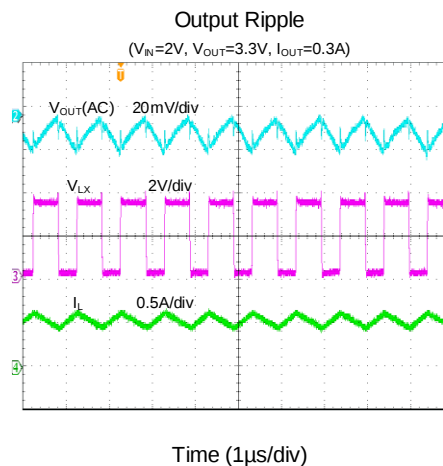
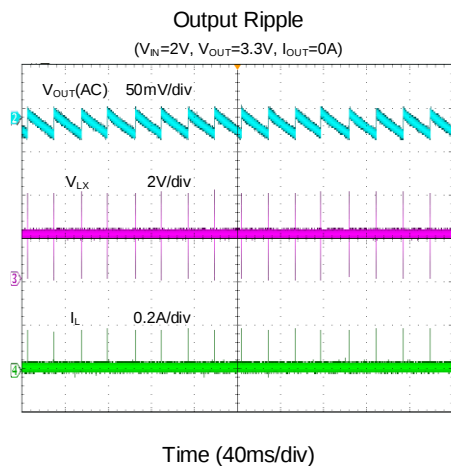
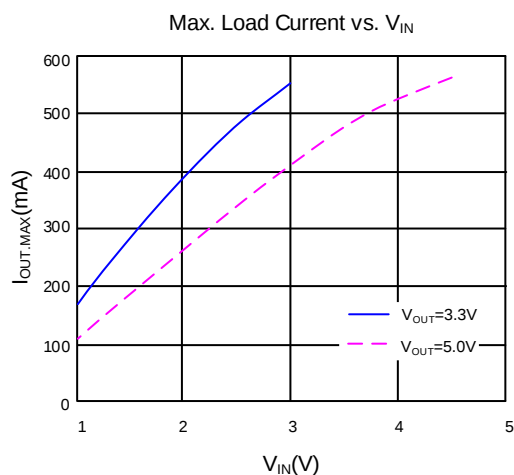
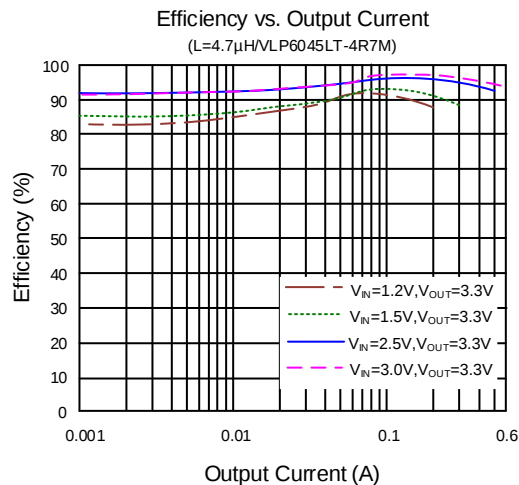
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		0.85		5.5	V
Input UVLO Threshold	V_{UVLO}			0.7	0.85	V
Input UVLO Hysteresis	V_{HYS}			0.04		V
Quiescent Current	V_{IN}	$V_{FB}=1.3V, V_{EN}=V_{IN}=1V$, $V_{OUT}=3.4V$		0.7		μA
	V_{OUT}			5		μA
Shutdown Current	I_{SHDN}	$V_{EN}=0V, V_{IN}=2.4V$		0.1	1	μA
Linear Charge Current	I_{CHARGE}	$V_{OUT}<0.5V_{IN}$		0.3		A
Feedback Reference Voltage	V_{REF}		0.4925	0.5	0.5075	V
Low Side Main FET R_{ON}	$R_{DS(ON)1}$			100		$m\Omega$
Synchronous FET R_{ON}	$R_{DS(ON)2}$			170		$m\Omega$
EN Input Voltage High	$V_{EN,H}$	$V_{IN}\leq 1.6V$ and $V_{OUT}\leq 1.6V$	0.7			V
		$V_{IN}>1.6V$ or $V_{OUT}>1.6V$	1.2			V
EN Input Voltage Low	$V_{EN,L}$	$V_{IN}\leq 1.6V$ and $V_{OUT}\leq 1.6V$			0.25	V
		$V_{IN}>1.6V$ or $V_{OUT}>1.6V$			0.4	V
EN Leakage Current	$I_{EN,LK}$	$V_{EN}=3.3V$	-1		1	μA
Min ON Time	$t_{ON,MIN}$			60		ns
Min OFF Time	$t_{OFF,MIN}$			140		ns
Soft-start Time	t_{SS}			1		ms
Switching Frequency	f_{SW}	$V_{OUT}=3.3V$, CCM		1		MHz
Valley FET Current Limit	$I_{LMT,VAL}$		0.6			A
Output Over Voltage Threshold	V_{OVP}			5.8		V
Output Over Voltage Hysteresis	$V_{OVP,HYS}$			0.3		V
Thermal Shutdown Temperature	T_{SD}			150		$^{\circ}C$
Thermal Shutdown Hysteresis	T_{HYS}			20		$^{\circ}C$

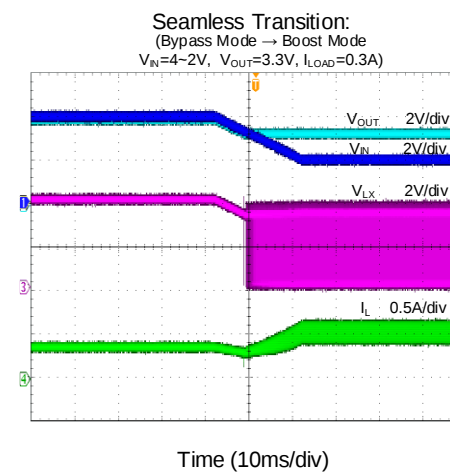
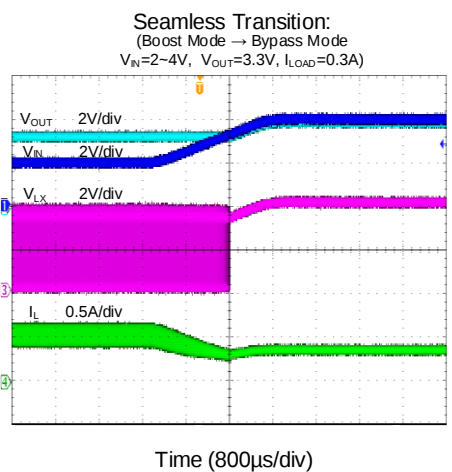
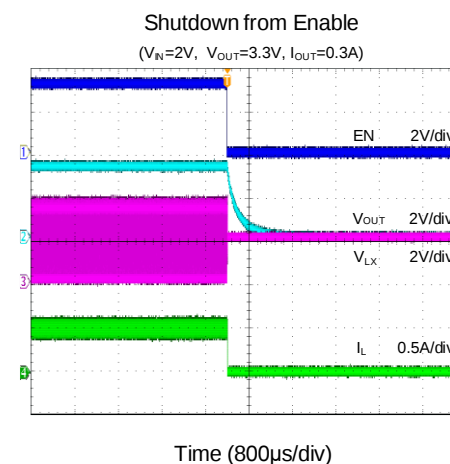
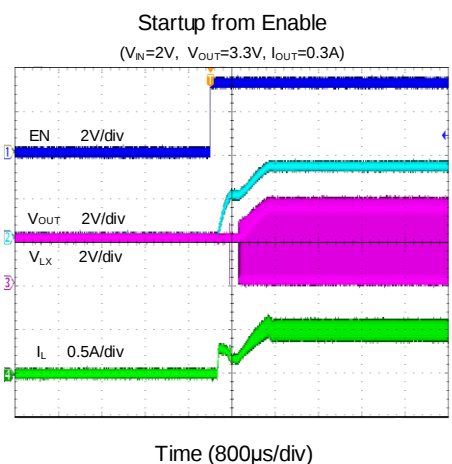
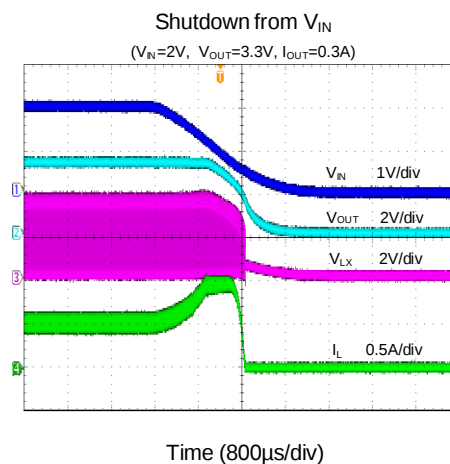
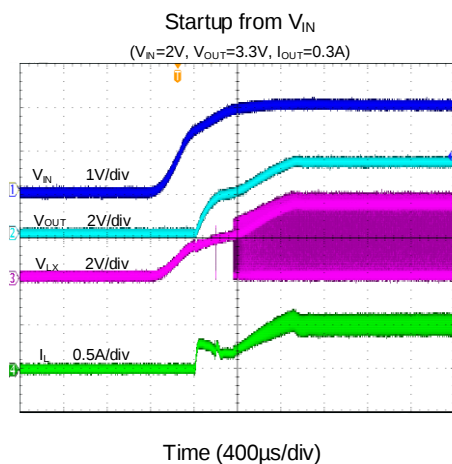
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

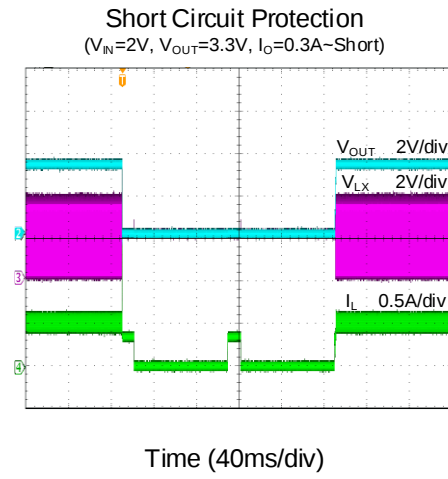
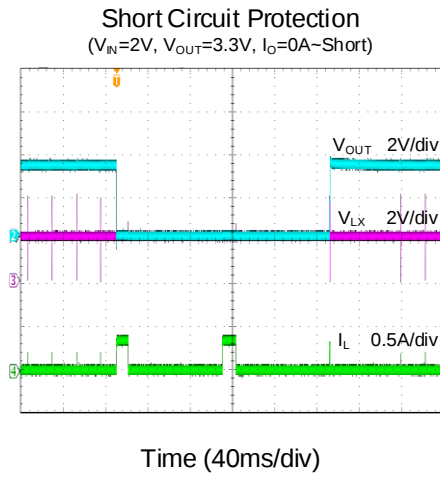
Note 2: Package thermal resistance is measured in the natural convection at $T_A = 25^{\circ}C$ on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics







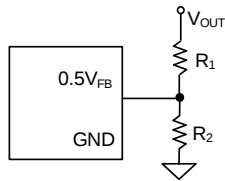
Applications Information

Because of the high integration in the SY20492D, the application circuit based on this regulator is rather simple. Only input capacitor C_{IN} , output capacitor C_{OUT} , inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2 :

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2 . A value of between 100k and 1M is recommended for both resistors. If V_{OUT} is 3.3V, $R_1=510k$ is chosen, using following equation, then R_2 can be calculated to be 91k:

$$R_2 = \frac{0.5V}{V_{OUT} - 0.5V} R_1 (\Omega)$$



Input Capacitor C_{IN} :

The ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L \times f_{SW} \times V_{OUT}} (A)$$

To minimize the potential noise problem, a typical X5R or a better grade ceramic capacitor should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} , and IN/GND pins. In this case, a 22 μ F low ESR ceramic capacitor is recommended.

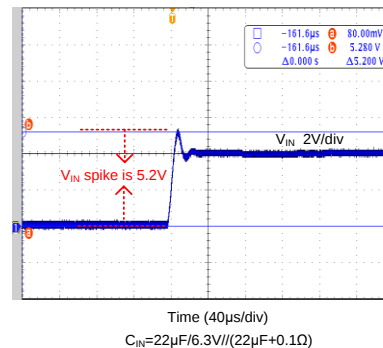
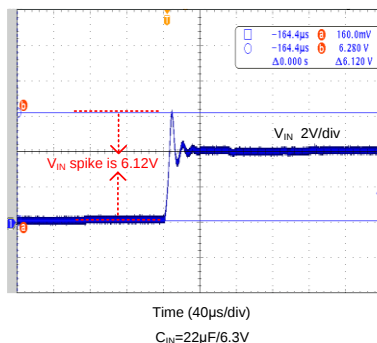
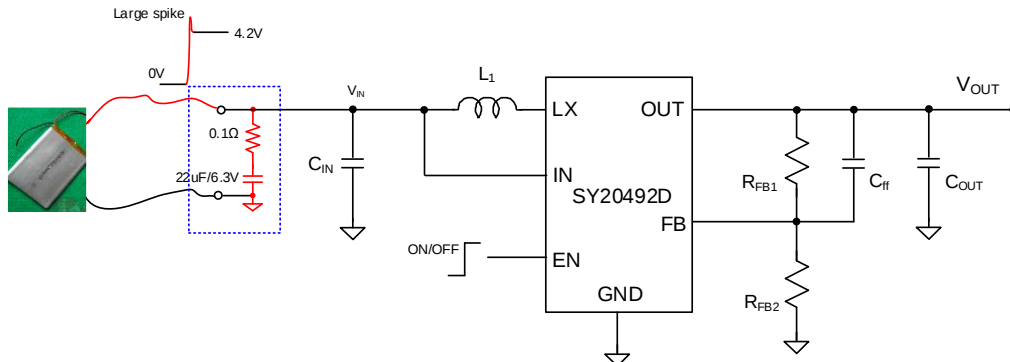
Output Capacitor C_{OUT} :

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or a better grade ceramic capacitor with 6.3V rating and greater than 22 μ F capacitance.

Li-Ion Battery Hot Plug Consideration:

In the mass production stage, the Li-Ion Battery will always hot plug in between IC IN and GND pin. The hot plug may lead to large voltage spike and even lead to IC EOS fail. To avoid this potential risk, 1pcs 22 μ F ceramic cap serial with 0.1 Ω resistor is recommended to absorb the input voltage spike.

With the recommended input absorb solution, the voltage spike can be reduced from 6.12V to 5.2V.



Output Inductor L:

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}} \right)^2 \frac{(V_{OUT} - V_{IN})}{f_{SW} \times I_{OUT_MAX} \times 40\%} (H)$$

Where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

The SY20492D is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT_MIN} > \left(\frac{V_{OUT}}{V_{IN}} \right) \times I_{OUT_MAX} + \frac{V_{IN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with $DCR < 50m\Omega$ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low ($< 0.4V$) will shut down the device. During shutdown mode, the SY20492D shutdown current drops to lower than $1\mu A$, driving the EN pin high ($> 1.2V$) will turn on the IC again.

Layout Design:

The layout design of SY20492D is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN} , L , R_1 and R_2 .

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2) C_{IN} must be close to the Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.
- 3) C_{OUT} must be close to the Pins OUT and GND. The loop area formed by C_{OUT} and GND must be minimized.
- 4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 5) The components R_1 and R_2 , and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.
- 6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down $1M\Omega$ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

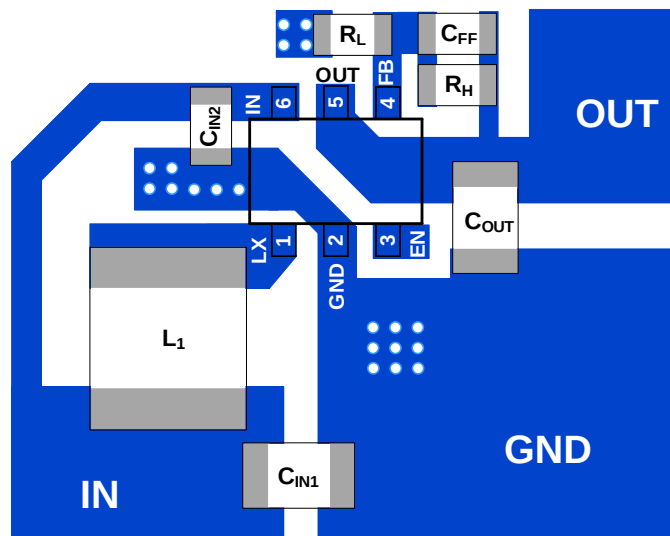
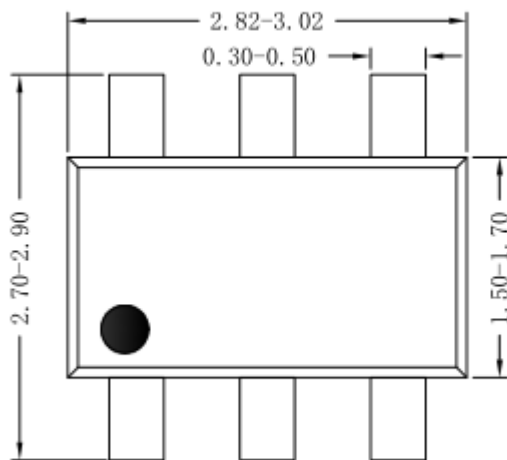
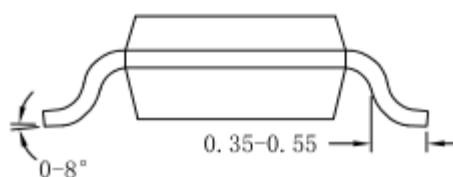


Figure4. PCB Layout Suggestion

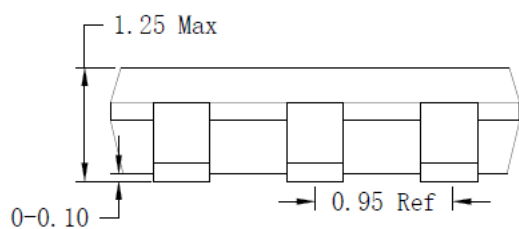
SOT23-6 Package Outline & PCB Layout Design



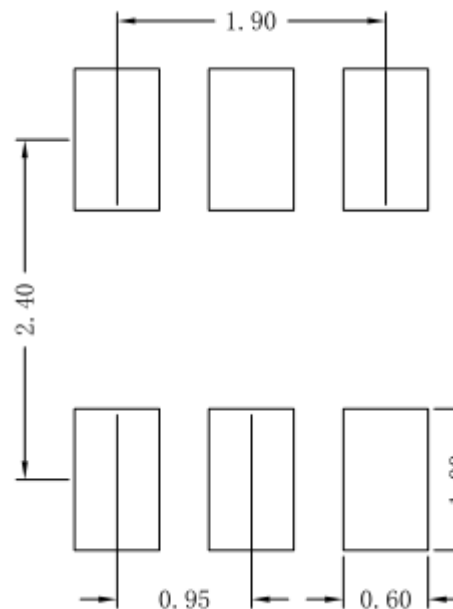
Top View



Side View



Side View

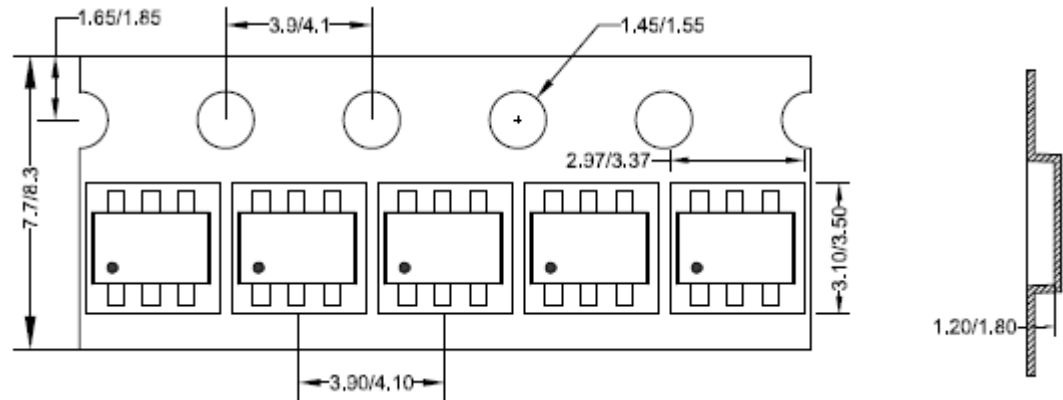


Recommended Pad Layout

Notes: All dimension in millimeter and exclude mold flash & metal burr.

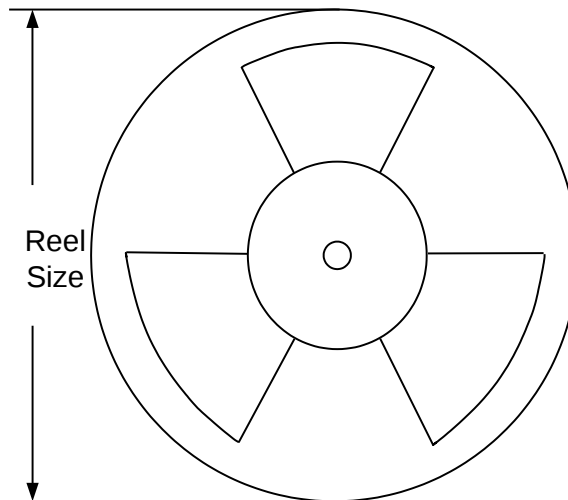
Taping & Reel Specification

1. Taping orientation for packages (SOT23-6)



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Aug. 25, 2022	Revision 0.9B	Fix a typo in “Feedback Resistor Dividers R_1 and R_2 ” information (page8) -- Feedback Reference Voltage is 0.5V,(not 1.2V), consistent with the data in the EC table
Nov.25, 2021	Revision 0.9A	Update the package outline (The package thickness changes from 1.30Max to 1.25Max.)
May.14, 2021	Revision 0.9	Initial Release

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