General Description

The SY20489C is a high efficiency synchronous, step-up Boost converter designed for one-cell Li-Ion or Li-polymer, or a two to three-cell alkaline Ni-Cd or Ni-MH battery powered applications. It can convert down to 2.5V input voltage and up to 5.6V output voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch.

The SY20489C can disconnect the output from input during the shutdown mode. When input voltage exceeds the regulated output voltage, the SY20489C enters bypass mode automatically.

Features

- 2.5V Minimum Input Voltage
- Adjustable Output Voltage from 2.5V to 5.6V
- Min 3A Valley Current Limit
- Capable for Seamless Transition between Boost and Bypass Mode
- Load Disconnect During Shutdown
- Low $R_{DS(ON)}$ (Main Switch/Synchronous Switch) at 5.0V Output: 70mΩ/100mΩ
- Output OVP Protection
- RoHS Compliant and Halogen Free
- Compact package CSP1.54×0.9-6

Ordering Information

SY20489 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20489CUMC	CSP1.54×0.9-6	

Applications

- All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment.

Typical Applications

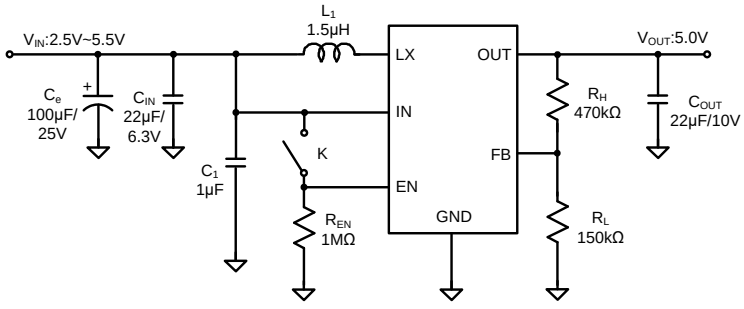


Figure 1. Schematic Diagram

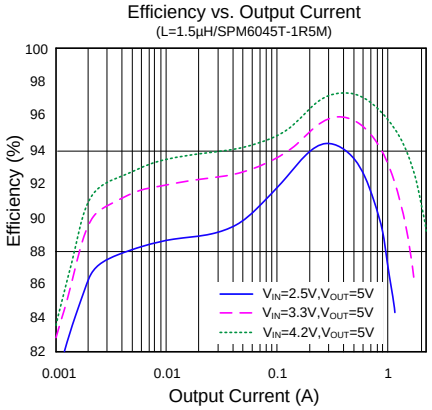
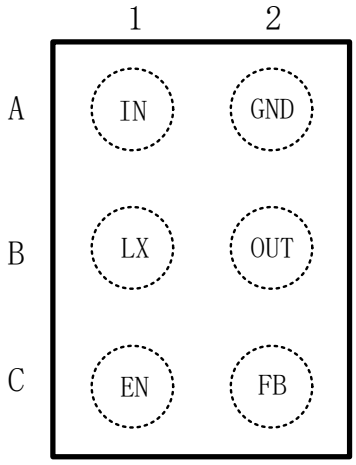


Figure2. Efficiency vs. Output Current

Pinout (top view)



(CSP1.54×0.9-6)

Top mark: **K5*xyz*** for (Device code: K5, ***x=year code, y=week code, z= lot number code***)

Name	Pin Number	Description
IN	A1	Signal input pin. Decouple this pin to the GND pin with at least a 1μF ceramic capacitor for noise immunity consideration.
LX	B1	Inductor node. Connect an inductor between the IN pin and the LX pin.
EN	C1	Enable pin. Pull high to turn on. Do not leave it floating.
GND	A2	Ground pin.
OUT	B2	Output pin. Decouple this pin to GND pin with at least a 22μF ceramic capacitor.
FB	C2	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=1.2× (1+R_H/R_L).

Block Diagram

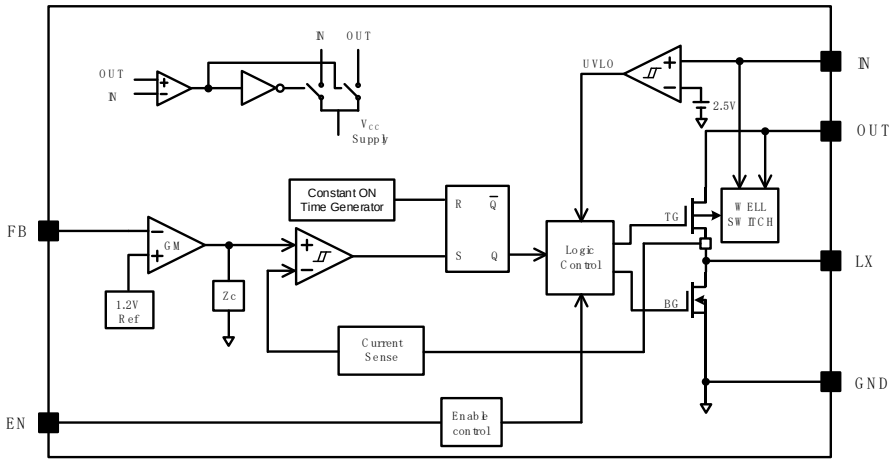


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

All Pins ---------- 6.0V
Power Dissipation, P_D@ T_A=25°C, CSP1.54×0.9-6----------1.35 W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 74°C/W
θ_{JC} ---------- 2°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- 65°C to 150°C

Recommended Operating Conditions (Note 3)

IN ---------- 2.5V to 5.5V
OUT---------- 2.5V to 5.6V
EN, FB ---------- 0V to V_{OUT}+0.3V
All other pins ---------- 0-5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =3.0V, V_{OUT}=5.0V, I_{OUT}=500mA, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		2.5		5.5	V
Output Voltage Range		V_{OUT}		2.5		5.6	V
Quiescent Current	V_{IN}	I_Q	Io=0A,V_{EN}=V_{IN}=3.0V,		8		μA
	V_{OUT}		V_{OUT}=5.0V,V_{FB}=105%V_{REF}		32		μA
Shutdown Current		I_{SHDN}	V_{EN}=0V, V_{IN}=3.0V		0.1	1	μA
Linear Charge Current		I_{CHARGE}	V_{OUT}<0.5V_{IN}		1.5		A
Input Vin UVLO Threshold		V_{UVLO}				2.5	V
V_{IN} UVLO Hysteresis		V_{SYS}			0.1		V
EN Rising Threshold		V_{ENH}		1.2			V
EN Falling Threshold		V_{ENL}				0.4	V
EN Leakage Current		I_{EN}		-1		1	μA
Low Side Main FET R_{ON}		$R_{DS(ON)1}$	V_{OUT}=5.0V		70		mΩ
Synchronous FET R_{ON}		$R_{DS(ON)2}$	V_{OUT}=5.0V		100		mΩ
Synchronous FET Current Limit		I_{LIM}		3.0			A
Switching Frequency		Fsw			1.0		MHz
Feedback Reference Voltage		V_{REF}	T_A = 25°C	1.182	1.2	1.218	V
			T_A = 0~50°C	1.17	1.2	1.23	V
Minimum ON Time		t_{ON_MIN}			80		ns
Minimum OFF Time		t_{OFF_MIN}			80		ns
OUT Pin OVP Protection					6.0		V
OUT Pin OVP Hysteresis		OVP_{HYS}			0.25		V
Thermal Shutdown Temperature		T_{SD}			150		°C
Thermal Shutdown Hysteresis		T_{HYS}			20		°C

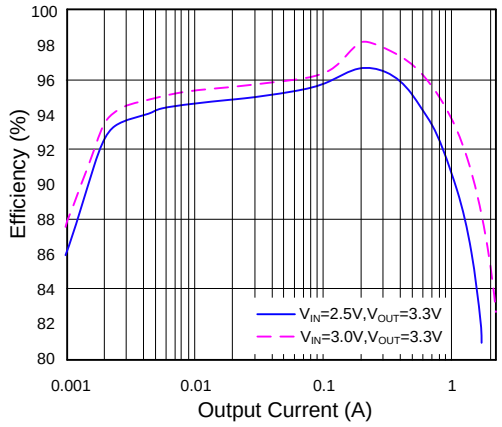
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

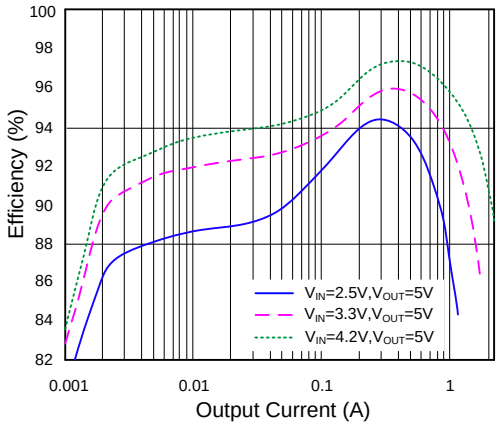
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

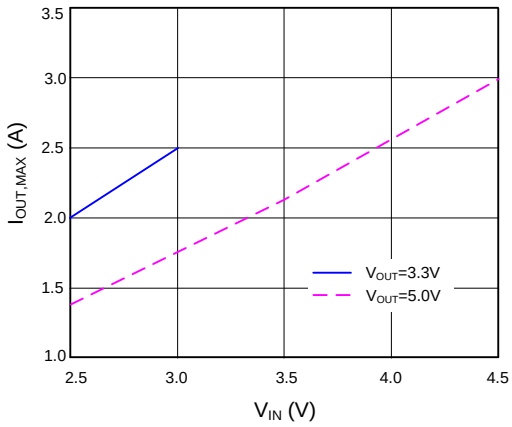
Efficiency vs. Output Current
(L=1.5μH/SPM6045T-1R5M)



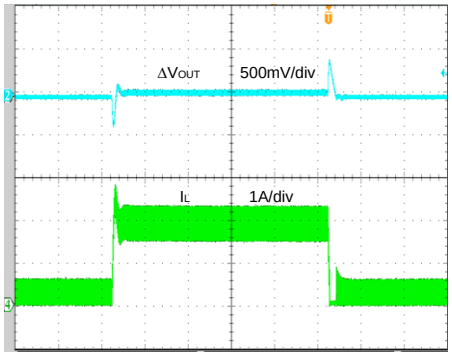
Efficiency vs. Output Current
(L=1.5μH/SPM6045T-1R5M)



Max Load Current vs. V_{IN}

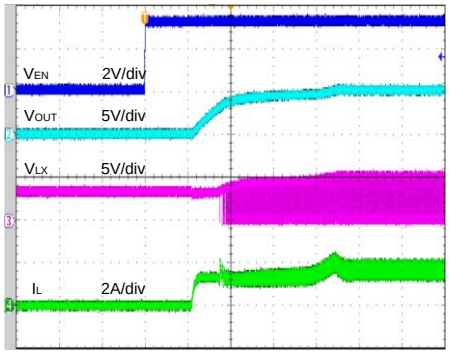


Load Transient
(V_{IN}=3.3V,V_{OUT}=5V,I_{OUT}=0.1A~1A)



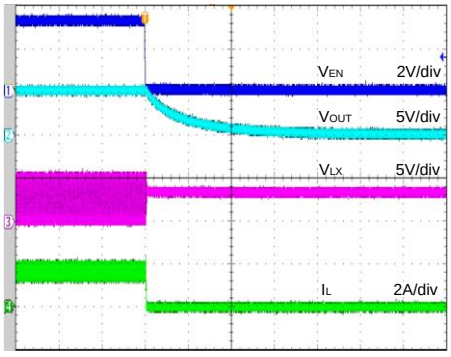
Time (400μs/div)

Startup from Enable
(V_{IN}=3.3V,V_{OUT}=5V,I_{OUT}=1A)



Time (100μs/div)

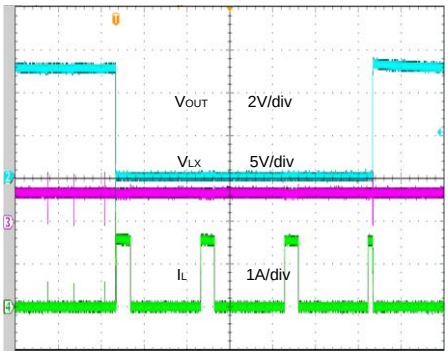
Shutdown from Enable
(V_{IN}=3.3V,V_{OUT}=5V,I_{OUT}=1A)



Time (100μs/div)

Short Circuit Protection

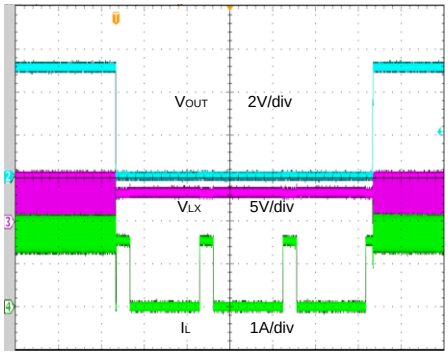
(V_{IN}=3.3V,V_{OUT}=5V,0A to Short)



Time (20ms/div)

Short Circuit Protection

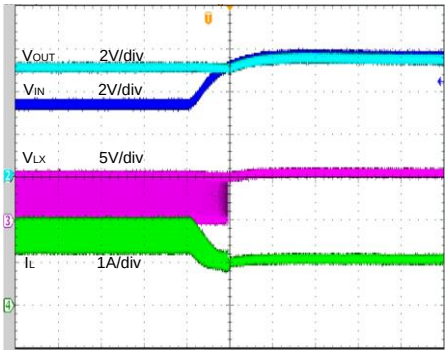
(V_{IN}=3.3V,V_{OUT}=5V,1A to Short)



Time (20ms/div)

Seamless Transition: Boost Mode→Bypass Mode

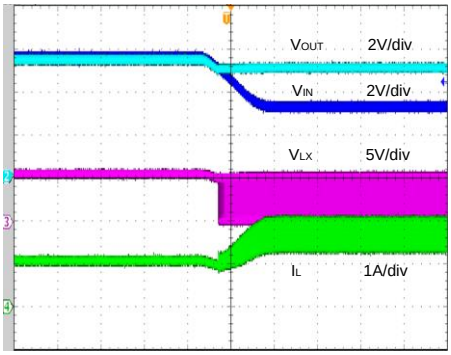
(V_{IN}=3.3V~5.5V, V_{OUT}=5.0V, I_{OUT}=1.0A)



Time (400μs/div)

Seamless Transition: Bypass Mode→Boost Mode

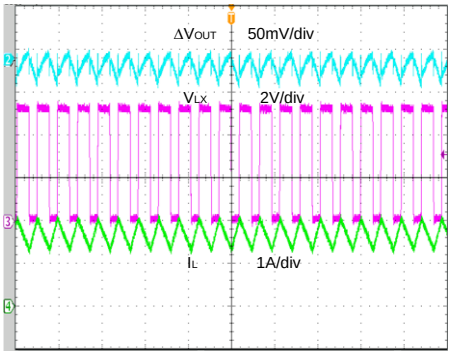
(V_{IN}=5.5V~3.3V, V_{OUT}=5.0V, I_{OUT}=1.0A)



Time (2ms/div)

Output Ripple

(V_{IN}=3.3V,V_{OUT}=5V,I_{OUT}=1A)



Time (2μs/div)

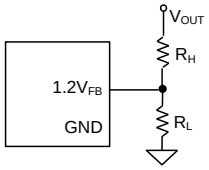
Applications Information

Because of the high integration for SY20489C, only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L and feedback resistors (R_H and R_L) need to be selected for the targeted applications specifications.

Feedback resistor dividers R_H and R_L:

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 10kΩ and 1MΩ is recommended for both resistors. If V_{OUT} is 5.0V, R_H=470kΩ is chosen, using following equation, then R_L can be calculated to be 148.4kΩ:

$$R_L = \frac{1.2V}{V_{OUT}-1.2V} R_H$$



Input capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

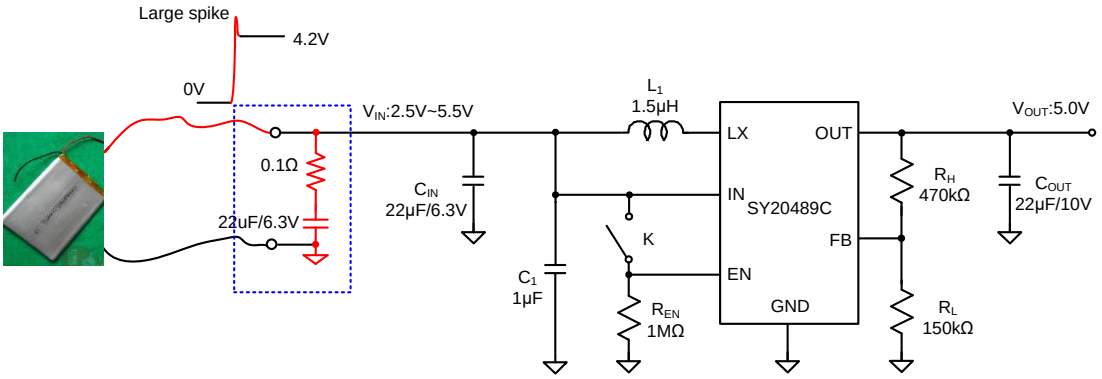
$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L \times F_{SW} \times V_{OUT}}$$

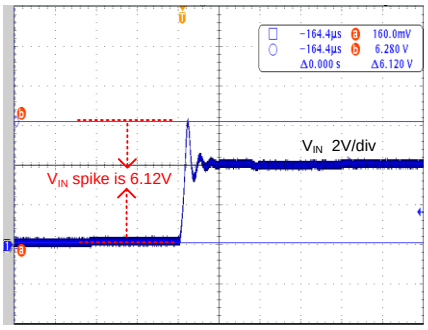
To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 22μF low ESR ceramic capacitor is recommended.

Li-Ion battery hot plug consideration:

In the mass production stage, the Li-Ion Battery will always hot plug in between IC IN and GND pin. The hot plug may lead to large voltage spike and even lead to IC EOS fail. To avoid this potential risk, 1pcs 22uF ceramic cap serial with 0.1Ω resister is recommended to absorb the input voltage spike.

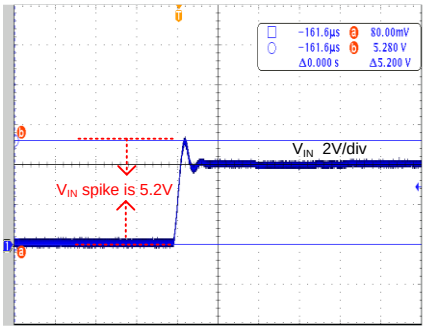
With the recommended input absorb solution, the voltage spike can be reduced from 6.12V to 5.2V.





Time (40μs/div)

C_{IN}=22μF/6.3V



Time (40μs/div)

C_{IN}=22μF/6.3V//(22μF+0.1Ω)

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 10V rating and greater than 22μF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = (\frac{V_{IN}}{V_{OUT}})^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20489C regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,MAX} + \frac{V_{IN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY20489C shutdown current drops to lower than 1μA. Driving the EN pin high (> 1.2V) will turn on the IC again.

Layout Design:

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, C_{OUT}, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. GND pin is recommended to connect to exposed paddle directly. Reasonable via holes are recommended to be placed under the exposed paddle for the better performance consideration.
2) For Boost converter, the output current is discontinuous. So the loop area formed by C_{OUT}, OUT and GND must be minimized.
3) The decoupling capacitor of IN to GND C_{IN} must be placed as close as possible with IN pin.
4) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.
5) The components R_H, R_L and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to the FB pin.

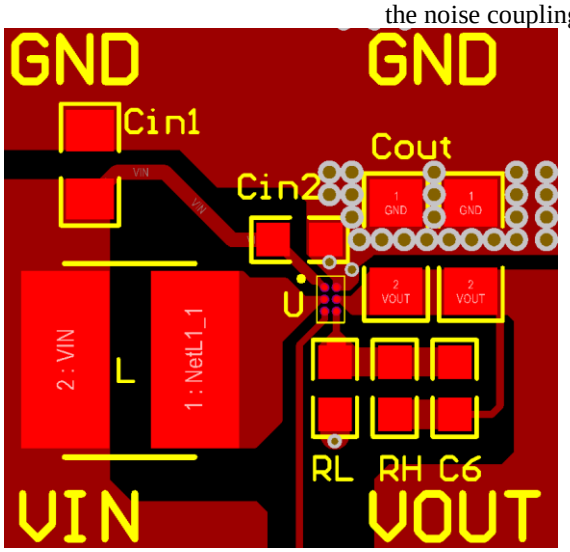
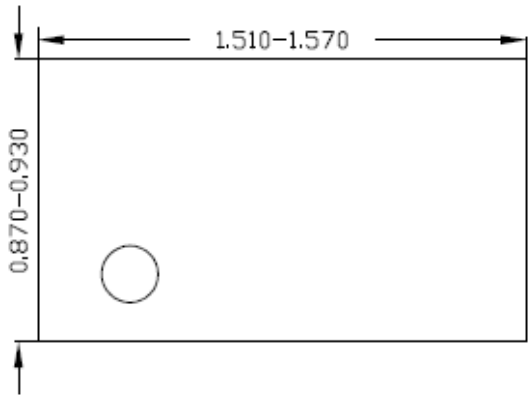
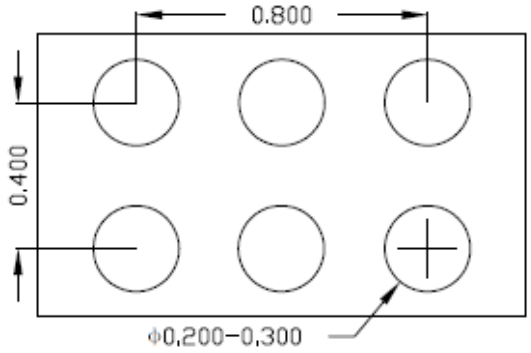


Figure4. PCB Layout Suggestion

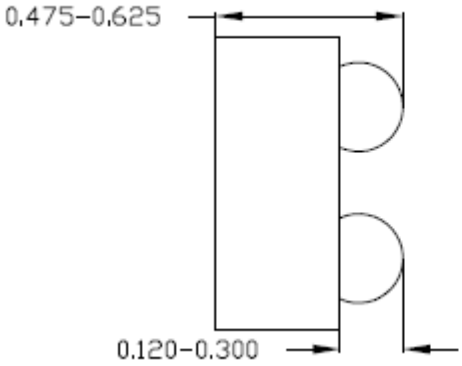
CSP1.54×0.9-6 Package Outline Drawing



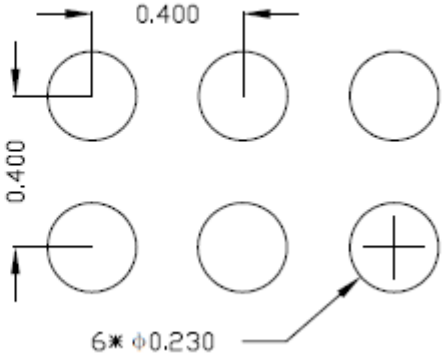
Top view



Bottom view



Side view



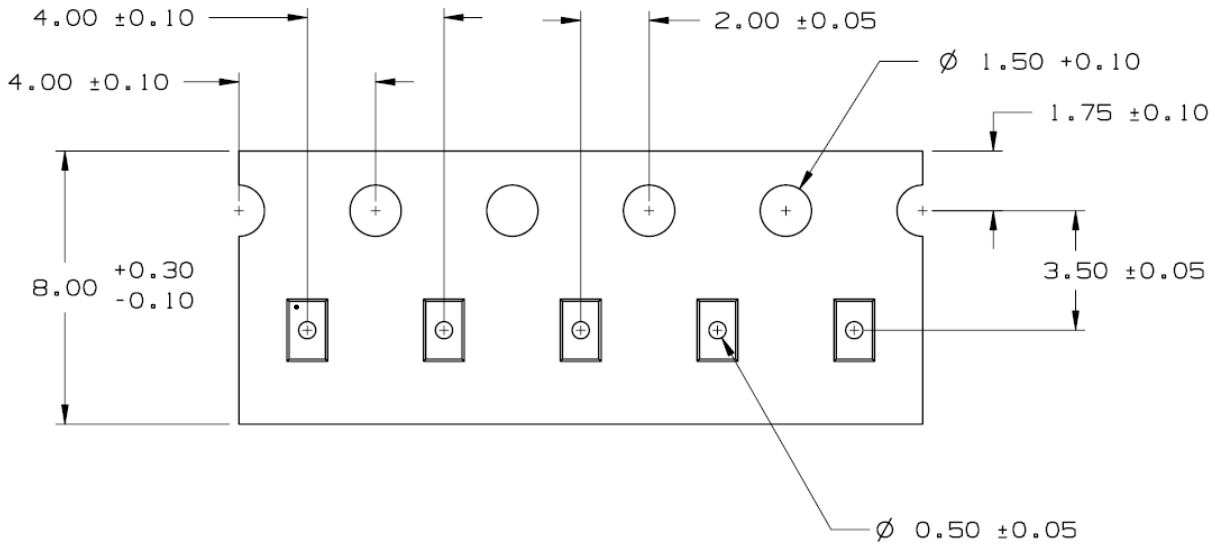
Recommended PCB Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

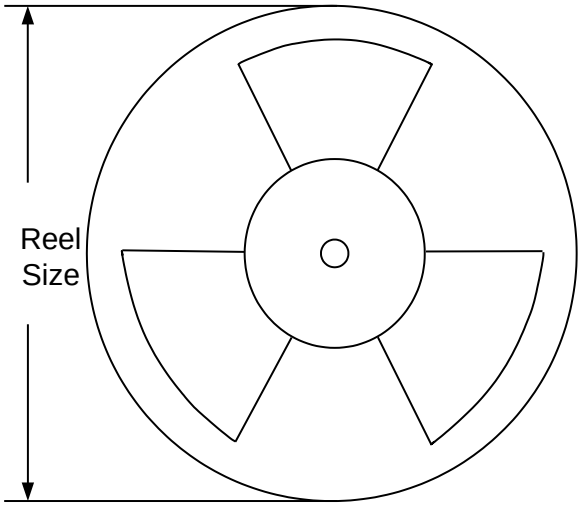
1. Taping orientation

CSP1.54×0.9-6



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP1.54×0.9-6	8	4	7"	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jun.16, 2021	Revision 0.9A	Add taping & reel specification.
Sep.16, 2020	Revision 0.9	Initial Release

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