SY20489B

5.5V Maximum Output, 3A Valley Current 1MHz Synchronous Boost Converter

General Description

The SY20489B is a high efficiency, synchronous step-up boost converter designed for single-cell lithium (Li-ion or Li-polymer) or two-cell to three-cell nickel (alkaline Ni-Cd or Ni-MH) battery-powered applications. It can operate down to 2.5V input and up to 5.5V output voltage. It uses NMOS for the main switch and PMOS for the synchronous switch.

The SY20489B disconnects the output from the input during shutdown mode. When the input voltage exceeds the regulated output voltage, the SY20489B will enter bypass mode automatically. The low operating current, along with a 0.1μA shutdown current (typ.) makes this device suitable for battery applications where extended battery life is important.

The SY20489B is available in a compact TSOT23-6 package.

Features

- 2.5V Minimum Input Voltage
- Adjustable Output Voltage from 2.5V to 5.5V
- Minimum 3A Valley Current Limit
- Capable of Seamless Transition between Boost and Bypass Mode
- Load Disconnect During Shutdown
- Low $R_{DS(ON)}$ at 5.0V Output: 50mΩ Main, 90mΩ Synchronous
- Output Overvoltage Protection (OVP)
- RoHS-Compliant and Halogen-Free
- Compact Package: TSOT23-6

Applications

Single-cell lithium or dual-cell nickel battery-powered devices (MP3 players, PDAs, etc.)

Typical Application

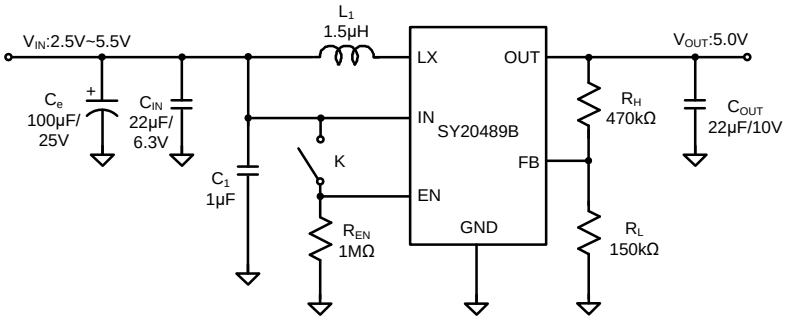


Figure 1. Schematic Diagram

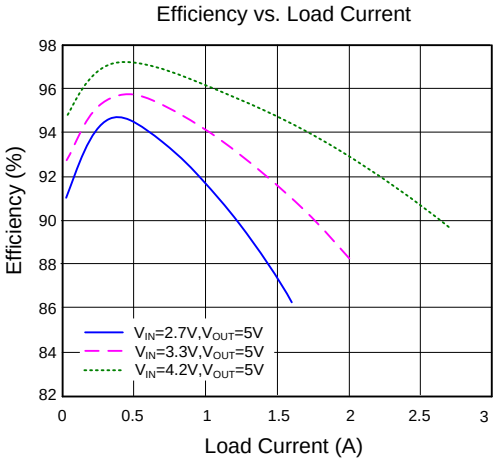


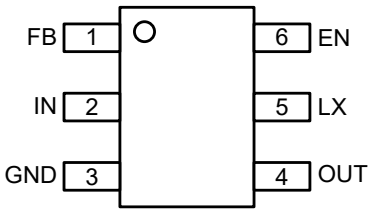
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20489BADC	SOT23-6 RoHS-Compliant and Halogen-Free	**bD*xyz***

Device code: bD
x = year code, y = week code, z = lot number code

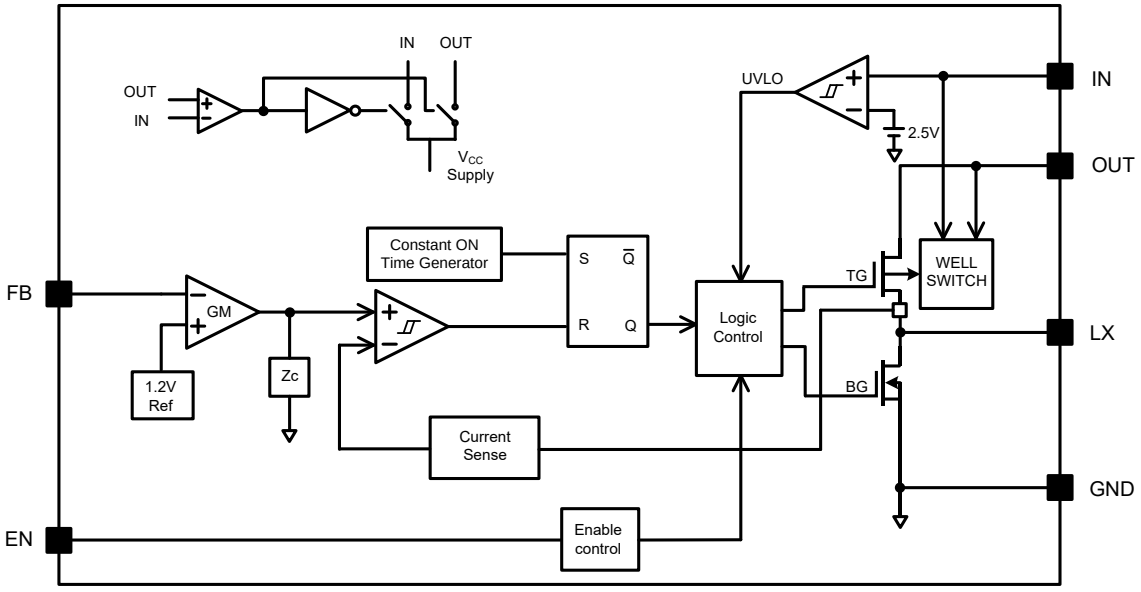
Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	FB	Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT} = 1.2 \times (1 + R_H/R_L)$.
2	IN	Signal input pin. Decouple this pin to the GND pin with at least a 1μF ceramic capacitor for noise immunity consideration.
3	GND	Ground pin.
4	OUT	Output pin. Decouple this pin to the GND pin with a minimum 22μF ceramic capacitor.
5	LX	Inductor node. Connect an inductor between the IN pin and the LX pin.
6	EN	Enable pin. Pull low to disable the device, high to enable. Do not leave this pin floating.

Functional Block Diagram



Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
FB, IN, OUT, LX, EN		6	V
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	52	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	32	
P_D Power Dissipation T_A = 25°C	1.92	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.5	5.5	V
OUT	2.5	5.5	
EN, FB	0	V_{OUT}+0.3	
LX	0	5.5	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 3.0V, V_{OUT} = 5.0V, I_{OUT} = 500mA, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		2.5		5.5	V
Output Voltage Range		V_{OUT}		2.5		5.5	V
Quiescent Current	V_{IN}	I_Q	I_O = 0A,V_{EN} = V_{IN} = 3.0V,		8		μA
	V_{OUT}		V_{OUT} = 5.0V,V_{FB} = 105%V_{REF}		32		μA
Shutdown Current		I_{SHDN}	V_{EN} = 0V, V_{IN} = 3.0V		0.1	1	μA
Linear Charge Current		I_{CHARGE}	V_{OUT} < 0.5V_{IN}		1.5		A
Input V_{IN} UVLO Threshold		V_{UVLO}				2.5	V
V_{IN} UVLO Hysteresis		V_{SYS}			0.1		V
EN Rising Threshold		V_{ENH}		1.2			V
EN Falling Threshold		V_{ENL}				0.4	V
Low Side Main FET R_{ON}		$R_{DS(ON)1}$	V_{OUT} = 5.0V		50		mΩ
Synchronous FET R_{ON}		$R_{DS(ON)2}$	V_{OUT} = 5.0V		90		mΩ
Synchronous FET Current Limit		I_{LIM}		3.0			A
Switching Frequency		fsw			1.0		MHz
Feedback Reference Voltage		V_{REF}		1.182	1.2	1.218	V
Minimum On-Time		t_{ON_MIN}			80		ns
Minimum Off-Time		t_{OFF_MIN}			80		ns
OUT Pin OVP Protection					6.0		V
OUT Pin OVP Hysteresis		OVP_{HYS}			0.25		V
Thermal Shutdown Temperature		T_{SD}			150		°C
Thermal Shutdown Hysteresis		T_{HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

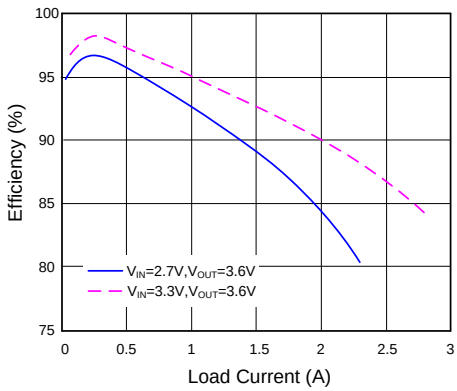
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

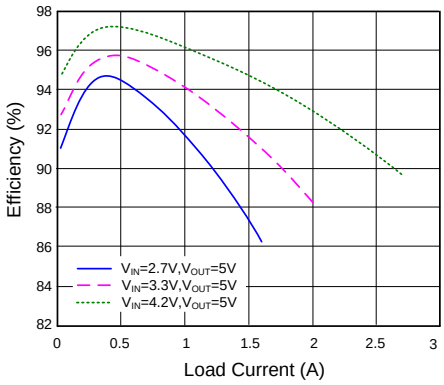
Typical Performance Characteristics

(T_A= 25ºC, V_{IN}=3.3V, V_{OUT} = 5V, L = 1.5µH, C_{OUT}= 22µF, unless otherwise specified.)

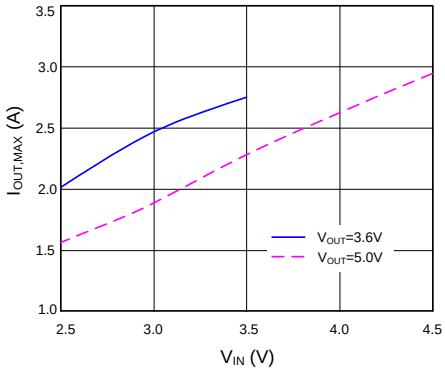
Efficiency vs. Load Current



Efficiency vs. Load Current

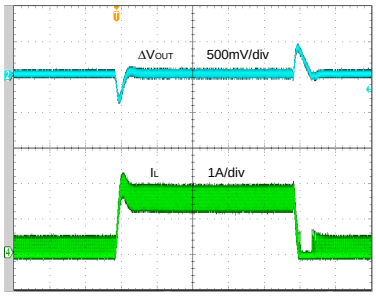


Max Load Current vs. V_{IN}



Load Transient

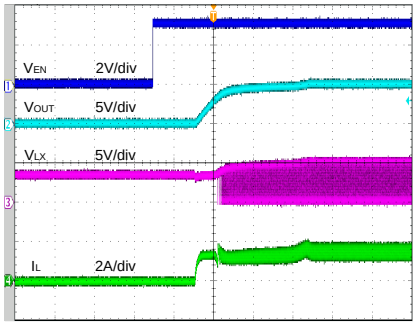
(V_{IN}=3.3V,V_{OUT}=5V,Io=0.1A~1A)



Time (100µs/div)

Startup from Enable

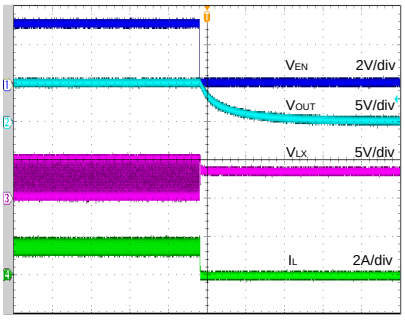
(V_{IN}=3.3V,V_{OUT}=5V,Io=1A)



Time (100µs/div)

Shutdown from Enable

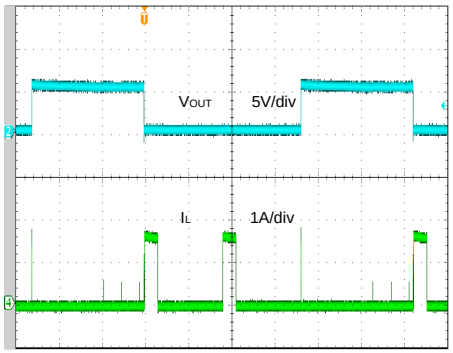
(V_{IN}=3.3V,V_{OUT}=5V,Io=1A)



Time (100µs/div)

Short Circuit Protection

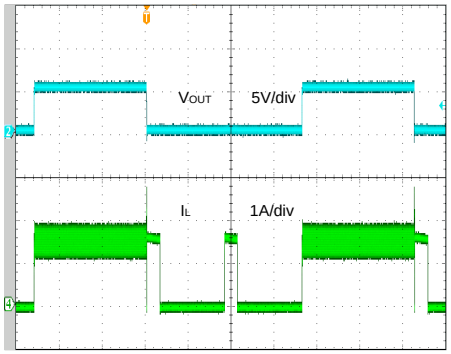
(V_{IN}=3.3V,V_{OUT}=5V,0A to Short)



Time (20ms/div)

Short Circuit Protection

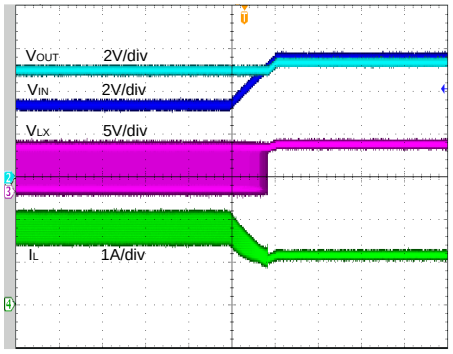
(V_{IN}=3.3V,V_{OUT}=5V,1A to Short)



Time (20ms/div)

Seamless Transition: Boost Mode→Bypass Mode

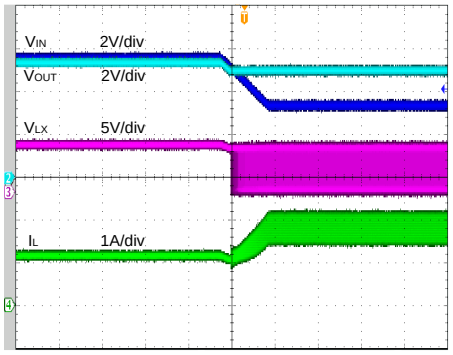
(V_{IN}=3.3V~5.5V, V_{OUT}=5.0V, Io=1.0A)



Time (10ms/div)

Seamless Transition: Bypass Mode→Boost Mode

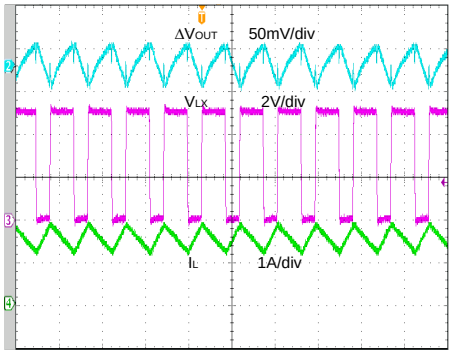
(V_{IN}=5.5V~3.3V, V_{OUT}=5.0V, Io=1.0A)



Time (10ms/div)

Output Ripple

(V_{IN}=3.3V,V_{OUT}=5V,Io=1A)



Time (1μs/div)

Application Information

Operation

The SY20489B operates using constant on-time valley current control. The one-shot circuit or on-time generator, which determines how long to turn on the high side power switch, is fundamental to any constant on-time (COT) architecture. Each on-time (t_{ON}) is a fixed period internally calculated to operate the step-down regulator at the desired switching frequency over the input and output voltage range, where $t_{ON} = t_{SW} \times (V_O - V_{IN})/V_O$.

The low side FET is turned on at the start of every switching cycle, and inductor current ramps up. After turning on for the period t_{ON}, the low side FET closes and the high side FET opens. During this period, inductor current decays until it is lower than the valley current threshold V_{COMP}. An internal signal then sets and the low side FET starts turning on in a new switching cycle. See Figure 3 for details.

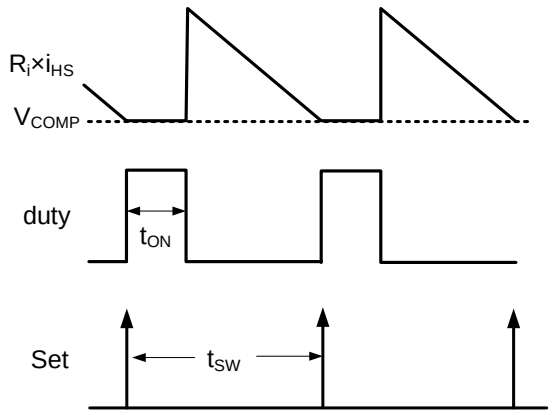


Figure 3. Constant On-Time Valley Current Control

The following paragraphs describe the selection process for the input capacitor C_{IN}, the output capacitor C_{OUT}, the inductor L, and the feedback resistor divider (R_H and R_L).

Feedback Resistor divider R_H and R_L:

Choose R_H and R_L in the feedback resistor divider to configure the output voltage. A value between 100kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. If V_{OUT} = 3.3V and R_H is chosen to be 510kΩ, then R_L can be calculated as 300kΩ using the following formula:

$$R_L = \frac{1.2V}{V_{OUT}-1.2V} R_H$$

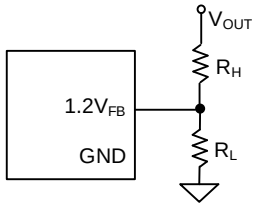


Figure 4. Feedback Resistor Divider

Input Capacitor C_{IN}

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current..

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L\, f_{SW} \times V_{OUT}}$$

For the best performance, select a typical X5R or better grade ceramic capacitor. The component should be placed as close as possible to the IN and GND pins, while also minimizing the loop area formed by C_{IN} and the IN/GND pins. In this case, a 22µF low ESR ceramic capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use an X5R or better grade ceramic capacitor with a 10V rating and at least 22µF capacitance.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, both should be considered.

$$V_{RIPPLE,\ ESR1} = I_{LPEAK} \times ESR$$

$$V_{RIPPLE,\ ESR2} = I_{LVALLEY} \times ESR$$

$$V_{RIPPLE,CAP} = \frac{I_{OUT} \times (1\text{-}D)}{C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Li-Ion Battery Hot Plug Consideration

In the mass production stage, the Li-Ion battery will always hot plug between the IN and GND pins. The hot plug may lead to large voltage spikes, or even to IC EOS failure. To avoid this potential risk, place one 22µF ceramic capacitor in series with a 0.1Ω resistor to absorb the input voltage spike. With this solution, the voltage spike can be reduced from 6.12V to 5.2V. See Figure 5 and Figure 6 for more details.

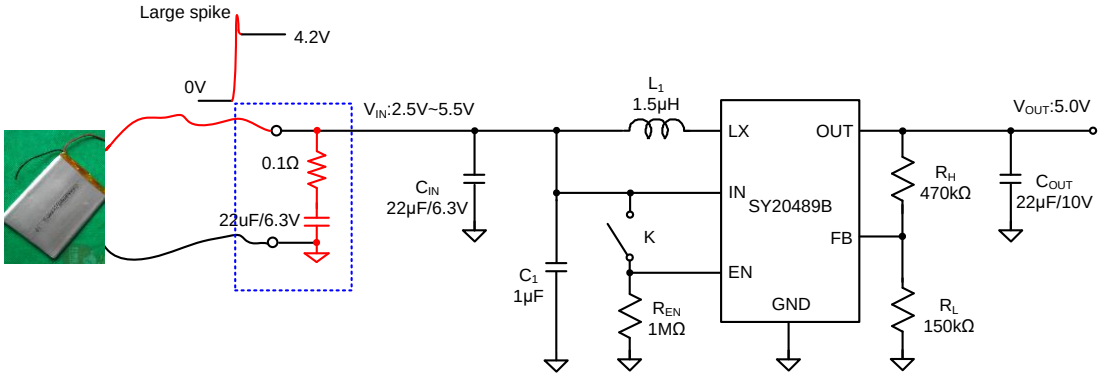


Figure 5. Voltage Spike Suppression

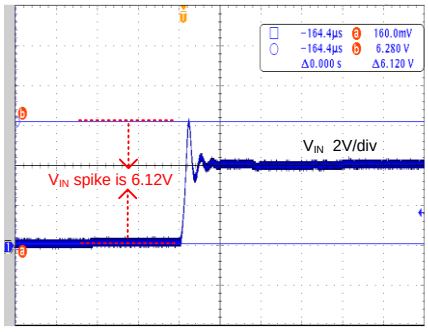


Figure 6. Voltage Spike without Suppression

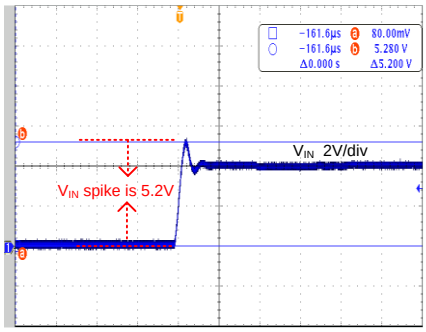


Figure 7. Voltage Spike with Suppression

Inductor L

Consider the following when choosing this inductor:

- Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{f_{SW} \times I_{OUT\_MAX} \times 40\%}$$

  where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

  The SY20489B has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

- The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN} \times \eta}\right) \times I_{OUT\_MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

- The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR greater than 50mΩ to achieve a good overall efficiency.

Enable Operation

Driving the EN pin high (>1.2V) enables normal operation. Driving the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY20489B shutdown current drops to less than 1μA.

Overvoltage Protection

The SY20489B provides output overvoltage protection. If the output voltage exceeds V_{OVP} (typ. 6V), the device stops switching, and the main switch is turned off. When the output voltage returns to the normal operating range, the device resumes operation.

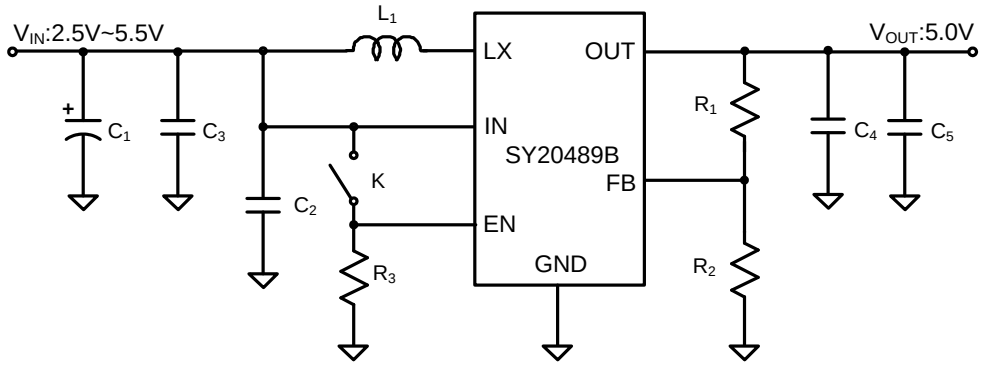
Overcurrent Protection

The SY20489B provides cycle-by-cycle overcurrent protection and turns off the main power MOSFET once the inductor current reaches the overcurrent limit threshold. During overcurrent protection, the output voltage drops as a function of the load. As soon as the overload condition is removed, the converter resumes operation.

Thermal Protection

The SY20489B includes overtemperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature cools down by approximately 20°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

Typical Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage (V)	Output Current Limit (A)
2.5-5	5	1

BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1	100μF/25V Electrolytic Capacitor		
L_1	1.5μH/5.5A inductor	VLC5045T-1R5M	TDK
	1.5μH/3.8A inductor	LTF5022T-1R5M	TDK
C_2	1μF/25V, 0603, X5R	C1608X5R1E105K	TDK
C_3	22μF/6.3V/X5R, 0805	C2012X5R0J226M	TDK
C_4	22μF/10V, 1206, X5R	C3216X5R1A226M	TDK
C_5	NC		
R_1	470kΩ, 0603, 1%		
R_2	150kΩ, 0603, 1%		
R_3	1MΩ, 0603		

Recommended Components for Typical Applications

V_{OUT}(V)	R_L (kΩ)	R_H (kΩ)	L(μH)	C_{OUT}
5	470	150	1.5	22μF/10V/X5R,1206
3.3	510	300	1.5	22μF/10V/X5R,1206

Recommended PCB Layout

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- Place the following components as close as possible to the IC: C_{IN}, C_{OUT}, L, R_H, and R_L.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. If board space allows, a ground plane is highly recommended. Connect the GND pin to the exposed paddle directly. Place via holes under the exposed paddle.
- C_{IN} must be close to the IN pin. Minimize the loop area formed by C_{OUT}, OUT, and GND.
- Minimize the PCB copper area associated with the LX pin to reduce EMI emissions.
- To avoid crosstalk, R_H, R_L, and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout.

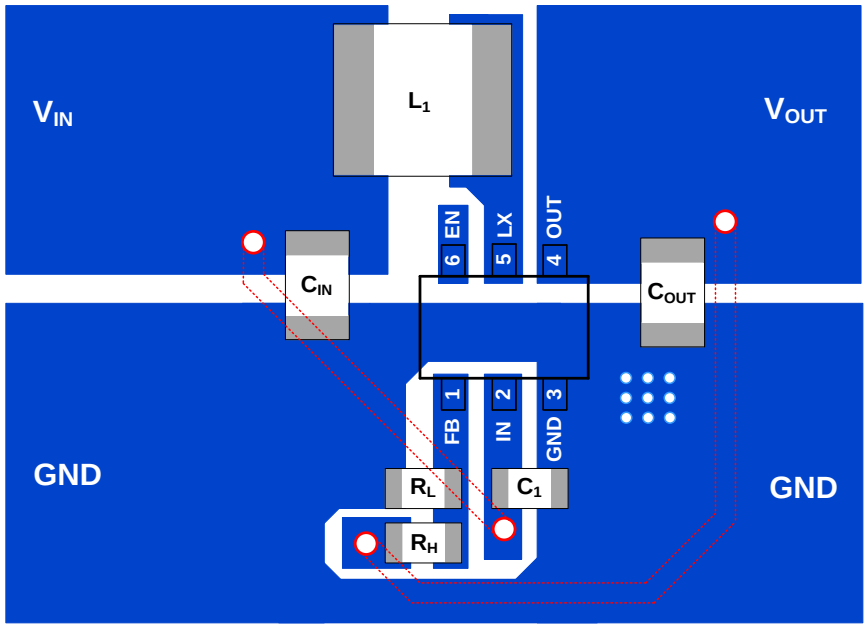
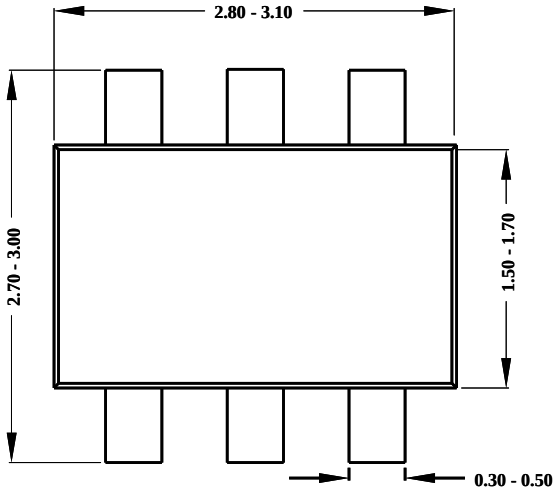
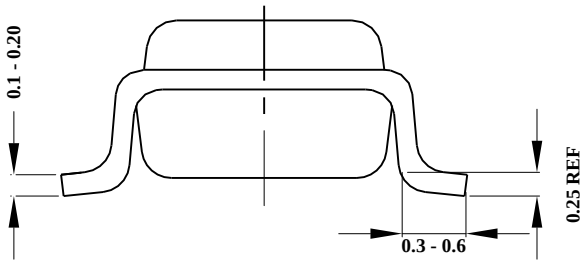


Figure 8. Suggested PCB Layout

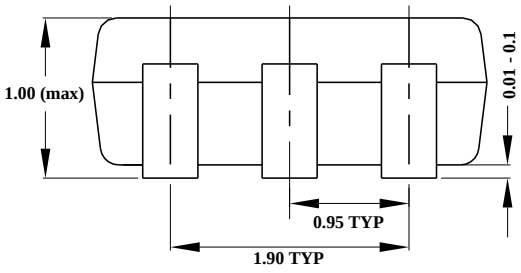
TSOT23-6 Package Outline Drawing



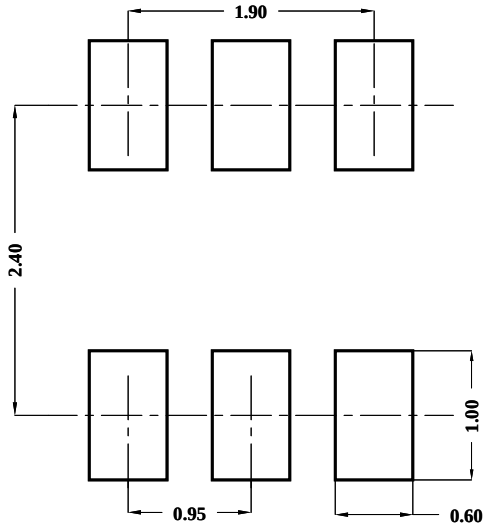
Top view



Side view A



Side view B

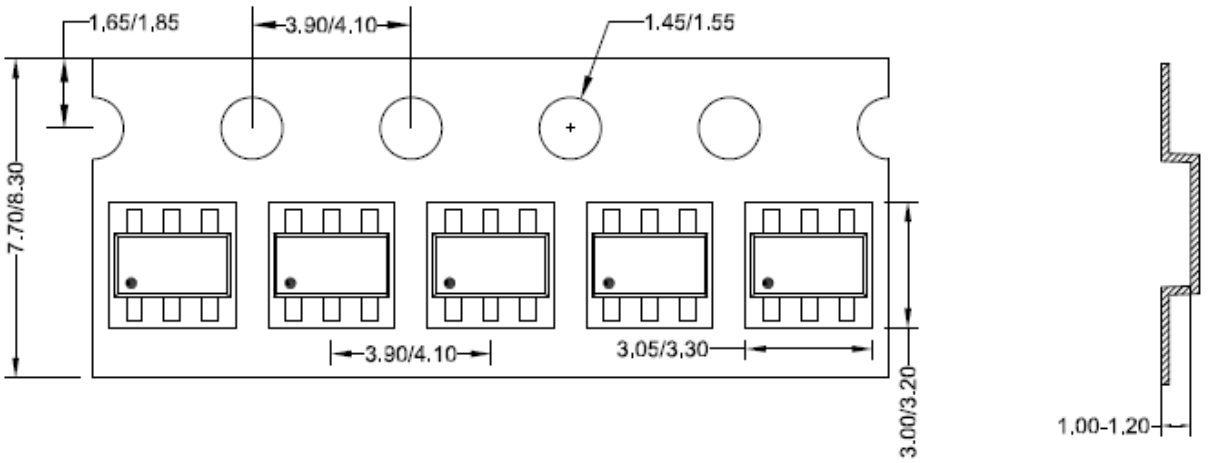


Recommended pad layout (reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

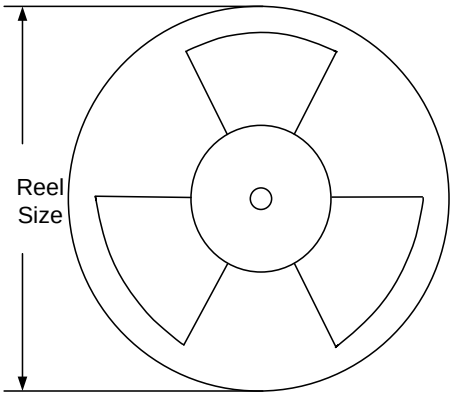
Taping and Reel Specification

TSOT23-6 taping orientation



Feeding direction ⟶

Carrier tape and reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
TSOT23-6	8	4	7	400	160	3000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.20, 2024	Revision 1.0	Language improvements for clarity.
Aug. 15, 2017	Revision 0.9	Initial Release

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