SY20419

1.8V Minimum Input and 5. 5V Maximum Output High Efficiency 1A Valley Current Synchronous Boost

General Description

The SY20419 is a high efficient, synchronous, step-up Boost converter designed for one-cell Li-Ion or Li-polymer, or a two to three-cell alkaline Ni-Cd or Ni-MH battery powered applications. It can convert down to 1.8V input voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch.

The SY20419 can disconnect the output from input during the shutdown mode. When input voltage exceeds the regulated output voltage, the SY20419 enters bypass mode automatically.

Features

- 1.8V Minimum Input Voltage
- Adjustable Output Voltage from 1.8V to 5.5V
- Min 1A Valley Current Limit
- CCM Only Operation
- Load Disconnect During Shutdown
- Low $R_{DS(ON)}$ (Main Switch/Synchronous Switch) at 3.3V Output: 70/125mΩ
- Output OVP
- RoHS Compliant and Halogen Free
- Auto Bypass Mode When $V_{IN} \geq V_{OUT}$
- Compact Package DFN2×1.5-6

Ordering Information

SY20419 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20419SUD	DFN2×1.5-6	----

Applications

- All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment

Typical Applications

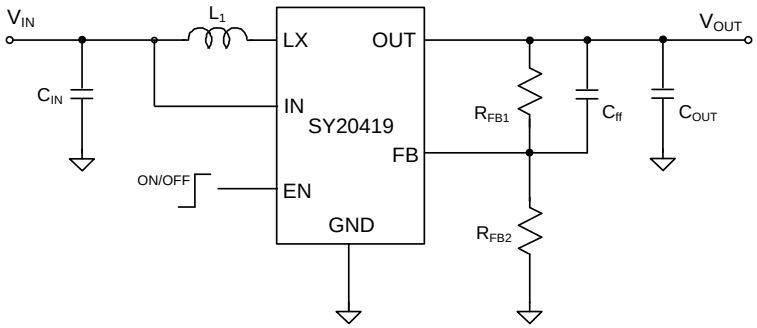


Figure1. Schematic Diagram

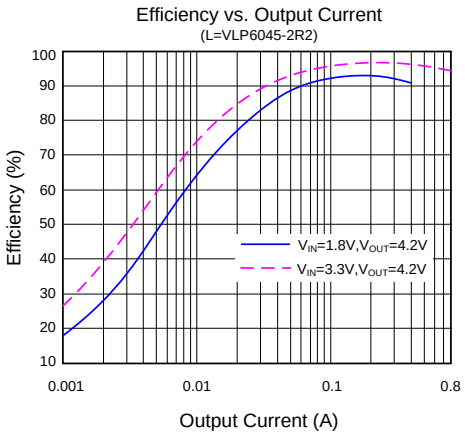
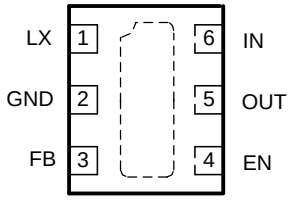


Figure 2. Efficiency vs. Load Current

Pinout (top view)



(DFN2×1.5-6)

Top mark: **9E*xyz* *for SY20419SUD*** (Device code: **9E**, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
LX	1	Inductor node. Connect an inductor between the IN pin and the LX pin.
GND	2	Ground pin.
FB	3	Feedback pin. Connect a resistor R_{FB1} between OUT and FB, and a resistor R_{FB2} between FB and GND to program the output voltage. V_{OUT}=1.2V× (R_{FB1}/R_{FB2}+1).
EN	4	Enable pin. Pull high to turn on. Do not leave it floating.
OUT	5	Output pin. Decouple this pin to the GND pin with a minimum of 22μF ceramic capacitor.
IN	6	Input pin.

Block Diagram

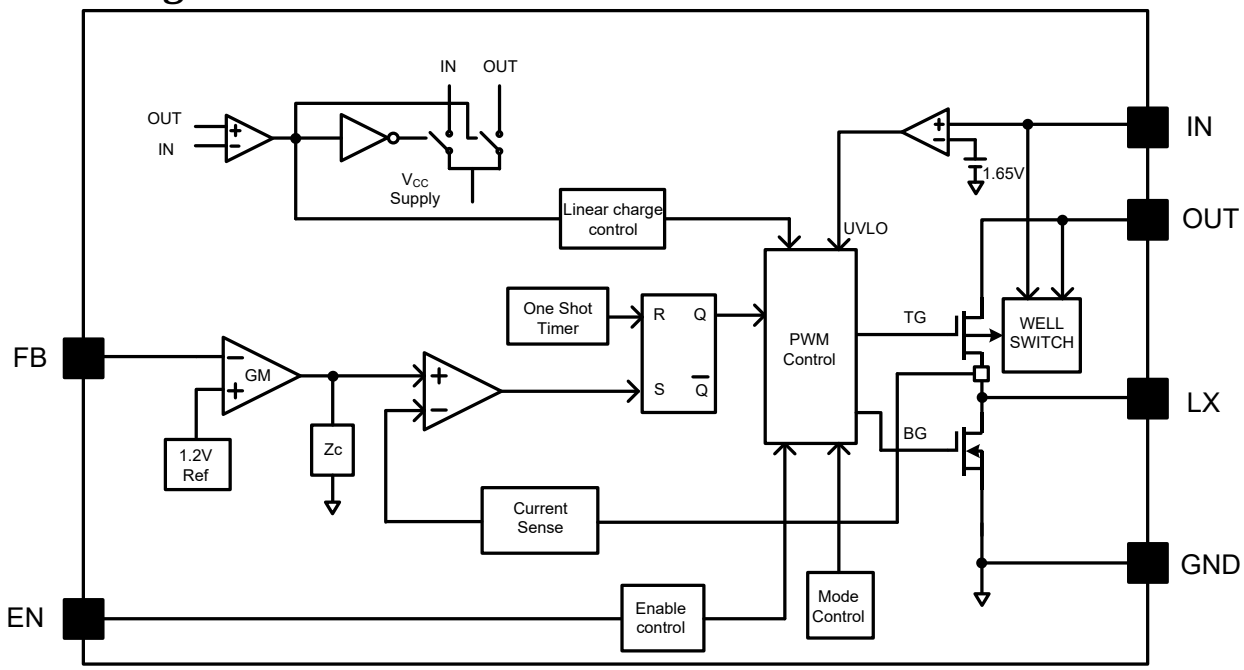


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

FB, IN, OUT, EN ---------- -0.3V to 6.0V
LX ---------- -0.3V (*1) to 6.0V (*2)
Power Dissipation, P_D@ T_A=25°C DFN2×1.5-6---------- 1.67W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 60°C/W
θ_{JC} ---------- 15°C /W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
(*1) LX Voltage tested down to -3V< 20ns
(*2) LX Voltage tested up to +7V< 20ns

Recommended Operating Conditions (Note 3)

IN ---------- 1.8V to 5.5V
OUT---------- 1.8V to 5.5V
EN ---------- 0V to V_{OUT}+0.3V
All Other Pins ---------- 0-5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =2.4V, V_{OUT}=3.3V, I_{OUT}=500mA, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		1.8		5.5	V
Input UVLO Threshold	V_{UVLO}			1.65	1.75	V
Input UVLO Hysteresis	V_{HYS}			0.13		V
Shutdown Current	I_{SHDN}	V_{EN}=0V,V_{IN}=2.4V		0.1	1	μA
Linear Charge Current	I_{CHARGE}	V_{OUT}<0.5V_{IN}		0.5		A
Feedback Reference Voltage	V_{REF}		1.182	1.2	1.218	V
Low Side Main FET R_{ON}	$R_{DS(ON)1}$			70		mΩ
Synchronous FET R_{ON}	$R_{DS(ON)2}$			125		mΩ
EN Input Voltage High	$V_{EN,H}$		1.2			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
EN Leakage Current	$I_{EN,LK}$	V_{EN}=3.3V	-1		1	μA
Min ON Time	$t_{ON,MIN}$			60		ns
Min OFF Time	$t_{OFF,MIN}$			140		ns
Soft-start Time	t_{SS}			1		ms
Switching Frequency	f_{SW}	V_{OUT}=3.3V		1		MHz
Valley FET Current Limit	$I_{LMT,VAL}$		1			A
Negative Current Limit	$I_{LMT,NEG}$		-0.5			A
Output Over Voltage Threshold	V_{OVP}			5.8		V
Output Over Voltage Hysteresis	$V_{OVP,HYS}$			0.3		V
Thermal Shutdown Temperature	T_{SD}			150		˚C
Thermal Shutdown Hysteresis	T_{HYS}			20		˚C

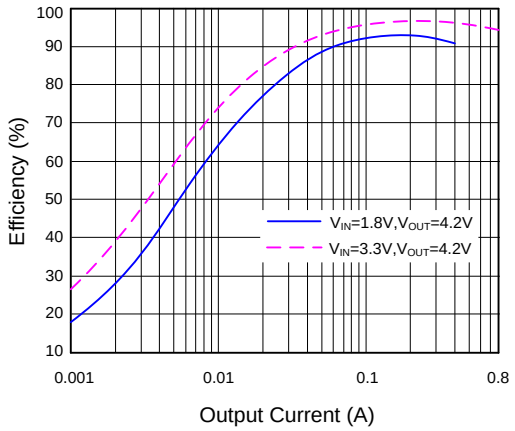
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25˚C on a two-layer Silergy Evaluation Board.

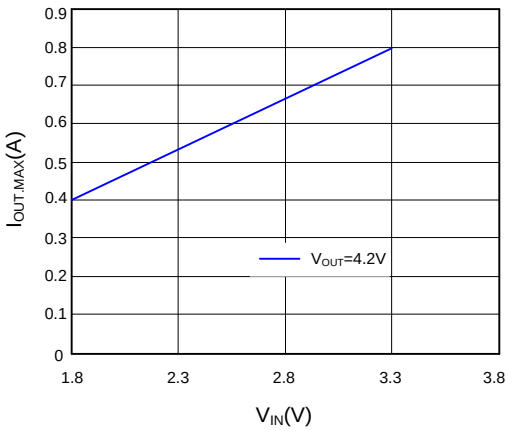
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

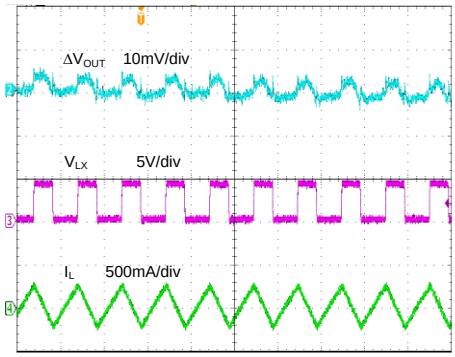
Efficiency vs. Output Current
(L=VLP6045-2R2)



Max Load Current vs. V_{IN}

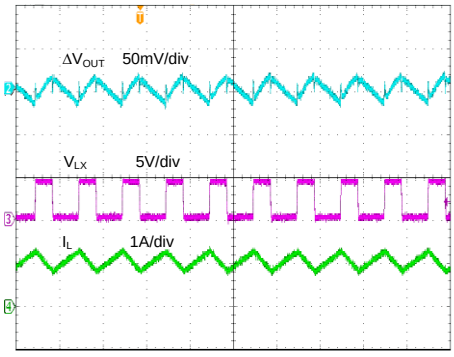


Output Ripple
(V_{IN}=1.8V, V_{OUT}=4.2V, I_{OUT}=0A)



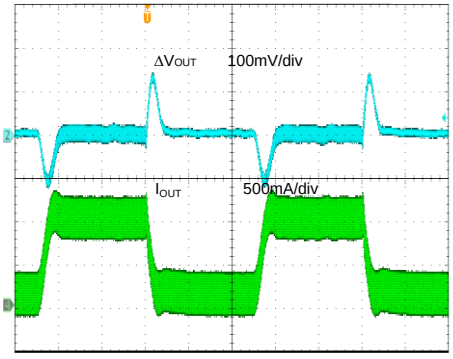
Time (1μs/div)

Output Ripple
(V_{IN}=1.8V, V_{OUT}=4.2V, I_{OUT}=0.4A)



Time (1μs/div)

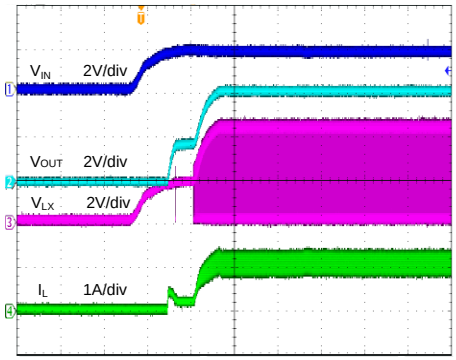
Load Transient
(V_{IN}=1.8V, V_{OUT}=4.2V, I_{OUT}=0.03~0.3A)



Time (200μs/div)

Startup from V_{IN}

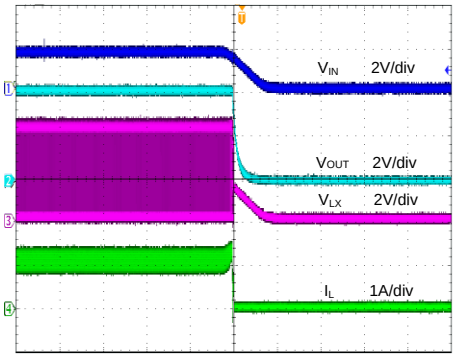
(V_{IN}=1.8V, V_{OUT}=4.2V, I_{OUT}=0.4A)



Time (800µs/div)

Shutdown from V_{IN}

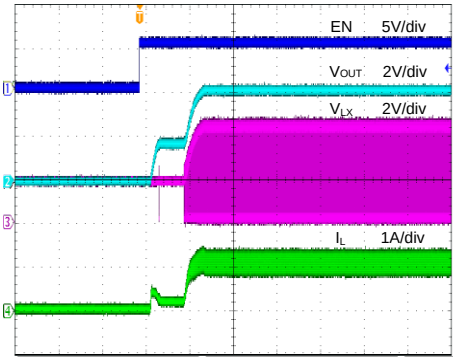
(V_{IN}=1.8V, V_{OUT}=4.2V, I_{OUT}=0.4A)



Time (2ms/div)

Startup from Enable

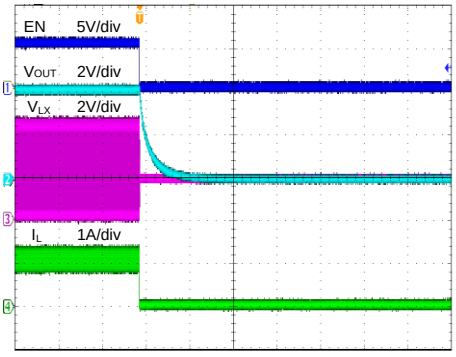
(V_{IN}=1.8V, V_{OUT}=4.2V, I_{OUT}=0.4A)



Time (800µs/div)

Shutdown from Enable

(V_{IN}=1.8V, V_{OUT}=4.2V, I_{OUT}=0.4A)

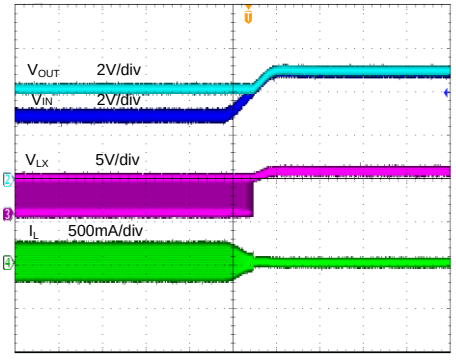


Time (800µs/div)

Seamless Transition:

(Boost Mode → Bypass Mode

V_{IN}=3.3~5V, V_{OUT}=4.2V, I_{OUT}=0A)

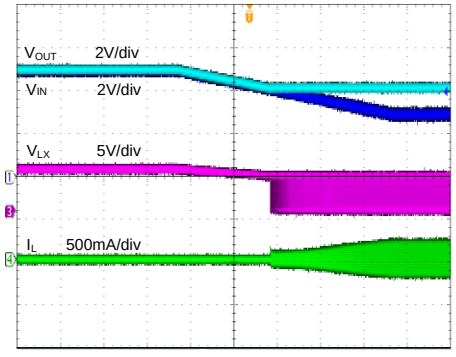


Time (2ms/div)

Seamless Transition:

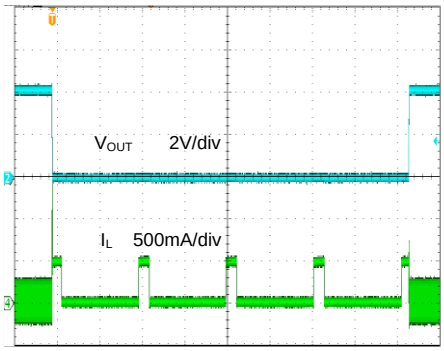
(Bypass Mode → Boost Mode

V_{IN}=5~3.3V, V_{OUT}=4.2V, I_{OUT}=0A)



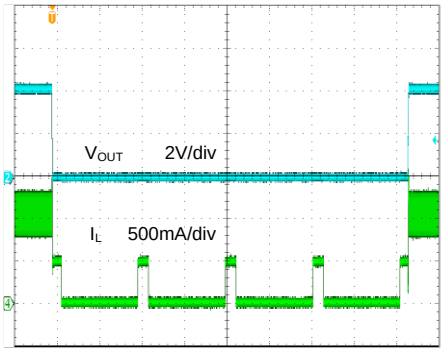
Time (4ms/div)

Short Circuit Protection
(V_{IN}=1.8V, V_{OUT}=4.2V, I_O=0A~Short)



Time (40ms/div)

Short Circuit Protection
(V_{IN}=1.8V, V_{OUT}=4.2V, I_O=0.4A~Short)



Time (40ms/div)

Applications Information

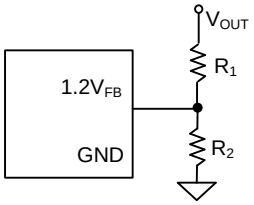
Because of the high integration in the SY20419, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the inductor L and the feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 100kΩ and 1MΩ is recommended for both resistors. If V_{OUT} is 3.3V, R_1=510kΩ is chosen, using following equation, then R2 can be calculated to be 300kΩ:

$$R_2 = \frac{1.2V}{V_{OUT} - 1.2V} R_1$$

.



Input Capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L \times f_{SW} \times V_{OUT}}$$

To minimize the potential noise problem, a typical X5R or a better grade ceramic capacitor should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} and IN/GND pins. In this case, a 22µF low ESR ceramic capacitor is recommended.

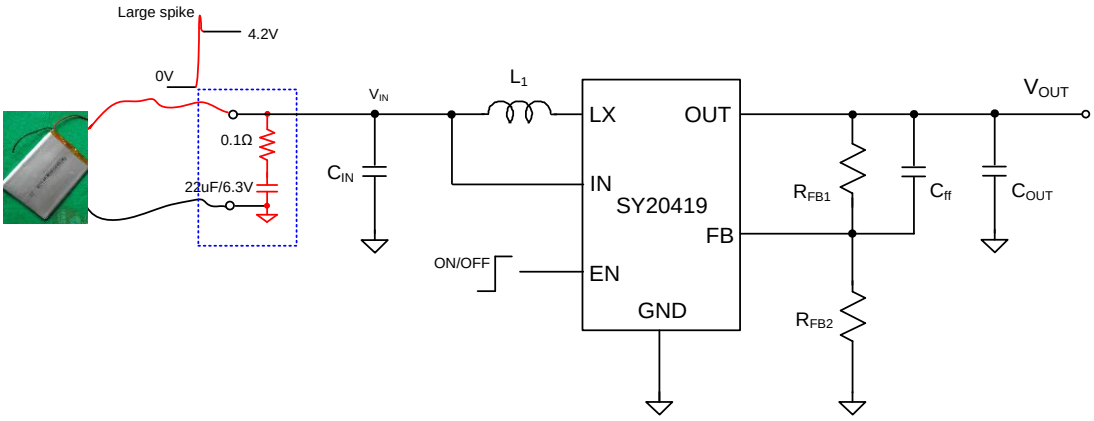
Output Capacitor C_{OUT}:

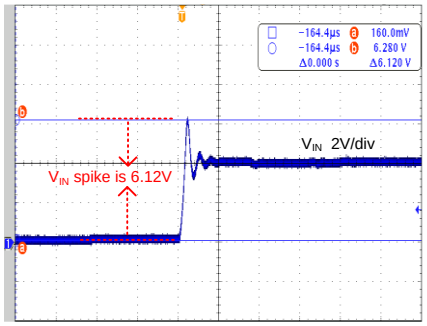
The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or a better grade ceramic capacitor with 6.3V rating and greater than 22µF capacitance.

Li-Ion Battery Hot Plug Consideration:

In the mass production stage, the Li-Ion Battery will always hot plug in between IC IN and GND pin. The hot plug may lead to large voltage spike and even lead to IC EOS fail. To avoid this potential risk, 1pcs 22µF ceramic cap serial with 0.1Ω resister is recommended to absorb the input voltage spike.

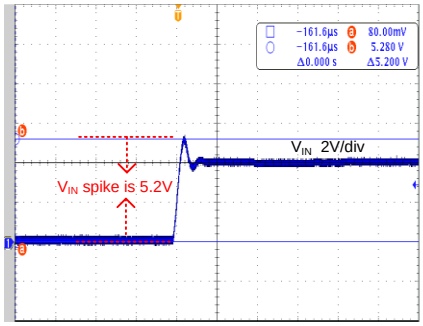
With the recommended input absorb solution, the voltage spike can be reduced from 6.12V to 5.2V.





Time (40μs/div)

C_{IN}=22μF/6.3V



Time (40μs/div)

C_{IN}=22μF/6.3V//(22μF+0.1Ω)

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20419 regulator is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,MAX} + \frac{V_{IN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY20419 shutdown current drops to lower than 1μA, driving the EN pin high (> 1.2V) will turn on the IC again.

Layout Design:

The layout design of SY20419 is relatively simple. For the best efficiency and minimum noise problems, the following components should be placed close to the IC: C_{IN}, C_{OUT}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to the IN and GND pins. The loop area formed by C_{IN} and GND must be minimized.

3) C_{OUT} must be close to the pins OUT and GND. The loop area formed by C_{OUT} and GND must be minimized.

4) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

5) The components R_1, R_2 and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

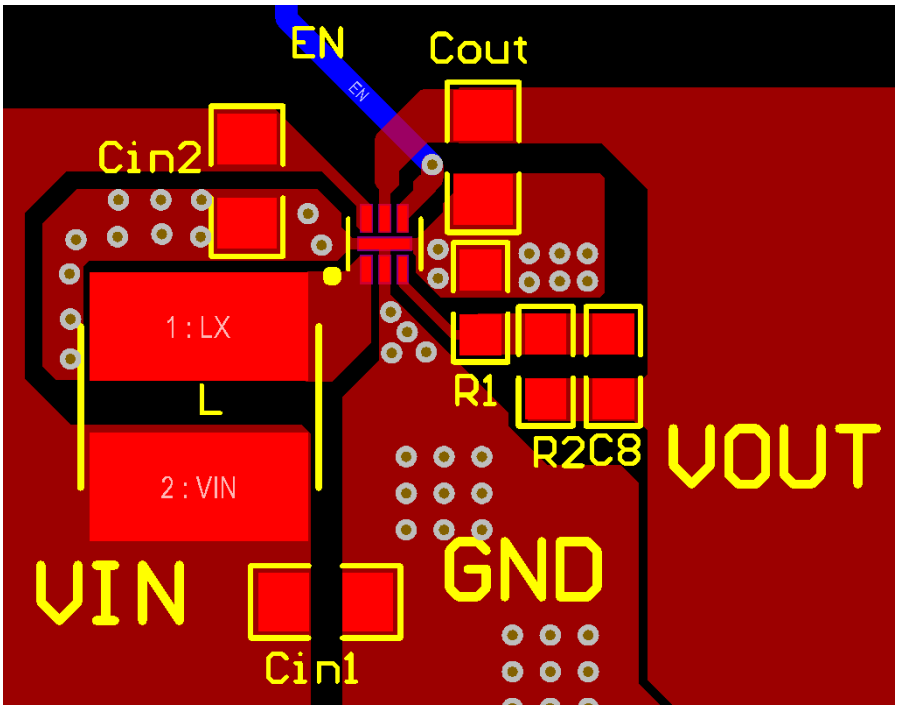
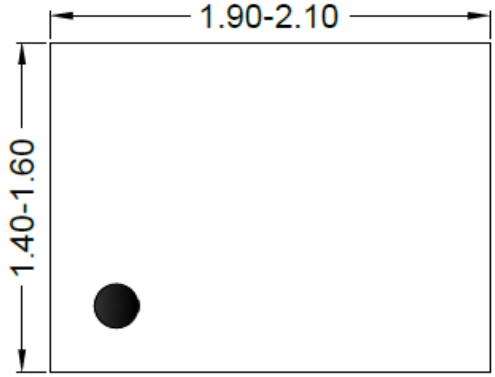
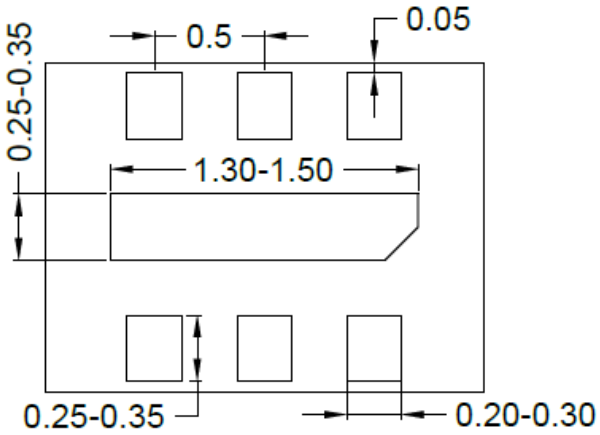


Figure4. PCB Layout Suggestion

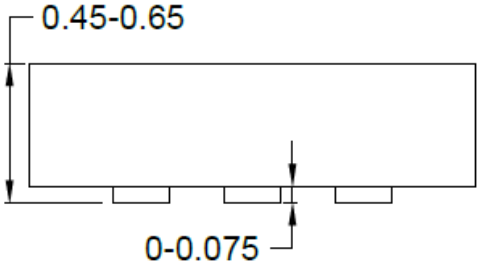
DFN2×1.5-6 Package Outline Drawing



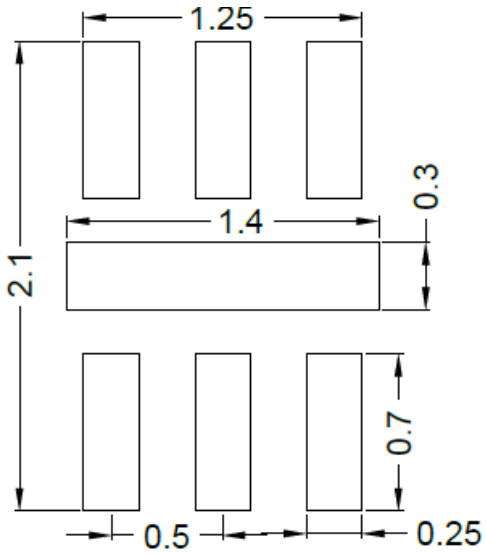
Top view



Bottom view



Side view



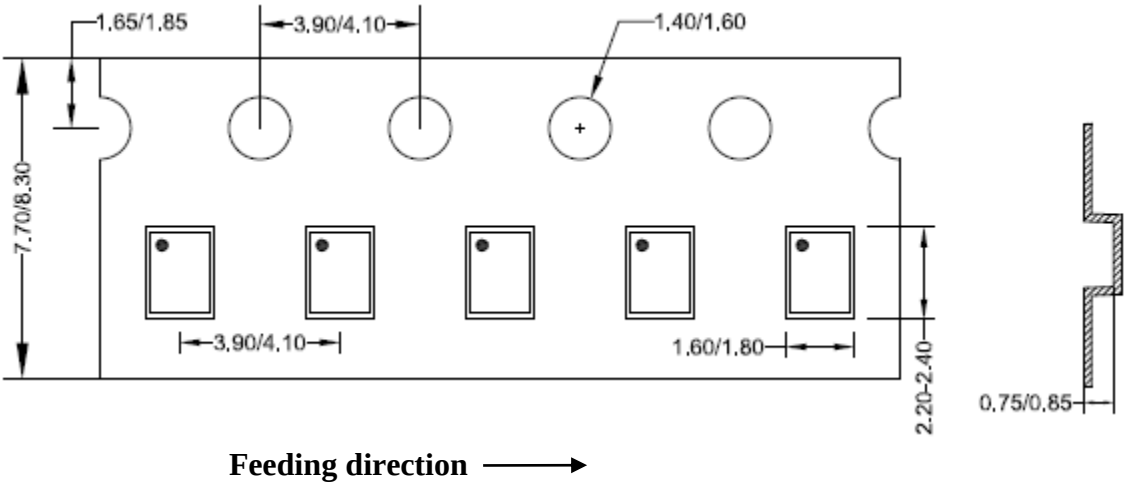
Recommended PCB layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

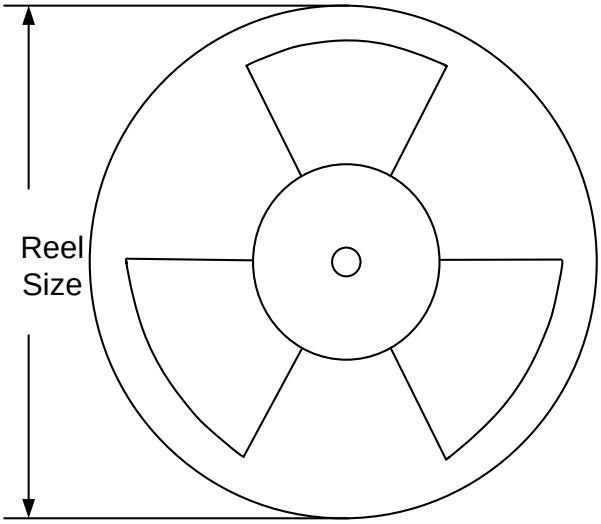
1. Taping orientation

DFN2×1.5



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2×1.5	8	4	7	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Sep.04, 2020	Revision 0.9	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com