

## General Description

SY22856A is a Flyback regulator targeting at Constant Current/Constant Voltage (CC/CV) applications. It integrates a 200V MOSFET in a compact SO8 package to minimize the size. Both the output current and voltage are sensed on the primary side, eliminating the opto-isolator and the secondary side feedback circuitry, and minimizing the overall system cost.

SY22856A adopts the quasi-resonant operation and the adaptive PWM/PFM control to achieve the highest average efficiency and the best EMI performance. In addition, to reduce capacitors and magnetic volume, the maximum frequency is up to 300kHz.

SY22856A provides reliable protections such as VCC Over Voltage Protection (OVP), Short Circuit Protection (SCP), Over Temperature Protection (OTP), Output Over Voltage Protection (OVP), VSEN Pin Short Protection, etc.

## Features

- Tight PSR CC/CV Regulation Over Entire Operating Range
- Integrated 200V MOSFET
- QR Mode and PWM/PFM Control for Higher Average Efficiency
- Maximum Switching Frequency Limitation 300kHz
- Low Start Up Current: 4μA Max
- Internal CC/CV Loop Compensation
- Reliable Protections for OVP, SCP, OTP
- Compact Package: SO8

## Applications

- Telecom Adapters
- POE Power Devices
- Security Cameras

Recommended operating output power	
Products	Output power
SY22856A	12W

## Typical Applications

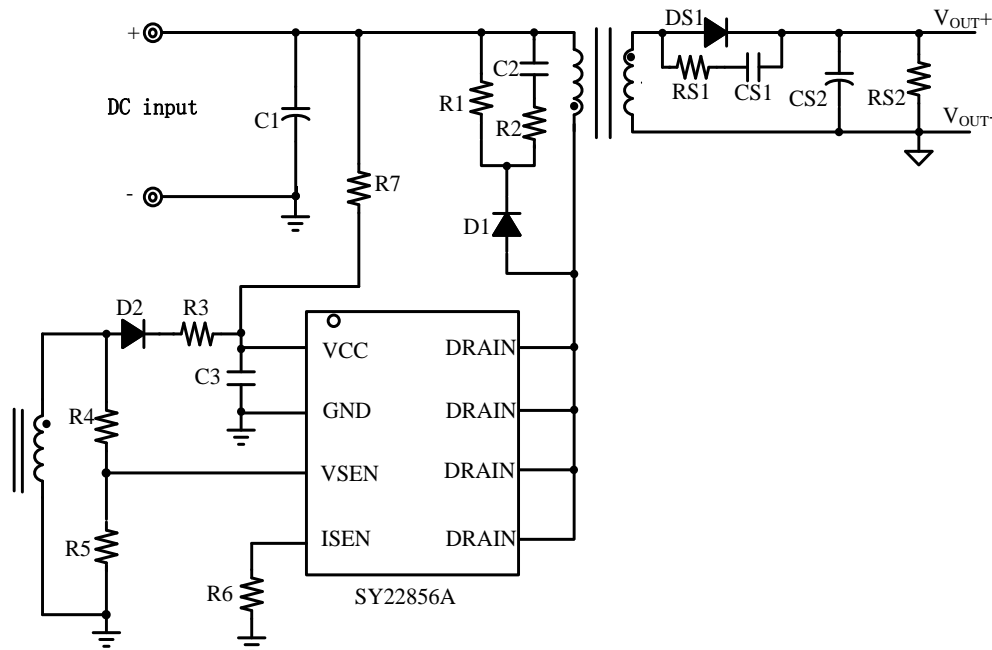
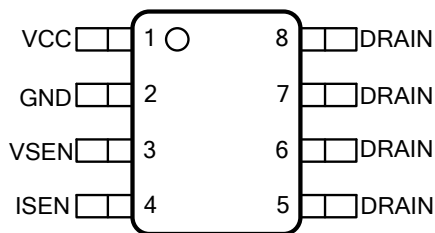
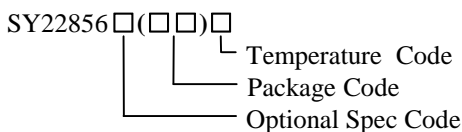


Figure 1. Schematic Diagram

## Ordering Information



Pinout (Top view)

Ordering Number	Package	Top Mark
SY22856AFAC	SO8	BSDxyz

x=year code, y=week code, z= lot number code

## Pinout (top view)

Pin	Name	Pin Description
1	VCC	Power supply pin.
2	GND	Ground pin.
3	VSEN	Output voltage sense pin. This pin receives the auxiliary winding voltage by a resistor divider. This pin also senses the winding voltage to provide the QR operation.
4	ISEN	Current sense pin. The current sense resistor is placed between this pin and the GND pin.
5,6,7,8	DRAIN	Drain of the internal power MOSFET.

## Absolute Maximum Ratings (Note 1)

VCC	-0.3V~26V
ISEN	-0.3V~3.6V
VSEN	-0.3V~V <sub>VCC</sub> +0.3V
Drain	200V
Power Dissipation, @ TA = 25°C SO8	1.1W
Package Thermal Resistance (Note 2)	
SO8, $\theta_{JA}$	150°C/W
SO8, $\theta_{JA}$	60°C/W
Junction Temperature Range	-45°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

## Recommended Operating Conditions (Note 3)

VCC	10V~15.5V
ISEN	0V~1V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 105°C

**Electrical Characteristics**(VCC = 12V (Note 3), T<sub>A</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Power Supply Section</b>						
VCC Turn-on Threshold	V <sub>VCC_ON</sub>		8.5	9.2	10	V
VCC Turn-off Threshold	V <sub>VCC_OFF</sub>		6.9	7.7	8.5	V
VCC OVP Voltage	V <sub>VCC_OVP</sub>		23.5	25	26.5	V
Start up Current	I <sub>ST</sub>	V <sub>VCC</sub> <V <sub>VCC_OFF</sub>	1	2	4.5	μA
Operating Current	I <sub>VCC</sub>	f=300kHz		2.6		mA
Quiescent Current	I <sub>Q</sub>	f=2kHz	290	380	470	μA
Shunt Current in OVP Mode	I <sub>VCC_OVP</sub>	V <sub>VCC</sub> >V <sub>VCC_OVP</sub>	8	16	26	mA
<b>Current Feedback Modulator Section</b>						
Internal Reference Voltage for Output Current	V <sub>REF</sub>		0.41	0.42	0.43	V
<b>ISEN Pin Section</b>						
Current Limit Voltage	V <sub>ISEN_LIM</sub>	V <sub>FBV</sub> <0.4V		0.7		V
		V <sub>FBV</sub> >0.4V	0.9	1	1.1	V
<b>VSEN Pin Section</b>						
VSEN Pin OVP Voltage Threshold	V <sub>VSEN_OVP</sub>		1.40	1.45	1.52	V
Internal Reference Voltage	V <sub>REFV</sub>		1.232	1.25	1.268	V
<b>Integrated Mosfet Section</b>						
Breakdown Voltage	V <sub>BV</sub>	V <sub>GS</sub> =0V, I <sub>DS</sub> =250μA	200	-	-	V
<b>Switching Section</b>						
Max ON Time	T <sub>ON_MAX</sub>			24		μs
Min ON Time	T <sub>ON_MIN</sub>			330		ns
Max OFF Time	T <sub>OFF_MAX</sub>		490	600	660	μs
Min OFF Time	T <sub>OFF_MIN</sub>			300		ns
Maximum Switching Frequency	F <sub>MAX</sub>		265	300	360	kHz
<b>Thermal Section</b>						
Thermal Shutdown Temperature	T <sub>SD</sub>			150		°C

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** θ<sub>JA</sub> is measured in the natural convection at T<sub>A</sub> = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

**Note 3:** Increase VCC pin voltage gradually higher than V<sub>VCC\_ON</sub> voltage then regulated to 12V.

**Block Diagram**

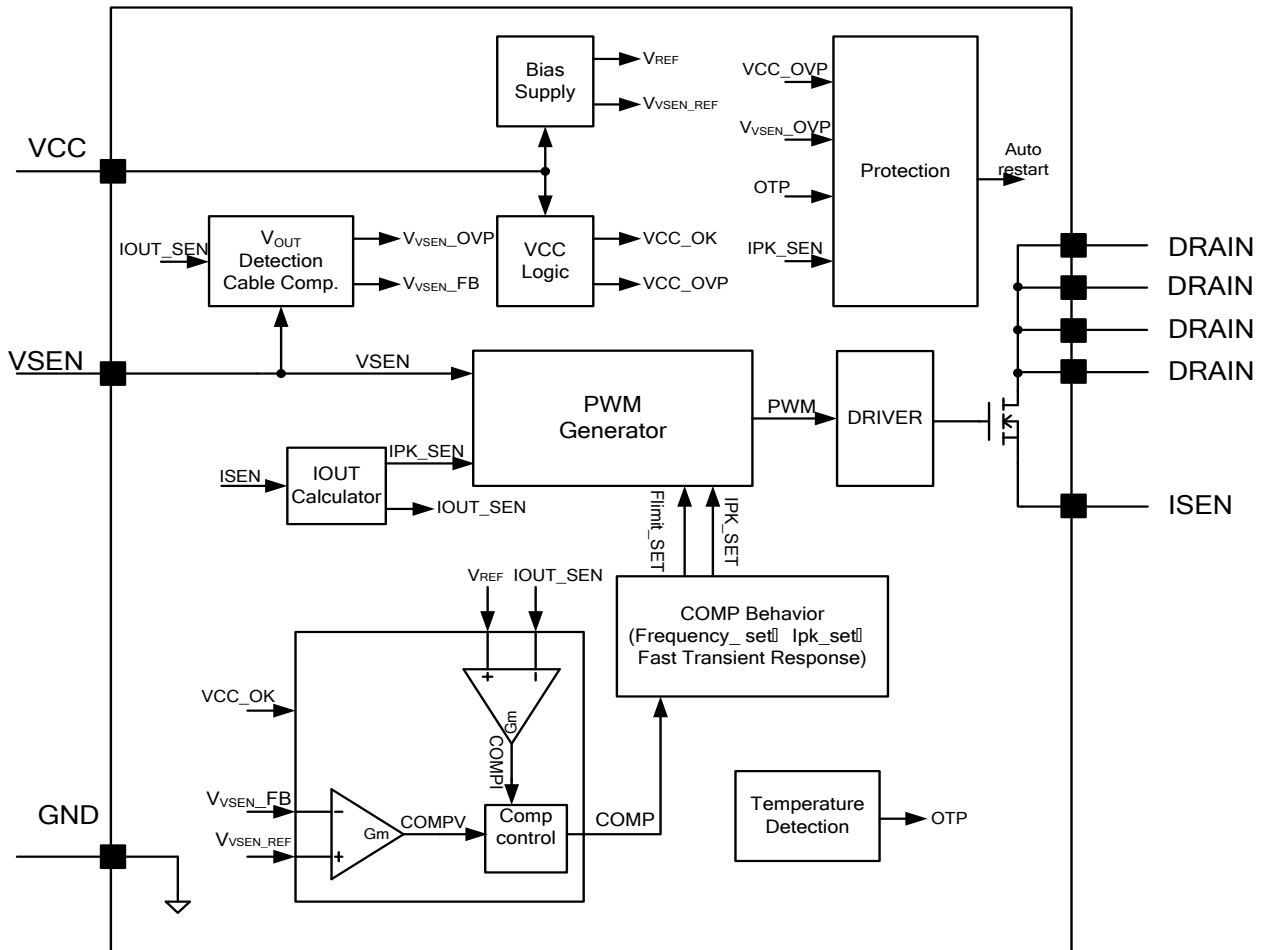


Fig.2 Block Diagram

**Typical Performance Characteristics**

(Test condition: input voltage: 36-60Vdc; output spec: 12Vdc/1A; Ambient temperature:  $25 \pm 5$ ; Ambient Humidity:  $65 \pm 25$  %.)

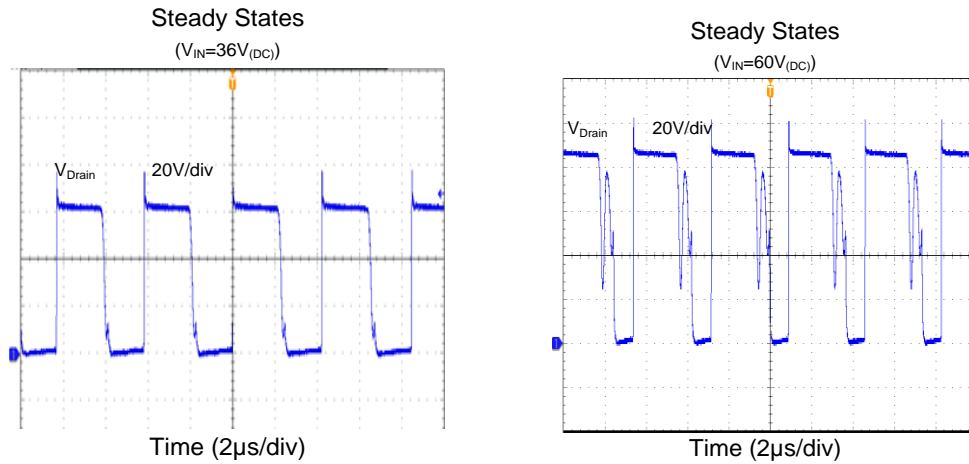


Fig.3 Steady State

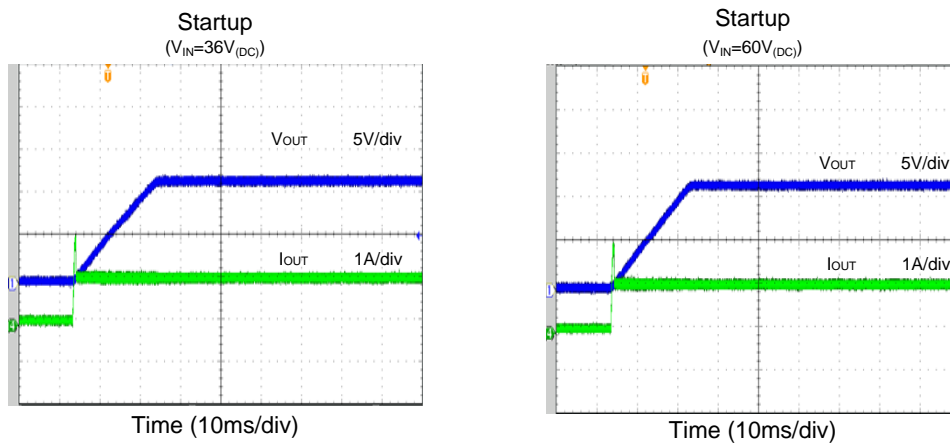


Fig.4 Start Up

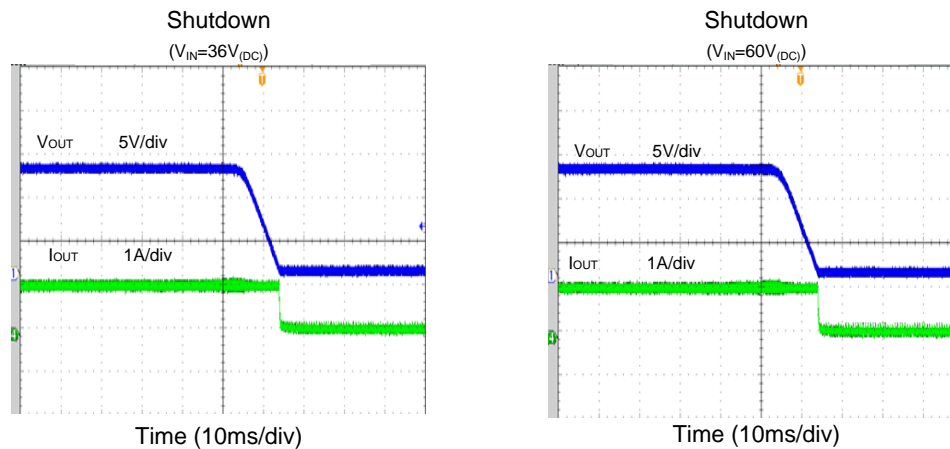


Fig.5 Shut Down

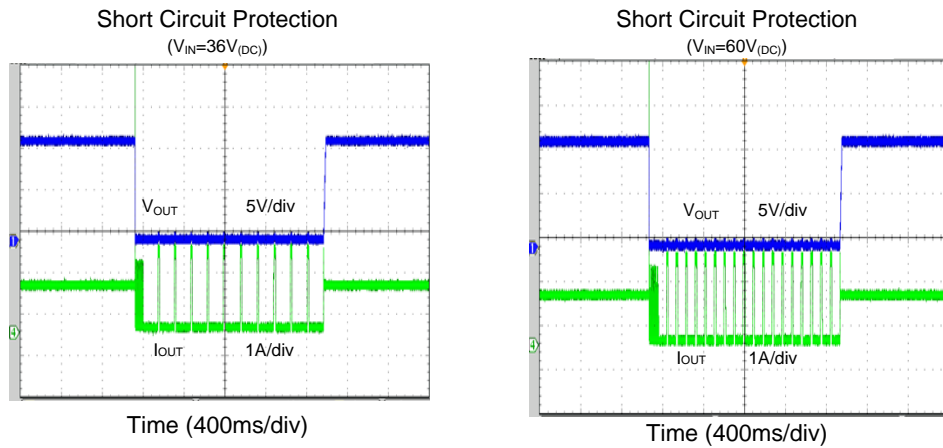


Fig.6 Short Circuit Protection

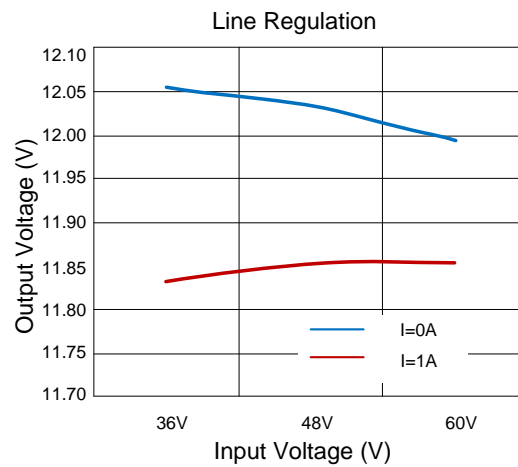


Fig.7 Line Regulation

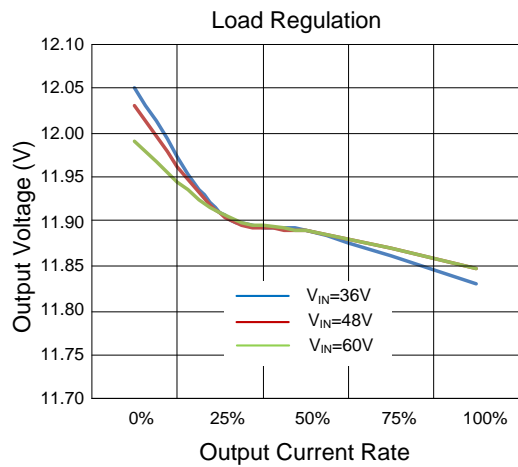


Fig.8 Load Regulation

## Operation

SY22856A is a flyback controller with several features to enhance performance of the converter for telecom adapters and POE applications.

To achieve higher efficiency and better EMI performance, SY22856A drives the Flyback converter in Quasi-Resonant mode. Adaptive PWM/PFM control is provided for highest average efficiency. To minimize the converter size, the maximum switching frequency is up to 300kHz.

The output current is monitored by primary side detection technology, and the maximum output current can be programmed in Over Current Protection and Short Circuit Protection.

SY22856A is available with SO8 package.

## Applications Information

### Start up

When DC input is activated, the input voltage charges the VCC capacitor ( $C_{VCC}$ ) via the startup resistor  $R_{ST}$ . When the voltage on the VCC pin reaches 9.2V typical ( $V_{VCC\_ON}$ ), the controller internal blocks are enabled. Then the SY22856A starts working, energy is being stored and then transferred from the transformer primary to the secondary windings. In the meantime,  $V_{VCC}$  will be pulled down by internal consumption of IC until the auxiliary winding of Flyback transformer supplies enough energy to maintain  $V_{VCC}$  above  $V_{VCC\_OFF}$ .

The whole start up procedure is divided into two sections shown in Fig.9. The startup time  $t_{ST}$  composes of  $t_{STC}$  and  $t_{STO}$ ,  $t_{STC}$  is the  $C_{VCC}$  charged up interval, and  $t_{STO}$  is the output voltage built-up interval. And usually  $t_{STO}$  is much smaller than  $t_{STC}$ .

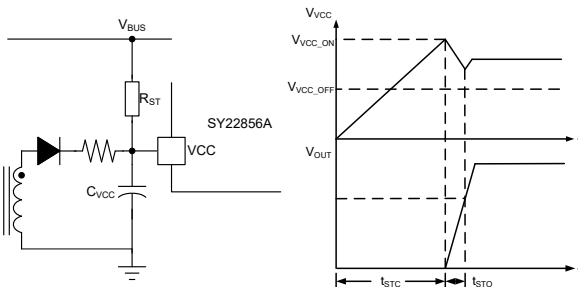


Fig.9 Start up

The startup resistor  $R_{ST}$  and  $C_{VCC}$  can be designed according to below rules:

(a) Preset start-up resistor  $R_{ST}$ , make sure that the current through  $R_{ST}$  is larger than  $I_{ST}$  and smaller than  $I_{VCC\_OVP}$  for the normal start and safe protection.

$$\frac{V_{BUS\_MAX}}{I_{VCC\_OVP}} < R_{ST} < \frac{V_{BUS\_MIN}}{I_{ST}} \quad (1)$$

Where  $V_{BUS}$  is the input rectified voltage.

(b) Select  $C_{VCC}$  to obtain an ideal start up time  $t_{ST}$ .

$$C_{VCC1} = \frac{\left(\frac{V_{BUS\_MIN}}{R_{ST}} - I_{ST}\right) \times t_{ST}}{V_{VCC\_ON}} \quad (2)$$

(c) Select  $C_{VIN}$  to ensure the output voltage is built up at one try.

$$C_{VCC2} = \frac{\frac{V_{VCC\_OFF} + V_{VCC\_Diode}}{N_{AS}} \cdot C_{OUT} \frac{V_{VCC\_ON} + V_{VCC\_OFF}}{2} \cdot I_{VCC}}{(I_{OUT\_LIM} - I_O) \cdot 0.5(V_{VCC\_ON}^2 - V_{VCC\_OFF}^2)} \quad (3)$$

$N_{AS}$  is the turn ratio of auxiliary winding compared to secondary winding,  $C_{OUT}$  is the output capacitance,  $I_{OUT\_LIM}$  is the output current OCP value,  $I_O$  is the output current,  $V_{VCC\_Diode}$  is the forward voltage of the VCC rectifier diode and  $I_{VCC}$  is the operating current of the controller.

(d) The  $C_{VCC}$  should be larger than  $C_{VCC2}$  and smaller than  $C_{VCC1}$ . If the  $C_{VCC}$  is not big enough to build up the output voltage at one time, then increase  $C_{VCC1}$  and decrease  $R_{ST}$ , go back to step (a) and retry until the ideal start up procedure is obtained.

### Shut down

After DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VCC pin,  $V_{VCC}$  will drop down. Once  $V_{VCC}$  is below  $V_{VCC\_OFF}$ , the IC will stop working and  $V_{COMP}$  will be discharged to zero.

## Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Flyback converter.

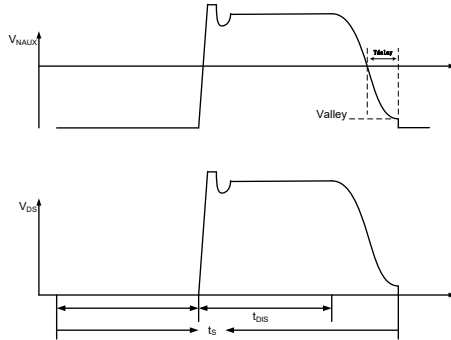


Fig.10 QR mode operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

## Output Voltage Control (CV control)

In order to achieve primary side constant voltage control, the output voltage is detected by the auxiliary winding voltage.

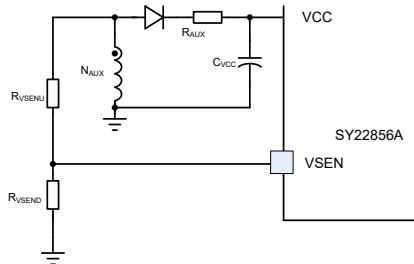


Fig.11 VSEN pin connection

As shown in Fig.12, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D-F}) \times \frac{N_{AUX}}{N_S} \quad (1)$$

$N_{AUX}$  is the turns of auxiliary winding;  $N_S$  is the turns of secondary winding;  $V_{D-F}$  is the forward voltage of the power diode.

At the current zero-crossing point,  $V_{D-F}$  is nearly zero, so  $V_{OUT}$  is proportional with  $V_{AUX}$  exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN-REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (4)$$

Where  $V_{VSEN-REF}$  is the internal voltage reference.

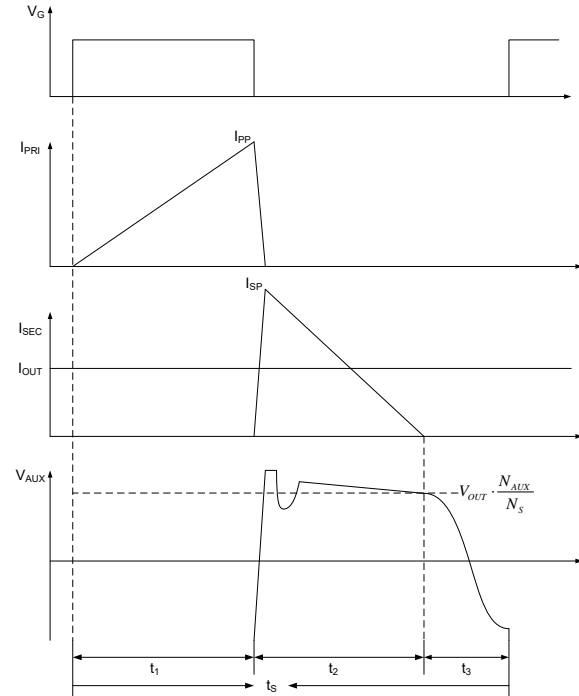


Fig.12 Auxiliary winding voltage waveforms

## Output Current Control (CC control)

The output current is regulated by SY22856A with primary side detection technology, the maximum output current  $I_{OUT-LIM}$  can be set by

$$I_{OUT-LIM} = \frac{k_1 \times V_{REF} \times N_{PS}}{R_S} \quad (5)$$

Where  $k_1$  is the output current weight coefficient;  $V_{REF}$  is the internal reference voltage;  $R_S$  is the current sense resistor.

$k_1$  and  $V_{REF}$  are all internal constant parameters,  $I_{OUT-LIM}$  can be programmed by  $N_{PS}$  and  $R_S$ .

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT}} \quad (6)$$

$K_1$  is set to 0.5

When over current operation or short circuit operation happens, the output current will be limited at  $I_{OUT-LIM}$ . The V-I curve is shown as Fig.13.

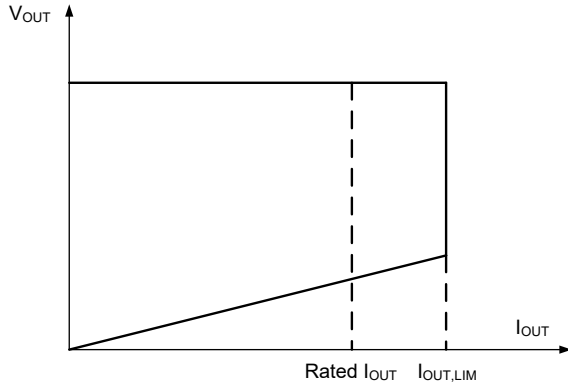


Fig.13 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage  $\Delta V_{ISEN-C}$  is added to ISEN pin during ON time to improve such performance. This  $\Delta V_{ISEN-C}$  is adjusted by the upper resistor of the divider connected to VSEN pin.

$$\Delta V_{ISEN-C} = V_{BUS} \times \frac{N_{AUX}}{N_p} \times \frac{1}{R_{VSENU}} \times k_2 \quad (7)$$

Where  $R_{VSENU}$  is the upper resistor of the divider;  $k_2$  is an internal constant as the modification coefficient.

The compensation is mainly related with  $R_{VSENU}$ , larger compensation is achieved with smaller  $R_{VSENU}$ . Normally,  $R_{VSENU}$  ranges from 50k $\Omega$ ~150k $\Omega$ .

### Short Circuit Protection (SCP)

There are two kinds of situations, one is the valley signal cannot be detected by VSEN, the other is the valley signal can be detected by VSEN.

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. There are two cases, the one is without valley detection, MOSFET cannot be turned on until maximum off time is reached. If MOSFET is turned on with maximum off-time for 64 times continuously which can not detected valley, IC will be shut down and enter into hiccup mode. The other is that IC will be shut down and enter into hiccup mode when  $V_{VCC}$  below  $V_{VCC-OFF}$  within 64 times.

When the output voltage is not low enough to disable valley detection in short condition, SY22856A will operate in CC mode until  $V_{VCC}$  is below  $V_{VCC-OFF}$ .

In order to guarantee SCP function not effected by voltage spike of auxiliary winding, a filter resistor  $R_{AUX}$  is needed.

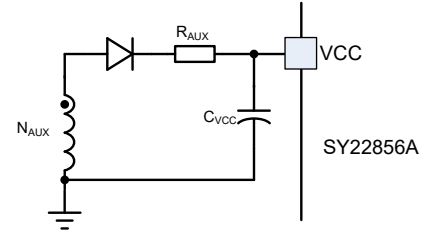


Fig. 14 Filter resistor  $R_{AUX}$

### Output voltage OVP protection

The secondary maximum voltage is limited by the SY22856A. When the VSEN pin signal exceeds 1.45V, SY22856A will stop switching and discharge the VCC voltage. Once  $V_{VCC}$  is below  $V_{VCC-OFF}$ , the IC will shut down and be charged again by HV start up.

### VSEN pin short protection

The SY22856A has a protection against faults caused by a shorted VSEN pin or a shorted pull-down resistor. During start-up, the voltage on the VSEN pin is monitored. In normal situations, the voltage on the VSEN pin reaches the sense protection trigger level. When the VSEN voltage does not reach this level, the VSEN pin is shorted and the protection is activated. The IC stops switching and discharge the VCC voltage. Once  $V_{VCC}$  is below  $V_{VCC-OFF}$ , the IC will shut down and be charged again by HV start up. In order to ensure reliable detection, the pull-down resistor should larger than 2k $\Omega$ .

### ISEN pin short protection

The SY22856A has a protection against faults caused by a shorted ISEN pin. During start-up, the voltage on the ISEN pin is monitored. If the  $V_{ISEN}$  does not exceed 150mV after 4 $\mu$ S, the protection will be triggered. The IC stops switching and discharge the VCC voltage. Once  $V_{VCC}$  is below  $V_{VCC-OFF}$ , the IC will shut down and be charged again by HV start up.

## Power Device Design

## MOSFET and DIODE

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX} = V_{DC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \quad (8)$$

$$V_{D\_R\_MAX} = \frac{V_{DC\_MAX}}{N_{PS}} + V_{OUT} \quad (9)$$

Where  $V_{DC\_MAX}$  is maximum input DC voltage;  $N_{PS}$  is the turns ratio of the Flyback transformer;  $V_{OUT}$  is the rated output voltage;  $V_{D\_F}$  is the forward voltage of secondary power diode;  $\Delta V_S$  is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (10)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (11)$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (12)$$

$$I_{D\_AVG} = I_{OUT} \quad (13)$$

Where  $I_{P\_PK\_MAX}$  and  $I_{P\_RMS\_MAX}$  are maximum primary peak current and RMS current, which will be introduced later.

## Transformer ( $N_{PS}$ and $L_M$ )

$N_{PS}$  is limited by the electrical stress of the power MOSFET:

$$N_{PS} \leq \frac{V_{MOS\_BR\_DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (14)$$

Where  $V_{MOS\_BR\_DS}$  is the breakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle  $t_s$  consists of three parts: current rising time  $t_1$ , current falling time  $t_2$  and quasi-resonant time  $t_3$  shown in Fig.15.

When the operation condition is with minimum input DC RMS voltage and full load, the switching frequency is minimum frequency, the maximum peak current through MOSFET and the transformer happens.

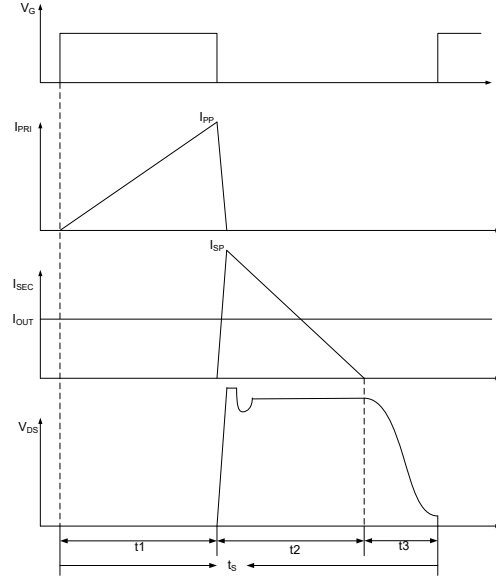


Fig.15 switching waveforms

Once the minimum frequency  $f_{S\_MIN}$  is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select  $N_{PS}$

$$N_{PS} \leq \frac{V_{MOS\_BR\_DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (16)$$

(b) Preset minimum frequency  $f_{S\_MIN}$

(c) Compute inductor  $L_M$  and maximum primary peak current  $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}} \quad (17)$$

$$L_m = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} \quad (18)$$

Where  $C_{Drain}$  is the parasitic capacitance at drain of MOSFET;  $\eta$  is the efficiency;  $P_{OUT}$  is rated full load power

(d) Compute current rising time  $t_1$  and current falling time  $t_2$

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS}} \quad (19)$$

$$t_2 = \frac{L_m \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (20)$$

$$t_s = \frac{1}{f_{S\_MIN}} \quad (21)$$

(e) Compute primary maximum RMS current  $I_{P\_RMS\_MAX}$  for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_s}} \quad (22)$$

(f) Compute secondary maximum peak current  $I_{S\_PK\_MAX}$  and RMS current  $I_{S\_RMS\_MAX}$  for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (23)$$

$$I_{S\_RMS\_MAX} = \frac{\sqrt{3}}{3} N_{PS} \cdot I_{P\_PK\_MAX} \cdot \sqrt{\frac{t_2}{t_s}} \quad (24)$$

### Transformer design ( $N_P$ , $N_S$ , $N_{AUX}$ )

The design of the transformer is similar with ordinary Flyback transformer. The parameters below are necessary:

Necessary parameters	
Turns ratio	$N_{PS}$
Inductance	$L_M$
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area  $A_e$ .

(b) Preset the maximum magnetic flux  $\Delta B$

$$\Delta B = 0.22 \sim 0.26 T$$

(c) Compute primary turn  $N_P$

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (25)$$

(d) Compute secondary turn  $N_S$

$$N_S = \frac{N_P}{N_{PS}} \quad (26)$$

(e) compute auxiliary turn  $N_{AUX}$

$$N_{AUX} = N_S \times \frac{V_{VCC}}{V_{OUT}} \quad (27)$$

Where  $V_{VCC}$  is the working voltage of VCC pin (11V~15V is recommended).

(f) Select an appropriate wire diameter

With  $I_{P\_RMS\_MAX}$  and  $I_{S\_RMS\_MAX}$ , select appropriate wire to make sure the current density ranges from 4A/mm<sup>2</sup> to 10A/mm<sup>2</sup>.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to (a) and redesign the transformer until the ideal transformer is achieved.

### RCD snubber for MOSFET

The power loss of the snubber  $P_{RCD}$  is evaluated first

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (28)$$

Where  $N_{PS}$  is the turns ratio of the Flyback transformer;  $V_{OUT}$  is the output voltage;  $V_{D\_F}$  is the forward voltage of the power diode;  $\Delta V_S$  is the overshoot voltage clamped by RCD snubber;  $L_K$  is the leakage inductor;  $L_M$  is the inductance of the Flyback transformer;  $P_{OUT}$  is the output power.

The  $R_{RCD}$  is related with the power loss:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (29)$$

The  $C_{RCD}$  is related with the voltage ripple of the snubber  $\Delta V_{C\_RCD}$ :

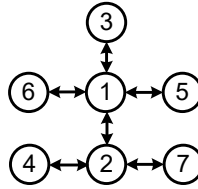
$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} \cdot f_S \cdot \Delta V_{C\_RCD}} \quad (30)$$

## Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



- Ground ①: ground of BUS capacitor.
- Ground ②: ground of bias supply capacitor.
- Ground ③: ground node of auxiliary winding.
- Ground ④: ground node of divider resistor.
- Ground ⑤: primary ground node of Y capacitor.
- Ground ⑥: ground node of current sample resistor.
- Ground ⑦: ground of IC GND.

- (d) bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.
- (e) Loop of ‘Source pin – current sample resistor – GND pin’ should be kept as small as possible.
- (f) The resistor divider connected to VSEN pin is recommended to be put beside the IC.

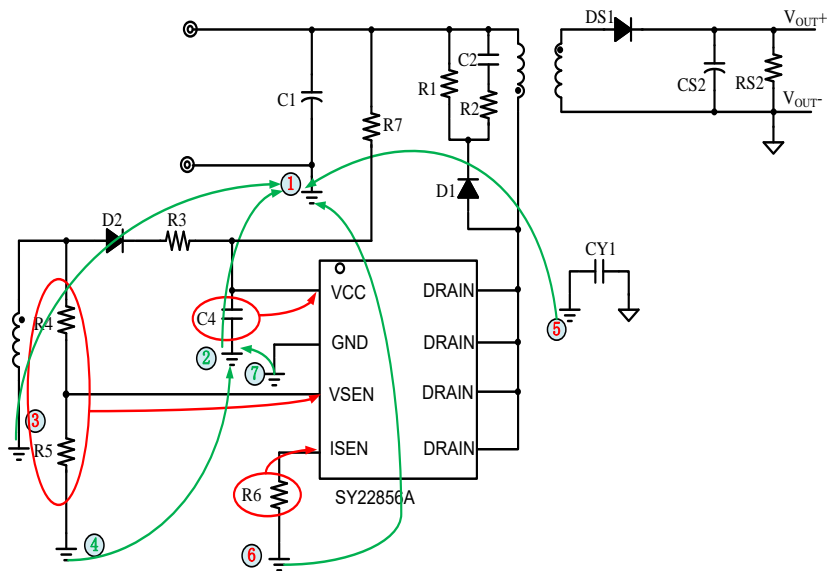


Fig.16 recommended layout

## Design Example

A design example of typical application is shown below step by step.

### #1. Identify design specification

Design Specification			
V <sub>DC</sub>	36V~60V	V <sub>OUT</sub>	12V
I <sub>OUT</sub>	1A	η	82%

### #2. Transformer design (N<sub>PS</sub>, L<sub>M</sub>)

Refer to Power Device Design

Conditions			
V <sub>DC,MIN</sub>	36V	V <sub>DC-MAX</sub>	60V
ΔV <sub>S</sub>	60V	V <sub>MOS-(BR)DS</sub>	200V
P <sub>OUT(max)</sub>	12W	V <sub>D,F</sub>	1V
C <sub>Drain</sub>	60pF	f <sub>S-MIN</sub>	230kHz

#### (a) Compute turns ratio N<sub>PS</sub> first

$$\begin{aligned}
 N_{PS} &\leq \frac{V_{MOS-(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D,F}} \\
 &= \frac{200V \times 0.9 - 60V - 60V}{12V + 1V} \\
 &= 4.6
 \end{aligned}$$

N<sub>PS</sub> can be set to

$$N_{PS} = 2$$

#### (b) f<sub>S,MIN</sub> is preset

$$f_{S\_MIN} = 230\text{kHz}$$

#### (c) Compute inductor L<sub>M</sub> and maximum primary peak current I<sub>P,PK,MAX</sub>

$$\begin{aligned}
 I_{P\_PK\_MAX} &= \frac{2P_{OUT}}{\eta \times \left( V_{DC\_MIN} \frac{N_{PS} V_O}{N_{PS} V_O + V_{DC\_MIN}} \right)} + \pi \cdot \sqrt{\frac{2P_{OUT}}{\eta} \cdot C_{drain} \cdot f_{S-MIN}} \\
 &= \frac{2 \times 12W}{0.82 \times \left( 36V \times \frac{2 \times 12V}{2 \times 12V + 36V} \right)} + \pi \cdot \sqrt{\frac{2 \times 12}{0.82} \times 60 \times 10^{-12} \times 230 \times 10^3} \\
 &= 2.093A
 \end{aligned}$$

$$L_m = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}}$$

$$= \frac{2 \times 12W}{0.82 \times (2.1A)^2 \times 230KHz}$$

$$= 29\mu H$$

Set:  $L_m = 29\mu H$

(d) Compute current rising time  $t_1$  and current falling time  $t_2$

$$t_1 = \frac{L_m \times I_{P\_PK\_MAX}}{V_{DC\_MIN}} = \frac{29\mu H \times 2.093A}{36V} = 1.685\mu s$$

$$t_2 = \frac{L_m \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} = \frac{29\mu H \times 2.093A}{2 \times (12V + 1V)} = 2.334\mu s$$

$$t_3 = \pi \times \sqrt{L_m \times C_{Drain}} = \pi \times \sqrt{29\mu H \times 60pF} = 0.131\mu s$$

$$t_s = t_1 + t_2 + t_3 = 1.685\mu s + 2.334\mu s + 0.131\mu s = 4.15\mu s$$

(e) Compute primary maximum RMS current  $I_{P\_RMS\_MAX}$  for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_s}} = \frac{\sqrt{3}}{3} \times 2.093A \times \sqrt{\frac{1.685\mu s}{4.15\mu s}} = 0.77A$$

(f) Compute secondary maximum peak current  $I_{S\_PK\_MAX}$  and RMS current  $I_{S\_RMS\_MAX}$  for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2 \times 2.01A = 4.02A$$

$$I_{S\_RMS\_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_s}} = 2 \times \frac{\sqrt{3}}{3} \times 2.093A \times \sqrt{\frac{2.334\mu s}{4.15\mu s}} = 1.812A$$

#3. Select secondary power diode

Refer to Power Device Design

Known conditions at this step			
$V_{DC\_MAX}$	60V	$N_{PS}$	1
$V_{OUT}$	12V	$V_{D\_F}$	1V
$\Delta V_S$	60V		

Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX} = \frac{V_{DC\_MAX}}{N_{PS}} + V_{OUT}$$

$$= \frac{60V}{2} + 12V$$

$$= 42V$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2 \times 2.093A = 4.186A$$

$$I_{D\_AVG} = 1A$$

#4. Set current sense resistor to achieve ideal output current

Known conditions at this step			
$N_{PS}$	1		
$V_{REFMAX}$	1V	$I_{OUT,LIM}$	1.25A

The current sense resistor is

$$R_s = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT}}$$

$$= \frac{0.5 \times 0.42V \times 2}{1.3A}$$

$$= 0.32\Omega$$

Set  $R_s$

$$R_s = 0.51\Omega \square 0.68\Omega$$

#5. Set  $V_{SEN}$  pin

Refer to  $V_{OUT}$

First identify  $R_{VSEN}$  need for line regulation.

Parameters Designed			
$R_{VSEN}$	51k $\Omega$		

Then compute  $R_{VSEND}$

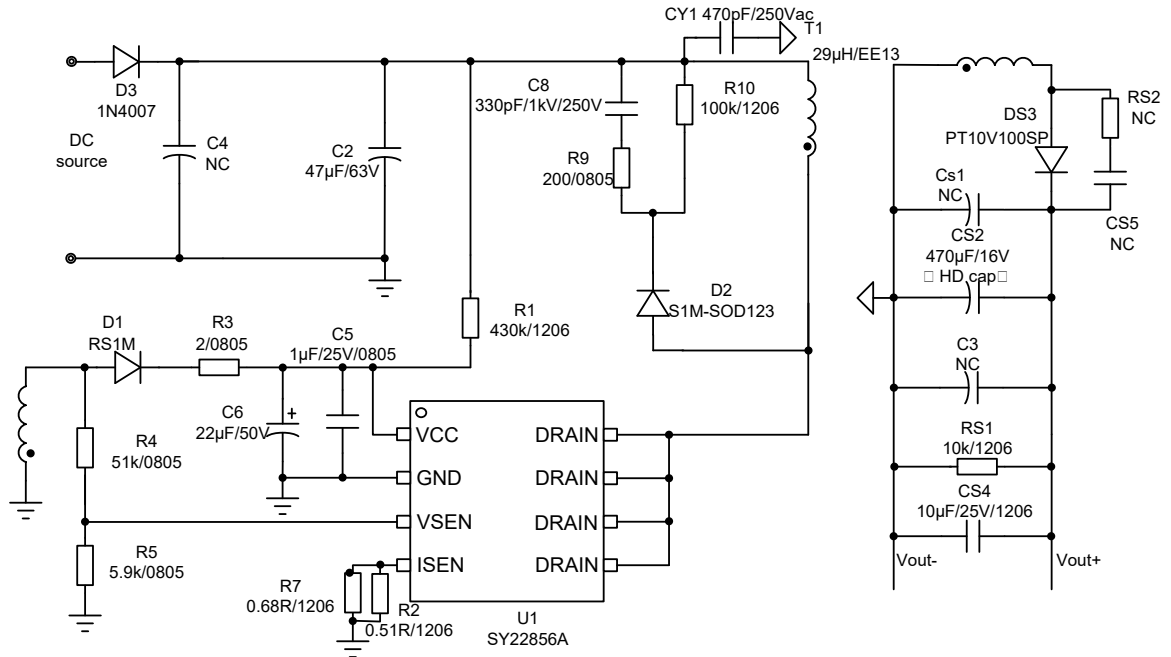
Conditions			
$V_{OUT}$	12V	$V_{VSEN\_REF}$	1.25V
$R_{VSEN}$	51k $\Omega$	$N_s$	6
$N_{AUX}$	6		

$$R_{VSEND} = \frac{R_{VSEN}}{\frac{V_{OUT} N_{AUX}}{V_{VSEN\_REF} N_s} - 1} = \frac{51K}{\left(\frac{12V \times 6}{1.25V \times 6} - 1\right)} = 5.9K$$

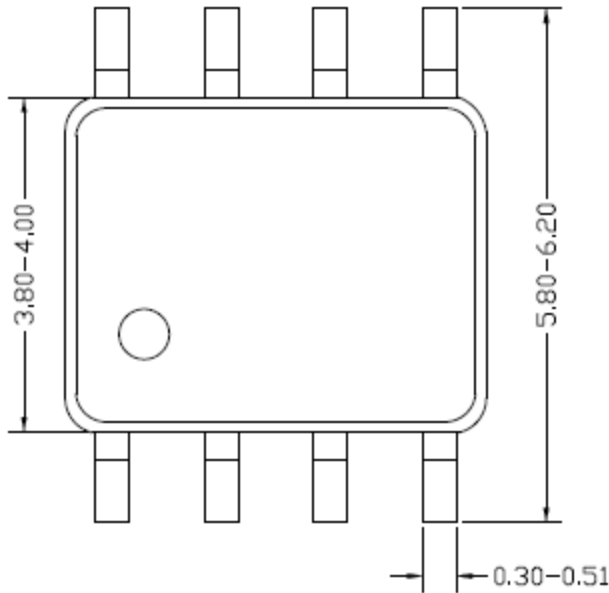
Set  $R_{VSEND}$

$$R_{VSEND} = 5.9k\Omega$$

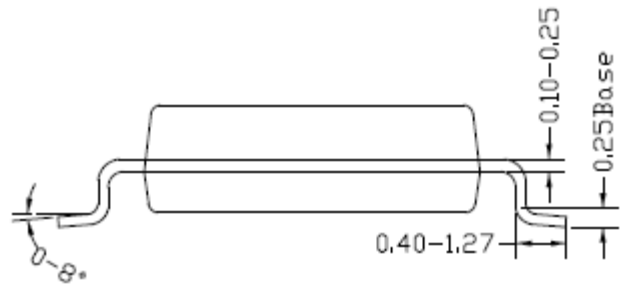
#8. Final result



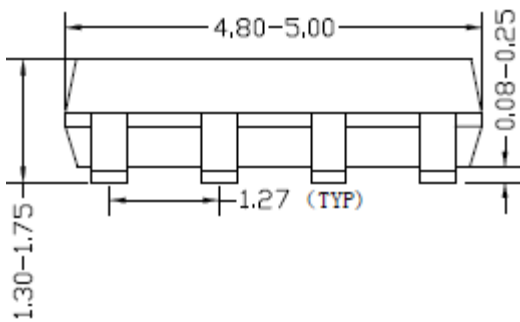
**SO8 Package outline & PCB layout design**



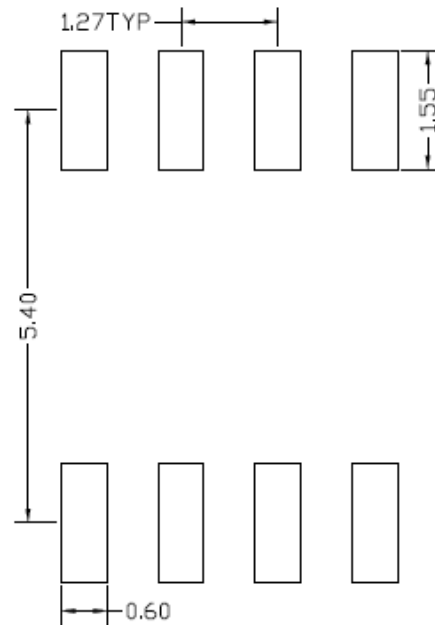
**Top view**



**Side view**



**Front view**

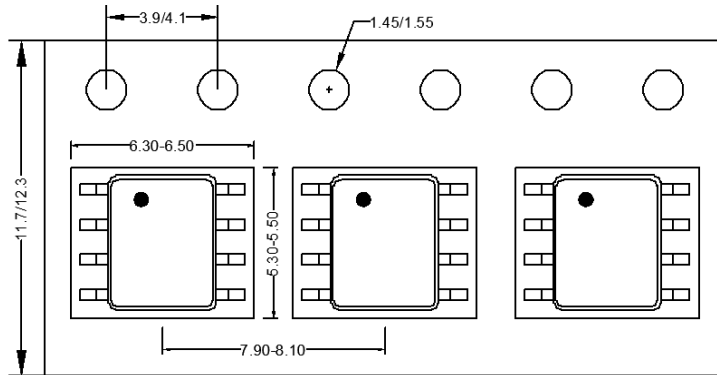


**Recommended Pad Layout  
(Reference only)**

**Notes: All dimension in millimeter and exclude mold flash & metal burr.**

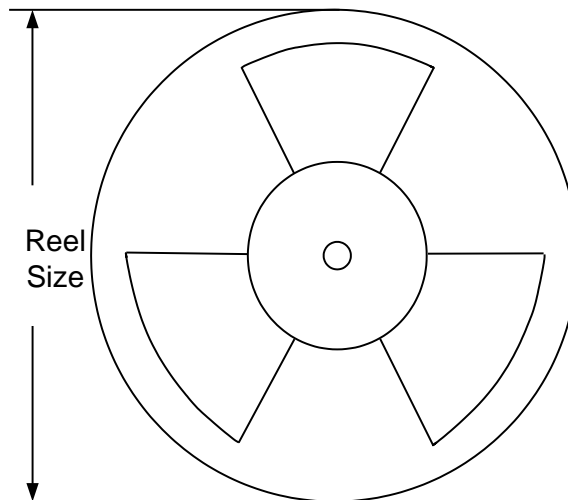
## Taping & Reel Specification

### 1. Taping orientation for packages (SO8)



Feeding direction →

### 2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

### 3. Others: NA



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