SA33101

36V Synchronous Buck Controller for Automotive Application

General Description

The SA33101 is a synchronous step-down controller that can generate output voltages from 0.7V to 5.3V by driving the external high/low side NMOS. The user-settable switching frequency can be adjusted from 250kHz to 1.0MHz through an external resistor, and can be synchronized with an external clock. The device supports three operating modes: PWM mode, PLL PWM mode and PFM mode. These modes can be selected under the conditions of the MODE pin. In particular, the automatic PFM mode increases efficiency under light load conditions.

The SA33101 has the protection functions including cycle by cycle current limit function, UVD (Under Voltage Detection), OVD (Over Voltage Detection), OVP (Over Voltage Protection), SCP (Short Circuit Protection) and thermal shut down. Also, the PGOOD (Power Good) pin provides the status of output.

The CLKOUT Pin of SA33101 is equipped with phase shift 180°function to meet the multiphase application. For EMI reduction purpose, spread-spectrum clock generator for diffused oscillation frequency at the PWM operation is available.

The SA33101 is available in SSOP18E package.

Ordering Information

SA33101□(□□□)

Package Code

Optional Spec Code

Ordering Number	Package Type	Note
SA33101HSP	SSOP18E	------

Features

- AEC-Q100-Grade 1 -40℃~125℃
- Wide Input Voltage Ranges from 4.0 V to 36V
- Start-up Input Voltage: 4.5V
- Output Voltage Range from 0.7V to 5.3V
- Fold Back Reference Voltage: 640mV±1%
- Adjustable Switching Frequency: 250kHz to 1MHz
- Spread Frequency Function
- Adjustable Soft-start Time
- Pre-bias Start-up
- Output Voltage Abnormal Detection, Shows on PGOOD Pin, UVD/OVD
- Cycle by Cycle Current Limit Protection
- Thermal Shut down When Tj>160℃
- Reliable Protection: SOP/UVD/OVD/OVP/OTP
- Package: SSOP18E

Applications

- DC/DC Converter
- Power Module
- Automotive Power Supply Unit
- Power Source for Control Units Including EV
- Inverter and Charge Controller

Typical Applications

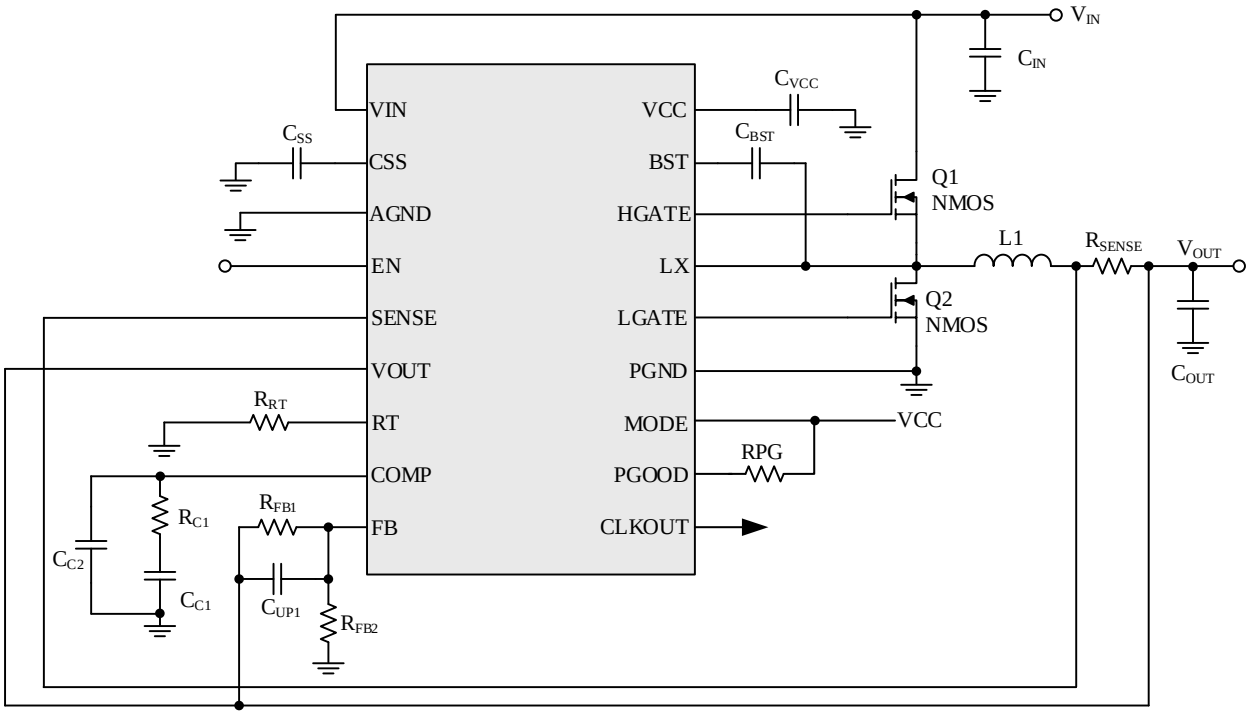
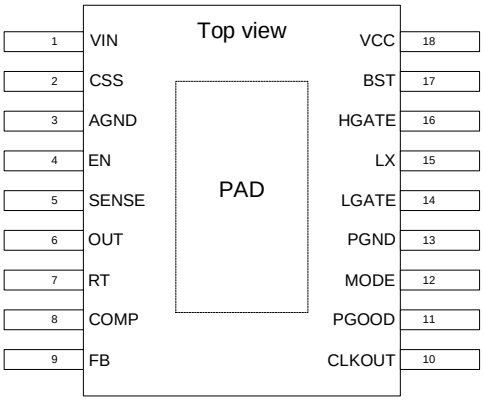


Fig.1 Schematic Diagram (BUCK Topology)

Pinout (top view)



(SSOP18E)

Top Mark: **FGR*xyz***, **(**Device code: FGR; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Description	
VIN	1	Power supply pin.
CSS	2	Soft-start programming pin. An external capacitor connected from CSS pin to AGND pin to programming soft-start time.
AGND	3	Analog GND pin.
EN	4	Chip enable pin, logic high enable.
SENSE	5	Positive input to the inductor current sense amplifier.

VOUT	6	Negative input to the inductor current sense amplifier.
RT	7	Switching frequency adjustment pin. $R_{RT}(k\Omega) = 41993 \times f_{sw}(kHz)^{\wedge} (-1.039)$
COMP	8	Output of the error amplifier. An external RC network connected between COMP and AGND compensates the regulator feedback loop.
FB	9	Feedback pin for output voltage regulation. The value of V_{OUT} can be calculated by $V_{OUT}=0.64(R_{top}+R_{bot})/ R_{bot}$.
CLKOUT	10	Clock output pin.
PGOOD	11	Power good, open drain output.
MODE	12	Mode set pin.
PGND	13	Power ground pin.
LGATE	14	Output of the low side gate driver. Connect directly to the gate of the low side MOSFET.
LX	15	Switching node pin.
HGATE	16	Output of the high side driver. Connect directly to the gate of the high side MOSFET.
BST	17	Bootstrap pin.
VCC	18	Internal LDO output. Connect a capacitor to ground.
	Exposed pad	Exposed pad. The exposed pad is on the bottom side of the device. It is not connected to SGND or PGND electrically. Connect the exposed pad to SGND and PGND during PCB layout for better thermal performance.

Block Diagram

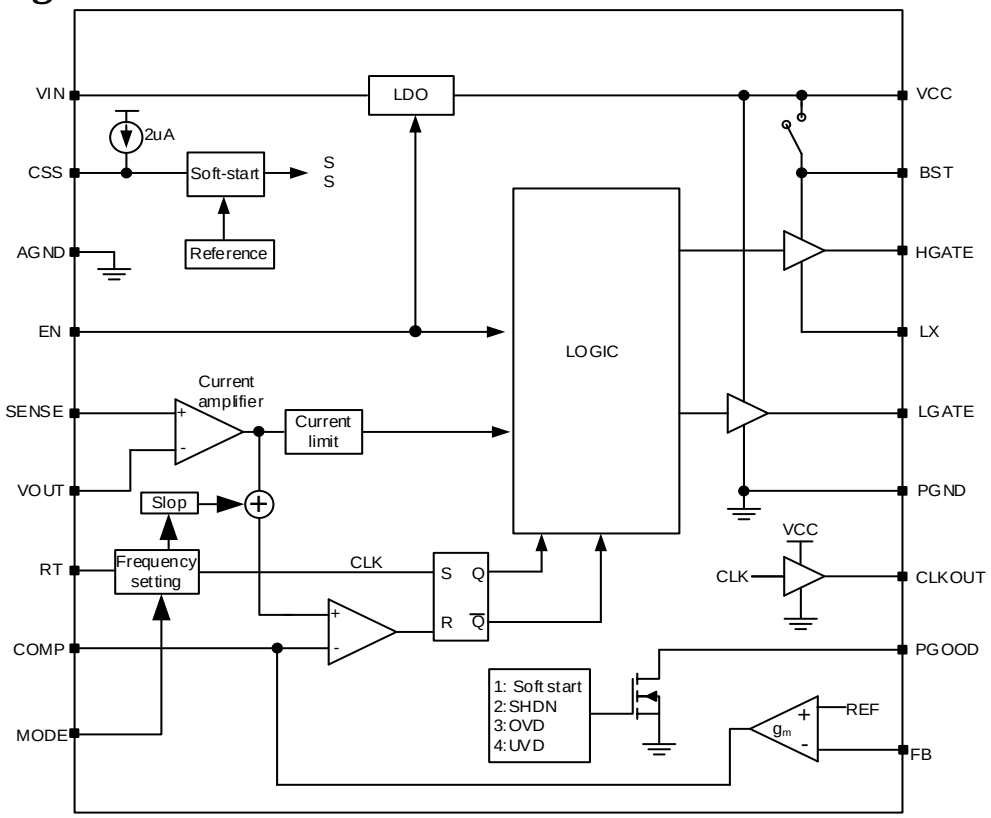


Fig.2 Detailed Block Diagram

Absolute Maximum Ratings (Note 1)

VIN, EN, LX, VOUT, SENSE, CSS, FB ---------- -0.3V to 42V
COMP, MODE, PGOOD, CLKOUT, VCC, VBST-VLX, LGATE ---------- -0.3V to 6V
RT ---------- -0.3V to 10V
HGATE ---------- LX-0.3 to BST
Dynamic LX to GND Voltage in 20ns Duration---------- -5V to 42V
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 32℃/W
θ_{JC_TOP}---------- 8℃/W
Junction Temperature Range ---------- -40℃~ 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -55℃ to 150℃
Human Body Mode(HBM) ---------- ±2KV
Charge Device Mode corner PIN（1，9，10， and 18)(CDM) ---------- ±750V
Charge Device Mode other PIN(CDM) ---------- ±500V

Recommended Operating Conditions (Note 3)

V_{IN} ---------- 4V to 36V
V_{OUT} ---------- 0.7V to 5.3V
Ambient Temperature Range ---------- -40℃ to 125℃

Electrical Characteristics

(-40℃≤T_J≤125℃, VIN = 10V, C_{VIN}=1uF, C_{REF}=100nF, R_{RC}=100k, C_{RC}=330pF unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Input & VCC Supply						
Start-up Voltage	V_{START}			4	4.5	V
VCC Regulate Voltage	Vcc	V_{FB}=0.672V	4.9	5.1	5.3	V
Standby Current	$I_{STANDBY}$	V_{IN}=12V, EN=0		3	20	μA
VIN Supply Current at PWM without Switching	I_{VIN1}	V_{FB}=0.672V, MODE=5V, V_{OUT}=SENSE=LX=5V		1.8	3.5	mA
VIN Supply Current at PFM without Switching	I_{VIN2}	V_{FB}=0.672V, MODE=0V, V_{OUT}=SENSE=LX=5V		192	280	μA
VCC UVLO Threshold	V_{UVLO2}	V_{CC} Rising	3.8	4	4.2	V
	V_{UVLO1}	V_{CC} Falling	3.1	3.3	3.5	V
Fold Back						
FB Reference	V_{FB}	Ta=25℃	0.6336	0.64	0.6464	V
		-40℃≤Ta≤125℃	0.6272		0.6528	V
FB Pin OVD Threshold	V_{FBOVD1}	V_{FB} Rising	0.66	0.694	0.72	V
	V_{FBOVD2}	V_{FB} Falling	VFB+0.005	0.664	0.7	V
FB Pin UVD Threshold	V_{FBUVD1}	V_{FB} Rising	0.58	0.613	0.634	V
	V_{FBUVD2}	V_{FB} Falling	0.55	0.578	0.6	V
FB Pin Current	I_{FBH}	V_{FB}=0.64V	-0.1		0.1	μA
	I_{FBL}	V_{FB}=0V	-0.25		0	μA

Switching Frequency/T_{on_min}/T_{off_min}						
Oscillation Frequency	f_{OSC0}	RT=135kohm	218	250	282	kHz
	f_{OSC1}	RT=32kohm	945	1080	1215	kHz
Minimum T_{off}	T_{off_min}	From falling edge of HGATE to falling edge of LGATE	175		300	nS
Minimum T_{on}	T_{on_min}			100	135	nS
Synchronizing Frequency	F_{SYNC}	F_{OSC} as the reference	f_{OSC}x0.5		f_{OSC}x1.5	
			250		1000	kHz
Soft Start						
Soft -start Time	T_{SS1}	CSS OPEN	0.35		1.0	mS
	T_{SS2}	Css=4.7nF	1.3		2.3	mS
Charge Current for SS	I_{TSS}	CSS=0V	1.7	2	2.3	μA
CSS Voltage at The End of Soft Start	V_{SSEND}		0.62		0.72	V
Discharge Resistance Integrate in CSS Pin	R_{DIS_CSS}	V_{IN}=12V, EN=0V, CSS=3V	2	4.2	5.5	kΩ
Internal GATE Driver MOS						
On Resistance of HGATE Pull Up	$R_{UPHGATE}$	BST-LX=5V, I_{HGATE}=-100mA		2.5	5	Ω
On Resistance of HGATE Pull Low	$R_{DOWNHGATE}$	BST-LX=5V, I_{HGATE}=100mA		1.5	3.5	Ω
On Resistance of LGATE Pull Up	$R_{UPLGATE}$	VCC-PGND=5V, I_{LGATE}=-100mA		4	7	Ω
On Resistance of LGATE Pull Low	$R_{DOWNLGATE}$	VCC-PGND=5V, I_{LGATE}=100mA		1.5	3.5	Ω
Current Limit						
Current Limit Threshold	V_{ILIMIT}	SENSE-VOUT	58	70	82	mV
Reverse Current Limit Threshold	$V_{IREVLIMIT}$	SENSE-VOUT	-47	-35	-23	mV
MOS Fault Protection						
LX Short to GND Protection Threshold	$V_{LXSHORTL}$	LX short to GND	0.37		0.55	V
LX Short to VIN Protection Threshold	$V_{LXSHORTH}$	LX short to VIN	0.37		0.55	V
EN/MODE/CLKOUT/PGOOD Threshold						
EN High Threshold	V_{ENH}		1.3			V
EN Low Threshold	V_{ENL}				0.9	V
EN High Input Current	I_{ENH}	EN=44V	0.2		5	μA
EN Low Input Current	I_{ENL}	EN=0V	-1	0	1	μA
Highest MODE High Threshold	V_{MODEH}	Mode high voltage range	0.5		1.1	V
MODE Hysteresis Voltage	V_{MODEL}	Hysteresis voltage of V_{MODEH} and V_{MODEL}	10	55	110	mV
MODE High Input Current	I_{MODEH}	MODE=6V	1		6.6	μA
MODE Low Input Current	I_{MODEL}	MODE=0V	-1	0	1	μA
CLKOUT High Voltage	$V_{CLKOUTH}$	CLKOUT	4.7		VCC	V
CLKOUT Low Voltage	$V_{CLKOUTL}$	CLKOUT	0		0.1	V

PGOOD Pin Off Voltage	V_{PGOFF}	VIN=4V, PG=1mA		0.26	0.54	V
PGOOD Pin Off Current	I_{PGOFF}	VIN=12V, EN=0, PG=6V	-0.1	0	0.1	μA
Loop Amplify						
Loop Amplify	gm (EA)	COMP=1.5V	0.5	1	1.55	mS
Protection						
Cross Zero Current Threshold	V_{XZ}		-8.5	-3.9	0.5	mV
Vout Over Voltage Threshold	V_{OUTOV}		5.7	5.9	6.2	V
Thermal Shut Down	T_{TSD}	Ta Rising	150	160		℃
Thermal Shut Down Recovery	T_{TSR}	Ta Falling	125	140		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

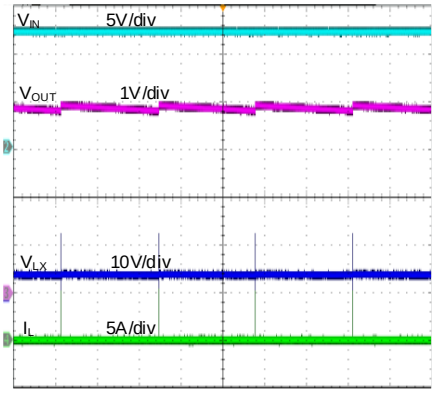
Note 3: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 4: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

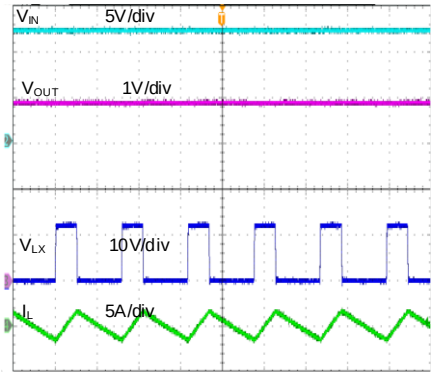
V_{IN}=12V, V_{OUT}=3.8V, L=2.2uH, C_{OUT}=200uF

Steady States
(I_{OUT}=0A, PFM)



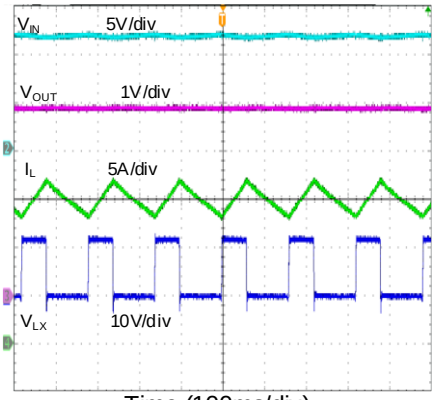
Time (100ms/div)

Steady States
(I_{OUT}=0A, PCCM)



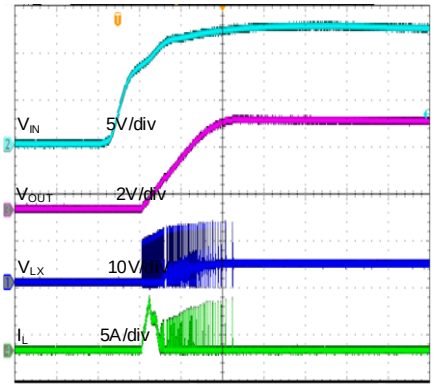
Time (2us/div)

Steady States
(I_{OUT}=15A, PFM)



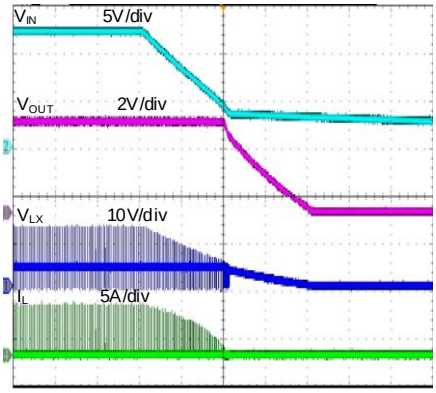
Time (100ms/div)

Start Up
(I_{OUT}=0A,PFM)



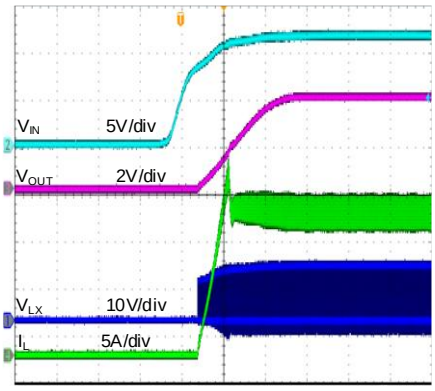
Time (800us/div)

Shutdown
(I_{OUT}=0A, PFM)



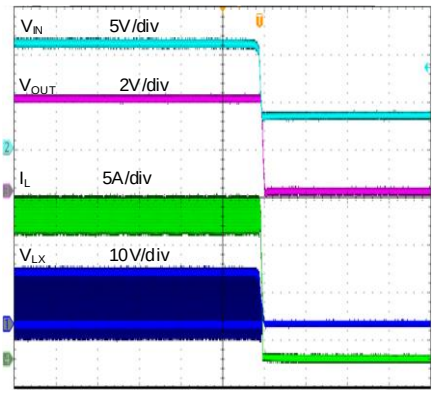
Time (100ms/div)

Start Up
(I_{OUT}=15A, PFM)



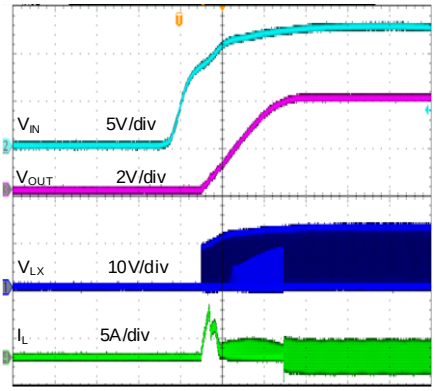
Time (800us/div)

Shutdown
(I_{OUT}=15A, PFM)



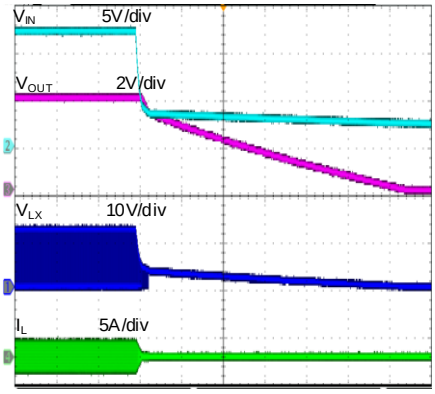
Time (800us/div)

Start Up
(I_{OUT}=0A, FCCM)



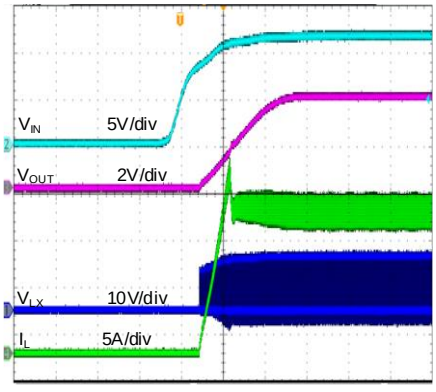
Time (800us/div)

Shutdown
(I_{OUT}=0A, FCCM)



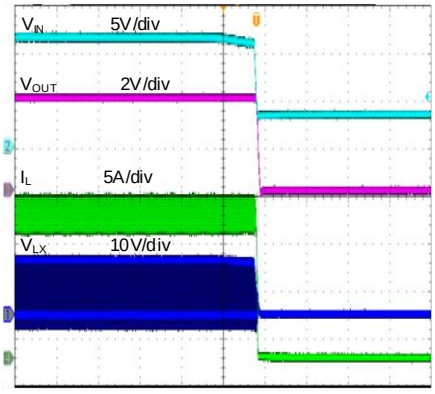
Time (100ms/div)

Start Up
(I_{OUT}=15A, FCCM)



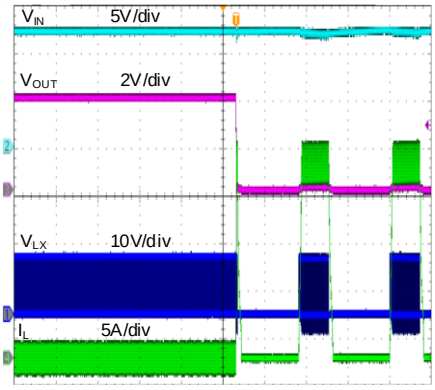
Time (800us/div)

Shutdown
(I_{OUT}=15A, FCCM)



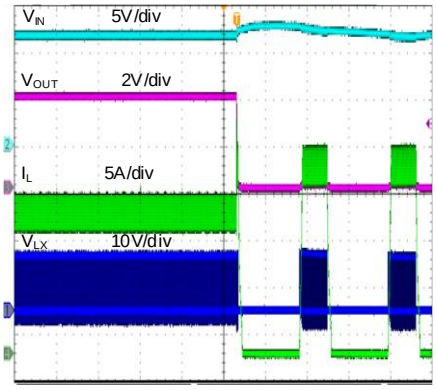
Time (800us/div)

Short Output Protection
(I_{OUT}=0A)



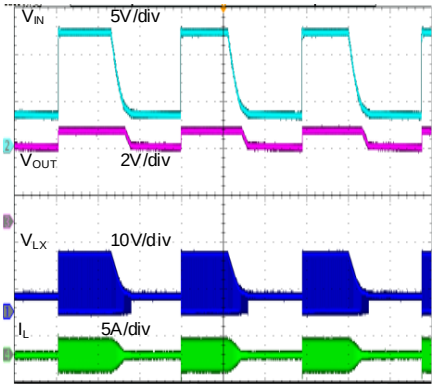
Time (2ms/div)

Short Output Protection
(I_{OUT}=15A)



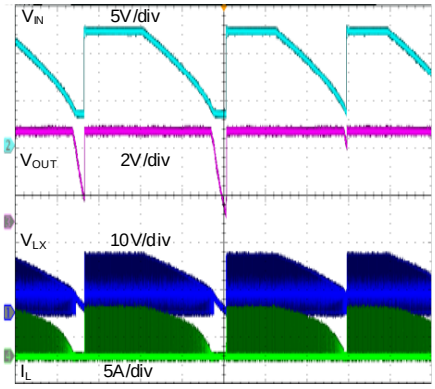
Time (2ms/div)

Pre-bias Function
(I_{OUT}=0A,FCCM)



Time (2ms/div)

Pre-bias Function
(I_{OUT}=3A,FCCM)



Time (2ms/div)

Operation Principle

The SA33101 is a fixed frequency and current mode controller for Buck topology.

Mode PIN Function

The operation mode of SA33101 can be changed among PLL mode, PWM mode and PFM mode by adding different signal to the MODE pin: Connect MODE below MODEL, the IC will operate in PFM mode; Connect MODE above MODEH, the IC will operate in PWM mode; Connect a clock to MODE pin, the IC will operate in PLL mode and switching frequency will follow the frequency of external clock.

PLL Mode:

When an external clock is added to the MODE pin, the IC will operate in PLL mode with an average switching frequency equal to the frequency of the external clock. Spread frequency function is also enabled for better EMC. When the external clock is too high or too low, the SA33101 will set the clamp switch frequency based on RT. It is recommended that the external clock be set between 0.5×F_RT and 1.5×F_RT.

PWM Mode:

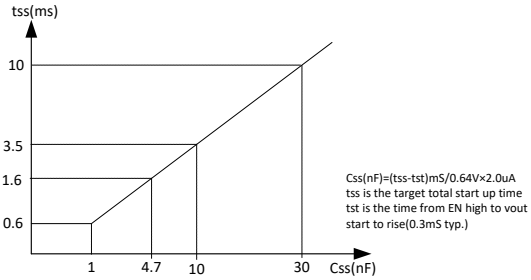
When the connection mode is higher than MODEH, select PWM mode. In PWM mode, the switching frequency is determined only by the RT resistance even at light load, the output voltage ripple is reduced.

PFM Mode

When connection mode is under MODEL, select PFM mode. In PFM mode, the SA33101 operates in CCM under heavy load and DCM under light load. The operating mode of CCM and DCM depends on the inductive current. When IL decreases to zero, the SA33101 will enter the DCM mode. When IL is greater than zero, the SA33101 will enter the CCM mode. In DCM, if the inductive current disappears for a long time, the IC will enter standby mode to save the working current of the IC.

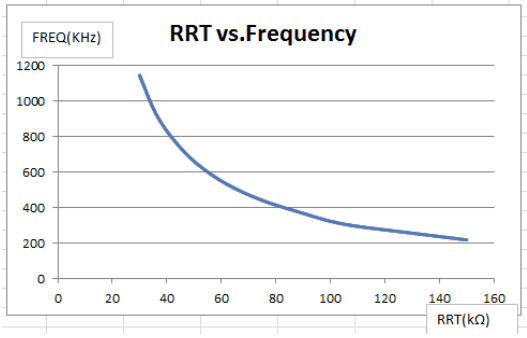
CSS PIN Function:

Connect an external CSS ceramic capacitor between CSS pin and AGND pin to adjust the soft-start time. The SA33101 builds in a min soft-start time curve, which is 630us typical. This curve will work when setting time of external ceramic capacitor is shorter than 630us to avoid over shot. The output current from CSS pin is 2uA typical, select different capacitor to change the soft start time. The curve Css vs. Tss is below:



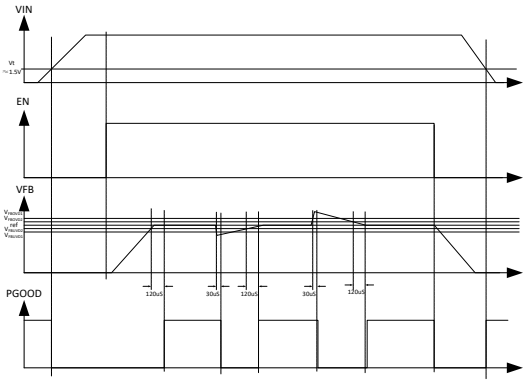
RT Pin Function:

The RT pin is used for SA33101 switching frequency setting. Choosing a different RT resistor will control the SA33101 switch from 200kHz to 1.2MHz. The EC-table guarantees the switching frequency when R_{RT} ranges from 135KΩ to 32KΩ. Switching frequency vs. R_{RT} curve is below (R_{RT} [kΩ] = 41993 x f_{OSC} [kHz] ^ (-1.039)):



PGOOD Pin Function:

The PGOOD pin indicates the output voltage status after soft start. When VOUT is lowered or raised, PGOOD is pulled down by the internal drain MOS. When VOUT returns to normal voltage, PGOOD is pulled up by an external resistor connected to the VCC or other voltage source.

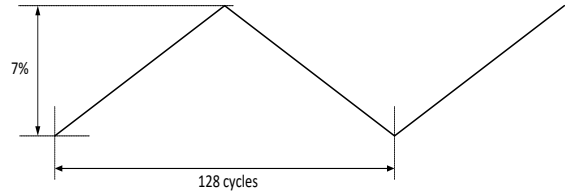


CLKOUT PIN Function:

A 180°phase shift clock output relative to the internal oscillator at CLKOUT pin is for cascaded power supplies or multichannel power supplies to reduce current ripple at input capacitor and EMI filter size. This CLKOUT is signal with 50% duty cycle. When the first SA33101 is operating in frequency decrease mode, CLKOUT will become asynchronous to internal oscillator.

Spread Frequency Function:

The spread frequency function works for EMC reduction. The SA33101 changes the switching frequency each 128 cycles and the range is ±3.5%.



Pre-bias Function

The SA33101 incorporates pre-bias to provide a smooth output voltage when a cold crank or constant start causes the output voltage to drop.

Current Limit Function

The SA33101 provides cycle by cycle current limit function. When the voltage SENSE-VOUT is higher than V_{LIMIT}, HGATE will be off and then LGATE on, when the voltage SENSE-VOUT<$V_{IREVLIMIT}$, LGATE will be off and HGATE will be on.

Under Voltage Detection

Under voltage detection monitoring the voltage from FB pin, when VFB drops lower than V_{FBUVD2} and keeps longer than 30uS, the SA33101 will be pull down PGOOD voltage, with voltage on FB higher than V_{FBUVD1} and keep longer than 120uS, PGOOD is pull high again.

Under Voltage/VOUT Short to GND Protection（SOP）

After the soft start is complete, the SA33101 will monitor the FB pin output voltage, and when the FB pin voltage is below 220mV and the duration is greater than 20uS, SA33101 will burp.

Over Voltage Detection

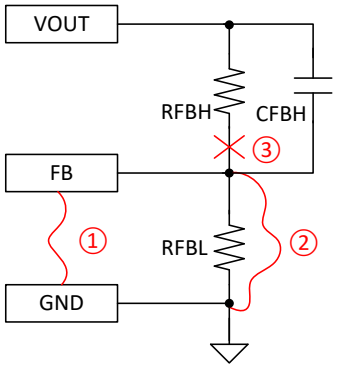
Over voltage detection monitoring the voltage on FB pin, when VFB rises higher than V_{FBOVD1} and keeps longer than 30uS, SA33101 will pull down PGOOD, with voltage on FB lower than V_{FBOVD2} and keep longer than 120uS, PGOOD is pull high again.

Output over Voltage Protection

When the output voltage reaches V_{OUT_OV} (type 5.9V), the SA33101 will monitor the output voltage from the VOUT pin. The SA33101 will enter hiccup mode.

FB Abnormal Detection

The SA33101 combines the signals detected by FB pin and VOUT pin to detect FB anomalies. When V_{OUT}>1.2V and V_{FB}<15mV are detected, FB is abnormal and the IC will enter hiccup mode. (FB pin short to GND/RFBH open/RFBL short to GND; It is noteworthy that in the case CFBH is used, VFB will be coupled by CFBH, VFB will be higher than 15mV, and V_{OUT} may rise to V_{OUT_OV}).



① FB pin short to GND;
② RFBL short to GND;
③ RFBH open

LX Short to VIN or LX Short to GND Protection

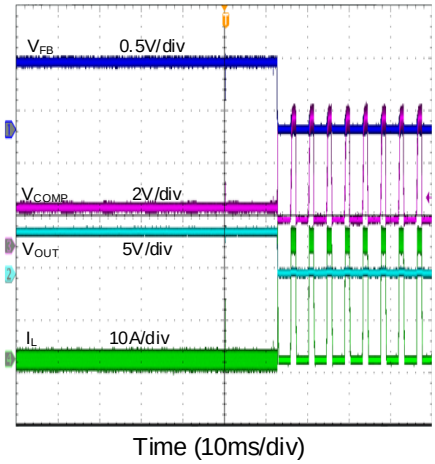
Abnormal current will occur in high side MOS or low side MOS in below cases:

1. High side MOS DS short/open
2. Low side MOS DS short/open
3. Inductor short
4. HGATE open
5. LGATE open

Detect VIN-VLX when HGATE is on. If VIN-VLX is higher than VLXSHORTH, the IC will stop PWM and enter hiccup mode. Detect VLX when LGATE is on. If VLX is higher than VLXSHORTL, the IC will stop PWM and enter hiccup mode.

Over Current Protection

After the SA33101 soft start is completed, the inductive current will be detected from RSENSE cycle by cycle. When the detection is constant 128 cycles VRSENSE> VILIMIT, the IC will enter the burp rising mode.



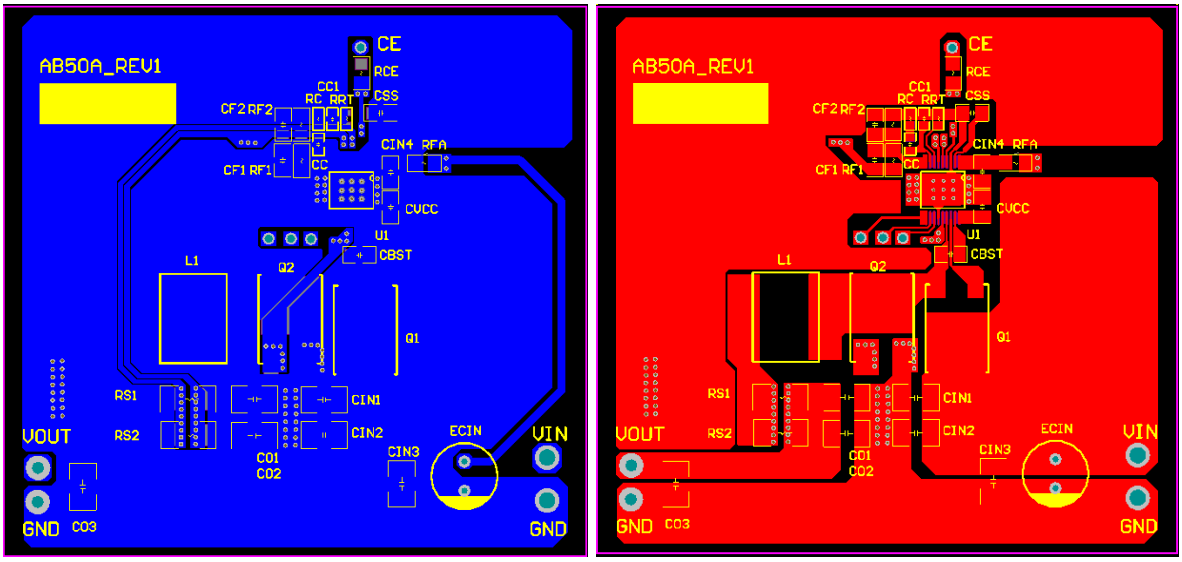
Hiccup up Mode

The SA33101 burping mode stops HGATE and LGATE, discharges CSS and COMP, and attempts to restart after a delay of 3ms.

Thermal Shut Protection

The SA33101 integrates an internal junction temperature monitor. If the temperature higher than $T_{TSD,}$ The IC will shut down until junction temperature lower than TTSR again. During thermal, the IC will turn off IC power supply from VIN to VCC, high side MOS and low side MOS, discharge CSS/COMP.

Layout Design

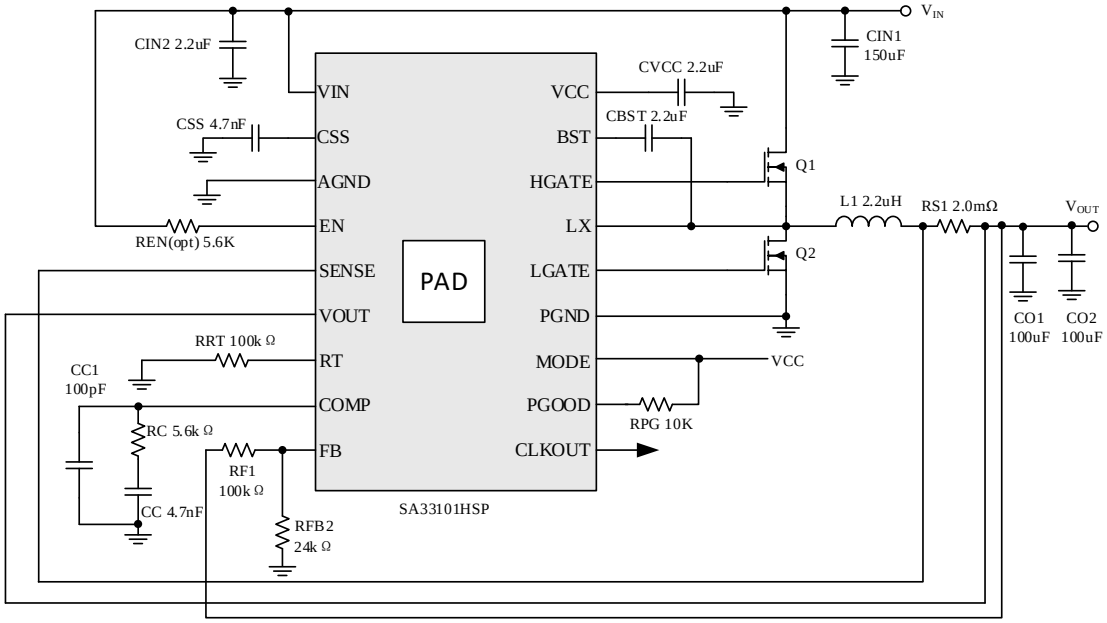


(a) A ceramic capacitor is needed to connect from COMP pin to AGND to avoid noise disturbance.

(b) It is recommended that the smaller the Kelvin sampling loop from the sensing resistor to the IC, the greater the current. (Sense pin and VOUT pin to current sense resistor)

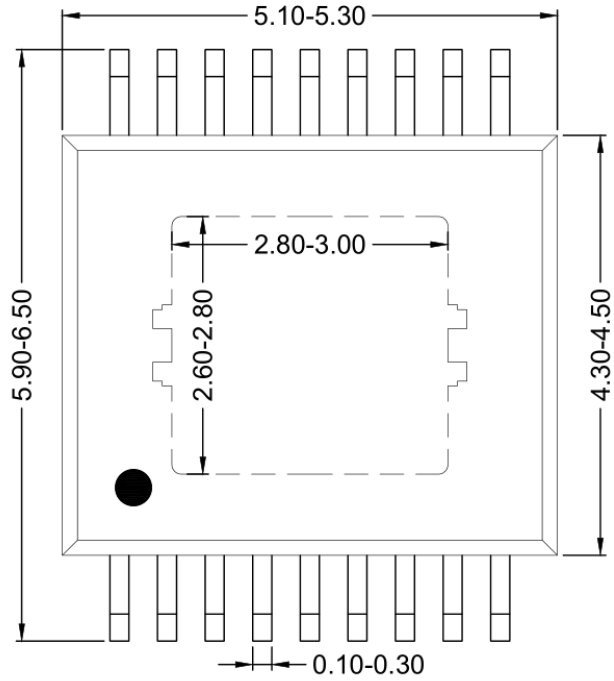
(c)AGND/PGND and VIN/VOUT GND connect together in PCB.

Application Example

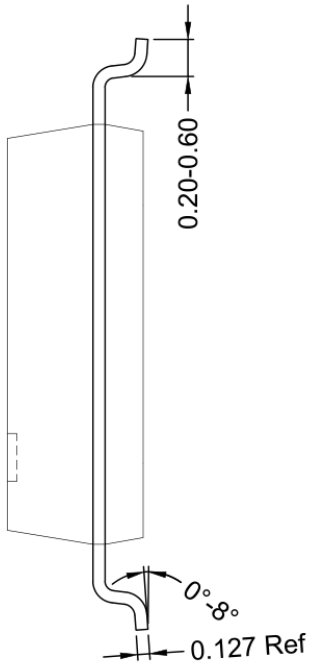


VOUT=3.3V, ILOAD=15A, FSW=300KHz

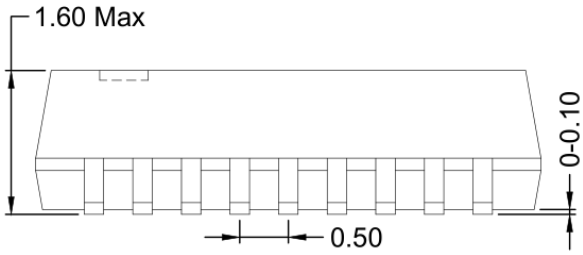
SSOP18E Package Outline Drawing



Top View



Side View



Front View

Note：All dimension in millimeter and exclude mold flash & metal burr.

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 30, 2023	Revision 0.9	Initial Risk Production Release
June 30, 2024	Revision 1.0	Initial Production Release

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