SA22900

50V, Dual-Phase Stackable Synchronous Boost Controller

General Description

The SA22900 is a dual-phase stackable synchronous boost controller. It operates over a wide input voltage range from 5V to 50V and utilizes constant frequency peak current mode control. The SA22900 operates at a switching frequency ranging from 50kHz to 1.1MHz per phase and can be synchronized to an external clock. It supports single-phase, dual-phase, and 4-phase operation to reduce output ripple and capacitance. Additionally, the spread spectrum function can be used to minimize peak emissions, resulting in lower electromagnetic interference (EMI).

The SA22900 features external soft-start, enable control, and an open-drain power good indicator. It also includes comprehensive protection features, such as cycle-by-cycle overcurrent protection, input overvoltage protection, output overvoltage protection, and thermal shutdown for reliable operation. The fault protection response can be configured for either latch-off or hiccup recovery.

The SA22900 is available in compact QFN5×5-32 package.

Key Features

- Wide Input/Output Voltage Range: 5V to 50V
- 1.6V±1% Reference Voltage over -40℃~125 ℃
- Selectable 1-, 2-, or 4 (Two Devices Paralleled) Interleaved Phase Operation
- Supports Spread Spectrum Function
- Power Good Indicator
- Supports External Synchronization
- Supports Tracking Function
- Integrated N-channel MOSFET Drivers: 5V 2A Sourcing/3A Sinking
- Programmable Frequency Per Phase: 50kHz to 1.1MHz
- Programmable Dead Time and Minimum Duty Cycle
- Light Load Operating Mode Selection: PFM or FCCM
- Selectable Phase Drop and Phase Add Function
- Fully Protected for Over Voltage, Over Current and Over-Temperature
- Selectable Hiccup or Latch-off Fault Response
- RoHS Compliant and Halogen Free
- Compact Package QFN5×5-32
- Automotive AEC- Q100 Grade 1 Qualified

Applications

- Automotive Power Systems
- Audio Amplifiers
- Automotive Boost Applications
- Industrial and Telecommunication Power Supplies

Typical Application

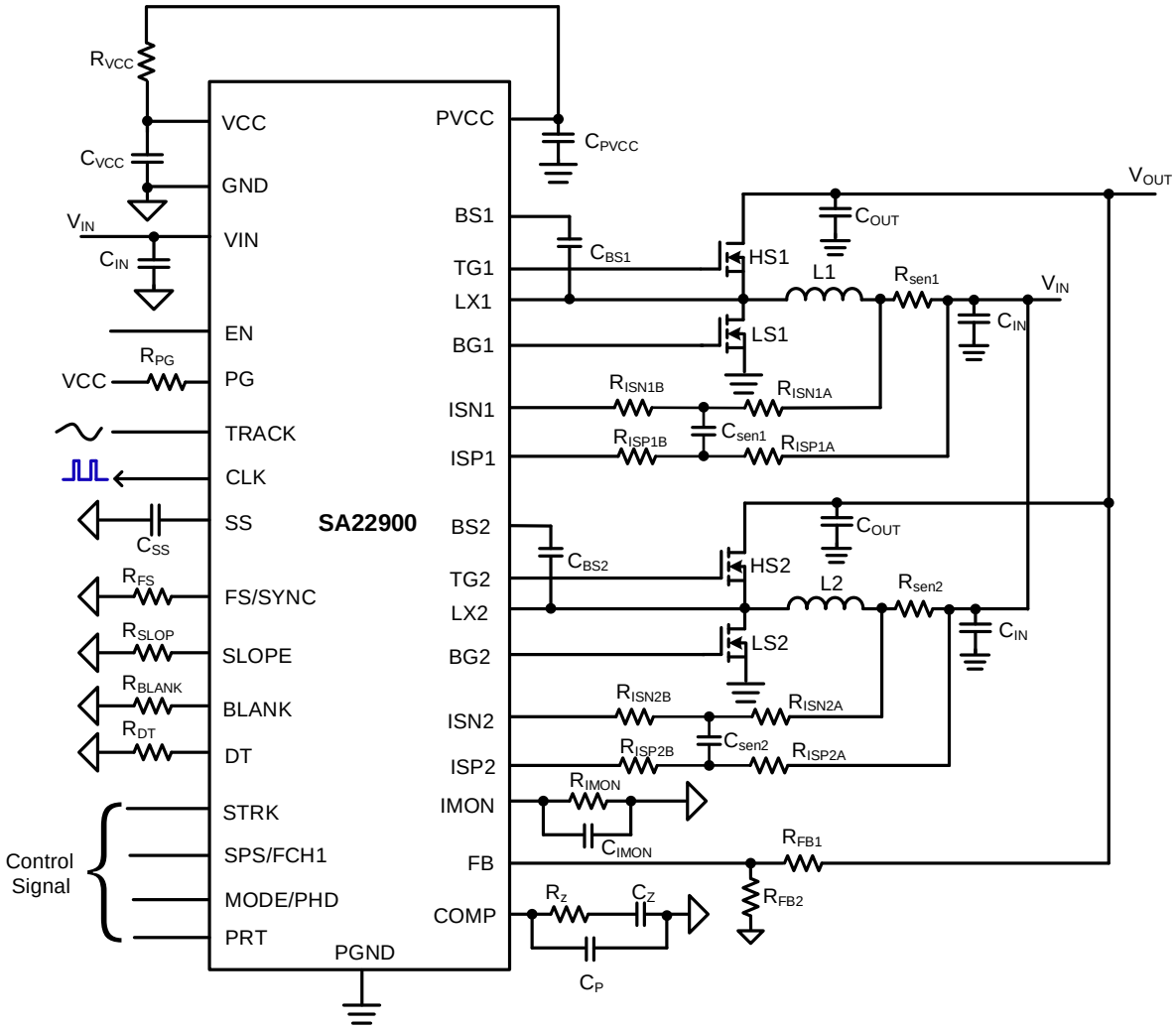


Figure 1a. Typical Application Circuit for Dual-phase Operation

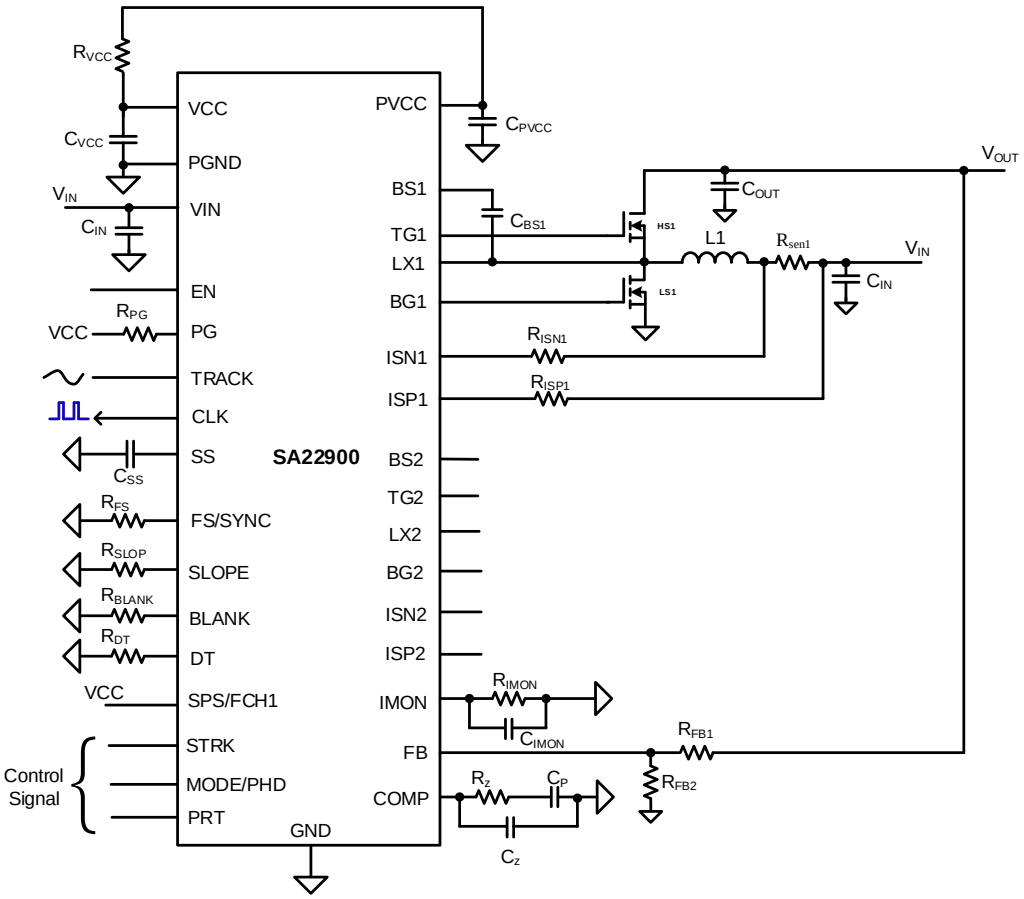


Figure 1b. Typical Application Circuit for Single-phase Operation

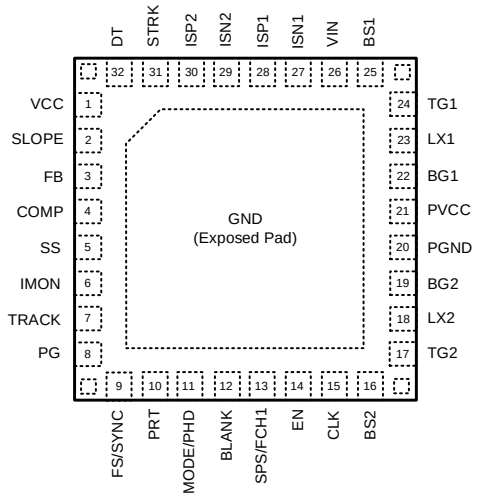
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA22900QEQ	QFN5×5-32 RoHS-Compliant and Halogen-Free	**GHC*xyz***

Device code: GHC

x = year code, y = week code, z = lot number code

Pin Out (top view)



Pin Description

Pin Name	Pin Number	Pin Description
VCC	1	Internal analog circuitry power supply pin. Place a ceramic decoupling capacitor between this pin and GND with a value of at least one 1μF. A small series resistor (10Ω or smaller) between PVCC and VCC can be used to filter noise. An external source bias with voltage ranging from 4.75V to 5.25V can also be used.
SLOPE	2	Internal slope compensation pin. Program the slope compensation value using a resistor connected from this pin.
FB	3	Output feedback pin. Connect this pin to the center point of the output resistor divider to adjust the V_{OUT} voltage: $V_{OUT} = V_{REF} \times (1+R_{FB1}/R_{FB2})$
COMP	4	Compensation pin. Connect the RC network between this pin and ground.
SS	5	Soft-start pin. Connect a capacitor from this pin to GND to program the soft-start time.
IMON	6	The average current monitor pin. This represents the sum of the two phases' inductor currents and is the input current for the boost. It is also used for average current limiting and protection functions. Connect a resistor in parallel with a capacitor from this pin to GND to monitor the average current.
TRACK	7	External reference input pin. Program the STRK to set the input reference signal, which can be either a digital or analog signal. If the TRACK function is not used, connect this pin to VCC to select the internal 1.6V reference.
PG	8	Open-drain power good indicator. Pulled low, when output UV/OV or input OV conditions are detected. High-impedance during normal operation.
FS/SYNC	9	Frequency setting and synchronization input pin. Connect a resistor from this pin to GND to program the switching frequency between 50kHz to 1100kHz. When connected to an external clock, the internal oscillator synchronizes to the external clock. If the external clock is removed, it will work in either Hiccup or Latch-off mode, configured by the PRT pin. The phase dropping mode is not supported with external synchronization.
PRT	10	Protection mode setting pin. Connect this pin to VCC to activate the Hiccup protection, and connect this pin to ground for Latch-off protection.
MODE/PHD	11	Operating mode under light load and phase dropping selection pin. The phase dropping mode can't be utilized with external synchronization.

Pin Name	Pin Number	Pin Description
BLANK	12	Current sensing blank time after low side FET turns on. Connect a resistor from this pin to ground to program the blanking time. The minimum on time is also limited by this setting.
SPS/FCH1	13	Spread spectrum and only channel1 operating mode selection pin.
EN	14	Enable control. Pull high to enable the device, pull low to disable the device. The internal impedance from EN to GND is around 6MΩ.
CLK	15	Synchronize clock output for the second device. The phase is delayed by 90 degrees compared to the channel1 of the device. Leave this pin floating if not used.
BS2	16	Bootstrap pin for Channel2. Decoupling this pin to the LX2 pin with a 0.47μF ceramic capacitor is recommended. If the high-side driver is not needed (as in asynchronous boost applications), this pin can be left floating.
TG2	17	Channel 2 high-side gate driver output.
LX2	18	Inductor connection for channel2. Connect this pin to the inductor's switching node.
BG2	19	Channel 2 low-side gate driver output.
PGND	20	Power ground pin.
PVCC	21	Internal 5.2V LDO output. Power supply for internal control circuits. Decouple this pin to PGND with at least one 10uF ceramic capacitor.
BG1	22	Channel 1 low-side gate driver output.
LX1	23	Inductor connection for channel1. Connect this pin to the inductor's switching node.
TG1	24	Channel 1 high-side gate driver output.
BS1	25	Bootstrap pin for Channel1. Decoupling this pin to the LX1 pin with a 0.47μF ceramic capacitor is recommended. If the high-side driver is not needed (as in asynchronous boost applications), this pin can be left floating.
VIN	26	Power input pin. Decouple this pin to GND with a minimum 22μF ceramic capacitor.
ISN1	27	Negative potential input of channel1 current sense amplifier. The sensed current signal is used for channel1 current mode control, peak current limit and average current limit.
ISP1	28	Positive potential input of channel1 current sense amplifier.
ISN2	29	Negative potential input of channel2 current sense amplifier. The sensed current signal is used for channel2 current mode control, peak current limit and average current limit
ISP2	30	Positive potential input of channel2 current sense amplifier.
STRK	31	The input signal format selection for the TRACK pin. Pull this pin high to accept analog input signals. Pull this pin low to accept digital input signals. This pin can be left floating when the TRACK function is not used.
DT	32	Connecting a resistor from this pin to ground programs the dead time to prevent shoot-through.
GND	Exposed Pad	Signal ground. Connect this pad to large ground plane for good thermal performance.

Block Diagram

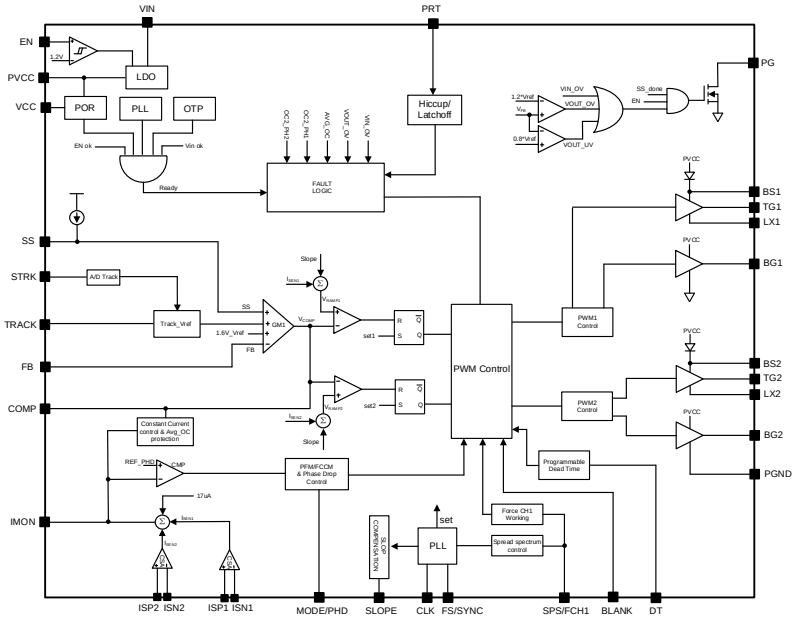


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN, LX1, LX2, ISN1, ISP1, ISN2, ISP2, EN	-0.3	60	V
VBS1-LX1, VBS2-LX2	-0.3	6.5	
TG1-LX1, TG2-LX2	-0.3	BS+0.3	
PVCC, VCC	-0.3	6	
VISN1-VISP1, VISN2-VISP2	-0.6	+0.6	
All Other Pins	-0.3	Vcc+0.3	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	
ESD Rating			
HBM (Human Body Model)	-2000	2000	V
CDM (Charged Device Model)	-700	700	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	26.8	°C/W
θ_{JC_TOP} Junction-to-Case Top Thermal Resistance	13.8	
θ_{JC_BOT} Junction-to-Case Bottom Thermal Resistance	3.4	

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	5	50	V
PVCC VCC	4.9	5.5	
Upper Driver Supply Voltage, VBS1-VLX1/ VBS2-VLX2	3.5	6	
ISN1 to ISP1 and ISN2 to ISP2 Differential Voltage	-0.3	+0.3	
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C to +125°C. Typical values are at T_J =25°C, unless otherwise specified (Note 4).)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input	Input Voltage Range	V_{IN}		5		50	V
	Input Quiescent Current	$I_{Q,SW}$	EN = 5V, V_{IN} = 12V, PVCC = VCC, BS1 and BS2 supplied by PVCC, f_{SW} = 300kHz, BGx = OPEN, TGx = OPEN		10	13	mA
		$I_{Q,NON-SW}$	EN = 5V, VIN = 12V, PVCC = VCC, BS1 and BS2 supplied by PVCC, non-switching, BGx = OPEN, TGx = OPEN		3	4	mA
	Shutdown Current	I_{SD}	EN = GND		1.5	4	μA
Internal Linear Regulator (PVCC&VCC)	PVCC UVLO Rising Threshold	$V_{PVCC,RISING}$		4.35	4.50	4.75	V
	PVCC UVLO Hysteresis	$V_{PVCC,HYS}$			1.3		V
	PVCC Regulator Output Voltage	V_{PVCC}	I_{PVCC} = 10mA	5.0	5.2	5.4	V
	PVCC Load Regulation	$V_{PVCC,REG}$	$I_{\_PVCC}$ = 80mA, measure the PVCC dropout voltage		0.5		V
	PVCC Output Current Limit	I_{LMT_PVCC}	V_{IN} = 6V, V_{PVCC} = 4.5V	130	175	250	mA
	VCC Pin UVLO Rising Threshold	$V_{VCC,RISING}$		4.35	4.50	4.75	V
	VCC Pin UVLO Hysteresis	$V_{VCC,HYS}$			0.4		V
Feedback Reference	Feedback Reference Voltage	V_{REF}		1.584	1.600	1.616	V
	FB Pin Input Current	I_{FB}	V_{FB} = 1.6V, TRACK = Open	-50		50	nA
Enable	EN Rising Threshold	$V_{EN,R}$		1.13	1.21	1.33	V
	EN Falling Threshold	$V_{EN,F}$		0.85	0.95	1.10	V
	EN Threshold Hysteresis	$V_{EN,HYS}$			250		mV
PWM Switching Frequency	Switching Frequency Program Range	$f_{SW,RNG}$	R_{FS} =10 ~250kΩ (0.1%)	50		1100	kHz
	Switching Frequency Setting Accuracy	f_{SW}	R_{FSYNC} = 40.2kΩ (0.1%)	270	300	330	kHz
	Minimum ON-Time Accuracy	t_{MIN,ON_ACC}	Minimum duty cycle (Blanking time setting) R_{BLANK} = 25kΩ (0.1%)	120	160	200	ns
	Maximum Duty Cycle	D_{MAX}	f_{SW} = 300kHz, R_{DT} = 18.2kΩ	87.5	90	92.5	%
Synchronization (FSYNC Pin)	Sync Input Voltage High	$V_{SYNC,H}$		3.5			V
	Sync Input Voltage Low	$V_{SYNC,L}$				1.5	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	Sync Frequency Program Range	$f_{SW\_SYNC,RNG}$		80		1000	kHz
	Sync Input Minimum Pulse Width	$t_{SYNC,MIN}$	Both rise to fall and fall to rise	20			ns
Soft-Start	Soft-Start Charging Current	I_{SS}		4.3	4.9	5.5	μA
	Minimum Soft-Start Pre-Bias Voltage	$V_{SS,BIAS\_MIN}$			0		V
	Maximum Soft-Start Pre-Bias Voltage	$V_{SS,BIAS\_MAX}$			1.6		V
	Soft-Start Pre-bias Voltage Accuracy	$V_{SS,BIAS\_ACC}$	V_{FB} = 500mV	-25	0	25	mV
	Soft-Start Clamp Voltage	$V_{SS,CLAMP}$		4.0	4.3	4.6	V
	Turn on Delay Time	$t_{ON,DELAY}$	From UVLO ok to initiation of soft-start.		0.6	0.85	ms
Current Sense Amplifier	ISNx and ISPx Common-Mode Voltage Range	$V_{CM,RANGE}$			4		V
	ISNx and ISPx Input Differential Voltage Range	$V_{DIFF,ISP-ISN}$			±0.3		V
	ISNx/ISPx Input Current	I_{ISNX}/ I_{ISPX}	Sourcing out of pin, EN = 5V, VISNx = VISPx, VCM = 4V to 50V	100	123	150	μA
IMON function	IMON Offset Current		V_{SENx}=0V, R_{ISPx}=1510Ω(0.1%), VISNx = VISPx, VCM = 4V to 50V	16	17	18	μA
	IMON Current Accuracy		V_{SENx}=68mV, R_{ISPx}=1510Ω(0.1%), VISNx = VISPx, VCM = 4V to 50V	27	28.3	29.5	μA
	Phase-Drop Falling Threshold	V_{PHDRP}	When V_{IMON} falls below V_{PHDRP} drop off Phase 2	1	1.1	1.2	V
	Phase-Add Rising Threshold	V_{PHADD}	When V_{IMON} rises above V_{PHADD} add back Phase 2	1.05	1.15	1.25	V
	Phase-Drop Threshold Hysteresis	V_{PHDRP_HYS}		45	55	65	mV
	Constant Current Control Reference Accuracy	$V_{REF,CC}$	Measure the IMON pin Voltage	1.576	1.600	1.624	V
	Average Current Over Fault Threshold	$V_{AVG,OC}$	Measure the IMON Pin Voltage	1.9	2	2.1	V
	Average Current Over Fault Delay Time	AVG_{OC_DEALY}			5	12	μs
Peak Current	Peak Current Limit Threshold	$V_{PK,LMT}$	R_{ISPx}=1510Ω (0.1%), measure the voltage of R_{SENx} for OC1 (I_{OC1_TH}=80μA)	100	125	150	mV

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	Peak Current Fault Protection Threshold	$V_{PK,FAULT}$	R_{ISPx}=1510Ω (0.1%), measure the voltage of R_{SENx} for OC2 (I_{OC2_TH}=105μA)	130	160	190	mV
	Peak Current Fault Protection Blanking Time	$t_{PK,BLANK}$			3		cycles
Zero Current	Zero Current Detection Threshold	V_{ZERO}	R_{ISPx}=1510Ω (0.1%), measure the voltage of R_{SENx}	-5	1.3	9	mV
Negative Current	Negative Current Limit Threshold	$V_{ILM, NEG}$	R_{ISPx}=1510Ω (0.1%), measure the voltage of R_{SENx} ($I_{OC\_NG\_TH}$=-48μA)	-100	-72	-50	mV
Gate Drivers	TG Source Resistance	R_{TG_SOURCE}	100mA source current, V_{BS} - V_{LX} = 4.4V		1.2		Ω
	TG Source Current	I_{TG_SOURCE}	V_{TG} – V_{LX} = 2.5V, V_{BS} – V_{LX} = 4.4V		2		A
	TG Sink Resistance	R_{TG_SINK}	100mA sink current, V_{BS} - V_{LX} = 4.4V		0.6		Ω
	TG Sink Current	I_{TG_SINK}	V_{TG} - V_{LX} = 2.5V, V_{BS} - V_{LX} = 4.4V		2		A
	BG Source Resistance	R_{BG_SOURCE}	100mA source current, PVCC = 5.2V		1.2		Ω
	BG Source Current	I_{BG_SOURCE}	V_{BG} - PGND = 2.5V, PVCC = 5.2V		2		A
	BG Sink Resistance	R_{BG_SINK}	100mA sink current, PVCC = 5.2V		0.55		Ω
	BG Sink Current	I_{BG_SINK}	V_{BG} - PGND = 2.5V, PVCC = 5.2V		3		A
	TG to LX Internal Resistor	R_{TG_LX}			50		kΩ
	BG to PGND Internal Resistor	R_{BG_GND}			50		kΩ
	Boot-Strap UVLO Rising Threshold	$V_{BS,RISING}$		2.6	3	3.3	V
	Boot-Strap UVLO Falling Threshold	$V_{BS,FALLING}$		2.5	2.85	3.15	V
	Dead Time When TG Falling to BG Rising	t_{DT1}	R_{DT} = 10k (0.1%)	100	125	150	ns
	Dead Time When BG Falling to TG Rising	t_{DT2}	R_{DT} = 10k (0.1%)	65	90	115	ns
Input Overvoltage Protection	Input Overvoltage Rising Threshold	V_{IN,OVP_RISE}	EN = 5V, V_{IN} rising	57	58.5	60	V
	Input Overvoltage Delay Time	V_{IN,OVP_DELAY}	EN = 5V, V_{IN} rising		5	12	μs
Output Overvoltage Protection	FB Overvoltage Rising Threshold	V_{FB,OVP_RISE}		118	120	122	%Vref
	FB Overvoltage Falling Threshold	V_{FB,OVP_FALL}		114	116	118	%Vref
	Overvoltage Threshold Hysteresis				4		%Vref
	FB Overvoltage Trip Delay				1	3	μs

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Undevoltage Protection	Undervoltage Falling Threshold	V_{FB,UVP_FALL}		78	80	82	%Vref
	Undervoltage Rising Threshold	V_{FB,UVP_RISE}		82.5	84	86.5	%Vref
	Undervoltage Threshold Hysteresis				4		%Vref
Power Good	Power Good Low Voltage		PG LOW, I_{PG} = 0.5mA		0.06	0.4	V
	Power Good from Low to High Delay Time (PFM)	$T_{PG\_DELAY(PFM)}$	The delay time from SS clamp to PG high		0.5	0.6	ms
	Power Good from Low to High Delay Time (FCCM)	$T_{PG\_DELAY(FCCM)}$	The delay time from SS clamp to PG high		100	120	ms
	Power Good from High to Low Delay Time				10	12	μs
Tracking Function	TRACK Input Reference Voltage Range	TRACK,RANGE		0		1.6	V
	TRACK Input Reference Voltage Accuracy	TRACK,ACC	Analog Signal Input, Measure at the FB pin, V_{TRACK} = 1.5V	-4	0	4	%
	TRACK SS_DONE Threshold	TRACK,SS_DONE	Analog Signal Input	0.28	0.3	0.32	V
	TRACK Input Logic Low	TRACK,L	Digital Signal Input			0.8	V
	TRACK Input Logic High	TRACK,H	Digital Signal Input	2			V
		TRACK,DUTY_ACC	50% duty cycle input under 2.5V high voltage, frequency = 400kHz, measure at the FB pin	1.235	1.272	1.3	V
STRK	STRK Input Logic Low (Digital)	$V_{STRK,L}$				0.8	V
	STRK Input Logic High (Analog)	$V_{STRK,H}$		2.1			V
Protection	PRT Input Logic Low (Latch-off)	$V_{PRT,L}$				0.8	V
	PRT Input Logic High (Hiccup)	$V_{PRT,H}$		2.1			V
MODE/PHD	MODE/PHD Input Logic Low	$V_{MODE/PHD,L}$				0.7	V
	MODE/PHD Input Logic High	$V_{MODE/PHD,H}$		VCC-0.4			V
SPS/FCH1	SPS/FCH1 Input Logic Low	$V_{SPS/FCH1,L}$				0.7	V
	SPS/FCH1 Input Logic High	$V_{SPS/FCH1,H}$		VCC-0.4			V
OTP	Thermal Shutdown Temperature	T_{SD}		150	160	175	°C
	Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Prolonged exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2oz four-layer Silergy evaluation board using nine thermal vias. Case temperature θ_{JC} is measured at pin 20.

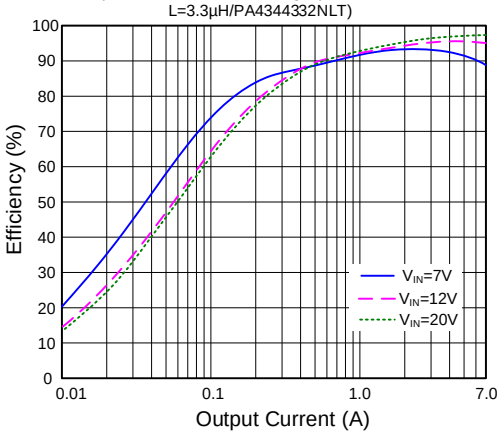
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions with $T_A \approx T_J$ = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, testing, or statistical correlation.

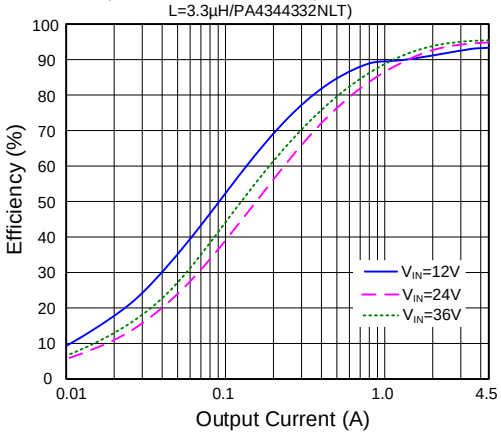
Typical Performance Characteristics

(1-phase: T_A=25°C, V_{OUT}=25V, f_{SW}=400kHz, L=3.3μH, C_{OUT}=10μF×2(MLCC)+100μF×4(E-Cap), unless otherwise specified;
2-phases: T_A=25°C, V_{OUT}=45V, f_{SW}=400kHz, L=3.3μH, C_{OUT}=10μF×2(MLCC)+100μF×4(E-Cap), unless otherwise specified.)

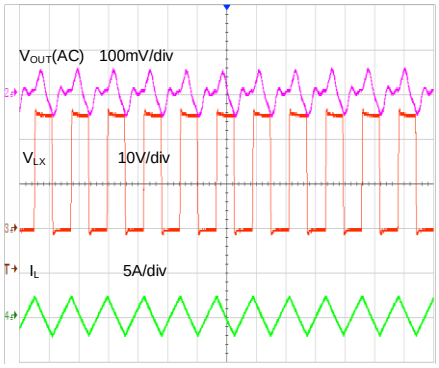
Efficiency vs. Output Current
(V_{OUT}=25V,f_{SW}=400kHz, single phase, FCCM, L=3.3μH/PA4344332NLT)



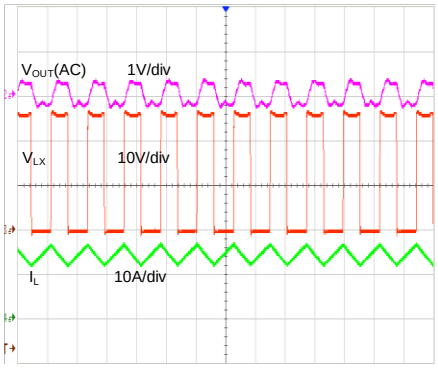
Efficiency vs. Output Current
(V_{OUT}=45V,f_{SW}=400kHz, dual phase, FCCM, L=3.3μH/PA4344332NLT)



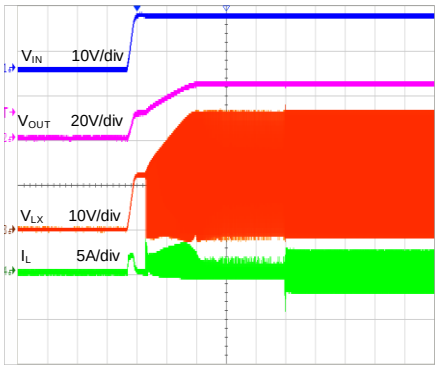
Output Ripple
(V_{IN}=12V,V_{OUT}=25V,I_{LOAD}=0A, single phase, FCCM)



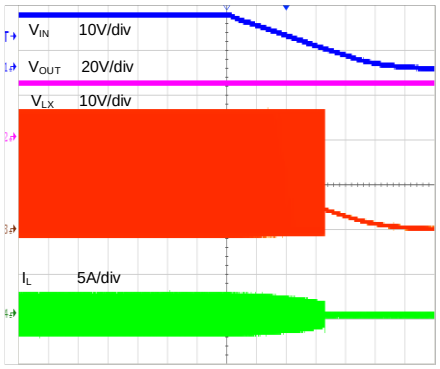
Output Ripple
(V_{IN}=12V,V_{OUT}=25V,I_{LOAD}=7A, single phase, FCCM)



Startup from VIN
(V_{IN}=12V,V_{OUT}=25V,I_{LOAD}=0A, single phase, FCCM)

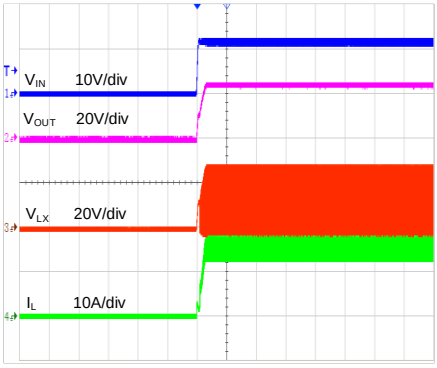


Shutdown from VIN
(V_{IN}=12V,V_{OUT}=25V,I_{LOAD}=0A, single phase, FCCM)



Startup from VIN

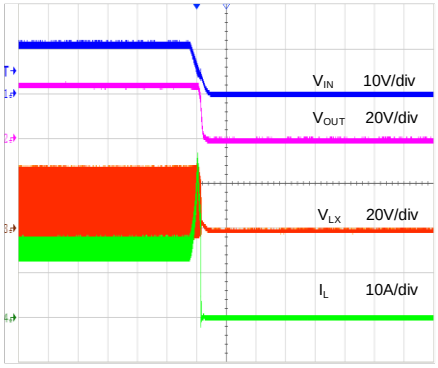
(V_{IN}=12V,V_{OUT}=25V,I_{LOAD}=7A, single phase, FCCM)



Time (20ms/div)

Shutdown from VIN

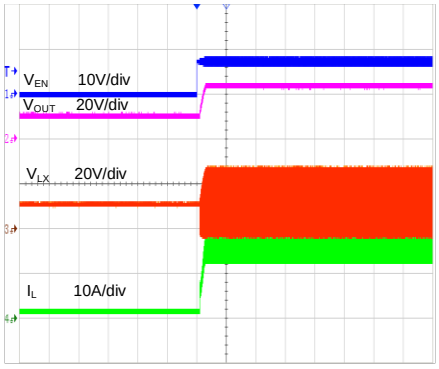
(V_{IN}=12V,V_{OUT}=25V,I_{LOAD}=7A, single phase, FCCM)



Time (20ms/div)

Startup from EN

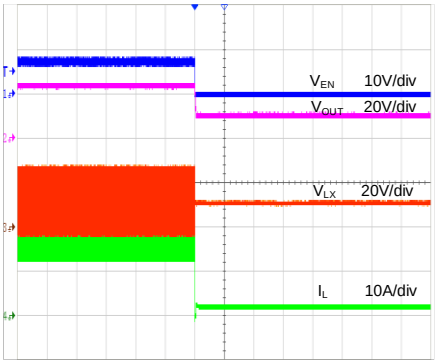
(V_{IN}=12V,V_{OUT}=25V,I_{LOAD}=7A, single phase, FCCM)



Time (20ms/div)

Shutdown from EN

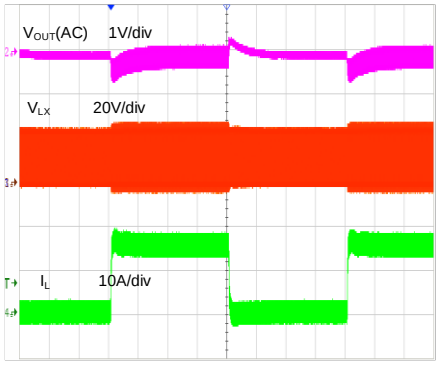
(V_{IN}=12V,V_{OUT}=25V,I_{LOAD}=7A, single phase, FCCM)



Time (20ms/div)

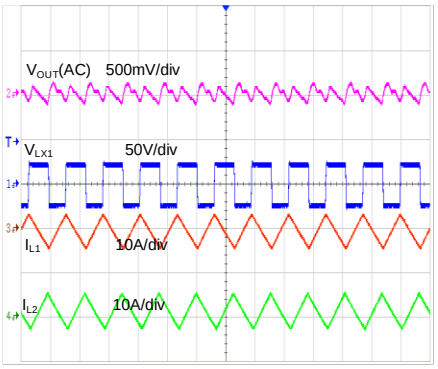
Load Transient

(V_{IN}=12V,V_{OUT}=25V,I_{LOAD}=0~7A, single phase, FCCM)



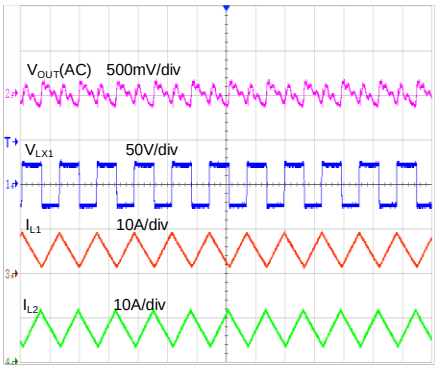
Time (1ms/div)

Output Ripple
(V_{IN}=24V,V_{OUT}=45V,I_{LOAD}=0A, dual phase, FCCM)



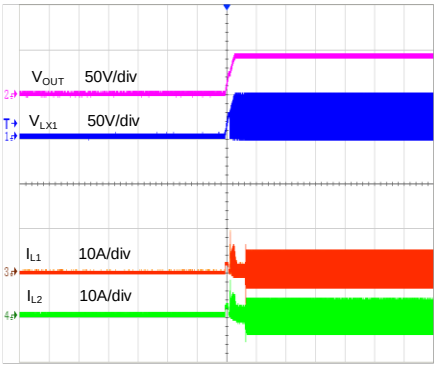
Time (2µs/div)

Output Ripple
(V_{IN}=24V,V_{OUT}=45V,I_{LOAD}=7A, dual phase, FCCM)



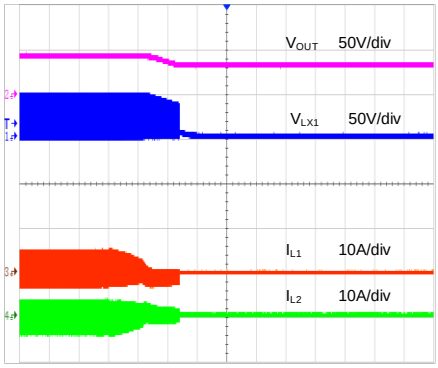
Time (2µs/div)

Startup from VIN
(V_{IN}=24V,V_{OUT}=45V,I_{LOAD}=0A, dual phase, FCCM)



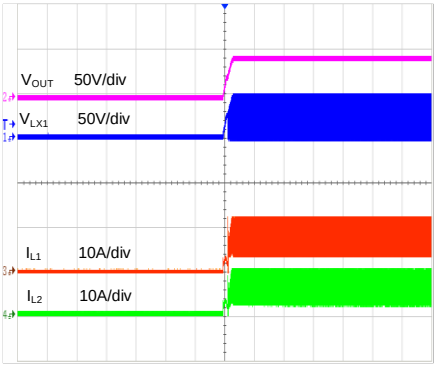
Time (20ms/div)

Shutdown from VIN
(V_{IN}=24V,V_{OUT}=45V,I_{LOAD}=0A, dual phase, FCCM)



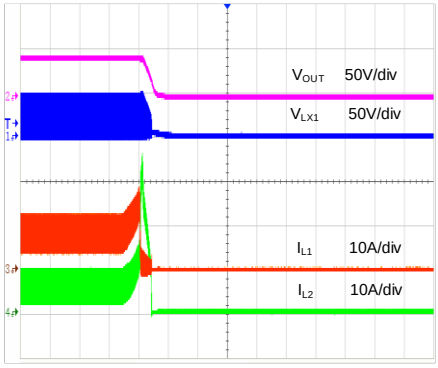
Time (20ms/div)

Startup from VIN
(V_{IN}=24V,V_{OUT}=45V,I_{LOAD}=7A, dual phase, FCCM)



Time (20ms/div)

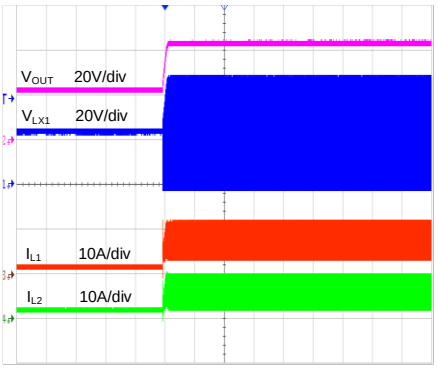
Shutdown from VIN
(V_{IN}=24V,V_{OUT}=45V,I_{LOAD}=7A, dual phase, FCCM)



Time (20ms/div)

Startup from EN

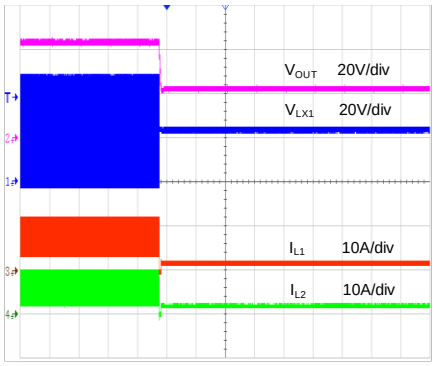
(V_{IN}=24V,V_{OUT}=45V,I_{LOAD}=7A, dual phase, FCCM)



Time (20ms/div)

Shutdown from EN

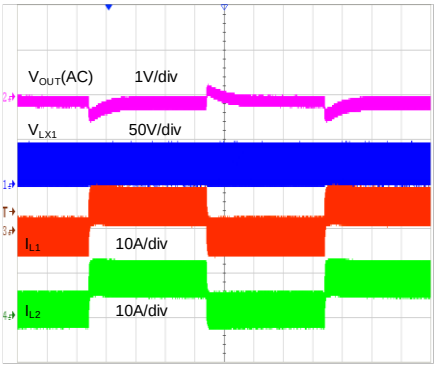
(V_{IN}=24V,V_{OUT}=45V,I_{LOAD}=7A, dual phase, FCCM)



Time (20ms/div)

Load Transient

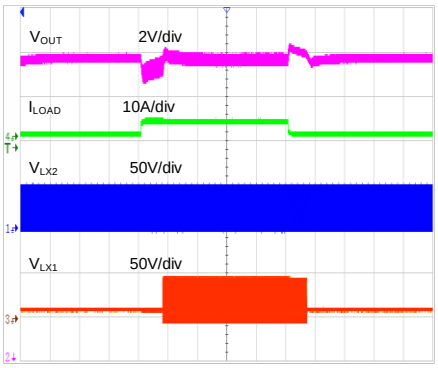
(V_{IN}=24V,V_{OUT}=45V,I_{LOAD}=0~7A, dual phase, FCCM)



Time (1ms/div)

Phase Drop and Phase Add

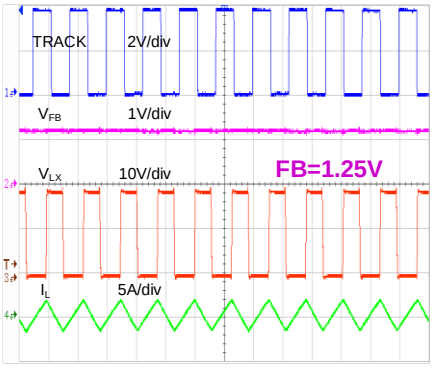
(V_{IN}=12V,V_{OUT}=45V,I_{LOAD}=0~4A, enable phase drop, FCCM)



Time (2ms/div)

Digital Track

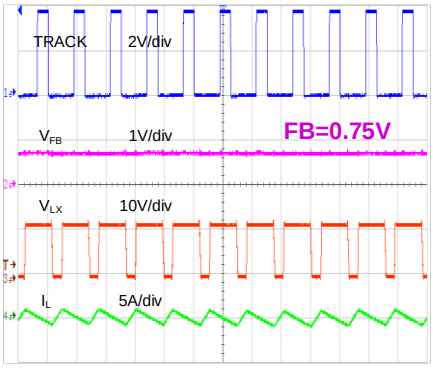
(V_{IN}=9V, FS_{TRK}=400kHz, D_{TRK}=0.5, single phase, FCCM)



Time (2μs/div)

Digital Track

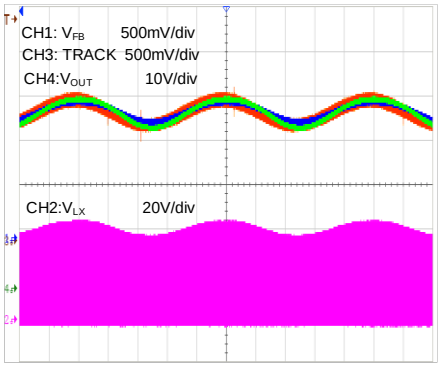
(V_{IN}=9V, FS_{TRK}=400kHz, D_{TRK}=0.3, single phase, FCCM)



Time (2μs/div)

Analog Track

(V_{IN}=12V, single phase, FCCM)



Time (2ms/div)

Operation Description

The SA22900 is a two-phase boost synchronous controller with a wide input/output voltage range from 5V to 50V. It integrates 2A source and 3A sink drivers to efficiently support external MOSFETs. The device uses a constant frequency, peak current mode control modulation method, requiring slope compensation when the duty cycle exceeds 50%.

The SA22900 supports both PFM and FCCM modes for light loads by configuring the MODE/PHD and SPS/FCH1 pins. The spread spectrum and phase drop functions can also be enabled to enhance EMI performance and improve light load efficiency. It allows for the setting of dead time for different MOSFETs to achieve optimized efficiency and reliable MOSFET driving. The SA22900 features a unique tracking function that can accept either digital or analog signals to control the output voltage through reference voltage adjustment.

The SA22900 can select either a latch-off or hiccup response action for built-in protection features, including peak current protection (OC2), input overvoltage protection (VIN_OV), output overvoltage protection (VOUT_OV), and average overcurrent protection (AVG_OC). It supports constant current (CC) mode to limit input current, which maintains a constant input current under overload conditions.

The SA22900 uses constant frequency and peak current mode control. At the beginning of each PWM cycle, the low-side MOSFET conducts based on the fixed oscillator clock, causing the inductor current to rise. As shown in Figure 2, when V_{RAMPx} (I_{SENx} plus compensation slope) reaches V_{COMP} (the output voltage of Gm1), the low-side MOSFET is turned off, and the high-side MOSFET is turned on after a dead time, t_{DT2}. The high-side MOSFET will turn off when the next PWM cycle clock occurs or when the inductor current reaches zero during PFM operation.

The SA22900 achieves current sharing capability by comparing each phase V_{RAMPx} with the same V_{COMP}. As a result, the peak value of V_{RAMPx} for each phase is identical. Due to the consistent compensation slope between the two phases, the peak current of each phase is also controlled to be the same.

Power on Sequence

The recommended power-on sequence is as follows: the device should be enabled after the input voltage exceeds 5V. This ensures that the internal LDO produces a VCC that is higher than the rising threshold of 4.5V (typical), resulting in reliable power-on performance. When powering off, it is also recommended to disable the device when the input voltage exceeds 5V.

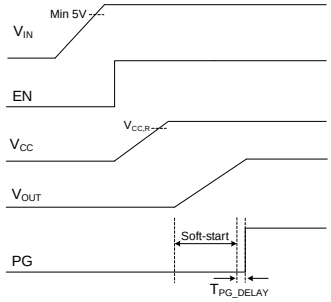


Figure3. Power On Sequence

Enable

EN is a high-voltage capable input with a stable threshold that provides control of device start-up logic. Pulling the EN pin low (<0.95V) will shut down the device. During shutdown mode, driving the EN pin high (>1.21V) will turn the IC on again.

Operation Mode Configuration

For light load current when $I_{OUT} < 0.5\Delta I_L$, the current through the inductor will ramp down to near zero before the next period begins. Under these conditions, the device can operate in pulse frequency modulation (PFM) mode to optimize efficiency or be forced into continuous conduction mode (FCCM) with a fixed operating frequency.

The SA22900 supports a spread spectrum (SPS) function to optimize EMI performance. This spread spectrum architecture varies the switching frequency, significantly reducing both peak radiated and conducted noise.

The operating frequency varies ±10% around the frequency set by R_{FS}. The modulation signal is a triangular wave with a period of 230 µs. With this method, f_{SW} decreases by 10% and returns to the set frequency in 115 µs, and then increases by 10% and returns to the set frequency in 115 µs.

The internal spread spectrum does not interfere with the external clock applied to the FS/SYNC pin. It is active only when the device operates with an internally generated switching frequency.

The SA22900 automatically performs phase shedding based on the voltage of V_{IMON} when the phase dropping function is enabled. When the load current decreases and V_{IMON} falls below 1.1V, Phase 2 is disabled. Conversely, when the load current increases and V_{IMON} exceeds 1.15V, Phase 2 is enabled. When the SPS/FCH1 pin is pulled high, the SA22900 operates in forced single-phase mode.

As the following table shows, all these functions can be configured by the MODE/PHD pin and the SPS/FCH1 pin.

SPS/FCH1 / MODE/PHD	GND	VCC	FLOAT
GND	2-phases FCCM SPS OFF	1-phase FCCM SPS OFF	2-phases FCCM SPS ON
VCC	2-phases PFM SPS OFF	1-phase PFM SPS OFF	2-phases PFM SPS ON
FLOAT	2-phases PFM SPS OFF Enable phase drop	1-phase FCCM SPS ON	2-phases PFM SPS ON Enable phase drop

Table 1: Mode Configuration Table

Soft Start

The SA22900 provides a programmable soft-start time to limit inrush current during startup. Connecting a capacitor between the SS pin and GND sets the soft-start time. The voltage at the SS pin ramps up via a 4.9 μA current source, providing the reference for the FB during the soft-start period.

For the boost converter, the output voltage is pre-charged to approximately VIN through the body diode of the high-side MOSFET. Meanwhile, the SS pin will be pre-biased to the corresponding FB voltage. The soft start time can then be calculated using the following equation, as the output voltage rises from VIN to the final setting voltage V_{OUT_SET}:

$$t_{ss} = V_{REF} \times \left(1 - \frac{V_{IN}}{V_{OUT\_SET}}\right) \times \frac{C_{SS}}{4.9\mu A}$$

External Bootstrap Capacitor

This device integrates a floating power supply for the gate drivers that control the high-side switches. Proper operation requires a 470 nF low ESR ceramic capacitor to be connected between the BS and the LX pins. This bootstrap capacitor supplies the gate driver voltage for the high-side power MOSFETs.

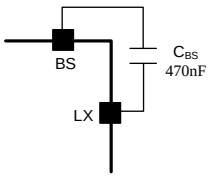


Figure4. External BS Capacitor

Programmable Adaptive Dead Time Control

The SA22900 can program adaptive dead time for drivers to optimize operation under different conditions. Adjusting dead time for various external MOSFET applications will simultaneously maximize efficiency and prevent shoot-through. The selection of RDT resistance and dead time is shown in Figure 5, where t_{DT1} represents the dead time from TG falling to BG rising, and t_{DT2} represents the dead time from BG falling to TG rising. The minimum recommended RDT resistor is 5 kΩ.

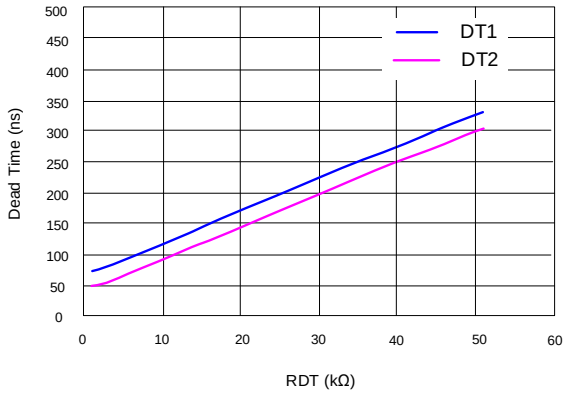


Figure 5. Dead Time vs RDT

Minimum On-Time (Blank Time)

The minimum on-time of BGx can be programmed using the R_{BLANK} resistor. The minimum on-time should be set with consideration for the minimum duty cycle application, particularly when VIN is close to VOUT. This design also aims to allow the internal circuits to filter out noise spikes after BGx turns on. A 5 kΩ resistor is recommended as the minimum blanking time resistor. Figure 6 illustrates the selection of the appropriate R_{BLANK} and minimum on-time.

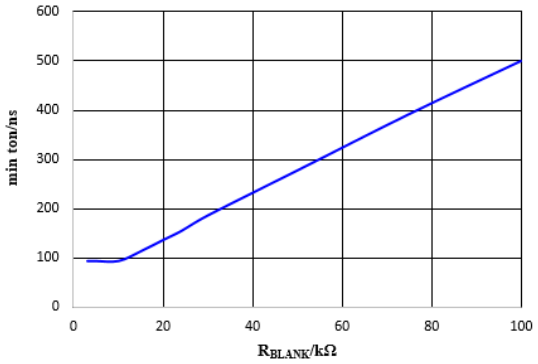


Figure 6. Minimum ton vs R_{BLANK}

Frequency and Synchronization

The FS/SYNC pin can be used to set the switching frequency (f_{SW}) of the device by connecting a resistor from the FS/SYNC pin to GND. The switching frequency is adjustable from 50 kHz to 1.1 MHz. It can be calculated using the following equation, and Figure 7 illustrates the relationship between frequency and R_{FS}.

$$f_{SW} = \frac{1.257 \times 10^{10}}{R_{FS}(\Omega) + 1369.5}(Hz)$$

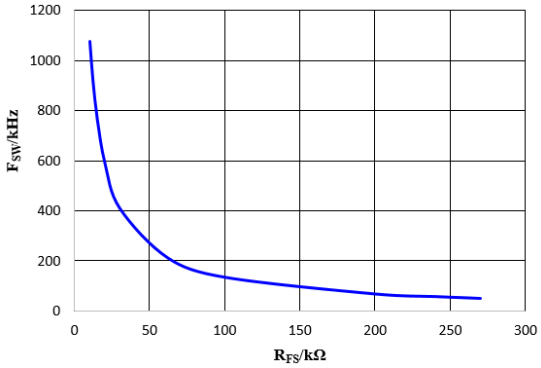


Figure 7. f_{SW} vs R_{FS}

The switching frequency of the SA22900 can be synchronized with an external clock signal applied to the FS/SYNC pin. It detects the rising edge of the input clock and synchronizes the rising edge of BG1 with a t_{DT1} delay. The switching frequency of each phase is equal to the SYNC clock frequency.

The CLK pin outputs a clock signal with a switching frequency. Its amplitude is VCC, and the pulse width is $t_{SW}/12$. The rising edge of the CLK signal is delayed by $t_{SW}/4$ - t_{DT1} after the rising edge of BG1. Connect the master CLK pin to the slave FS/SYNC pin for 4-phase interleaved operation. The rising edge of BG1 in the slave IC is delayed by 35 ns + tDT1. Therefore, the total delay time between BG1_slave and BG1_master is $t_{SW}/4$ + 35 ns, resulting in an approximate 90° phase shift.

4-Phase Operation

Two SA22900 devices can be used in parallel to achieve 4-phase interleaved operation. Connect the master CLK pin and the slave FS/SYNC pin together to synchronize the switching frequency. The phase shift is approximately 90° between BG1_master and BG1_slave, enabling 4-phase interleaved operation. Additionally, the respective COMP, FB, SS, EN, and IMON pins should be connected between the two devices.

Current Sense

The SA22900 peak current control architecture requires continuous sampling of the inductor current for rapid control. The SA22900 current sense amplifier continuously monitors the I_{Lx} signal by measuring the voltage across R_{SENx}.

The sense current of each phase is used for peak current limit (OC1), peak current protection (OC2), constant current mode (CC), average overcurrent protection (AVG_OC), current balance, and phase drop functions in multi-phase applications. Figure 8 illustrates the internal circuit for the individual phase current sense module.

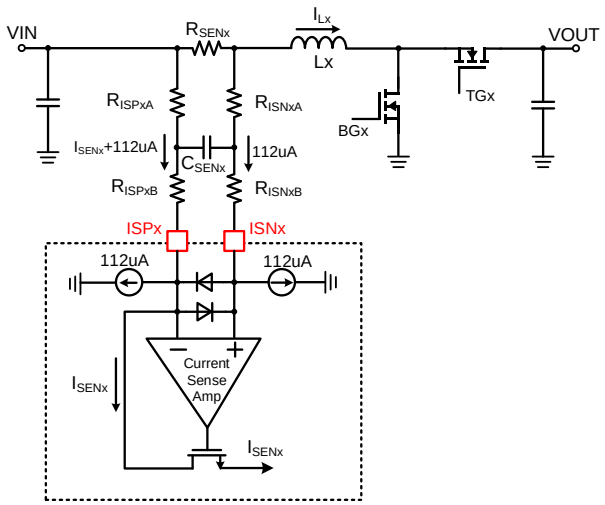


Figure 8. Current Sense Block

As shown in Figure 8, the RC network between the R_{SENx} and ISPx/ISNx pins is the recommended configuration. The ISPx pin should be connected to the positive terminal of R_{SENx} through the resistor R_{ISPx}. R_{ISPx} is used to set the current sense gain externally and is composed of R_{ISPxA} and R_{ISPxB}.

$$R_{ISPx} = R_{ISP\times A} + R_{ISP\times B}$$

There is a 112 μA bias current sink, connected to the ISPx and ISNx pins. The ISNx pin should be connected to the negative side of R_{SENx} through resistor R_{ISNx}. R_{ISNx} is composed of R_{ISNxA} and R_{ISNxB} and should have the same value as R_{ISPx}. It is recommended to set R_{ISPxA} equal to R_{ISNxA} and R_{ISPxB} equal to R_{ISNxB}, and to insert a capacitor C_{SENx} between them, as shown in Figure 8. The symmetrical circuit will help filter noise from the small current sense signals.

$$R_{ISNx} = R_{ISN\times A} + R_{ISN\times B}$$

$$R_{ISPx} = R_{ISNx}$$

The I_{SENx} is the output of the current sense amplifier and is proportional to each phase inductor current I_{Lx} due to the circuit structure.

$$I_{SENx} = I_{LX} \times \frac{R_{SENx}}{R_{ISPx}}$$

Average Current Monitor (IMON)

The IMON pin is used to monitor the total average input current of the two-phase boost converter. The IMON current can be calculated using the following equation: the single-phase sense current is divided by 8, summed together, and then a 17μA bias current is added to the sum.

$$I_{IMON} = \frac{I_{SEN1} + I_{SEN2}}{8} + 17 \times 10^{-6}$$
$$= \frac{I_{L1} \times R_{SEN1}}{8 \times R_{ISP1}} + \frac{I_{L2} \times R_{SEN2}}{8 \times R_{ISP2}} + 17 \times 10^{-6}$$

Considering that, for most applications, two phases are consistent, Assume RSEN1 = RSEN2 = RSEN and RISP1 = RISP2 = RISP. The total current of I_{L1} and I_{L2} is the input average current I_{IN}. Thus, the equation can be simplified:

$$I_{IMON} = \frac{I_{IN} \times R_{SEN}}{8 \times R_{ISP}} + 17 \times 10^{-6}$$

Place a resistor R_{IMON} between IMON and GND to convert the IMON current into IMON voltage. Additionally, place a capacitor C_{IMON} between IMON and GND to filter out the ripple, allowing the IMON voltage to represent the total input average current of the two phases. The IMON voltage can be calculated as follows:

$$V_{IMON} = I_{IMON} \times R_{IMON}$$

As shown in Figure 2, V_{IMON} is configured for the 'Constant Current Control & AVG_OC Protection' module and the comparator for phase drop, serving the following functions:

1. Constant current (CC) control is used for input current limit. The reference of CC control is 1.6V, when V_{IMON} increases to 1.6V, the SA22900 will work in CC mode and the input constant current can be calculated as follows:

$$I_{IN\_CC} = \left(\frac{1.6}{R_{IMON}} - 17 \times 10^{-6}\right) \times \frac{R_{ISP}}{R_{SEN}} \times 8(A)$$

2. AVG_OC is used for input over current protection. When V_{IMON} is above 2V, the AVG_OC fault is triggered. SA22900 stops switching and enters either hiccup or latch-off mode which set by PRT pin. Due to the constant current loop limiting V_{IMON} signal to around 1.6V, AVG_OC is not easily triggered and is used as a last resort protection.

$$I_{IN\_AVG\_OC} = \left(\frac{2}{R_{IMON}} - 17 \times 10^{-6}\right) \times \frac{R_{ISP}}{R_{SEN}} \times 8(A)$$

3. When phase dropping function is enabled, SA22900 will do phase shedding automatically according to the voltage of V_{IMON}. The phase dropping mode is not allowed under external clock synchronization.

   When the load current decreases and V_{IMON} falls below 1.1V, Phase 2 is disabled. The current dropping threshold can be calculated using:

$$I_{IN\_DROP} = \left(\frac{1.1}{R_{IMON}} - 17 \times 10^{-6}\right) \times \frac{R_{ISP}}{R_{SEN}} \times 8(A)$$

   When the load current increases and V_{IMON} exceeds 1.15V, Phase 2 is enabled. The current threshold for activation can be calculated using the following formula:

$$I_{IN\_ADD} = \left(\frac{1.15}{R_{IMON}} - 17 \times 10^{-6}\right) \times \frac{R_{ISP}}{R_{SEN}} \times 8(A)$$

Slope Compensation

For constant frequency with peak current mode control, slope compensation should be considered when the duty cycle exceeds 50%. By connecting a resistor, R_{SLOPE}, from the SLOPE pin to ground, the SA22900 can adjust the slope compensation value. This feature offers greater flexibility in the selection of external components.

It is necessary to design slope compensation appropriately. If the slope compensation is too low, the converter may exhibit subharmonic oscillation. Conversely, if the slope compensation is excessive, the phase margin of the device will be reduced.

Figure 9 illustrates a block diagram related to slope compensation. For current mode control, the compensation slope rate K_{SL} must theoretically exceed 50% of the slope rate KF, as depicted in Figure 9.

R_{SLOPE} can be calculated using the following equation:

$$R_{SLOPE} = \frac{6.67 \times 10^5 \times L_x \times R_{ISPx}}{K_{SLOPE} \times (V_{OUT} - V_{IN}) \times R_{SENx}}$$

In the formula, K_{SLOPE} represents the gain of the compensation slope compared to the descent slope of the inductor current. For example, the compensation slope is equal to the descent slope of the inductor current when K_{SLOPE} = 1. In theory, K_{SLOPE} should be greater than 0.5; however, in practical applications, K_{SLOPE} is typically greater than 1.

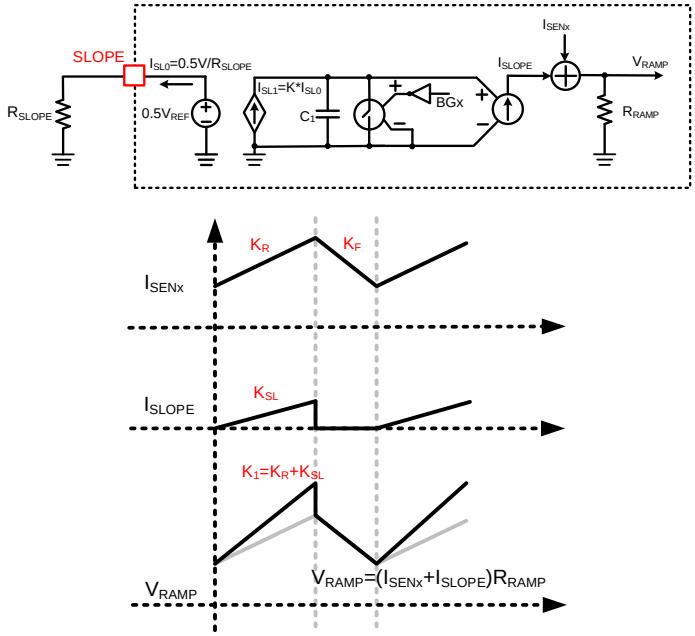


Figure 9. Slope Compensation Block and Waveform

Digital/Analog Track Function

The SA22900 features a unique tracking function that can accept either digital or analog signals, allowing users to adjust the reference voltage externally. By connecting the STRK pin to GND or VCC, the TRACK pin can receive digital or analog signals. Figure 10 illustrates the block diagram of the tracking function. Gm1 utilizes the lowest voltage among SS, TRK_REF, and 1.6V_{REF} as the actual reference voltage. When TRK_REF is the lowest voltage, the output voltage can be adjusted based on the variation of the TRACK signal.

When STRK=GND (DTRK mode), the TRACK pin receives a digital signal input. As shown in Figure 10, V_1 is the output of the selector. The PWM signal at the TRACK pin controls the switching of Q_1 and Q2. V_1 is a PWM signal with a 2.5V amplitude and a duty cycle D (where D is the duty cycle of the TRACK PWM signal). After the 2-stage RC filter, the TRK_REF voltage can be calculated by:

$$V_{TRK\_REF} = 2.5D$$

The amplitude of the PWM signal at the TRACK pin does not affect the TRK_REF accuracy; only the duty cycle alters the TRK_REF value. The cutoff frequency of the 2-stage low-pass RC filter is designed to be approximately 1.75 kHz. Due to the fixed bandwidth, the frequency for the track signal is recommended to be set around 400 kHz.

When STRK=VCC (ATRK mode), the TRACK pin receives an analog signal input. As shown in Figure 10, V_2 is the output of the selector. With the same 2-stage RC filter, the TRK_REF value is equal to the voltage on the TRACK pin.

For the track function, TRK_REF has an effective range. When TRK_REF exceeds 1.6V, Gm1 will use 1.6V_{REF} as the actual reference, rendering the track function inactive. There is no limit on the minimum voltage of TRK_REF; however, for the boost converter, the minimum output voltage is VIN minus the body diode drop of the high-side MOSFET. Therefore, the corresponding FB voltage represents the minimum effective voltage for TRK_REF. It is important to note that the SS_DONE signal checks if TRK_REF is greater than or equal to 0.3V as one of the conditions for judgment; thus, TRK_REF should exceed 0.3V to ensure a proper soft start.

If the track function is not used, the TRACK pin should be connected to VCC, and the internal reference will be fixed at 1.6 V.

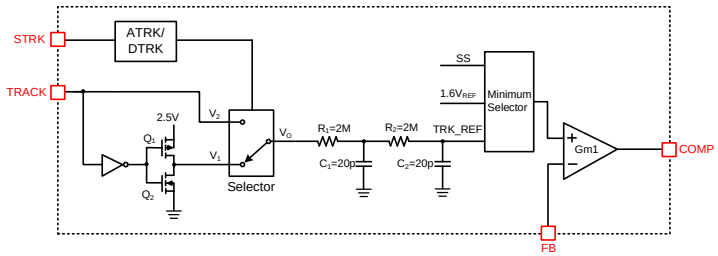


Figure 10. Track Function Block

Fault Protections

The SA22900 features comprehensive fault protection and current limiting to ensure reliability. By configuring the PRT pin, the protection response can be selected as either Hiccup or Latch-off.

When the PRT pin is pulled high (e.g., VCC), the SA22900 operates in hiccup mode for protection. If a fault condition is detected, the device ceases switching and restarts after 500 ms. This operation will continue to repeat until the fault is cleared.

When the PRT pin is pulled low (e.g., to GND), the SA22900 operates in latch-off mode for protection. If a fault condition is detected, the device ceases switching and will not restart, even after the fault has been removed.

The fault lists which can be set with hiccup or latch-off response are shown below:

Fault	Trigger condition and description
VIN_OV	Input overvoltage protection, (VIN>58V)
AVG_OC	Input average overcurrent protection, (IMON>2V)
OC2_PEAK	Peak current protection, (I_{SENx}>105μA)
VOUT_OV	Output overvoltage protection, (FB>120%V_{REF})

Input Overvoltage Protection

The SA22900 samples the VIN pin voltage divided by 48 (VIN/48) to obtain input voltage information. By using a comparator to compare VIN/48 to a 1.21V reference, the SA22900 can detect if a VIN_OV fault is triggered. When VIN exceeds 58V for 5μs, the VIN_OV fault is activated, and the PG pin is pulled down. The SA22900 stops switching and enters either hiccup mode or latch-off mode, depending on the PRT pin voltage. VIN_OV fault detection is activated at the beginning of the soft-start process.

Average Overcurrent Protection (AVG_OC)

When V_{IMON} exceeds 2V, an AVG_OC fault is triggered. The SA22900 ceases switching and enters either hiccup mode or latch-off mode.

Peak Current Protection (OC2)

The SA22900 features peak current protection (OC2) for the inductor current. The internal overcurrent protection threshold (OC2_TH) is 105 μA. When I_{SENx} reaches 105 μA in each phase, the OC2 fault is triggered. The SA22900 stops switching and enters either hiccup mode or latch-off mode. In hiccup mode, when both phases fall below 105 μA, the device will resume normal operation after completing a full soft-start cycle.

The peak current protection (OC2) for inductor current can be calculated by:

$$I_{OC2x} = 105 \times 10^{-6} \times \frac{R_{ISPx}}{R_{SENx}} (A)$$

Output Overvoltage Protection

The SA22900 samples the feedback (FB) voltage to detect an output overvoltage fault (VOUT_OV). If the FB voltage exceeds 120% of the reference voltage (VREF), the VOUT_OV fault is triggered, causing the power-good (PG) pin to be pulled down. The SA22900 ceases switching and enters either hiccup mode or latch-off mode. In hiccup mode, when the FB voltage falls below 116% of V_{REF}, the device will resume normal operation after completing a full soft-start cycle. VOUT_OV fault detection is activated at the beginning of the soft-start process.

$$V_{OUT\_OV\_RISE} = 1.2 \times V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

$$V_{OUT\_OV\_FALL} = 1.16 \times V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Output Undervoltage Protection

The SA22900 samples the feedback (FB) voltage to detect whether there is an output undervoltage fault (VOUT_UV). If the FB voltage is lower than 80% of V_{REF}, the VOUT_UV fault is triggered, and the power good (PG) pin is pulled down. However, the SA22900 will continue switching and operate normally without initiating any fault protection action. When the FB

voltage rises above 84% of V_{REF}, the PG pin will be pulled high after a delay.

$$V_{OUT\_UV\_FALL} = 0.8 \times V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

$$V_{OUT\_UV\_RISE} = 0.84 \times V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Peak Current Cycle-by-Cycle Limit (OC1)

The SA22900 features cycle-by-cycle peak current limiting (OC1) for the inductor current without hiccup or latch-off protection. The OC1 protection for both phases is independent. The internal peak current limit threshold (OC1_TH) is 80 μA. When I_{SENx} reaches 80 μA in each phase, the OC1 fault will be triggered. Subsequently, the BGx of the corresponding phase is turned off to prevent the inductor current from rising further on a cycle-by-cycle basis.

The peak current limit (OC1) for inductor current can be calculated by:

$$I_{OC1x} = 80 \times 10^{-6} \times \frac{R_{ISPx}}{R_{SENx}} (A)$$

Negative Current Cycle-by-Cycle Limit (OC_NEG)

The SA22900 features cycle-by-cycle negative current limit (OC_NEG) for the inductor current without hiccup or latch-off protection. The OC_NEG protection for both phases is independent. The internal negative current limit threshold (OC_NG_TH) is -48 μA. When I_{SENx} reaches -48 μA for each phase, the OC_NEG fault will be triggered. Subsequently, the TGx of the corresponding phase is turned off to prevent the inductor current from ramping down cycle by cycle. The negative current limit (OC_NEG) for the inductor current can be calculated as follows:

$$I_{OCNEGx} = -48 \times 10^{-6} \times \frac{R_{ISPx}}{R_{SENx}} (A)$$

Over-temperature Protection (OTP)

The device includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This circuitry will shut down switching operation when the junction temperature exceeds 160°C. Once the junction temperature cools down by approximately 20°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, ensure adequate cooling so that the junction temperature does not exceed the OTP threshold.

PGOOD Signal

PG is an open-drain output pin. This pin will pull to ground if the output voltage is lower than 80% of the regulation voltage or higher than 120% of the regulation voltage. Otherwise, this pin will enter a high-impedance state if the output voltage is higher than 84% of the regulation voltage or lower than 116% of the regulation voltage. When another fault is triggered (e.g., VIN_OV), the PG pin will also pull to ground. After the fault is removed, PG will reset to high after a delay of 0.5 ms.

PVCC &VCC

An internal linear regulator produces a 5.2V supply at PVCC from VIN. It is recommended to connect a 10μF/10V or higher X7R type ceramic capacitor between PVCC and PGND. VCC should be connected to PVCC through an RC filter to reduce noise for the internal analog circuit. Typically, a ceramic capacitor (e.g., 1μF) should be connected from VCC to GND, along with a small resistor (e.g., 10Ω) from PVCC to VCC.

Application Information

Feedback Resistor Divider R_{FB1} and R_{FB2}

Choose R_{FB1} and R_{FB2} to program the desired output voltage. To minimize power consumption under light load conditions, it is advisable to select large resistance values for both R_{FB1} and R_{FB2}. A resistance value between 10 kΩ and 1 MΩ is recommended for both resistors. If R_{FB1} is selected, R_{FB2} can be calculated using the following formula:

$$R_{FB2} = \frac{V_{REF} \times R_{FB1}}{V_{OUT} - V_{REF}} (\Omega)$$

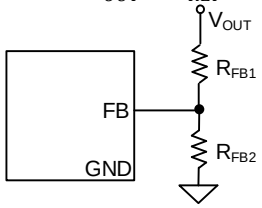


Figure 11. Feedback Resistor Divider

Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\sqrt[2]{3} \times L \times f_{SW} \times V_{OUT}} (A)$$

To minimize potential noise issues, place a typical X5R or better grade ceramic capacitor very close to the power input and PGND. Care should be taken to minimize the loop area formed by C_{IN}, the input, and PGND. In this case, a minimum of a 22 µF low ESR ceramic capacitor is recommended for the power input.

Output Capacitor C_{OUT}

Both steady-state ripple and transient requirements must be considered when selecting this capacitor. Therefore, a combination of electrolytic and ceramic capacitors is used in the SA22900.

Using several ceramic capacitors in parallel will effectively filter high-frequency spikes. These capacitors should be placed as close as possible to the switches. For optimal performance, it is recommended to use X5R or a higher-grade ceramic capacitor with a rating of 100V and a capacitance greater than 10µF. Electrolytic capacitors placed in parallel can be used to improve load transients and reduce output ripple due to their larger capacitance values.

Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be around 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{f_{SW} \times I_{OUT\_MAX} \times 40\%} (H)$$

Where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current. The SA22900 is less sensitive to variations in ripple current. Consequently, the final choice of inductance may differ slightly from the calculated value without significantly impacting performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions. The maximum peak current happens under minimum input voltage condition.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN\_MIN}}\right) \times I_{OUT\_MAX} + \frac{V_{IN\_MIN}}{V_{OUT}} \times \frac{(V_{OUT} - V_{IN\_MIN})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to meet the desired efficiency requirements. It is desirable to choose an inductor with DCR<5mΩ to achieve a good overall efficiency.

Power MOSFET

The voltage rating of the power MOSFET should be selected to exceed the maximum drain-to-source voltage. For safe operation, an adequate voltage margin should be considered.

Loop Compensation

The SA22900 incorporates a peak current mode control scheme, which consists of two feedback loops. The inner loop, known as the current loop, does not require any external compensation components. In contrast, the outer loop, referred to as the voltage loop, is compensated using external components.

In most applications, a Type A or Type B compensation network, as shown in Fig. 12a and Fig. 12b, can be used to stabilize the voltage loop. Type A is the most widely used and functions effectively for power stages lagging down to -90˚, where the boost provided by the output capacitor's ESR must be canceled. Type B is used when the effect of the output capacitor's ESR can be neglected.

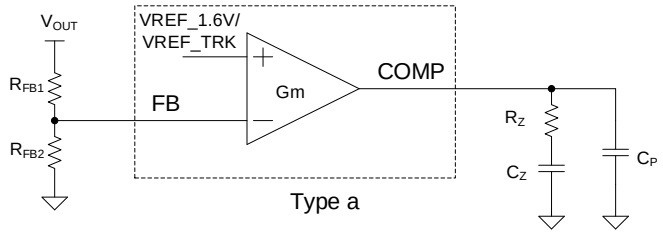


Figure.12a Type A Loop Compensation

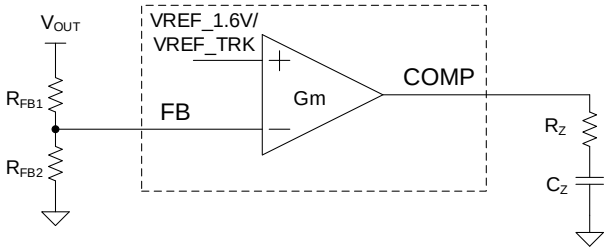


Figure.12b Type B Loop Compensation

To calculate the output voltage sense loop external components, follow the following steps.

1. Select the crossover frequency f_C of the closed loop. It is recommended that the crossover frequency f_C is selected as 1/5 of the right half plane zero (f_{RHPZ}) and 1/10 of the switching frequency for the tradeoff of stability and transient response of the system. The system has faster response at higher crossover frequency.

$$f_{RHPZ} = \frac{(1 - D_{MAX})^2 \times V_{OUT}}{2\pi \times L \times I_{OUT}}$$

For a single phase, L represents the inductance. For multiphase systems, L is equal to 1/N of the single-phase inductance, where N is the number of phases. This value represents the equivalent inductance for a multiphase boost converter with N phases.

2. Select a R_Z value of the R-C series combination connected to the COMP pin.

$$R_Z = \frac{V_{OUT}}{G_{m1} \times G_{fc} \times V_{REF}}$$

Where G_{m1} is the error amplifier gain 2mS, G_{fc} is gain of the power stage at crossover frequency.

$$G_{fc} = \frac{(1 - D_{MAX})}{2\pi \times f_C \times C_{OUT} \times R_i}$$

Where R_i is the current sense gain:

$$R_i = \frac{6500 \times R_{SEN}}{N \times R_{SET}}$$

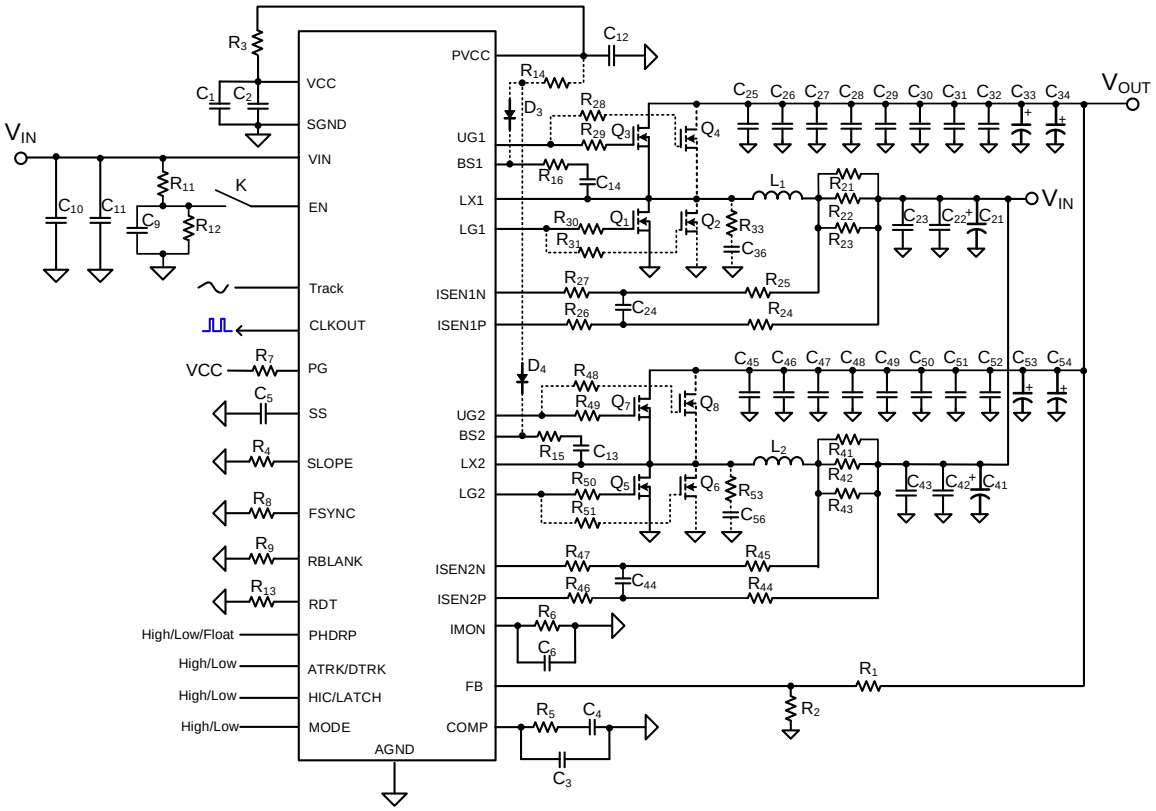
3. Select a C_Z value of the R-C series combination connected to the COMP pin. The capacitor C_Z is used for obtaining enough DC gain of loop. The place of the compensation zero decides phase margin at the crossover frequency. Place the compensation zero at or before the dominant pole of R_L and C_{OUT}. R_L is the load resistance, which equals to V_{OUT}/I_{OUT}.

$$C_Z = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_Z}$$

4. A high frequency pole is recommended to attenuate the high frequency noise. Place this pole to cancel the ESR zero of C_{OUT}

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_Z}$$

Application Schematic (V_{OUT} = 25V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
Q1,Q3,Q5,Q7	NMOS		
C21,C31,C33,C34,C53,C54	100μF/100V, Electrolytic Capacitor		
C1	1μF/25V/X7R,0603	C1608X7R1E105K	TDK
C2,C4,C6,C10	0.1μF/100V/X7R,0603	C1608X7R1H104K	TDK
C3,C9,C24,C44	1nF/50V/X7R,0603	C1608X7R1H102K	TDK
C5	47nF/50V/X7R,0603	C1608X7R1H473K	TDK
C11	1μF/100V/X7S,0805	C2012X7S2A105K	TDK
C12	10μF/25V/X5R,0603	C1608X5R1E106M	TDK
C13,C14	470nF/50V/X7R,0603	C1608X7R1H474K	TDK
C22,C23,C25….C32, C42,C43,C45….C52,	1μF/100V/X7R,1206	C3216X7R2A105K	TDK
R1	100K, 1%, 0603		
R2	6.8K, 1%, 0603		
R3,R24,R25,R29,R30, R44,R45,R49,R50	10Ω, 1%, 0603		
R4	15K, 1%, 0603		
R5	5.1K, 1%, 0603		
R6	62K, 1%, 0603		
R7	10K, 1%, 0603		
R8,R9	30K, 1%, 0603		
R11	10K, 1%, 0603		
R12	1M, 1%, 0603		
R13	20K, 1%, 0603		

Reference Designator	Description	Part Number	Manufacturer
R15,R16	0Ω, 1%,0603		
R21,R22,R23,R41,R42,R43	3mΩ, 1%, 1206		
R26,R27,R46,R47	430Ω, 1%,0603		
Q2,Q4,Q6,Q8,R28,R31,R48,R51, R33,C36,R53,C56,R14,D3,D4	Spare		
L1,L2	3.3μH	PCMB104T-3R3MS	Cyntec

Recommend Components for Typical Applications

Output Voltage (V)	$R_Z(R_5)$	$C_Z(C_4)$	$C_P(C_3)$	R_1(kΩ)	R_2(kΩ)	L_1/Part Number
25	5.1K	100nF	1nF	100	6.8	3.3μH/ PCMB104T-3R3MS
45	5.1K	220nF	10nF	100	3.6	3.3μH/ PCMB104T-3R3MS

Layout Design

1. It is desirable to maximize the PCB copper area connecting to PGND/GND pin to achieve better thermal performance and noise immunity. If the board space allows, a designated ground plane layer is highly recommended.
2. C_{IN} must be close to VIN and GND pins.
3. C_{OUT} must be close to power MOSFETs. The loop area formed by C_{OUT}, LX and PGND pins must be minimized.
4. The PCB copper area associated with LX pin must be minimized to improve the noise immunity.
5. The components R_{FB1} and R_{FB2} and the trace connecting to the FB pin must NOT be adjacent to the LX/BG/TG/BS nodes on the PCB layout to minimize the noise coupling to FB pin.
6. Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.
7. Place the PVCC capacitor close to PVCC pin using short, direct copper trace to one nearest device PGND pin.
8. Place the VCC capacitor close to VCC pin using short, direct copper trace to one nearest device GND pin.
9. Keep the driver traces as short as possible with relatively large width.
10. The components R_{ISPxB}, R_{BIASxB}, and C_{SENx} should be placed as close as possible to the IC and must NOT be adjacent to the LX/BG/TG/BS nodes on the PCB layout to minimize the noise coupling.

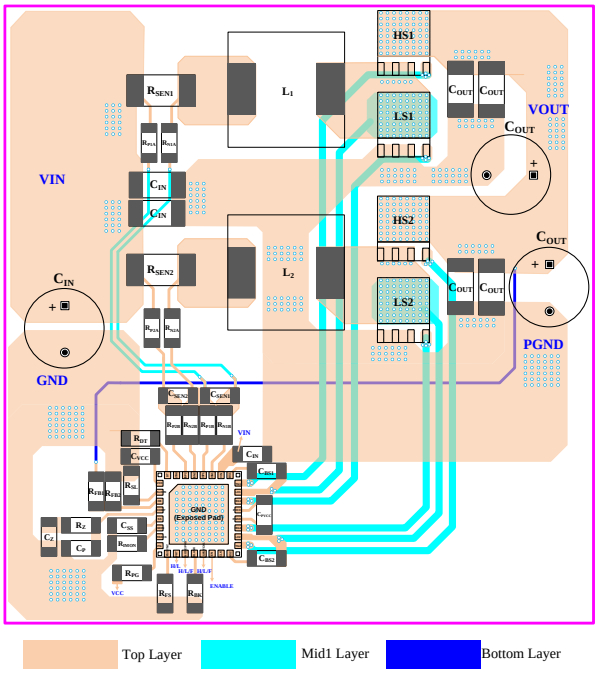
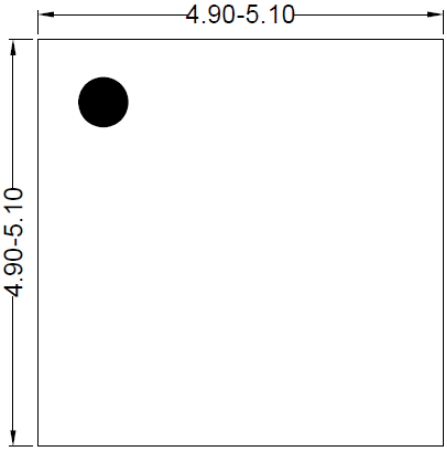
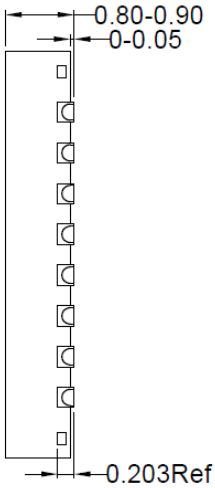


Figure 13. PCB Layout Suggestion

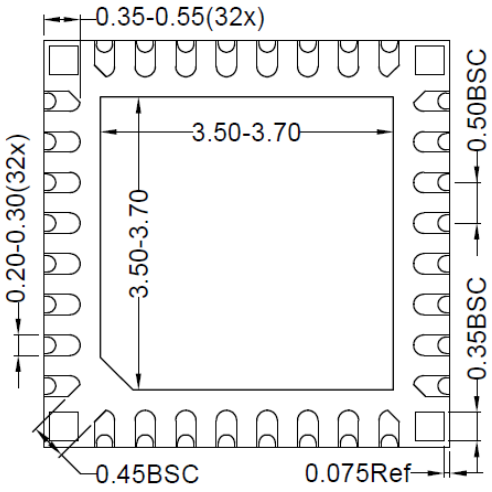
QFN5x5-32 Package Outline Drawing



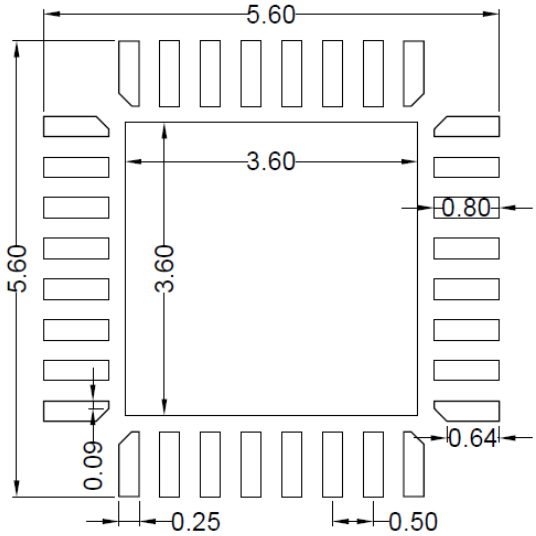
Top View



Side View



Bottom View

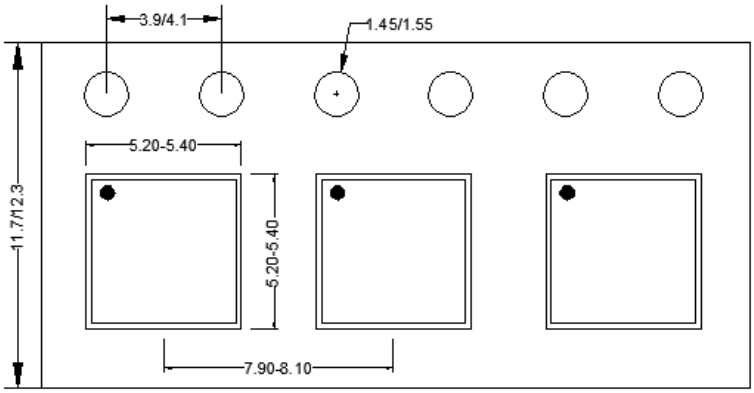


Recommended PCB layout
(Reference only)

Notes: *All dimensions in millimeter and exclude mold flash & metal burr.*

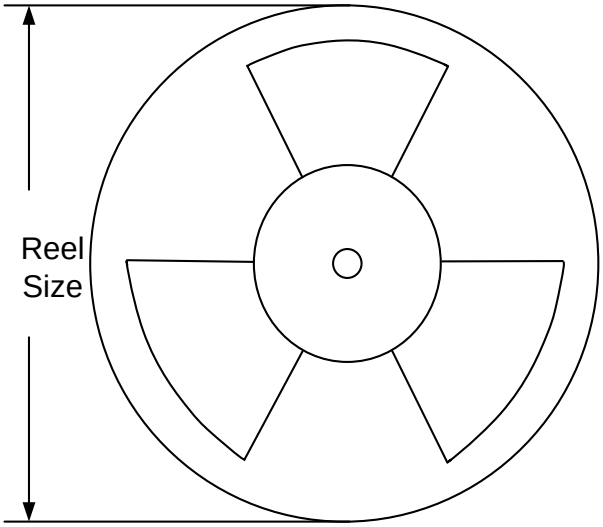
Tape and Reel Information

Tape Dimensions and Pin1 Orientation



Direction of Feed ⟶

Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5x5-32	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warranted. Please ensure that you have the latest revision.

Date	Revision	Change
Mar. 26, 2026	Revision 1.0B1	Update the Pin Description of Pin 4 (COMP). Delete the description of “Clamping the IMON voltage to COMP pin using a diode activates the constant input average current control.” on Page 4
July 25, 2025	Revision 1.0B	1. Delete Ambient Temperature on Page 7 2. Corrected the Dead Time Value on Page 9 3. Corrected the SPS switching frequency on Page 17 4. Corrected the *Figure 5. Dead time vs RDT* on Page 18 5. Corrected the wiring error in the Soft Start on Page 18 6. Corrected the wiring error in the Fault Protection on Page 21
May 29, 2025	Revision 1.0A	Corrected the wiring error in the schematic diagram on Page 25
Dec.11, 2024	Revision 1.0	Initial Release

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