SY86802L

2.5V to 16V Protection Switch with Blocking FET Control

General Description

The SY86802L is a highly integrated protection switch and robust defense against over current, shorts circuits, excessive inrush current, and reverse current.

Extremely low power path resistance $R_{DS(ON)}$ helps to reduce power loss during the normal operation. An open-drain indicator pin is opened to show the operation status of device. It integrates the over-temperature protection and over current protection with latch off mode.

Current limit level can be set with a single external resistor. Applications with particular voltage ramp requirements can set the SST pin with a single capacitor to ensure proper output ramp rates. The SY86802L can be connected "Back-to-Back" with an external NFET which driven by the BFET pin to prevent current flow from load to source.

The SY86802L adopts compacted QFN2×2-12 footprint.

Features

- 2.5V to 16V Input Voltage Range
- Extremely Low Power Path Resistance $R_{DS(ON)}$ $R_{DS(ON)}$=30mΩ (typ.)
- Open-drain Indicator Pin for Operation Status
- 1A to 5A Adjustable I_{ILMT}
- ±10% I_{ILMT} Accuracy at 3A
- Reverse Blocking Support when EN OFF
- Programmable OUT Slew Rate
- Built-in Thermal Shutdown and Latch-off
- RoHS Compliant and Halogen Free
- Small Footprint –QFN (2mm×2mm)

Applications

- Power Bank
- LCD Panel
- HDD and SSD Drives
- Set Top Boxes
- Servers / AUX Supplies
- Fan Control
- PCI/PCIe Cards
- Adapter Powered Devices

Ordering Information

SY86802 □(□□□)

Package Code

Optional Spec Code

Ordering Number	Package Type	Note
SY86802LTLQ	QFN2×2-12	----

Typical Applications

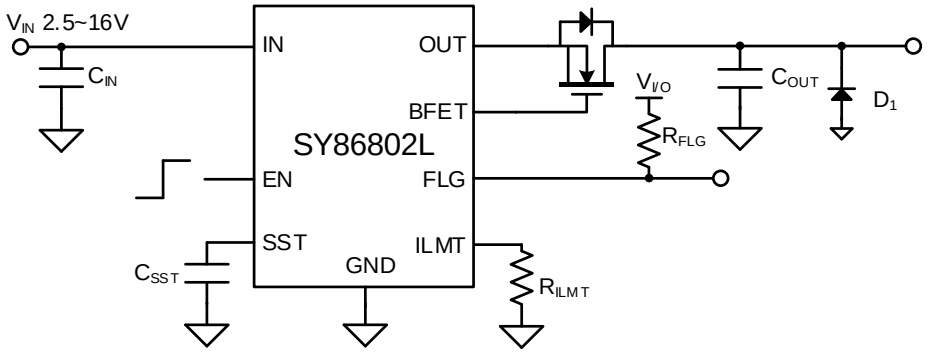
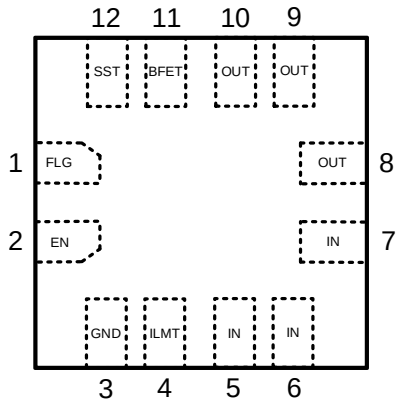


Figure1. Schematic Diagram

Pinout (top view)



(QFN2×2-12)

Top mark: h6***xyz*** (Device code: h6, ***x=year code, y=week code, z= lot number code***)

Pin Name	NO.	Pin Description
FLG	1	Open-drain indicator pin. FLG will be pulled down when over current, short circuit or thermal shutdown occurs.
EN	2	Pull high to enable the SY86802L. Do not leave it floating.
GND	3	GND.
ILMT	4	A resistor from this pin to GND will set the over current limit.
IN	5, 6, 7	Input voltage and supply voltage; connect a 1μF or greater ceramic capacitor from IN to GND as close to the device as possible.
OUT	8, 9, 10	Power-switch output.
BFET	11	Connect this pin to the gate of a blocking NFET. This pin can be left floating if it is not used.
SST	12	Connect a capacitor from this pin to GND to control the ramp rate of OUT at device turn-on.

Block Diagram

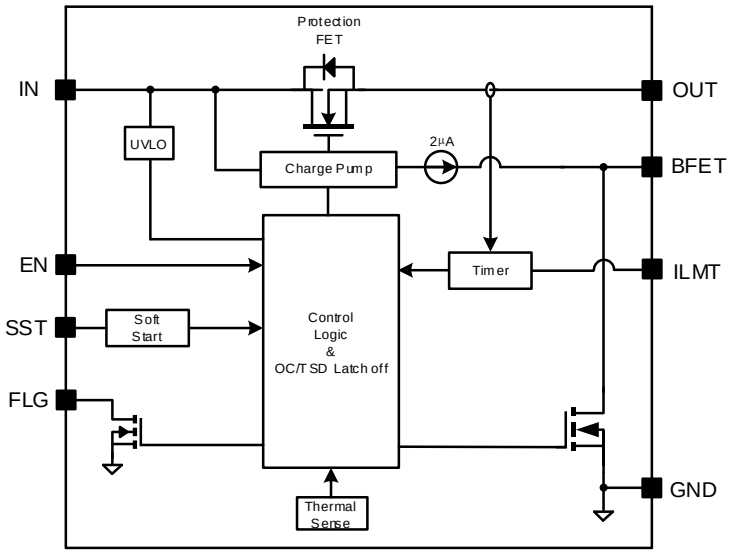


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, EN, FLG ---------- -0.3V to 18V
OUT ---------- -0.3V to IN+0.3V
BFET ---------- -0.3V to 26V
ILMT, SST ---------- -0.3V to 3.6V
FLG Continuous Output Sink Current ---------- 25mA
BFET Continuous Output Sink Current ---------- 20mA
Power Dissipation, P_D @ T_A = 25°C---------- 2.7W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 46° C/W
θ_{JC} ---------- 18° C/W
Junction Temperature Range ---------- -40°C to +150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN ---------- 2.5V to 6.5V
BFET ---------- 0V to IN+6V
EN ---------- 0V to 16V
SST, ILMT ---------- 0V to 3V
OUT Continuous output current ---------- 0A to 5A
FLG Continuous Output Sink Current ---------- 0mA to 10mA
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(–40 ≤ T_J ≤ 125°C, V_{IN} = 12 V, V_{EN} = 2 V, R_{ILMT} =1.1kΩ, C_{SST} = OPEN, R_{FLG} =10kΩ. Typical values are at 25°C. All voltages are with respect to GND, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		16	V
IN Rising UVLO Threshold Voltage	V_{UVLO}				2.45	V
Hysteresis				100		mV
Shutdown Current	I_{SHDN}	EN=0V		2		μA
Bias Current	I_Q	EN=2V		62		μA
On Resistance	$R_{DS(ON)}$	T_J = 25°C	24	30	36	mΩ
		T_J = 125°C		45	52	mΩ
OUT Overload Current Limit	I_{OC}	R_{ILMT} = 5.5 kΩ	0.80	1.00	1.20	A
		R_{ILMT} = 3.65 kΩ	1.30	1.50	1.70	A
		R_{ILMT} = 2.75 kΩ	1.80	2.00	2.20	A
		R_{ILMT} = 1.85 kΩ	2.70	2.97	3.30	A
		R_{ILMT} = 1.1 kΩ	4.50	5.00	5.50	A
Over Current Protection Response Time	t_{OC}	RILMT=5.5kΩ, I_{LOAD}=1.2A		2		ms
Soft-start Time Range	t_{SST}	Note 4	0.5		90	ms
Soft-start Time Accuracy			-30%		30%	t_{SST}
Turn-On Delay	$t_{d(ON)}$	EN → H to I_{VIN} = 100 mA, 1A resistive load at OUT		200		μs
Turn-Off Delay	$t_{d(OFF)}$	EN → L to 0.9×OUT		100		μs
Output Discharge Resistor	R_{DIS}	V_{IN}=5V, EN=0, V_{OUT}=0.1V		170		Ω
BFET Charging Current	I_{BFET}	V_{BFET} = V_{OUT}		2		μA
BFET Clamp Voltage	$V_{BFETmax}$	V_{BFET}-V_{IN}		6		V
BFET Discharging Resistance to GND	$R_{BFETdis}$	V_{EN} = 0 V, I_{BFET} = 100 mA	15	30	60	Ω
BFET Turn-On Duration	$t_{BFET-ON}$	EN→H to V_{BFET} = 12V, C_{BFET} = 1nF		6		ms
		EN→H to V_{BFET} = 12V, C_{BFET} = 10nF		60		ms
BFET Turn-Off Duration	$t_{BFET-OFF}$	EN→L to V_{BFET} = 1V, C_{BFET} = 1nF		7.5		μs
		EN→L to V_{BFET} = 1V, C_{BFET} = 10nF		8.5		μs
EN Pin Logic-High Voltage	V_{ENH}		1			V
EN Pin Logic-Low Voltage	V_{ENL}				0.4	V
FLG Output Low Voltage	V_{FLGL}	I_{FLG}=1mA			200	mV
Thermal shutdown threshold	T_{SD}			150		°C
Thermal shutdown Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note4: Recommended Current Soft-start Time Program Table

SST Capacitor (nF)	None	10	47	100
SR (V/ms)	6.67	1.74	0.37	0.17

Recommended Formula for C_{SST} & Soft-start Slew Rate Calculation

$$SR_{OUT} = \frac{17\mu}{C_{SST}(nF)}(V/ms)$$

$$t_{SST} = 0.8 \times \frac{V_{IN}}{SR_{OUT}}(ms)$$

For a 12V application, a 100nF SST cap can make the OUT rise time equal to 56ms

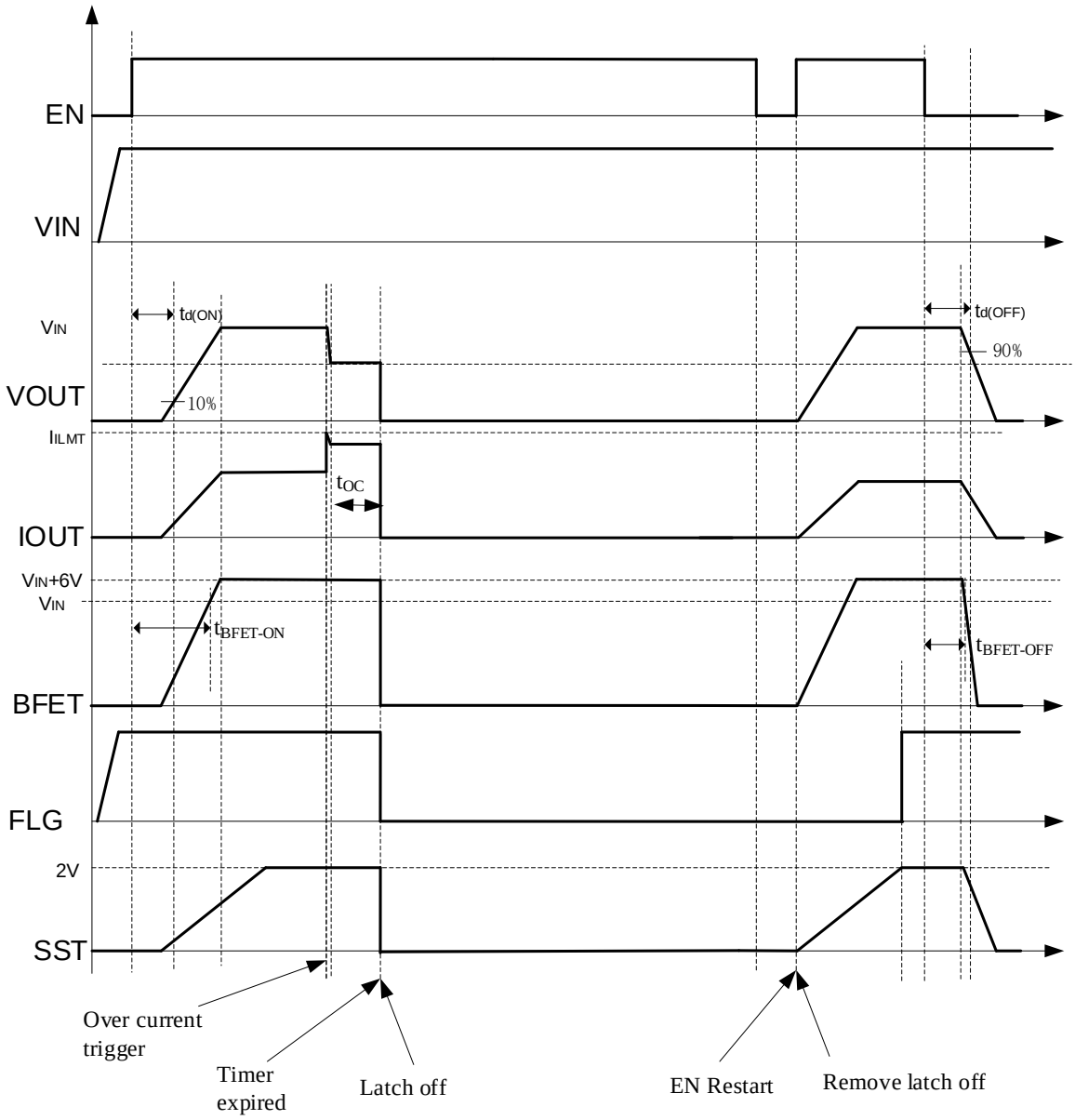
Note5: Recommended Current Limit Program Table

Current Limit Resistance (kΩ)	5.5	2.75	2.2	1.85	1.55	1.4	1.2	1.1
Current Limit (A)	1.0	2.0	2.5	3.0	3.5	4.0	4.5	5.0

Recommended Formula for R_{ILMT} & Current Limit Calculation:

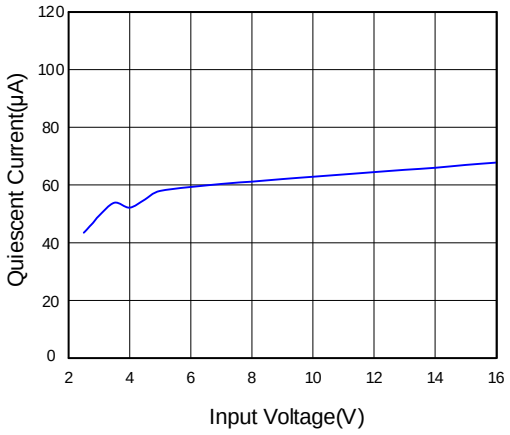
$$R_{ILMT} = \frac{5.5k}{I_{ILMT}}(\Omega)$$

Timing Diagram

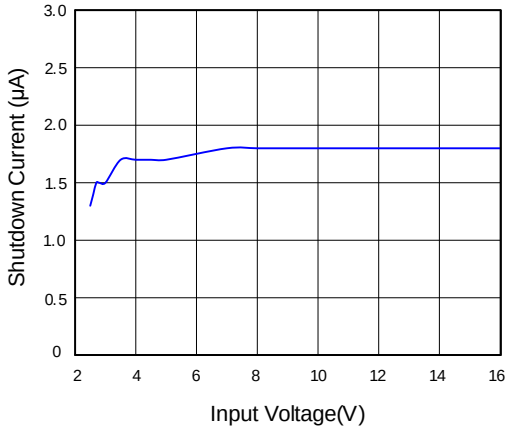


Typical Performance Characteristics

Quiescent Current vs. Input Voltage

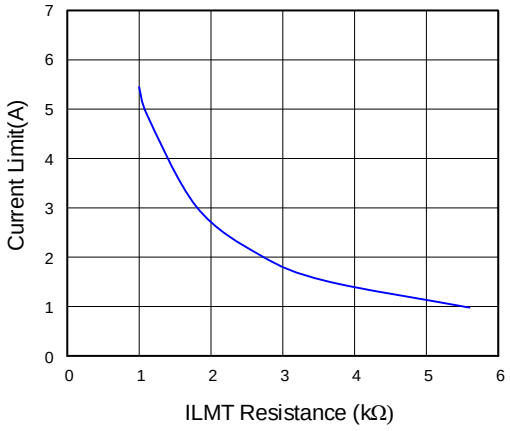


Shutdown Current vs. Input Voltage



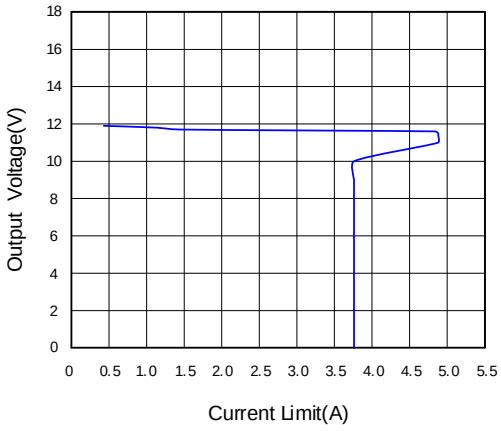
Current Limit vs. ILMT Resistance

(V_{IN}=12V)



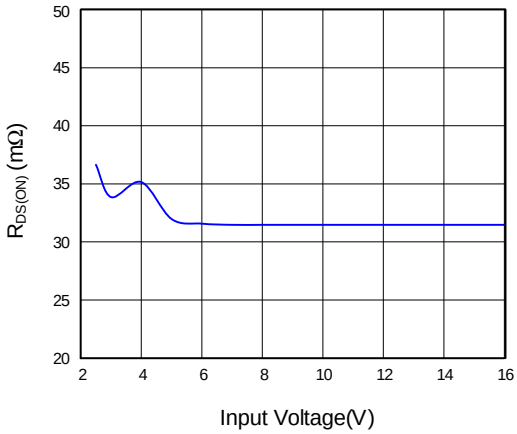
Output Voltage Vs. Current Limit

(V_{IN}=5V, R_{ILMT}=1.1kΩ)



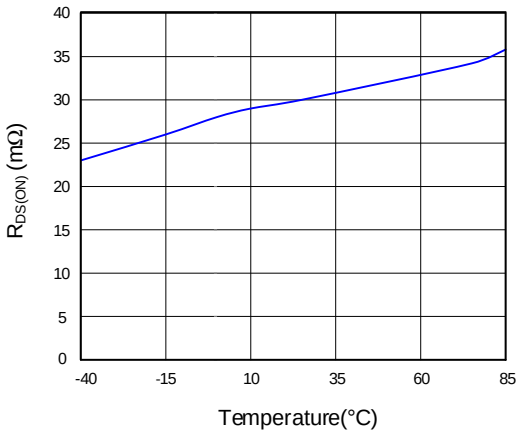
$R_{DS(ON)}$ vs. Input Voltage

(I_{OUT}=1A)



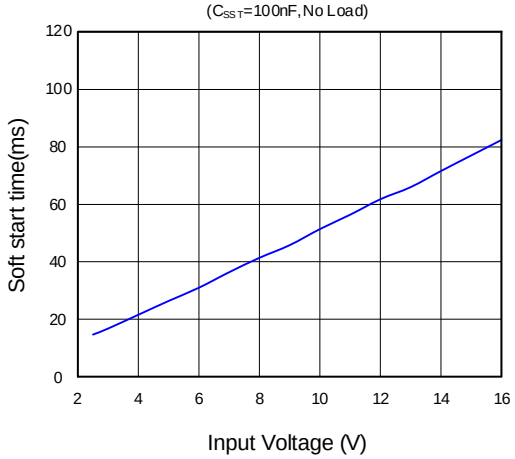
$R_{DS(ON)}$ vs. Temperature

(V_{IN}=12V, I_{OUT}=1A)



Soft Start Time vs. Input Voltage

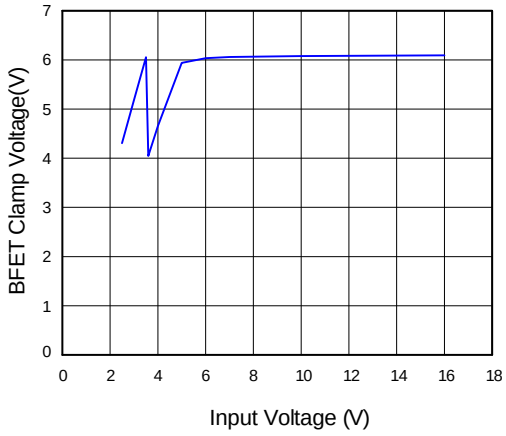
(C_{SST}=100nF, No Load)



Soft Start Time vs. SST Capacitance

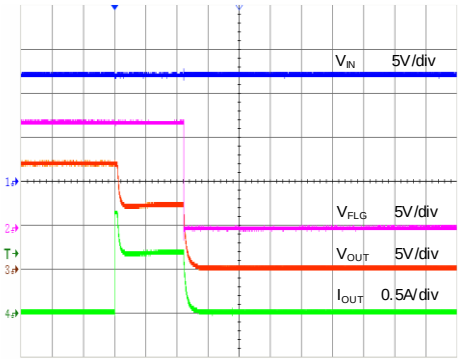
(V_{IN}=12V, No Load)

BFET Clamp Voltage (V_{BFET}-V_{IN}) vs. Input Voltage



OCP Response

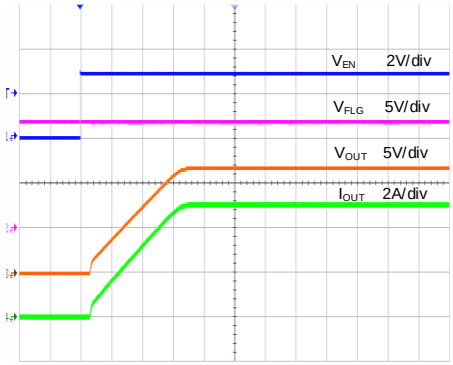
(V_{IN}=12V, EN=3V, R_{ILMT}=5.5kΩ (1A Current Limit), C_{SST} = OPEN, R_{FLG}=100kΩ ,I_{OUT} from 0A to 1.1A)



Time (1ms/div)

Turn ON with Enable

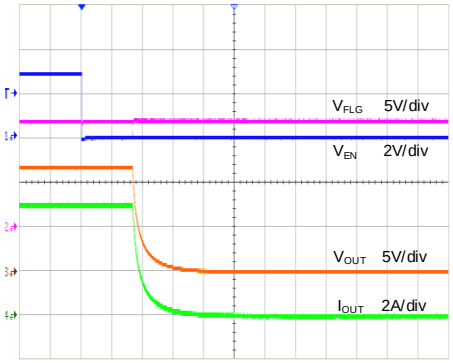
(V_{IN}=12V, EN=0V to 3V, R_{ILMT}=510Ω, C_{SST}=OPEN, R_{FLG}=100kΩ, 5A Load)



Time (500µs/div)

Turn OFF with Enable

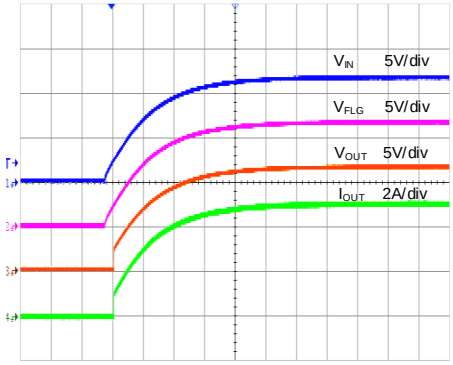
(V_{IN}=12V, EN=3V to 0V, R_{ILMT}=510Ω, C_{SST}=OPEN, R_{FLG}=100kΩ, 5A Load)



Time (50µs/div)

Turn ON with VIN

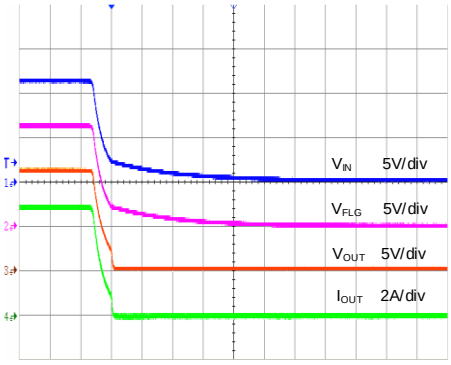
(V_{IN}=0V to 12V, EN=3V, R_{ILMT}=510Ω, C_{SST}=OPEN, R_{FLG}=100kΩ, 5A Load)



Time (20ms/div)

Turn OFF with VIN

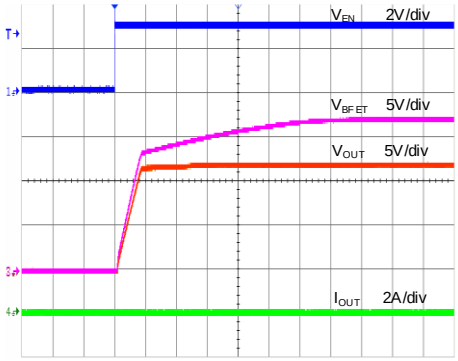
(V_{IN}=12V to 0V, EN=3V, R_{ILMT}=510Ω, C_{SST}=OPEN, R_{FLG}=100kΩ, 5A Load)



Time (1ms/div)

BFET Turn On

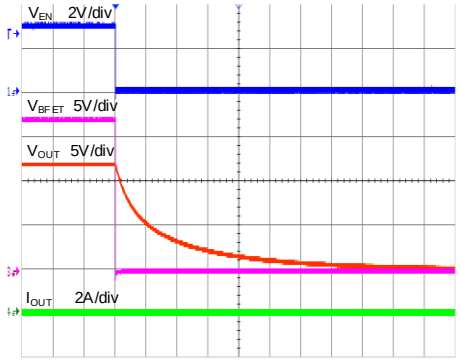
(V_{IN}=12V, EN=0V to 3V, C_{SST} = open, R_{ILMT}=0Ω, Add BFET MOS, 100kΩ Load)



Time (2ms/div)

BFET Turn Off

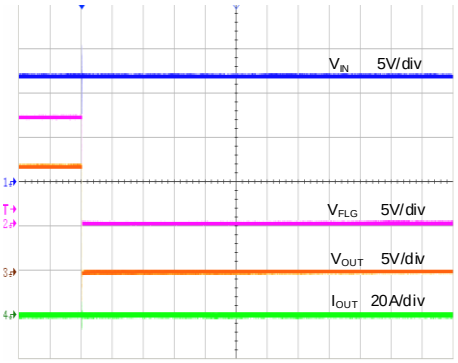
(V_{IN}=12V, EN=3V to 0V, C_{SST} = open, R_{ILMT}=0Ω, Add BFET MOS, 100kΩ Load)



Time (50ms/div)

Short Circuit Response

(V_{IN}=12V, EN=3V, C_{IN}=470μF+10μF, C_{OUT} = 10μF, R_{ILMT} =1.1kΩ (5A Current Limit), C_{SST} = OPEN, R_{FLG}=100kΩ)



Time (1ms/div)

Operation

Soft Start Time Programming

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum t_{SST}) on the output. Equation calculate soft start time is shown below:

SST Cap (nF)	None	10	47	100
SR (V/ms)	6.67	1.74	0.37	0.17
t_{SST} /VIN=12V(ms)	1.4	5.5	26	56

Recommended formula for C_{SST} & Soft-start slew rate calculation:

$$SR_{OUT} = \frac{17\mu}{C_{SST}(nF)}(V/ms)$$

$$t_{SST} = 0.8 \times \frac{V_{IN}}{SR_{OUT}}(ms)$$

BFET Control

The SY86802L integrated a BFET pin for disconnecting input supply from rest of system in the event of power failure at VIN. The BFET pin is controlled by either input UVLO event or EN (see Table 1). When EN/UVLO is held low, the internal MOSFET is turned off and BFET pin is discharged, then blocking current flow from V_{OUT} to V_{IN}. BFET can source charging current of 2 μA (Typ.) and sink (discharge) current from the gate of the external FET via a 26Ω internal discharge resistor to initiate fast turn-off. BFET clamp voltage is 6V(Typ.), choose a low gate voltage N-FET with excellent $R_{DS(ON)}$ is strongly recommend. if an application doesn't need external blocking function, left BFET pin floating.

Table 1. BFET

EN > V_{EN}H	V_{IN}>V_{UVLO}	BFET MODE
H	H	Charge
X	L	Discharge
L	X	Discharge

Over Current Protection

The device continuously monitors the load current and keeps it limited to the value programmed by R_{ILMT}. After start-up event and during normal operation, current limit is set to I_{OC} (over current limit). The recommended 1% resistor for R_{ILMT} is 1.1k to 5.5k to ensure stability of internal regulation loop. Recommended Formula for R_{ILMT} & Current Limit Calculation:

$$I_{OC} = \frac{5.5k}{R_{ILMT}}(A)$$

When an over-current condition (I_{OC}<I_{LOAD}<1.6×I_{OC}) occurs, the device maintains a constant output current and reduces the output voltage accordingly for 2 milliseconds before the device latch off.

When a short condition (I_{LOAD}>1.6×I_{OC}) is detected, the power path will be latched off immediately.

Thermal Shutdown

Internal over temperature shutdown disables turns off the FET when T_J > 150°C (typical). The device is latched off.

FLG Response

The FLG open-drain output is asserted (active low) during an over-temperature or current limit or short condition. It is normally pulled high by an external pull-up resistor. The output remains asserted until the fault condition is removed. SY86802L is designed to eliminate false FLG reporting by using an internal deglitch circuit for current limit conditions without the need for external circuitry. This ensures that FLG is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Over-temperature is not deglitched and assert the FLG signal immediately.

Supply Filter Capacitor

A 1μF or larger input ceramic capacitor is strongly recommended to be placed close to the IC. Furthermore, an output short will cause ringing on the input without the input capacitor. It could destroy the internal circuitry when the input transient exceeds the absolute maximum supply voltage even for a short duration.

Output Filter Capacitor

A 1μF output ceramic capacitor is recommended to be placed close to the IC and output connector to reduce voltage drop during load transient. Higher values of output capacitor can be used to further reduce the drop during high current application. during short circuit scenario, output could be pulled to very negative voltage by parasitic wire inductor. it is stronger recommended parallel connected a Schottky diode to absorb to large negative voltage spike to keep output voltage is with the range of absolute voltage rating.

PCB Layout Guide

For best performance of the SY86802L, the following guidelines must be strictly followed:

1. Keep all VBUS traces as short and wide as possible and use at least 2-ounce copper for all VBUS traces.

2. Locate the output capacitor as close to the connectors as possible to lower impedance (mainly inductance) between the port and the capacitor and improve transient performance.

3. Input and output capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling.

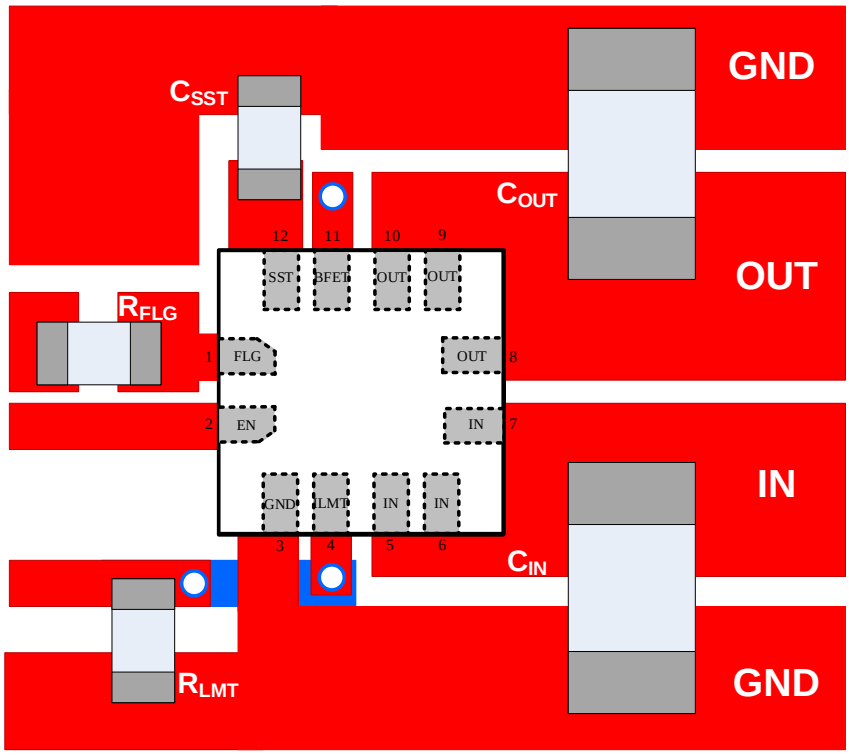
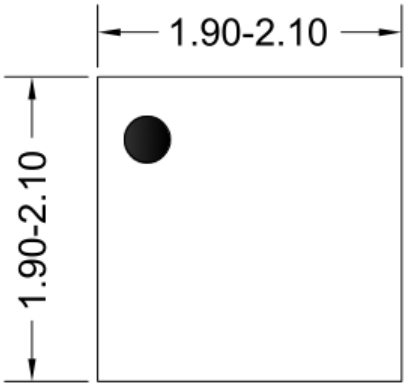
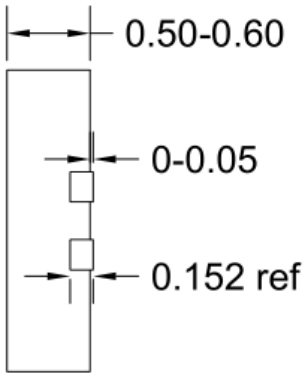


Figure3. PCB Layout Suggestion

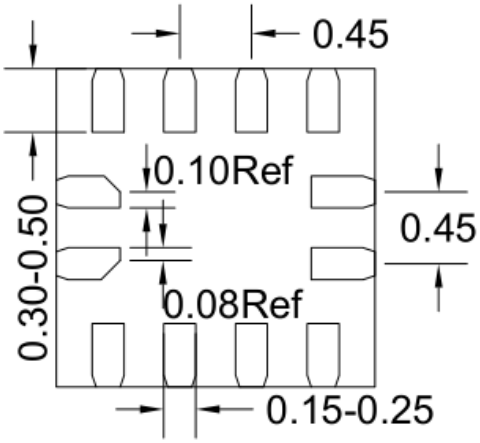
QFN2×2-12 Package Outline Drawing



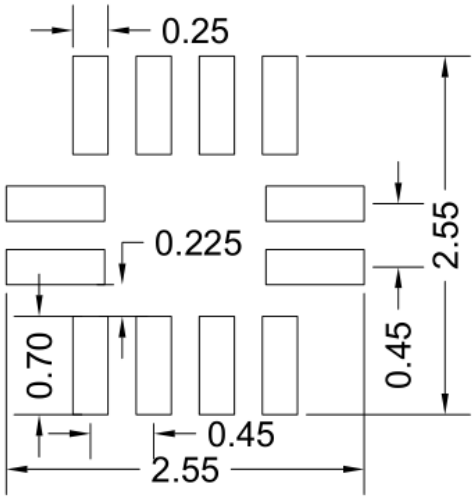
Top view



Side view



Bottom view



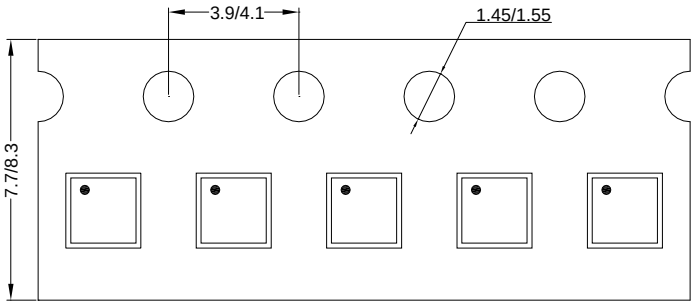
Recommended PCB layout

Notes: 1. All dimension in millimeter and exclude mold flash & metal burr.
2. Recommended PCB layout only for reference.

Taping & Reel Specification

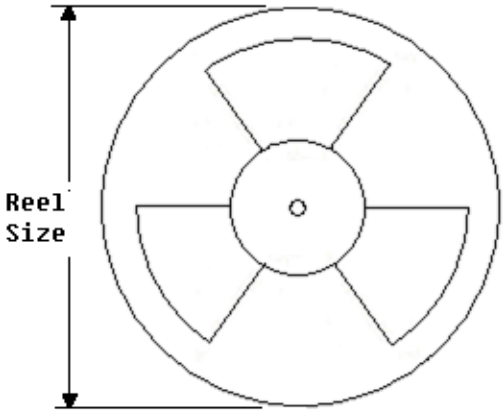
1. Taping orientation

QFN2×2



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2×2	8	4	7"	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
July 22, 2023	Revision 1.0	Initial Production Release
July 22, 2022	Revision 0.9	Initial Release

IMPORTANT NOTICE

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