

General Description

The SY28480B is a 0.76mΩ ultra-low on-resistance with integrated N-Channel MOSFET efuse for use in high current applications such as base stations and servers. It integrates overcurrent protection, soft-start capabilities to reduce inrush current and high accurate current monitor.

The SY28480B is available in a compact QFN5mm×5mm- 32 package.

Applications

- Servers
- Base Station
- Hot Swap Applications

Features

- Wide Input Range: 4.5 V to 18 V
- Up to 60 A Peak Current Output, 50 A Continuous
- Integrated N-Channel MOSFET with 0.76 mΩ Ultra Low R_{ON}
- Optional Output Discharge Function when Disabled
- Adjustable Slew Rate Control
- Adjustable Current Limit
- Accurate Analog Load Current Monitor
- Adjustable Over Current Alert Output
- Temperature Indicator
- Fault Detection with status OK Output
- Built-in Insertion Delay
- Can be used in Parallel for Higher Current Applications
- Latch off for Following Protection Features
 - ◆ Soft Start Duration Timeout
 - ◆ Thermal Shutdown
 - ◆ Fast Short-Circuit Protection
 - ◆ Current Limiting Response Timeout
- Compact Package Minimizes the Board Space: QFN 5 mm× 5 mm-32

Typical application

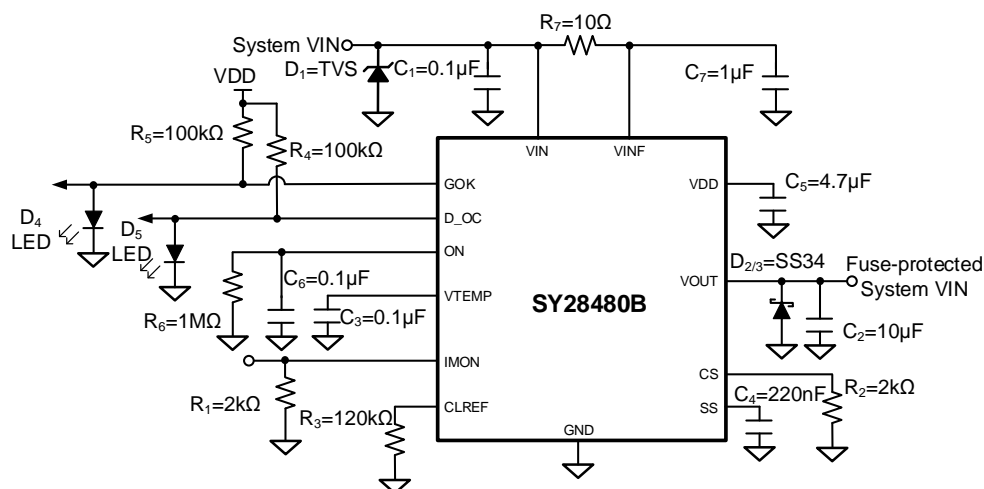


Figure1. Schematic Diagram

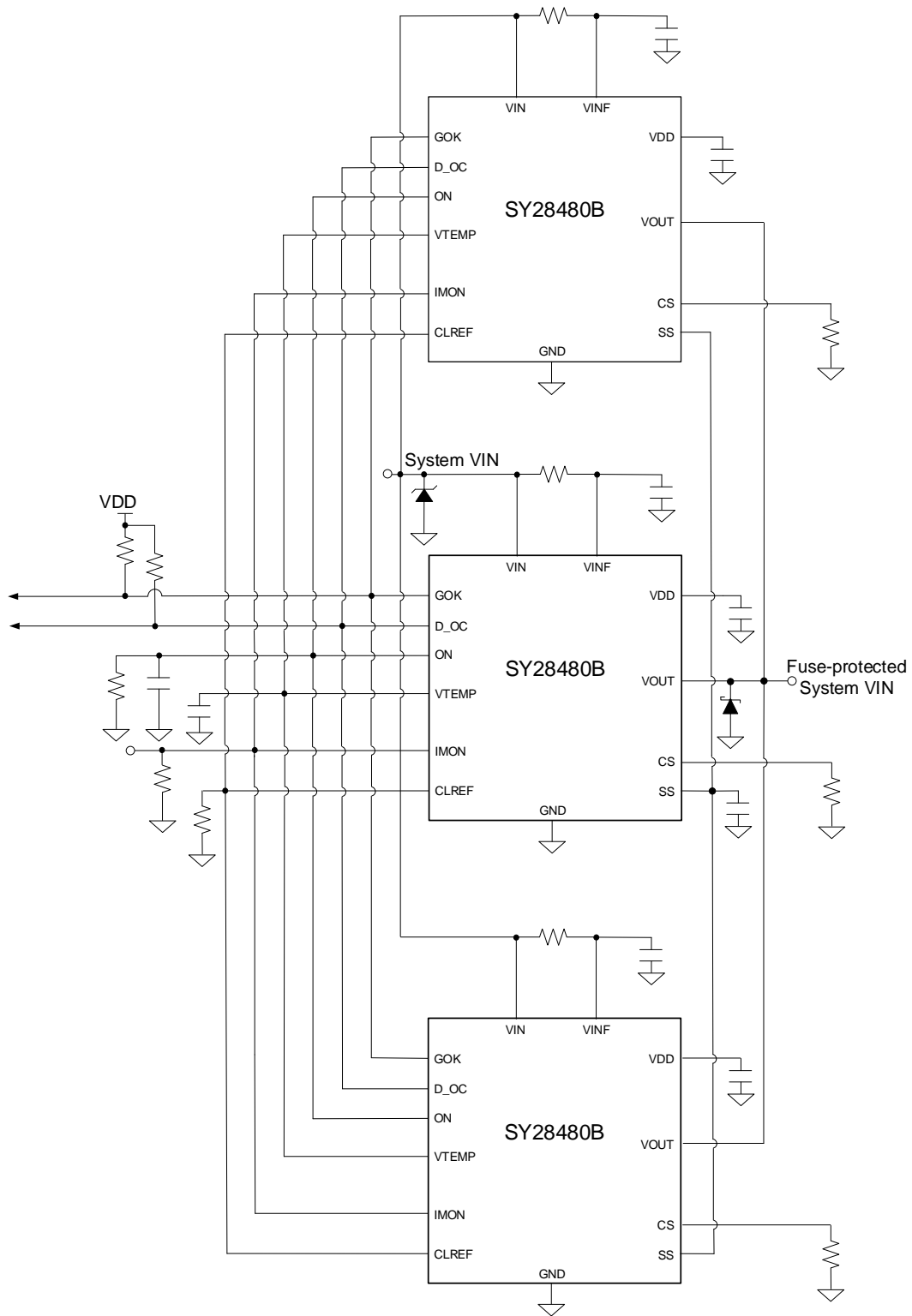


Figure2. Parallel Fuse Operation Schematic

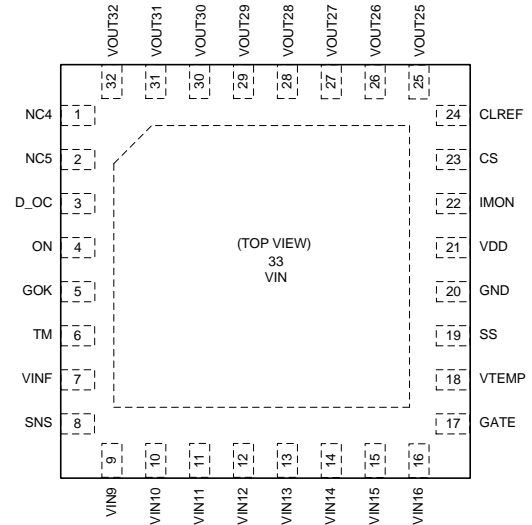
Ordering Information

Pinout (top view)

Ordering Part Number	Package Type	Top Mark
SY28480BQEQ	QFN5x5-32 RoHS Compliant and Halogen Free	GAWxyz

Device code: GAW

x=year code, y=week code, z= lot number code



Pin Description

Pin Name	Pin Number	Pin Description
NC4	1	No electrical connection internally. May connect to any potential.
NC5	2	No electrical connection internally. May connect to any potential.
D_OC	3	Over current indicator output (open drain). Low indicates the device is limiting current. The D_OC output does not report current limiting during soft-start.
ON	4	Enable output pull down resistance control.
GOK	5	OK status indicator output (open drain). Low indicates that the device was turned off by a fault.
TM	6	Test pin. Do not connect to this pin. Leave floating.
VINF	7	Control circuit power supply input. Connect to VIN pins through an RC filter.
SNS	8	Internal FET sense pin. Do not connect to this pin. Leave floating.
VIN09	9	Input of high current output switch.
VIN10	10	Input of high current output switch.
VIN11	11	Input of high current output switch.
VIN12	12	Input of high current output switch.
VIN13	13	Input of high current output switch.
VIN14	14	Input of high current output switch.
VIN15	15	Input of high current output switch.
VIN16	16	Input of high current output switch.
GATE	17	Internal FET gate pin. It should be connected to the cathode of an anode grounded diode. To alleviate the risk of oscillation when output capacitance is small or a long input/output cable (large parasitic inductance), it is recommended to place a 4.7nF ceramic capacitor between this pin and GND.
VTEMP	18	Analog temperature monitor output.
SS	19	Soft Start time programming pin. Connect a capacitor to this pin to set the soft start time.
GND	20	Ground.
VDD	21	Linear regulator output.



SY28480B

Pin Name	Pin Number	Pin Description
IMON	22	Analog current monitor output.
CS	23	Current sense feedback output (current). Scaling the voltage developed at this pin with a resistor to ground makes this also an input for several current limiting functions and over current indicator D_OC.
CLREF	24	Current limit setpoint input for normal operation (after soft-start).
VOUT25	25	Output of high current output switch.
VOUT26	26	Output of high current output switch.
VOUT27	27	Output of high current output switch.
VOUT28	28	Output of high current output switch.
VOUT29	29	Output of high current output switch.
VOUT30	30	Output of high current output switch.
VOUT31	31	Output of high current output switch.
VOUT32	32	Output of high current output switch.
VIN33	33	Input of high current output switch.

Block Diagram

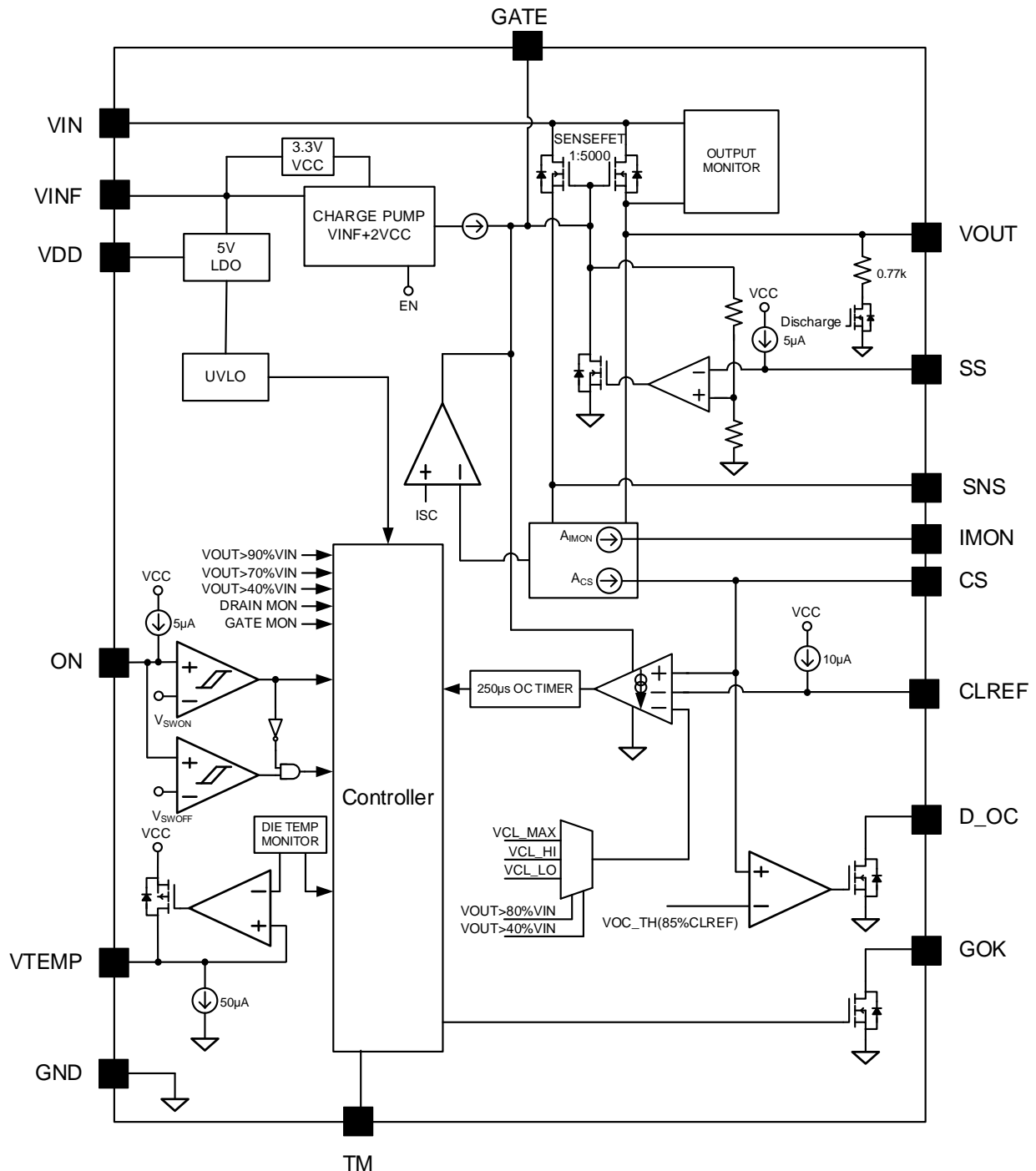


Figure3. Block Diagram



Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
VINx, VINF	-0.3	20	V
VOUTx	-0.3V/-1V(<500ms)	20	
VDD	-0.3	6	
GOK, D_OC, ON, VTEMP, CLREF, IMON, CS, SS	-0.3	VDD+0.3	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	28	°C/W
θ_{JC} Junction-to-case Thermal Resistance	21.3	
P_D Power Dissipation $T_A = 25^\circ\text{C}$	3.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN, VINF	4.5	18	V
VDD, GOK, D_OC, ON, VTEMP, CLREF, IMON, CS, SS	0	5.5	
Maximum Continuous Output Current: I_{AVE}		50	A
Peak Output Current: I_{PEAK}		60	
VDD Output Load Capacitance Range: C_{VDD}	2.2	10	μF
VTEMP Output Load Capacitance Range: C_{VTEMP}	0.1		μF
Soft-start Duration: t_{SS}	10	100	ms
CS Load Resistance Range: R_{CS}	1.8	4	4k Ω
CLREF Voltage Range: V_{CLREF}	0.2	1.4	V
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(VINx=VINf=12V, VON=3.3V, CVINF=0.1μF, CVDD=4.7μF, CVTEMP=0.1μF, RVTEMP = 1kΩ, C_{SS}=100nF, T_J=-40°C to 125°C, typical values are T_J=25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VINF INPUT						
Quiescent Current	I _Q	V _{ON} >1.4V, null load		1.44	3.0	mA
		V _{ON} >1.4V, fault			3.0	mA
		V _{ON} <0.8V		1.44	3.0	mA
		V _{ON} <0.8V, VINF=16V			3.0	mA
VDD REGULATOR						
VDD Output Voltage	V _{DD_NL}	I _{VDD} = 0 mA, VINF = 6 V	4.6	4.95	5.2	V
VDD Load Capability	I _{DDLOAD}	VINF = 5.5 V			30	mA
VDD Current Limit	I _{DD_CL}	VINF = 12 V and VINF = 6 V	50	88		mA
VDD Dropout Voltage		I _{VDD} = 25 mA, VINF = 4.5 V		85	200	mV
UVLO Threshold - rising	V _{DD_UVR}		4.1	4.3	4.5	V
UVLO Threshold - falling	V _{DD_UVF}		3.8	4.0	4.2	V
ON INPUT						
Bias Current	I _{ON}	From pin into a 0 V or 1.5 V source	4.0	5.0	6.0	μA
Switch ON Threshold	V _{SWON}		1.3	1.4	1.5	V
Switch OFF/ Pulldown Upper Threshold	V _{SWOFF}			1.2		V
Pulldown Lower Threshold	V _{PDOFF}			0.8		V
Switch ON Delay Timer	t _{ON}	From ON transitioning above V _{SWON} to SS start	0.6	1.0	2.5	ms
Switch OFF Delay Time (Note 4)	t _{OFF}	From ON transitioning below V _{SWOFF} to GATE pulldown		1		μs
ON Current Source Clamp Voltage	V _{ON_CLMP}	Max pullup voltage of current source		3.0		V
Load Pulldown Delay Timer	t _{PD_DEL}	From ON transitioning into the range between V _{SWOFF} and V _{PDOFF}		2.0		ms
Output Pulldown Resistance	R _{PD}	V _{OUT} = 12 V, PD mode = 1		0.77		kΩ
SS PIN						
Bias Current	I _{SS}	From pin into a 0V or 1V source	4.62	5.15	5.62	μA
Gain to VOUT	AV _{SS}	T _J =25°C	9.6	10	10.4	V/V
SS Pulldown Voltage	V _{OL_SS}	0.1 mA into pin during ON delay		3		mV
GOK OUTPUT						
Output Low Voltage	V _{OL_GOK}	I _{GOK} = 1 mA			0.1	V
Off-state Leakage Current	I _{LK_GOK}	V _{GOK} = 5 V			1.0	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
IMON/CS OUTPUT							
IMON or CS Current (single eFuse) Based on 10 μ A/A+1.5 μ A	I_{IMON}/I_{CS}	$T_J = 0$ to 85°C	$I_{OUT} = 5$ A (Note 4)		51.5		μ A
			$I_{OUT} = 10$ A (Note 4)		101.5		μ A
			$I_{OUT} = 25$ A (Note 4)		251.5		μ A
			$I_{OUT} = 50$ A (Note 4)		501.5		μ A
Accuracy (single eFuse)		$T_J = 0$ to 85°C	$I_{OUT} = 5$ A (Note 4)	-6		+6	%
			$I_{OUT} = 10$ A (Note 4)	-4		+4	%
			$I_{OUT} = 25$ A (Note 4)	-4		+4	%
			$I_{OUT} = 50$ A (Note 4)	-4		+4	%
Pre-Biased Offset Current Load for Auto-Zero Op-Amp	I_{AZ_BIAS}			1.5		μ A	
CURRENT LIMIT & CLREF PIN							
Current Limit Voltage	V_{CL_TH}	If $V_{CS} > V_{CL_TH}$ current limiting regulation occurs via gate	95	98	101	% V_{CLREF}	
Current Limit Clamp Voltage	V_{CL_LO}	$V_{OUT} < 40\%V_{IN}$, $V_{CLREF} > 0.15$ V	135	152	165	mV	
	V_{CL_HI}	$40\%V_{IN} < V_{OUT} < 80\%V_{IN}$ $V_{CLREF} > 0.5$ V	480	504	520	mV	
Max Current Limit Reference Voltage	V_{CL_MX}	$V_{OUT} > 80\%V_{IN}$, $V_{CLREF} > 1.6$ V	1.55	1.6	1.65	V	
Response Time (Note 4)	t_{CL_REG}	$V_{CS} > V_{CLREF}$ until current limiting		100		μ s	
CLREF Bias Current	I_{CL}	From pin into a 1.2 V source	9.6	10	10.4	μ A	
CLREF Current Source Clamp Voltage	V_{CL_CLMP}	Max pullup voltage of current source		3.0		V	
FET Turn-off Timer	t_{CL_LA}	Delay between current limit detection and FET turn-off (GOK = 0)		250		μ s	
D_OC OUTPUT							
Overcurrent Threshold	V_{OC_TH}	If $V_{CS} > V_{OC_TH}$ D_OC pin pulls low	83	86	90	% V_{CLREF}	
Output Low Voltage	V_{OL_DOC}	$I_{DOC} = 1$ mA			0.1	V	
Off-state Leakage Current	I_{LK_DOC}	$V_{DOC} = 5$ V			1.0	μ A	
Delay (rising) (Note 4)		$V_{CS} < \text{limit}$ until D_OC rising		1.0		μ s	
Delay (falling) (Note 4)		$V_{CS} > \text{limit}$ until D_OC falling		1.0		μ s	
SHORT CIRCUIT PROTECTION							
Current Threshold (Note 4)	I_{SC}			100		A	
Response Time (Note 4)	t_{SC}	From $I_{OUT} > I_{LIMSC}$ until gate pulldown		500		ns	
VTEMP OUTPUT							
Bias Voltage	$V_{VTEMP25}$	At 25°C		550		mV	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Gain (Note 4)	A_{VTEMP}	$0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		10		mV/°C
Load Capability	R_{VTEM}	At 25°C		1		kΩ
Pulldown Current	I_{VTEMP}	At 25°C		50		μA
Thermal Shutdown						
Temperature Shutdown (Note 4)	T_{TSD}	GOK pulls down		140		°C
OUTPUT SWITCH(FET)						
On Resistance	$R_{DS(ON)}$	$T_J = 25^{\circ}\text{C}$		0.76	1.0	mΩ
Off-state Leakage Current	I_{DSOFF}	$V_{IN} = 16\text{ V}, V_{ON} < 1.2\text{ V}, T_J = 25^{\circ}\text{C}$			1.0	μA
FAULT DETECTION						
V_{DS} Short Threshold	V_{DS_TH}	Startup postponed if $V_{OUT} > V_{DS_TH}$ at $V_{ON} > V_{SWON}$ transition		90		%VIN
V_{DS} Short OK Threshold	V_{DS_OK}	Startup resumed if $V_{OUT} < V_{DS_OK}$ any time after postponed		70		%VIN
V_{GD} Short Threshold	V_{DG_TH}	Startup postponed if $V_G > V_{DG_TH}$ at $V_{ON} > V_{SWON}$ transition		3.1		V
V_{GD} Short OK Threshold	V_{DG_OK}	Startup resumed if $V_G < V_{DG_OK}$ anytime after postponed		3.0		V
V_G Low Threshold (Note 4)	V_{G_TH}	Latch if $V_{GD} < V_{G_TH}$ after t_{SSF_END} or t_{GATE_FLT}		3.4		V
V_{OUT} Low Threshold (Note 4)	V_{OUTL_TH}	Latch if $V_{OUT} < V_{OUTL_TH}$ after t_{SSF_END}		90		%VIN
Gate Fault Timer (Note 4)	t_{GATE_FLT}	Time from $V_{GD} < V_{G_TH}$ transition after t_{SSF_END} completed		200		ms
Startup Timer Failsafe (Note 4)	t_{SSF_END}	Time from $V_{ON} > V_{SWON}$ transition, Max programmable soft-start time		200		ms

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

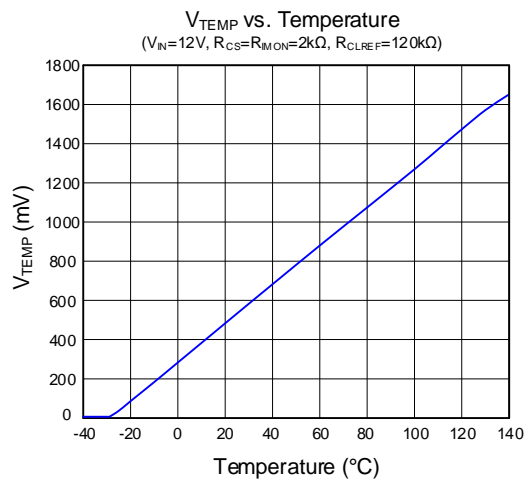
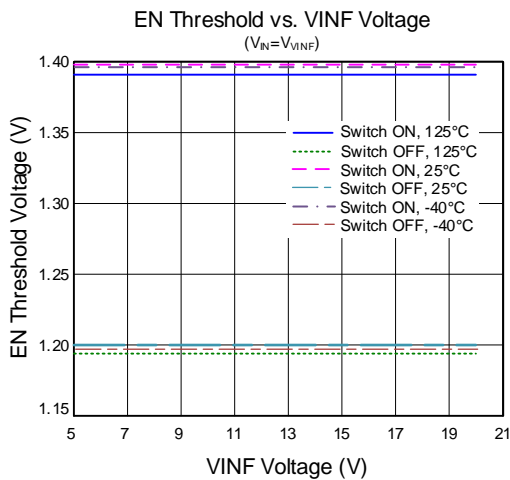
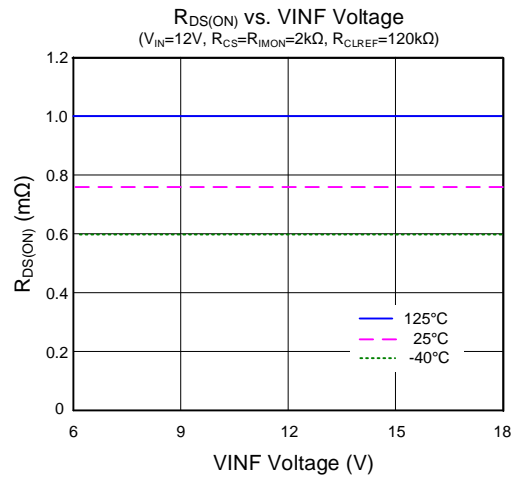
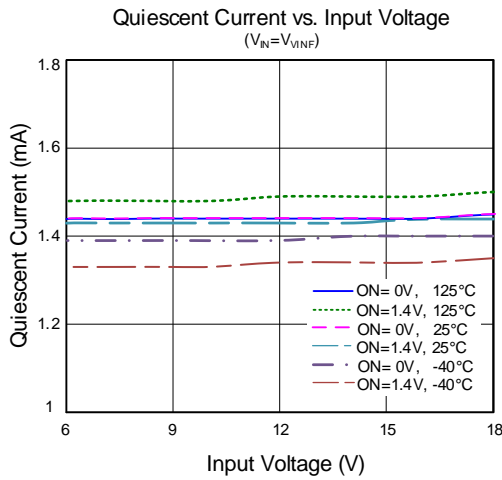
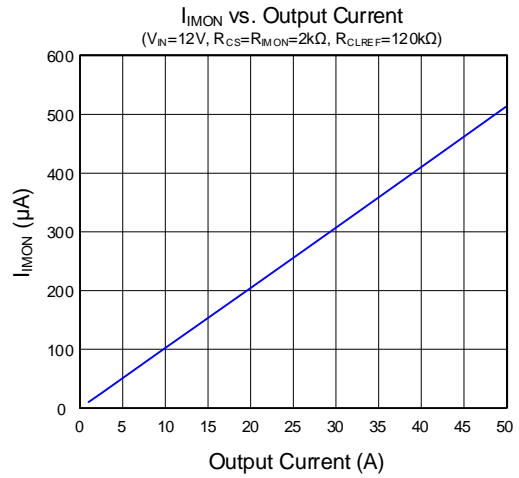
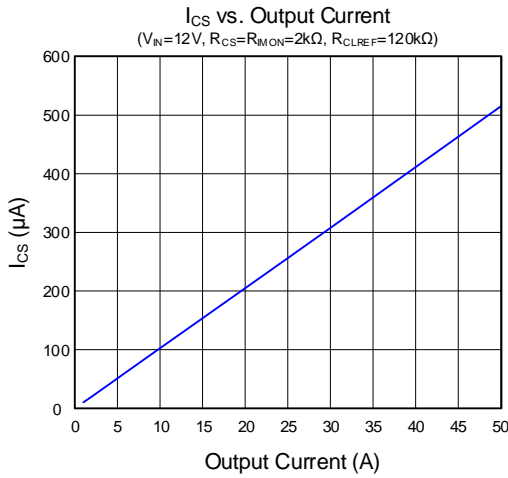
Note 2: θ_{JA} is simulated in the natural convection at $T_A = 25^{\circ}\text{C}$ on Silergy EVB test board.

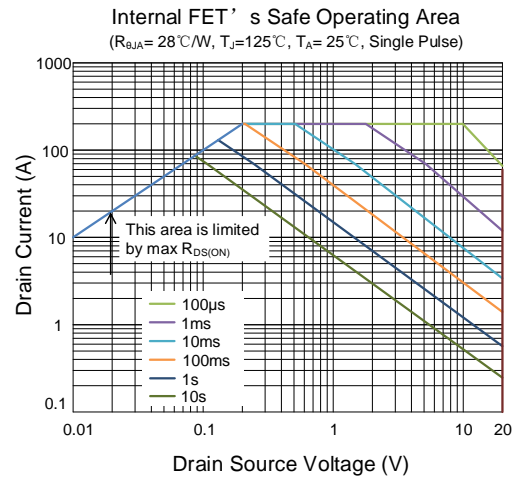
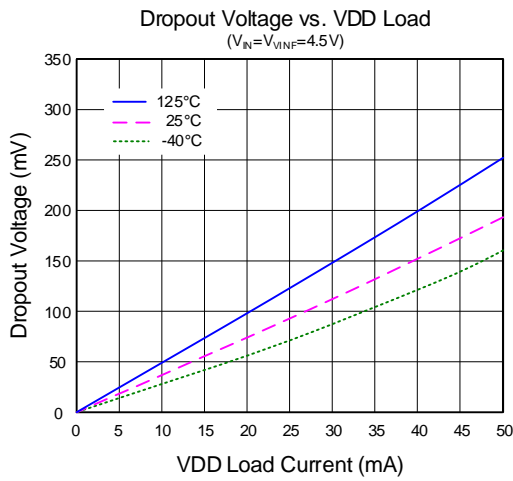
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design but not production tested.

Note 5: I_{CL_LOTH} indicates the threshold that triggers the timing of current limit when $V_{OUT} < 40\%V_{IN}$ and $V_{CLREF} > 0.15\text{V}$, but not the actual current limit clamp threshold. If $I_{OUT} > I_{CL_LOTH}$ for a continuous duration $> t_{CL_LA}$, then the device latches.

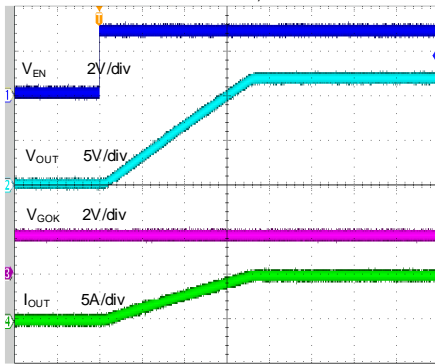
Typical Performance Characteristics





Startup from EN

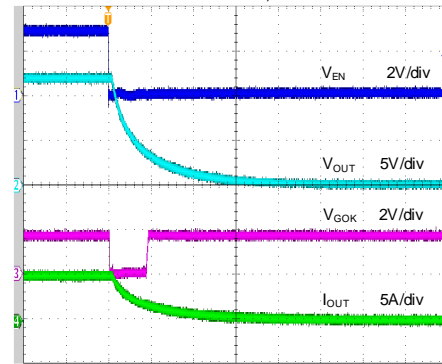
($V_{IN}=V_{VIN}=12V$, $R_{CS}=R_{MON}=2k\Omega$, $R_{CLREF}=120k\Omega$, $C_{SS}=220nF$, 2.4Ω Load)



Time (20ms/div)

Shutdown from EN

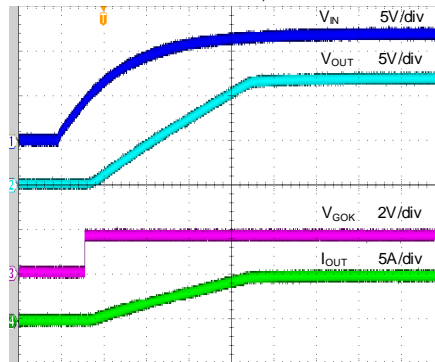
($V_{IN}=V_{VIN}=12V$, $R_{CS}=R_{MON}=2k\Omega$, $R_{CLREF}=120k\Omega$, $C_{SS}=220nF$, 2.4Ω Load)



Time (20µs/div)

Startup from V_IN

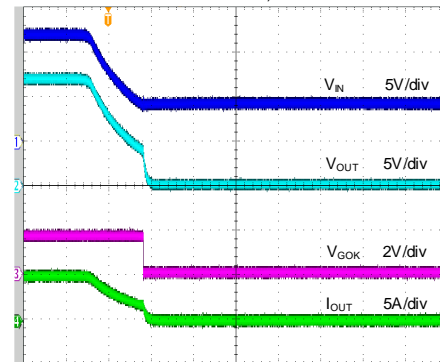
($V_{IN}=V_{VIN}=12V$, $R_{CS}=R_{MON}=2k\Omega$, $R_{CLREF}=120k\Omega$, $C_{SS}=220nF$, 2.4Ω Load)



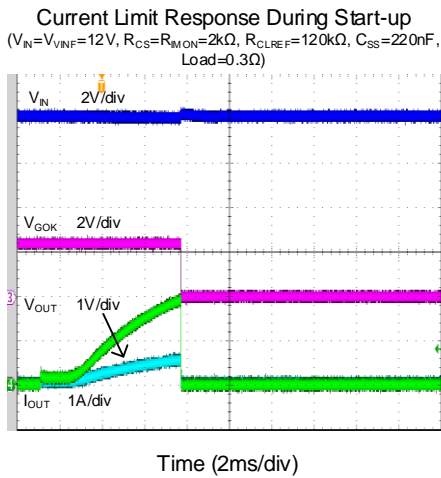
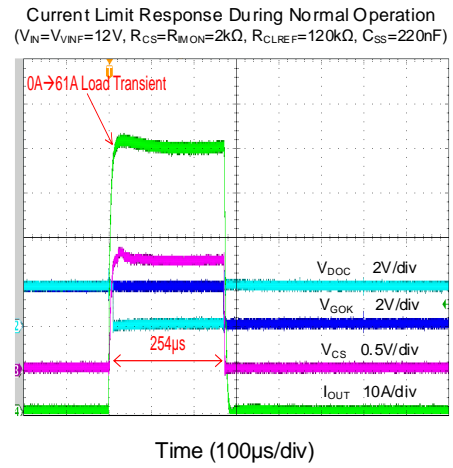
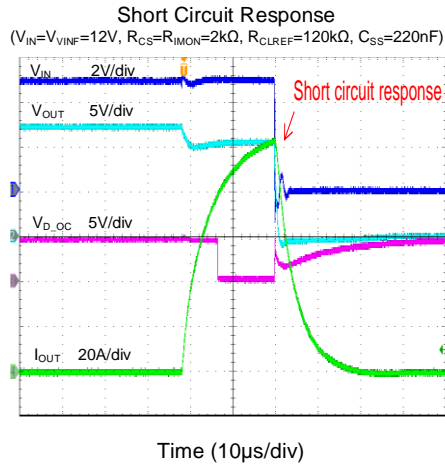
Time (20ms/div)

Shutdown from V_IN

($V_{IN}=V_{VIN}=12V$, $R_{CS}=R_{MON}=2k\Omega$, $R_{CLREF}=120k\Omega$, $C_{SS}=220nF$, 2.4Ω Load)



Time (400µs/div)



Operation

The SY28480B is a current limited N-channel MOSFET co-packaged with a smart hot swap controller designed for servers or hot swap applications. It incorporates the over temperature protection, over current protection, and short circuit protection. It can be used either alone, or in a parallel configuration for higher current applications.

VDD Output

The SY28480B provides a 5V output VDD source with current limit up to I_{DD_CL} . Shall connect this pin a 2.2 μ F to 10 μ F to GND. And place as close as possible to the SY28480B.

ON/OFF Control

Without under voltage and any other faults occurring, the output switch will turn on when V_{ON} is above V_{SWON} . When V_{ON} is below V_{SWOFF} , the switch will turn off.

If V_{ON} remains between V_{PDOFF} and V_{SWOFF} for more than t_{PD_DEL} , the switch will turn off, and V_{OUT} will have a 0.77k Ω pull-down resistance to ground.

The ON pin sources a 5 μ A pull up current, connect a capacitor from ON pin to GND can program the startup delay time after V_{IN} is higher than UVLO.

Programmable Soft Start Time

The SY28480B can program output start up time by connecting a capacitor from the SS pin to GND. Soft start capacitor can be calculated by:

$$C_{SS} = (t_{SS} \times I_{SS} \times A_{V_{SS}}) / V_{IN}$$

(Where t_{SS} is the target soft-start time).

The recommended range of t_{SS} is 10-100ms. The Soft Start Time vs. C_{SS} curve is shown in Figure4:

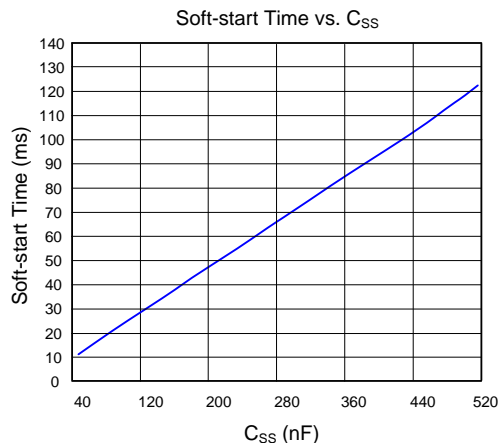


Figure4. Soft Start Time vs. C_{SS}

For parallel application, the SS pins shall be connected together to share one soft start cap so that no slew rate is consistent of each other. The same soft start time make the charging current of each device is same so that the inrush current is balanced.

GOK Output (Gate OK)

The GOK pin is an open-drain output that is pulled low to report the fault under the following conditions:

VDD	VON	Condition	GOK
<UVLO	X	X	Low
>UVLO	Low	VDS OK fail	Low
>UVLO	Low	VGD OK fail	Low
>UVLO	High	$V_{OUT} < 90\% \times V_{IN}$, after soft start done	Low
>UVLO	High	VGS OK fail after t_{SS_END}	Low
>UVLO	High	VGS OK fail after t_{GATE_FLT}	Low
>UVLO	High	Current limit lasts longer than t_{OC_LA}	Low
>UVLO	High	Junction temperature over	Low

IMON Output (Current Monitor)

The IMON pin sources a current A_{IMON} , which is proportional (10 μ A/A) to load current. Connect a resistor from this pin to GND to get voltage signal that can be connect to ADC to monitor the load current.

Connect a capacitor from this pin to GND can act as a low pass filter for ADC converter.

CLREF Pin (Current Limit and Over-Current Reference)

The voltage on the CLREF pin act as a reference of current limit regulation point. This pin internal will source a 10 μ A current. Connect a resistor from this pin to GND, can program the current limit threshold. The V_{CLREF} value can be calculated by: $V_{CLREF} = I_{CL} \times R_{CLREF}$

The voltage is also can be given by an external voltage source or a DAC. The recommended voltage range for CLREF is between 0.2V to 1.4V.

CS Input/Output (Current Set)

The CS pin sources a current A_{CS} that is proportional ($A_{CS} = 10\mu$ A/A) to load current. Connect a resistor from this pin to GND to get voltage which act as a feedback signal of current limit regulation loop.

During normal operation ($V_{ON} > V_{SWON}$ for longer than t_{SS_END}). When the voltage on the CS pin (V_{CS}) is higher than V_{CL_TH} (V_{CL_TH} is equals to V_{CLREF} , and will be

clamped at V_{CL_MX} , if $V_{CL_TH} > V_{CL_MX}$, the internal current limit loop will regulate the output current based on formula: $I_{OUT} = V_{CL_TH} / (R_{CS} \times A_{CS})$

At each stage of startup, the current limit reference voltage is clamped based on the following:

- When $V_{OUT} < 40\%$ of V_{IN} , $V_{CL_TH} = V_{CL_LO}$ or V_{CLREF} (whichever is lower).
- When V_{OUT} is between 40% and 80% of V_{IN} , $V_{CL_TH} = V_{CL_HI}$ or V_{CLREF} (whichever is lower).
- When V_{OUT} exceeds 80% of V_{IN} , $V_{CL_TH} = V_{CL_MX}$ or V_{CLREF} (whichever is lower).

If the current limit duration exceeds t_{CL_LA} , the device will latch off.

The CS pin must not have any capacitive loading other than parasitic device capacitance in order to operate properly. The recommended range of R_{CS} is between 1.8kΩ and 4kΩ.

VINF Pin

VINF is the power supply input for internal control circuit. Connecting an RC filter, 10Ω resistor and 1μF ceramic capacitor, to this pin as close as possible

CS AMP OFFSET BIAS

The SY28480B pre-biased an offset to keep internal high accurate auto-zero amplifier operates at null load or light load condition.

The internal IMON and CS current source follow below relationship: $I_{OUT} = (I_{CS} - I_{AZ_BIAS})/10\mu$ and $I_{OUT} = (I_{MON} - I_{AZ_BIAS})/10\mu$.

For typical 1.5μA I_{AZ_BIAS} , there has 0.15A positive offset in I_{OUT} sense.

DOC Output (Over-current Indicator)

The D_OC pin is an open-drain output that indicates when an over current condition exists after soft start is complete. When the voltage on the CS pin, V_{CS} is higher than V_{OC_TH} , D_OC is pulled low. If V_{CS} is lower than V_{OC_TH} , D_OC is high impedance and can be pulled high by external pull up resistor.

VTEMP Output (Temperature Indicator)

VTEMP is a voltage output proportional 10mV/°C to device junction temperature, with an offset voltage. If multiple VTEMP outputs are connected, the voltage of all VTEMP outputs will be driven to the voltage produced by the hottest SY28480B. A 0.1μF capacitor or greater must be connected from the VTEMP pin to ground. The V_{VTEMP} value can be calculated by:

$$V_{VTEMP} = V_{VTEMP25} + (T_{TEMP} - 25^{\circ}C) \times A_{VTEMP}$$

(where T_{TEMP} is the current temperature)

Protection Features

For the following protection features, the FET latches off, unless noted otherwise.

Protection Features	Description	FET Status
Over-Current Limiting	Current limiting condition exists anytime for a continuous duration $> t_{CL_LA}$	Latch off
Over-Soft Start Duration	$V_{OUT} < V_{OUTL_TH}$ when t_{SSF_END} expires	Latch off
Short Circuit Protection	Switch current exceeds I_{SC} , the device reacts within t_{SC}	Latch off
Over-Temperature Shutdown	The FET controller temperature $> T_{TSD}$, then the FET latches.	Latch off
VIN to VOUT Short	The device is disabled and $V_{OUT} > V_{DS_TH}$ then GOK is pulled low and the device is prevented from powering up. The device is allowed to power up once $V_{OUT} < V_{DS_OK}$.	Non-Latch off
GATE to VIN Short	The device is disabled and $GATE > V_{DG_TH}$, then GOK is pulled low and device is prevented from powering up. The device allowed to power up once $GATE < V_{DG_OK}$.	Non-Latch off
GATE Leakage-Startup	$(GATE - VINF) < V_{G_TH}$ at t_{SSF_END} , then GOK is pulled low	Latch off
Gate Leakage-Normal Operation	$(GATE - VINF) < V_{G_TH}$ for t_{GATE_FLT} time after the soft start timer completes, then GOK is pulled low	Latch off

FET SOA Limits

Power FET's SOA should not be exceeded. In-built timed current limits and fault-monitoring circuit make the power FET work within SOA limits in normal operation status.

Multiple Fuse Power Up

When multiple SY28480B are paralleled together, the SY28480Bs will turn on together. Keeping the current through each switch within 1 A (typical) helps to prevent overstress on each switching during soft start.

When paralleled multiple SY28480B encounter fault, the system can recover the E-fuse by resetting their VDD with below buffer and reset circuit.

Input Filter Capacitor

A 0.1 μ F or larger input ceramic capacitor is strongly recommended to be placed close to the VIN. A VOUT short will cause ringing on the VIN without the VIN capacitor. It could cause the N-MOSFET electrical over stress when the VIN transient exceeds the absolute maximum voltage rating even for a short duration. However, if there have a hot plug scenario, in order to reduce the inrush current during hot plug, it is necessary to consider reducing the input capacitance comprehensively.

Output Filter Capacitor

A 10 μ F ceramic capacitor is recommended to be placed close to the VOUT to reduce voltage drop during load transient. Higher values of ceramic capacitor can be used for further reducing the drop during high current application.

Transient Voltage Suppressor

The SY28480B specifies an absolute maximum voltage of 20V and is designed to tolerate brief over voltage events due to hot plug surges. To protect the SY28480B from an over voltage event, install a unidirectional transient voltage suppressor (TVS) such as an SMAJ20CA between the VIN and GND pins.

OUT Schottky Diode

An anti-parallel schottky diode is suggested to be placed near the VOUT pin to absorb the negative ringing. A low forward voltage and large forward current schottky diode is recommend.

PCB Layout Guide

For best performance of the SY28480B, the following guidelines must be strictly followed:

1. Keep all power traces as short and wide as possible and use at least 2-ounce copper for all power traces.
2. Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance.
3. Locate the output capacitor as close to the connectors as possible to lower impedance (mainly inductance) between the port and the capacitor and improve transient performance.
4. Input and output filter capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling.
5. Locate the RC filter as close to VINF as possible to stabilize the bias supply.

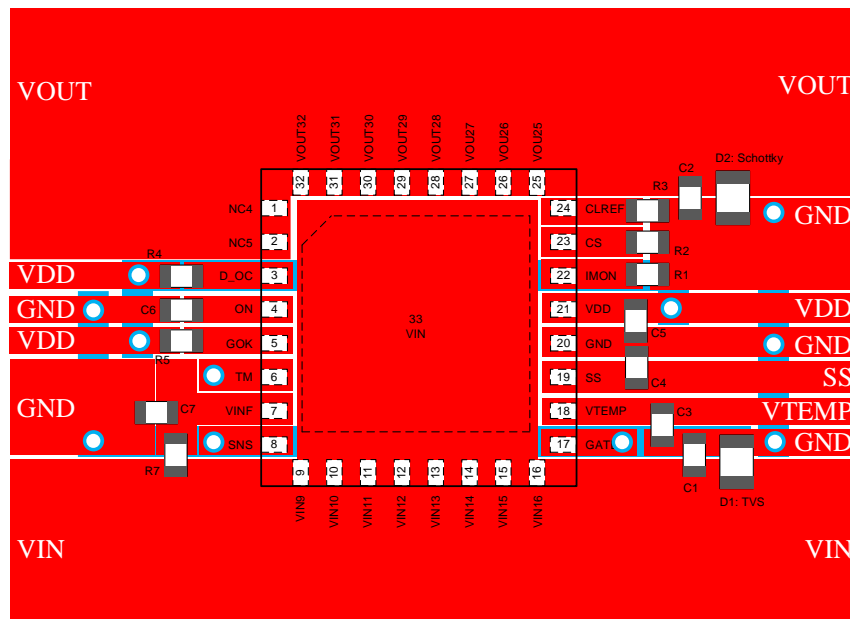
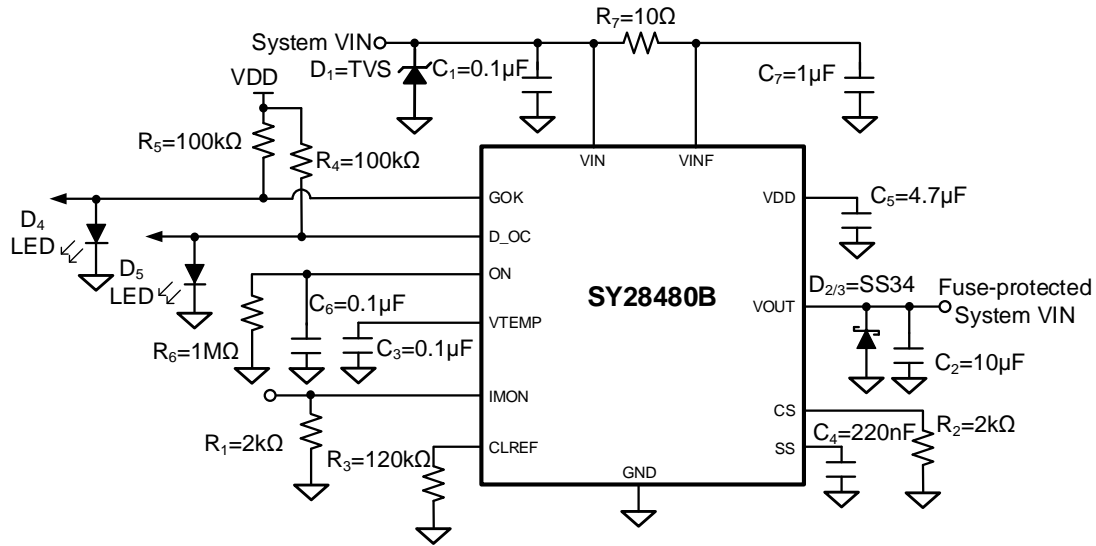


Figure5. PCB Layout Suggestion



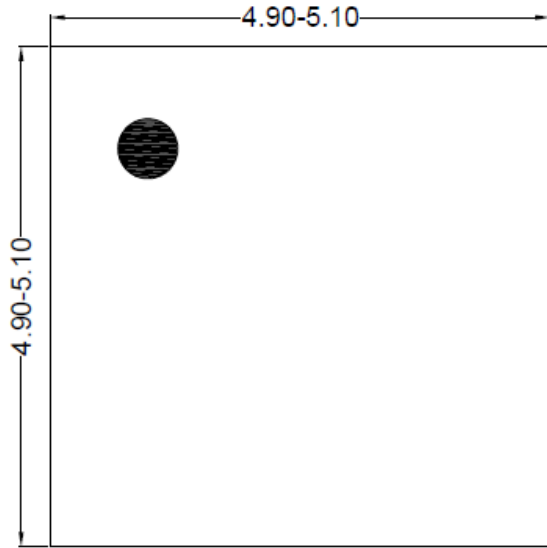
Schematic



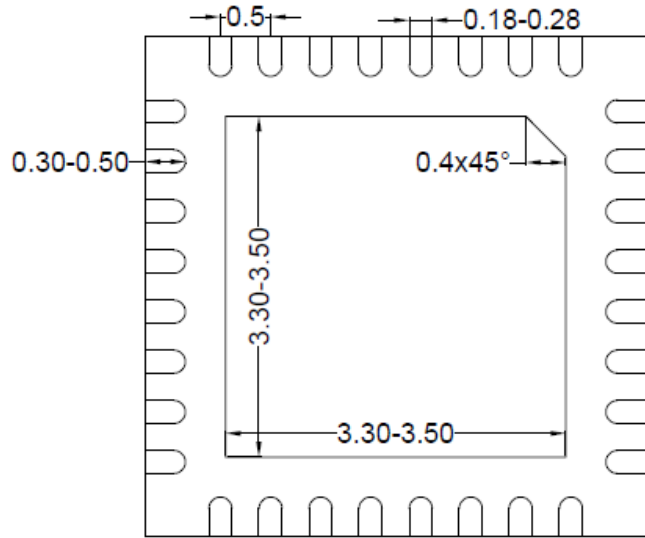
BOM List

Reference Designator	Description	Part Number	Manufacturer
C1	0.1μF/50V, 0603	GCJ188R71H104KA12	Murata
C2	10μF/50V, 1206	GRT31CR61H106KE01L	Murata
C3	0.1μF/50V, 0603	GCJ188R71H104KA12	Murata
C4	220nF/50V, 0603	CGA3E3X7R1H224K080AE	Murata
C5	4.7μF/16V, 0603	GRM185R61C475KE11D	Murata
C6	0.1μF/50V, 0603	GCJ188R71H104KA12	Murata
C7	1μF/50V, 0603	GRM188R61C105MA12D	Murata
R1	2kΩ, 0603	RC0603FR-072KL	YAGEO
R2	2kΩ, 0603	RC0603FR-072KL	YAGEO
R3	120kΩ, 0603	RC0603FR-07120KL	YAGEO
R4	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R5	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R6	1MΩ, 0603	RC0603FR-071ML	YAGEO
R7	10Ω, 0603	RC0603FR-0710RL	YAGEO
D1	TVS/20V	SMAJ20CA	PHY
D2/3	Schottky/40V	SS34	TOSHIBA
D4/5	LED	/	/

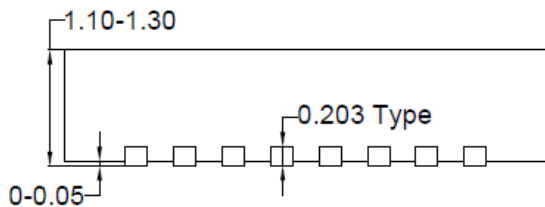
QFN5.0×5.0-32 Package Outline Drawing



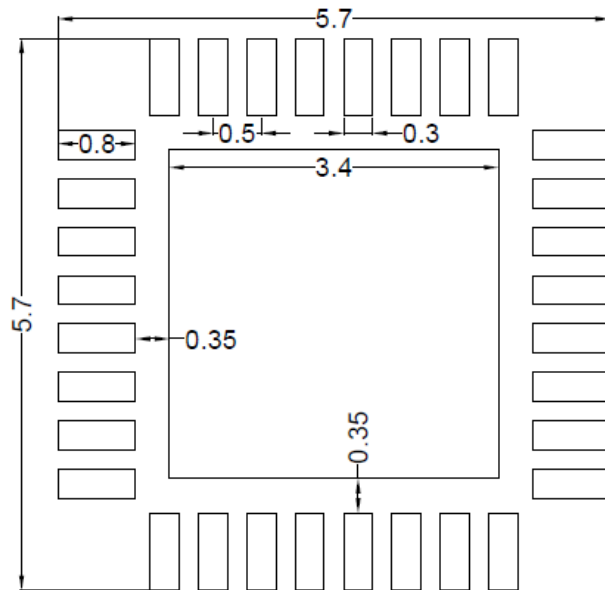
Top view



Bottom view



Side view

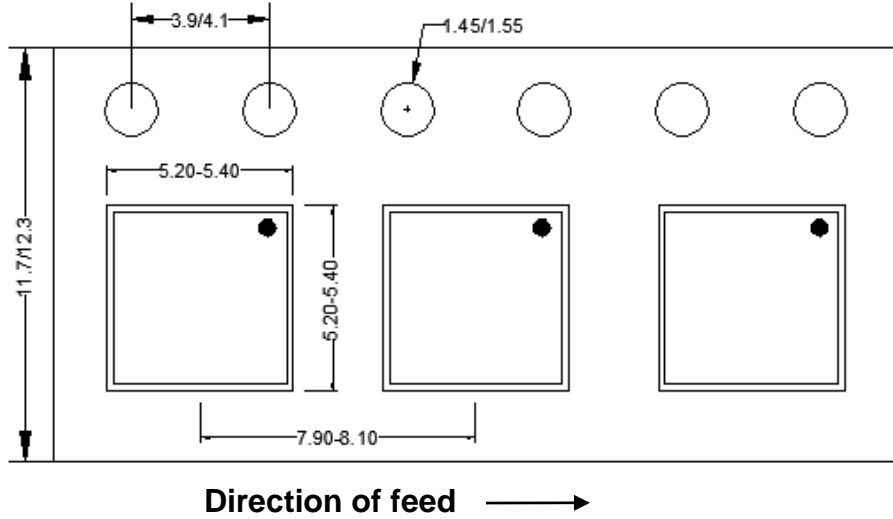


**Recommended PCB layout
(Reference only)**

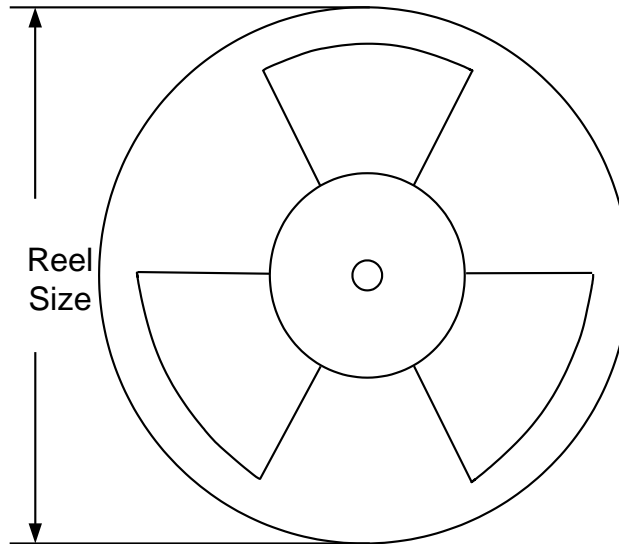
Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;

Tape and Reel Information

1. Tape dimensions and pin1 orientation



2. Reel dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5x5	12	8	13"	400	400	5000



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.24, 2024	Revision 1.0	Initial Release

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