

General Description

The SQ24802K2 is a compact and fully integrated eFuse that provides power management and circuit protection capabilities. The SQ24802K2 requires minimal external components and provides various protection modes. It can effectively protect against overvoltage, overload, short circuit, and excessive inrush current conditions.

The current limit threshold can be easily configured using an external resistor. Additionally, internal output clamping circuit can effectively limit the occurrence of overvoltage events without the need for external components.

Applications with specific voltage ramp requirements can use a single capacitor to regulate dV/dT and ensure the desired output ramp rate.

The SQ24802K2 is available in a compact DFN 2mm×2mm – 8pin package.

Features

- Low Power Path Resistance
 $R_{DS(ON)}=31m\Omega$ (Typical)
- Overvoltage Protection Clamp at 14V
- Adjustable Current Limit (I_{LIMIT}) : 1A to 5A
- Adjustable Output Slew Rate Control (SLEW)
- Overtemperature Protection (OTP)
- Fault Indication Pin (FLT_N)
- Protection Mode: Auto-Restart
- Operating Voltage Range: 4.2V to 16V,
 $V_{ABSMAX} = 18V$
- Compact Package: DFN2×2-8

Applications

- Industrial Systems
- Hot-Swap Applications
- Digital Televisions
- SSDs and HDDs
- Adapter Powered Systems

Typical Application

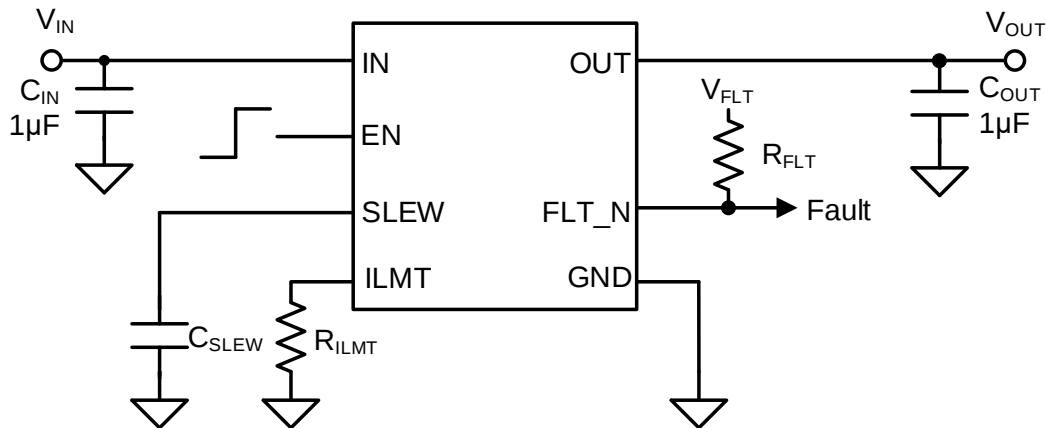


Figure1. Schematic Diagram

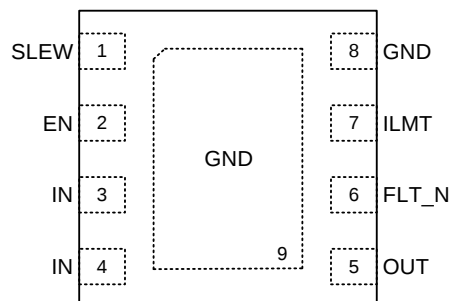
Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ24802K2DFD	DFN2x2-8 RoHS Compliant and Halogen Free	LFWxyz

Device code: LFW

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Description

Pin Name	Pin Number	Pin Description
SLEW	1	Connect a capacitor from this pin to the GND to control the ramp rate of OUT at the device turn-on.
EN	2	Active high enable. A resistor divider can be used to adjust the undervoltage lockout threshold. Do not leave floating.
IN	3, 4	Input and supply voltage, connect at least a 1μF ceramic capacitor from this pin to GND and place the capacitor as close to the device as possible.
OUT	5	Power-switch output. Connect at least a 1μF ceramic capacitor from this pin to GND and place the capacitor as close to the device as possible.
FLT_N	6	The fault event indicator is pulled low when a fault is detected. It is an open drain output that requires an external pull up resistance. Leave it floating if not used.
ILMT	7	A resistor from this pin to GND will set the overcurrent and short-circuit limits.
GND	8, 9	GND.

Block Diagram

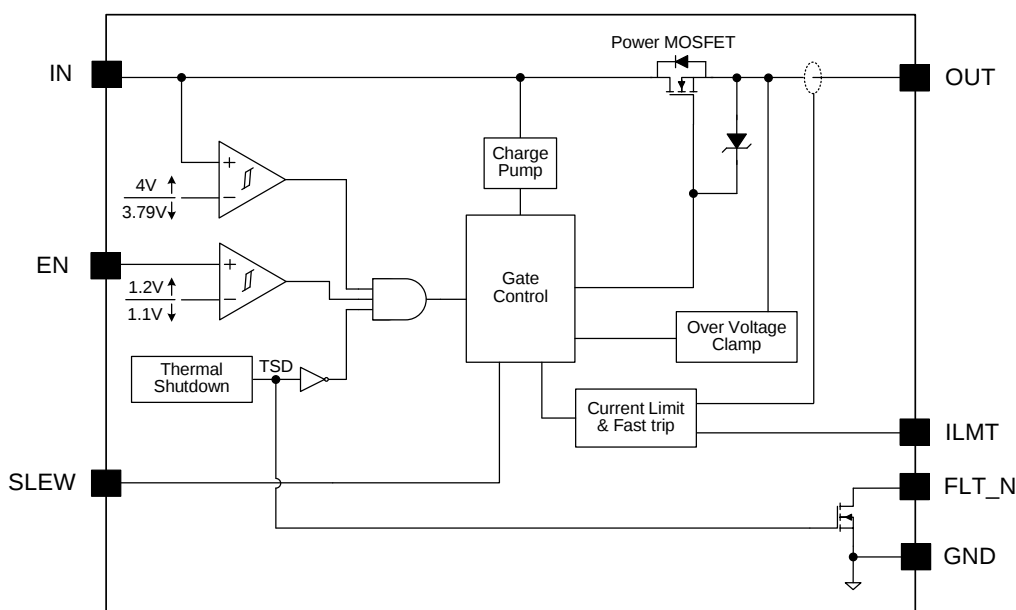


Figure2. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)		Min	Max	Unit
IN, EN		-0.3	18	V
OUT		-0.3	IN+0.3	
FLT_N		-0.3	7	
ILMT, SLEW		-0.3	3.6	
Lead Temperature (Soldering, 10 sec.)			260	°C
Junction Temperature, Operating		-40	150	
Storage Temperature		-65	150	
Electrostatic Discharge	HBM (Human Body Mode)		±2500	V
	CDM (Charged Device Mode)		±500	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	60	°C/W
θ_{JC} Junction-to-case Thermal Resistance	36	
P_D Power Dissipation $T_A = 25^\circ\text{C}$	1.67	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	4.2	16	V
EN, FLT_N	0	6	
SLEW, ILMT	0	3	
OUT Continuous Output Current	0	5	A
Junction Temperature	-40	125	°C

Electrical Characteristics

($V_{IN} = 12\text{ V}$, $V_{EN} = 5\text{ V}$, $R_{ILMT} = 487\Omega$, $C_{SLEW} = \text{OPEN}$. R_{OUT} [between OUT to GND] = open, schematic of figure 1.

$T_J = -40^\circ\text{C}$ to 125°C , typical values are at $T_J = 25^\circ\text{C}$, unless otherwise specified (Note 4))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.2		16	V
IN Undervoltage Protection Threshold	V_{UVLO_R}	V_{IN} rising	3.8	4	4.2	V
	V_{UVLO_F}	V_{IN} falling	3.59	3.79	3.99	V
Shutdown Current	I_{SHDN}	$V_{EN} < 0.5\text{ V}$, $0\text{ V} \leq V_{IN} \leq 18\text{ V}$		5.8	12	μA
Quiescent Current	I_Q	$V_{EN} \geq V_{ENR}$		72	120	μA
Output Voltage While Clamping	V_{CLAMP}	V_{IN} rising, $R_{OUT} = 10\text{ k}\Omega$, -40°C to 85°C	13.3	14	14.7	V
Peak Output Clamp Response Time (Note 5)	t_{CLPF}	$I_{OUT} = 4\text{ A}$		300		μs
		$I_{OUT} = 100\text{ mA}$		300		μs
EN Turn On to 95% $\times V_{OUT}$	t_{ON}	$R_{OUT} = 100\Omega$	210	410	660	μs
		$C_{SLEW} = 3300\text{ pF}$, $R_{OUT} = 100\Omega$	850	1400	2100	μs
EN Threshold Voltage, rising	V_{ENR}		1.13	1.2	1.27	V
EN Threshold Voltage, falling	V_{ENF}		1.03	1.1	1.17	V
EN Input Leakage Current	I_{EN}	$0\text{ V} \leq V_{EN} \leq 5\text{ V}$	-100	0	100	nA
MOSFET On Resistance	R_{ON}	$T_J = 25^\circ\text{C}$	21	31	37	$\text{m}\Omega$
				39	53	$\text{m}\Omega$
Current Monitor Gain As Measured on ILMT Pin (I_{ILMT} / I_{OUT})	G_{IMON}	$I_{OUT} = 4\text{ A}$	213	228	243	$\mu\text{A/A}$
		$I_{OUT} = 1\text{ A}$	206	224	242	
Overload Current Limit	I_{LIMIT}	$R_{ILMT} = 487\Omega$	3.55	4.19	4.6	A
		$R_{ILMT} = 1780\Omega$	0.97	1.175	1.29	A
		$R_{ILMT} = 4420\Omega$	0.39	0.485	0.54	A
Current Limit Response Time (Note 5)	t_{LIM}	$I_{OUT} > I_{LIMIT} + 20\%$ to $I_{OUT} \leq I_{LIMIT}$		300		μs
Short-Circuit Response Time (Note 5)	t_{SC}	$I_{OUT} > I_{SC}$ to MOSFET shutdown		1		μs
FLT_N Pin Resistance (Note 5)	R_{FLT_N}	FLT_N falling		20		Ω
FLT_N Pin Leakage Current	I_{FLT_N}	$V_{EN} = 2\text{ V}$, $V_{FLT_N} = 0\text{ V}$ to 6 V	-0.1		0.1	μA
Thermal Shutdown Threshold (Note 5)	T_{SD}			157		$^\circ\text{C}$
Thermal Shutdown Hysteresis (Note 5)	T_{SDHYS}			15		$^\circ\text{C}$
Thermal Shutdown Auto-Retry Interval (Note 5)	$t_{TSD,RST}$	Device enabled and $T_J < T_{SD} - T_{SDHYS}$		4		ms
Output Rising Slew Rate $R_{OUT} = 100\Omega$	SR_{ON}	$V_{IN} = 5\text{ V}$		48.3		V/ms
		$V_{IN} = 5\text{ V}$, $C_{SLEW} = 3.3\text{ nF}$		11.4		
		$V_{IN} = 12\text{ V}$		39.7		
		$V_{IN} = 12\text{ V}$, $C_{SLEW} = 3.3\text{ nF}$		10.5		
Turn On Delay $R_{OUT} = 100\Omega$	$t_{D,ON}$	$V_{IN} = 5\text{ V}$		154		μs
		$V_{IN} = 5\text{ V}$, $C_{SLEW} = 3.3\text{ nF}$		196		
		$V_{IN} = 12\text{ V}$		158		
		$V_{IN} = 12\text{ V}$, $C_{SLEW} = 3.3\text{ nF}$		245		

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Rise Time $R_{OUT} = 100\Omega$	t_R	$V_{IN} = 5V$		93.3		μs
		$V_{IN} = 5V, C_{SLEW} = 3.3nF$		396		
		$V_{IN}=12V$		242		
		$V_{IN}=12V, C_{SLEW} = 3.3nF$		915		
Turn Off Delay $R_{OUT} = 100\Omega$	$t_{D,OFF}$	$V_{IN} = 5V$		7.1		μs
		$V_{IN} = 5V, C_{SLEW} = 3.3nF$		7.3		
		$V_{IN}=12V$		7		
		$V_{IN}=12V, C_{SLEW} = 3.3nF$		7.1		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured with natural convection at $T_A = 25^\circ C$ on a Silergy test board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Production tested at $25^\circ C$. Limits are guaranteed by design, test or statistical correlation.

Note 5: Guaranteed by design but not production tested.

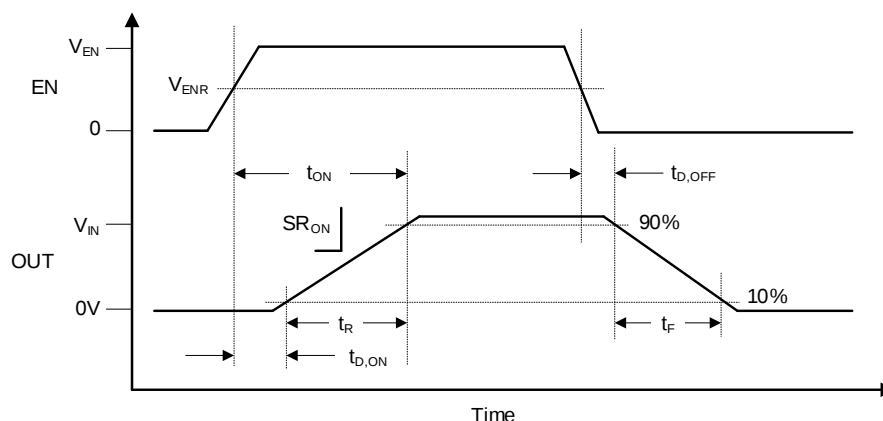
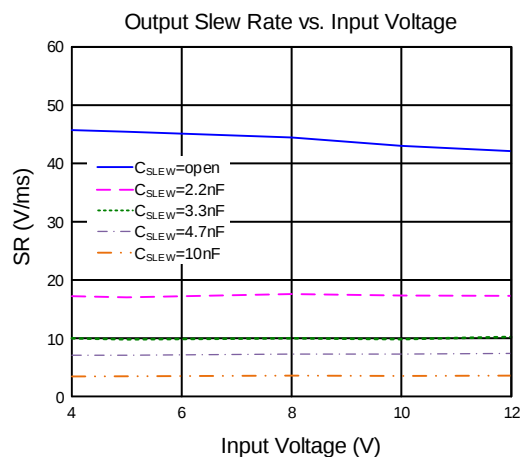
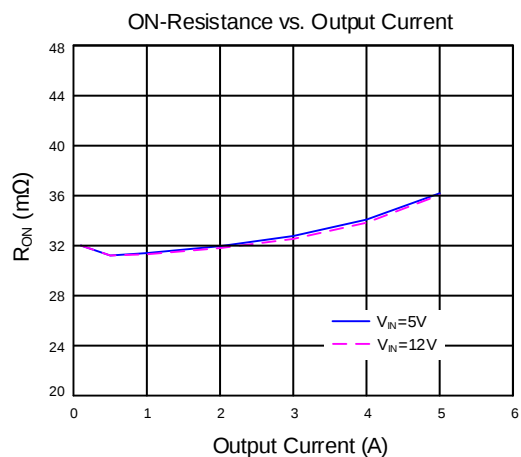
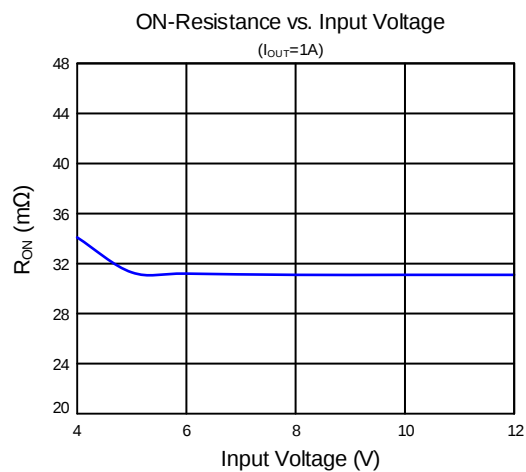
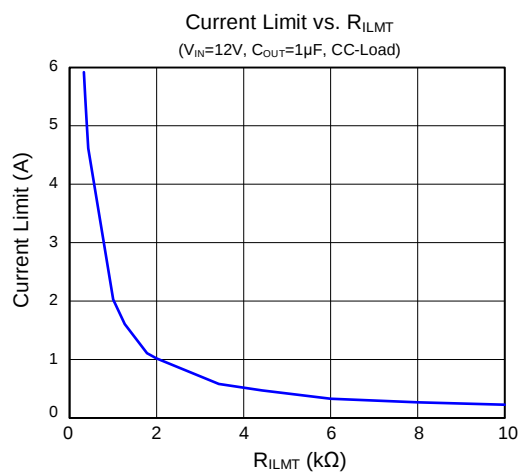
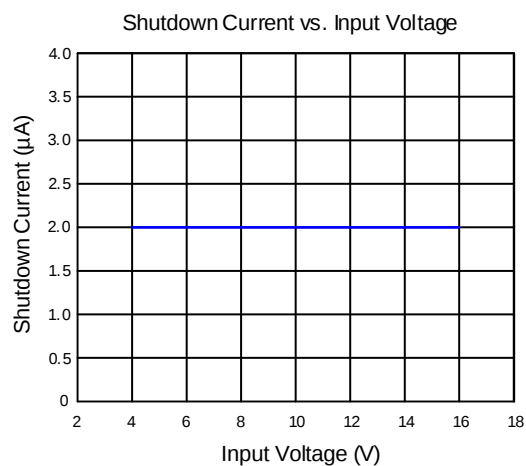
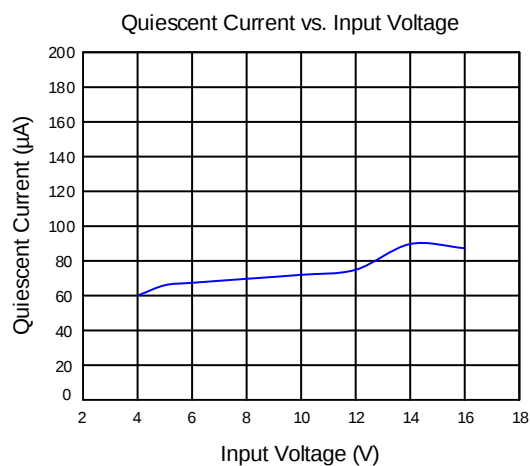
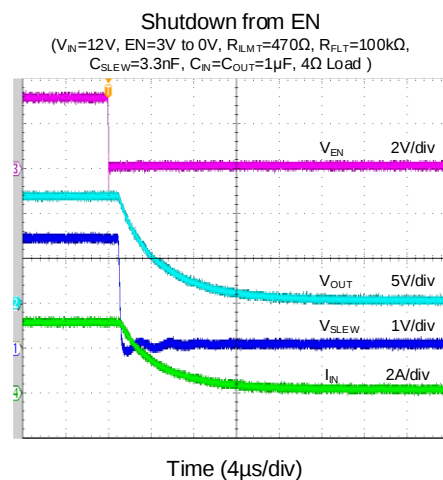
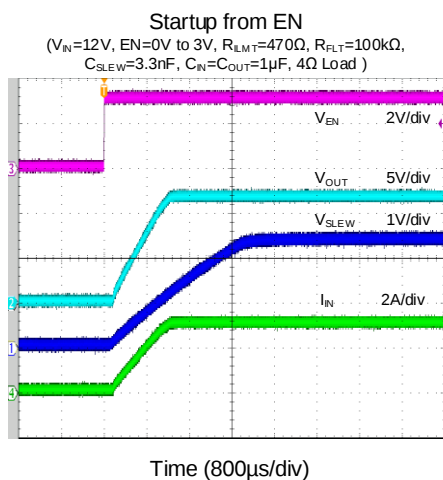
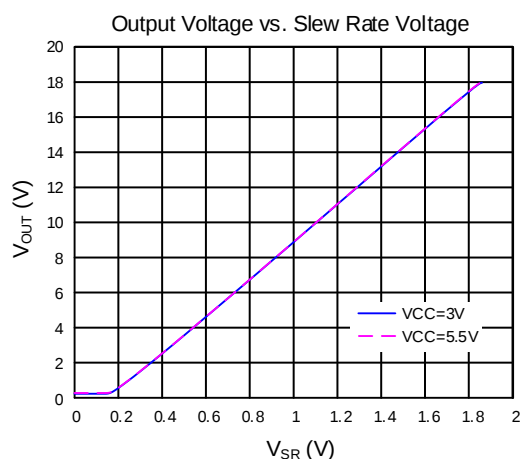
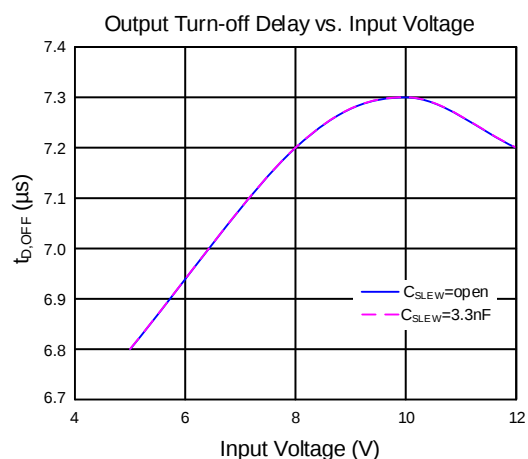
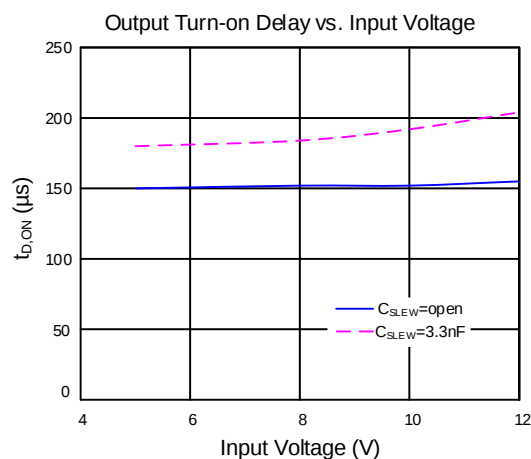
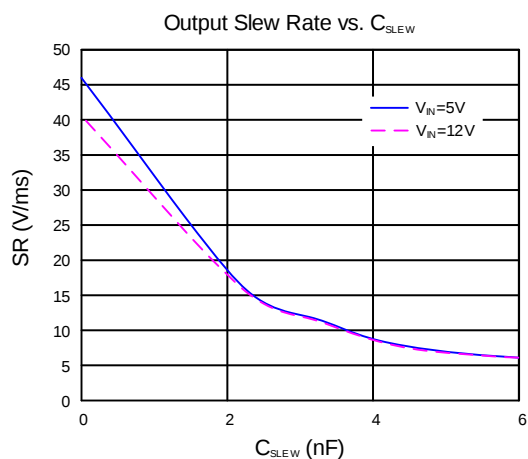
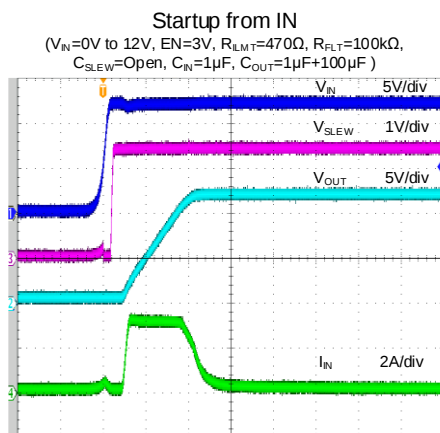


Figure 3. Switching Time

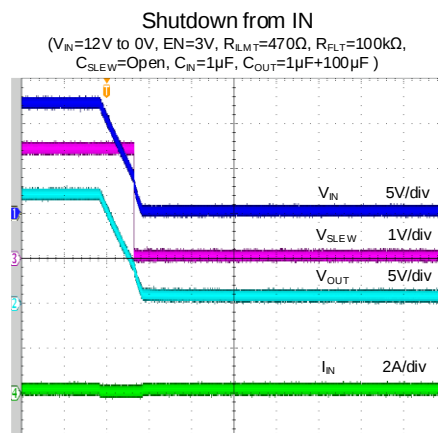
Typical Performance Characteristics



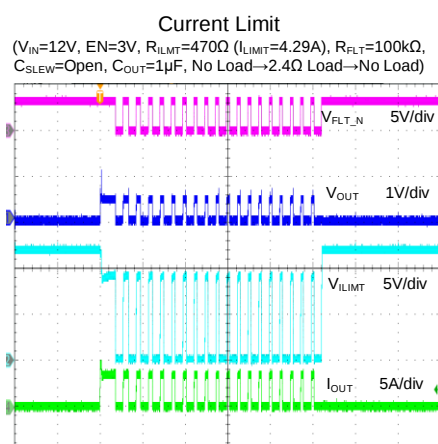




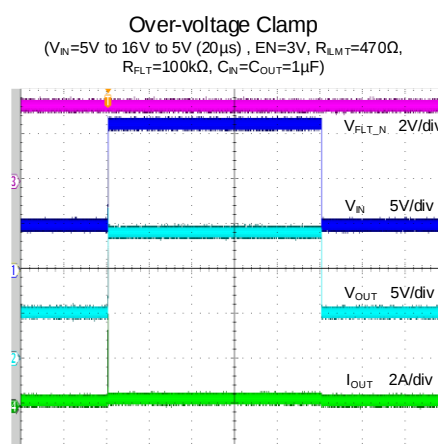
Time (200 μ s/div)



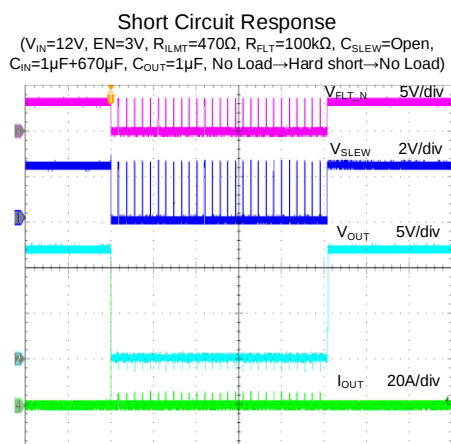
Time (10ms/div)



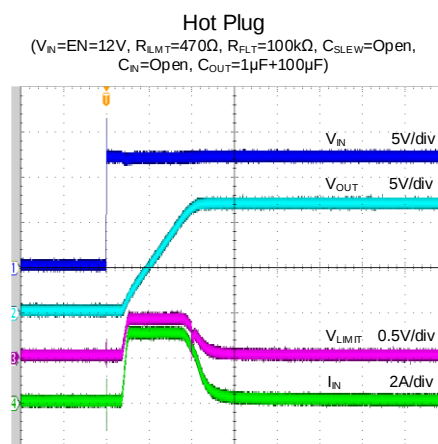
Time (20ms/div)



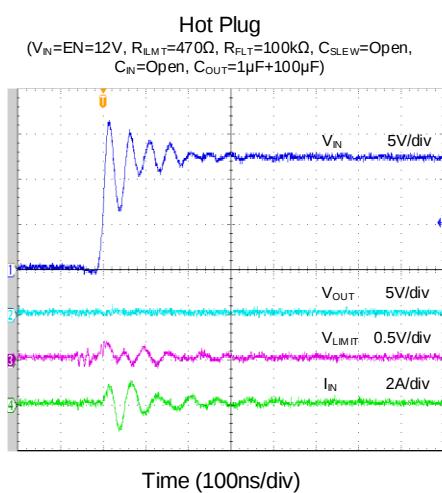
Time (20ms/div)



Time (20ms/div)



Time (200 μ s/div)



Application Information

Overvoltage Clamp (OVC)

OVC limits the OUT voltage to protect the load if the input supply exceeds the preset clamp threshold, V_{CLAMP} . This reduces the need to rely on conventional external protection devices such as TVS or Zener diodes.

If the input voltage exceeds the V_{CLAMP} , the device will clamp the output voltage to the V_{CLAMP} within a short response time (t_{CLPF}). If the input voltage remains below the clamp threshold, the output voltage will be equal to the input voltage.

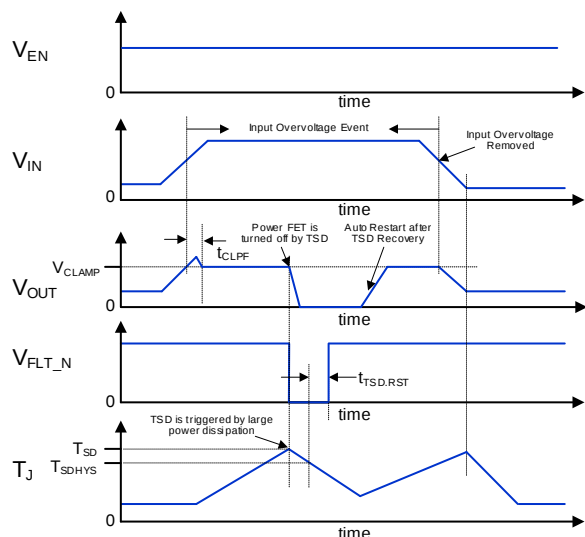


Figure 4. Overvoltage Clamp Response

Overcurrent Protection

The device continuously monitors the load current and keeps it limited to the value programmed by R_{ILMT} . After startup and during normal operation, the current limit is set to I_{LIMIT} . A 1% resistor is recommended for the R_{ILMT} to ensure stability of the internal regulation loop. Recommended formula for calculating R_{ILMT} based on the target current limit:

$$R_{ILMT} = \frac{2000}{I_{LIMIT} - 0.04} (\Omega)$$

When an overcurrent condition occurs ($I_{LIMIT} < I_{LOAD} < 2.5 \times I_{LIMIT}$), the device will maintain a constant output current and the output voltage will start falling. Thermal shutdown protection will occur if the fault is present long enough to activate thermal limiting. The device will remain off until the junction temperature decreases by approximately 20°C , at which point the device will auto restart. The device will continue to cycle ON/OFF until the overcurrent condition is resolved.

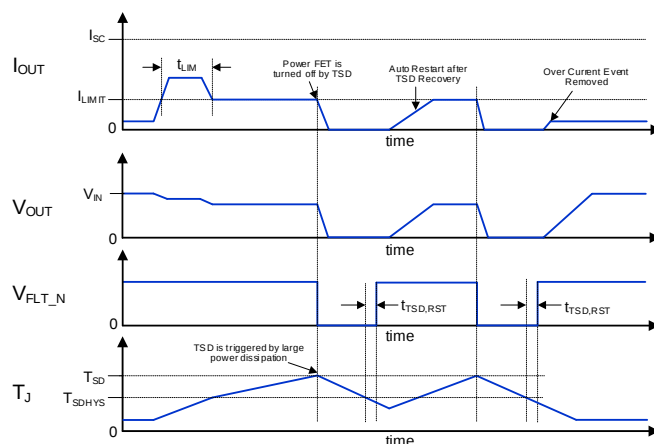


Figure 5. Overcurrent Response

When a short-circuit condition is detected ($I_{LOAD} > 2.5 \times I_{LIMIT}$), the SQ24802K2 immediately turns off the power path. It employs a fast-trip comparator with a threshold I_{SC} ($2.5 \times I_{LIMIT}$) to rapidly shut down the power MOSFET within $1\mu\text{s}$. The fast-trip circuit briefly keeps the internal MOSFET off for a few microseconds, and then the device gradually powers on, enabling the current-limit loop to regulate the output current to I_{LIMIT} . After this, the device attempts to restart under current limit conditions.

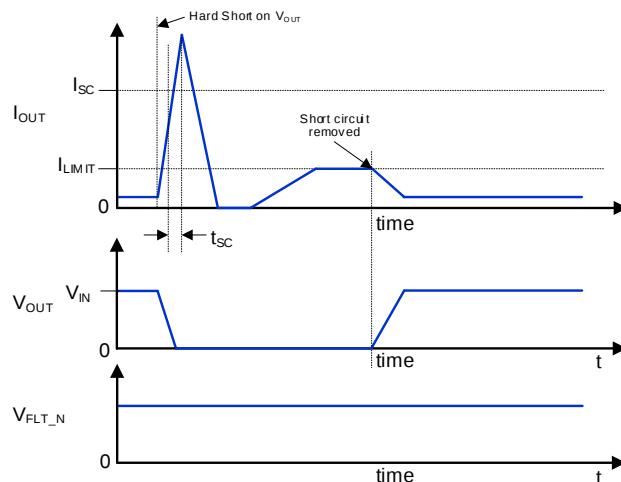


Figure 6. Short Circuit Response

Under Voltage Lockout (UVLO)

The SQ24802K2 features an integrated UVLO protection mechanism that turns off the MOSFET when the input voltage (V_{IN}) falls below the UVLO threshold. This device also offers a programmable UVLO threshold via the EN pin. Connect a voltage divider to the EN pin to monitor the input voltage. If EN drops below V_{ENF} (enable threshold, falling), the Power MOSFET will be turned off.

When maintaining the IN above the high UVLO upper threshold and EN above V_{ENR} (enable threshold, rising), the SQ24802K2 initiates the startup sequence and keeps the MOSFET in the ON state, ensuring power delivery from IN to OUT.

The design of both IN UVLO and EN includes hysteresis to prevent oscillation when the voltages at the IN or EN pins are near the threshold values.

Soft-start Time Programming

The SQ24802K2 integrates programmable output ramp control to minimize inrush current during startup. Connect a capacitor from SLEW to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum t_R) on the output.

Recommended formula for calculating C_{SLEW} and Soft-start slew rate:

$$\text{Slew Rate} = \frac{32000}{C_{SLEW} (\text{pF})} \left(\frac{\text{V}}{\text{ms}} \right)$$

$$t_R = 0.8 \times \frac{V_{IN}}{\text{Slew Rate}} (\text{ms})$$

FLT_N Response

The FLT_N open-drain output is pulled low during overtemperature condition. It is normally pulled high by an external pull-up resistor. The output will stay low until the fault condition is resolved. It is typically held high by an external pull-up resistor while in high-impedance state. The fault condition is cleared if the device loses power and T_J is below T_{SDHYS} . It is recommend that the pull up resistor is 100kΩ for 3.3V IO line.

Input Filter Capacitor

It is highly recommended to place a ceramic capacitor of 1μF or larger close to the device for optimal performance. The absence of an input capacitor can lead to ringing on the input in the event of an output short. This ringing can damage the internal circuitry if the input transient exceeds the absolute maximum supply voltage, even for a short duration.

Output Filter Capacitor

It is highly recommended to place a 1μF output ceramic capacitor close to the device and the output connector to reduce the voltage drop during load transients. Higher output capacitor values can further reduce the voltage drop. During a short-circuit scenario, parasitic wire inductance can pull the output to a negative voltage exceeding the normal operating conditions. A parallel Schottky diode is recommended to absorb large negative voltage transients, ensuring the output voltage remains within the absolute voltage ratings.

PCB Layout Guide

For the best performance of the SQ24802K2, the following guidelines must be strictly followed:

1. Keep all VBUS traces as short and wide as possible and use 2-ounce copper for connections.
2. Place the output capacitor as close to the device and the connectors as possible to improve transient performance and reduce the impedance and inductance between the port and the capacitor.
3. The input and output capacitors should be placed closed to the device and connected to the ground plane to reduce noise coupling.

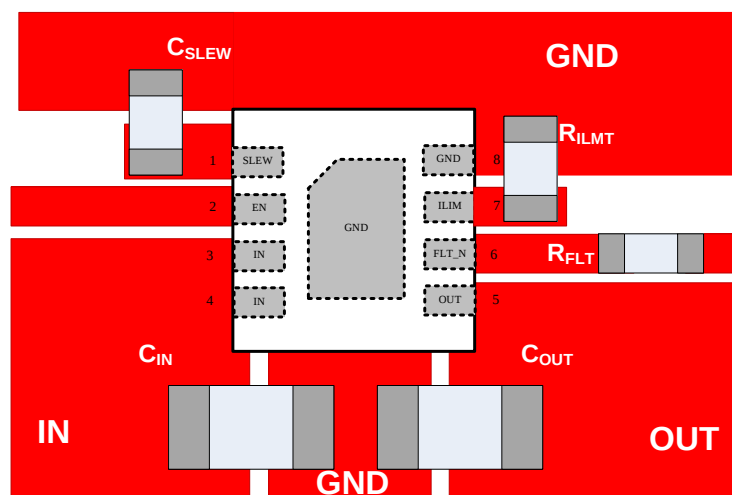
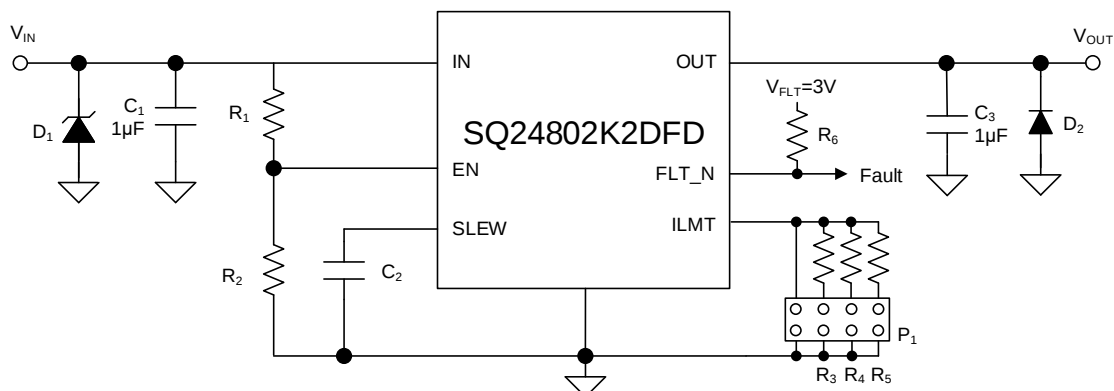


Figure 7. PCB Layout Suggestion

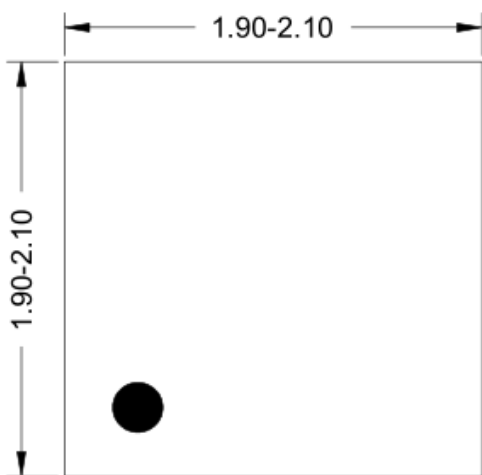
Schematic



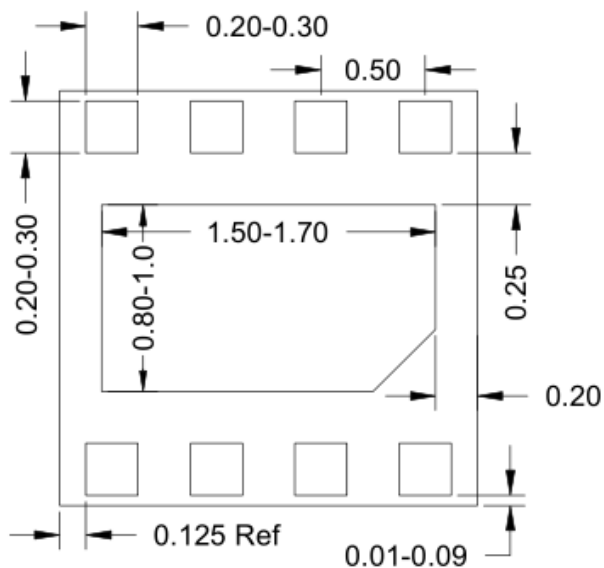
BOM List

Reference Designator	Description	Part Number	Manufacturer
C1	1μF/25V, ±10%, X5R, 0805	GRM21BR61E105KA99L	Murata
C2	4.7nF/50V, ±10%, X7R, 0603	GRM188R71H472KA01D	Murata
C3	1μF/50V, ±10%, X5R, 1206	GRM31CR71H105KA61L	Murata
R1	91kΩ, 1%, 0.1W, 0603	RC0603FR-0791KL	YAGEO
R2	12kΩ, 1%, 0.1W, 0603	RC0603FR-0712KL	YAGEO
R3	487Ω, 1%, 0.1W, 0603	RC0603FR-07487RL	YAGEO
R4	1780Ω, 1%, 0.1W, 0603	RC0603FR-071K78L	YAGEO
R5	4420Ω, 1%, 0.1W, 0603	RC0603FR-074K42L	YAGEO
R6	100kΩ, 1%, 0.1W, 0603	RC0603FR-07100KL	YAGEO
D1	TVS(optional)		Any
D2	Schottky(optional)		Any
P1	Jumper, 2×4, Gold		Any

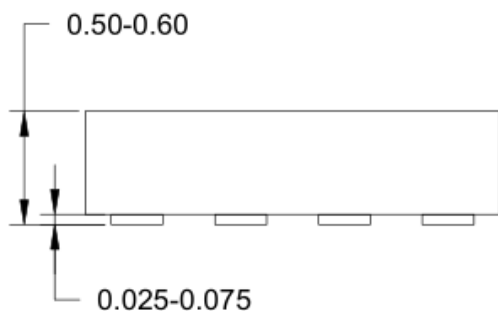
DFN2×2-8 Package Outline Drawing



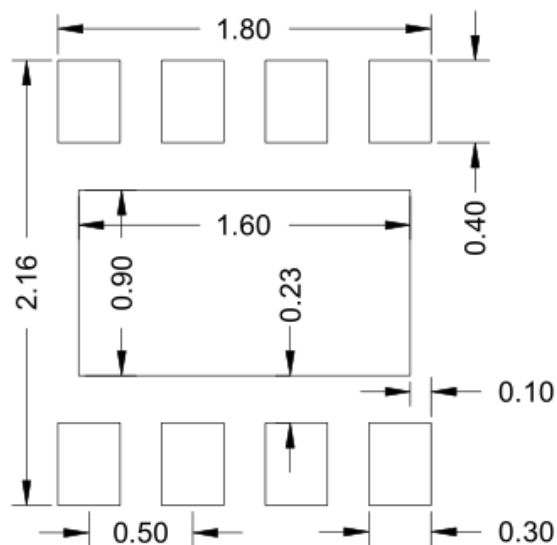
Top View



Bottom View



Side View

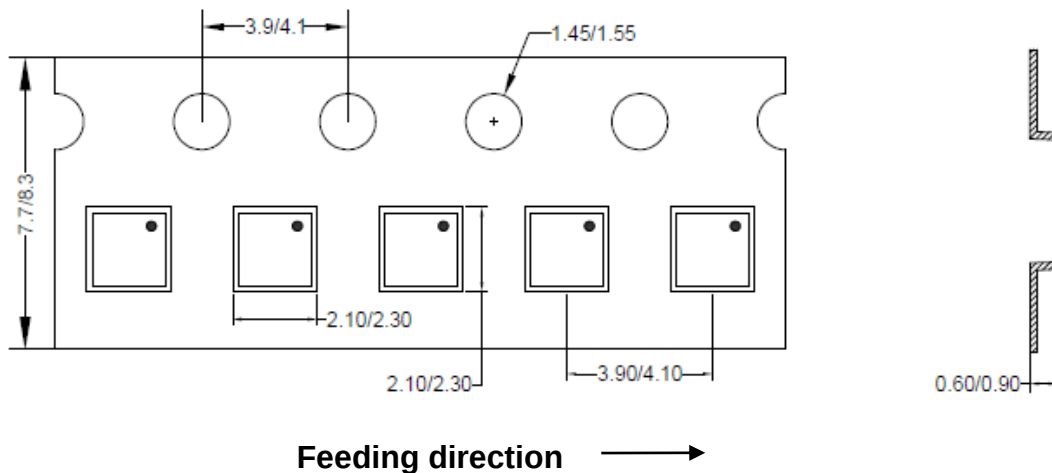


**Recommended PCB layout
(Reference only)**

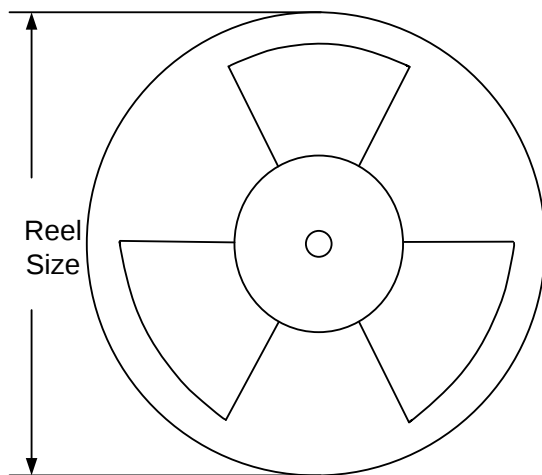
Notes: All dimensions are in millimeters and don't include mold flash & metal burr.

Tape and Reel Information

1. Tape Dimensions and Pin1 Orientation



2. Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
DFN2x2-8	8	4	7"	280	160	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Sep.05, 2025	Revision 1.0	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.
2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.
3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.
4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.
5. **Terms and conditions of commercial sale.** Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at <http://www.silergy.com/stdterms>, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.
6. **No offer to sell or license.** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com

©2025 Silergy Corp.

All Rights Reserved.