SA21816C

2.7V-18V Switch with True Reverse Blocking

General Description

The SA21816C smart switch is a highly integrated circuit and power management device, offering a range of protection functions, including a low-power DevSleep mode.

It operates across a wide input voltage range from 2.7V to 18V, making it suitable for controlling various DC BUS voltages in SSD applications. The device features integrated back-to-back MOSFETs for bidirectional current control, ideal for systems with load-side energy reservoirs that must not drain back to a failed supply BUS.

The SA21816C includes programmable features such as overcurrent, output slew rate control, overvoltage, and undervoltage thresholds, requiring minimal external components. It provides PGOOD, FLT_N, and precise current monitoring outputs for comprehensive system status monitoring and downstream load control. The device's precise programmability and low I_Q DevSleep mode enhance the simplicity of SSD power management design.

The SA21816C achieves true reverse current blocking by monitoring the condition V_{IN} < (V_{OUT} - 25mV). This facilitates a rapid transition to a boosted voltage energy storage element in systems where the backup voltage exceeds the BUS voltage.

Features

- AEC-Q100 Grade 1 Qualified
- Ultra Low $R_{DS(ON)}$: 46mΩ R_{ON} (Typical)
- Adjustable Current Limit: 0.6A to 5.3A
- IMON Current Indicator Output
- Operating I_Q: 130μA (V_{IN} = 12V, Typical)
- Reverse Current Blocking
- Programmable Output Slew Rate Control
- Power Good and Fault Outputs
- -40°C to 125°C Junction Temperature Range
- 2.7V - 18V Operating Voltage, 21V Max
- RoHS Compliant and Halogen Free
- Compact Package: QFN 3×4-20

Applications

- Automotive Applications
- ADAS (Advanced Driver Assistance Systems)
- Cameras and Radar Sensors
- USB Hubs
- Power MUX
- Power Management Backup

Typical Application

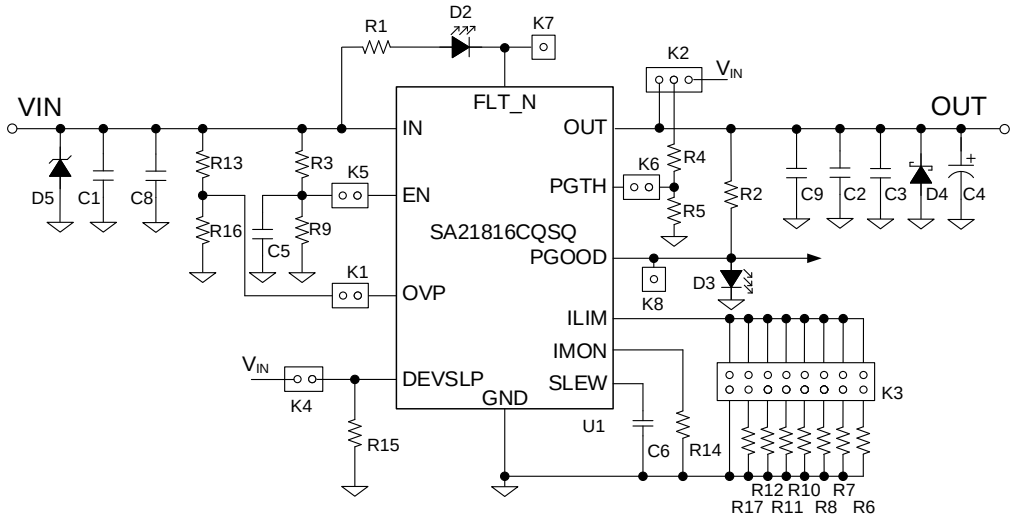


Figure 1. Schematic Diagram

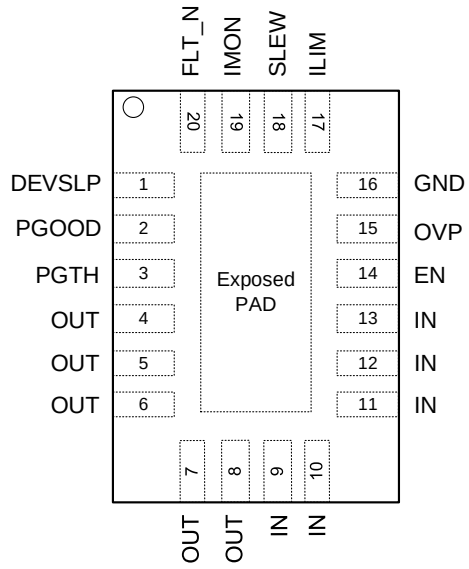
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA21816CQSQ	QFN3×4-20 RoHS Compliant and Halogen Free	**GKM*xyz***

Device code: GKM

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin NO.	I/O	Pin Description
DEVSLP	1	I	Active High. Controls DevSleep Mode. DevSleep mode (Low Power Mode) will activate with a high at this pin. If unused, leave it floating or connect it to GND.
PGOOD	2	O	Active High. A high indicates PGTH has crossed the threshold value. It is an open drain output. If unused, leave it floating.
PGTH	3	I	Positive input of PGOOD comparator. If unused, connect it to OUT or GND.
OUT	4-8	O	Power Output of the device.
IN	9-13	I	Power Input and supply voltage of the device.
EN	14	I	Input for setting programmable undervoltage lockout threshold. An undervoltage event will open internal MOSFET and assert FLT_N to indicate power failure.
OVP	15	I	Input for setting programmable overvoltage protection threshold. An overvoltage condition opens the internal MOSFET and asserts FLT_N to indicate an overvoltage event.
GND	16	-	Ground pin.
ILIM	17	I/O	Connecting a resistor from this pin to GND sets the overload and short-circuit current limit.
SLEW	18	I/O	Connecting a capacitor from this pin to GND sets the ramp rate of output voltage.
IMON	19	O	This pin sources a scaled-down current through the internal MOSFET. Connecting a resistor from this pin to GND converts the current into a proportional voltage, serving as an analog current monitor. If unused, leave it floating.
FLT_N	20	O	Fault event indicator. It goes low to indicate fault conditions due to undervoltage, overvoltage, reverse voltage, and thermal shutdown events. It is an open drain output. If unused, leave it floating.
Exposed Pad	-		The GND terminal must be connected to the exposed PAD. The exposed PAD must be connected to a PCB ground plane using several vias for optimal thermal performance.

Block Diagram

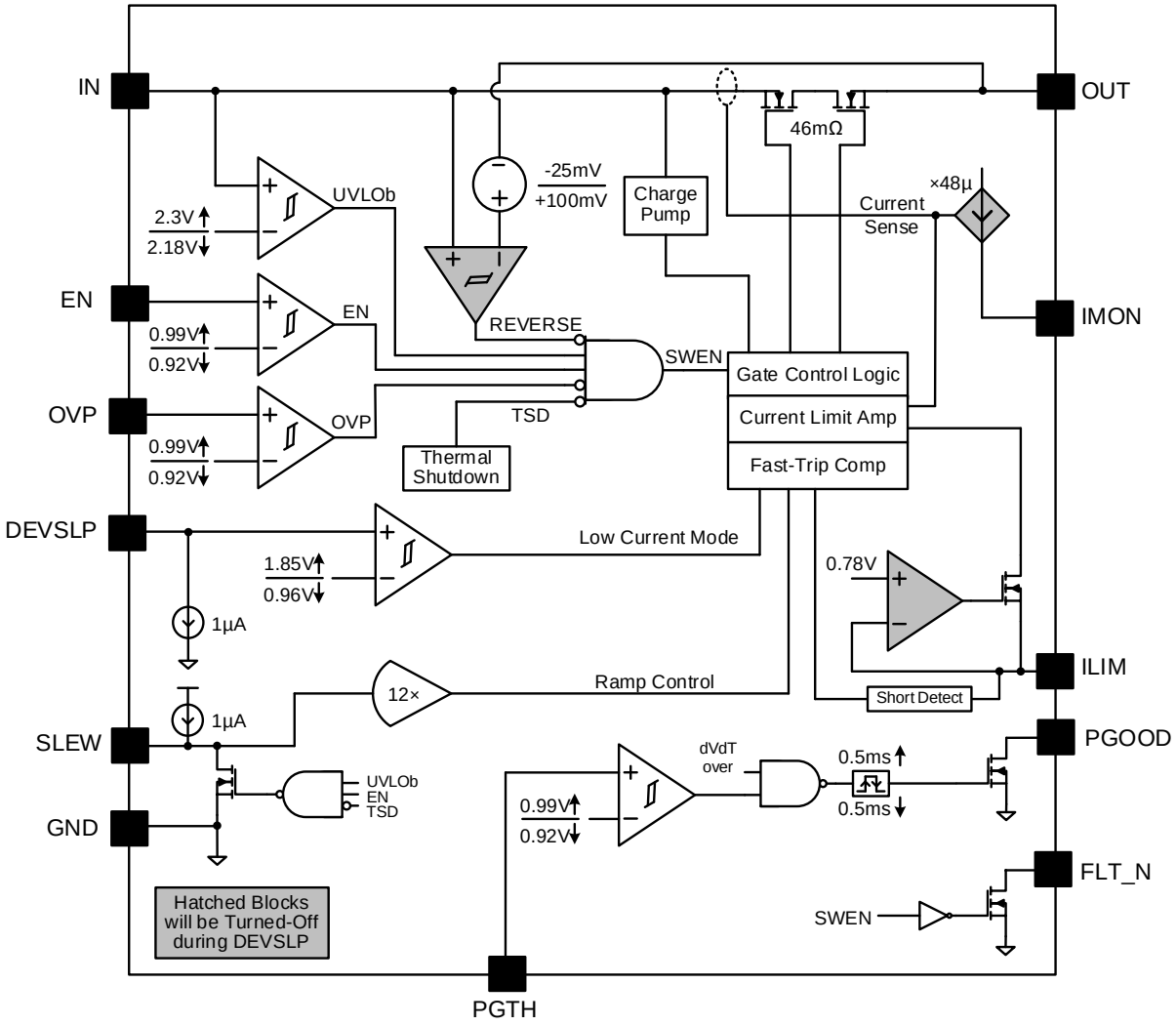


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN, PGTH, PGOOD, EN, OVP, DEVSLP, FLT_N	-0.3	21	V
OUT	-0.3	18	
SLEW, IMON	-0.3	7	
ILIM	-0.3	3.6	
PGOOD, FLT_N, SLEW Sink Current		10	mA
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	31.5	°C/W
θ_{JC} Junction-to-case Thermal Resistance	26	
P_D Power Dissipation T_A = 25°C	3.17	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.7	18	V
OUT, PGTH, PGOOD, EN, OVP, DEVSLP, FLT_N	0	18	
SLEW, IMON	0	6	
ILIM	0	3.3	
R_{ILIM}	16.9	150	kΩ
R_{IMON}	1		
C_{OUT}	0.1		µF
C_{SLEW}		470	nF
Junction Temperature	-40	125	°C
Ambient Temperature	-40	125	

Electrical Characteristics

(–40°C ≤ T_J=T_A ≤ 125°C, 2.7V ≤ V_{IN} ≤ 18V, V_{EN} = 2V, V_{OVP} =V_{DEVSLP} =V_{PGTH} = 0V, R_{ILIM} = 150kΩ, C_{OUT} =1µF, C_{SLEW}= OPEN, PGOOD = FLT_N = IMON = OPEN. typical values are at V_{IN}=12V, T_J=25°C, unless otherwise specified (Note 4)).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage and Internal Under-voltage Lockout						
Input Voltage Range	V_{IN}		2.7		18	V
Input UVLO Threshold	V_{UVLO}		2.2	2.3	2.4	V
UVLO Hysteresis	V_{HYS}		112	122	132	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0 V, V_{IN} = 3 V	3	9.5	16	µA
		V_{EN} = 0 V, V_{IN} = 12 V	3	11	20	
		V_{EN} = 0 V, V_{IN} = 18 V	3	11	25	
Quiescent Current	I_Q	V_{EN} = 2 V, V_{IN} = 3 V	60	121	165	µA
		V_{EN} = 2 V, V_{IN} = 12 V	65	130	170	
		V_{EN} = 2 V, V_{IN} = 18 V	65	130	170	
DevSleep Mode Current	I_{Q_DEVSLP}	V_{DEVSLP} = 0 V, V_{IN} = 2.7V to 18V	60	117	155	µA
Enable And Undervoltage Lockout (EN) Input						
EN Logic High	V_{ENH}		0.96	0.99	1.02	V
EN Logic Low	V_{ENL}		0.89	0.92	0.95	V
EN Threshold Voltage for Low I_Q Shutdown, Falling	V_{SHUTF}		0.23	0.47	0.66	V
EN Hysteresis for Low I_Q Shutdown				56		mV
EN Input Leakage Current	I_{EN}	0 V ≤ V_{EN}≤ 18 V	-100	0	100	nA
Over Voltage Protection (OVP) Input						
Overvoltage Threshold Voltage, Rising	V_{OVPR}		0.96	0.99	1.02	V
Overvoltage Threshold Voltage, Falling	V_{OVPF}		0.89	0.92	0.95	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OVP Input Leakage Current	I_{OVP}	0 V ≤ V_{OVP}≤ 5 V	-100	0	100	nA
DEVSLP Mode Input (DEVSLP): Active High						
DEVSLP Threshold Voltage, Rising	$V_{DEVSLPR}$		1.6	1.85	2	V
DEVSLP Threshold Voltage, Falling	$V_{DEVSLPF}$		0.8	0.96	1.1	V
DEVSLP Input Leakage Current	I_{DEVSLP}	0 V ≤ V_{OVP}≤ 18 V	0.5	1	1.35	µA
Output Ramp Control (SLEW)						
SLEW Charging Current	I_{SLEW}	V_{SLEW} = 0 V	0.8	1	1.2	µA
SLEW Discharging Resistance	R_{SLEW}	V_{EN} = 0V, I_{SLEW} = 10mA sinking		16	35	Ω
SLEW Maximum Capacitor Voltage	$V_{SLEWmax}$		1.4	2.5	3.1	V
SLEW to OUT Gain	G_{SLEW}	$\Delta V_{OUT}/\Delta V_{SLEW}$	11.4	11.9	12.2	V/V
MOSFET – Power Switch						
IN to OUT - ON Resistance	$R_{DS(ON)}$	1A ≤ I_{OUT}≤ 5A, T_J = 25°C		46	56	mΩ
		1A ≤I_{OUT}≤5A, -40°C≤T_J≤85°C		46	72	
		1A ≤I_{OUT}≤ 5A, -40°C≤T_J≤125°C		46	83	
Current Limit Programming (ILIM)						
ILIM Bias Voltage	V_{ILIM}			0.78		V
Current Limit	I_{LIM}	R_{ILIM} = 150 kΩ, (V_{IN} - V_{OUT}) = 1V	0.5	0.58	0.68	A
		R_{ILIM} = 88.7kΩ, (V_{IN} - V_{OUT}) = 1V	0.86	0.99	1.12	
		R_{ILIM} = 42.2kΩ, (V_{IN} - V_{OUT}) = 1V	1.82	2.08	2.35	
		R_{ILIM} = 24.9kΩ, (V_{IN} - V_{OUT}) = 1V	3.01	3.45	3.89	
		R_{ILIM} = 20kΩ, (V_{IN} - V_{OUT}) = 1V	3.73	4.28	4.81	
		R_{ILIM} = 16.9kΩ, (V_{IN} - V_{OUT}) = 1V	4.42	5.05	5.68	
		R_{ILIM} = OPEN	0.31	0.45	0.58	
		R_{ILIM} = SHORT	0.47	0.67	0.86	
DevSleep Mode Current Limit	$I_{DEVSLP(LIM)}$		0.47	0.67	0.86	A
Short-circuit Current Limit (Note 5)	I_{OS}	R_{ILIM} = 42.2kΩ, V_{IN}=12V, (V_{IN} - V_{OUT}) = 5V	1.72	2.07	2.45	A
		R_{ILIM} = 24.9kΩ, V_{IN}=12V, (V_{IN} - V_{OUT}) = 5V	3	3.49	4.05	
		R_{ILIM} = 16.9kΩ, V_{IN}=12V, (V_{IN} - V_{OUT}) =5V, -40°C≤T_J≤85°C	4.4	5.11	6	
Fast-Trip Comparator Threshold	$I_{FASTRIP}$		1.4 × I_{LIM} +2.2			A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Monitor Output (IMON)						
Gain Factor I_{IMON}/I_{OUT}	G_{IMON}	1 A ≤ I_{OUT}≤ 5 A	43.4	47.85	52.3	μA/A
Pass MOSFET Output (OUT)						
OUT Leakage Current in OFF State	I_{LKG_OUT}	V_{IN} =18V, V_{EN} = 0V, V_{OUT} = 0V (Sourcing)	-2	0	2	μA
		V_{IN} =2.7V, V_{EN} =0V, V_{OUT} = 0V (Sinking)	6	13	20	
V_{IN} -V_{OUT} Threshold for Reverse Protection Comparator, Falling	V_{REVTH}		-40	-25	-10	mV
V_{IN} -V_{OUT} Threshold for Reverse Protection Comparator, Rising	V_{FWDTH}		80	100	120	mV
Fault Flag (FLT_N): Active Low						
FLT_N Internal Pull-Down Resistance	R_{FLT_N}	V_{OVP} = 2 V, I_{FLT_N} = 5 mA sinking	15	30	60	Ω
FLT_N Input Leakage Current	I_{FLT_N}	0V ≤I_{FLT_N}≤ 18V	-1	0	1	μA
Positive Input for POWER-GOOD Comparator (PGTH)						
PGTH Threshold Voltage, Rising	V_{PGTHR}		0.96	0.99	1.02	V
PGTH Threshold Voltage, Falling	V_{PGTHF}		0.89	0.92	0.95	V
PGTH Input Leakage Current	I_{PGTH}	0 V ≤V_{PGTH}≤ 18 V	-100	0	100	nA
POWER-GOOD Comparator Output (PGOOD): Active High						
PGOOD Internal Pull-Down Resistance	R_{PGOOD}	V_{PGTH} = 0V, I_{PGOOD} = 5 mA sinking	15	30	60	Ω
PGOOD Input Leakage Current	I_{PGOOD}	0 V ≤ V_{PGOOD}≤ 18 V	-1	0	1	μA
Thermal Shut Down (TSD)(Note 5)						
TSD Threshold	T_{TSD}			160		°C
TSD Hysteresis	T_{TSDHYS}			12		°C
Overvoltage Protection Input (OVP)						
OVP Disable Delay	$t_{OVP(dly)}$	OVP↑ (100mV above V_{OVPR}) to FLT_N↓		2		μs
ENABLE						
EN Turn on Delay	$t_{ON(dly)}$	EN↑(100mV above V_{ENR}) to V_{OUT} = 100 mV, C_{SLEW}< 0.8 nF		220		μs
		EN↑(100mV above V_{ENR}) to V_{OUT} = 100 mV, C_{SLEW} ≥ 0.8 nF	100 + 150 ×C_{SLEW}			μs
EN Turn off Delay	$t_{OFF(dly)}$	EN↓(100mV below V_{ENF}) to FLT_N↓		2		μs
Output Ramp Control						
Output Ramp Time	t_{SLEW}	EN↑to V_{OUT} = 4.5V, with C_{SLEW} = open		0.295		ms
		EN↑to V_{OUT} = 11V, with C_{SLEW} = open	0.31	0.49	0.66	
		EN↑to V_{OUT} = 11V, with C_{SLEW} = 1nF		1.355		
Current Limit						
Fast-Trip Comparator Delay (Note 5)	$t_{FASTRIP(dly)}$	I_{OUT}> $I_{FASTRIP}$		320		ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Protection Comparator(Note 5)						
Reverse Protection Comparator Delay	$t_{REV(dly)}$	(V_{IN} - V_{OUT})↓(1 mV overdrive below V_{REVTH}) to FLT_N↓		10		µs
		(V_{IN} - V_{OUT})↓(10 mV overdrive below V_{REVTH}) to FLT_N↓		1		
	$t_{FWD(dly)}$	(V_{IN} - V_{OUT})↑(10 mV overdrive below V_{REVTH}) to FLT_N↑		3.1		
POWER-GOOD Comparator Output (PGOOD): Active High						
PGOOD Delay (de-glitch) Time	t_{PGOODR}	Rising edge	0.28	0.54	0.86	ms
	t_{PGOODF}	Falling edge	0.28	0.54	0.86	ms
Thermal Shut Down (TSD)						
Retry Delay in TSD				128		ms

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured with natural convection at T_A = 25°C on a highly effective four-layer thermal conductivity test board of JESD5-2,-5,-7 thermal measurement standards.

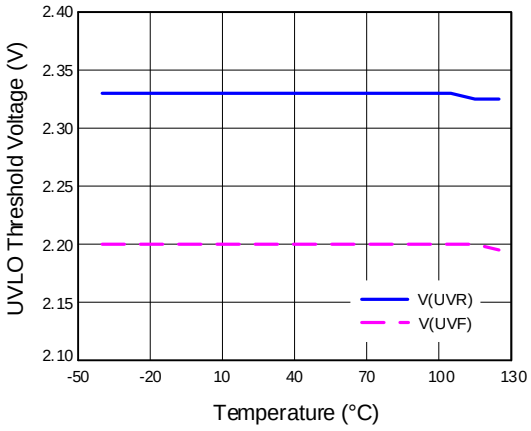
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$= 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

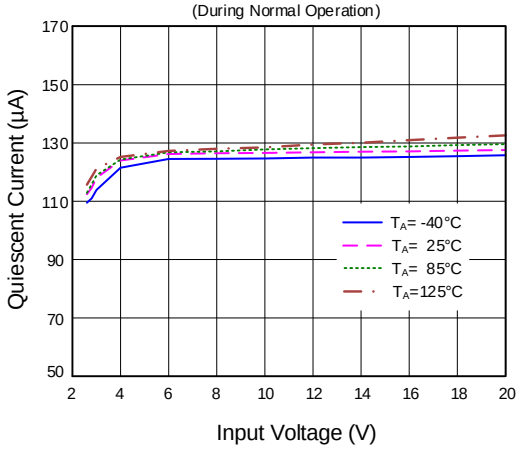
Note 5: Guaranteed by design or statistical correlation and not production tested.

Typical Performance Characteristics

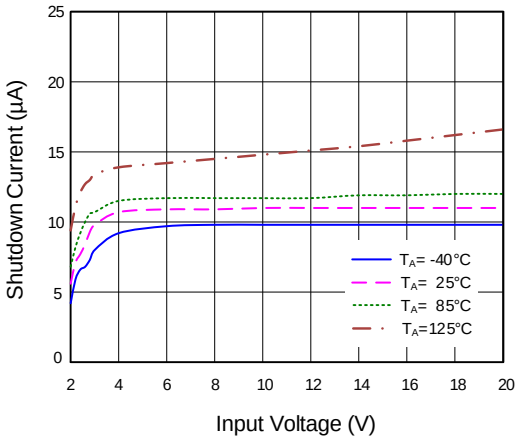
UVLO Threshold Voltage vs. Temperature



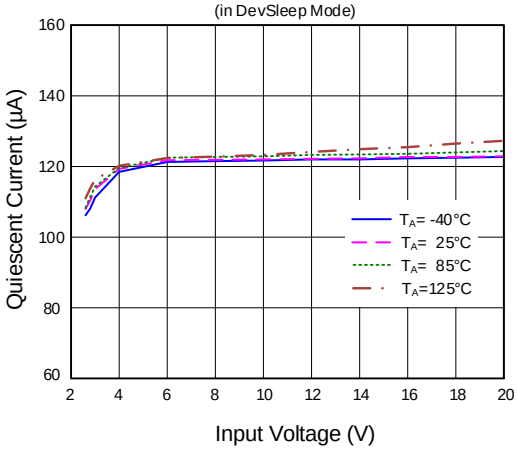
Quiescent Current vs. Input Voltage
(During Normal Operation)



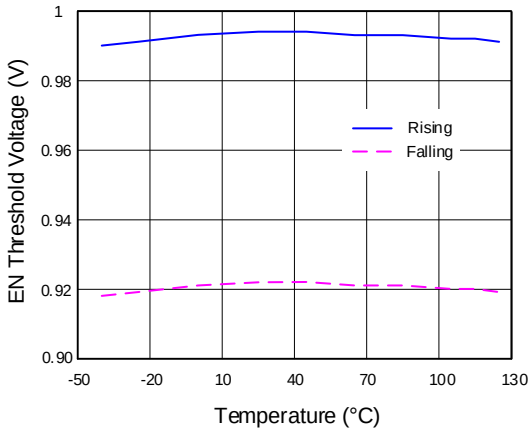
Shutdown Current vs. Input Voltage



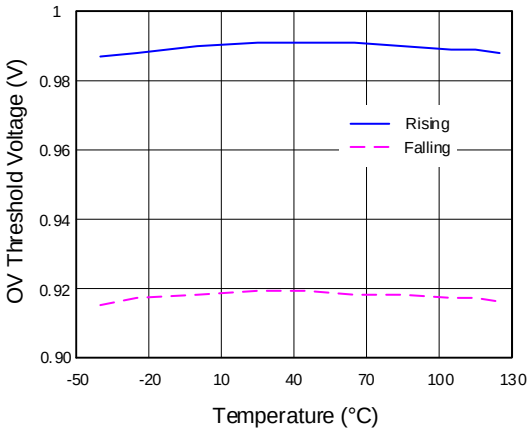
Quiescent Current vs. Input Voltage
(in DevSleep Mode)



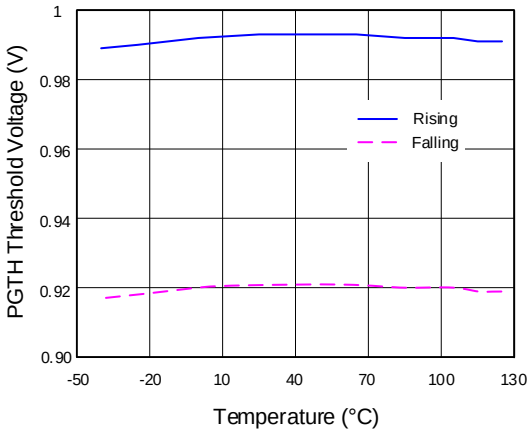
EN Threshold Voltage vs. Temperature



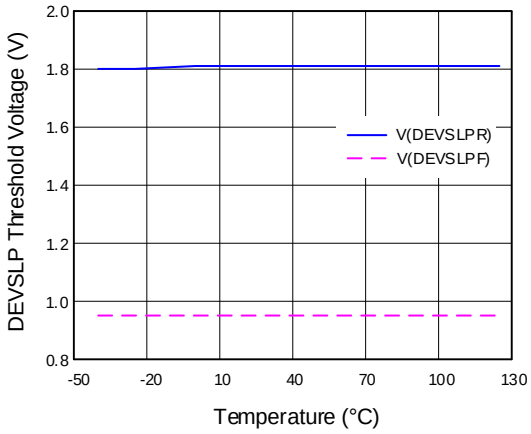
OV Threshold Voltage vs. Temperature



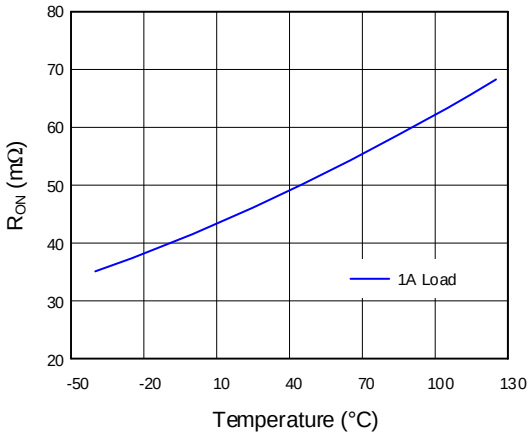
PGTH Threshold Voltage vs. Temperature



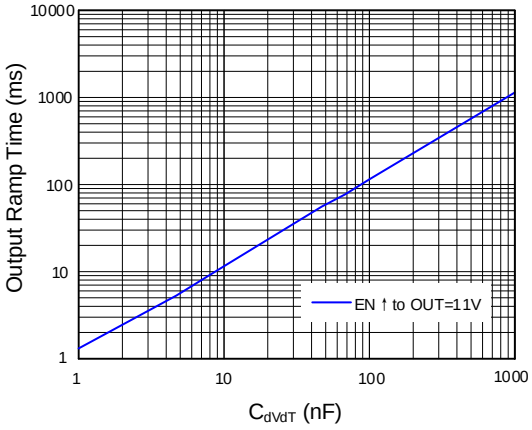
DEVSLP Threshold Voltage vs. Temperature



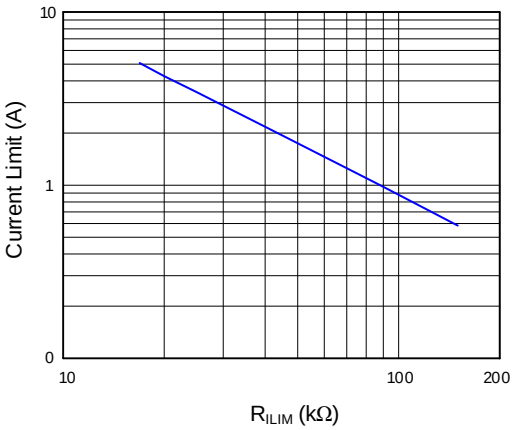
R_{ON} vs. Temperature



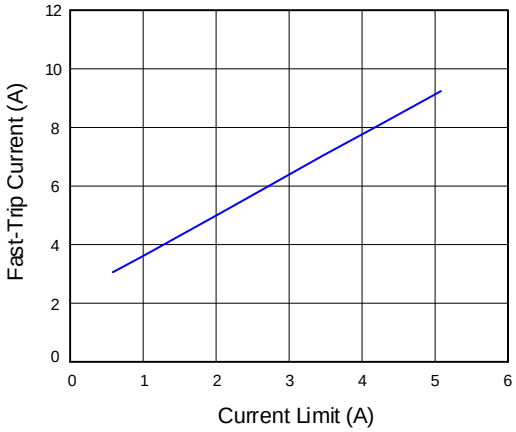
Output Ramp Time vs. C_{dVdT}



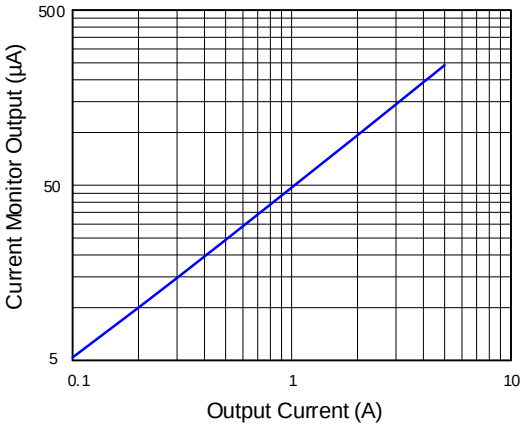
Current Limit vs. Current Limit Resistor



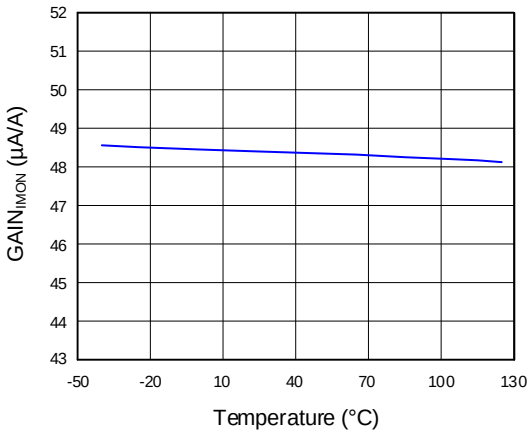
Fast-Trip Threshold vs. Current Limit



Current Monitor Output vs. Output Current

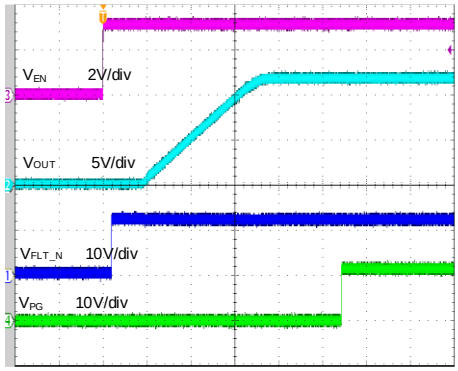


$GAIN_{IMON}$ vs. Temperature



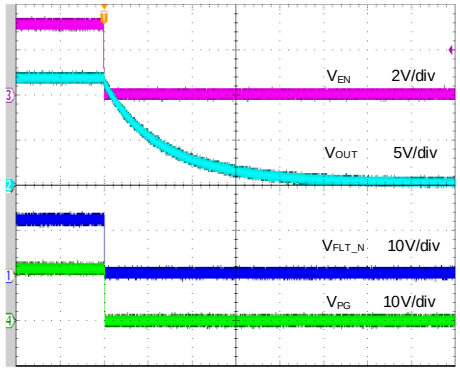
Startup from Enable

(V_{IN}=12V, V_{EN}=3V, C_{SLEW}=1nF, C_{OUT}=100μF, 6Ω Load)



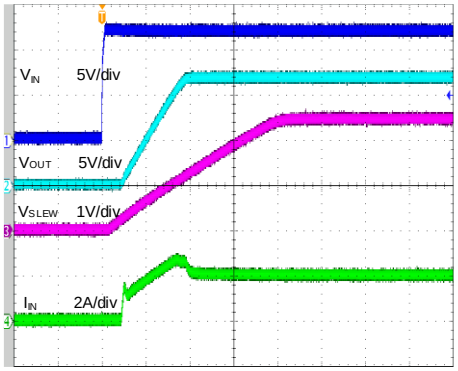
Shutdown from Enable

(V_{IN}=12V, V_{EN}=3V, C_{SLEW}=1nF, C_{OUT}=100μF, 6Ω Load)



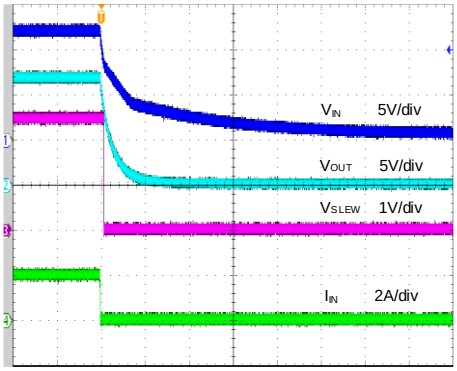
Startup from VIN

(V_{IN}=12V, C_{SLEW}=1nF, C_{IN}=100nF, C_{OUT}=100μF, 6Ω Load)



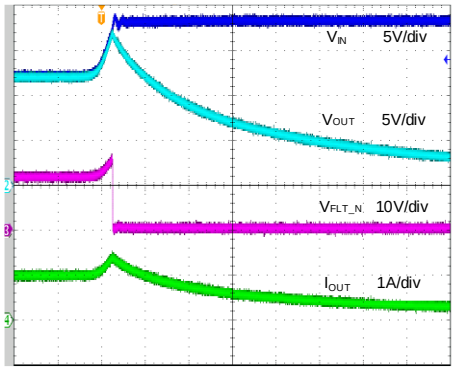
Shutdown from VIN

(V_{IN}=12V, C_{SLEW}=1nF, C_{IN}=100nF, C_{OUT}=100μF, 6Ω Load)



Overvoltage Shutdown

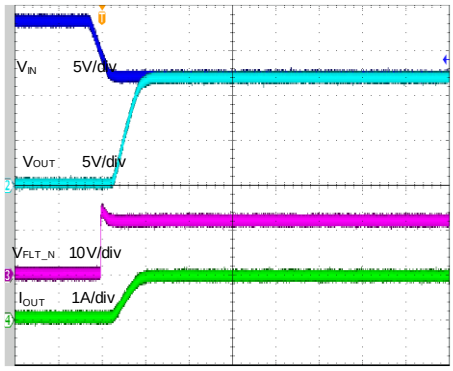
(V_{IN}=12V→18V (OVP set=16V), C_{OUT}=10μF, 12Ω Load)



Time (20μs/div)

Overvoltage Recovery

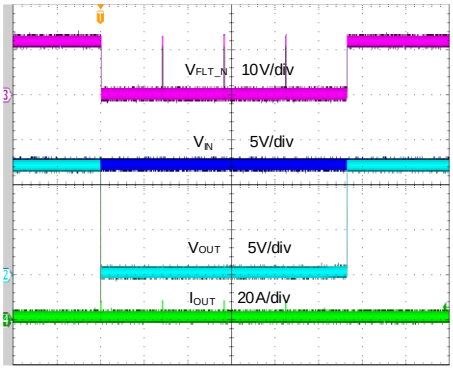
(V_{IN}=18V→12V, C_{OUT}=10μF, 12Ω Load)



Time (200μs/div)

Hard-Short: Auto-Retry and Recovery from Short

(V_{IN}=12V, C_{IN}=C_{OUT}=10μF, R_{ILIM}=16.9kΩ)



Time (100ms/div)

Application Information

The SA21816CQSQ is a smart load switch featuring integrated back-to-back MOSFETs and advanced protection circuitry, making it suitable for systems and applications operating between 2.7V and 18V.

The device provides hot-swap power management for hot-plug applications with an in-rush current limit during a programmable soft-start. The device is equipped with a precision overcurrent limit to minimize the over-design of the input power supply. The device also integrates a short-circuit protection that helps protect both the part and system from a sudden high-current event when a short circuit is detected. The overcurrent limit can be programmed between 0.6A and 5.3A using an external resistor.

This device is designed to safeguard systems, such as USB hubs, from sudden short-to-battery events at the output. It monitors V_{IN} and V_{OUT} to enable true reverse blocking at the output, activating this protection when a short-to-battery fault condition or an input power failure is identified.

Undervoltage Lockout and Overvoltage Set Point:

The undervoltage lockout (UVLO) and overvoltage trip point can be set with an external voltage divider network consisting of resistors R1, R2, and R3, connected between the IN, EN, OVP, and GND pins of the device.

The required values for the undervoltage and overvoltage settings are determined by solving these equations:

$$V_{OVPR}(V)=\frac{R_3}{R_1+R_2+R_3}\times V_{OV}$$

$$V_{ENR}(V)=\frac{R_2+R_3}{R_1+R_2+R_3}\times V_{UV}$$

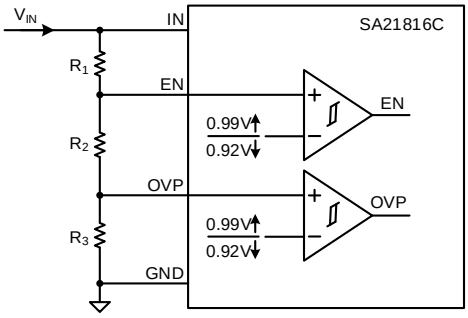


Figure 3. UVLO and OVP Thresholds Set by R_1, R_2 and R_3

It is recommended that larger resistance values for R1, R2, and R3 be used to minimize the input current drawn from the power supply.

However, this can introduce errors in these calculations due to leakage currents from external devices connected to the resistor string. It is recommended to use a resistor string current 20 times greater than the expected leakage current to obtain optimal threshold accuracy.

Overvoltage Protection

Setting the overvoltage protection (OVP) falling threshold (V_{OVPF}) below the normal operating voltage is not recommended, as it could lead to unintended OVP activation, especially when the enable (EN) is turned on and the input voltage (V_{IN}) exceeds V_{OVPF}. To prevent such mis-triggering, activate EN before increasing V_{IN}. It is important to note that if OVP is triggered under these conditions, the SA21816C will not recover from OVP because V_{IN} will not decrease below V_{OVPF}.

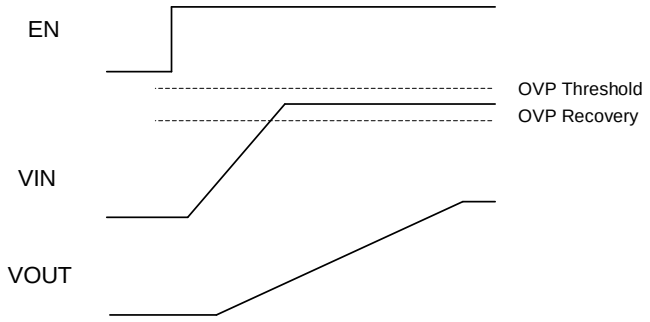


Figure 4. VIN and EN Timing Sequence

Overload Protection:

The device continuously monitors the load current and limits it to the value programmed by R_{ILIM}. During overload events, the current limit is set to I_{LIM} (over-load current limit), as shown in the following equation:

$$I_{LIM}=\frac{89}{R_{ILIM}}$$

Where:

- I_{LIM} is the overload current limit in Amperes
- R_{ILIM} is the current limiting resistor value, in kΩ

The internal current-limit amplifier maintains the output current at ILIM during the current-limiting phase. This regulation causes the output voltage to decrease, resulting in increased power dissipation for the internal MOSFET. If this condition persists, it will result in a thermal shutdown, turning off the device. During thermal shutdown, the SA21816C enters an auto-retry cycle 128ms after $T_J < [T_{TSD} - 12°C]$. The fault pin FLT_N is also activated (driven low) to signal a fault condition.

Short-Circuit Protection:

The device features a separate high-bandwidth current sense comparator with a fast-trip threshold ($I_{FASTRIP}$). $I_{FASTRIP}$ is adjusted based on the selected current limit:

$$I_{FASTRIP}=1.4\times I_{LIM}+2.2$$

During a transient short-circuit event, the device experiences a rapid increase in current. The current-limit amplifier, limited by its bandwidth, cannot respond instantly to this surge. Therefore, the fast-trip circuit intervenes, allowing the device to control the surge within 1µs upon detecting a short-circuit (I_{OUT} > $I_{FASTRIP}$). It temporarily switches off the internal MOSFET for several microseconds, after which the current limit amplifier takes over, regulating the output current to ILIM. Then, the device behaves similarly to if it were in an overload condition.

Current Monitoring:

The device provides a current mirror at the IMON pin proportional to the output current. A resistor R_{IMON} connected from the IMON pin to the GND converts the sensed current to a voltage. The sense voltage at the IMON pin is calculated using the following equation:

$$V_{IMON}=(I_{OUT}\times GAIN_{IMON}+I_{IMON\ OS})\times R_{IMON}$$

Where:

- $GAIN_{IMON}$ = Gain factor I_{IMON}/I_{OUT} = 48µA/A
- I_{OUT} = Load current
- I_{IMON_OS} = 0.8µA (typ)

This output can be connected to a downstream ADC for system health monitoring. The R_{IMON} must be configured based on the maximum input voltage range of the ADC used. R_{IMON} is set using the following formula:

$$R_{IMON}=\frac{V_{IMONmax}}{I_{LIM}\times 48\times 10^{-6}}\text{k}\Omega$$

If the IMON pin voltage is not digitized with an ADC, R_{IMON} can be selected to produce a 1V/1A voltage at the IMON pin by selecting a resistor value of 20kΩ. (1% tolerance is recommended for optimal accuracy).

This pin should not have a bypass capacitor to avoid delay in the current monitoring information.

IN, OUT, and GND Pins

The device has multiple input (IN) and output (OUT) pins.

All the IN pins should be connected to each other and to the power source. C_{IN} is a bypass capacitor that helps control transient voltages, limit emissions, and reduce noise from local power supply. Where acceptable, a value of 0.1µF to 10µF is recommended for C_{IN}. The voltage rating should be 20% higher than the maximum expected input voltage.

The GND terminal is the most negative voltage in the circuit and is used as a reference unless otherwise specified.

Device Functional Modes

The SA21816C features a dedicated DevSleep interface pin (DEVSLP) to control the device and help it enter low-power mode.

The DEVSLP pin is designed to interface with standard signals from the host controller. Pulling the DEVSLP pin high activates the device's low-power DevSleep mode. In DevSleep mode, the quiescent current is reduced to below 155µA (117µA typical), while the output voltage is maintained. The current limit is adjusted to IDEVSLP(LIM), and functions like the reverse blocking comparator and the current monitor are disabled. However, all other protection features remain engaged, ensuring system safety even in DevSleep mode.

Hot Plug-in and In-Rush Current Control

The device has a controlled output slew rate, providing soft start functionality. This limits the inrush current caused by the output capacitor(s) charging, and enables these devices to be used in hot-swap applications. The slew rate can be decreased with an external capacitor added between the SLEW pin and the ground (as shown in Figure 4). With an external capacitor present, the slew rate can be determined by the following equation:

$$I_{SLEW}=(\frac{C_{SLEW}}{GAIN_{SLEW}})\times(\frac{dV_{OUT}}{dt})$$

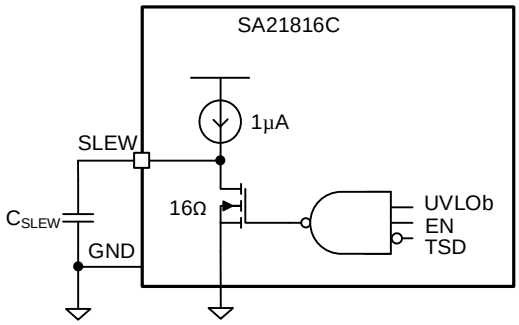


Figure 5. Output Ramp-Up Time (t_{SLEW}) set by C_{SLEW}

Where:

- I_{SLEW} = 1µA (typical)
- $\frac{dV_{OUT}}{dt}$ = Desired output slew rate
- $GAIN_{SLEW}$ = SLEW to OUT gain = 12

The total ramp time (t_{SLEW}) of V_{OUT} for 0 to V_{IN} can be determined using the following equation:

$$t_{SLEW}=8.3\times10^{4}\times V_{IN}\times C_{SLEW}$$

The SLEW pin can be left floating if the slew rate is not decreased. When left floating, the device uses the default value of 36V/ms for the output slew rate.

FAULT Response

The FLT_N pin asserts (active low) when one of the following fault conditions are detected: undervoltage, overvoltage, reverse blocking, and thermal shutdown. The FLT_N signal remains asserted until the fault conditions are addressed and the device resumes regular operation. An internal "deglitch" circuit for undervoltage and overvoltage (2.2μs typical) conditions filters unexpected false faults during transients on the input bus. Using this pin requires an external pull-up resistor to an external voltage rail. If FLT_N reporting is not used in the application, the FLT_N pin may be left open or tied to the ground. V_{IN} falling below V_{UVF} = 2.1V resets the FLT_N pin status.

Reverse Blocking

The SA21816C monitors the reverse voltage from IN to OUT, and when it exceeds -25 mV, the device will shut off its internal MOSFETs to stop the flow of reverse current. It will begin to recharge the GATE when V_{IN} > (V_{OUT} + 100mV). The output voltage may drop before GATE reaches V_{TH} (gate-source threshold voltage). It is recommended that large output capacitors be utilized to minimize this voltage drop.

In addition, the device provides an instant warning signal (FLT_N) to the controller to initiate the data backup process. Its rapid true reverse blocking feature reacts in 1μs (typical), ensuring that the charge in the capacitor bank is retained. This feature allows the system to maintain power for a longer duration for data protection, and reduces the capacitance required in the capacitive reservoir.

Power Good Comparator

The power-good (PGOOD) output can indicate whether the output voltage is above a user-defined threshold and can, therefore, be considered within the acceptable range by downstream DC-DC converters or system monitoring circuits. A resistor divider connected to the PGTH pin sets an accurate power-good threshold for the output voltage. The PGOOD pin is an open-drain output that is high-impedance when the voltage at the PGTH pin is higher than 0.99 V.

The PGOOD signal has deglitch time incorporated to ensure that internal MOSFET is fully biased before downstream converters apply heavy load. Controlling the de-glitch delay can be done by using the equation:

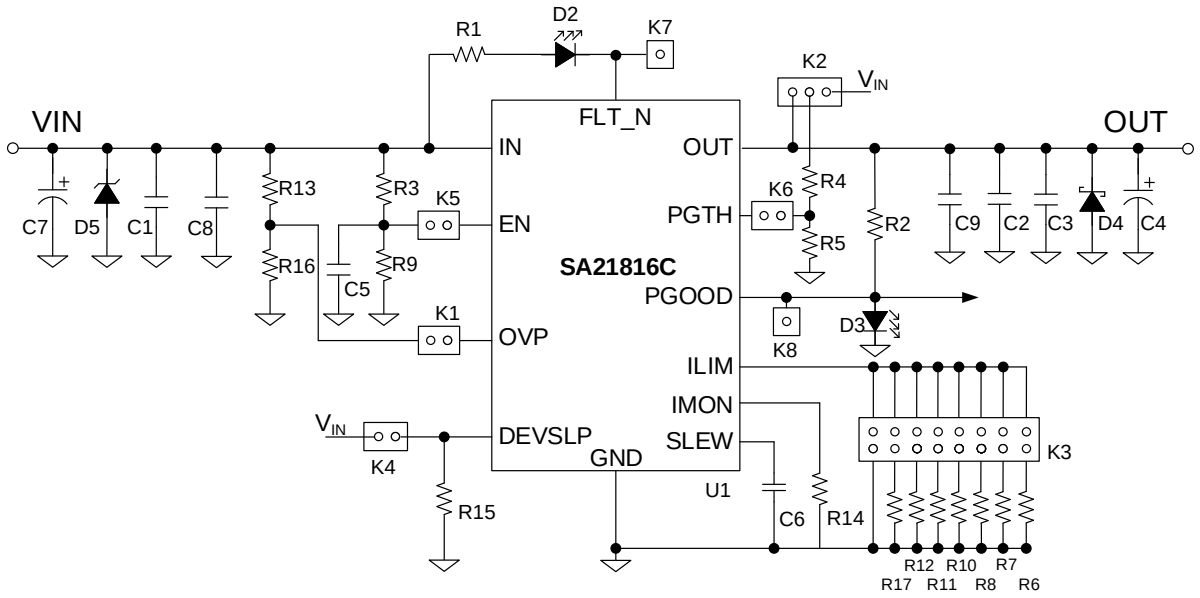
$$t_{PGOOD(degl)} = \text{Maximum}\{(2.5\times10^{5}\times C_{SLEW}), t_{PGOODR}\}$$

The pin requires an external pull-up resistor to the input or output voltage rails. If PGOOD reporting is not used, PGOOD may be left open or tied to the ground.

Thermal Shutdown

Internal overtemperature shutdown turns off the MOSFET when T_J > 160°C (typical). The SA21816C starts an auto-retry cycle 128ms after T_J drops below [T_{TSD} - 12°C]. During the thermal shutdown, the fault pin FLT_N is driven low to signal a fault condition.

Application Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1, C_2, C_3, C_9	10μF/50V, 1206	GRM319R61E106KA12D+A01	Murata
C_4,C_7	electrolytic capacitor (optional)		
C_5	1nF/50V, 0603	GRM188R61H102KA01D+C01A	Murata
C_6	10nF/50V, 0603	GRM188R61H102KA01D+C01A	Murata
C_8	100nF/50V, 0402 (optional)		
D_2, D_3	LED		
D_4	40V, 5A, Schottky	SS54	
D_5	TVS (optional)		
R_1, R_2, R_4, R_{15}	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R_3	120kΩ, 0603	RC0603FR-07120KL	YAGEO
R_5, R_{16}	10kΩ, 0603	RC0603FR-0710KL	YAGEO
R_6, R_{13}	150kΩ, 0603	RC0603FR-07150KL	YAGEO
R_7	88.7kΩ, 0603	RC0603FR-0788K7L	YAGEO
R_8	42.2kΩ, 0603	RC0603FR-0742K2L	YAGEO
R_9	15kΩ, 0603	RC0603FR-0715KL	YAGEO
R_{10}	24.9kΩ, 0603	RC0603FR-0724K9L	YAGEO
R_{11}, R_{14}	20kΩ, 0603	RC0603FR-0720KL	YAGEO
R_{12}	16.9kΩ, 0603	RC0603FR-0716K9L	YAGEO
R_{17}	39kΩ, 0603	RC0603FR-0739KL	YAGEO

PCB Layout Guide

For the best performance of the SA21816C, the following guidelines must be followed:

1. A 0.1μF or greater ceramic decoupling capacitor is recommended for all applications between the IN terminal and the GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated or its value reduced.

2. Place the decoupling capacitor as close as possible to the device's IN and GND terminals. It is important to minimize the loop area created by the connections between the bypass capacitor, the IN terminal, and the GND terminal of the device.

3. Place all external components, including R_{ILIM}, C_{SLEW}, R_{IMON}, and resistors for UVLO and OVP, close to their connection pins. Connect the components to the SGND with the shortest trace length to reduce parasitic effects.

4. Keep the connections between the R_{ILIM} and R_{IMON} components to the device short to reduce parasitic effects on the current limit and ensure current monitoring accuracy. These traces should not be coupled to any switching signals on the board.

5. Connect the SGND plane to the PGND (main power ground) at a single point near the input capacitor's negative terminal.

6. Protection devices such as TVS, snubbers, capacitors, or diodes, should be placed in close proximity to the device they intend to protect. Their traces should be short to minimize parasitic inductance. For example, positioning a Schottky diode across the output can absorb negative voltage transients.

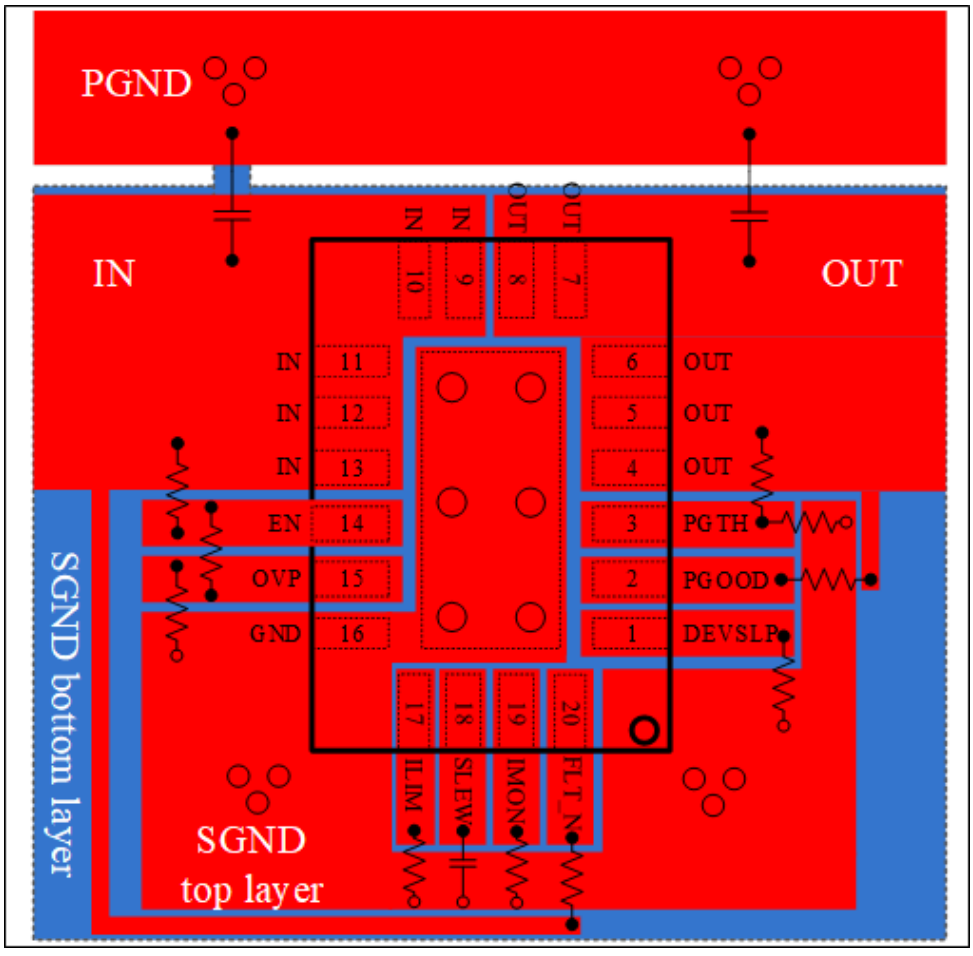
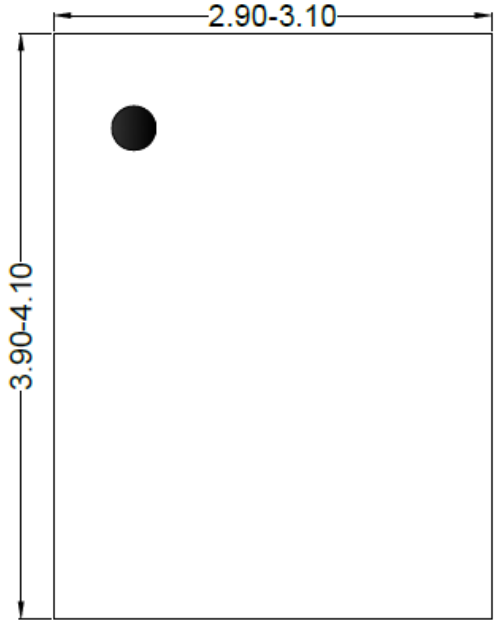
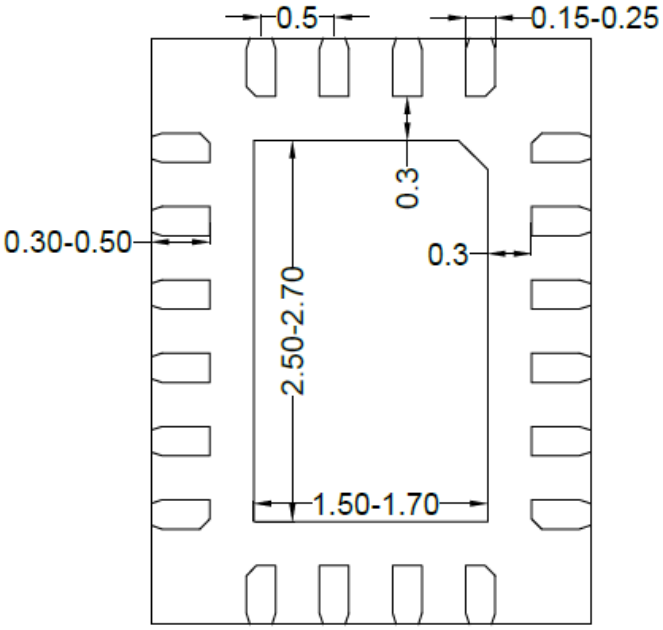


Figure 6. PCB Layout Suggestion

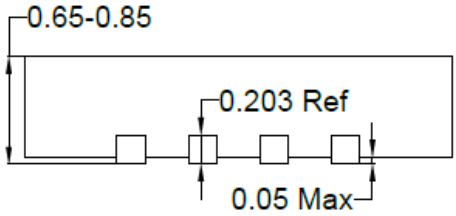
QFN3×4-20 Package Outline Drawing



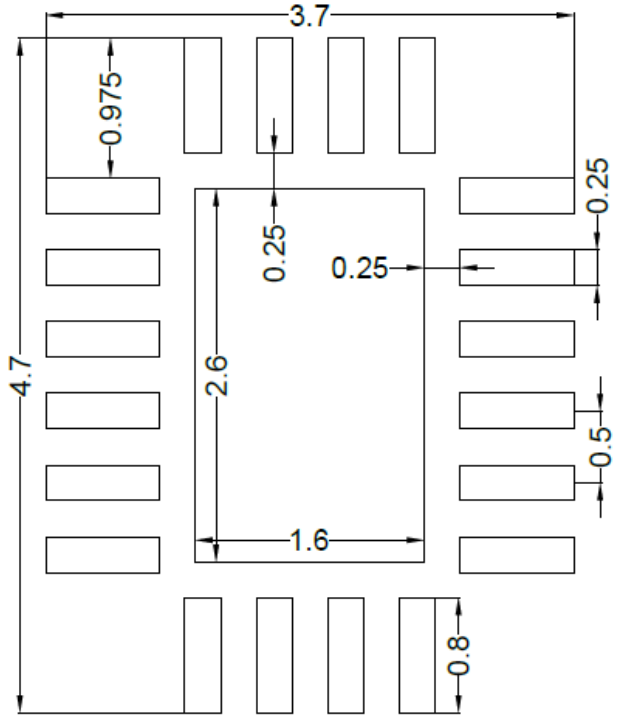
Top View



Bottom View



Side View

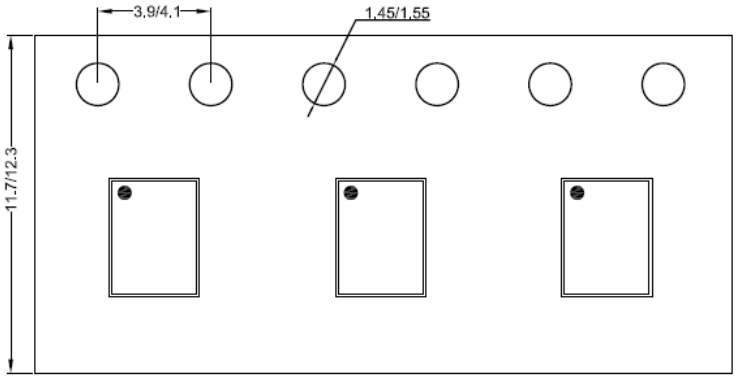


Recommended PCB Layout
(Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

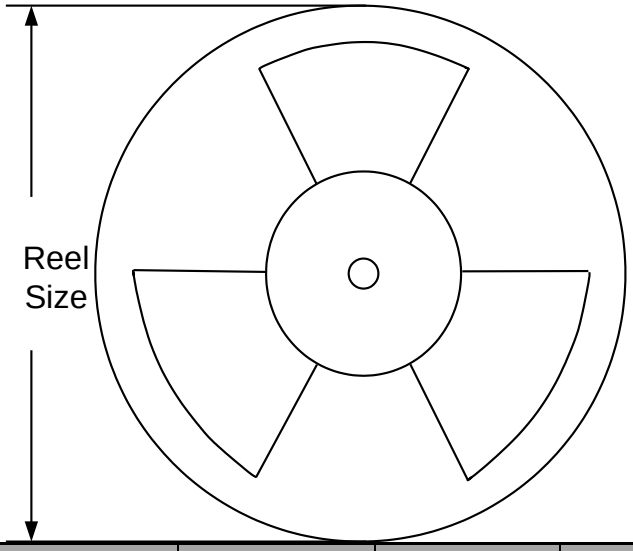
Tape and Reel Information

Tape Dimensions and Pin1 Orientation



Direction of Feed ⟶

Reel Dimensions



Package Type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.18, 2024	Revision 1.0	Initial Release

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