# USB Type-C PD and PWM Buck-Boost Controller with AnyPower™ and PD Safe® Features

## General Description

The RT7860 is a USB Type-C Power Delivery (USBC PD) and PWM buck-boost controller with highly integrated functions and flexibility for USB PD provider applications. The IC has an embedded ARM Cortex™-M0 MCU, which handles various functions of communication protocol, smart control of the PWM converter, firmware-based protections, and customized functions. The IC features hardware-based protections, such as inductor peak current limit, VBUS overvoltage protection (VBUS OVP), VIN undervoltage protection (VIN UVP), VIN overvoltage protection (VIN OVP), VO undervoltage protection (VO UVP), and VCONN current-limit protection, so that the protections have faster responses and can still function even when the MCU is not activated. The RT7860 can offer an excellent USB PD solution for a USB-PD Provider application with few external components and simple PCB layout.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

## Ordering Information

RT7860□-□

- Packing
  A: Standard
- Package Type
  N: WQFN-48L 6x6 (W-Type)
  (Exposed Pad-Option 1)

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

## Applications

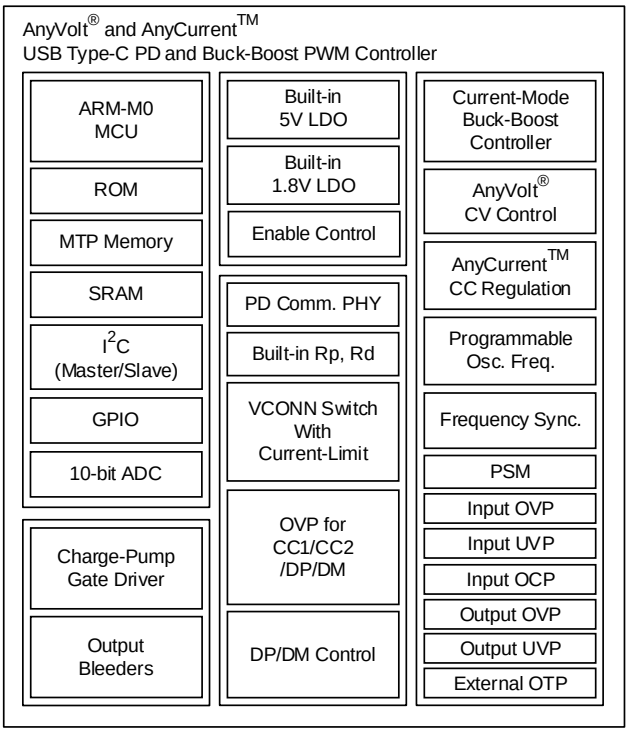
- USB Type-C Power Delivery Car Charger

## Features

- **Support USB Type-C Power Delivery (PD) Provider**
- **Type-C, USB PD and Communication Protocols**
  - **Compliant with USB PD 3.1 Specification, USB Type-C Cable and Connector Specification 2.1**
  - **VCONN Output 100mW**
  - **Support Other Proprietary Communication Protocols through Internal MCU, DP and DM Pins**
- **Integrated PWM Buck-Boost Controller (Support Up to 65W)**
  - **Wide Input Voltage Range: 4.5V to 30V**
  - **Wide Output Voltage Range: 3.3V to 21V**
  - **Peak-Current Mode PWM Operation**
  - **Internal Compensation for CV, CC**
  - **Programmable PWM Switching Frequency (200kHz to 600kHz)**
  - **Pulse-Skipping Mode for Light-Load Efficiency; Selectable Forced CCM Operation**
- **AnyPower™ for Constant Voltage Output and Constant Current Output**
- **PD Safe®**
  - **Adjustable Converter Input Overcurrent Limit (INOC)**
  - **Fast Response VIN OVP/UVP Detection**
  - **Programmable VBUS OVP and VO UVP**
  - **Fast Response OVP for CC1/2 and D+/D-**
  - **Adjustable External OTP/Internal OTP**
  - **CC1/2 Output Current Limit**
  - **CC1/2, D+/D- 25V Tolerant**
- **Cable Voltage Drop Compensation for VBUS**
- **Switching Frequency Synchronization for Better EMI**
- **Adjustable Gate Drive Current for Better EMI**
- **Firmware-based Functions**
  - **VIN De-Rating and Power Sharing**
- **Master and Slave I²C Interfaces, LED Drivers, GPIOs**
- **Built-in Output Bleeders for Quick VBUS Discharge**

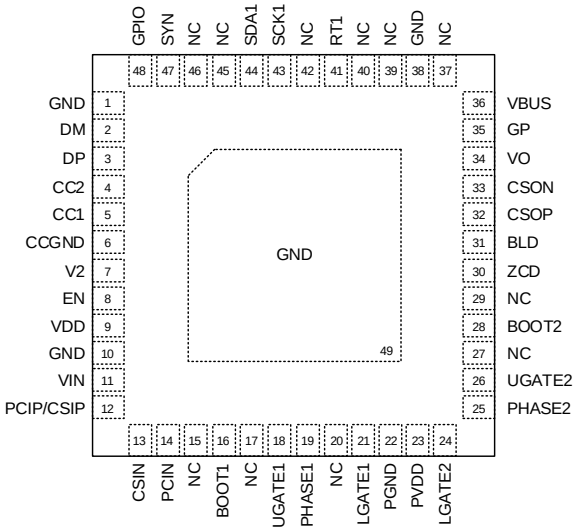
- **EN Control for Power Saving**
- **Built-in Charge Pump for Driving Cost-Effective N-MOSFETs**
- **Built-in Internal LDO**
- **Online Firmware Update via Slave I²C Interface or CC1/2 Interface**
- **Available in WQFN-48L 6x6 Package**

## Simplified Functional Block Diagram




## Pin Configuration

(TOP VIEW)

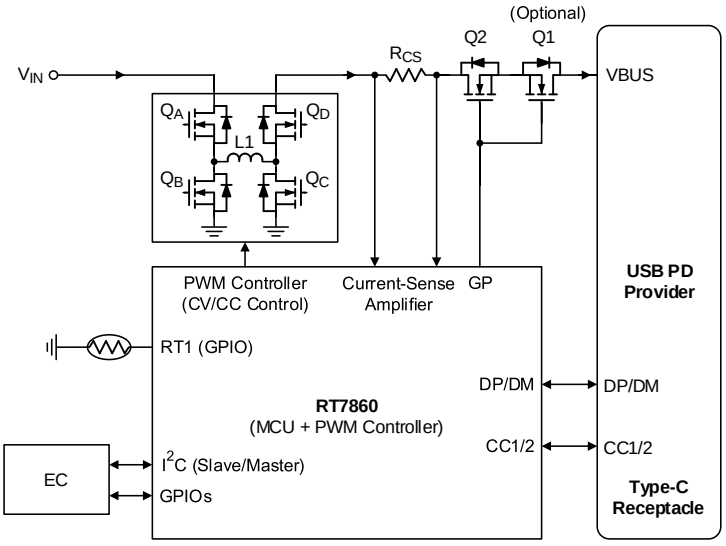



WQFN-48L 6x6

## Marking Information


RT7860N: Product Code
YMDNN: Date Code

## Simplified Application Circuit

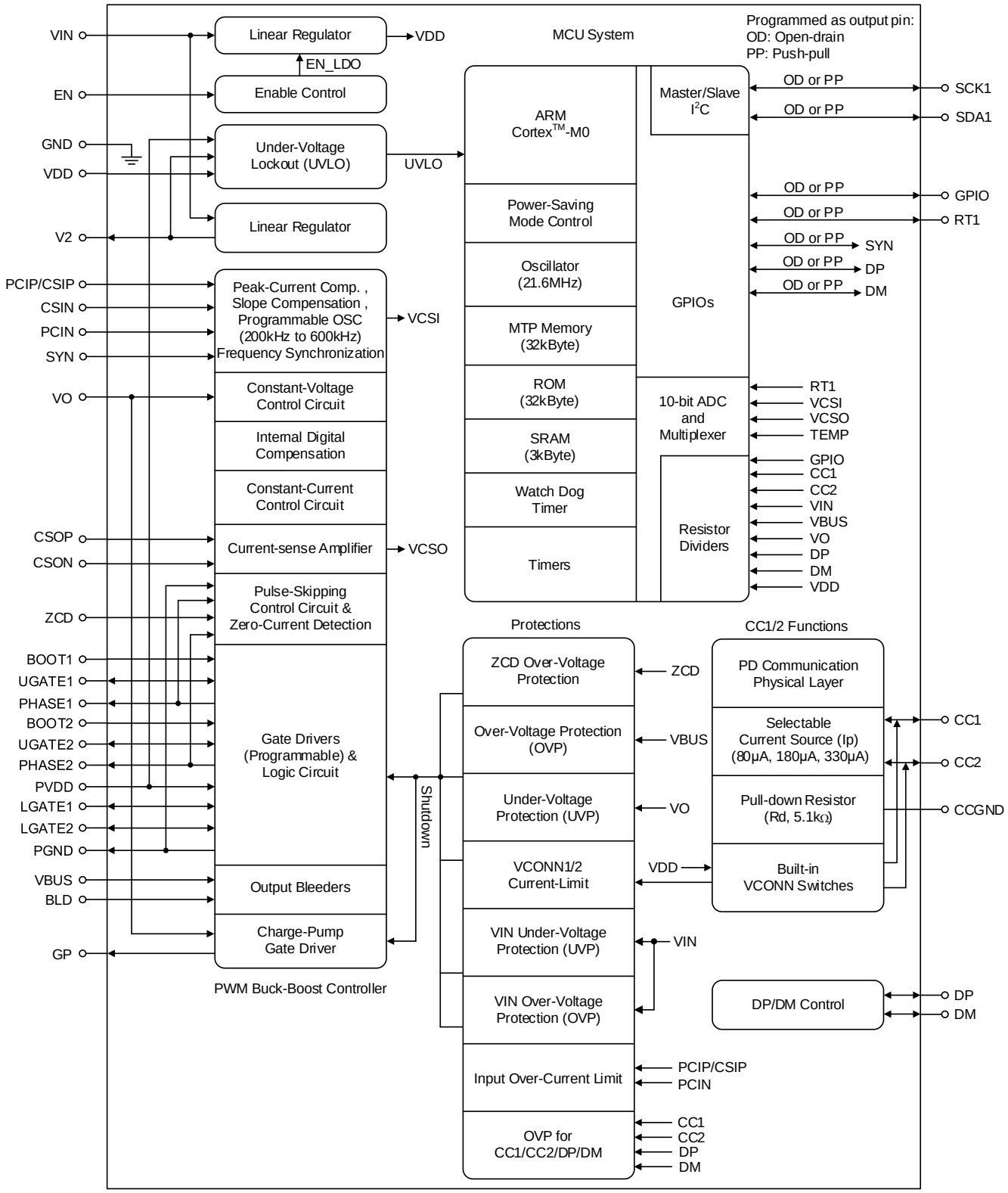


## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1, 10, 38 | GND | Analog ground. |
| 2 | DM | Input/Output pin of built-in DPDM interface for BC1.2 and proprietary protocols. Connect this pin to D- pin of a USB connector. This pin can be set as an open-drain or push-pull GPIO pin. |
| 3 | DP | Input/Output pin of built-in DPDM interface for BC1.2 and proprietary protocols. Connect this pin to D+ pin of a USB connector. This pin can be set as an open-drain or push-pull GPIO pin. |
| 4 | CC2 | Type-C connector Configuration Channel (CC) 2. Generally, this input/output pin is connected to USB Type-C connector CC2 terminal. |
| 5 | CC1 | Type-C connector Configuration Channel (CC) 1. Generally, this input/output pin is connected to USB Type-C connector CC1 terminal. |
| 6 | CCGND | Analog ground. |
| 7 | V2 | Internal 1.8V linear regulator output to supply power for internal circuitry. An MLCC (1μF typ. or greater) must be connected from this pin to ground. |
| 8 | EN | Enable control input with internal pull high source. Keep floating for normal operation. A logic-low voltage to disable the IC for power saving. |
| 9 | VDD | Output pin of the VIN-to-VDD linear regulator. An external MLCC (at least 4.7μF, 0805/X5R/25V) and a 5.6V zener diode (tolerance 5.6V±2%) must be connected from this pin to GND pin. |
| 11 | VIN | Input voltage to the converter and the IC. An aluminum hybrid polymer capacitor (at least 68μF) must be connected from converter VIN to ground. |
| 12 | PCIP/CSIP | Positive peak-current signal input pin and positive average-current signal input pin. |
| 13 | CSIN | Negative average-current signal input pin. |
| 14 | PCIN | Negative peak-current signal input pin. |
| 15, 17, 20, 27, 29, 37, 39, 40, 42, 45, 46 | NC | No internal connection. |
| 16 | BOOT1 | Bootstrap capacitor connection node. Connect a 0.1μF ceramic capacitor from this pin and the PHASE1 pin to power the internal 1st high-side gate driver. |
| 18 | UGATE1 | 1st High-side gate driver output. |
| 19 | PHASE1 | Negative power-rail pin of the 1st high-side gate driver. |
| 21 | LGATE1 | 1st Low-side gate driver output. |
| 22 | PGND | Ground of the low-side gate drivers and one input pin of zero-current detection at the MOSFET controlled by LGATE1. Connect this pin to the source of the MOSFET. |
| 23 | PVDD | Bias voltage (5V typ.) supply for the low-side gate drivers. It is recommended to connect an external MLCC (1μF) from this pin to PGND pin. |
| 24 | LGATE2 | 2nd Low-side gate driver output. |
| 25 | PHASE2 | Negative power-rail pin of the 2nd high-side gate driver. |
| 26 | UGATE2 | 2nd High-side gate driver output. |
| 28 | BOOT2 | Bootstrap capacitor connection node. Connect a 0.1μF ceramic capacitor from this pin and the PHASE2 pin to power the internal 2nd high-side gate driver. |

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 30 | ZCD | One input pin of zero-current detection (at the MOSFET controlled by UGATE2) and Output overvoltage protection input pin. |
| 31 | BLD | Bleeder connection node. An output bleeder, comprising a pull-low NMOS, is built in to provide another path to discharge the output capacitor of the PWM converter. Connect this pin to the converter output through an external resistor. |
| 32 | CSOP | Positive input of a current-sense amplifier to sense the output current for constant current regulation and also through an ADC to the MCU. Connect this pin to the positive terminal of output current-sense resistor via an RC filter. |
| 33 | CSON | Negative input of a current-sense amplifier for output constant-current regulation and output current detection. Connect this pin to the negative terminal of output current-sense resistor via an RC filter. |
| 34 | VO | Input of feedback voltage from converter output. The voltage is monitored for output undervoltage protection. |
| 35 | GP | Charge-pump gate diver output. It drives N-channel power MOSFET(s) to turn on/off the output power path. |
| 36 | VBUS | USB-C VBUS voltage input. The voltage at this pin is monitored for USB-C VBUS overvoltage protection with an 8-bit programmable threshold voltage. |
| 41 | RT1 | Open-drain/push-pull GPIO, analog input or external over-temperature protection (EOTP) input pin. Connect an NTC from this pin to GND pin for the EOTP. |
| 43 | SCK1 | Open-drain clock signal input/output pin of the Slave/Master $I^2C$ interface. This pin can be set as an open-drain or push-pull GPIO pin. |
| 44 | SDA1 | Open-drain data signal input/output pin of the Slave/Master $I^2C$ interface. This pin can be set as an open-drain or push-pull GPIO pin. |
| 47 | SYN | Switching frequency synchronization in two port application. |
| 48 | GPIO | General-purpose input/output. |
| 49 (Exposed Pad) | GND | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |

## Functional Block Diagram



## Operation

The RT7860 is a versatile USB Type-C Power Delivery (USB-C PD) and PWM Buck-Boost controller designed especially for applications as Providers. It is a highly integrated solution, comprising four main functional blocks: MCU System, PWM Buck-Boost Controller, Protections and CC1/2 Functions as depicted in the "Functional Block Diagram".

The MCU System embeds an ARM Cortex™-M0 MCU, a multi-time programming (MTP) memory, a ROM, an SRAM, a 10-bit ADC (analog to digital converter), an $I^2C$ interface (slave and master) and GPIO (general purpose input or output) pins. The MCU System is programmed to perform power controls, customized functions, as a policy engine and a device policy manager. This MCU reports the operating status of PD operation, such as present input/output voltage, output current and external temperature to an EC (embedded controller) or AP (application processor) and receives commands from the EC/AP, as a system policy manager, via the slave $I^2C$ interface. The GPIO pins can be used to control high-speed multiplexers or other customized functions.

The "PWM Buck-Boost controller" consists of an AnyVolt® constant-voltage (CV) control circuit (9.93mV/step, typ.), an AnyCurrent™ constant-current (CC) control circuit, an output current-sense amplifier (7.8mA to 12.5mA /step, depending on the current-sense resistor), built-in gate drivers, one charge-pump gate driver and output bleeders (at BLD and VBUS pins). Generally, either the CV or the CC control circuit regulates the output voltage or current through peak-current mode PWM operation. Diode emulation function and pulse-skipping mode (PSM) are built in to improve power efficiency at light loads. The output current-sense amplifier (OCS-AMP) allows current-sense resistors as low as 5mΩ to 15mΩ for reducing power loss. Moreover the charge-pump driver adopts N-channel MOSFETs for on/off control of output power-path, instead of P-channel MOSFETs having higher cost. In operation the output bleeders at BLD and VBUS pins can be turned on to discharge output voltage (VBUS) during the VBUS negative transition, in the hard reset process, or after the removal of the USB-C connector.

The PD Safe® power delivery operation consists of overvoltage protection (OVP) at the VBUS pin, undervoltage protection at the VO pin, output CC regulation and VCONN1/2 output current-limit function. With the PD Safe® feature, trip levels of the OVP and UVP can be set dynamically for each output voltage target. The CC regulation level is also adaptively programmed according to the current level in full load.

The "CC1/2 Functions" block consists of the physical layer, three selectable levels of the pull-up current sources Ip (instead of resistors Rp), a controllable pull-down resistor Rd and programmable $V_{CONN}$ power-path switches.

### Undervoltage Lockout (UVLO)

The RT7860 UVLO function continuously monitors bias voltages at the VDD and V2 pins. When both of the supply voltages ($V_{DD}$ and $V_{V2}$) rise above the respective rising UVLO thresholds, the internal UVLO signals will go low to activate the MCU. In addition, the IC also monitors the bias voltage at the PVDD pin for UVLO function. Only when all of the UVLO signals go low, or the PWM Buck controller will not be activated; meanwhile the MCU or PWM controllers will be kept in the "Undervoltage Lockout" state to prevent any undesirable operation.

### Pulse-Skipping Mode (PSM) with Diode Emulation

When a switch-mode converter operates in light load condition, most power loss is caused by switching losses. To reduce switching loss in light load condition, the switching frequency needs to be reduced by entering the pulse-skipping mode (PSM) and the discontinuous conduction mode (DCM). In this operation, an internal compensation voltage $V_{COMP}$ is compared by a PSM comparator, which has a programmable PSM threshold.

When the internal compensation voltage $V_{COMP}$ is above the PSM threshold, the converter works in normal fixed-frequency PWM mode. As long as the $V_{COMP}$ drops below the PSM threshold, the converter will enter the pulse-skipping mode to reduce switching frequency and thus diminish switching losses. The PSM threshold also defines the minimum inductor peak current in PSM

operation. Setting a larger PSM threshold will give a higher minimum peak current which in turn gives a lower switching frequency at light load for better light load efficiency at the cost of increased output voltage ripple. Conversely, a lower PSM threshold gives lower peak current and lower PSM ripple at the cost of worse light load efficiency.

A Diode Emulation Mode (DEM) is also a necessary function to avoid delivering energy from converter output to converter input during dynamic output voltage control. The DEM function is equipped with two zero-current detection (ZCD) circuits for the low-side and high-side MOSFETs respectively controlled by the LGATE1 and UGATE2 pins: The Source-to-Drain voltage ($V_{SDB}$, detected via PGND and PHASE1 pins) of the low-side MOSFET is compared with a zero-current threshold ($V_{TH\_ZCDB}$). When the $V_{SDB}$ drops below the $V_{TH\_ZCDB}$ voltage, the RT7860 turns off the low-side MOSFET thereby avoiding reverse inductor current. In DEM operation, the behavior of the low-side MOSFET resembles a diode. The second ZCD circuit compares the Source-to-Drain voltage ($V_{SDD}$, detected via PHASE2 and ZCD pins) of the high-side MOSFET with a zero-current threshold ($V_{TH\_ZCDD}$) to achieve the DEM function.

### Cable Voltage Drop Compensation (CDC)

In a power delivery system with both a Provider and a Consumer, the Provider with the RT7860 AnyVolt® feature can slightly adjust its CV output voltage to compensate voltage drop across the USB cable. A PD controller of the Consumer can request higher VBUS voltage from the Provider through PD communication to achieve an accurate application voltage.

There is another method to implement the CDC function without PD communication. The RT7860 can use the ADC to detect the output current-sense voltage ($V_{CSO}$) between CSOP and CSON pins and adaptively add a proper output voltage offset ($V_{CDC}$) to compensate the cable voltage drop. The output voltage offset ($V_{CDC}$) is gradually added by adjusting the CV regulated output voltage ($V_{REG\_VO}$) and is approximately proportional to the converter output current ($I_{OUT}$). $V_{CDC}$ is approximately determined by the following equation:

$V_{CDC} = I_{OUT} \times R_{CABLE}$

where:

$R_{CABLE}$ is a preset value of parasitic resistance of USB cable.

### VBUS Overvoltage Protection (VBUS OVP)

In Figure 1, the VBUS OVP function is a hardware-based protection which monitors the voltage at the VBUS pin via a built-in resistor-divider. When the VBUS voltage exceeds its OVP threshold, the output of the OVP comparator goes high and starts the debounce time counting. At the end of the debounce time counting, the signal VBUS OVP goes high to turn off the PWM controller. The OVP trip voltage is programmable from 3.3V to 24V (8-bit, 100mV/step typ.) and its debounce time is also selectable to meet various application requirements.

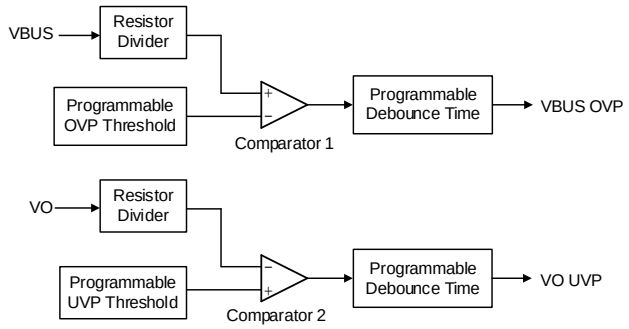



Figure 1. Functional diagram of VBUS OVP and VO UVP

### VO Undervoltage Protection (VO UVP)

In Figure 1, the VO UVP function is a hardware-based protection which monitors the voltage at the VO pin via a built-in resistor-divider. When the VO voltage falls below its UVP threshold, the output of the UVP comparator goes high and starts the debounce time counting. At end of the debounce time, the signal VO UVP goes high to turn off PWM controller. The UVP trip voltage is programmable from 3V to 20V (8-bit, 100mV/step typ.) and its debounce time is also selectable to avoid false triggering and to meet various application requirements.

### AnyCurrent™ Constant-Current (CC) Regulation

It is noted that a robust system is very important in USB PD operations, the AnyCurrent™ CC regulation allows setting the most suitable CC level for a negotiated PD system.

The RT7860 integrates a current-sense amplifier to sense output current for CC regulation and also through an ADC to the MCU for the output current to be recorded. The amplifier accurately sense the current-sense voltage (i.e., $V_{CS}$ = output current x current-sense resistor) between the CSOP and CSON pins. The recommended current-sense voltage range for CC regulation is from 5mV to 35mV which is programmed by an internal 10-bit DAC (digital-to-analog converter) with 0.0625mV/step resolution.

### Power-Path Gate Driver for Driving N-Channel MOSFETs

The RT7860 integrates a power-path gate driver to control external output blocking MOSFETs between the output of the PWM converter and the USB-C VBUS terminal. A built-in charge pump is included to supply the gate driver to turn on the external N-channel power MOSFETs, which allow power systems to be more cost-effective, compared to the counterpart, P-channel power MOSFETs.

### Online Firmware Update via Slave I²C or CC1/CC2 Interface

The embedded MTP memory allows the RT7860's firmware to be updated by an EC (Embedded Controller) or AP (Application Processor) through the I²C slave interface. The RT7860 provides some firmware-programmable design features, which greatly eases the design efforts during product development stage. End users are also allowed to update the firmware through CC1/CC2.

## Absolute Maximum Ratings (Note 1)

- V2 to GND ---------- –0.3V to 2.5V
- VDD, PVDD to GND ---------- –0.3V to 6.5V
- VBUS, CSOP, CSON, VO, BLD, ZCD to GND ---------- –0.3V to 25V
- CSOP to CSON Voltage ($V_{CSOP-CSON}$) ---------- –5V to 5V
- GP to GND ---------- –0.3V to 33V
- VIN, PCIN, PCIP/CSIP, CSIN to GND (DC) ---------- –0.3V to 32V
  (< 0.4s) ---------- –0.3V to 36V
- ZCD to CSOP ($V_{ZCD-CSOP}$) and
  ZCD to CSON Voltage ($V_{ZCD-CSON}$) ---------- –0.3V to 6.5V
- PCIP/CSIP to CSIN Voltage ($V_{PCIP/CSIP-CSIN}$) ---------- –5V to 5V
- VIN to PCIP/CSIP ($V_{VIN-PCIP/CSIP}$) and
  VIN to PCIN Voltage ($V_{VIN-PCIN}$) and
  VIN to CSIN Voltage ($V_{VIN-CSIN}$) ---------- –0.3V to 6.5V
- PCIP/CSIP to PCIN Voltage ($V_{PCIP/CSIP-PCIN}$) ---------- –5V to 5V
- EN to GND ---------- –0.3V to 6.5V
- $I^2C$ Pins (SCK1, SDA1) to GND ---------- –0.3V to 6.5V
- GPIO Pins (SYN, GPIO, RT1) to GND ---------- –0.3V to 6.5V
- DP, DM to GND ---------- –0.3V to 25V
- CC1, CC2 to GND ---------- –0.3V to 25V
- BOOT1/2 to PHASE1/2 ($V_{BOOT-PHASE}$) ---------- –0.3V to 6.5V
- UGATE1/2 to PHASE1/2 ---------- –0.3V to $V_{BOOT-PHASE}$ + 0.3V
- PHASE1 to GND (DC) ---------- –0.3V to 30V
  (< 20ns) ---------- –5V to 36V
- PHASE2 to GND (DC) ---------- –0.3V to 25V
  (< 20ns) ---------- –5V to 30V
- LGATE1/2 to PGND ---------- –0.3V to $V_{PVDD}$ + 0.3V
- PGND, CCGND to GND ---------- –0.3V to 0.3V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  WQFN-48L 6x6 ---------- 3.73W
- Package Thermal Resistance (Note 2)
  WQFN-48L 6x6, $\theta_{JA}$ ---------- 26.8°C/W
  WQFN-48L 6x6, $\theta_{JC}$ ---------- 1.3°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

## Recommended Operating Conditions (Note 4)

- PWM Converter Input Voltage, $V_{IN}$ ---------- 4.5V to 30V
- PWM Converter Output Voltage, $V_{OUT}$ ---------- 3V to 22V
- VDD Output Voltage/PVDD Supply Voltage ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C
- Minimum MTP Memory Write/Erase Cycles ---------- 100cycles at 25°C

## Electrical Characteristics

($V_{DD}$ = $V_{PVDD}$ = $V_{VCONN}$ = 5V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VDD and V2 Linear Regulators (VDD LDO and V2 LDO), Undervoltage Lockout (UVLO) and Enable Control** | | | | | | |
| VDD Output Voltage (5.0V Normal/4.3V DGM) | $V_{REG\_VDD}$ | In normal mode, $V_{IN}$ = 12V, Io = 0mA, $C_{VDD}$ = 4.7μF | 4.7 | 5 | 5.3 | V |
| | | In deep-green mode, $V_{IN}$ = 12V, Io = 0mA, $C_{VDD}$ = 4.7μF | 3.9 | 4.2 | 4.5 | |
| VDD Load Regulation Drop Voltage (5.0V Normal) | $V_{DROP\_VDD12}$ | $V_{IN}$ = 12V, Io = 100mA, $C_{VDD}$ = 4.7μF | -- | 0.3 | -- | V |
| | $V_{DROP\_VDD5}$ | $V_{IN}$ = 5V, Io = 100mA, $C_{VDD}$ = 4.7μF | -- | 0.3 | -- | V |
| VDD Short Current | $I_{SC\_VDD}$ | $V_{IN}$ = 12V, $V_{DD}$ = 3V short to GND | -- | 150 | -- | mA |
| VIN Normal Operating Current | $I_{OP\_VIN}$ | $V_{IN}$ = 12V, PWM = MCU = on, digital output pins = open | -- | 10 | -- | mA |
| VIN Operating Current in Deep Green-Mode (DGM) | $I_{DGM\_VIN}$ | $V_{IN}$ = 12V, PWM = off, MCU = off, no load current, CC1/CC2 RX detection | -- | 0.5 | -- | mA |
| VIN Operating Current in Deep Green-Mode (DGM_LQ) | $I_{DGM\_LQ\_VIN}$ | $V_{IN}$ = 12V, PWM = MCU = off, CC1/CC2 falling detection only | -- | 120 | -- | μA |
| VIN Operating Current in EN Reset-Mode | $I_{RST\_VIN}$ | $V_{IN}$ = 12V, EN = 0, PWM = MCU = off, digital output pins = open, VDD off | -- | 10 | 50 | μA |
| V2 Output Voltage | $V_{REGV2}$ | In normal mode IV2 = 20mA load, CV2 = 1μF | 1.62 | 1.8 | 1.98 | V |
| V2 Short-Circuit Current | $I_{SC\_V2}$ | $V_{IN}$ =12V, VDD = 5V V2 short to GND | -- | 50 | -- | mA |
| VDD POR Voltage Threshold | | $V_{DD}$ rising | 3.8 | 4 | 4.2 | V |
| VDD UVLO Voltage Hysteresis | | $V_{DD}$ falling | -- | 0.225 | -- | V |
| PVDD POR Threshold | | $V_{PVDD}$ rising | 3.8 | 4 | 4.2 | V |
| PVDD UVLO Hysteresis | | $V_{PVDD}$ falling | -- | 0.2 | -- | V |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PVDD Input Current in PWM Shut Down | | $V_{IN}$ =12V, $V_{DD}$ = 5V, $V_{PVDD}$ = 5V, PVDD_EN = off, PWM = off | -- | -- | 3 | μA |
| EN Internal Pull-High Voltage | | $V_{IN}$ = 12V, $V_{DD}$ = 5V, EN open | 3 | -- | 5 | V |
| EN Internal Pull-High Resistor | | $V_{IN}$ = 12V, $V_{DD}$ = 5V, EN = 0 | -- | 1200 | -- | kΩ |
| EN Threshold Voltage | $V_{IH\_EN}$ | $V_{IN}$ = 12V, $V_{DD}$ = 5V | 1.5 | -- | VDD | V |
| | $V_{IL\_EN}$ | $V_{IN}$ = 12V, $V_{DD}$ = 5V | 0 | -- | 0.4 | |
| **PWM Controller – Programmable Oscillator, Maximum On-Time,** | | | | | | |
| PWM Frequency Range | $f_{PWM}$ | Programmable | 200 | -- | 600 | kHz |
| PWM Frequency Accuracy | | $f_{PWM}$ = 300kHz/400kHz | –6 | -- | 6 | % |
| **MCU Section** | | | | | | |
| MCU Clock Frequency | $f_{MCU}$ | | 19.4 | 21.6 | 23.8 | MHz |
| OSC 80K Frequency in Deep Green-Mode | $f_{80K}$ | | -- | 80 | -- | kHz |
| **PWM Controller – Constant-Voltage (CV) Control Loop** | | | | | | |
| CV Regulated Voltage Range at VO Pin | $V_{REG\_VO}$ | Programmable (11-bit), 9.93mV/step | 3 | -- | 22 | V |
| CV Regulated Voltage Accuracy at VO Pin (CVDAC_11bit) | | $V_{OUT}$ = 3.3V/5V/9V/12V/15V/20V | –100 | -- | 100 | mV |
| **PWM Controller – Constant-Current (CC) Control Loop and Output** | | | | | | |
| CSON and CSOP Operating Voltage Range | | | 3 | -- | 22 | V |
| CC Regulated Voltage Range between CSOP and CSON Pins (CCDAC_10bit) | $V_{REF\_CC}$ | CSAgain = 40, programmable (10-bit), 0.0625mV/step (typ.), $V_{CSON}$ and $V_{CSOP}$ > 3V | 5 | -- | 35 | mV |
| CC Regulated Voltage Accuracy between CSOP and CSON Pins | | CSAgain = 40, Nominal $V_{REF\_CC}$ = 5mV/15mV/25mV | –0.5 | -- | 0.5 | mV |
| CSOP/CSON Input Current | | PWM bias = on | -- | -- | 50 | μA |
| | | PWM bias = off | -- | -- | 1 | |
| CSA Detection Voltage Range between CSIP and CSIN Pins | | CSAgain = 40 | 5 | -- | 35 | mV |
| CSIP/CSIN Input Current in VinCSA | | PWM bias = on | -- | -- | 50 | μA |
| | | PWM bias = off | -- | -- | 1 | |
| **PWM Controller – Input Current Comparison, Slope Compensation** | | | | | | |
| Maximum Input Overcurrent (INOC) Voltage Threshold Range | $V_{TH\_CSMAX}$ | Programmable | 30 | -- | 150 | mV |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Maximum Input Overcurrent (INOC) Voltage Threshold Accuracy | | $V_{TH\_CSMAX}$ = 30mV, 120mV | –6 | -- | 6 | mV |
| Voltage Rate Range of Slope Compensation | | Programmable | 0 | -- | 80 | mV/μs |
| PCIP/CSIP Input Current in INOC | | In PSM, $V_{CSIP}$ = 24V | -- | -- | 50 | μA |
| | | PWM bias = off, $V_{CSIP}$ = 24V | -- | -- | 3 | |
| PCIN Input Current | | In PSM, $V_{CSIN}$ = 24V | -- | -- | 30 | μA |
| | | PWM bias = off, $V_{CSIN}$ = 24V | -- | -- | 3 | |
| **PWM Controller – Zero-Current Detection (ZCD)** | | | | | | |
| MOS-D ZCD Voltage Threshold between PHASE2 and ZCD Pins | $V_{TH\_ZCDD}$ | To compare the PHASE2-to-ZCD voltage | -- | 4 | -- | mV |
| MOS-B ZCD Voltage Threshold between PGND and PHASE1 Pins | $V_{TH\_ZCDB}$ | To compare the PGND-to-PHASE1 voltage | -- | 4 | -- | mV |
| ZCD Input Current | | In PSM, $V_{ZCD}$ = 20V | -- | -- | 300 | μA |
| | | PWM bias = off, $V_{ZCD}$ = 20V | -- | -- | 90 | |
| **PWM Controller – Gate Drivers** | | | | | | |
| UGATE1/2 Pull-High Resistance | | Programmable, $V_{BOOT1/2\text{-}PHASE1/2}$ = 5V, $V_{BOOT1/2\text{-}UGATE1/2}$ = 0.1V | -- | 1.7 | -- | Ω |
| | | | -- | 5 | -- | |
| | | | -- | 10 | -- | |
| | | | -- | 20 | -- | |
| UGATE1/2 Pull-Low Resistance | | $V_{UGATE1/2}$-$V_{PHASE1/2}$ = 0.1V | -- | 0.8 | -- | Ω |
| LGATE1/2 Pull-High Resistance | | Programmable, $V_{PVDD}$-$V_{LGATE1/2}$ = 0.1V | -- | 1.7 | -- | Ω |
| | | | -- | 5 | -- | |
| | | | -- | 10 | -- | |
| | | | -- | 20 | -- | |
| LGATE1/2 Pull-Low Resistance | | $V_{LGATE1/2}$ = 0.1V | -- | 0.8 | -- | Ω |
| Dead-Time at LGATE1/2 Falling Edge | | | -- | 40 | -- | ns |
| Dead-Time after UGATE1/2 Falling Edge | | | -- | 40 | -- | ns |
| **System Protections – Overvoltage, Undervoltage, and Overcurrent Protections (OVP, UVP, and OCP)** | | | | | | |
| VIN UVP Voltage Threshold Range | $V_{TH\_VINUV}$ | Programmable, (8-bit), 125mV/step (typ.) | 4 | -- | 27 | V |
| VIN UVP Voltage Threshold Accuracy | | Setting of $V_{TH\_VINUVP}$ = 5V/10V/15V | –5 | -- | 5 | % |
| VIN OVP Voltage Threshold Range | $V_{TH\_VINOV}$ | Programmable, (8-bit), 125mV/step (typ.) | 4 | -- | 30 | V |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VIN OVP Voltage Threshold Accuracy | | Setting of $V_{TH\_VINOVP}$ = 19V/26V | –5 | -- | 5 | % |
| VBUS OVP Voltage Threshold Range | $V_{TH\_VBUSOV}$ | Programmable, (8-bit), 100mV/step (typ.) | 3.3 | -- | 24 | V |
| VBUS OVP Voltage Threshold Accuracy | | Setting of $V_{TH\_VBUSOV}$ = 12V/20V | –5 | -- | 5 | % |
| VBUS OVP Voltage Threshold Accuracy | | Setting of $V_{TH\_VBUSOV}$ = 3.3V/ 5V | –0.3 | -- | 0.3 | V |
| ZCD Pin OVP Voltage Threshold (VO Pin Open, OVP) | $V_{TH\_ZCDOV}$ | | –7 | 125 | 7 | % |
| VO UVP Voltage Threshold Range | $V_{TH\_VOUV}$ | Programmable, (8-bit), 100mV/step (typ.) | 3 | -- | 20 | V |
| VO UVP Voltage Threshold Accuracy | | Setting of $V_{TH\_VOUV}$ = 5V/12V/20V | –5 | -- | 5 | % |
| VO UVP Voltage Threshold Accuracy | | Setting of $V_{TH\_VOUV}$ = 3V | –0.2 | -- | 0.2 | V |
| VO UVP Blanking Time during Start-Up | | (Note 5) | -- | 5 | -- | ms |
| | | | -- | 10 | -- | |
| | | | -- | 20 | -- | |
| | | | -- | 40 | -- | |
| **USB PD Controller – CC1/2 Voltage Detections, BMC Transmitter/Receiver and VCONN Switches** | | | | | | |
| CC1/2 Pull-Up Current Source – 1 | Ip1 | For default USB power | 64 | 80 | 96 | µA |
| CC1/2 Pull-Up Current Source – 2 | Ip2 | For 1.5A and 5V | 165.6 | 180 | 194.4 | µA |
| CC1/2 Pull-Up Current Source – 3 | Ip3 | For 3.0A and 5V | 303.6 | 330 | 356.4 | µA |
| CC1/2 Open-Loop Clamping Voltage for pull-up Source | $V_{CC\_CLAMP}$ | $V_{DD}$ = 5V @ pull-up current 330µA | 2.9 | 3.25 | -- | V |
| CC1/2 Pull-Down Resistor | Rd | $V_{DD}$ = 5V @ pull-up 56kΩ | 4.6 | 5.1 | 5.6 | kΩ |
| Transmitter High-Level Output Voltage Range | | | 1.05 | 1.125 | 1.2 | V |
| Transmitter Low-Level Output Voltage Range | | | 0 | -- | 75 | mV |
| Rising Time of the Transmitter Output Voltage | | From 10% to 90%, CL = 200pF to 600pF | 300 | -- | -- | ns |
| Falling Time of the Transmitter Output Voltage | | From 90% to 10%, CL = 200pF to 600pF | 300 | -- | -- | ns |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Receiver High-Level Input Voltage Range | | | -- | 0.8 | -- | V |
| | | | -- | 0.7 | -- | |
| | | | -- | 0.6 | -- | |
| | | | -- | 0.5 | -- | |
| Receiver Low-Level Input Voltage Range | | | -- | 0.5 | -- | V |
| | | | -- | 0.4 | -- | |
| | | | -- | 0.3 | -- | |
| | | | -- | 0.2 | -- | |
| VCONN On-Resistance of VDD-to-CC1/2 MOSFET | | $V_{DD}$=5V, output current = 20mA | -- | 10 | 15 | Ω |
| VCONN Output Voltage Drop VDD-to-CC1/2 MOSFET | | $V_{DD}$=5V, output current = 20mA | -- | 0.2 | 0.3 | V |
| VCONN Current-Limit Threshold | | CC1/CC2 = GND | -- | 50 | -- | mA |
| CC1/CC2 Short to VBUS Protection | | | 5.7 | 6 | 6.3 | V |
| **DPDM Interfaces in Source Role Operation** | | | | | | |
| On-Resistance of DP-to-DM MOSFET | | | -- | -- | 40 | Ω |
| DP/DM High-Level Output Voltage | $V_{OH\_DPDM}$ | Sourcing current = 2mA | -- | 3.3 | -- | V |
| | | | -- | 1.8 | -- | |
| DP/DM Low-Level Output Voltage | $V_{OL\_DPDM}$ | Sinking current = 2mA | -- | -- | 0.3 | V |
| DP/DM Voltage Falling Threshold for Plug-Out Detection | $V_{REF1\_DPDM}$ | | -- | 0.3 | -- | V |
| | | | -- | 0.4 | -- | |
| | | | -- | 0.5 | -- | |
| | | | -- | 0.6 | -- | |
| Input Voltage Offset Selection VREF2H_DPDM, VREF2L_DPDM | $V_{IN\_LEV}$ | | -- | 0 | -- | V |
| | | | -- | 0.4 | -- | |
| RX Upper Input Voltage Threshold | $V_{REF2H\_DPDM}$ | $V_{IN\_LEV}$ = 0V | -- | 0.8 | -- | V |
| | | | -- | 1.3 | -- | |
| | | | -- | 1.9 | -- | |
| | | | -- | 2.05 | -- | |
| | | $V_{IN\_LEV}$ = 0.4V | -- | 1.2 | -- | |
| | | | -- | 1.7 | -- | |
| | | | -- | 2.3 | -- | |
| | | | -- | 2.45 | -- | |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RX Lower Input Voltage Threshold | $V_{REF2L\_DPDM}$ | $V_{IN\_LEV}$ = 0V | -- | 0.6 | -- | V |
| | | | -- | 1.1 | -- | |
| | | | -- | 1.8 | -- | |
| | | | -- | 1.95 | -- | |
| | | $V_{IN\_LEV}$ = 0.4V | -- | 1 | -- | |
| | | | -- | 1.5 | -- | |
| | | | -- | 2.2 | -- | |
| | | | -- | 2.35 | -- | |
| DP/DM Internal Pull-Low Resistance | $R_{DWN\_DPDM}$ | | 16 | 20 | 24 | kΩ |
| DP/DM Output Voltage for Divider Mode | | | 1.13 | 1.2 | 1.27 | V |
| | | | 1.88 | 2 | 2.12 | |
| | | | 2.57 | 2.7 | 2.84 | |
| | | | 3.14 | 3.3 | 3.47 | |
| Output Resistance DP/DM for Divider Mode 2.0/2.7/3.3 | | | -- | 30 | -- | kΩ |
| Output Resistance DP/DM for Divider Mode 1.2 | | | -- | 100 | -- | kΩ |
| DP/DM Output Voltage-1 for SRC | $V_{SRC1\_DPDM}$ | | -- | 0.6 | -- | V |
| DP/DM Output Voltage-2 for SRC | $V_{SRC2\_DPDM}$ | | -- | 3.3 | -- | V |
| DP/DM Short to VBUS Protection | | | 5.415 | 5.7 | 5.985 | V |
| **Charge-Pump Gate Drivers and Bleeders** | | | | | | |
| GP On-Resistance of Pull-Low MOSFET | | Pull-low NMOS is on, sinking $I_{GP}$ = 10mA, $V_{DD}$ = 5.0V | -- | -- | 200 | Ω |
| Maximum GP Voltage | | $V_{VO}$ = 20V, $R_{GP\text{-}to\text{-}GND}$ = 667kΩ | $V_{VO}$ + 4V | $V_{VO}$ + 4.5V | $V_{VO}$ + 10V | V |
| BLD On-Resistance of Pull-Low MOSFET | | Pull-low NMOS is on, sinking $I_{BLD}$ = 10mA, $V_{DD}$ = 5V | -- | 20 | 40 | Ω |
| BLD Leakage Current | | $V_{BLD}$ = 20V, pull-low NMOS is off $V_{DD}$ = 5V | -- | -- | 1 | μA |
| VBUS Bleeder Resistor | | Pull-low NMOS is on $V_{DD}$ = 5V and $V_{BUS}$ = 23V | -- | 1.2 | -- | kΩ |
| **Digital Input and Output – $I^2C$ Pins (SCK1 and SDA1) and GPIO Pins (SCK1, SDA1, SYN, GPIO and RT1)** | | | | | | |
| $I^2C$/GPIO High-Level Input Voltage Range | $V_{IH}$ | For the pins configured as input pins | 1.5 | -- | -- | V |
| $I^2C$/GPIO Low-Level Input Voltage Range | $V_{IL}$ | For the pins configured as input pins | -- | -- | 0.4 | V |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I^2C$/GPIO High-Level Output Voltage | $V_{OH}$ | Sourcing current = 2mA, for the pins configured as push-pull output pins | VDD - 1.5V | VDD - 0.8V | -- | V |
| $I^2C$/GPIO Low-Level Output Voltage | $V_{OL}$ | Sinking current = 2mA | -- | -- | 0.3 | V |
| $I^2C$/GPIO Leakage Current | | Pin input voltage = 5V | -- | -- | 1 | μA |
| RT1 Current Source | | $V_{RT1}$ < 2.7V | 92 | 100 | 108 | μA |

**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

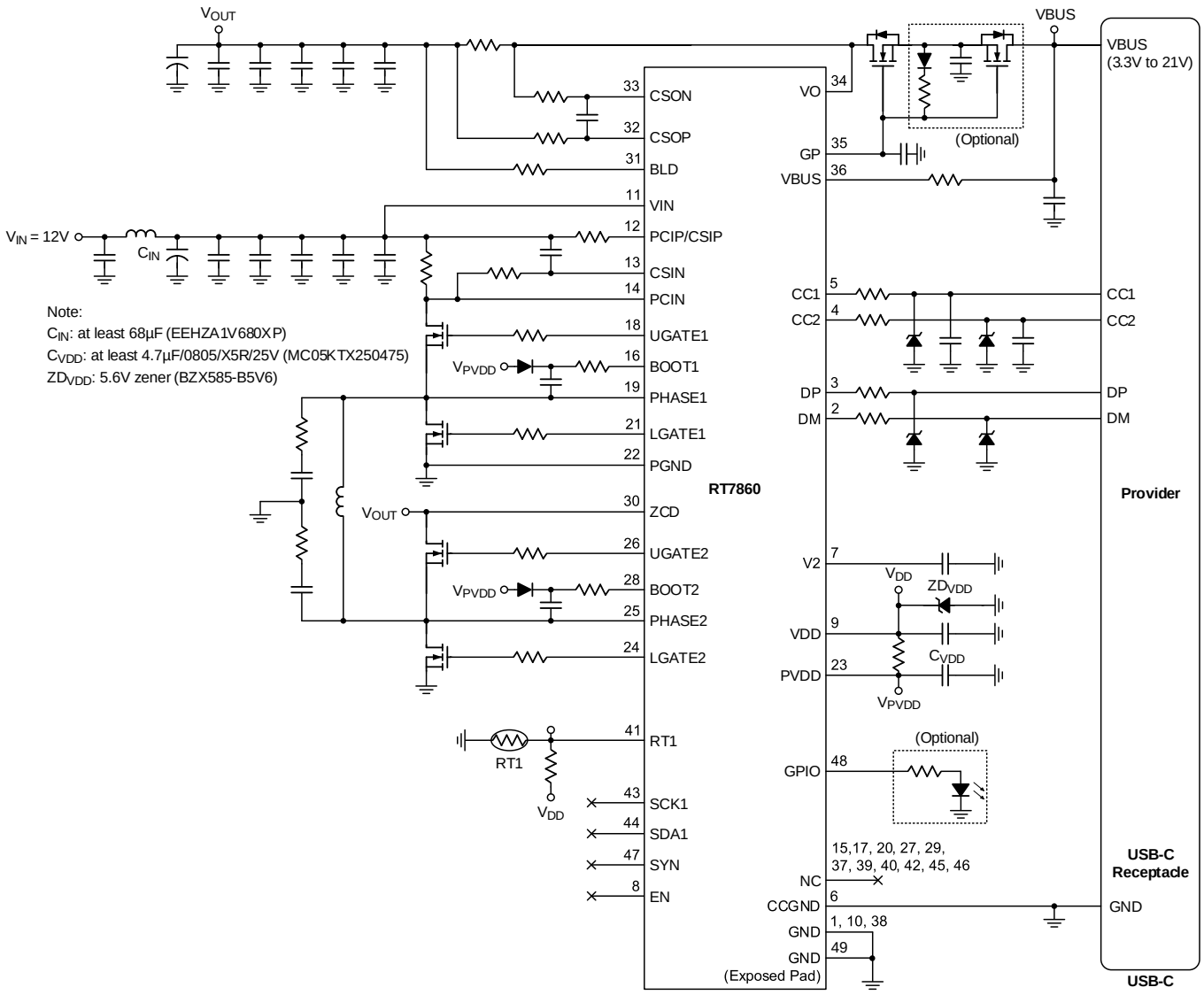
**Note 2.** $\theta_{JA}$ is measured under natural convection (still air) at $T_A$ = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. $\theta_{JC}$ is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precautions are recommended.

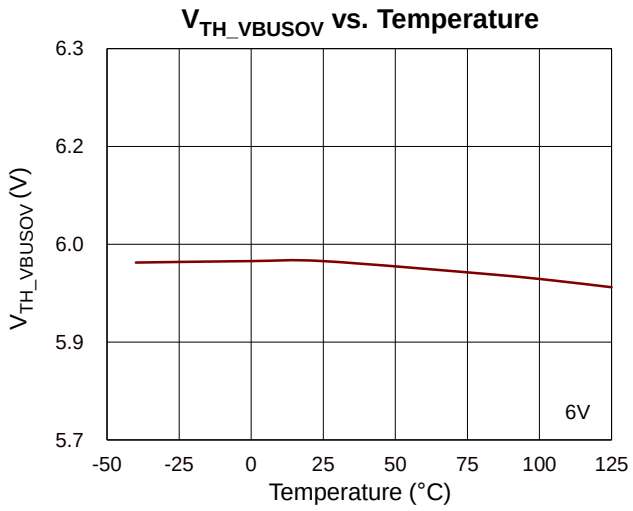
**Note 4.** The device is not guaranteed to function outside its operating conditions.

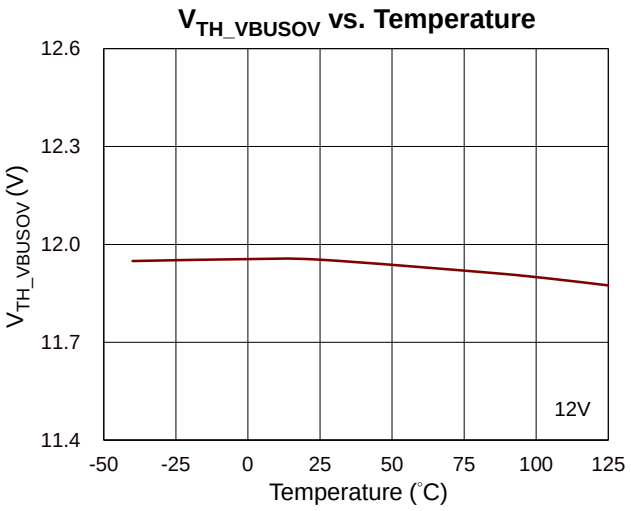
**Note 5.** Guaranteed by design.

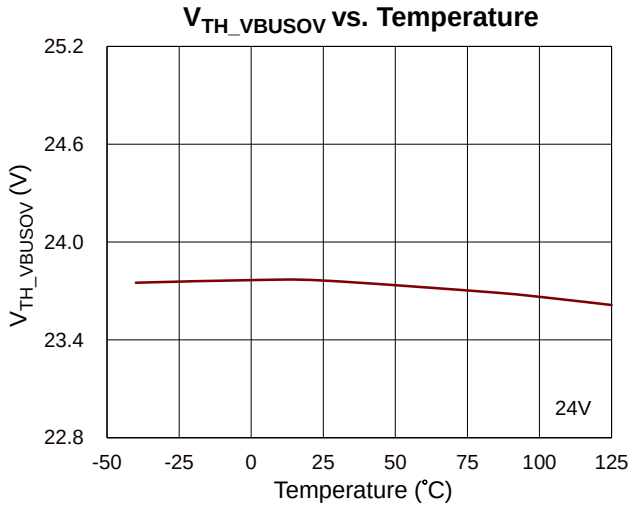
## Typical Application Circuit

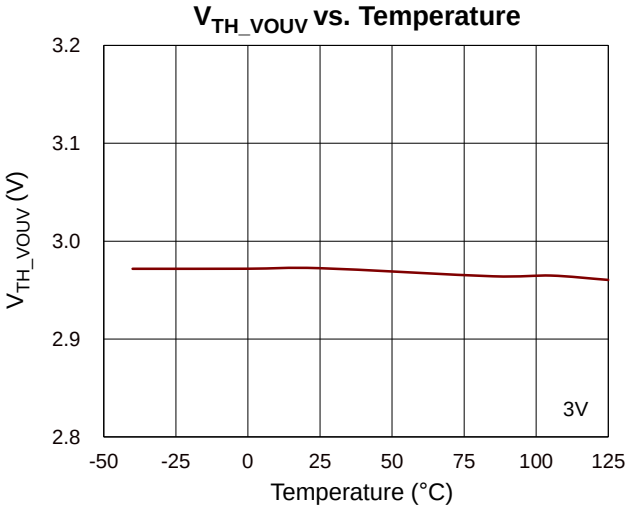


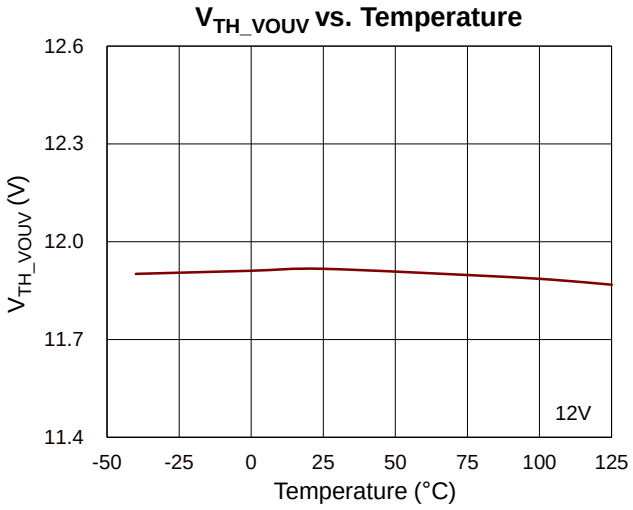
## Typical Operating Characteristics

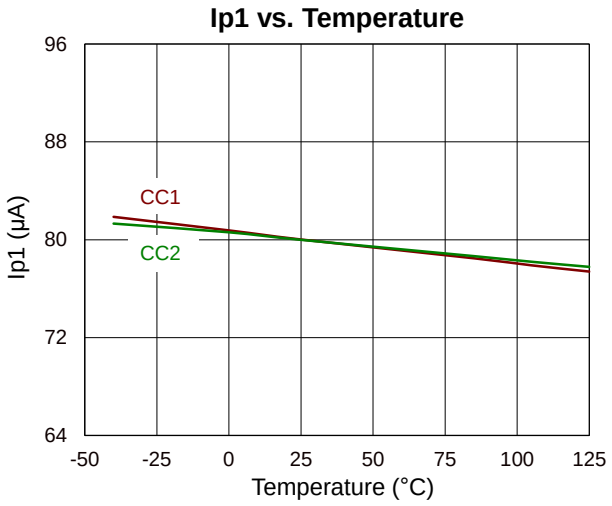


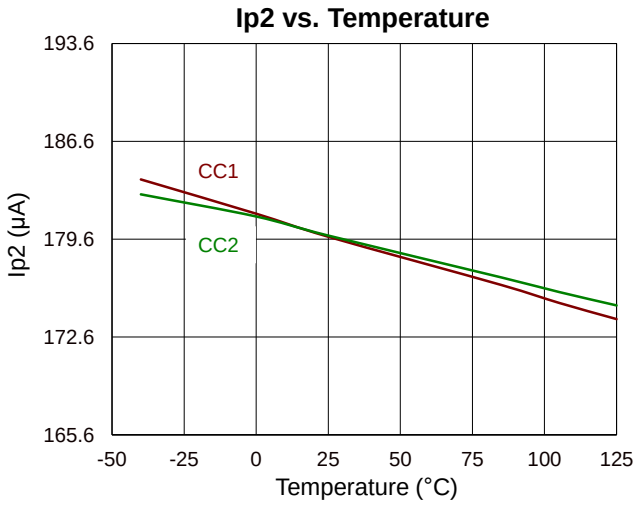



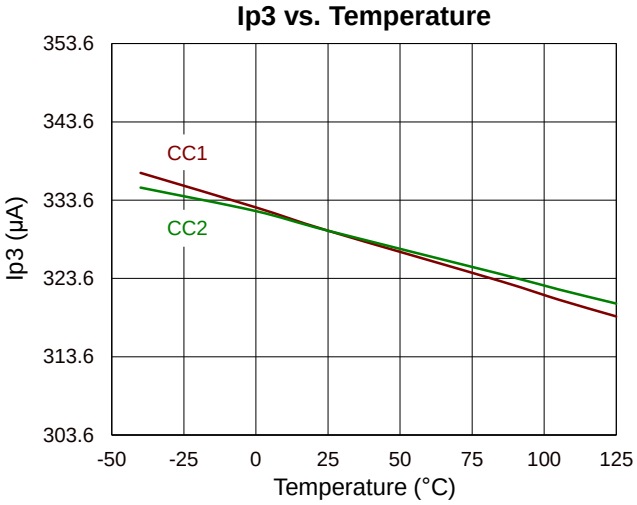



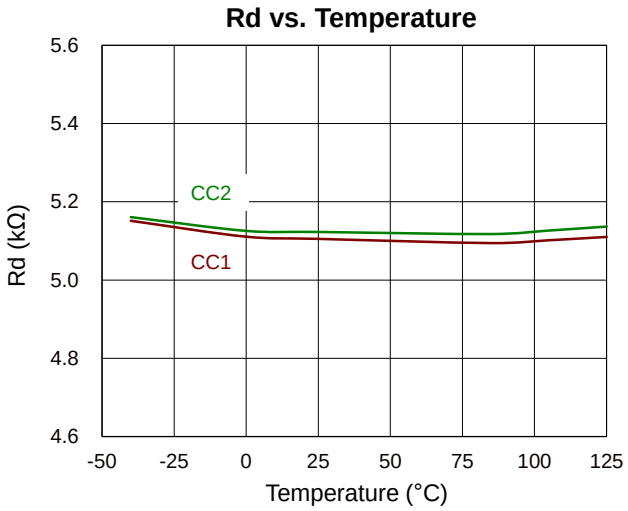



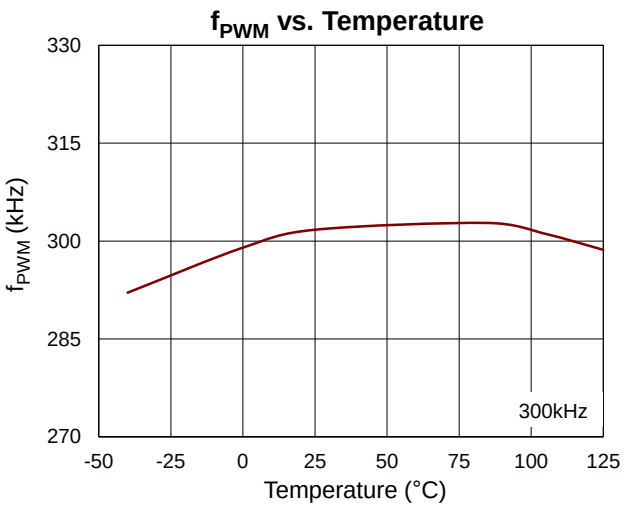



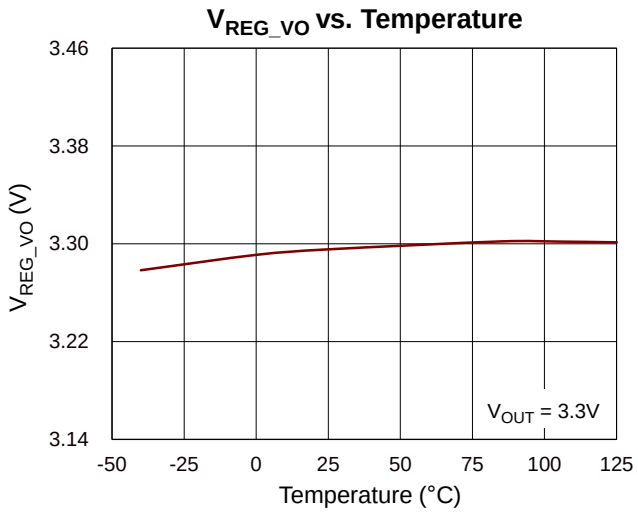



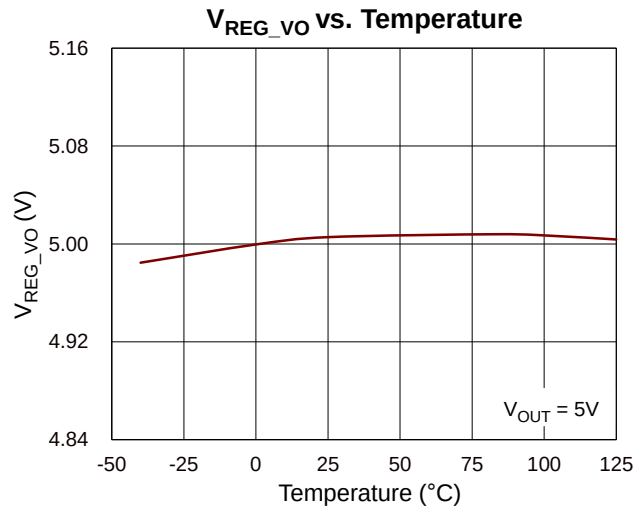


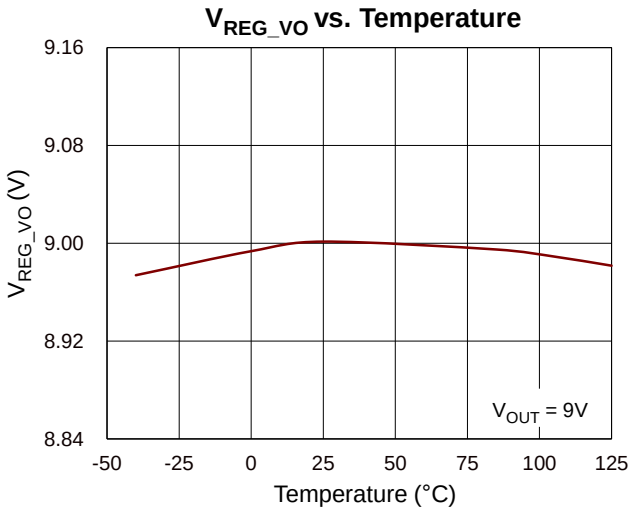



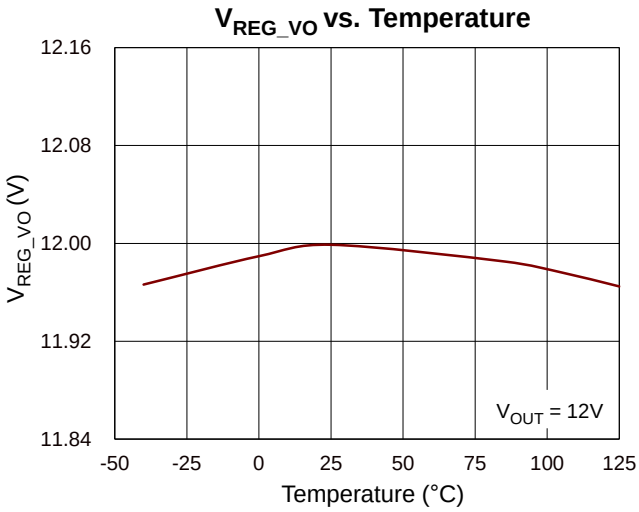



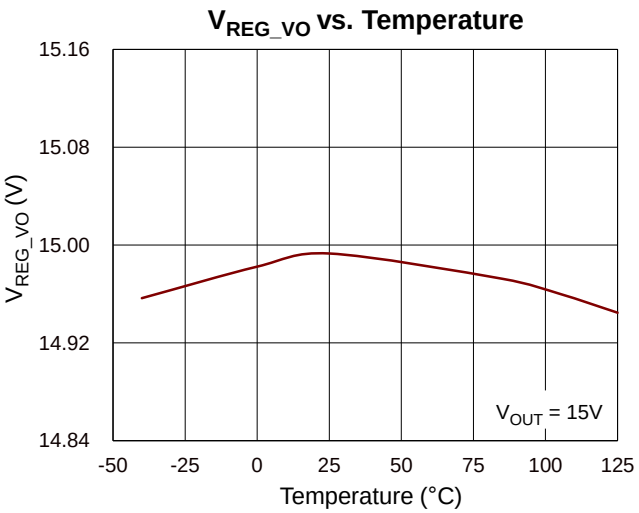



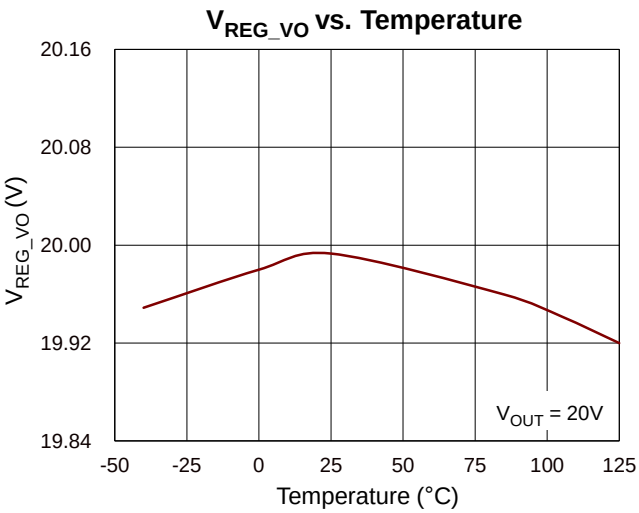



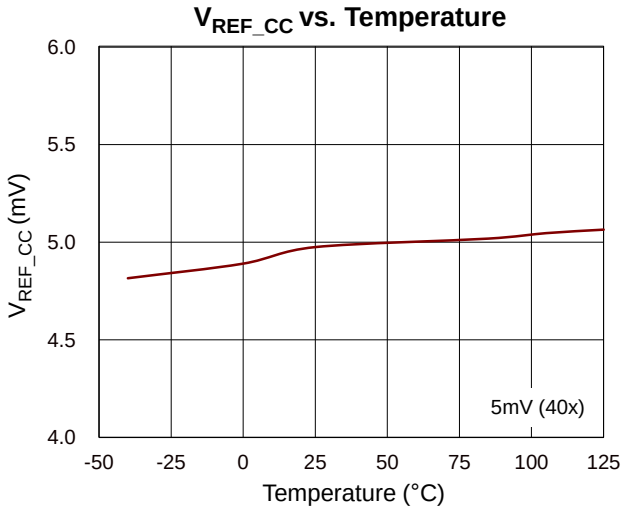



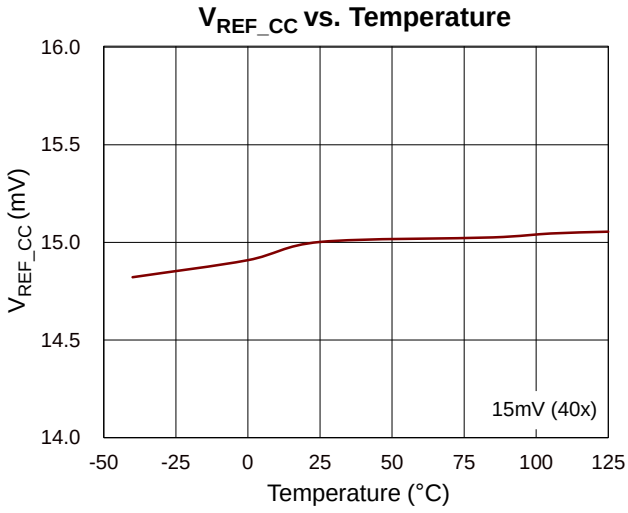


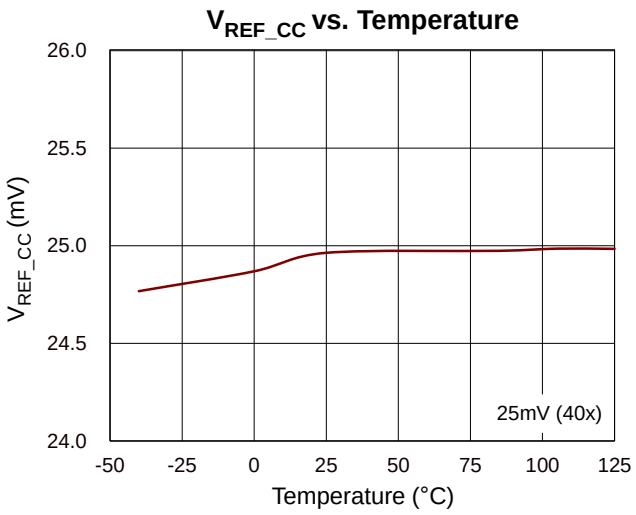



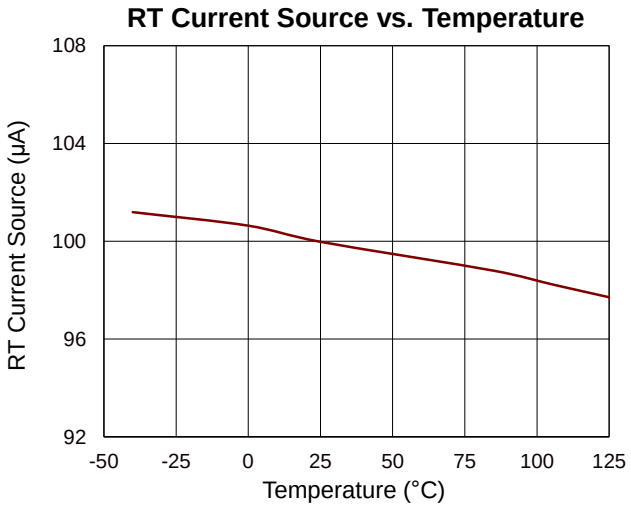





## Application Information

***Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.***

### Calculating Output Discharge Time

Figure 2 shows the functional block diagram of two built-in output bleeders at VBUS and BLD pins. The VBUS bleeder consists of an internal resistor (1.2kΩ typ.) and a pull-low MOSFET ($Q_{BLD2}$) for discharging the capacitors at VBUS side; the BLD bleeder consists of an external resistor ($R_{BLD\_EXT}$) and a pull-low MOSFET ($Q_{BLD1}$) for discharging the capacitors at the output of the PWM converter. If the blocking MOSFETs (Q1A and Q1B) are on during discharging, the BLD bleeder with larger current capability dominates the discharge time. If the blocking MOSFETs are off, the discharge time ($t_{DIS\_CVBUS}$) of the capacitor connected to the VBUS pin is determined by the following equation:

$$t_{DIS\_CVBUS} = R_{BLD\_INT} \times C_{VBUS} \times \ln\left(\frac{V_{BUS\_INI}}{V_{BUS\_FINAL}}\right)$$

where:

- $R_{BLD\_INT}$ is total internal resistance during on-state of the internal MOSFET $Q_{BLD2}$.
- $C_{VBUS}$ is the total capacitance, coupled to the VBUS pin.
- $V_{BUS\_INI}$ is the initial bus voltage before the discharging.
- $V_{BUS\_FINAL}$ is the final bus voltage at end of the discharging.

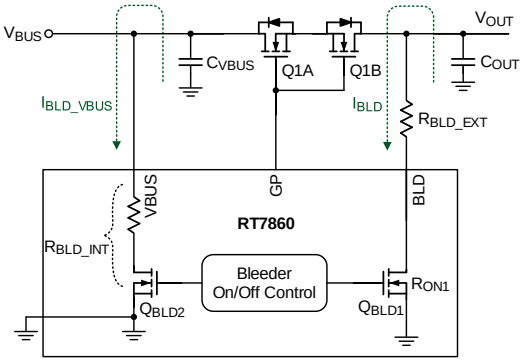



Figure 2. Functional Diagram of the Output Bleeders

Similar to the operation of the VBUS bleeder, the discharge time ($t_{DIS\_COUT}$) of the capacitor connected to the output of the PWM converter is determined by the following equation:

$$t_{DIS\_COUT} = \left(R_{BLD\_EXT} + R_{ON1}\right) \times C_{OUT} \times \ln\left(\frac{V_{OUT\_INI}}{V_{OUT\_FINAL}}\right)$$

where:

- $R_{BLD\_EXT}$ is resistance of the external resistor.
- $R_{ON1}$ is on-resistance of the internal MOSFET $Q_{BLD1}$.
- $C_{OUT}$ is the total capacitance connected to the output of the PWM converter.
- $V_{OUT\_INI}$ is the initial voltage of the PWM converter output before discharging.
- $V_{OUT\_FINAL}$ is the final voltage of the PWM converter output at end of discharging.

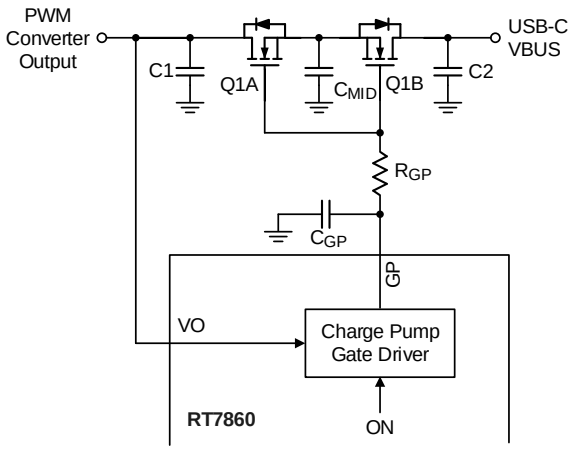



Figure 3. Functional Diagram of the Power-Path Control

### Using Charge-Pump Gate Driver for Power-Path On/Off Control

Figure 3 shows the application schematic of a power-path on/off control. In this schematic, two N-channel MOSFETs of low on-resistance driven by a built-in gate driver, supplied by the charge pump, are employed to turn on or off the power-path between the PWM converter output and the USB-C VBUS terminal. If the internal control signal “ON” goes high, the GP voltage ($V_{GP}$) will be pulled high to turn on the power MOSFETs (Q1A and Q1B) and connect the power-path. If “ON” goes low, $V_{GP}$ will be pulled low by a built-in MOSFET to disconnect the power-path.

Power input (VO) is needed for the charge pump, and the VO pin must be connected the PWM converter output to ensure the power MOSFETs can be turned on successfully.

An optional MLCC capacitor ($C_{GP}$) can be used to reduce the $V_{GP}$ rising rate and surge current in the power-path as the power MOSFETs being switched on. When the power MOSFETs being switched off, the parasitic inductor and capacitors, C1 or C2, on the power path may cause voltage ringing at the drain of the Q1A or Q1B. An optional gate resistor ($R_{GP}$) can be added to reduce the falling rate of the power-path current and prevent voltage spikes. A 1μF MLCC capacitor ($C_{MID}$) between the source terminals to ground is necessary in order to prevent oscillation due to such dual-MOSFET connection.

### Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a WQFN-48L 6x6 package, the thermal resistance, $\theta_{JA}$, is 26.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (26.8°C/W) = 3.73W for a WQFN-48L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curves in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

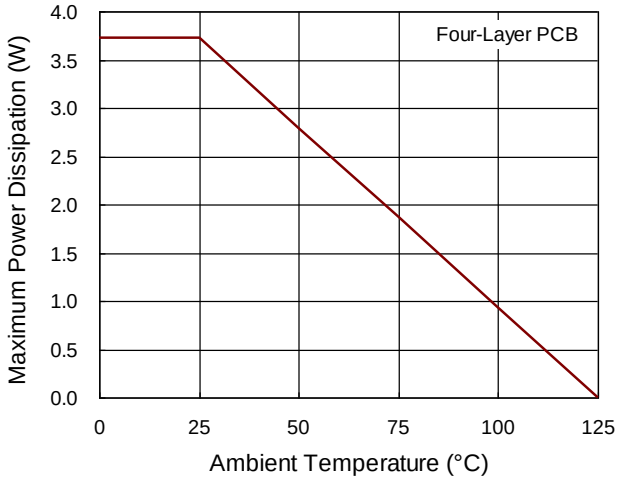



Figure 4. Derating Curve of Maximum Power Dissipation

### Layout Considerations

- Connect the IC GND pin and the exposed pad to a ground plane (IC-ground), and then connect the IC-ground to the USB GND terminals via a low-impedance path. The exposed pad is also used to dissipate the heat into PCB.
- Connect the decoupling MLCCs near the pins of VDD, V2, PVDD and VBUS. Connect the MLCCs to the pins and IC-ground via low impedance paths.

- Connect the decoupling MLCC from the BOOT1/2 pin to the PHASE1/2 pin via a short and low-impedance path.
- Connect the PGND and PHASE1 pins respectively to the Source and the Drain of low-side power MOSFET (controlled by LGATE1) via dedicated and low-impedance paths.
- Connect the PHASE2 and ZCD pins respectively to the Source and the Drain of high-side power MOSFET (controlled by UGATE2) via a dedicated and low-impedance paths.
- Connect the capacitor (between the CSOP and CSON pins) close to these pins. The paths of CSOP and CSON must be directly connected to the terminals of current-sense resistor ($R_{CSO}$) using Kelvin connections as shown in the layout shown in Figure 5.

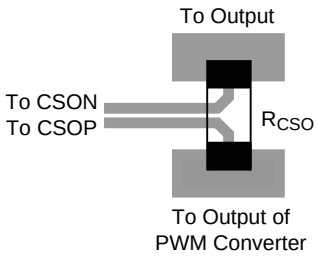



Figure 5. Kelvin Connections for the $R_{CSO}$

- Figure 6 is a recommended placement of the PWM Buck-Boost power-stage. Two critical loops "from $C_{IN1}$ → $R_{CSI}$ → $Q_A$ → $Q_B$ to $C_{IN1}$" and "from $C_{O1}$ → $Q_D$ → $Q_C$ to $C_{O1}$" must be as short as possible to minimize the switching noise at PCIP/CSIP, PCIN, PHASE1, PHASE2 and ZCD pins. The shorter paths also help to reduce radiated EMI. It is necessary to use an MLCC (10µF/50V, X5R/X7R) for the input capacitor ($C_{IN1}$) and output capacitor ($C_{O1}$). For reducing the input and output voltage ripples during heavy load operation, it is recommended to add more MLCCs or solid input and output capacitors. Moreover, to improve heat dissipation, one needs to increase the PCB areas for Drains of high-side and low-side MOSFETs.

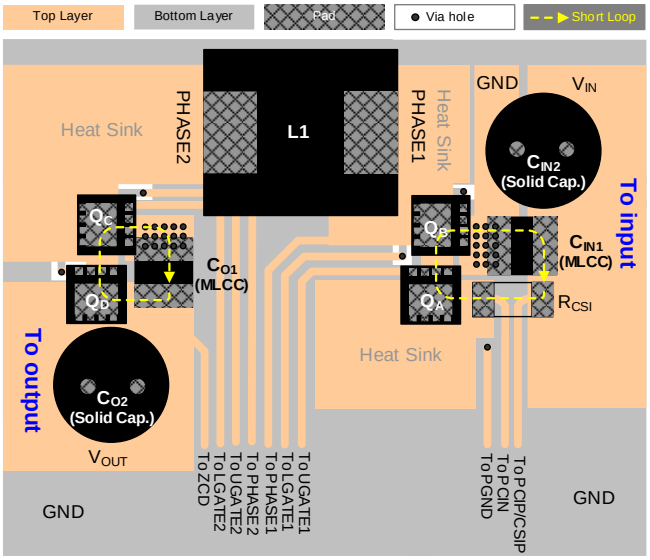



Figure 6. Recommended PCB Layout of the Power Stage

- To prevent the switching noises, separate the following signals from the switching nodes and the switching-current paths connected with PHASE pin:
  - Input and output current-sense signals
  - CC1 and CC2 signals
  - CV-loop feedback signal
- For improving ESD immunity, connect MLCCs close to the GND and VBUS terminals of the USB Type-C connector. Connect the capacitors to the USB VBUS and GND terminals through the low-impedance paths.

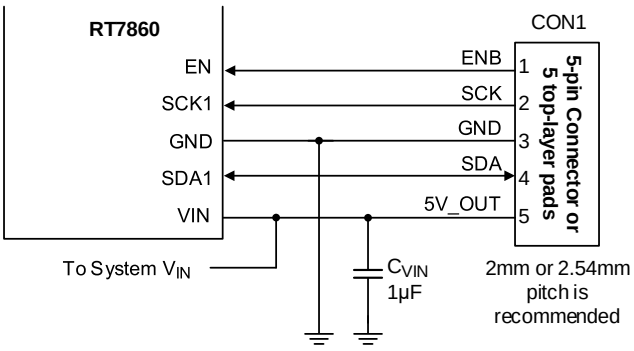


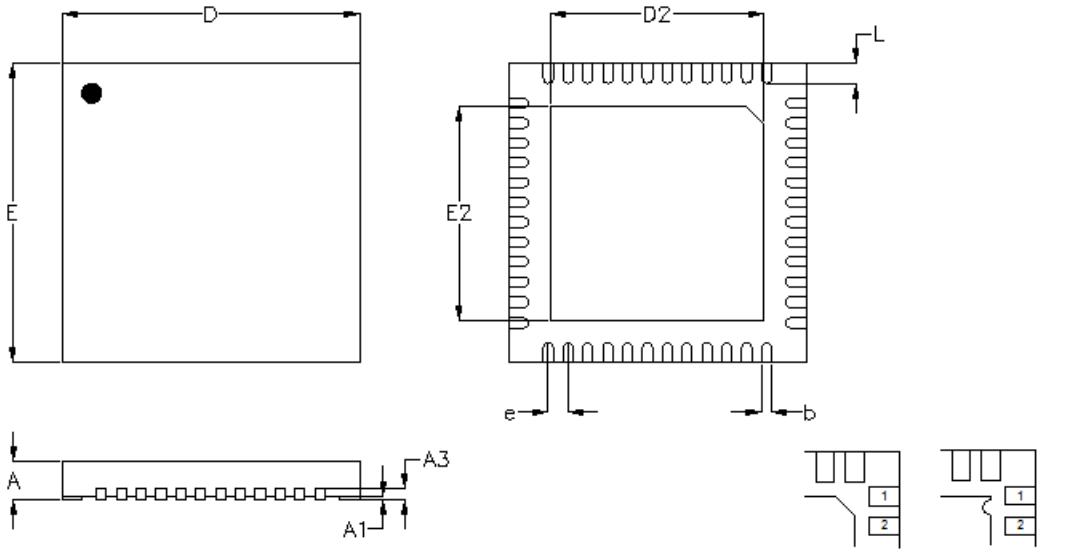

Figure 7. Connections for Manual Firmware Updates

### Manual Firmware Update

During product development stage, users might need to download or update the RT7860 firmware. This can be done by adding a 5-pin connector (CON1) or five test pads on PCBs for updating the RT7860 firmware manually as shown in Figure 7. This connector is then connected to a “Firmware update fixture” by a 5-pin cable. The fixture is also connected to a PC via a Micro USB cable and acts as a bridge between the RT7860 and the PC. With this setup, users can download firmware to the RT7860 by using the RT7860 graphic user interface (GUI) installed in the PC. During the firmware update process, the fixture can supply current (up to 40mA) to the RT7860 and the system $V_{IN}$ via the 5V_OUT pin of the 5-pin cable.

If the power from the fixture is enough to power the RT7860 and the system $V_{IN}$, it is not necessary to use the auxiliary input voltage for the system $V_{IN}$. On the other hand, if the system $V_{IN}$ consumes more current than the fixture capability, one needs to use an auxiliary input voltage.

## Outline Dimension




DETAIL A

Pin #1 ID and Tie Bar Mark Options

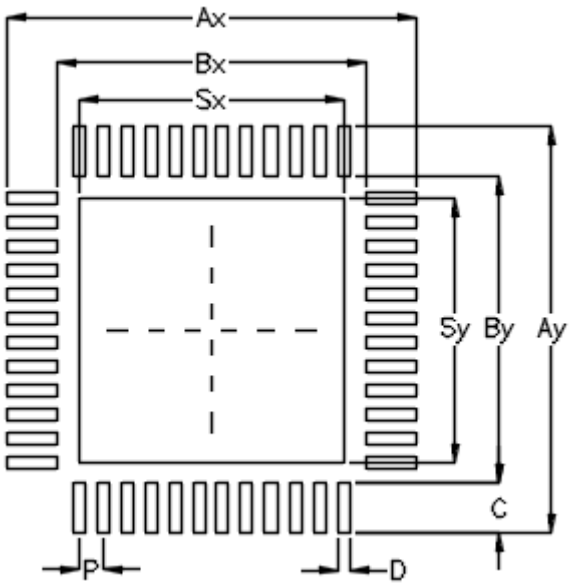
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|---|
| | | Min | Max | Min | Max |
| A | | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | | 0.175 | 0.250 | 0.007 | 0.010 |
| b | | 0.150 | 0.250 | 0.006 | 0.010 |
| D | | 5.950 | 6.050 | 0.234 | 0.238 |
| D2 | Option 1 | 4.250 | 4.350 | 0.167 | 0.171 |
| | Option 2 | 4.350 | 4.450 | 0.171 | 0.175 |
| | Option 3 | 4.650 | 4.750 | 0.183 | 0.187 |
| | Option 4 | 4.450 | 4.550 | 0.175 | 0.179 |
| E | | 5.950 | 6.050 | 0.234 | 0.238 |
| E2 | Option 1 | 4.250 | 4.350 | 0.167 | 0.171 |
| | Option 2 | 4.350 | 4.450 | 0.171 | 0.175 |
| | Option 3 | 4.650 | 4.750 | 0.183 | 0.187 |
| | Option 4 | 4.450 | 4.550 | 0.175 | 0.179 |
| e | | 0.400 | | 0.016 | |
| L | | 0.350 | 0.450 | 0.014 | 0.018 |

**W-Type 48L QFN 6x6 Package**

Note: The package of RT7860 uses Option 1.

## Footprint Information

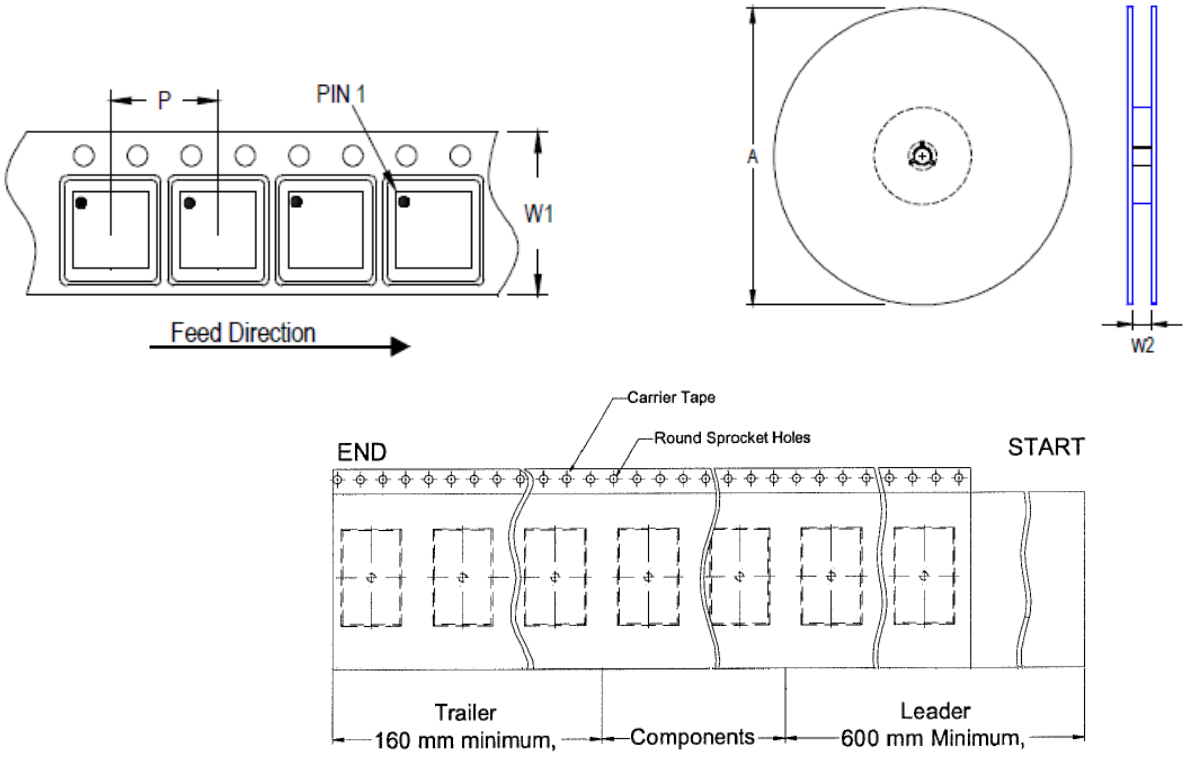



| Package | | Number of Pin | Footprint Dimension (mm) | | | | | | | | | Tolerance |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | P | Ax | Ay | Bx | By | C | D | Sx | Sy | |
| V/W/U/XQFN6x6-48 | Option1 | 48 | 0.40 | 6.80 | 6.80 | 5.10 | 5.10 | 0.85 | 0.20 | 4.40 | 4.40 | ±0.05 |
| | Option2 | | | | | | | | | 4.50 | 4.50 | |
| | Option3 | | | | | | | | | 4.70 | 4.70 | |
| | Option4 | | | | | | | | | 4.60 | 4.60 | |

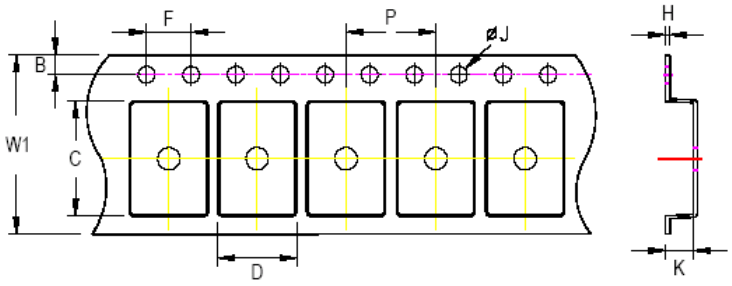
Note: The package of RT7860 uses Option 1.

## Packing Information

### Tape and Reel Data




| Package Type | Tape Size (W1) (mm) | Pocket Pitch (P) (mm) | Reel Size (A) | | Units per Reel | Trailer (mm) | Leader (mm) | Reel Width (W2) Min./Max. (mm) |
|---|---|---|---|---|---|---|---|---|
| | | | (mm) | (in) | | | | |
| QFN/DFN 6x6 | 16 | 12 | 330 | 13 | 2,500 | 160 | 600 | 16.4/18.4 |




**C, D and K are determined by component size. The clearance between the components and the cavity is as follows:**

**- For 16mm carrier tape: 1.0mm max.**

| Tape Size | W1 | P | | B | | F | | ØJ | | H |
|---|---|---|---|---|---|---|---|---|---|---|
| | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Max. |
| 16mm | 16.3mm | 11.9mm | 12.1mm | 1.65mm | 1.85mm | 3.9mm | 4.1mm | 1.5mm | 1.6mm | 0.6mm |

**Tape and Reel Packing**

| Step | Photo/Description | Step | Photo/Description |
|---|---|---|---|
| 1 |  Reel 13” | 4 |  1 reel per inner box **Box G** |
| 2 |  HIC & Desiccant (2 Unit) inside | 5 |  6 inner boxes per outer box |
| 3 |  Caution label is on backside of Al bag | 6 |  Outer box **Carton A** |

| Container / Package | Reel | | Box | | | | Carton | | |
|---|---|---|---|---|---|---|---|---|---|
| | Size | Units | Item | Weight(kg) | Reels | Units | Item | Boxes | Units |
| QFN and DFN 6x6 | 13” | 2,500 | Box G | 1.11 | 1 | 2,500 | Carton A | 6 | 15,000 |

### Packing Material Anti-ESD Property

| Surface Resistance | Aluminum Bag | Reel | Cover tape | Carrier tape | Tube | Protection Band |
|---|---|---|---|---|---|---|
| $\Omega/cm^2$ | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** |

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## Datasheet Revision History

| Version | Date | Description | Item |
|---|---|---|---|
| 00 | 2023/9/15 | Final | General Description on P1<br>Ordering Information on P1<br>Features on P1, 2<br>Simplified Application Circuit on P2<br>Functional Pin Description on P3<br>Operation on P6<br>Electrical Characteristics on P10, 16<br>Application Information on P22, 24<br>Outline Dimension on P26<br>Footprint Information on P27 |