

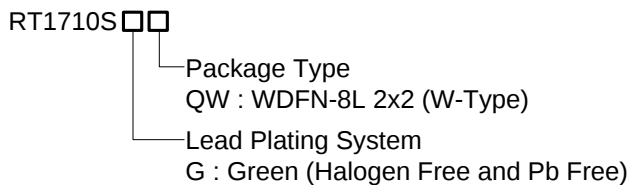
Cable ID for USB Type-C Cables

General Description

The RT1710S is a Type-C cable ID for active and passive cables. All USB Full-Featured Type-C cables shall be electronically marked. Electronically marked cables shall support USB Power Delivery Structured VDM Discover Identity command directed to SOP'. This provides a method to determine the characteristics of the cable, e.g. its current carrying capability, its performance, vendor identification, etc. This may be referred to as the USB Type-C Cable ID function.

The RT1710S is available in a WDFN-8L 2x2 package.

Ordering Information

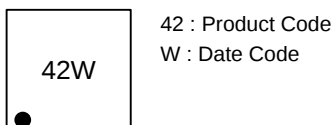


Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



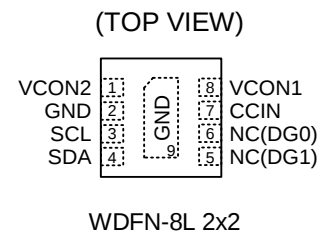
Features

- Support SOP' Communication
- Integrated Transceiver (BMC PHY)
- Embedded Both Side RA Resistor
- Embedded Both Side ISO Diode
- Embedded MTP
- Support Multi-Time Writable Memory to Store VDM Data
- Support 4V to 5.5V Operation on VCON1/VCON2 Pin
- Built-in Slew Rate Control for BMC Signal to Reduce the Effect of EMI
- Support Custom Structured VDM Writing Through CC Pin
- Support I²C Bus for Programming VDM Data
- 8-Lead WDFN Package

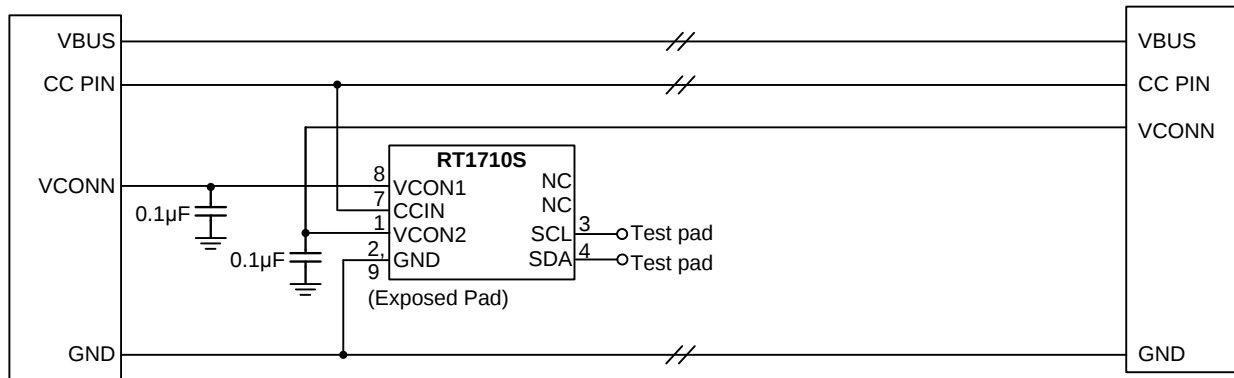
Applications

- USB Full-Featured Type-C Cables

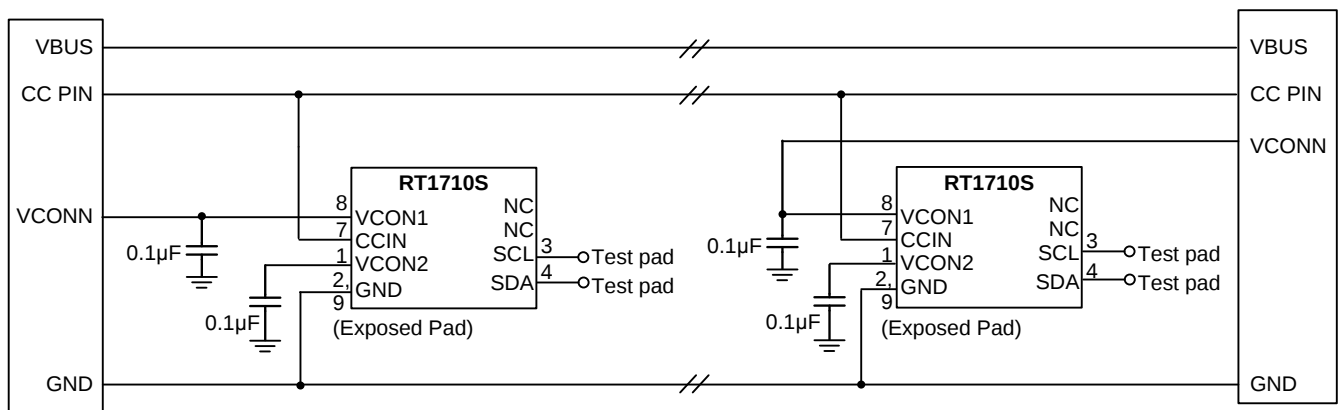
Pin Configuration



Typical Application Circuit



Electronically Marked Cable with VCONN connected through the cable

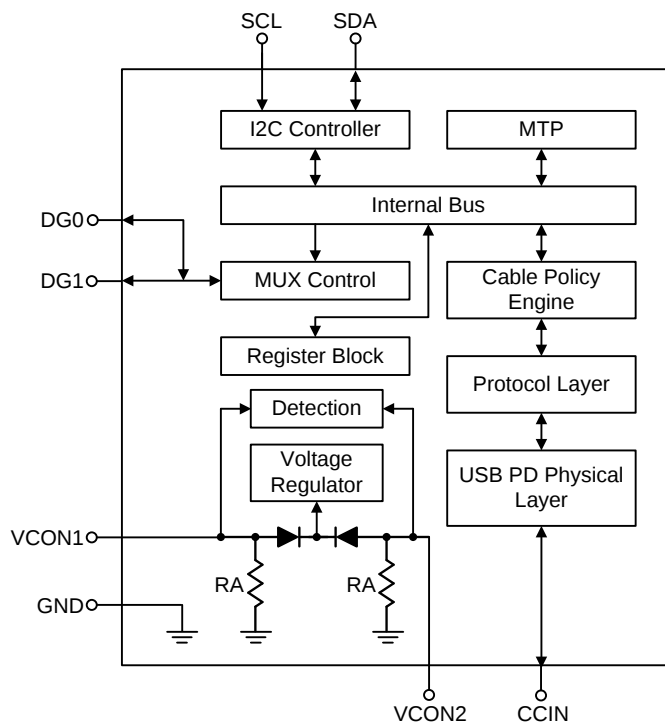


Electronically Marked Cable with SOP' at both ends

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VCON2	The input pin supplied from another side VCONN.
2	GND	Ground.
3	SCL	This pin is only used for debug. No internal connection.
4	SDA	This pin is only used for debug. No internal connection.
5	NC (DG1)	No internal connection.
6	NC (DG0)	No internal connection.
7	CCIN	Configuration channel pin used in the discovery, configuration and management of connections.
8	VCON1	The input pin supplied from VCONN.
9 (Exposed Pad)	GND	Power ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

SOP' Communication is recognized by electronics in one Cable Plug (which may be attached to either the UFP or DFP). SOP Communication between the Port Partners is not recognized by the Cable Plug. the term Cable Plug in the SOP' Communication case is used to represent a logical entity (RT1710S) in the cable which is capable of PD Communication.

Both SOP Communication and SOP' Communication take place over a single wire (CC pin). For a product which does not recognize SOP' Packets, this will look like a non-idle channel.

Absolute Maximum Ratings (Note1)

- VCON1/VCON2----- -0.3V to 6V
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
WDFN-8L 2x2----- 2.19W
- Package Thermal Resistance (Note 2)
WDFN-8L 2x2, θ_{JA} ----- 45.5°C/W
WDFN-8L 2x2, θ_{JC} ----- 11.5°C/W
- Lead Temperature (Soldering, 10 sec.)----- 260°C
- Junction Temperature----- 150°C
- Storage Temperature Range----- -65°C to 150°C
- ESD Susceptibility (Note 3)
HBM (Human Body Model) ----- 8kV
MM (Machine Model)----- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ----- 4V to 5.5V
- Ambient Temperature Range----- -40°C to 85°C
- Junction Temperature Range ----- -40°C to 125°C

Electrical Characteristics(V_{DD} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Common Normative Signaling Requirements						
Bit rate	f _{BitRate}		270	300	330	Kbps
Common Normative Signaling Requirements for Transmitter						
Maximum difference between the bit-rate during the part of the packet following the Preamble and the reference bit-rate.	p _{BitRate}		--	--	0.25	%
Time from the end of last bit of a Frame until the start of the first bit of the next Preamble.	t _{InterFrameGap}		25	--	--	μs
Time before the start of the first bit of the Preamble when the transmitter shall start driving the line.	t _{StartDrive}		-1	--	1	μs
BMC Common Normative Requirements						
Time to cease driving the line after the end of the last bit of the Frame.	t _{EndDriveBMC}		--	--	23	μs
Fall Time	t _{Fall}		300	--	--	ns
Time to cease driving the line after the final high-to-low transition	t _{HoldLowBMC}		1	--	--	μs
Rise Time	t _{Rise}		300	--	--	ns

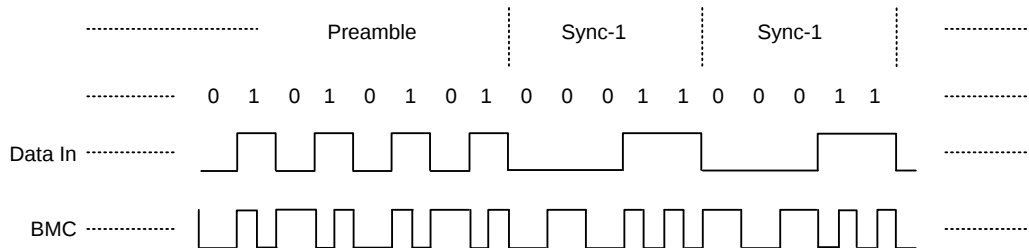
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Swing	V _{Swing}		1.05	1.125	1.2	V
Transmitter Output Impedance	Z _{Driver}		33	--	75	Ω
BMC Receiver Normative Requirements						
Cable Termination	R _A		800	--	1200	Ω
Time Window for Detecting Non-Idle	t _{TransitionWindow}		12	--	20	μs
Receiver Input Impedance	Z _{BmcRx}		10	--	--	MΩ

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

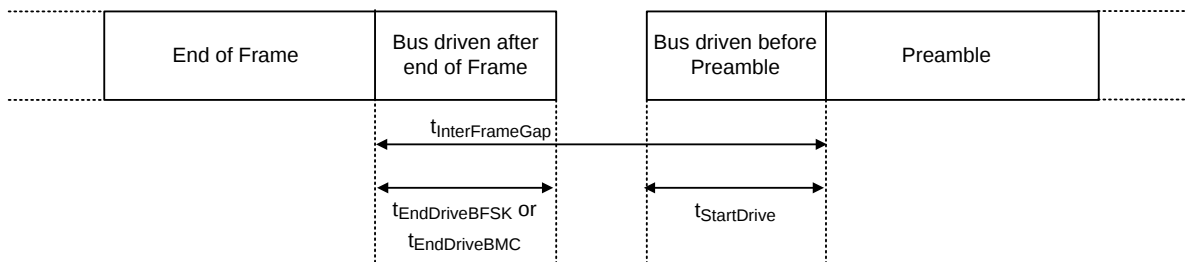
Note 2. θ_{JA} is measured under natural convection (still air) at $T_A = 25^\circ\text{C}$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

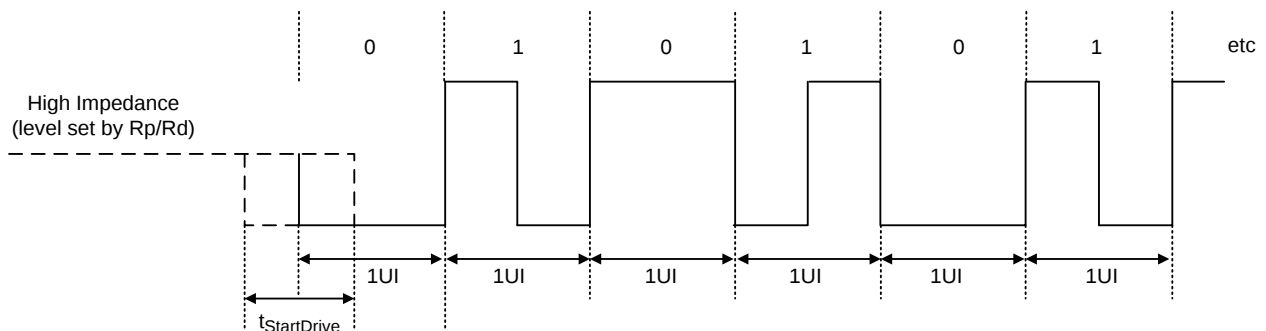
Note 4. The device is not guaranteed to function outside its operating conditions.



BMC Example

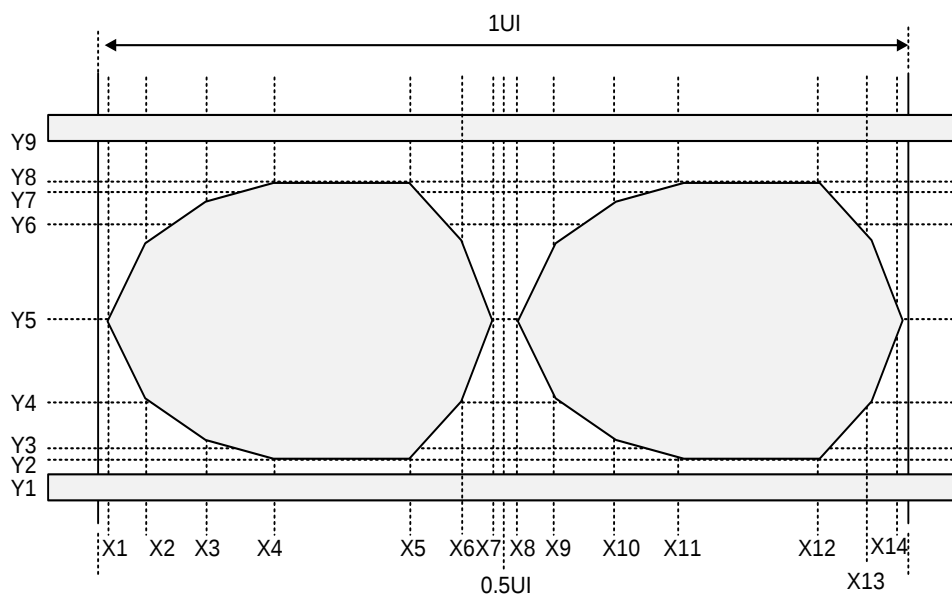


Inter-Frame Gap Timings

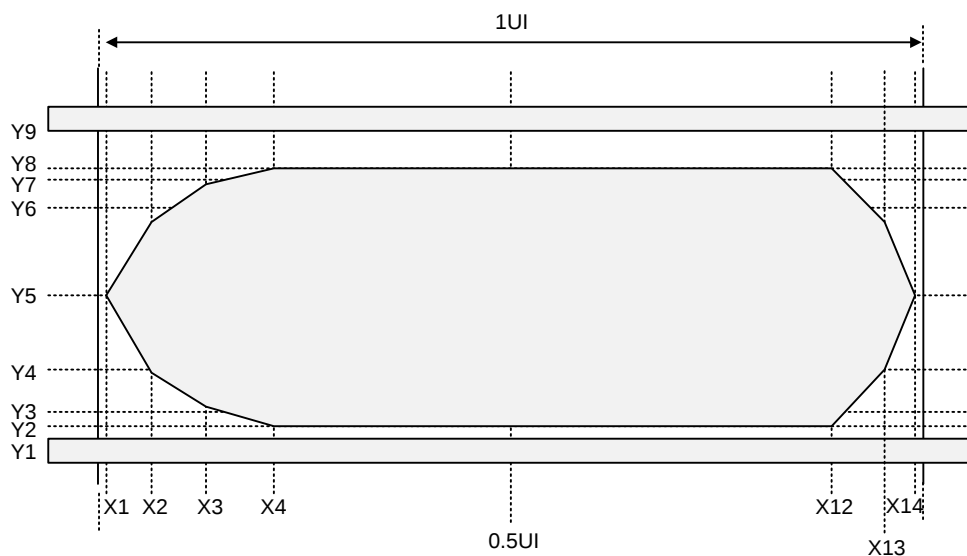


BMC Encoded Start of Preamble

BMC TC Mask Definition, Y values						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Lower bound of Outer mask	Y1Tx			-0.075		V
Lower bound of inner mask	Y2Tx			0.075		V
Y3Tx point	Y3Tx			0.15		V
Y4Tx point	Y4Tx			0.325		V
Inner mask vertical midpoint	Y5Tx			0.5625		V
Y6Tx point	Y6Tx			0.8		V
Y7Tx point	Y7Tx			0.975		V
Y8Tx point	Y8Tx			1.04		V
Upper Bound of Outer mask	Y9Tx			1.2		V



BMC Tx 'ONE' Mask



BMC Tx 'ZERO' Mask

Application Information

Start of Packet Sequence Prime (SOP')

The SOP' ordered set is defined as: two Sync-1 K-codes followed by two Sync-3 K-codes

K-code number	K-code in code table
1	Sync-1
2	Sync-1
3	Sync-3
4	Sync-3

A Cable Plug capable of SOP' Communications shall only detect and communicate with packets starting with SOP'.

A DFP or Source needing to communicate with a Cable Plug capable of SOP' Communications, attached between a Port Pair will be able to communicate using both packets starting with SOP' to communicate with the Cable Plug and starting with SOP to communicate with its Port Partner. The DFP or Source shall co-ordinate SOP and SOP' Communication so as to avoid collisions.

Setting the VDM Type field to 1 (Structured VDM) defines the use of bits Bit[14:0] in the Structured VDM Header. The fields in the Structured VDM Header are defined in Table.

The following rules apply to the use of Structured VDM messages:

- Structured VDMs shall only be used when an Explicit Contract is in place with the following exception :
Prior to establishing an Explicit Contract a Source may issue Discover Identity messages, to a Cable Plug using SOP' Packets, as an Initiator.
- Only the DFP shall be an Initiator of Structured VDMs except for the Attention Command that shall only be initiated by the UFP.
- Only the UFP or a Cable Plug shall be a Responder to Structured VDMs.
- Structured VDMs shall not be initiated or responded to under any other circumstances.
- A DFP or UFP which does not support Structured VDMs shall ignore any Structured VDMs received.
- A Command sequence shall be interruptible e.g. due to the need for a message sequence using SOP Packets.

Structured VDM

Bit(s)	Field	Description
Bit[31:16]	Standard or Vendor ID (SVID)	Unique 16 bit unsigned integer, assigned by the USB-IF
Bit[15]	VDM Type	1 = Structured VDM
Bit[14:13]	Structured VDM Version	Version Number of the Structured VDM (not this specification Version): Version 1.0 = 0 Values 1-3 are reserved
Bit[12:11]	Reserved	Shall be set to 0 and shall be ignored
Bit[10:8]	Object Position	For the Enter Mode and Exit Mode Commands: 000b = Reserved 001b..110b = Index into the list of VDOs to identify the desired Mode VDO 111b = Exit all Modes (equivalent of a power on reset). Shall not be used with the Enter Mode Command.
Bit[7:6]	Command Type	00b = Initiator 01b = Responder ACK 10b = Responder NAK 11b = Responder BUSY
Bit[5]	Reserved	Shall be set to 0 and shall be ignored

Bit(s)	Field	Description
Bit[4:0]	Command (note 1)	0 = Reserved, shall not be used 1 = Discover Identity 2 = Discover SVIDs 3 = Discover Modes 4 = Enter Mode 5 = Exit Mode 6 = Attention 7-15 = Reserved, shall not be used 16..31 = SVID Specific Commands

Note 1: In the case where a SID is used the modes are defined by a standard. When a VID is used the modes are defined by the Vendor.

Discover Identity

The Discover Identity Command is provided to enable an Initiator (DFP) to identify its Port Partner and for an Initiator (Source or DFP) to identify the attached Cable Plug (Responder).

The SVID in the Discover SVIDs Command shall be set to the PD SID by both the Initiator and the Responder for this Command.

The Discover Identity Command sent back by the Responder contains an ID Header, a Cert Stat VDO and some Type specific VDOs which depend on the Product Type. This specification defines the following Type specific VDOs:

Header No. of Data Objects = 4-7 ¹	VDM Header	ID Header	Cert Stat VDO	Product VDO	0..3 ² Product Type VDO(s)
--	---------------	--------------	---------------	-------------	--

ID Header

The ID Header contains the Vendor ID corresponding to the Power Delivery Product.

Bit(s)	Description
Bit[31]	Data Capable as USB Host : • Shall be set to one if the product is capable of enumerating USB Devices. • Shall be set to zero otherwise
Bit[30]	Data Capable as a USB Device : • Shall be set to one if the product is capable of enumerating as a USB Device. • Shall be set to zero otherwise
Bit[29:27]	Product Type : • 000b – Undefined • 001b – Hub • 010b – Peripheral • 011b – Passive Cable • 100b – Active Cable • 101b – Alternate Mode Adapter (AMA) • 111b..110b – Reserved, shall not be used.
Bit[26]	Modal Operation Supported : • Shall be set to one if the product supports Modal Operation. • Shall be set to zero otherwise
Bit[25:16]	Reserved. Shall be set to zero.
Bit[15:0]	16-bit unsigned integer. USB Vendor ID

Cert Stat VDO

The Cert Stat VDO contains the Test ID (TID) allocated by USB-IF during certification.

Bit(s)	Description
Bit[31:20]	Reserved, shall be set to zero.
Bit[19:0]	20-bit unsigned integer, TID

Product VDO

The Product VDO contains identity information relating to the product.

Bit(s)	Description
Bit[31:16]	16-bit unsigned integer. USB Product ID
Bit[15:0]	16-bit unsigned integer. bcdDevice

Cable VDO

The Cable VDO defined in this section shall be sent when the Product Type is given as Passive or Active Cable.

Bit(s)	Field	Description
Bit[31:28]	Cable HW Version	0000b..1111b assigned by the VID owner
Bit[27:24]	Cable Firmware Version	0000b..1111b assigned by the VID owner
Bit[23:20]	Reserved	Shall be set to zero.
Bit[19:18]	Type-C to Type-A/B/C	00b = Type-A 01b = Type-B 10b = Type-C 11b = Captive
Bit[17]	Type-C to Plug/Receptacle	0 = Plug 1 = Receptacle (not valid when B19..18 set to Type-C or Captive)
Bit[16:13]	Cable Latency	0000b – reserved 0001b – <10ns (~1m) 0010b – 10ns to 20ns (~2m) 0011b – 20ns to 30ns (~3m) 0100b – 30ns to 40ns (~4m) 0101b – 40ns to 50ns (~5m) 0110b – 50ns to 60ns (~6m) 0111b – 60ns to 70ns (~7m) 1000b – 1000ns (~100m) 1001b – 2000ns (~200m) 1010b – 3000ns (~300m) 1011b1111b reserved Includes latency of electronics in Active Cable
Bit[12:11]	Cable Termination Type	00b = Both ends Passive, VCONN not required 01b = Both ends Passive, VCONN required 10b = One end Active, one end passive, VCONN required 11b = Both ends Active, VCONN required
Bit[10]	SSTX1 Directionality Support	0 = Fixed 1 = Configurable

Bit(s)	Field	Description
Bit[9]	SSTX2 Directionality Support	0 = Fixed 1 = Configurable
Bit[8]	SSRX1 Directionality Support	0 = Fixed 1 = Configurable
Bit[7]	SSRX2 Directionality Support	0 = Fixed 1 = Configurable
Bit[6:5]	VBUS Current Handling Capability	00b = VBUS not through cable 01b = 3A 10b = 5A 11b = reserved.
Bit[4]	VBUS through cable	0 = No 1 = Yes
Bit[3]	SOP" controller present	1 = SOP" controller present 0 = No SOP" controller present
Bit[2:0]	USB Super speed Signaling Support	000b = USB 2.0 only 001b = [USB3.1] Gen1 010b = [USB3.1] Gen1 and Gen2 011b.. 111b = reserved.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WDFN-8L 2x2 package, the thermal resistance, θ_{JA} , is 45.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (45.5^\circ\text{C/W}) = 2.19\text{W for a WDFN-8L 2x2 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

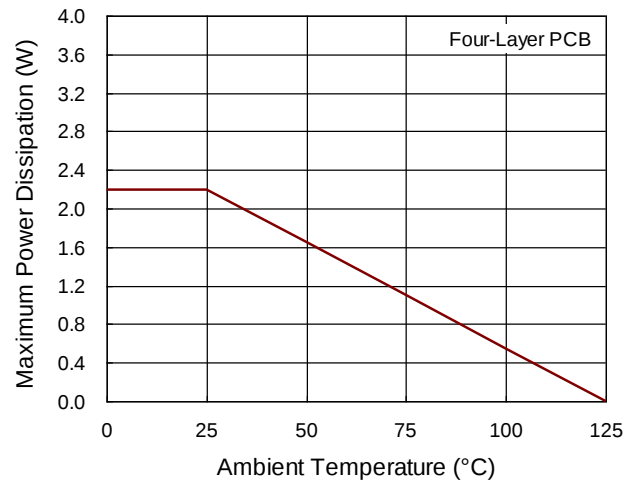


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Consideration

- PCB layout is very important for designing e-marked IC (RT1710S) circuits.
- Connect VCON1/VCON2 pins with bypass capacitor, and as near the pins as possible.
- The exposed pad of the chip should be connected to a large ground plane for thermal consideration.
- Keep the CC1 traces away from those sensing pins (D+,D-,SSTX+,SSTX-,SSRX+,SSRX-,SBU).

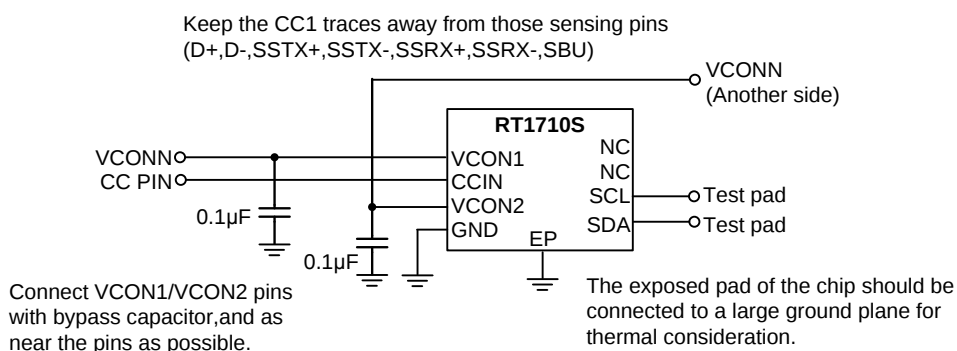
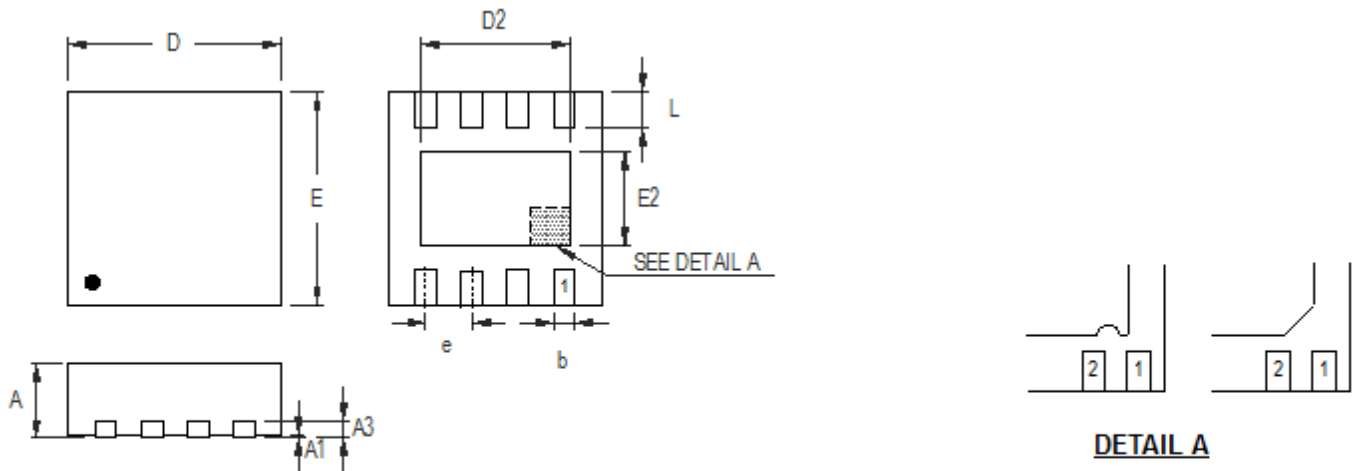


Figure 2. PCB Layout Guide

Outline Dimension



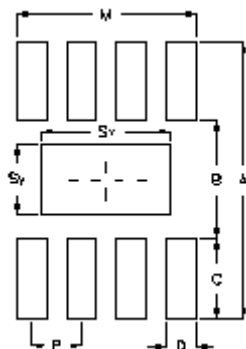
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-8	8	0.50	2.80	1.20	0.80	0.30	1.30	0.70	1.80	±0.05

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

Richtek products are sold by description only. Richtek reserves the right to change the circuitry and/or specifications without notice at any time. Customers should obtain the latest relevant information and data sheets before placing orders and should verify that such information is current and complete. Richtek cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Richtek product. Information furnished by Richtek is believed to be accurate and reliable. However, no responsibility is assumed by Richtek or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Richtek or its subsidiaries.

Copyright © 2017 Richtek Technology Corporation. All rights reserved. **RICHTEK** is a registered trademark of Richtek Technology Corporation.

www.richtek.com

DS1710S-00 February 2017