

General Description

The SY20810 is a single-channel load switch with a 2.8m Ω resistance. It features a controlled and adjustable turn-on mechanism and comes with an integrated Power Good (PG) indicator.

The device contains an N-channel MOSFET that can operate over an input voltage range of 0.6V to 5.5V and can support a maximum continuous current of 10A. The wide input voltage range and high current capability enable the device to be used in various applications. The low ON resistance of 2.8m Ω minimizes the voltage drop across the load switch, effectively reducing power loss.

The device's controlled rise time significantly mitigates inrush current associated with large bulk load capacitances, effectively minimizing or eliminating power supply droop. The design flexibility is enhanced through the adjustable slew rate via CSST, allowing for a trade-off between inrush current and power-up timing requirements. Additionally, the integrated PG indicator informs the system of the load switch status, aiding in seamless power sequencing.

The SY20810 is available in a compact DFN 2mm $\times$ 3mm-10pin package with an integrated thermal pad, enabling efficient dissipation of high power. The device is designed for operation across a wide temperature range, from -40 $^{\circ}$ C to +105 $^{\circ}$ C in free-air conditions.

Features

- V_{BIAS} Voltage Range: 2.5V to 5.5V
- V_{IN} Voltage Range: 0.6V to V_{BIAS}
- ON-Resistance
 - $R_{ON} = 2.8\text{ m}\Omega$ (typical) at $V_{IN} = 5\text{ V}$, $V_{BIAS} = 5\text{ V}$
 - $R_{ON} = 2.8\text{ m}\Omega$ (typical) at $V_{IN} = 3.3\text{ V}$, $V_{BIAS} = 3.3\text{ V}$
- 10-A Maximum Continuous Switch Current
- Quiescent Current
 - $I_{Q_VBIAS} = 63\mu\text{A}$ at $V_{BIAS} = 5\text{ V}$
- Shutdown Current
 - $I_{SD_VBIAS} = 5.5\mu\text{A}$ at $V_{BIAS} = 5\text{ V}$
 - $I_{SD_VIN} = 4\text{ nA}$ at $V_{BIAS} = 5\text{ V}$, $V_{IN} = 5\text{ V}$
- Controlled and Adjustable Slew Rate through C_{SST}
- Integrated Single Channel Load Switch
- Power Good (PG) Indicator
- Compact DFN2x3-10 Package
- ESD Performance
 - 2-kV HBM and 1-kV CDM

Applications

- Notebooks
- Desktop PC
- SSDs
- Servers
- Telecom systems

Typical Application

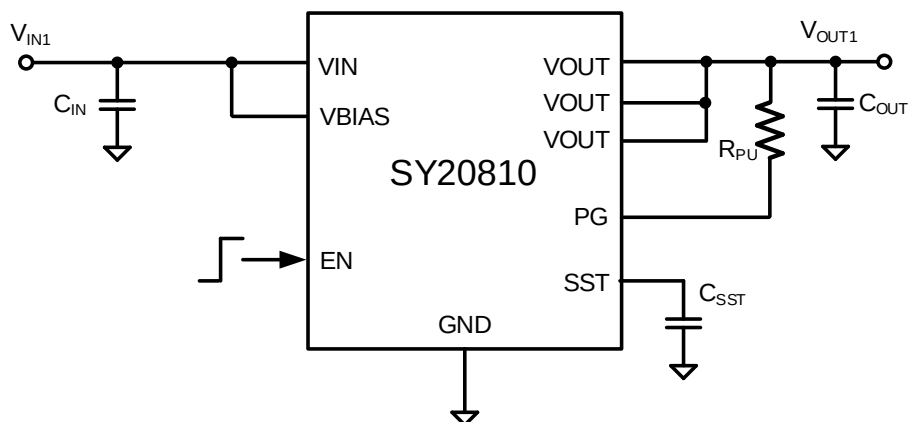


Figure 1. Schematic Diagram

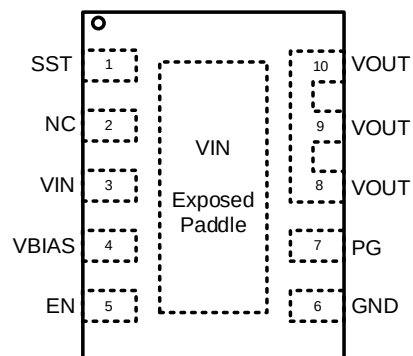
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20810DHC	DFN2×3-10 RoHS Compliant and Halogen Free	Wdxyz

Device code: Wd

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Number	Pin Name	Pin Description
1	SST	VOUT slew rate control.
2	NC	No connection.
3	VIN	Switch input. Bypass this input with a ceramic capacitor to GND.
4	VBIAS	Bias voltage. Power supply to the device.
5	EN	Active high switch control input. Do not leave it floating.
6	GND	Ground.
7	PG	Power good indicator. Active high, Open drain output. Tie to GND if not used.
8,9,10	VOUT	Switch output.
Exposed paddle	VIN	Switch input. Connected to a wide and thick power trace to achieve the best thermal and electrical performance.

Block Diagram

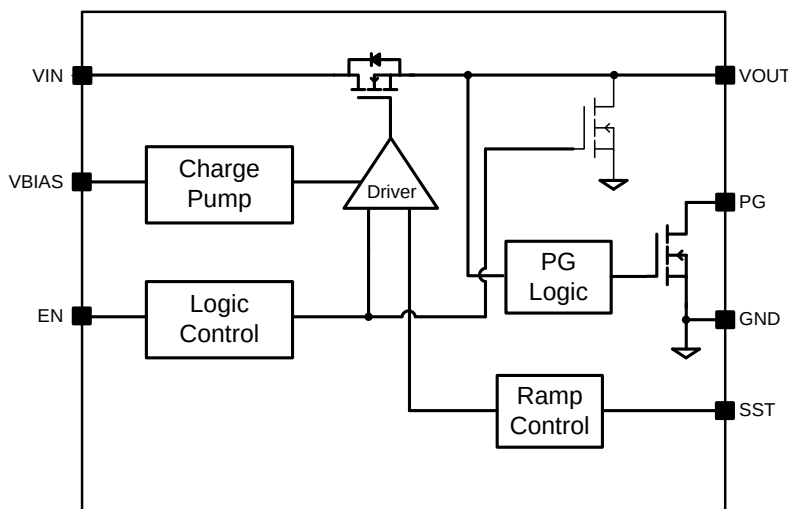


Figure 2. Block Diagram



Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
V _{IN} , V _{BIAS} , V _{OUT} , EN, PG	-0.3	6	V
SST	-0.3	V _{OUT} +6	
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ _{JA} Junction-to-Ambient Thermal Resistance	51.4	°C/W
θ _{JC} Junction-to-Case Thermal Resistance	65	
P _D Power Dissipation T _A = 25°C	2.43	W

ESD Susceptibility

Parameter (Note 2)	Min	Max	Unit
HBM (Human Body Mode)		2	kV
CDM (Charged Device Mode)		1	

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
V _{IN}	0.6	V _{BIAS}	V
V _{BAIS}	2.5	5.5	
V _{OUT}		V _{IN}	
EN, PG	0	5.5	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	105	

Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the operating ambient temp - 40°C ≤ T_A ≤ +105°C (full) and V_{BIAS} = 5V. Typical values are for T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Range for V _{IN}	V _{IN}		0.6		5.5	V
Voltage Range for V _{BUS}	V _{BUS}		2.5		5.5	V
V _{BIAS} UVLO	V _{BIAS_UVLO}				2.4	V
V _{BIAS} UVLO Hysteresis	V _{BIAS_HYS}			0.1		V
V _{BIAS} Quiescent Current	I _{Q_BIAS}	V _{BIAS} =5V, V _{IN} =EN=5V, -40°C to 85°C		75	98	μA
		V _{BIAS} =3.3V, V _{IN} =EN=3.3V, -40°C to 85°C		66	86	μA
		V _{BIAS} =5V, V _{IN} =EN=5V, -40°C to 105°C		75	100	μA
		V _{BIAS} =3.3V, V _{IN} =EN=3.3V, -40°C to 105°C		66	88	μA
V _{BIAS} Shutdown Current	I _{SHDN_BIAS}	V _{BIAS} =5V, V _{IN} =5V, EN=0V, V _{OUT} =0V, -40°C to 85°C		8	12	μA
		V _{BIAS} =5V, V _{IN} =5V, EN=0V, V _{OUT} =0V, -40°C to 105°C			12	μA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VIN Shutdown Current	ISHDN_VIN	VIN=5V, EN=0V, VOUT=0V, -40°C to 85°C			0.004	10	uA
		VIN=5V, EN=0V, VOUT=0V, -40°C to105°C				20	μA
		VIN=3.3V, EN=0V, VOUT=0V, -40°C to 85°C			0.003	7	μA
		VIN=3.3V, EN=0V, VOUT=0V, -40°C to105°C				14	μA
		VIN=2.5V, EN=0V, VOUT=0V, -40°C to 85°C			0.002	6	μA
		VIN=2.5V, EN=0V, VOUT=0V, -40°C to105°C				12	μA
		VIN=1.8V, EN=0V, VOUT=0V, -40°C to 85°C			0.002	6	μA
		VIN=1.8V, EN=0V, VOUT=0V, -40°C to105°C				10	μA
		VIN=1.05V, EN=0V, VOUT=0V, -40°C to 85°C			0.001	4	μA
		VIN=1.05V, EN=0V, VOUT=0V, -40°C to105°C				8	μA
		VIN=0.6V, EN=0V, VOUT=0V, -40°C to 85°C			0.001	4	μA
		VIN=0.6V, EN=0V, VOUT=0V, -40°C to105°C				7	μA
EN Leakage Current	IEN_LKG	VEN=5.5V, -40°C to105°C				0.1	μA
EN Turn-on Threshold	VEN_ON	TA=25°C		1.2			V
EN Turn-off Threshold	VEN_OFF	TA=25°C				0.4	V
PG Leakage Current	IPG_LKG	VPG=5.0V, -40°C to105°C				0.5	μA
PG Output Low Voltage	VPG_LOW	VEN=0V, IPG=1mA				0.2	V
Integrate FET RON	RDS(ON)	VBIAS=EN=5V, IOUT=1A	VIN=5V, -40°C to 85°C		2.8	5.7	mΩ
			VIN=5V, -40°C to 105°C			6	mΩ
			VIN=3.3V, -40°C to 85°C		2.8	5.7	mΩ
			VIN=3.3V, -40°C to 85°C			6	mΩ
			VIN=0.6V, -40°C to 85°C		2.8	5.7	mΩ
			VIN=0.6V, -40°C to 85°C			6	mΩ
		VBIAS=EN=3.3V, IOUT=1A	VIN=3.3V, -40°C to 85°C		2.8	5.7	mΩ
			VIN=3.3V, -40°C to 105°C			6	mΩ
			VIN=2.5V, -40°C to 85°C		2.8	5.7	mΩ
			VIN=2.5V, -40°C to 85°C			6	mΩ
			VIN=0.6V, -40°C to 85°C		2.8	5.7	mΩ
			VIN=0.6V, -40°C to 85°C			6	mΩ
Discharge Resistance	RDIS	VIN=5V			200		Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Characteristics						
VOUT Rise Time	t _{rise}	R _L =10Ω, C _L =0.1μF, C _{SST} =0pF, V _{BIAS} =EN=5V	V _{IN} =5V	31		μs
			V _{IN} =1.05V	13		μs
			V _{IN} =0.6V	10		μs
		R _L =10Ω, C _L =0.1μF, C _{SST} =0pF, V _{BIAS} =EN=3.3V	V _{IN} =3.3V	24		μs
			V _{IN} =1.05V	12		μs
			V _{IN} =0.6V	9		μs
Turn On Delay	t _{d_ON}	R _L =10Ω, C _L =0.1μF, C _{SST} =0pF, V _{BIAS} =EN=5V	V _{IN} =5V	26		μs
			V _{IN} =1.05V	26		μs
			V _{IN} =0.6V	27		μs
		R _L =10Ω, C _L =0.1μF, C _{SST} =0pF, V _{BIAS} =EN=3.3V	V _{IN} =3.3V	26		μs
			V _{IN} =1.05V	26		μs
			V _{IN} =0.6V	27		μs
VOUT Fall Time	t _{fall}	R _L =10Ω, C _L =0.1μF, C _{SST} =0pF, V _{BIAS} =EN=5V	V _{IN} =5V	2.3		μs
			V _{IN} =1.05V	2.2		μs
			V _{IN} =0.6V	2.2		μs
		R _L =10Ω, C _L =0.1μF, C _{SST} =0pF, V _{BIAS} =EN=3.3V	V _{IN} =3.3V	2.4		μs
			V _{IN} =1.05V	2.3		μs
			V _{IN} =0.6V	2.3		μs
PG Turn On Time	t _{PG_ON}	R _L =10Ω, C _L =0.1μF, C _{SST} =0pF, V _{BIAS} =EN=5V	V _{IN} =5V	192		μs
			V _{IN} =1.05V	134		μs
			V _{IN} =0.6V	131		μs
		R _L =10Ω, C _L =0.1μF, C _{SST} =0pF, V _{BIAS} =EN=3.3V	V _{IN} =3.3V	132		μs
			V _{IN} =1.05V	122		μs
			V _{IN} =0.6V	119		μs
PG Turn Off Time	t _{PG_OFF}	R _L =10Ω, C _L =0.1μF, C _{SST} =0pF, V _{BIAS} =EN=5V	V _{IN} =5V	1.3		μs
			V _{IN} =1.05V	1.3		μs
			V _{IN} =0.6V	1.3		μs
		R _L =10Ω, C _L =0.1μF, C _{SST} =0pF, V _{BIAS} =EN=3.3V	V _{IN} =3.3V	1.5		μs
			V _{IN} =1.05V	1.5		μs
			V _{IN} =0.6V	1.5		μs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a highly effective 4-layer thermal conductivity test board of JEDEC 51-7 thermal measurement standard. V_{OUT} of DFN2×3-10 package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

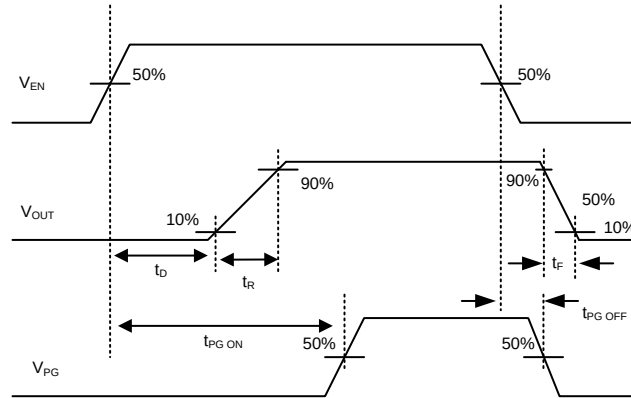
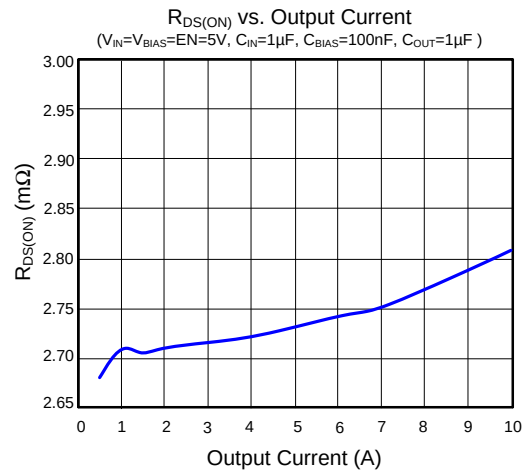
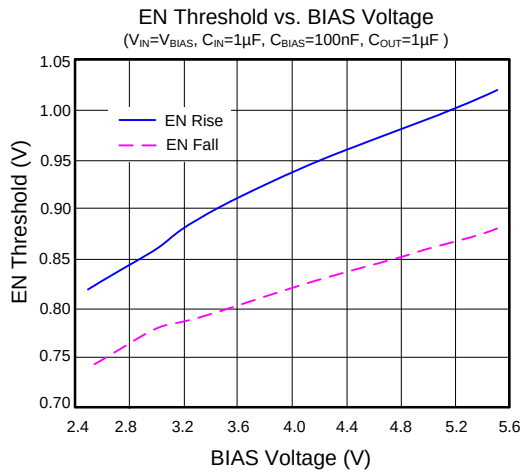
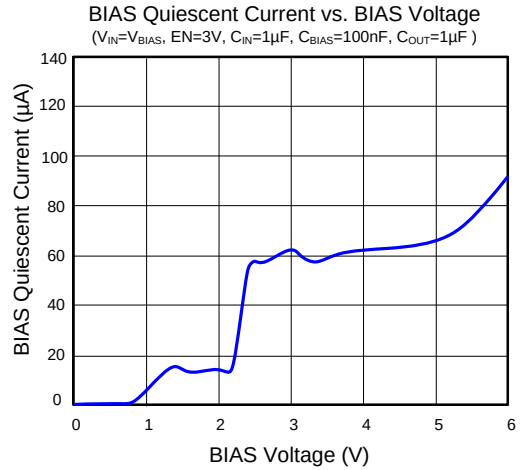
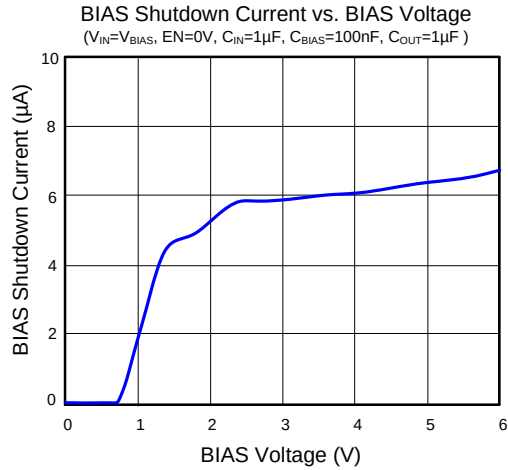
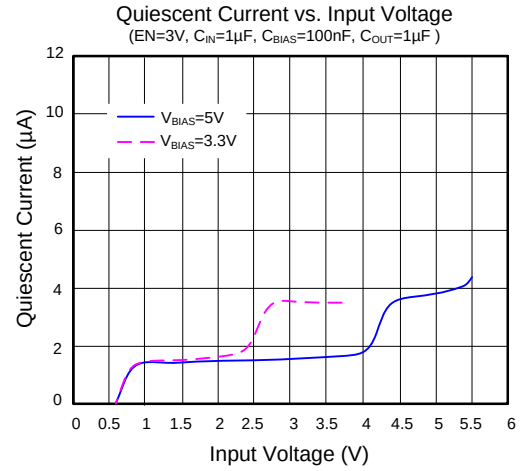
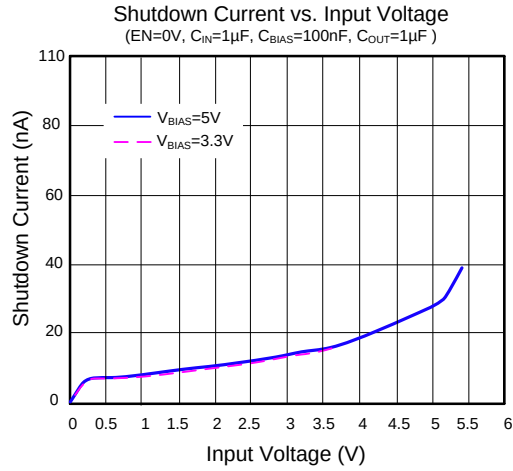
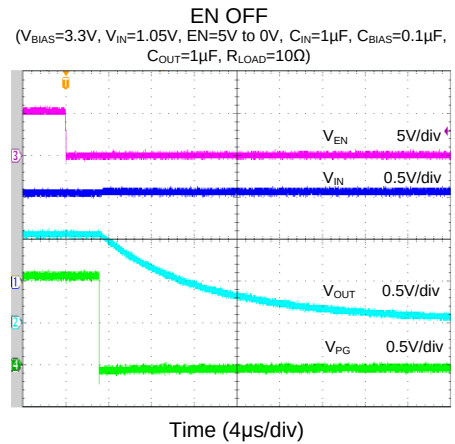
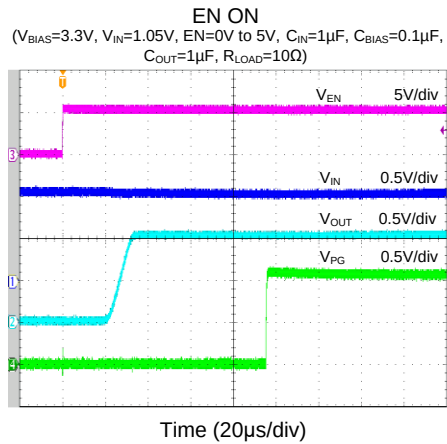
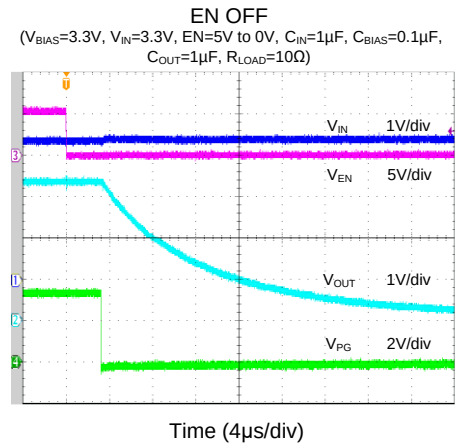
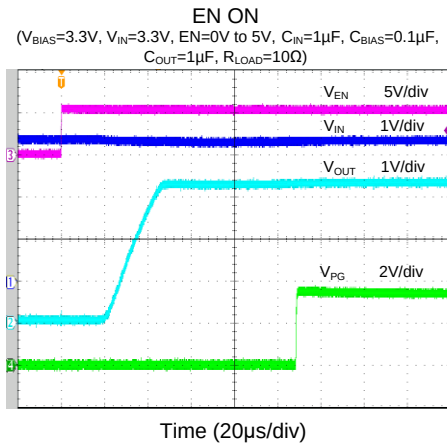
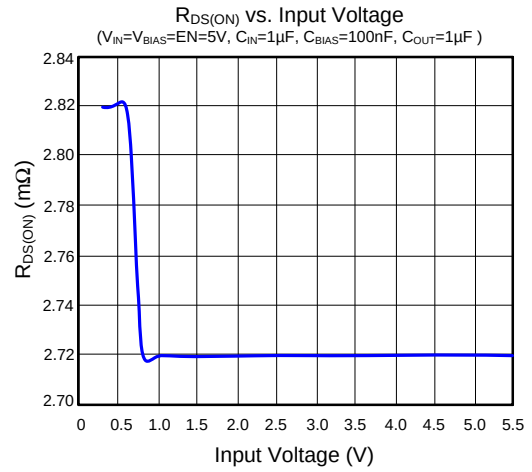
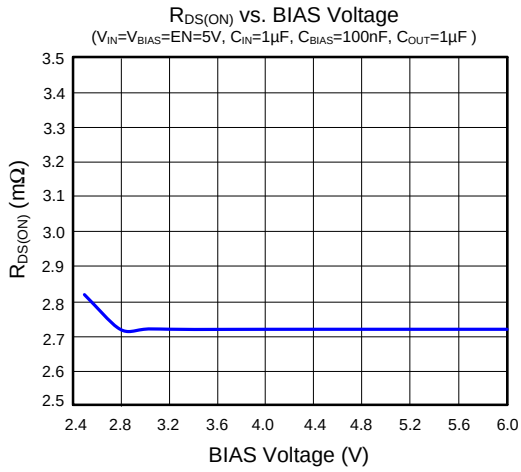
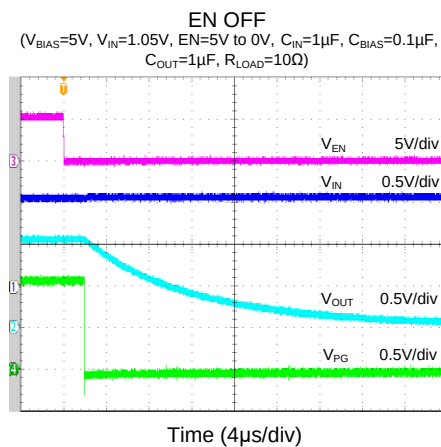
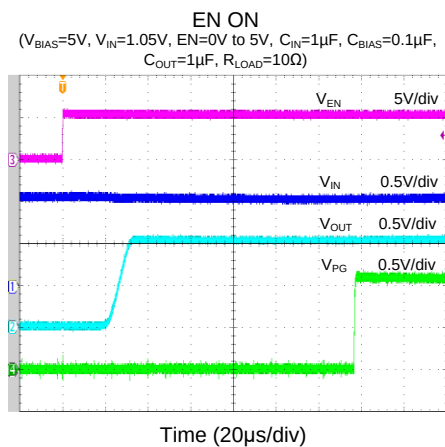
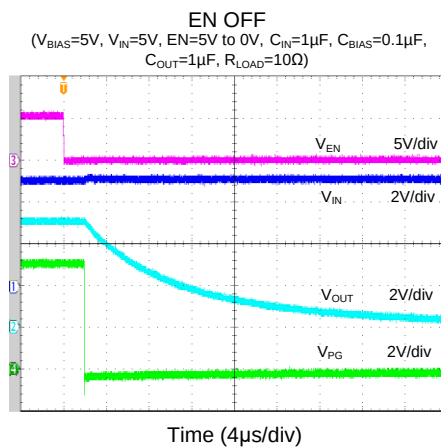
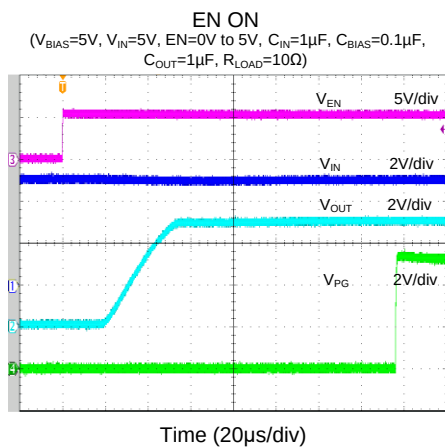


Figure 3. Timing Waveform

Typical Operating Characteristics







Application Information

The SY20810 is a single-channel load switch with a 2.8mΩ resistance. It features a controlled and adjustable turn-on mechanism and comes with an integrated PG indicator.

The device contains an N-channel MOSFET that can operate over an input voltage range of 0.6V to 5.5V and can support a maximum continuous current of 10A. The wide input voltage range and high current capability enable the device to be used in various applications. The low ON resistance of 2.8mΩ minimizes the voltage drop across the load switch, effectively reducing power loss.

The device's controlled rise time effectively minimizes inrush current induced by large bulk load capacitances, helping to reduce or eliminate power supply droop. The adjustable slew rate through SST offers design flexibility, allowing for a trade-off between inrush current and power-up timing requirements. The integrated Power Good (PG) indicator informs the system about the load switch status, facilitating seamless power sequencing.

In shutdown mode, the device exhibits a very low leakage current, preventing unnecessary leaks to downstream modules during standby. Additionally, the SY20810 features an optional on-chip 200Ω resistor for swift discharge of the output when the switch is disabled.

Input Pin:

It is recommended to include a capacitor between VIN and GND close to the device pins. This helps limit the voltage drop on the input supply induced by transient inrush currents when the switch is activated into a discharged capacitor at the load. Typically, a 1μF ceramic capacitor, CIN, is deemed sufficient. Higher values of CIN can be used to further reduce the voltage drop. A CIN to CL (load capacitance) ratio of 1 to 1 is recommended for minimizing VIN dip caused by inrush currents during startup.

Bias Capacitor:

For optimal decoupling performance, it is strongly recommended to include a decoupling capacitor of at least 0.1μF between the VBIAS pin and the ground pin. This capacitor should be placed close to the device as possible.

EN Pin:

The EN pin controls the state of the load switch. Asserting the pin high enables the switch. The minimum voltage that guarantees a logic high is 1.2V. This pin cannot be left floating and must be tied either high or low for proper functionality.

Output Delay Time Pin (SST):

The SY20810 features controlled rise time for effective inrush current control. The rise time is adjusted by connecting a capacitor to GND on the SST pin. Without any capacitor on SST, the rise time is at its minimum for the fastest timing. Equation 1 provides an approximate relationship between SST, VIN, and rise time when VBIAS is set to 5V. Rise time, as illustrated in Figure 3, is defined from the 10% to 90% measurement on VOUT.

$$t_R = (0.009 \times V_{IN} + 0.002) \times C_{SST} + 4.3 \times V_{IN} + 6 \quad (1)$$

Where:

- t_R is the rise time (in μs)
- V_{IN} is the input voltage (in V)
- C_{SST} is the capacitance value on the SST pin (in pF)

Table 1 contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where VIN and VBIAS are already in a steady state condition before the ON pin is asserted high.

Table 1. Rise Time vs. SST Capacitor

CSST (pF)	Rise Time (μs) at 25°C CL=1μF, CIN=1μF, RL=10Ω, VBIAS=5V				
	VIN=5V	VIN=3.3V	VIN=1.8V	VIN=1.05V	VIN=0.8V
0	27.2	20.1	13.32	9.28	8.16
220	37.6	26.8	17.3	11.76	10.04
470	48.1	34	21.4	14.2	12.2
1000	74	51.4	31.1	20.4	17.2
2200	134.8	92.4	55	35.1	28.5
4700	274.6	167.2	98.4	62	50.2
10000	485	324	186.8	117.6	95.2

Power Good (PG):

The SY20810 provides a Power Good (PG) output signal indicating that the pass FET gate is driven high, and the switch is on, with the On-resistance close to its final value (full load ready). The signal is active high and an open-drain output, capable of being connected to a voltage

source through an external pull-up resistor (RPU). This voltage source can be VOUT from the SY20810 or another external voltage. It's important to note that a valid output for PG requires VBIAS. Equation 2 outlines the approximate relationship between CSST, VIN, and PG turn-on time (tPG,ON) when VBIAS is set to 5V:

$$t_{PG,ON} = (0.0107 \times V_{IN} + 0.04) \times C_{SST} + 4.3 \times V_{IN} + 134 \quad (2)$$

Where:

- tPG,ON is the PG turn-on time (in μs)
- VIN is the input voltage (in V)
- CSST is the capacitance value on the CT pin (in pF)

Table 2 contains the PG turn-on time values measured on a typical device.

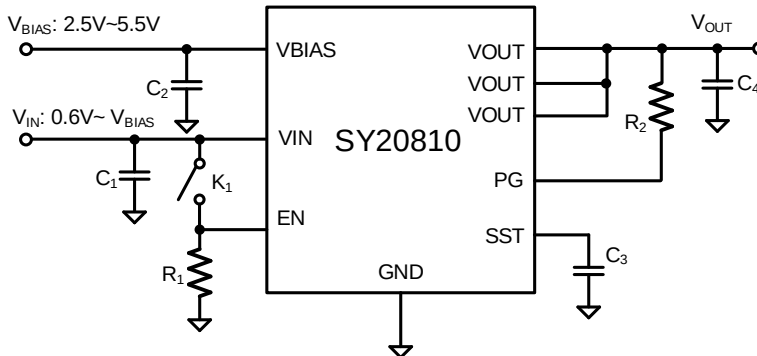
Table 2. PG Turn on Time vs. CT Capacitor

SST (pF)	Typical PG turn on time (μs) at 25°C CL=1 μF , CIN=1 μF , RL=10 Ω , VBIAS=5V, RPU=10k Ω				
	VIN=5V	VIN=3.3V	VIN=1.8V	VIN=1.05V	VIN=0.8V
0	155.4	148	140.2	137.2	137
220	178.2	166.4	155.2	150.4	150.2
470	201.2	185.2	170	163.4	163.0
1000	258	231.6	207.2	196.2	194.4
2200	395.2	343.6	295.6	273.6	268
4700	641	545	457	415	405
10000	1166	971	795	709	688

Power Supply Recommendations:

The device is designed to operate with a VBIAS range of 2.5V to 5.5V, and a VIN range of 0.6V to VBIAS. The supply must be well-regulated and placed as close to the device terminal as possible with the recommended 1 μF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. In the case where the power supply is slow to respond to a large load current step, additional bulk capacitance may also be required. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 μF may be sufficient.

Application Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
C ₁ , C ₄	1μF/50V, 0603, X5R	GRM31MR71H105K	Murata
C ₂	0.1μF/50V, 0603, X5R	GRM188R61H104K	
R ₁	1MΩ, 0603		
R ₂	10KΩ, 0603		

PCB Layout Guide:

For best performance of the SY20810, the following guidelines must be strictly followed:

1. Keep all power traces as short and wide as possible and use at least 2 ounce copper for all power traces.
2. Input and output capacitors should be placed close to the SY20810 and connected to the ground plane to reduce noise coupling and parasitic trace inductance.
3. The SST trace must be as short as possible to reduce parasitic capacitance.

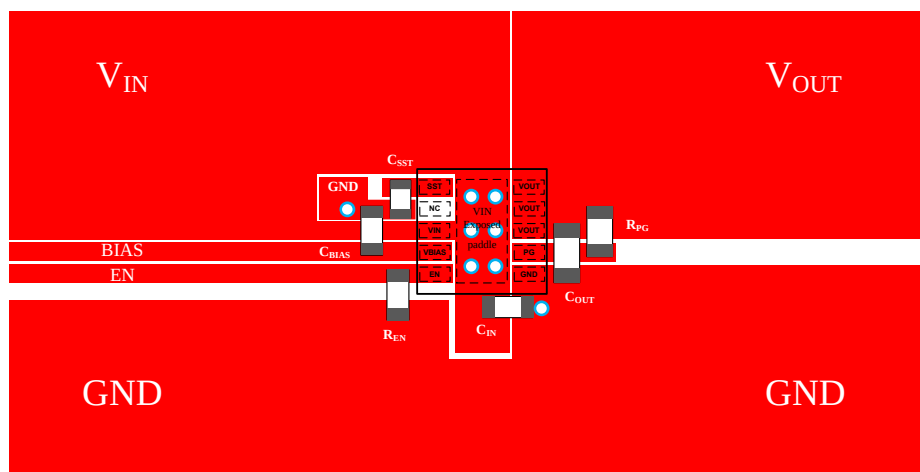
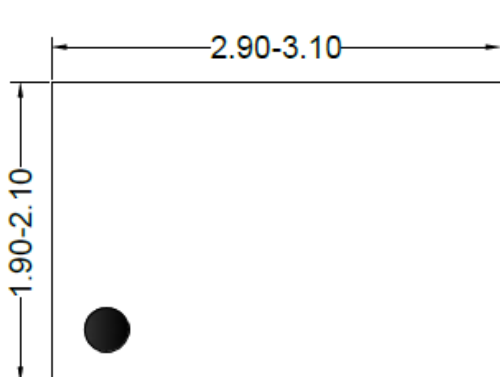
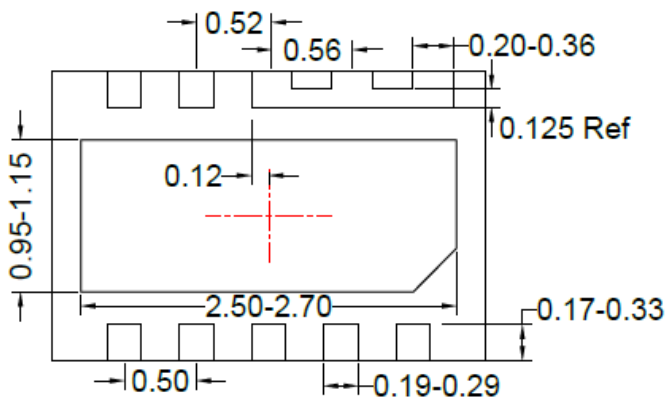


Figure 4. PCB Layout Suggestion

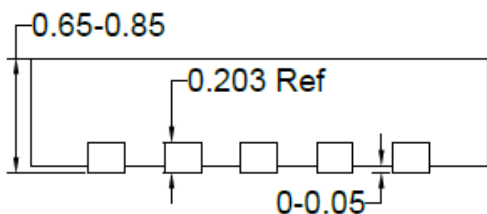
Package Outline Drawing



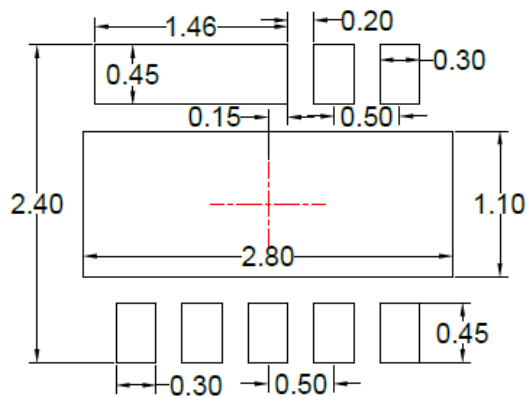
Top View



Bottom View



Front View

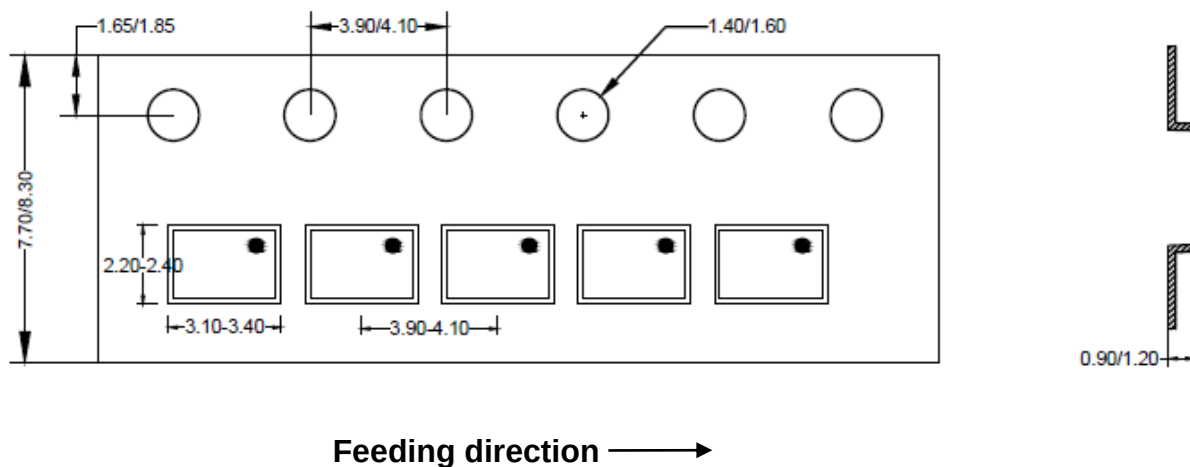


**Recommended PCB Layout
(Reference only)**

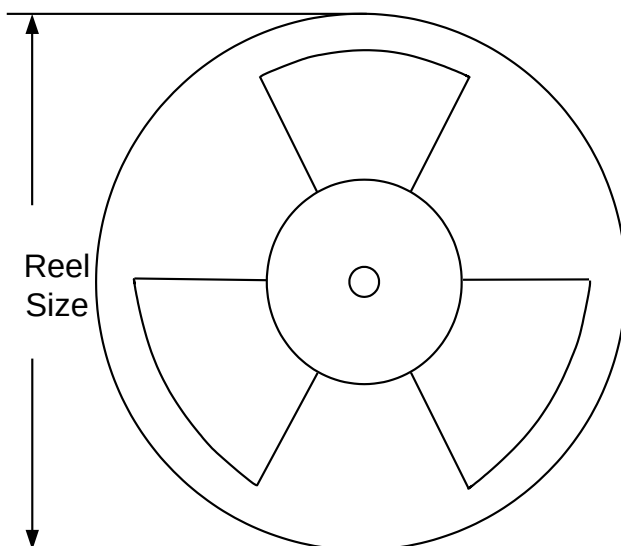
Notes: 1. All dimensions are in millimeters and exclude mold flash and metal burr.
2: The center of the PCB diagram refers to the chip center.

Taping & Reel Specification

DFN2×3 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN2×3-10	8	4	7"	400	160	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec. 08, 2023	Revision 1.0	Language improvements for clarity.
Aug.17, 2021	Revision 0.9	Initial Release

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