

Single-channel, Adjustable Voltage Monitor in Ultra-small Package

General Description

The SY28637A is a voltage monitor which operates from 1.7V to 6.5V and has a low quiescent current with an active-high push-pull output.

The SY28637A monitors voltage above 500mV with 1% threshold accuracy over temperature and provides a programmable delay time using external capacitors. The SY28637A offers an active-high enable input to power on and off the output. The SY28637A is ideal for power-supply sequencing, reset sequencing, and power-switching applications. Multiple devices can be cascaded for complex sequencing applications.

The SY28637A is fully specified over the $T_J = -40^{\circ}\text{C}$ to 125°C operating temperature range. The SY28637A is available in an ultra-small DFN1.45mm×1mm-6 pin package.

Features

- Adjustable Threshold Down to 500mV
- Operating Voltage: 1.7V to 6.5V
- Threshold Accuracy: 1% Over Temperature
- Capacitor-Adjustable Delay Time
- Active-High Enable Input
- Low Quiescent Current: 9 μA (Typical)
- External Enable Input
- Temperature Range: -40°C to 125°C
- Compact Package: DFN1.45×1.0-6

Applications

- DSPs, Microcontrollers and Microprocessors
- Notebook and Desktop Computers
- PDAs and Handheld Products
- Portable and Battery-Powered Products
- FPGAs and ASICs

Typical Application

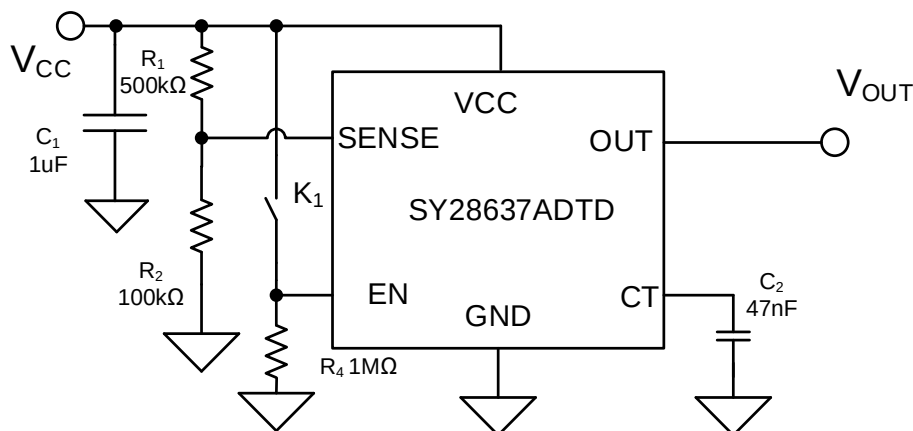


Figure 1. Schematic Diagram



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SY28637A

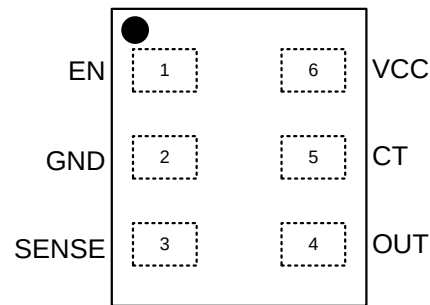
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY28637ADTD	DFN1.45×1-6 RoHS Compliant and Halogen Free	fxyz

Device code: f

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin NO.	I/O	Pin Description
CT	5	I	Capacitor-adjustable delay. The CT pin offers a user-adjustable delay time. Connecting this pin to a ground-referenced capacitor sets the delay time for SENSE rising above 0.5V to OUT asserting or EN asserting to OUT asserting. $t_{pd(r)}(s) = [C_{CT}(\mu F) \times 4] + 40\mu s$
EN	1	I	Active high input. Driving EN low makes OUT go low immediately, independent of V_{SENSE} . With V_{SENSE} already above V_{IT+} , drive EN high to make OUT go high after the capacitor-adjust delay time.
GND	2	-	Ground.
SENSE	3	I	This pin is connected to the monitored voltage using a external resistor divider. The output asserts after the capacitor-adjustable delay time when V_{SENSE} rises above 0.5V, and EN is asserted. The output de-asserts after a minimal propagation delay ($16\mu s$) when V_{SENSE} falls below $V_{IT+} - V_{HYS}$.
OUT	4	O	OUT is a push-pull output that is immediately driven low after V_{SENSE} falls below $(V_{IT+} - V_{HYS})$ or the EN input is low. OUT goes high after the capacitor-adjustable delay time when V_{SENSE} is greater than V_{IT+} and the EN pin is high.
VCC	6	I	Supply voltage input. Connect a 1.7V to 6.5V supply to VCC to power the device. Place a 0.1 μF ceramic capacitor close to this pin.

Block Diagram

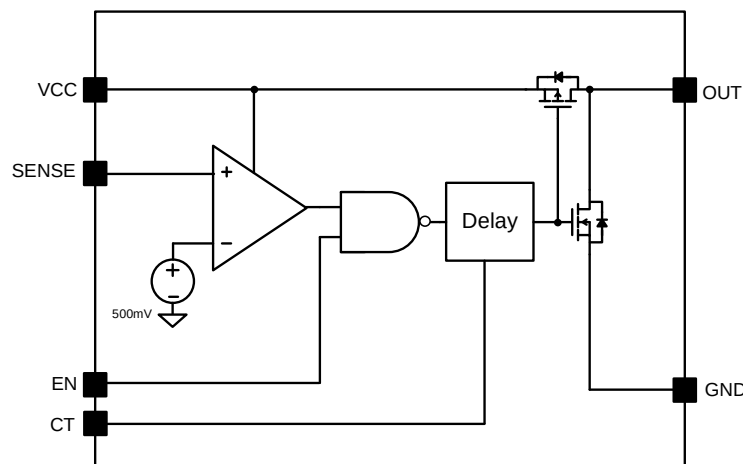


Figure 2. Block Diagram



Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VCC, EN, SENSE	-0.3	7	V
CT, OUT	-0.3	VCC+0.3	V
OUT Current	-10	+10	mA
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	125	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	293.8	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	165.1	
P _D Power Dissipation TA = 25°C	0.34	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VCC	1.7	6.5	V
OUT, CT, EN, SENSE	0	6.5	
OUT Current	0.0003	1	mA

Electrical Characteristics

Over the operating temperature range of T_J = -40°C to 125°C, and 1.7V < V_{CC} < 6.5V, typical values are at T_J = 25°C and V_{CC} = 3.3V. Unless otherwise noted. The values are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V _{CC}		1.7		6.5	V
Power on Reset Voltage	V _{POR}	V _{OL} (max) = 0.2V, I _{OUT} = 15μA (Note 4)		0.72		V
Supply Current (into the VCC pin)	I _{CC}	V _{CC} = 3.3V, T _A = 25°C, No load		9	12	μA
		V _{CC} = 3.3V, T _A = 125°C, No load		12	14	μA
		V _{CC} = 6.5V, T _A = 25°C, No load		11	13.5	μA
		V _{CC} = 6.5V, T _A = 125°C, No load		14	16	μA
Positive-going Input Threshold Voltage	V _{IT+}	V _{SENSE} rising, -40°C < T _J < 125°C	0.495	0.5	0.505	V
Hysteresis Voltage	V _{HYS}	V _{SENSE} falling		5		mV
SENSE Input Current	I _{SENSE}	V _{SENSE} = 0V to V _{CC} (Note 5)	-15		15	nA
CT Pin Charge Current	I _{CT}		260	310	360	nA
CT Pin Comparator Threshold Voltage	V _{CT}		1.18	1.238	1.299	V
CT Pin Down Resistance	R _{CT}			200		Ω
Low-level Input Voltage (EN/#EN pin)	V _{IL}				0.4	V
High-level Input Voltage (EN/#EN)	V _{IH}		1.4			V
Under Voltage Lockout	V _{UVLO}	V _{CC} falling, (Note 6)	1.3		1.7	V
EN/#EN Leakage		EN/#EN = V _{CC} or GND	-100		100	nA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low-level Output Voltage	V _{OL}	V _{CC} ≥ 1.2V, I _{SINK} = 90μA			0.3	V
		V _{CC} ≥ 2.25V, I _{SINK} = 0.5mA			0.3	V
		V _{CC} ≥ 4.5V, I _{SINK} = 1mA			0.4	V
High-level Output Voltage (push-pull)	V _{OH}	V _{CC} ≥ 2.25V, I _{SOURCE} = 0.5mA	0.8V _{CC}			V
		V _{CC} ≥ 4.5V, I _{SOURCE} = 1mA	0.8V _{CC}			V

Timing Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SENSE (rising) to OUT Propagation Delay	t _{PD(r)}	V _{SENSE} rising, C _{CT} = open		40		μs
		V _{SENSE} rising, C _{CT} = 0.047μF		190		ms
Sense (falling) to OUT Propagation Delay	t _{PD(f)}	V _{SENSE} falling	3	6	16	μs
Start-up Delay		(Note 7)		50		μs
EN Pin Minimum Pulse Duration	t _w		1			μs
EN Glitch Rejection	t _{EN_GLH}			100		ns
EN to OUT Delay Time (Output Disable)	t _{d_off}	EN de-asserted to output de-asserted		200		ns
EN to VOUT Delay Time	t _{d_ct}	EN asserted to output asserted delay, C _{CT} =open		20		μs
		EN asserted to output asserted delay, C _{CT} = 0.047uF		190		ms

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

Note 4: The lowest supply voltage (V_{CC}) at which output is active (OUT is low); t_{r_VCC} > 15 μs/V. Below V_{POR}, the output cannot be determined.

Note 5: Specified by design.

Note 6: When V_{CC} falls below the UVLO threshold, the output de-asserts (OUT goes low). Below V(POR), the output cannot be determined.

Note 7: During power on, V_{CC} must exceed 1.7V for at least 50μs (plus propagation delay time, t_{PD(r)}) before the output is in the correct state.

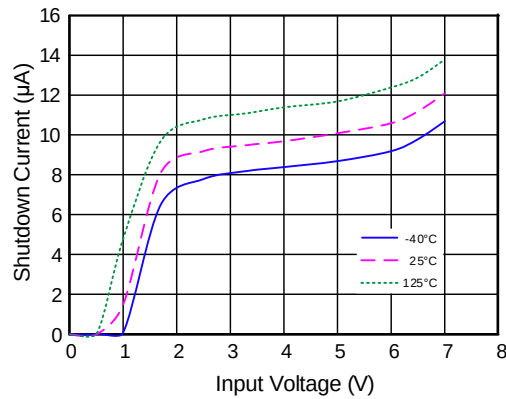


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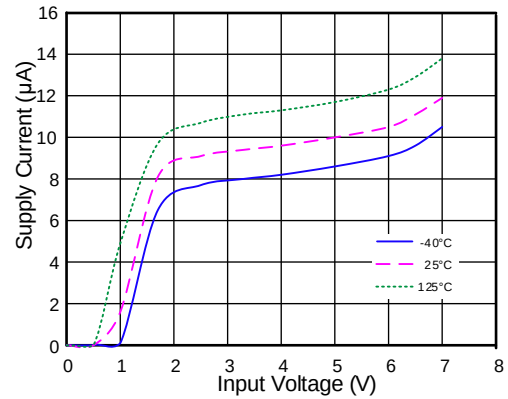
SY28637A

Typical Operating Characteristics

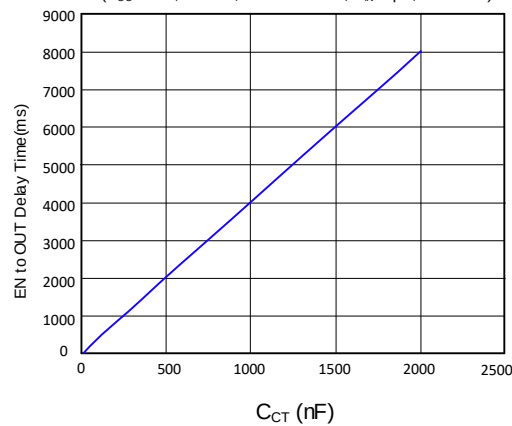
Shutdown Current vs. Input Voltage
($EN=0V$, $SENSE=0V$, $C_N=1\mu F$, $CT=Null$)



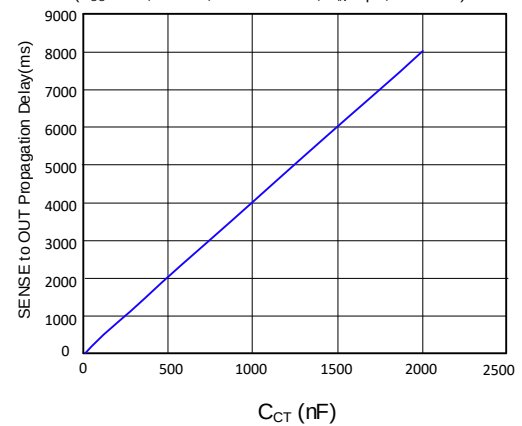
Supply Current vs. Input Voltage
($EN=V_{CC}$, $SENSE=0.6V$, $C_N=1\mu F$, $CT=Null$)



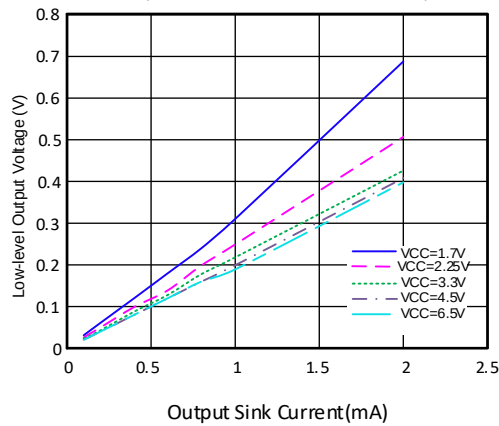
EN (Rising) to OUT Delay Time vs. C_{CT}
($V_{CC}=3.3V$, $EN=3V$, $SENSE=0.6V$, $C_N=1\mu F$, Null Load)



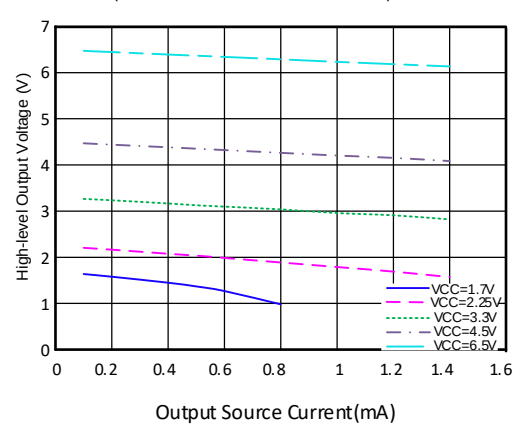
SENSE (Rising) to OUT Propagation Delay vs. C_{CT}
($V_{CC}=3.3V$, $EN=3V$, $SENSE=0.6V$, $C_N=1\mu F$, Null Load)



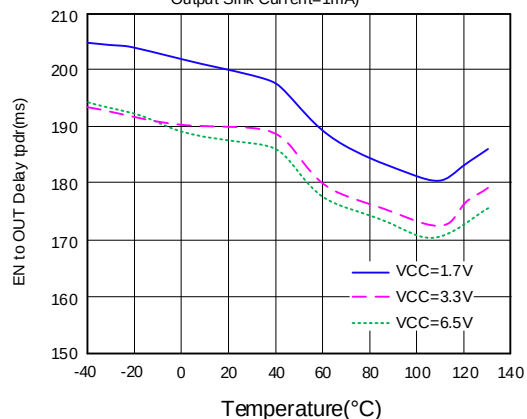
Output Voltage Low vs. Output Sink Current
($EN=0V$, $SENSE=0V$, $C_N=1\mu F$, $CT=Null$)



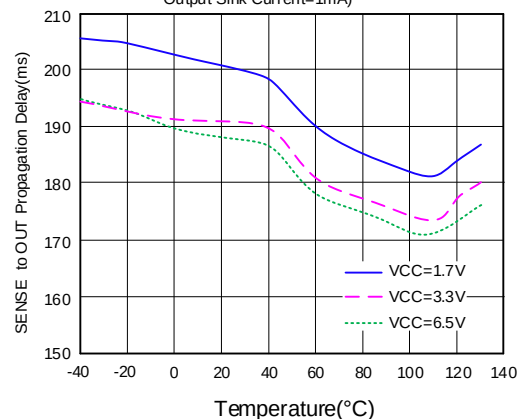
High-level output voltage vs. Output Source Current
($EN=3V$, $SENSE=3V$, $C_N=1\mu F$, $CT=Null$)



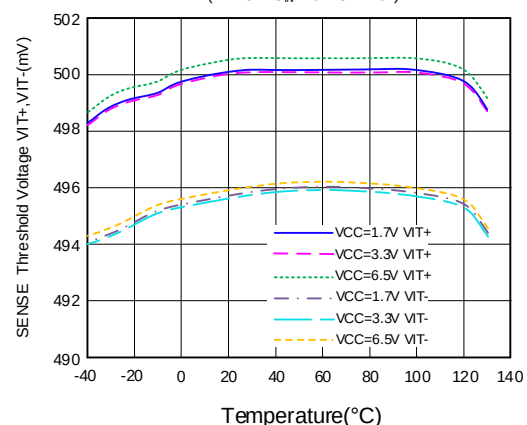
EN to OUT Delay vs. Temperature
(EN=3V, SENSE=0V to 0.6V, C_N=1μF, CT=47nF, Output Sink Current=1mA)



SENSE to OUT Propagation Delay vs. Temperature
(EN=3V, SENSE=0V to 0.6V, C_N=1μF, CT=47nF, Output Sink Current=1mA)

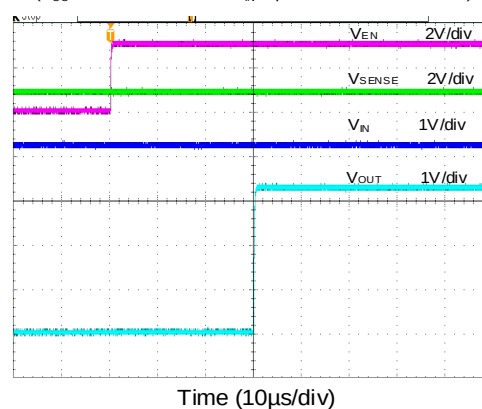


SENSE Threshold Voltage vs. Temperature
(EN=3V C_N=1μF CT=Null)



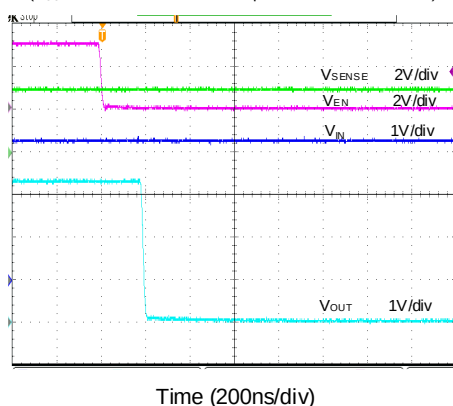
Startup from Enable

(V_{CC}=3.3V, EN=0V to 3V, C_N=1μF, SENSE=3V, CT=Null)



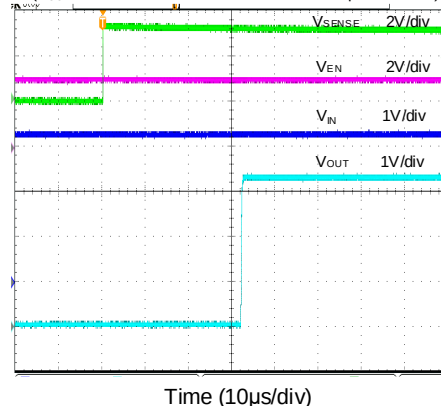
Shutdown from Enable

(V_{CC}=3.3V, EN=3V to 0V, C_N=1μF, SENSE=3V, CT=Null)



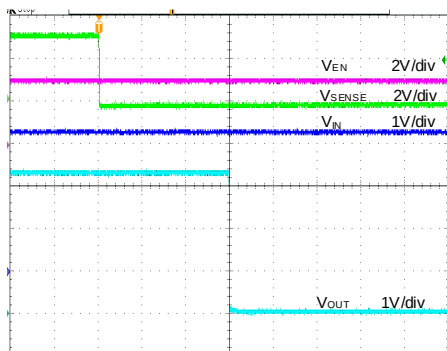
Startup from SENSE

(V_{CC}=3.3V, EN=3V, SENSE=0V to 3V, C_N=1μF, CT=Null)



Shutdown from SENSE

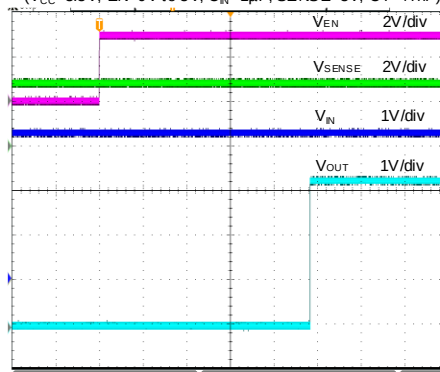
($V_{CC}=3.3V$, $EN=3V$, $SENSE=3V$ to $0V$, $C_N=1\mu F$, $CT=Null$)



Time (2μs/div)

Startup from Enable

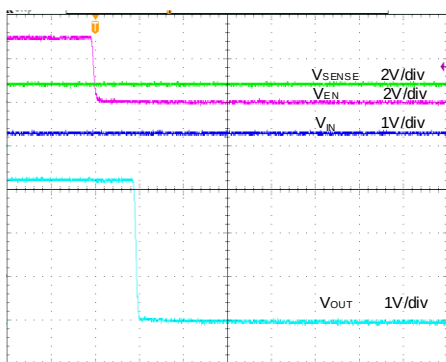
($V_{CC}=3.3V$, $EN=0V$ to $3V$, $C_N=1\mu F$, $SENSE=3V$, $CT=47nF$)



Time (40ms/div)

Shutdown from Enable

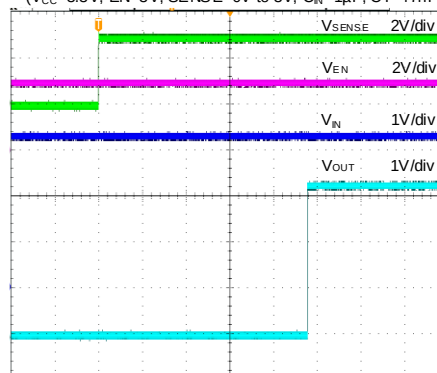
($V_{CC}=3.3V$, $EN=3V$ to $0V$, $C_N=1\mu F$, $SENSE=3V$, $CT=47nF$)



Time (200ns/div)

Startup from SENSE

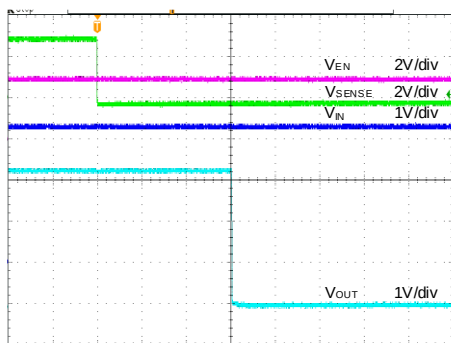
($V_{CC}=3.3V$, $EN=3V$, $SENSE=0V$ to $3V$, $C_N=1\mu F$, $CT=47nF$)



Time (40ms/div)

Shutdown from SENSE

($V_{CC}=3.3V$, $EN=3V$, $SENSE=3V$ to $0V$, $C_N=1\mu F$, $CT=47nF$)



Time (2μs/div)



Overview

The SY28637A operates from 1.7V to 6.5V and features low quiescent current with an active-high push-pull output.

The SY28637A monitors voltage above 500mV with 1% threshold accuracy over temperature, and provides a programmable delay time using an external capacitor. The SY28637A offers an active-high enable input to power on and off the output. The SY28637A is ideal for power-supply sequencing, reset sequencing, and power-switching applications. Multiple devices can be cascaded for complex sequencing applications.

The SY28637A is available in an ultra-small DFN1.45×1-6 package and is fully specified over the $T_J = -40^{\circ}\text{C}$ to 125°C operating temperature range.

Table 1. SY28637ADTD Truth Table

CONDITIONS		OUTPUT	STATUS
ENABLE = high	SENSE < VIT+	OUT = low	Output not asserted
ENABLE = low	SENSE < VIT+	OUT = low	Output not asserted
ENABLE = low	SENSE > VIT+	OUT = low	Output not asserted
ENABLE = high	SENSE > VIT+	OUT = high	Output asserted after delay

Timing Diagram

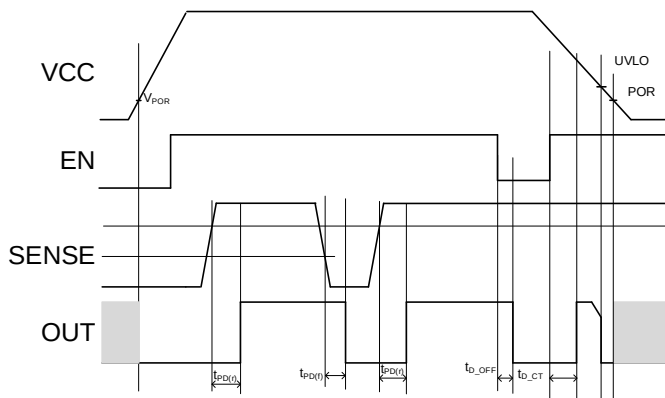
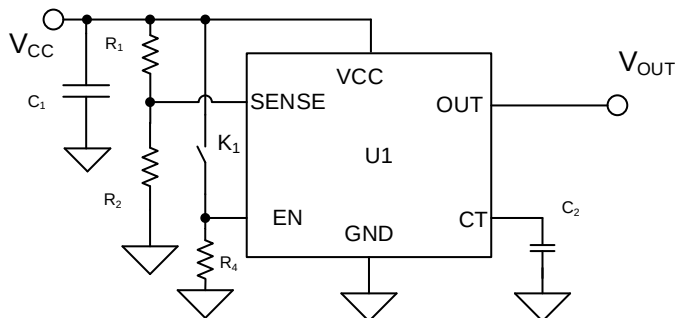


Figure 3. SY28637A Timing Diagram

Application Information

Schematic





BOM List

Reference Designator	Description	Part Number	Manufacturer
U1		SY28637ADTD	
C1	1μF/50V, 0603, X5R	GRM188R61H105K	Murata
C2	47nF/25V, 0603, X5R	GRM188R71H473K	Murata
R1	500kΩ, 0603		
R2	100kΩ, 0603		
R4	1MΩ, 0603		

Input Pin (SENSE)

The SENSE input pin can monitor a system voltage greater than 0.5V. If the voltage on the SENSE pin reaches V_{IT+} , and ENABLE is high, the output is asserted after the capacitor-adjustable delay time elapses. The output is de-asserted when the voltage on the SENSE pin falls below $(V_{IT+} - V_{hys})$. The comparator has a built-in hysteresis to ensure noise free output assertions and de-assertions. Although not required in most cases, using a 1nF to 10nF bypass capacitor at the SENSE input for noisy applications to reduce sensitivity to transients and parasitic layout is recommended. Equation 1 can be used to determine the target threshold voltage:

$$V_{TARGET} = (1 + R1/R2) \times 0.5 \text{ (V)} \quad (1)$$

Output Delay Time Pin (CT)

The OUT delay time can be adjusted by adding an external capacitor between the CT pin and ground. If the CT pin is floating, the device uses a delay of 40μs. The adjustable delay time can be determined using Equation 2:

$$t_{pd(r)} \text{ (s)} = [C_{CT} \text{ (}\mu\text{F)} \times 4] + 40 \mu\text{s} \quad (2)$$

The reset delay time is determined by the time it takes for an on-chip, precision 310nA current source to charge the external capacitor to 1.24V. When $SENSE > V_{IT+}$ and ENABLE is high, the internal current source is enabled and starts charging the external capacitors. The corresponding OUT will be asserted when the CT voltage across a capacitor reaches 1.24V. Note that a ceramic capacitor is recommended and that stray capacitance around this pin may cause errors in the reset delay time.

Output pin (OUT)

For typical applications, the output is connected to the processor's reset/enable input (DSP, CPU, FPGA, ASIC, etc.) or to a voltage regulator's input.

The SY28637A integrates push-pull output. This configuration doesn't require pull-up resistors, saving space on the board. However, all the interface logic levels must be examined for compatibility.

Enable Function

An external logic signal from processors can assert enable input to turn the output on or off.

The SY28637A offers an active-high enable input (ENABLE). Driving ENABLE high forces OUT high. The 0.4V (maximum) low and 1.4V (minimum) high allows the ENABLE input to be driven from a 1.5V or higher system supply.

Driving ENABLE high for the SY28637A device with $V_{SENSE} > V_{IT+}$ makes OUT go high after the capacitor-adjustable delay time.

PCB Layout Guide

For the best performance of the SY28637ADTD, the following guidelines must be followed:

- Keep all power traces as short and wide as possible and use at least 1-ounce copper for all power traces.
- Place a ground plane under all circuitry to lower resistance and inductance and improve DC and transient performance.
- Place the VCC decoupling capacitor close to the device.
- Avoid using long traces for the VCC supply node. The VCC capacitor (CVCC) and parasitic inductance from the supply to the capacitor can form an LC tank and create ringing with peak voltages above the maximum VCC voltage.
- Place the input and output capacitors close to the device and connect them to the ground plane to reduce noise coupling.

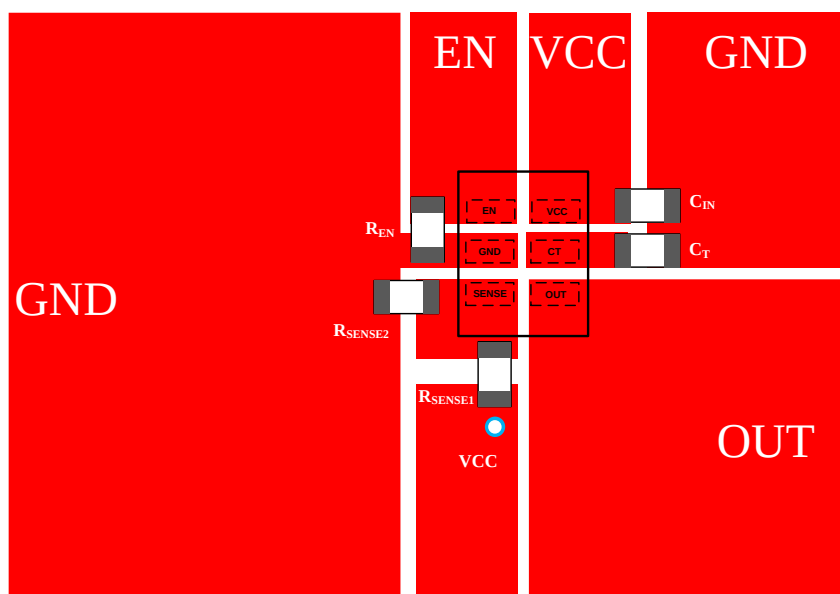
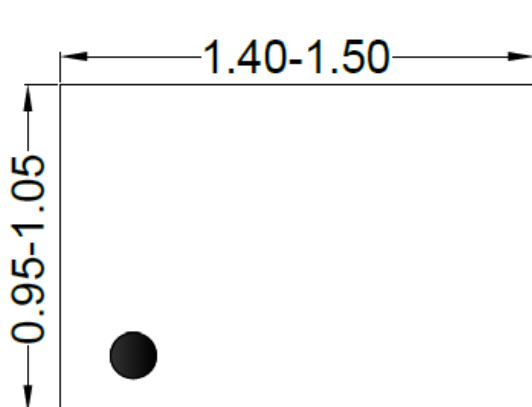
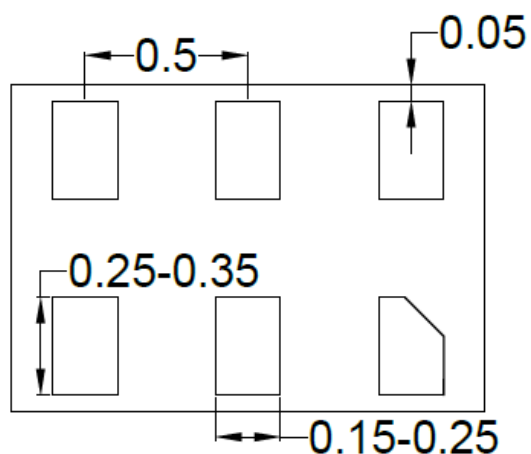


Figure 4. PCB Layout Suggestion

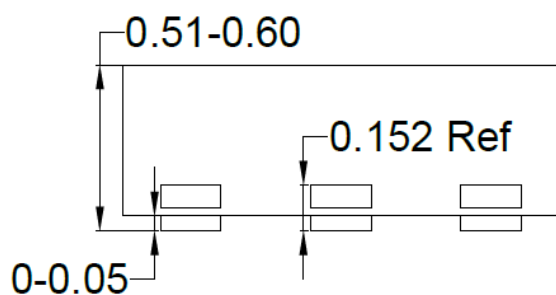
DFN1.45×1-6 Package Outline Drawing



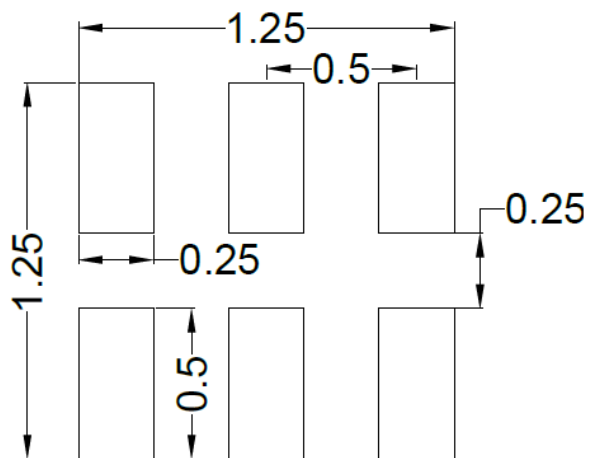
Top View



Bottom View



Side View

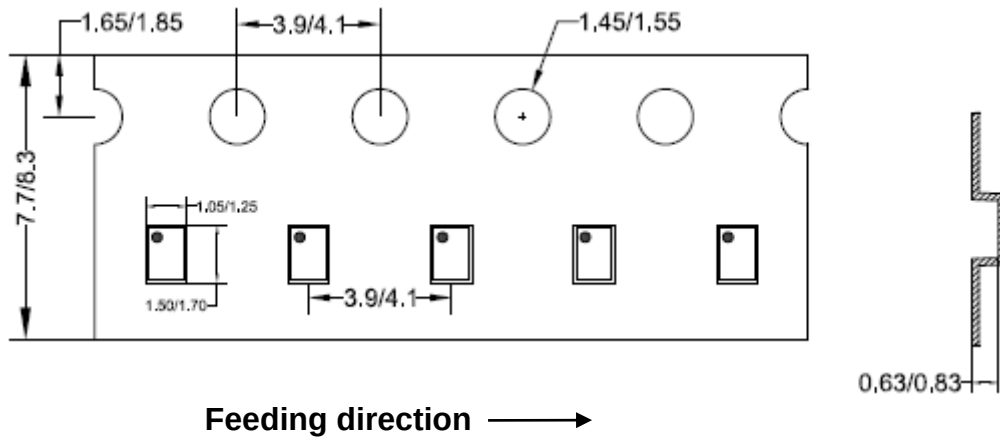


Recommended PCB Layout
(Reference only)

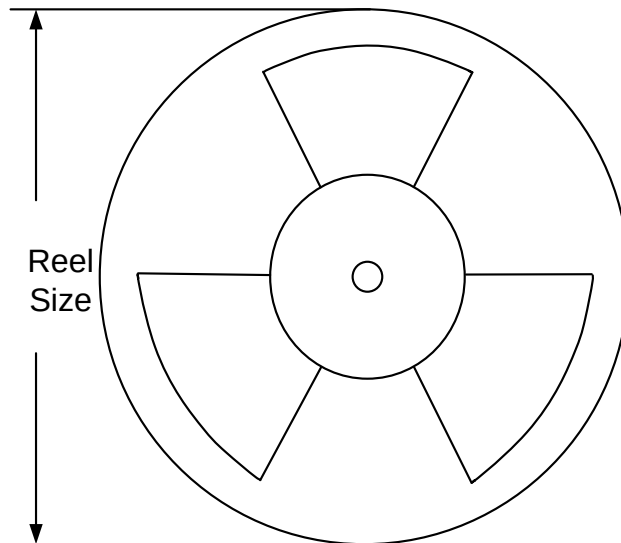
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Information

Tape Dimensions and Pin1 Orientation



Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.45×1	8	4	7"	400	160	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
July 03, 2025	Revision 1.0A	1. The logic gate in the Block Diagram changed from AND gate to NAND gate (Page 2) 2. Language improvements for clarity.
Oct. 09, 2023	Revision 1.0	Production Release
Oct. 09, 2022	Revision 0.9	Initial Risk Production Release

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