

MOSFET - Power, Single N-Channel, STD Gate, μ 8FL

40 V, 4.9 m Ω , 66 A

NVTFWS4D9N04XM

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (3.3 x 3.3 mm) for Compact Design
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Motor Drive
- Battery Protection
- Synchronous Rectification

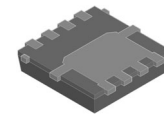
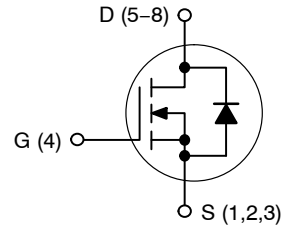
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	40	V
Gate-to-Source Voltage	DC V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	66
		$T_C = 100^\circ\text{C}$	47
Power Dissipation	P_D	38	W
Continuous Drain Current $R_{\theta JA}$	I_D	$T_A = 25^\circ\text{C}$	19
		$T_A = 100^\circ\text{C}$	13
Pulsed Drain Current	I_{DM}	265	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	32	A
Single Pulse Avalanche Energy ($I_{PK} = 32\text{ A}$)	E_{AS}	68	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

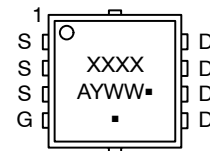
$V_{(BR)DSS}$	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
40 V	4.9 m Ω @ $V_{GS} = 10\text{ V}$	66 A

N-CHANNEL MOSFET



WDFNW8
(μ 8FL)
CASE 515AN

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVTFWS4D9N04XM

THEMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	3.91	°C/W
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{\theta JA}$	48.3	

- Surface-mounted on FR4 board using 650 mm², 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25°C		15		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, T_J = 25^\circ\text{C}$			1	μA
		$V_{DS} = 40\text{ V}, T_J = 125^\circ\text{C}$			100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}, T_J = 25^\circ\text{C}$		4.32	4.9	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 30\text{ }\mu\text{A}, T_J = 25^\circ\text{C}$	2.5	3.0	3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 30\text{ }\mu\text{A}$		-7.3		mV/°C
Forward Trans-conductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 10\text{ A}$		44		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		673		pF
Output Capacitance	C_{OSS}			433		
Reverse Transfer Capacitance	C_{RSS}			9		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DD} = 32\text{ V}; I_D = 30\text{ A}$		10.6		nC
Threshold Gate Charge	$Q_{G(TH)}$			2		
Gate-to-Source Charge	Q_{GS}			3.2		
Gate-to-Drain Charge	Q_{GD}			2.1		
Gate Resistance	R_G	$f = 1\text{ MHz}$		1.6		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 32\text{ V},$ $I_D = 30\text{ A}, R_G = 0\text{ }\Omega$		11.3		ns
Rise Time	t_r			4		
Turn-Off Delay Time	$t_{d(OFF)}$			17.1		
Fall Time	t_f			3.7		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}, T_J = 25^\circ\text{C}$		0.81	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 10\text{ A}, T_J = 125^\circ\text{C}$		0.66		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = 30\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 32\text{ V}$		23		ns
Charge Time	t_a			9		
Discharge Time	t_b			14		
Reverse Recovery Charge	Q_{RR}			9.5		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NVTFWS4D9N04XM

TYPICAL CHARACTERISTICS

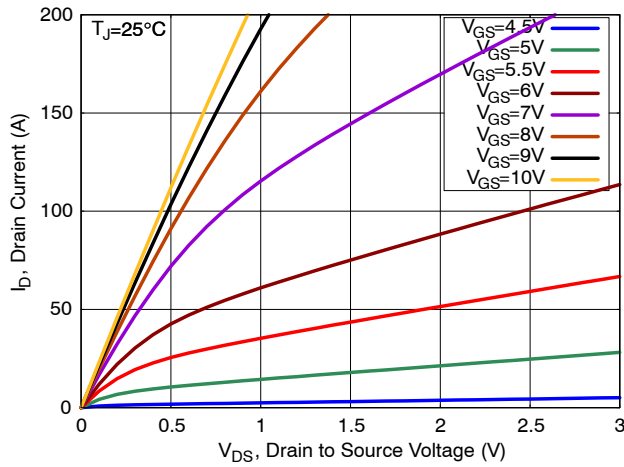


Figure 1. On-Region Characteristics

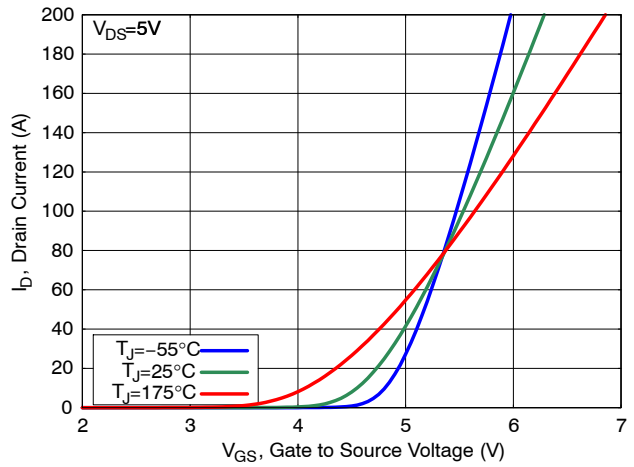


Figure 2. Transfer Characteristics

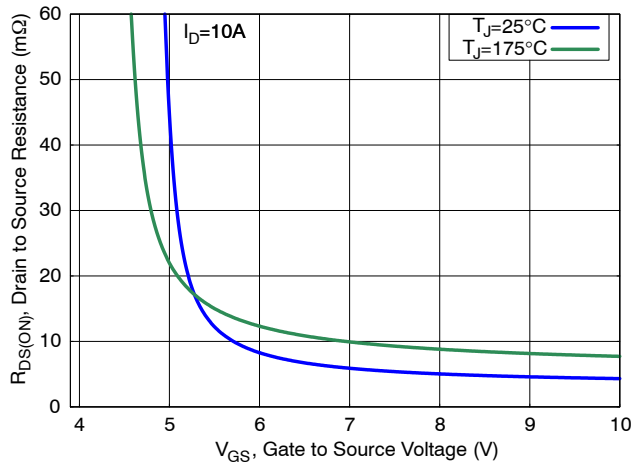


Figure 3. On-Resistance vs. Gate Voltage

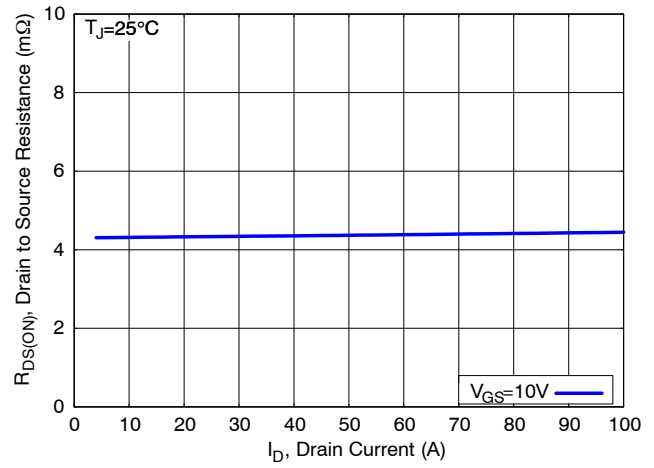


Figure 4. On-Resistance vs. Drain Current

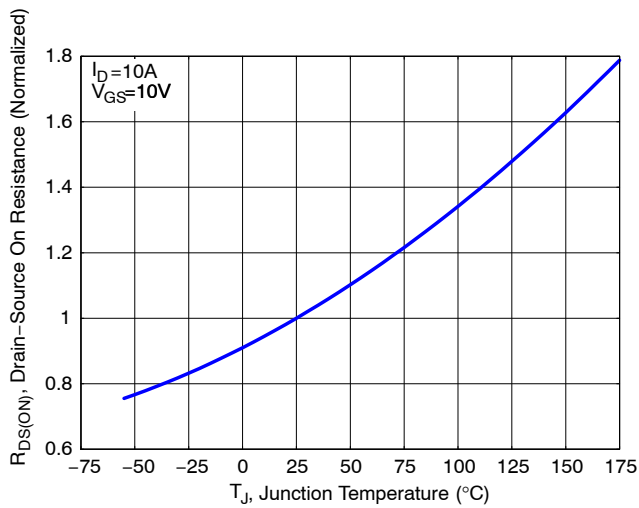


Figure 5. Normalized ON Resistance vs. Junction Temperature

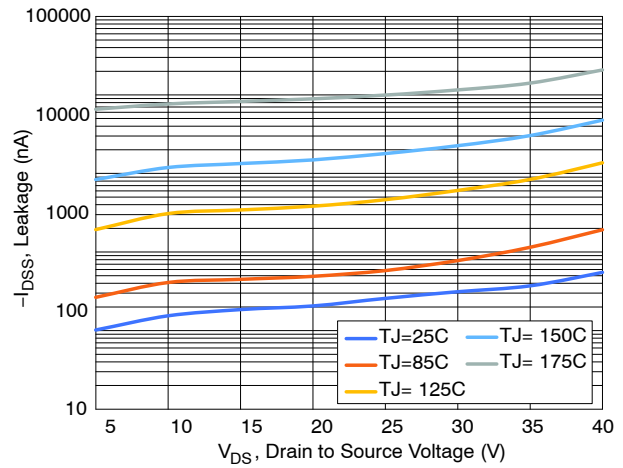


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVTFWS4D9N04XM

TYPICAL CHARACTERISTICS

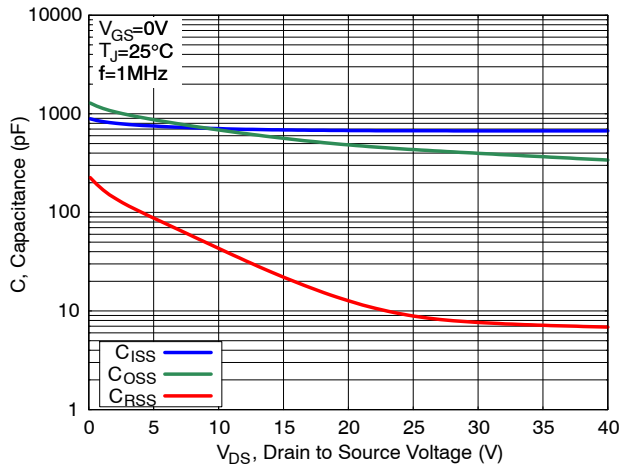


Figure 7. Capacitance Characteristics

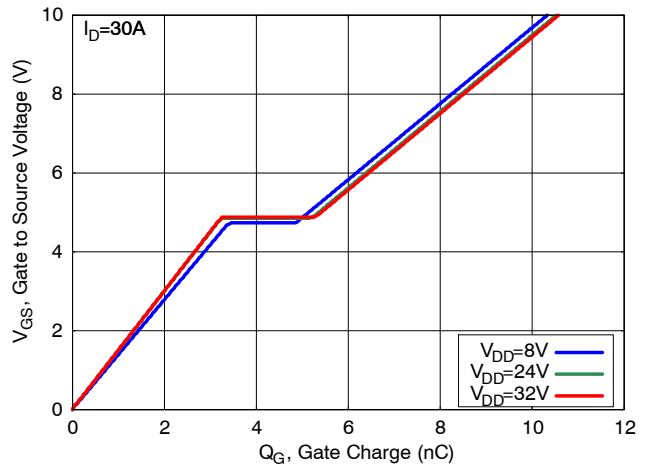


Figure 8. Gate Charge Characteristics

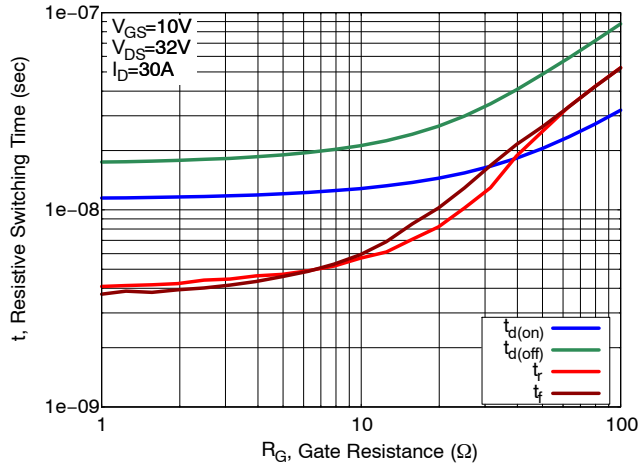


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

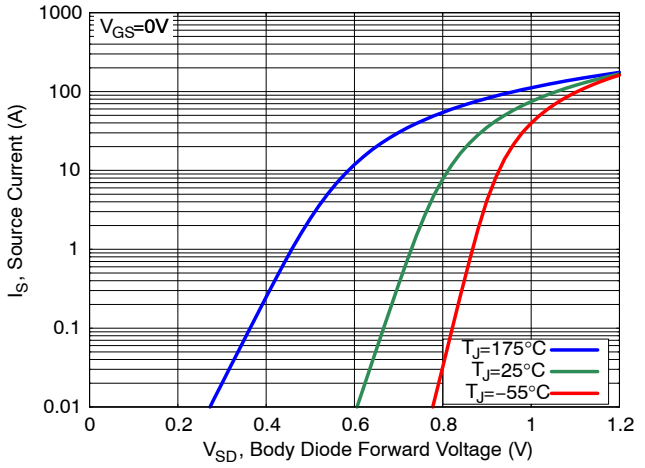


Figure 10. Diode Forward Characteristics

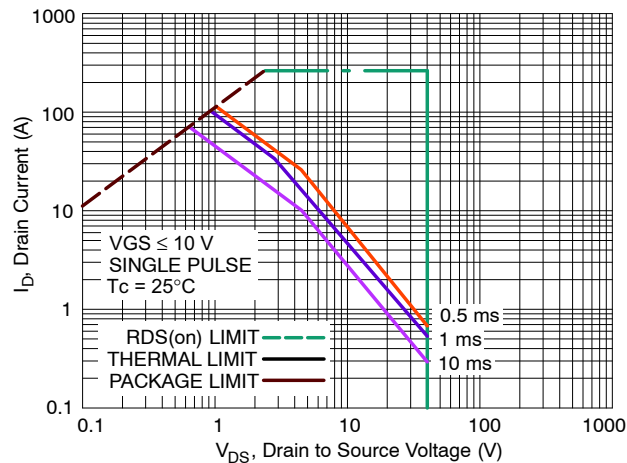


Figure 11. Safe Operating Area (SOA)

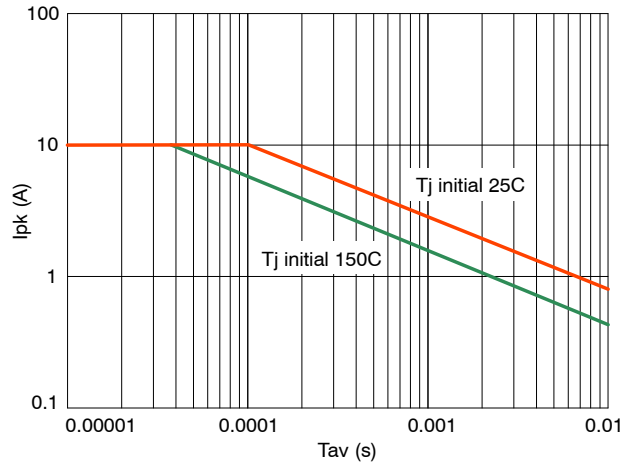


Figure 12. Avalanche Current vs. Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

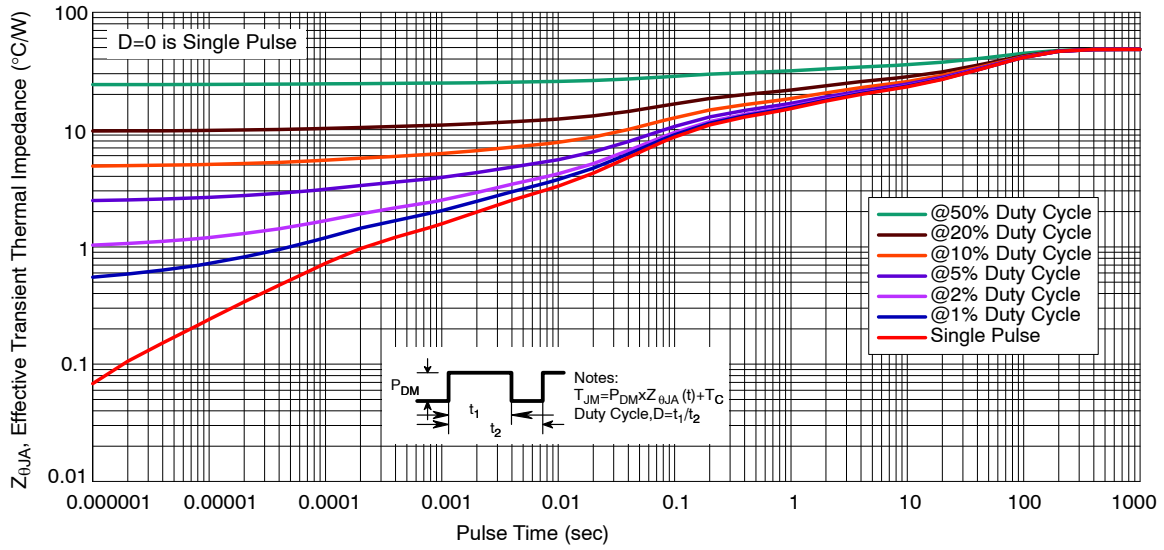


Figure 13. Transient Thermal Response

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVTFWS4D9N04XMTAG	4D9W	WDFNW8 3.3x3.3, 0.65P (Full-Cut μ 8FL WF) (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

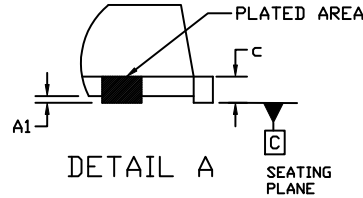
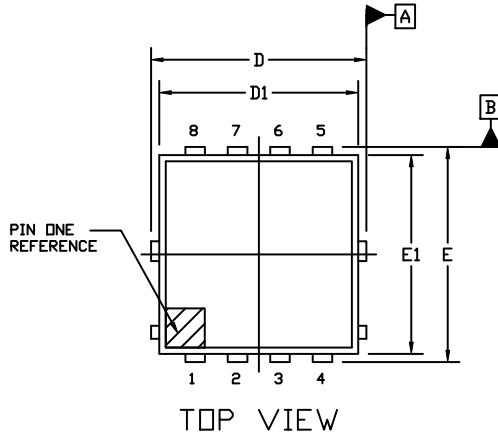
NVTFWS4D9N04XM

PACKAGE DIMENSIONS

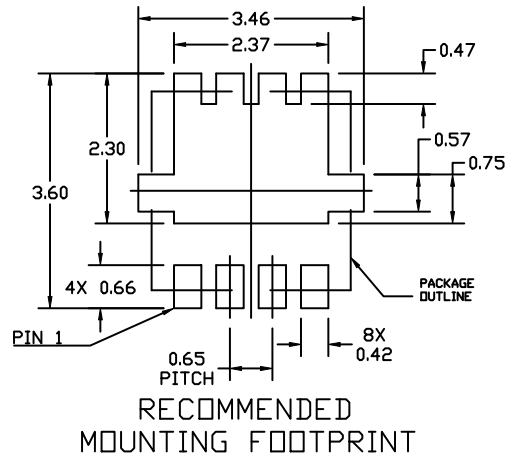
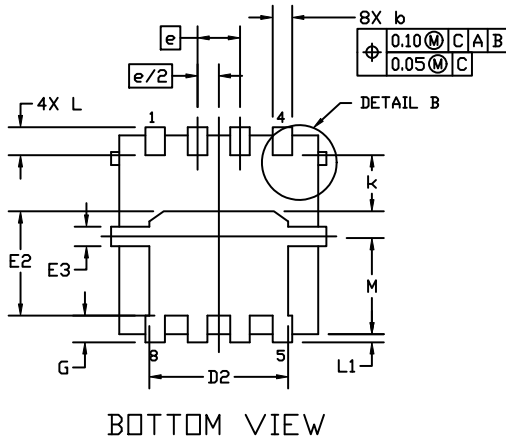
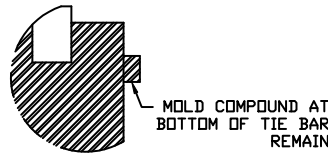
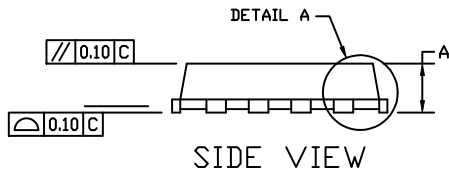
WDFNW8 3.3x3.3, 0.65P (Full-Cut μ 8FL WF) CASE 515AN ISSUE O

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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