AiPTS2102
2-Bit Bidirectional Level-Shifting, Voltage-Level Translator

Product Specification

Specification Revision History：

Version	Date	Description
2021-04-A1	2021-04	New
2023-08-A2	2023-08	Add order information
2024-05-B1	2024-05	Modify the content; Update the template

1、General Description

The AiPTS2102 is a 2-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 2-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both supplies can be supplied at any voltage between 1.65V and 5.5V. This flexibility makes the device suitable for translating between any of the voltage nodes (1.8V, 2.5V, 3.3V and 5.0V). Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$.

A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Features:

- Wide supply voltage range:
  $V_{CC(A)}$: 1.65V to 5.5V
  $V_{CC(B)}$: 1.65V to 5.5V
- Maximum data rates: 50Mbps
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5V
- Specified from -40℃ to +85℃
- Packaging information: QFN8

Ordering Information:

Reel packing specifications:

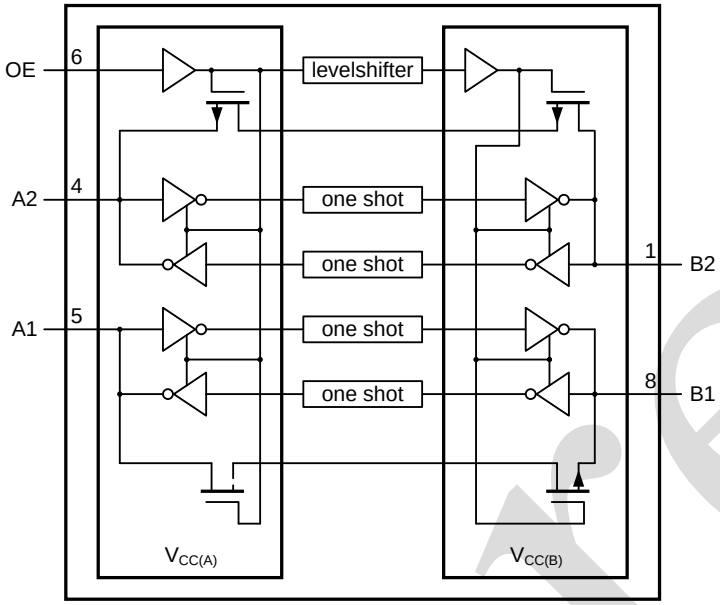
Type number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiPTS2102QH8.TR	QFN8	DKXX	3000CS/reel	30000PCS/box	Dimensions of plastic enclosure: 1.4mm×1.2mm Pin spacing: 0.4mm

Note 1: "XX" refers to variable content, meaning year and package batch serial number.

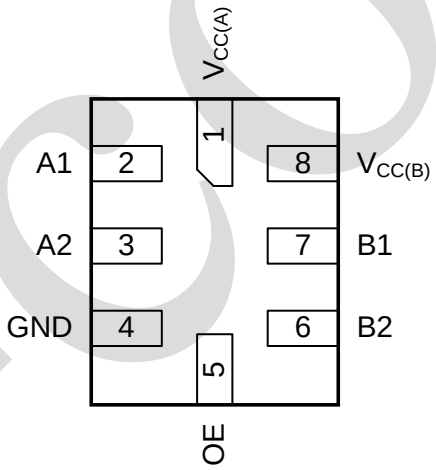
Note 2: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram



2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	$V_{CC(A)}$	supply voltage A
2	A1	data input or output (referenced to $V_{CC(A)}$)
3	A2	data input or output (referenced to $V_{CC(A)}$)
4	GND	ground (0V)
5	OE	output enable input (active HIGH; referenced to $V_{CC(A)}$)
6	B2	data input or output (referenced to $V_{CC(B)}$)
7	B1	data input or output (referenced to $V_{CC(B)}$)
8	$V_{CC(B)}$	supply voltage B

2.4、Function table

Supply voltage		Input	Input/Output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	An	Bn
1.65V to 5.5V	1.65V to 5.5V	L	Z	Z
1.65V to 5.5V	1.65V to 5.5V	H	input or output	input or output
GND	GND	X	Z	Z

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

[2] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into power-down mode.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Characteristic	Symbol	Conditions		Min.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-		-0.5	+6.5	V
supply voltage B	$V_{CC(B)}$	-		-0.5	+6.5	V
input voltage	V_I	A port and OE input		-0.5	+6.5	V
		B port		-0.5	+6.5	V
output voltage	V_O	Active mode	A or B port	-0.5	V_{CCO}+0.5	V
		Power-down or 3-state mode	A or B port	-0.5	+6.5	V
input clamping current	I_{IK}	V_I<0V		-50	-	mA
output clamping current	I_{OK}	V_O<0V		-50	-	mA
output current	I_O	V_O=0V to V_{CCO}		-	±50	mA
supply current	I_{CC}	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
ground current	I_{GND}	-		-100	-	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	250	mW
Soldering Temperature	T_L	10s		260		℃

Note:

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-		1.65	-	5.5	V
supply voltage B	$V_{CC(B)}$	-		1.65	-	5.5	V
ambient temperature	T_{amb}	-		-40	-	+85	℃
input transition rise and fall rate	Δt/ΔV	A, B or OE port	$V_{CC(A)}$=1.65V to 5.5V; $V_{CC(B)}$=1.65V to 5.5V	-	-	10	ns/V

Note:

[1] Hold the A and B sides of an unused I/O pair in the same state, both at V_{CCI} or both at GND.

3.3、Electrical Characteristics

3.3.1、DC Characteristics

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	A or B port	$V_{CC(A)}$=1.65V to 5.5V; $V_{CC(B)}$=1.65V to 5.5V	V_{CCI}-0.4	-	-	V
		OE input	$V_{CC(A)}$=1.65V to 5.5V; $V_{CC(B)}$=1.65V to 5.5V	0.65× $V_{CC(A)}$	-	-	V
LOW-level input voltage	V_{IL}	A or B port	$V_{CC(A)}$=1.65V to 5.5V; $V_{CC(B)}$=1.65V to 5.5V	-	-	0.4	V
		OE input	$V_{CC(A)}$=1.65V to 5.5V; $V_{CC(B)}$=1.65V to 5.5V	-	-	0.35× $V_{CC(A)}$	V
LOW-level output voltage	V_{OL}	A or B port; I_O=6mA	V_I≤0.15V; $V_{CC(A)}$=1.65V to 5.5V; $V_{CC(B)}$=1.65V to 5.5V	-	-	0.4	V
input leakage current	I_I	OE input; V_I=0V to $V_{CC(A)}$; $V_{CC(A)}$=1.65V to 5.5V; $V_{CC(B)}$=1.65V to 5.5V		-	-	±1	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V to 5.5V; $V_{CC(B)}$=0V to 5.5V		-	-	±2	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=0V to 5.5V		-	-	±2	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=0V to 5.5V		-	-	±2	uA
supply current	I_{CC}	V_I=0V or V_{CCI}; I_O=0A					
		$I_{CC(A)}$	$V_{CC(A)}$=1.65V to 5.5V; $V_{CC(B)}$=1.65V to 5.5V; OE=LOW or HIGH	-	-	5	uA
			$V_{CC(A)}$=1.65V to 5.5V; $V_{CC(B)}$=0V	-	-	2	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=1.65V to 5.5V	-	-	-2	uA
		$I_{CC(B)}$	$V_{CC(A)}$=1.65V to 5.5V; $V_{CC(B)}$=1.65V to 5.5V; OE=LOW	-	-	5	uA
			$V_{CC(A)}$=1.65V to 5.5V; $V_{CC(B)}$=0V	-	-	-2	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=1.65V to 5.5V	-	-	2	uA
input capacitance	C_I	OE input; $V_{CC(A)}$=$V_{CC(B)}$=0V		-	2.2	-	pF
input/output capacitance	$C_{I/O}$	A or B port; $V_{CC(A)}$=5.0V; $V_{CC(B)}$=5.0V		-	10	-	pF

Note:

[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.

3.3.2、AC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	V_{CCO}				Unit
			1.8V	2.5V	3.3V	5.0V	
LOW to HIGH output transition time	t_{TLH}	A or B port	7	5	4	3	ns
HIGH to LOW output transition time	t_{THL}	A or B port	4	6	8	11	ns
power dissipation capacitance	C_{PD}	OE=$V_{CC(A)}$; $V_{CC(A)}$=$V_{CC(B)}$; f_I=400kHz; V_I=V_{CCI}	-	-	-	13.5	pF

Note:

[1] V_{CCO} is the supply voltage associated with the output.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of the outputs.

[3] V_{CCI} is the supply voltage associated with the input.

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3.3.2、AC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	$V_{CC(B)}$								Unit
			1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
$V_{CC(A)}$=1.8V±0.15V											
HIGH to LOW propagation delay	t_{PHL}	A to B	3	7	3	6	3	5	5	7	ns
LOW to HIGH propagation delay	t_{PLH}	A to B	5	12	5	8	4	8	4	7	ns
HIGH to LOW propagation delay	t_{PHL}	B to A	3	7	3	6	3	5	5	7	ns
LOW to HIGH propagation delay	t_{PLH}	B to A	5	12	1	3	1	2	1	2	ns
OFF-state to LOW propagation delay	t_{PZL}	OE to A	9	16	9	18	10	14	10	15	ns
		OE to B	9	16	6	12	6	12	6	14	ns
LOW to OFF-state propagation delay	t_{PLZ}	OE to A	100	120	100	120	100	120	100	120	ns
		OE to B	100	120	100	120	100	120	100	120	ns
output skew time	$t_{sk(o)}$	between channels	-	1	-	1	-	1	-	1	ns
data rate	f_{data}	-	-	18	-	18	-	18	-	18	Mbps
$V_{CC(A)}$=2.5V±0.2V											
HIGH to LOW propagation delay	t_{PHL}	A to B	3	6	2	5	2	5	2	5	ns
LOW to HIGH propagation delay	t_{PLH}	A to B	1	3	2	4	2.5	7	2.5	5	ns
HIGH to LOW propagation delay	t_{PHL}	B to A	3	6	2	5	2	5	2	5	ns
LOW to HIGH propagation delay	t_{PLH}	B to A	5	8	2	4	1.5	3	1	3	ns
OFF-state to LOW propagation delay	t_{PZL}	OE to A	6	12	5	10	8	10	5	6	ns
		OE to B	9	18	5	10	4.5	9	4	8	ns
LOW to OFF-state propagation delay	t_{PLZ}	OE to A	100	120	100	120	100	120	100	120	ns
		OE to B	100	120	100	120	100	120	100	120	ns
output skew time	$t_{sk(o)}$	between	-	1	-	1	-	1	-	1	ns
data rate	f_{data}	-	-	18	-	32	-	32	-	32	Mbps
$V_{CC(A)}$=3.3V±0.3V											
HIGH to LOW propagation delay	t_{PHL}	A to B	3	5	2	5	2	4	2	4	ns
LOW to HIGH propagation delay	t_{PLH}	A to B	1	2	1.5	3	1.5	3	2	4	ns
HIGH to LOW propagation delay	t_{PHL}	B to A	3	5	2	5	2	4	2	4	ns
LOW to HIGH propagation delay	t_{PLH}	B to A	4	8	2.5	7	1.5	3	1	3	ns
OFF-state to LOW	t_{PZL}	OE to A	6	12	4.5	9	6	9	4	7	ns

propagation delay		OE to B	10	14	5	10	6	9	4	8	ns
LOW to OFF-state propagation delay	t_{PLZ}	OE to A	100	120	100	120	100	120	100	120	ns
		OE to B	100	120	100	120	100	120	100	120	ns
output skew time	$t_{sk(o)}$	between	-	1	-	1	-	1	-	1	ns
data rate	f_{data}	-	-	18	-	32	-	40	-	40	Mbps
$V_{CC(A)}$=5.5V±0.5V											
HIGH to LOW propagation delay	t_{PHL}	A to B	5	7	2	5	2	4	2	4	ns
LOW to HIGH propagation delay	t_{PLH}	A to B	1	2	1	3	1	3	1	3	ns
HIGH to LOW propagation delay	t_{PHL}	B to A	5	7	2	5	2	4	2	4	ns
LOW to HIGH propagation delay	t_{PLH}	B to A	4	7	2.5	5	2	4	1	3	ns
OFF-state to LOW propagation delay	t_{PZL}	OE to A	6	14	4	8	4	8	3	5	ns
		OE to B	10	15	5	8	4	7	4	5	ns
LOW to OFF-state propagation delay	t_{PLZ}	OE to A	100	120	100	120	100	120	100	120	ns
		OE to B	100	120	100	120	100	120	100	120	ns
output skew time	$t_{sk(o)}$	between	-	1	-	1	-	1	-	1	ns
data rate	f_{data}	-	-	18	-	32	-	40	-	52	Mbps

Note:

[1] All typical values are measured at nominal V_{CC} and T_{amb}=25℃.

[2] Skew between any two outputs of the same package switching in the same direction.

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4、Testing Circuit

4.1、AC Testing Circuit

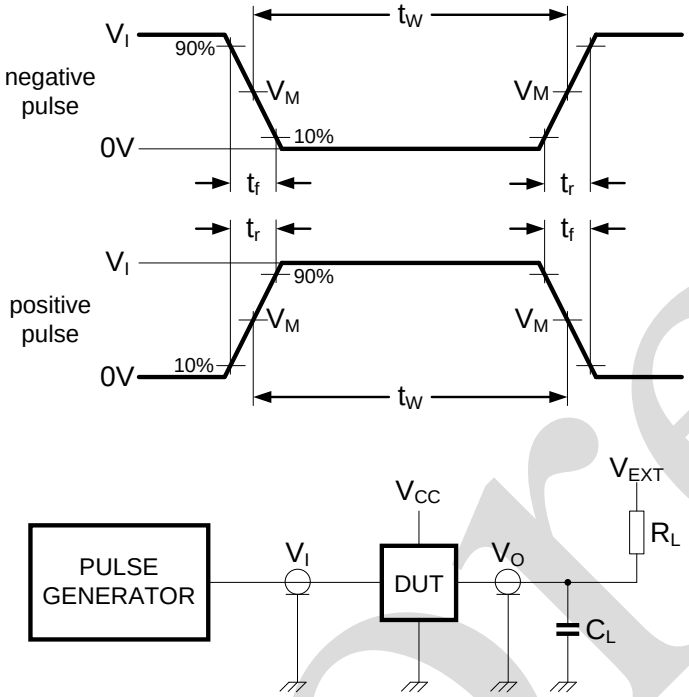

Figure 1. Test circuit for measuring switching times

All input pulses are supplied by generators having the following characteristics: PRR≤10MHz; Z_O=50Ω; dV/dt≥1.0V/ns.

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

V_{CCO}=Supply voltage associated with the output.

4.2、AC Testing Waveforms

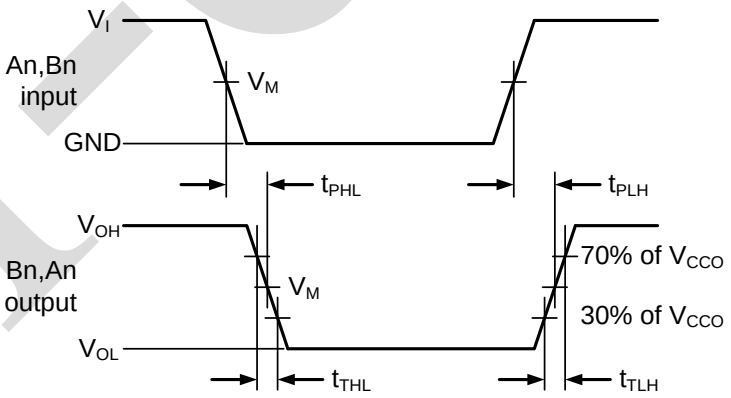

Figure 2. The data input (An, Bn) to data output (Bn, An) propagation delay times

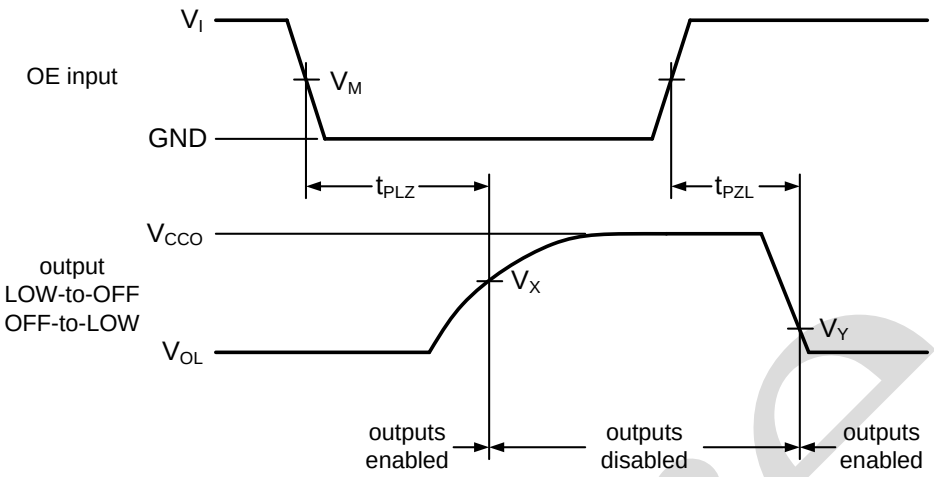

Figure 3. Enable and disable times

4.3、Measurement Points

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.65V to 5.5V	$0.5V_{CCI}$	$0.5V_{CCO}$	$0.5V_{CCO}$	$0.1V_{CCO}$

Note:

[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.

4.4、Test Data

Supply voltage		Input		Load	
$V_{CC(A)}$	$V_{CC(B)}$	V_I	t_r/t_f	C_L	R_L
1.65V to 1.95V	1.65V to 1.95V	V_{CCI}	≤2.0ns	50pF	2.2kΩ
2.3V to 2.7V	2.3V to 2.7V	V_{CCI}	≤2.0ns	50pF	2.2kΩ
3.0V to 3.6V	3.0V to 3.6V	V_{CCI}	≤2.5ns	50pF	2.2kΩ
4.5V to 5.5V	4.5V to 5.5V	V_{CCI}	≤2.5ns	50pF	2.2kΩ

Note:

[1] V_{CCI} is the supply voltage associated with the input.

5、Typical Application Circuit And Application Note

5.1、Applications

The AiPTS2102 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is targeted at I^2C or 1-wire buses which use open-drain drivers.

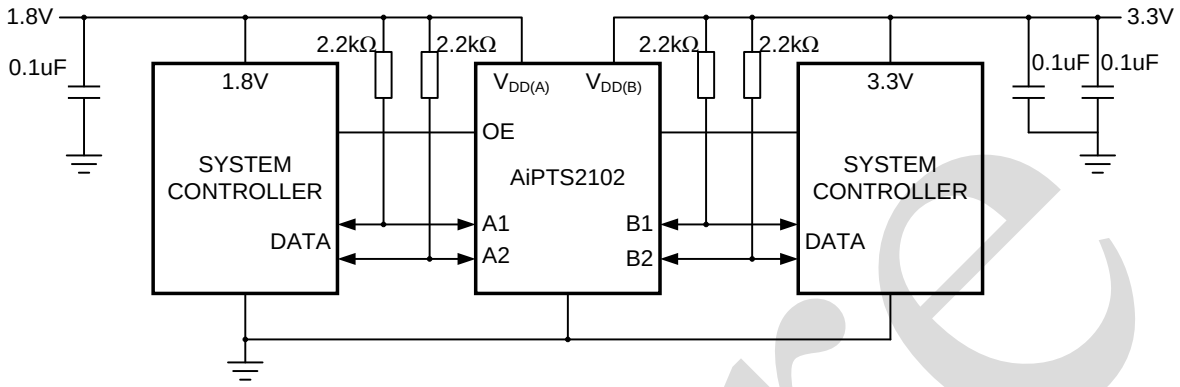

Figure 4. Typical voltage level-translation circuit

5.2、Input Driver Requirements

As the AiPTS2102 is a switch type translator, properties of the input driver directly affect the output signal. The external open-drain driver applied to an I/O, determines the static current sinking capability of the system. The maximum data rate, output transition times (t_{THL}, t_{TLH}) and propagation delays (t_{PHL}, t_{PLH}) are dependent upon the output impedance and edge-rate of the external driver.

5.3、Output Load Considerations

The maximum lumped capacitive load that can be driven is dependent upon the one-shot pulse duration and has been tuned to 600 pF. In cases with higher capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration. To avoid excessive capacitive loading and to ensure correct triggering of the one-shot, use short trace lengths and low capacitance connectors on AiPTS2102 PCB layouts. The length of the PCB trace should be such that the round-trip delay of any reflection is within the one-shot pulse duration. Such a length ensures low impedance termination and avoids output signal oscillations and one-shot retriggering.

5.4、Output Enable (OE)

An output enable input (OE) is used to disable the device. Setting OE=LOW causes all I/Os to assume the high-impedance OFF-state.

5.5、Power-Up

When either of the supplies $V_{CC(n)}$ is at 0 V, outputs are in the high-impedance OFF-state. One of the advantages of AiPTS010X/2102 translators is that either $V_{CC(A)}$ or $V_{CC(B)}$ may be powered up first. To reduce dissipation during power-up, ensure that output enable (OE) is defined. Connect it via a pull down resistor to GND or, if the application allows, hardwired to $V_{CC(A)}$. If the OE pin is hardwired to $V_{CC(A)}$, either supply can be powered up or down first. If a pull down is used, the following sequences are recommended.

For power-up:

1. Apply power to either supply pin
2. Apply power to other supply pin
3. Enable the device by driving OE HIGH

For power down:

1. Disable the device by driving OE LOW
2. Remove power from either supply pin
3. Remove power from other supply pin

5.6、Pull-Up Resistors On I/O Lines

Each A port I/O requires a pull-up resistor to $V_{CC(A)}$, and each B port I/O requires a pull-up resistor to $V_{CC(B)}$. Choose the magnitude of the pull-up resistors to ensure that the output voltage levels meet the application requirement.

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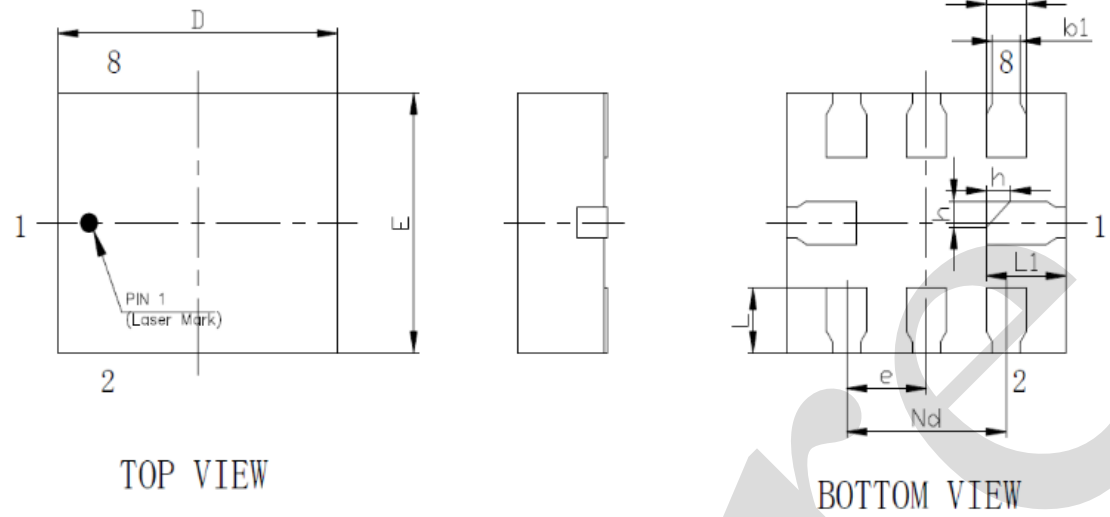
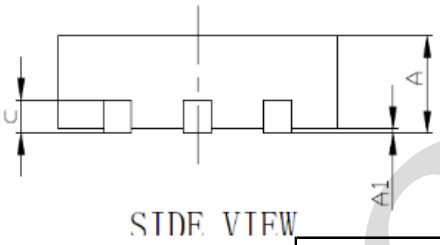
6、Package Information

6.1、QFN8





2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	0.40	0.50
A1	0	0.05
b	0.15	0.25
b1	0.14	
c	0.15	
D	1.35	1.45
e	0.40	
Nd	0.80	
E	1.15	1.25
L	0.25	0.35
L1	0.35	0.45
h	0.07	0.17

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

We recommend you to read this chapter carefully before using this product.

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