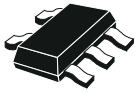
TS3121, TS3121A, TS3121P

Datasheet

Rail-to-rail, open-drain comparator with embedded Power-on Reset (P-version)



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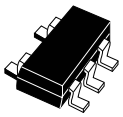


SOT23-5

Maturity status link
TS3121, TS3121A, TS3121P

Related products	
TS880	For lower supply current
TS3011	For higher speed
TS3021	For push-pull output

Features

- AEC-Q100 qualified
- Low offset voltage: 2 mV max @ 25 °C (A-grade version)
- Low power consumption: 70 µA typ.
- Wide supply voltage: 1.7 to 5.5 V
- Propagation delay: 60 ns
- Rail-to-rail input
- Open-drain output
- Output pin withstands voltages higher than V_{CC}
- Power-on Reset (TS3121P)
- Guaranteed start-up time (TS3121, TS3121A)
- High ESD tolerance: 4 kV HBM
- Extended temperature range: -40 to +125 °C
- Safety capable: documentation available to aid functional safety system design

Applications

- Industrial
- Automotive
- Power tools
- Overcurrent protection
- Controllers, sensors

Description

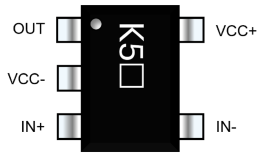
The TS3121, TS3121A and TS3121P single comparators permit high-speed response time at low power consumption over a supply voltage specified from 1.7 to 5.5 V. These devices operate over a wide temperature range from -40 °C to +125 °C making them ideal for industrial and automotive applications with the associated qualification.

An embedded power-on reset circuit in the TS3121P version ensures a known output condition while activating the supply rail.

Thanks to their small package size, the TS3121, TS3121A and TS3121P can be used in applications where space on the board is limited. It can thus reduce the overall cost of the PCB.

1 Pin configuration

Figure 1. Pin connection (top view)



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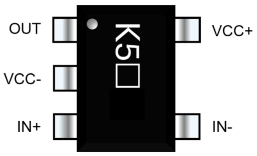
Dot or letter K denotes pin 1 position



SOT23-5

Dot or letter K denotes pin 1 position

Table 1. Pin description

Pin n°	Pin name	Description
1	OUT	Output
2	V_{CC-}	Negative supply voltage
3	IN+	Positive input voltage
4	IN-	Negative input voltage
5	V_{CC+}	Positive supply voltage

2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		6	V
V_{in}	Input voltage from V_{CC-}		-0.3 to V_{CC+}+0.3	V
I_{in}	Input current (2)		10	mA
V_{out}	Output voltage		6	V
T_{stg}	Storage temperature		-65 to +150	°C
T_j	Junction temperature		150	°C
R_{th-ja}	Thermal resistance junction to ambient (3) (4)	SOT23-5	250	°C/W
		SC70-5	205	
ESD	Human Body Model (HBM) (5)		4000	V
	Charged Device Model (CDM) (6)		1500	

1. *All voltage values, except differential voltage, are with respect to the network ground terminal.*
2. *Input current must be limited by a resistor in series with the inputs.*
3. *R_{th} are typical values.*
4. *Short circuits can cause excessive heating and destructive dissipation.*
5. *According to JEDEC standard JESD22-A114F.*
6. *According to ANSI/ESD STM5.3.1.*

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.7 to 5.5	V
V_{in}	Common mode input voltage range	-0.2 to V_{CC+} + 0.2	V
V_{out}	Output voltage	0 to 5.5	V
T	Operating free-air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 4. Electrical characteristics - V_{CC} = 5 V, V_{icm} = V_{CC}/2, T = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		DC performance				
V_{IO}	Input offset voltage	TS3121A, T = 25 °C	-2	0.5	+2	mV
		TS3121A, Tmin < T < Tmax	-4		+4	
		TS3121, TS3121P, T = 25 °C	-6	0.5	+6	
		TS3121, TS3121P, Tmin < T < Tmax	-8		+8	
$\lvert\Delta V_{IO}/\Delta T\rvert$	Input offset voltage drift	Tmin< T < Tmax		3	20	µV/°C
V_{HYST}	Input hysteresis voltage (1)			1		mV
$\lvert I_{IB}\rvert$	Input bias current (2)	T = 25 °C		5	50	pA
		Tmin < T < Tmax			200	
$\lvert I_{IO}\rvert$	Input offset current (2)	T = 25 °C		1	20	
		Tmin < T < Tmax			100	
CMRR	Common-mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	0 < V_{icm} < V_{CC}		70		dB
		Tmin < T < Tmax	55			
SVR	Supply voltage rejection: 20 log ($\Delta V_{cc}/\Delta V_{io}$)	ΔV_{cc} = 1.8 V to 5.0 V, V_{icm} = 0 V, T = 25 °C		80		
		ΔV_{cc} = 1.8 V to 5.0 V, V_{icm} = 0 V, Tmin < T < Tmax	58			
I_{sink}	Output sink current	V_{OUT} = V_{CC+}	100	140		mA
		Tmin < T < Tmax	70			
I_{OH}	High-level output leakage current, V_{OUT} = V_{CC} (3)	V_{OUT} = V_{CC}		460	800	pA
		Tmin < T < Tmax			250	nA
V_{OL}	Low-level output voltage I_{sink} = 1 mA	T = 25 °C		18	30	mV
		Tmin< T < Tmax			45	
I_{CC}	Supply current TS3121, TS3121A	Output low, V_{ID} = - 0.1 V		73	125	µA
		Tmin < T < Tmax			155	
		Output high, V_{ID} = +0.1 V		57	125	
		Tmin < T < Tmax			155	
	Supply current TS3121P	Output low, V_{ID} = - 0.1 V		100	148	
		Tmin < T < Tmax			155	
		Output high, V_{ID} = +0.1 V		80	148	
		Tmin < T < Tmax			155	
$t_{start-up}$	Start-up time TS3121, TS3121A	V_{CC} > 1.5 V		10	15	µs
t_{PoR}	Power-on Reset time TS3121P	V_{CC} > 1.5 V		10	15	
t_{PLH} (4)	Propagation delay (low to high), C_L = 15 pF, overdrive = 20 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C		170	235	ns
		Tmin < T < Tmax			250	
	C_L = 15 pF, overdrive = 100 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C		130	160	
		Tmin < T < Tmax			185	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{PHL} (5)	Propagation delay (high to low), C_L = 15 pF, overdrive = 20 mV, $V_{PU} = V_{CC}$	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		100	135 185	ns
	C_L = 15 pF, overdrive = 100 mV, $V_{PU} = V_{CC}$	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		60	85 125	
t_F	Fall time (90% to 10%)	C_L = 15 pF, R_{PU} = 2.5 kΩ, overdrive = 100 mV		2.5		

1. *Hysteresis is a built-in feature of the TS3121. It is defined as the voltage difference between the trip points.*
2. *Maximum values include unavoidable inaccuracies of the industrial tests.*
3. *Maximum high-level output leakage current at T = 25 °C is guaranteed by design.*
4. *t_{PLH} is measured when the output signal crosses a voltage level at 50% of Vcc with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} - 100 mV to V_{ICM} + overdrive.*
5. *t_{PHL} is measured when the output signal crosses a voltage level at 50% of Vcc with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} + 100 mV to V_{ICM} - overdrive.*

Table 5. Electrical characteristics - V_{CC} = 3.3 V, V_{icm} = V_{CC}/2, T = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	TS3121A, T = 25 °C	-2	0.5	+2	mV
		TS3121A, Tmin < T < Tmax	-4		+4	
		TS3121, TS3121P, T = 25 °C	-6	0.5	+6	
		TS3121, TS3121P, Tmin < T < Tmax	-8		+8	
$\lvert\Delta V_{IO}/\Delta T\rvert$	Input offset voltage drift	Tmin < T < Tmax		3	20	µV/°C
V_{HYST}	Input hysteresis voltage (1)			1		mV
$\lvert I_{IB}\rvert$	Input bias current (2)	T = 25 °C		5	50	pA
		Tmin < T < Tmax			200	
$\lvert I_{IO}\rvert$	Input offset current (2)	T = 25 °C		1	20	
		Tmin < T < Tmax			100	
CMRR	Common-mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	0 < V_{icm} < V_{CC}		70		dB
		Tmin < T < Tmax	50			
I_{sink}	Output sink current	V_{OUT} = V_{CC+}	45	70		mA
		Tmin < T < Tmax	35			
I_{OH}	High-level output leakage current, V_{OUT} = V_{CC} (3)	V_{OUT} = V_{CC}		425	700	pA
		Tmin < T < Tmax			200	nA
V_{OL}	Low-level output voltage I_{sink} = 1 mA	T = 25 °C		20	35	mV
		Tmin< T < Tmax			50	
I_{CC}	Supply current TS3121, TS3121A	Output low, V_{ID} = -0.1 V		71	125	µA
		Tmin < T < Tmax			155	
		Output high, V_{ID} = +0.1 V		56	125	
		Tmin < T < Tmax			155	
	Supply current TS3121P	Output low, V_{ID} = - 0.1 V		85	148	
		Tmin < T < Tmax			155	
		Output high, V_{ID} = +0.1 V		65	148	
		Tmin < T < Tmax			155	
$t_{start-up}$	Start-up time TS3121, TS3121A	V_{CC} > 1.5 V		10	15	µs
t_{PoR}	Power-on Reset time TS3121P	V_{CC} > 1.5 V		10	15	
t_{PLH} (4)	Propagation delay (low to high), C_L = 15 pF, overdrive = 20 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C		160	220	ns
		Tmin < T < Tmax			240	
	C_L = 15 pF, overdrive = 100 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C		130	160	
		Tmin < T < Tmax			175	
t_{PHL} (5)	Propagation delay (high to low), C_L = 15 pF, overdrive = 20 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C		90	115	
		Tmin < T < Tmax			160	
	C_L = 15 pF, overdrive = 100 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C		60	85	
		Tmin < T < Tmax			125	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_F	Fall time (90% to 10%)	C_L = 15 pF, R_{PU} = 2.5 kΩ, overdrive = 100 mV		3.5		ns

1. *Hysteresis is a built-in feature of the TS3121. It is defined as the voltage difference between the trip points.*
2. *Maximum values include unavoidable inaccuracies of the industrial tests.*
3. *Maximum high-level output leakage current at T = 25 °C is guaranteed by design.*
4. *t_{PLH} is measured when the output signal crosses a voltage level at 50% of Vcc with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} - 100 mV to V_{ICM} + overdrive.*
5. *t_{PHL} is measured when the output signal crosses a voltage level at 50% of Vcc with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} + 100 mV to V_{ICM} - overdrive.*

Table 6. Electrical characteristics - V_{CC} = 1.8 V, V_{icm} = V_{CC}/2, T = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	TS3121A, T = 25 °C	-2	0.5	+2	mV
		TS3121A, Tmin < T < Tmax	-4		+4	
		TS3121, TS3121P, T = 25 °C	-6	0.5	+6	
		TS3121, TS3121P, Tmin < T < Tmax	-8		+8	
$\lvert\Delta V_{IO}/\Delta T\rvert$	Input offset voltage drift	Tmin < T < Tmax		3	20	µV/°C
V_{HYST}	Input hysteresis voltage (1)			1		mV
$\lvert I_{IB}\rvert$	Input bias current (2)	T = 25 °C		5	50	pA
		Tmin < T < Tmax			200	
$\lvert I_{IO}\rvert$	Input offset current (2)	T = 25 °C		1	20	
		Tmin < T < Tmax			100	
CMRR	Common-mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	0 < V_{icm} < V_{CC}		70		dB
		Tmin < T < Tmax	50			
I_{sink}	Output sink current	V_{OUT} = V_{CC+}	11	18		mA
		Tmin < T < Tmax	9			
I_{OH}	High-level output leakage current, V_{OUT} = V_{CC} (3)	V_{OUT} = V_{CC}		193	700	pA
		Tmin < T < Tmax			200	nA
V_{OL}	Low-level output voltage I_{sink} = 1 mA	T = 25 °C		36	60	mV
		Tmin< T < Tmax			80	
I_{CC}	Supply current TS3121, TS3121A	Output low, V_{ID} = -0.1 V		78	125	µA
		Tmin < T < Tmax			155	
		Output high, V_{ID} = +0.1 V		81	125	
		Tmin < T < Tmax			155	
	Supply current TS3121P	Output low, V_{ID} = - 0.1 V, V_{ICM} = 0 V		75	148	
		Tmin < T < Tmax			155	
		Output high, V_{ID} = +0.1 V, V_{ICM} = 0 V		55	148	
		Tmin < T < Tmax			155	
$t_{start-up}$	Start-up time TS3121, TS3121A	V_{CC} > 1.5 V		10	15	µs
t_{PoR}	Power-on Reset time TS3121P	V_{CC} > 1.5 V		10	15	
t_{PLH} (4)	Propagation delay (low to high), C_L = 15 pF, overdrive = 20 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C		160	220	ns
		Tmin < T < Tmax			225	
	C_L = 15 pF, overdrive = 100 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C		130	160	
		Tmin < T < Tmax			175	
t_{PHL} (5)	Propagation delay (high to low), C_L = 15 pF, overdrive = 20 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C		90	115	
		Tmin < T < Tmax			165	
	C_L = 15 pF, overdrive = 100 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C		60	85	
		Tmin < T < Tmax			125	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_F	Fall time (90% to 10%)	C_L = 15 pF, R_{PU} = 2.5 kΩ, overdrive = 100 mV		3.5		ns

1. *Hysteresis is a built-in feature of the TS3121. It is defined as the voltage difference between the trip points.*
2. *Maximum values include unavoidable inaccuracies of the industrial tests.*
3. *Maximum high-level output leakage current at T = 25 °C is guaranteed by design.*
4. *t_{PLH} is measured when the output signal crosses a voltage level at 50% of Vcc with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} - 100 mV to V_{ICM} + overdrive.*
5. *t_{PHL} is measured when the output signal crosses a voltage level at 50% of Vcc with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} + 100 mV to V_{ICM} - overdrive.*

4 Typical performance characteristics

Figure 2. Supply current vs. supply voltage at $V_{icm} = V_{CC}$, output high

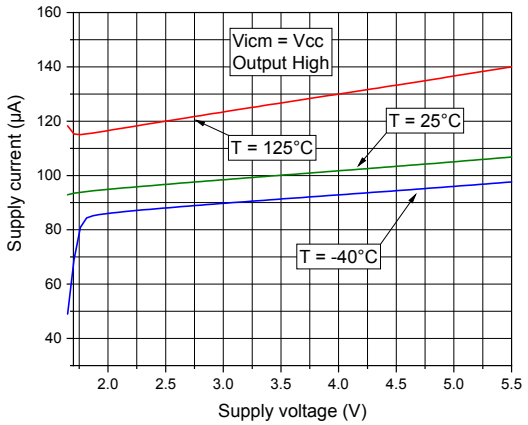


Figure 3. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$, output high

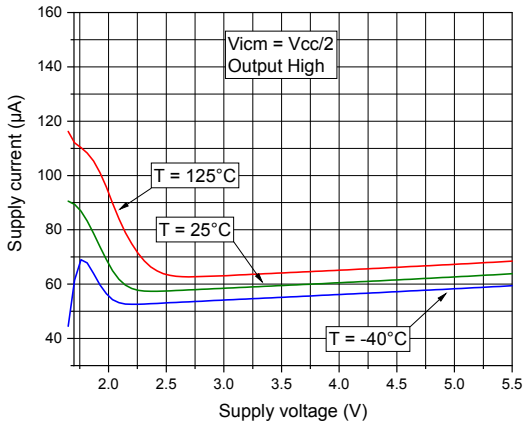


Figure 4. Supply current vs. supply voltage at $V_{icm} = V_{CC}$-, output high

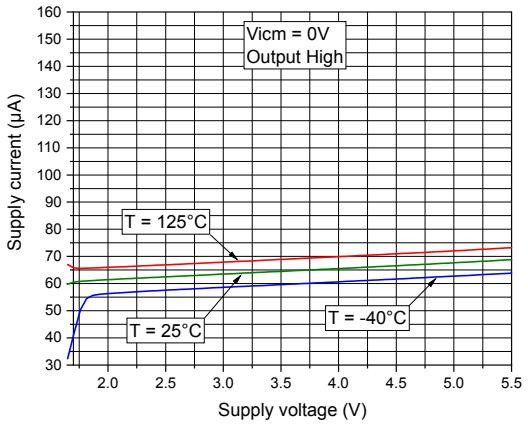


Figure 5. Supply current vs. supply voltage at $V_{icm} = V_{CC}$, output high

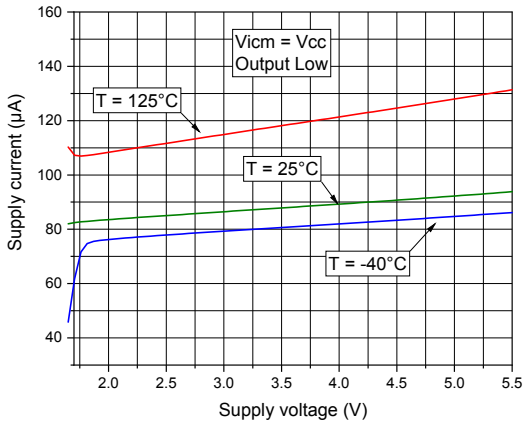


Figure 6. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$, output low

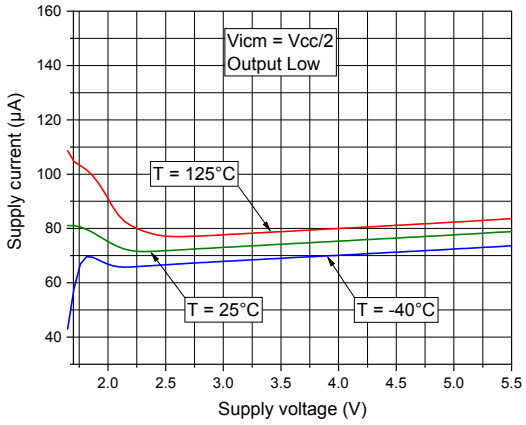


Figure 7. Supply current vs. supply voltage at $V_{icm} = V_{CC}$-, output low

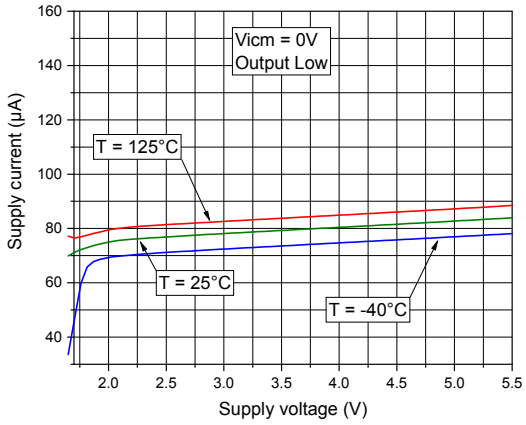


Figure 8. Supply current vs. input common-mode voltage at V_{CC} = 1.8 V, output high

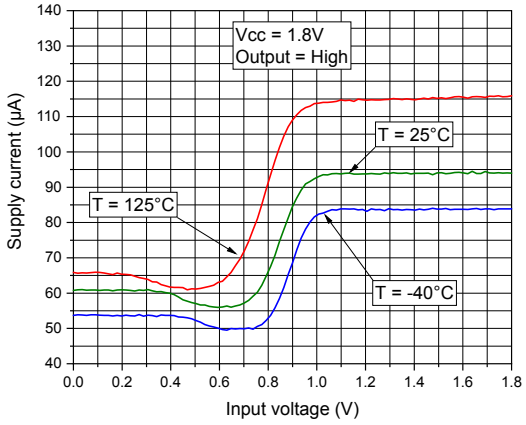


Figure 9. Supply current vs. input common-mode voltage at V_{CC} = 3.3 V, output high

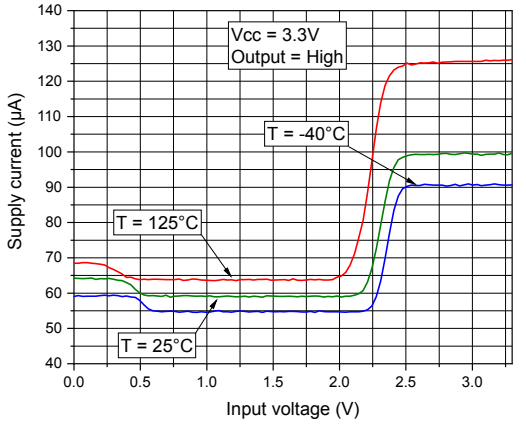


Figure 10. Supply current vs. input common-mode voltage at V_{CC} = 5.0 V, output high

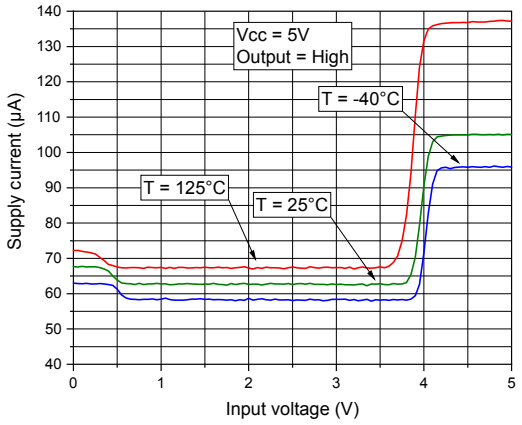


Figure 11. Input bias current vs. input common-mode voltage at V_{CC} = 1.8 V

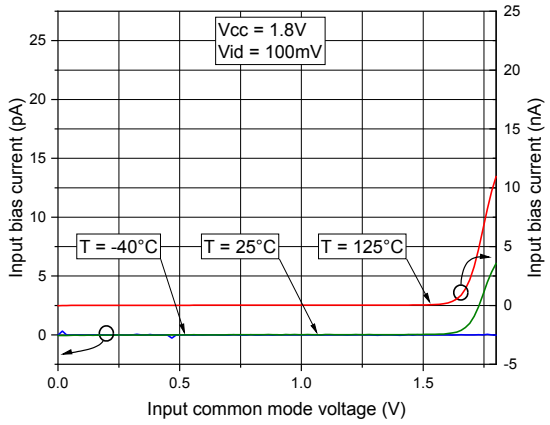


Figure 12. Input bias current vs. input common-mode voltage at V_{CC} = 3.3 V

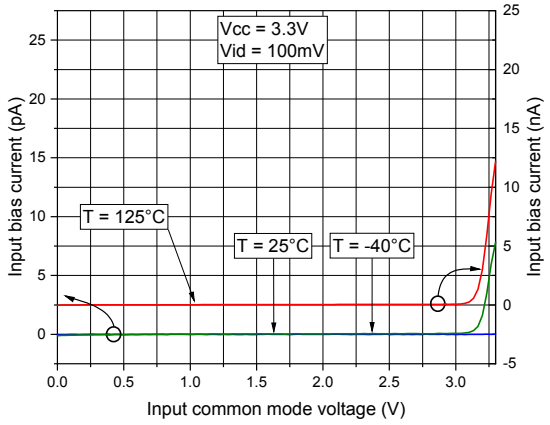


Figure 13. Input bias current vs. input common-mode voltage at V_{CC} = 5.0 V

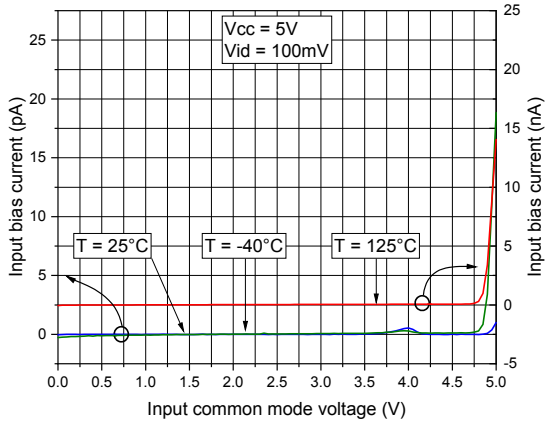


Figure 14. Input bias current vs. supply voltage at $V_{icm} = V_{CC}/2$

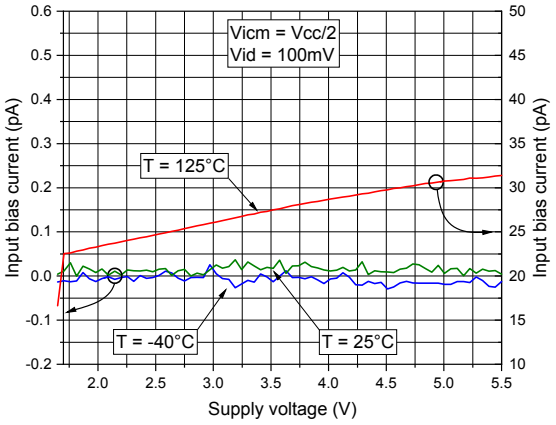


Figure 15. Input offset voltage vs. input common-mode voltage at $V_{CC} = 1.8$ V

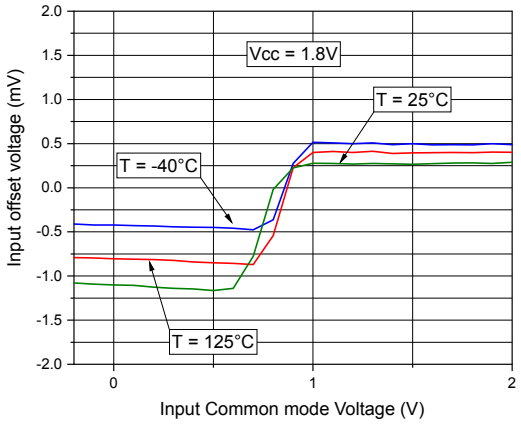


Figure 16. Input offset voltage vs. input common-mode voltage at $V_{CC} = 3.3$ V

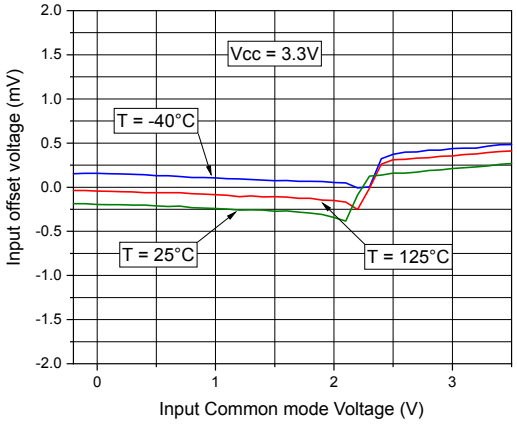


Figure 17. Input offset voltage vs. input common-mode voltage at $V_{CC} = 5.0$ V

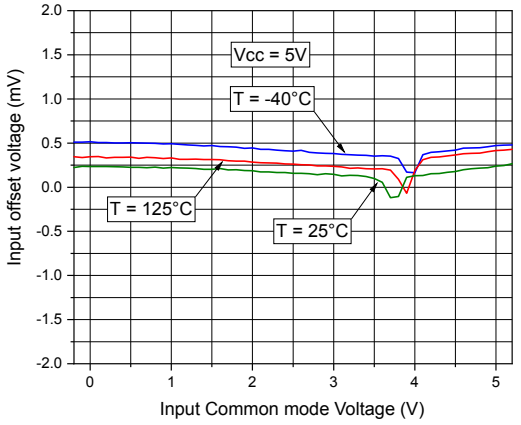


Figure 18. Input offset voltage vs. supply voltage at $V_{icm} = V_{CC}$-

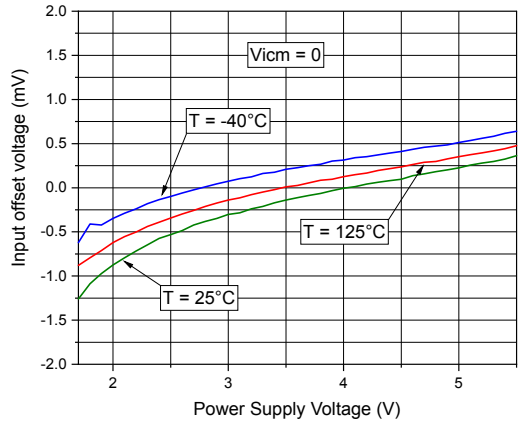


Figure 19. Input offset voltage vs. supply voltage at $V_{icm} = V_{CC}/2$

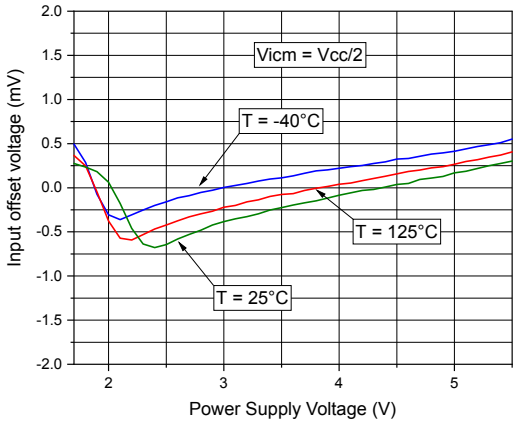


Figure 20. Input offset voltage vs. supply voltage at $V_{icm} = V_{CC}$

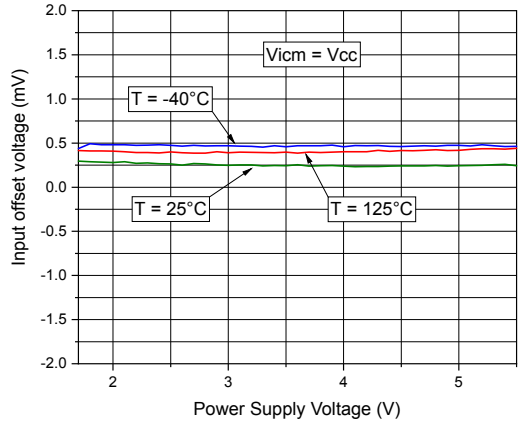


Figure 21. Input offset voltage drift vs. temperature from -40 °C to +25 °C

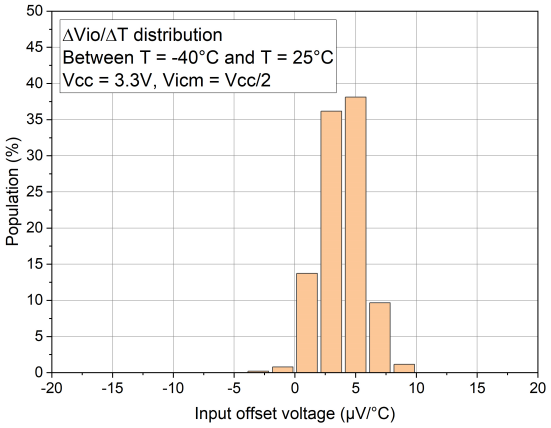


Figure 22. Input offset voltage drift vs. temperature from -25 °C to +125 °C

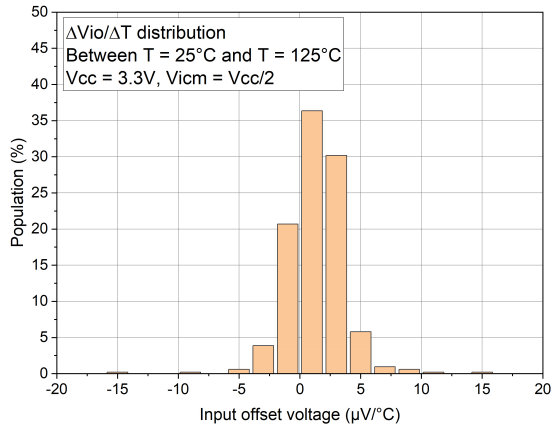


Figure 23. Input offset voltage vs. temperature at V_{CC} = 1.8 V

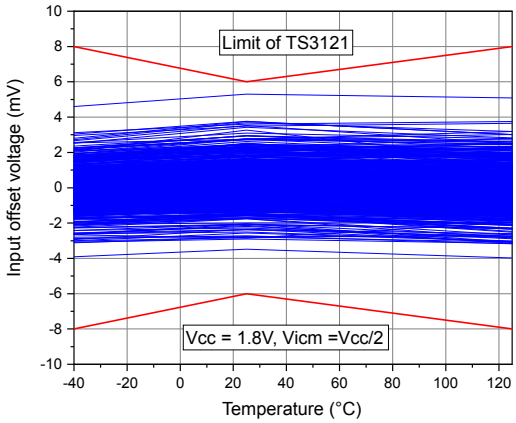


Figure 24. Input offset voltage vs. temperature at V_{CC} = 5.0 V

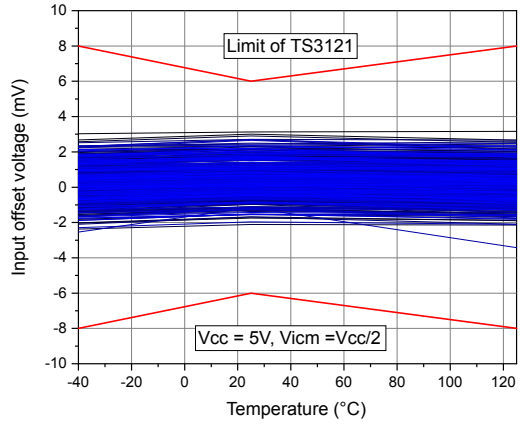


Figure 25. Input offset voltage distribution at V_{CC} = 1.8 V

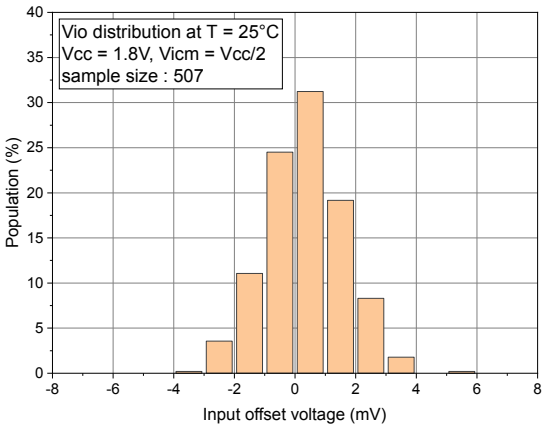


Figure 26. Input offset voltage distribution at V_{CC} = 3.3 V

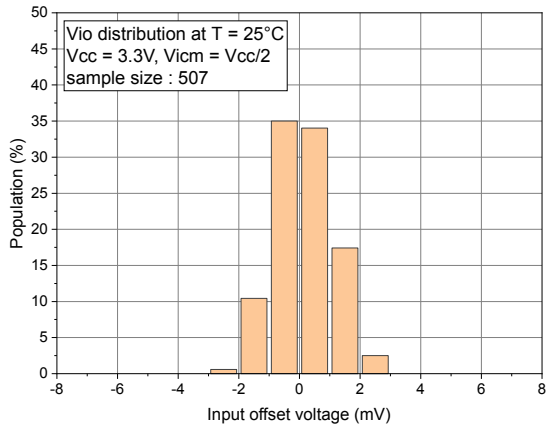


Figure 27. Input offset voltage distribution at V_{CC} = 5.0 V

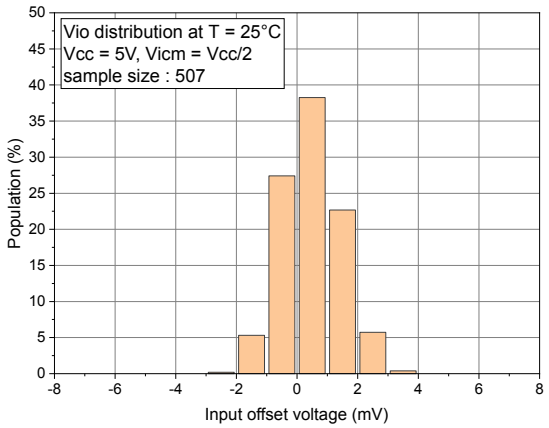


Figure 28. Output drop voltage vs. output sink current at V_{CC} = 1.8 V

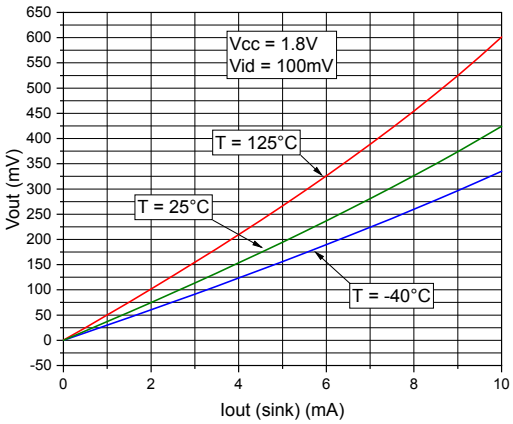


Figure 29. Output drop voltage vs. output sink current at V_{CC} = 3.3 V

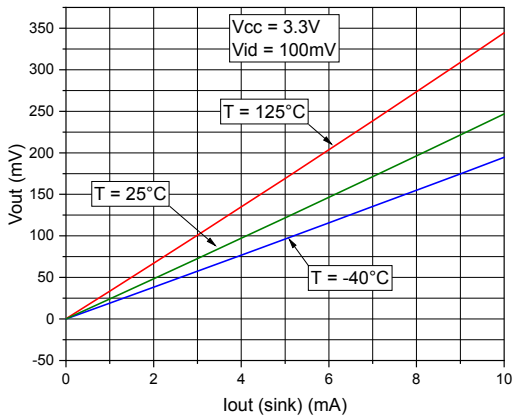


Figure 30. Output drop voltage vs. output sink current at V_{CC} = 5.0 V

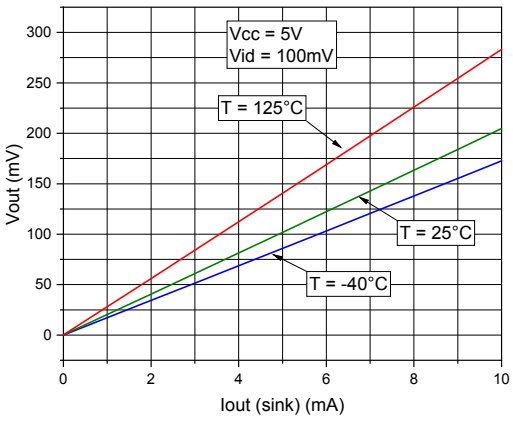


Figure 31. High-level output leakage current vs. output voltage at V_{CC} = 1.8 V

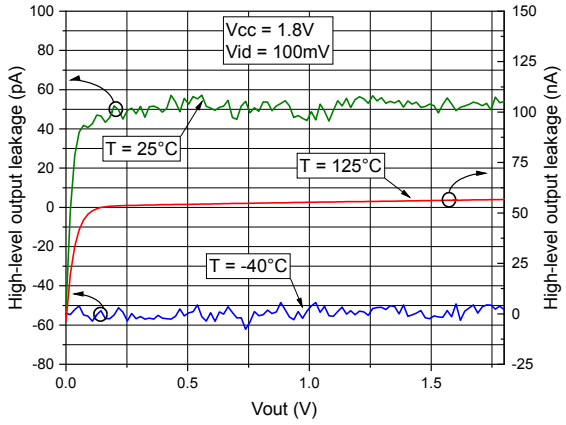


Figure 32. High-level output leakage current vs. output voltage at V_{CC} = 5.0 V

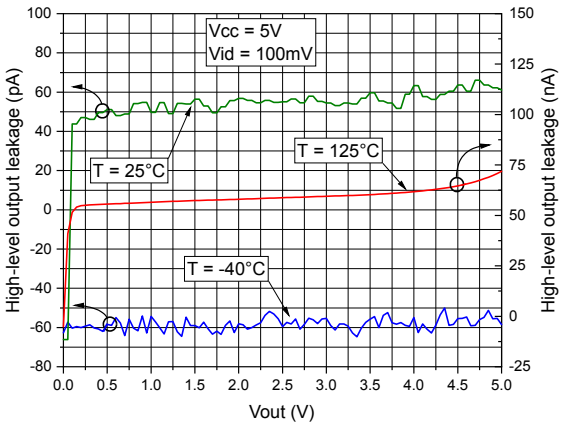


Figure 33. High-to-low propagation delay vs. overdrive at V_{CC} = 1.8 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

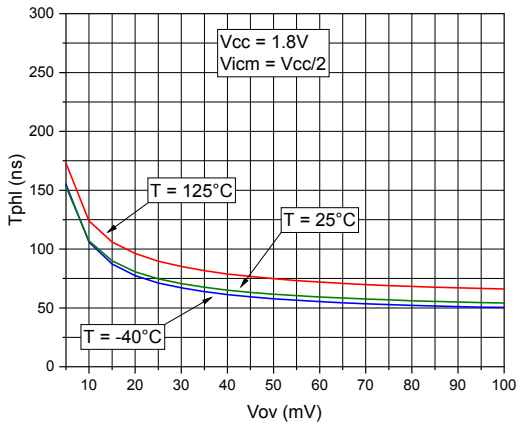


Figure 34. High-to-low propagation delay vs. overdrive at V_{CC} = 3.3 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

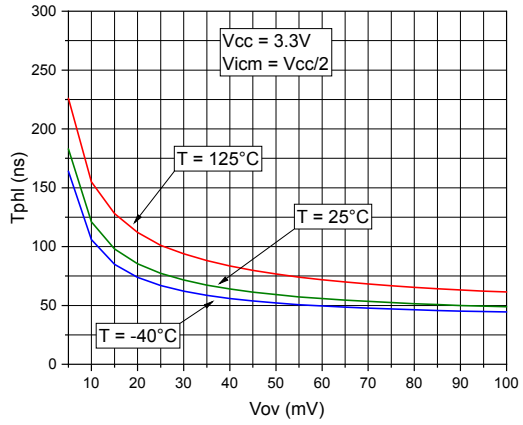


Figure 35. High-to-low propagation delay vs. overdrive at V_{CC} = 5.0 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

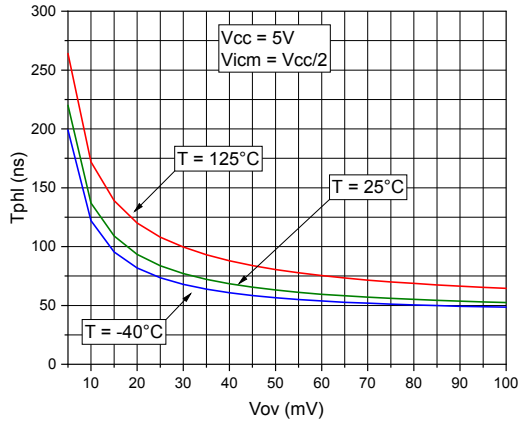


Figure 36. Low-to-high propagation delay vs. overdrive at V_{CC} = 1.8 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

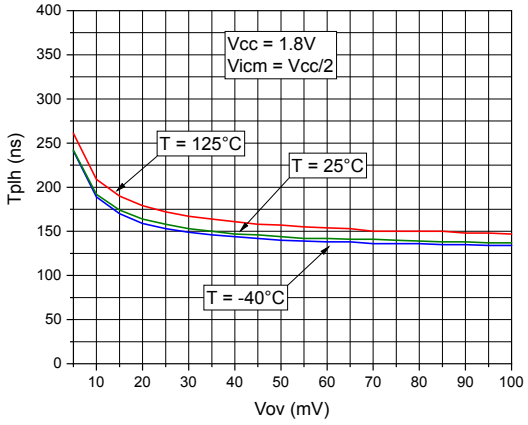


Figure 37. Low-to-high propagation delay vs. overdrive at V_{CC} = 3.3 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

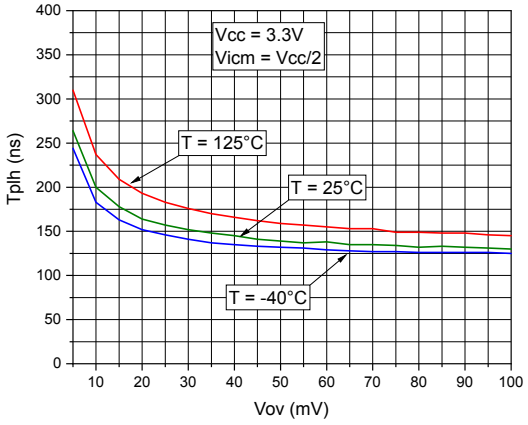


Figure 38. Low-to-high propagation delay vs. overdrive at V_{CC} = 5.0 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

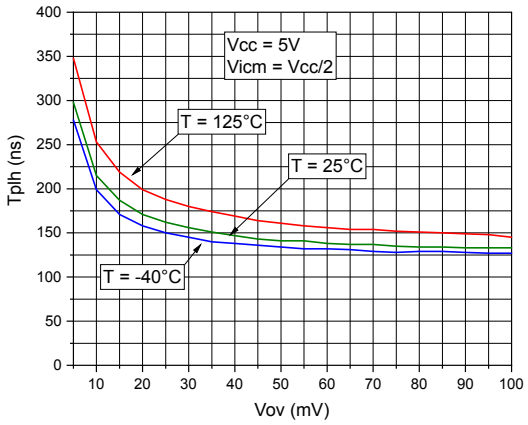


Figure 39. Low-to-high propagation delay vs. input common-mode voltage at V_{CC} = 1.8 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

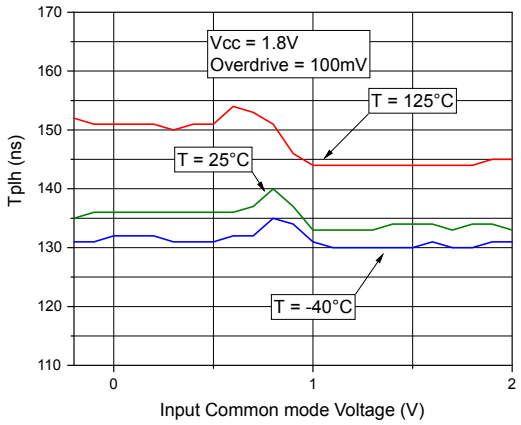


Figure 40. Low-to-high propagation delay vs. input common-mode voltage at V_{CC} = 3.3 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

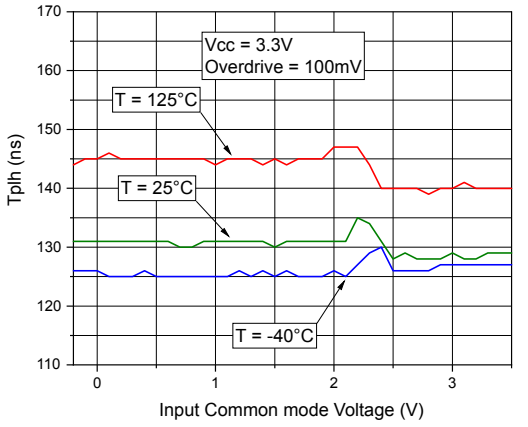


Figure 41. Low-to-high propagation delay vs. input common-mode voltage at V_{CC} = 5.0 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

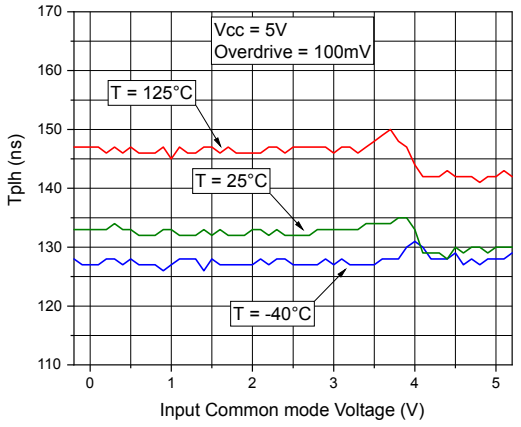


Figure 42. Low-to-high propagation delay vs. supply voltage at V_{icm} = V_{CC}/2, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

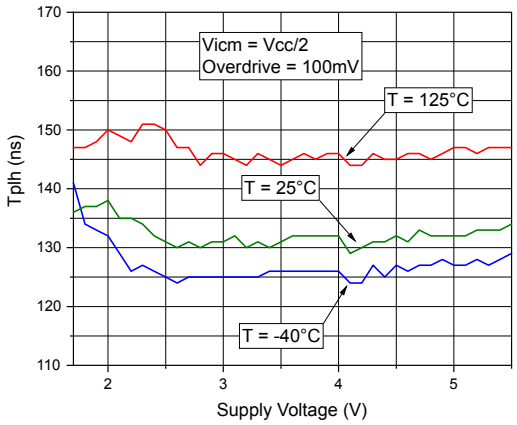


Figure 43. High-to-low propagation delay vs. input common-mode voltage at V_{CC} = 1.8 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

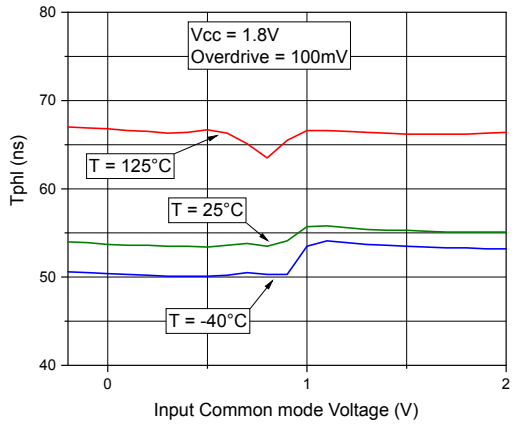


Figure 44. High-to-low propagation delay vs. input common-mode voltage at V_{CC} = 3.3 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

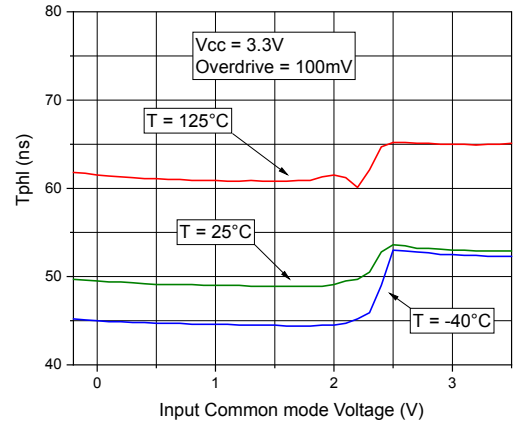


Figure 45. High-to-low propagation delay vs. input common-mode voltage at V_{CC} = 5.0 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

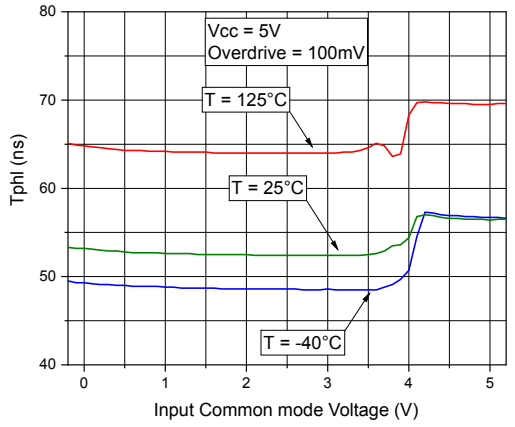


Figure 46. High-to-low propagation delay vs. supply voltage at V_{icm} = V_{CC}/2, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

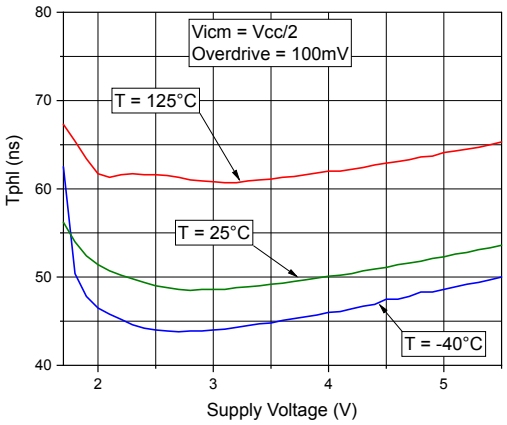


Figure 47. Power-on Reset output sequence V_{CC} = 1.8 V, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

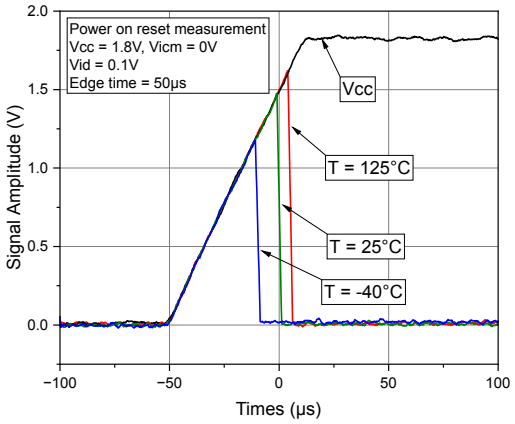


Figure 48. Power-on Reset output sequence V_{CC} = 3.3 V, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

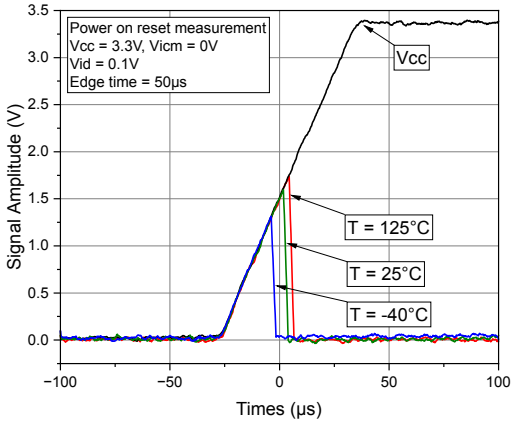
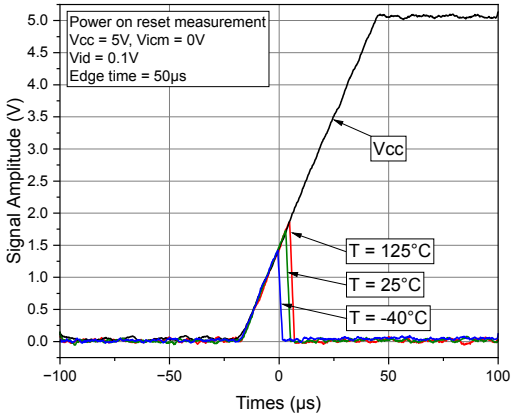


Figure 49. Power-on Reset output sequence V_{CC} = 5.0 V, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}



5 Application information

Input offset voltage drift versus temperature

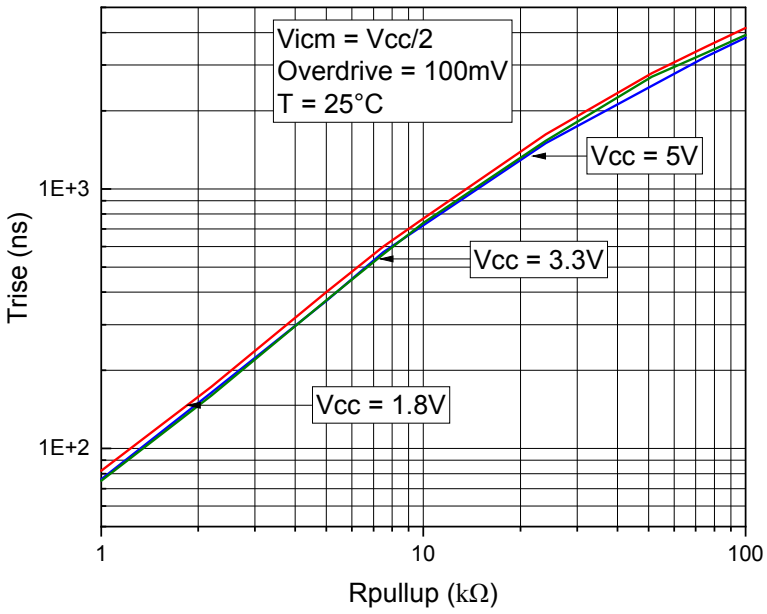
The input voltage drift variation versus temperature is defined as the offset variation related to the offset value measured at 25 °C. The signal chain accuracy at 25 °C can be compensated during the production at the application level. The maximum input voltage drift over the temperature enables the system designer to anticipate the effect of temperature variations.

$$\frac{\Delta V_{io}}{\Delta V} = \max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right| \quad (1)$$

Where T = -40 °C and +125 °C. The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a Cpk (process capability index) greater than 1.3. The datasheet reports the absolute worst-case value between -40 °C and +125 °C.

Resistor values for high-speed design

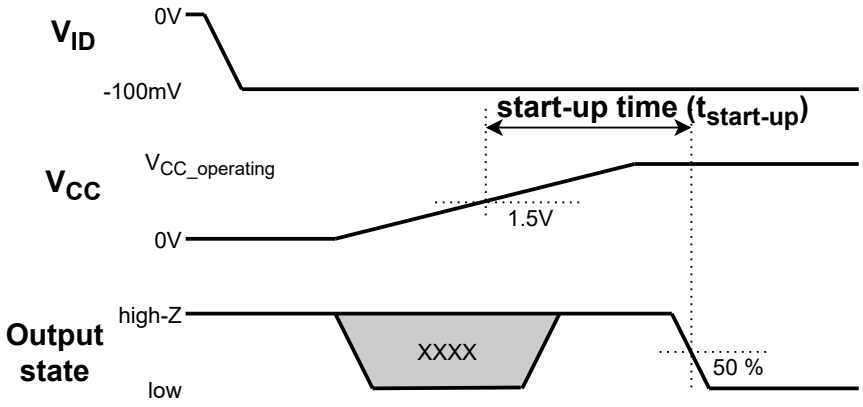
Figure 50. Rise time vs. pull-up resistor



Guaranteed start-up time (TS3121, TS3121A)

The TS3121 and TS3121A are tested in production for a guaranteed start-up time. Once the supply voltage crosses the minimum value of 1.5 V, the output voltage is settled in a stable condition within a maximum delay of $t_{start-up}$ = 15 µs. In applications with switched Vcc, care should be taken to keep the Vcc ramp-up below 0.5 V/µs to prevent false triggering of the integrated ESD protection circuit.

Figure 51. Start-up timing diagram

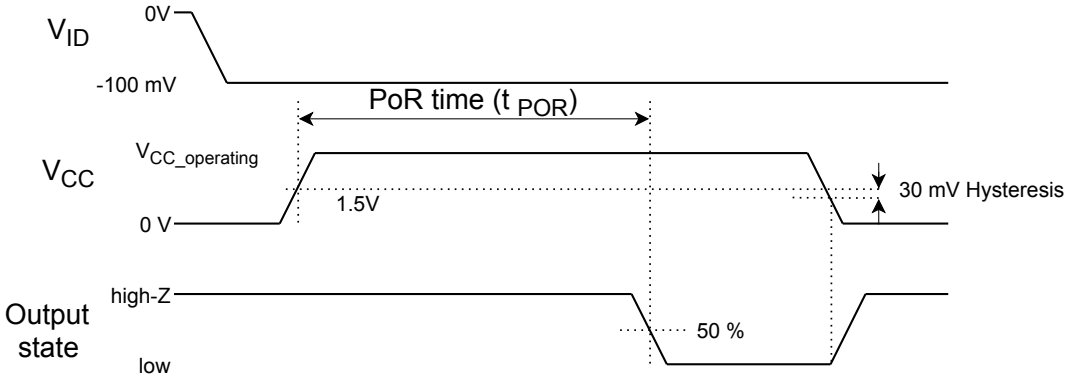


Power-on Reset (PoR) time (TS3121P)

The TS3121P has an embedded Power-On Reset (PoR) circuit for known start-up and power-down conditions. While the power supply (V_{CC}) is ramping up, the embedded PoR circuitry will keep the output in a high impedance (high-Z) state until the comparator's transistors are correctly biased and operational. The output will be operational after a maximum delay of t_{PoR} = 15 µs after the supply voltage crosses the minimum value of 1.5 V. The output will be in high impedance immediately when the supply voltage drops approximately 30 mV below the threshold of 1.5 V.

The PoR controller by design allows high reliability even for short on/off cycles below 1 ms. In applications with switched V_{CC}, care should be taken to keep the V_{CC} ramp-up below 0.5 V/µs to prevent false triggering of the integrated ESD protection circuit.

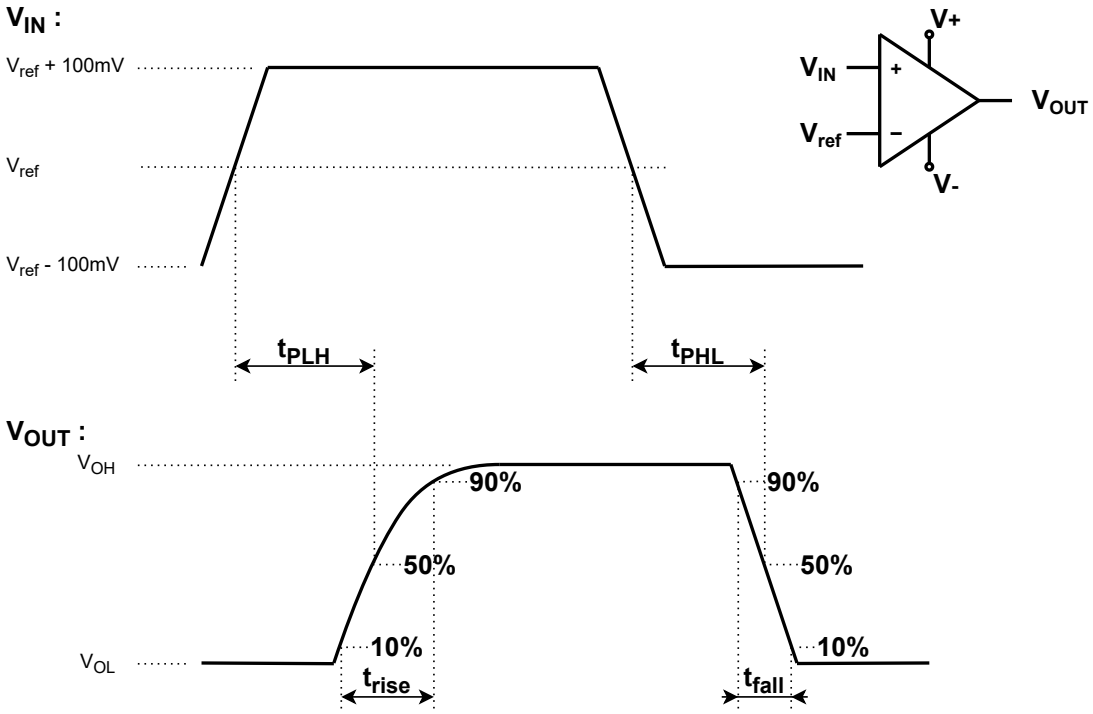
Figure 52. Power-on Reset timing diagram



Propagation delay

There is a delay between when the input crosses the reference voltage and the output responds. This is called the propagation delay. Propagation delay can be different between high-to-low and low-to-high input transitions. This is shown as t_{PLH} and t_{PHL} in Figure 53 and is measured from the mid-point of the input to the midpoint of the output. Note that for open-drain comparators, the output rise time t_{rise} and t_{PLH} strongly depend on the pull-up circuit connected to the output pin.

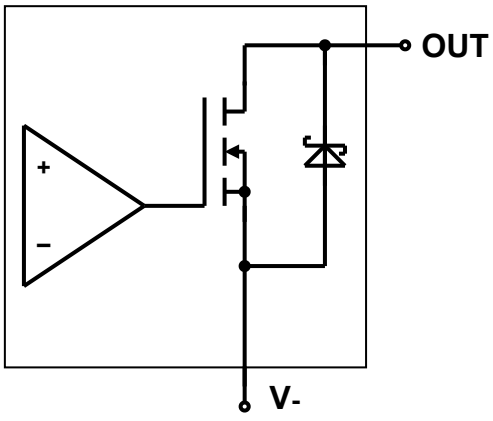
Figure 53. Propagation delay



Output stage

With a dedicated ESD clamp in the open-drain output stage, voltage levels higher than V_{CC} can be applied to the comparator output. The TS3121 can thus be used for level shifter applications where the output voltage is independent of the comparator supply voltage.

Figure 54. Output stage



PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the comparator, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition to minimizing parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace impedance.

Decoupling capacitor

To ensure op amp full functionality, it is recommended to place two decoupling capacitors of 100 nF and 10 nF as close as possible to the comparator supply pins. A good decoupling helps to reduce electromagnetic interference impact.

6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SC70-5 (or SOT323-5) package information

Figure 55. **SC70-5 (or SOT323-5) package outline**

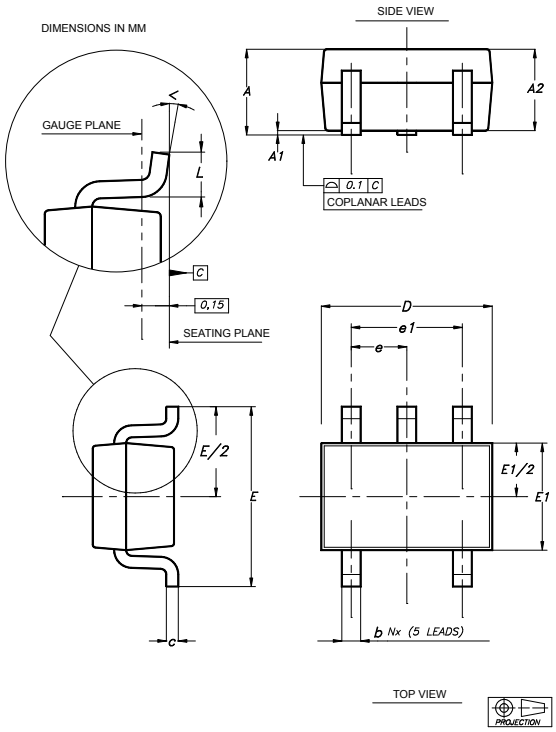


Table 7. **SC70-5 (or SOT323-5) package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

6.2 SOT23-5 package information

Figure 56. **SOT23-5 package outline**

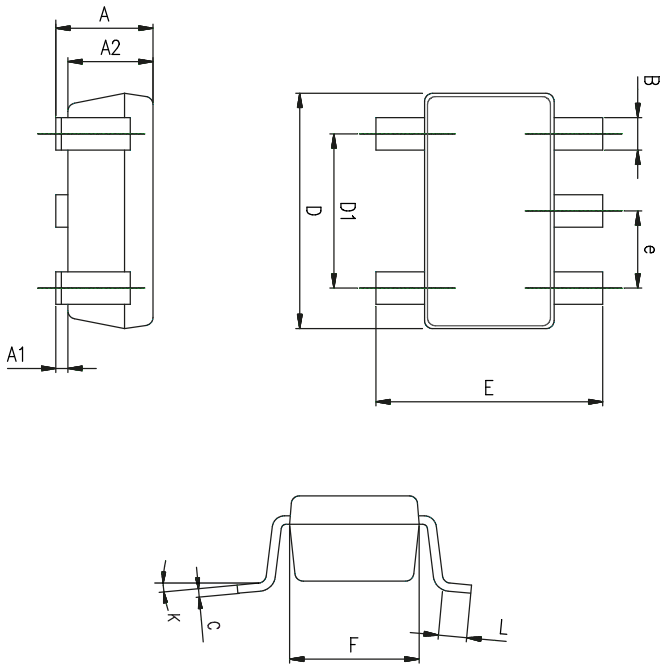


Table 8. **SOT23-5 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

7 Ordering information

Table 9. Order code

Order code	Package	Packaging	Marking
TS3121ICT	SC70-5	Tape and reel	K5T
TS3121AICT			K5U
TS3121IYCT (1)			K5V
TS3121AIYCT (1)			K5W
TS3121PICT			K5X
TS3121PIYCT (1)			K5Y
TS3121ILT	SOT23-5		K5T
TS3121AILT			K5U
TS3121IYLT (1)			K5V
TS3121AIYLT (1)			K5W
TS3121PILT			K5X
TS3121PIYLT (1)			K5Y

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
31-Jul-2024	1	Initial release.
14-Nov-2024	2	Updated description on the cover page.
10-Apr-2025	3	Updated Figure 1. Pin connection (top view).
03-Apr-2026	4	Updated features, added new part number TS3121P.

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