TS27M4C, TS27M4I, TS27M4M

Precision low power CMOS quad operational amplifiers

Features

- Low power consumption: 150 µA/op
- Output voltage can swing to ground
- Excellent phase margin on capacitive loads
- Unity gain stable
- Two input offset voltage selections

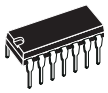
Description

These devices are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the ST silicon gate CMOS process allowing an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

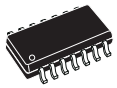
Three power consumptions are available thus offering the best consumption-speed ratio for your application:

- ICC = 10 µA/amp: TS27L4 (very low power)
- ICC = 150 µA/amp: TS27M4 (low power)
- ICC = 1 mA/amp: TS274 (standard)

These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see *Figure 4 on page 7*).



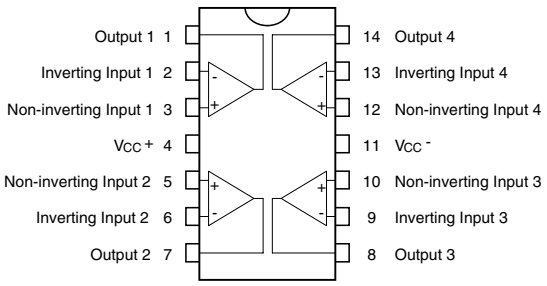
DIP14
(Plastic package)



SO14
(Plastic micropackage)

TSSOP14
(Thin shrink small outline package)

Pin connections (top view)



1 Circuit schematics

Figure 1. Block diagram

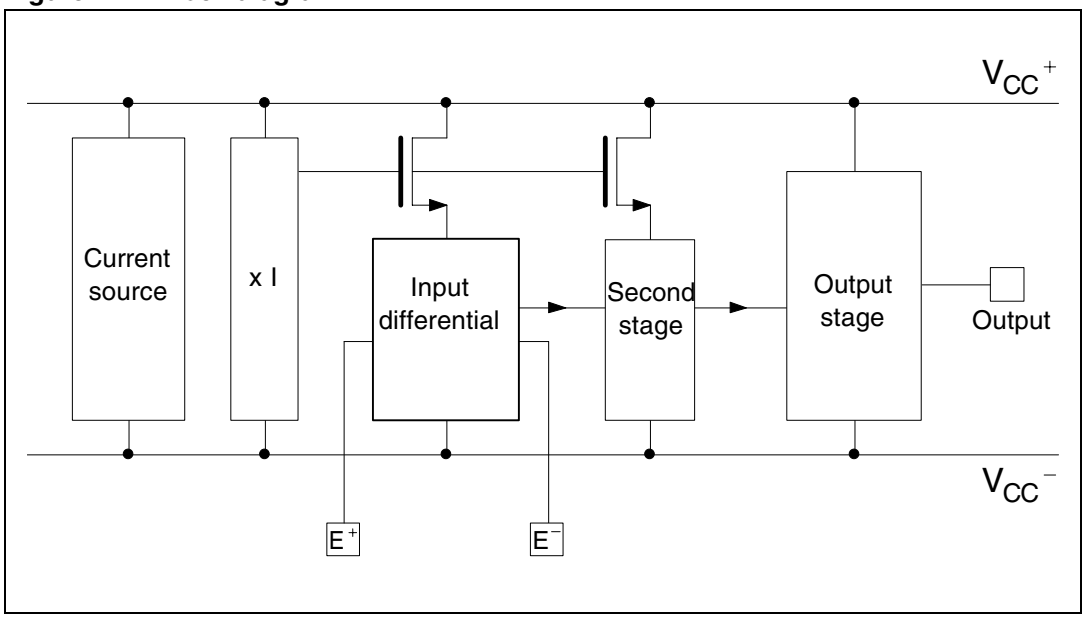
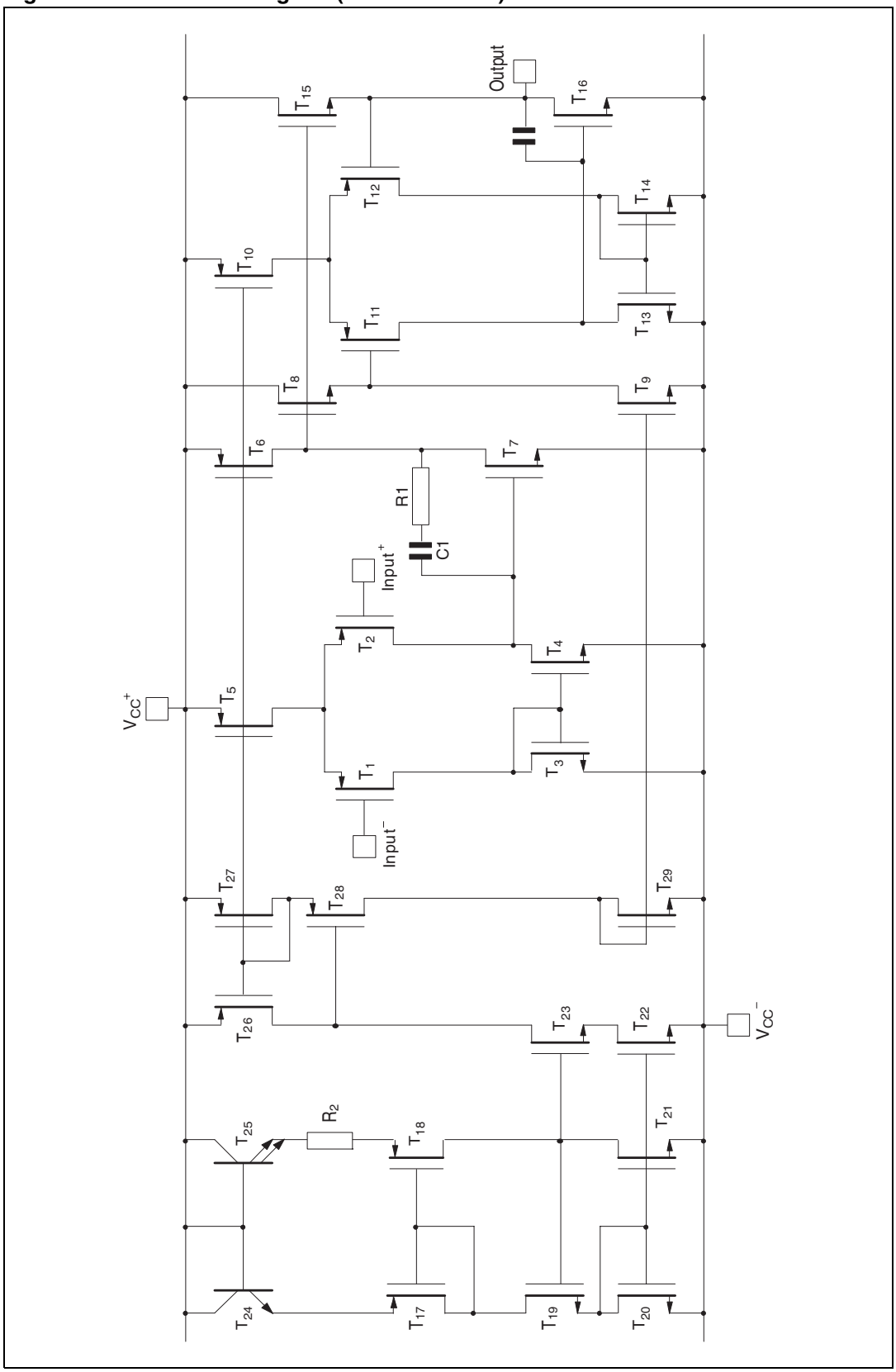


Figure 2. Schematic diagram (for 1/4 TS27M4)



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	TS27M4C/AC	TS27M4I/AI	TS27M4M/AM	Unit
V_{CC}+	Supply voltage (1)	18			V
V_{id}	Differential input voltage (2)	±18			V
V_{in}	Input voltage (3)	-0.3 to 18			V
I_o	Output current for $V_{CC}^+ \geq 15V$	±30			mA
I_{in}	Input current	±5			mA
T_{oper}	Operating free-air temperature range	0 to +70	-40 to +125	-55 to +125	°C
T_{stg}	Storage temperature range	-65 to +150			°C
R_{thja}	Thermal resistance junction to ambient (4) SO-14 TSSOP14 DIP14	 105 100 80			°C/W
R_{thjc}	Thermal resistance junction to case (4) SO-14 TSSOP14 DIP14	 31 32 33			°C/W
ESD	HBM: human body model(5)	1			kV
	MM: machine model(6)	100			V
	CDM: charged device model(7)	1.5			kV

1. All values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply voltage	3 to 16	V
V_{icm}	Common mode input voltage range	0 to V_{CC}^+ - 1.5	V

3 Electrical characteristics

Table 3. V_{CC}^+ = +10 V, V_{CC}^-= 0 V, T_{amb} = +25° C (unless otherwise specified)

Symbol	Parameter	TS27M4C/AC			TS27M4I/AI TS27M4M/AM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input offset voltage V_O = 1.4V, V_{ic} = 0V TS27M4C/I/M TS27M4AC/AI/AM $T_{min} \le T_{amb} \le T_{max}$ TS27M4C/I/M TS27M4AC/AI/AM		 1.1 0.9 	 10 5 12 6.5		 1.1 0.9 	 10 5 12 6.5	mV
DV_{io}	Input offset voltage drift		2			2		µV/°C
I_{io}	Input offset current note (1) V_{ic} = 5V, V_O = 5V $T_{min} \le T_{amb} \le T_{max}$		1	 100		1	 200	pA
I_{ib}	Input bias current (1) V_{ic} = 5V, V_O = 5V $T_{min} \le T_{amb} \le T_{max}$		1	 150		1	 300	pA
V_{OH}	High level output voltage V_{id} = 100mV, R_L = 100kΩ $T_{min} \le T_{amb} \le T_{max}$	8.7 8.6	8.9		8.7 8.5	8.9		V
V_{OL}	Low level output voltage V_{id} = -100mV			50			50	mV
A_{vd}	Large signal voltage gain V_{iC} = 5V, R_L = 100kΩ, V_o = 1V to 6V $T_{min} \le T_{amb} \le T_{max}$	30 20	50		30 10	50		V/mV
GBP	Gain bandwidth product A_v = 40dB, R_L = 100kΩ, C_L = 100pF, f_{in} = 100kHz		1			1		MHz
CMR	Common mode rejection ratio V_{iC} = 1V to 7.4V, V_o = 1.4V	65	80		65	80		dB
SVR	Supply voltage rejection ratio V_{CC}^+ = 5V to 10V, V_o = 1.4V	60	80		60	80		dB
I_{CC}	Supply current (per amplifier) A_v = 1, no load, V_o = 5V $T_{min} \le T_{amb} \le T_{max}$		150	200 250		150	200 300	µA
I_o	Output short-circuit current V_o = 0V, V_{id} = 100mV		60			60		mA
I_{sink}	Output sink current V_o = V_{CC}, V_{id} = -100mV		45			45		mA
SR	Slew rate at unity gain R_L = 100kΩ, C_L = 100pF, V_i = 3 to 7V		0.6			0.6		V/µs

Table 3. V_{CC}^+ = +10 V, V_{CC}^-= 0 V, T_{amb} = +25° C (unless otherwise specified) (continued)

Symbol	Parameter	TS27M4C/AC			TS27M4I/AI TS27M4M/AM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
ϕm	Phase margin at unity gain A_v = 40dB, R_L = 100kΩ, C_L = 100pF		45			45		Degrees
K_{OV}	Overshoot factor		30			30		%
e_n	Equivalent input noise voltage f = 1kHz, R_s = 100Ω		38			38		$\frac{nV}{\sqrt{Hz}}$
V_{o1}/V_{o2}	Channel separation		120			120		dB

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Figure 3. Supply current (each amplifier) versus supply voltage

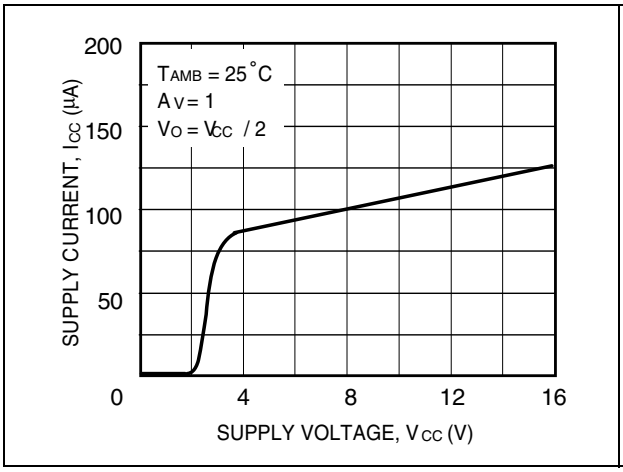


Figure 4. Input bias current versus free air temperature

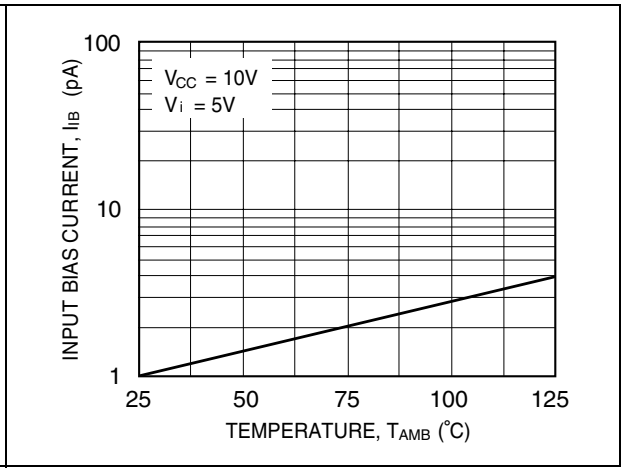


Figure 5. High level output voltage versus high level output current

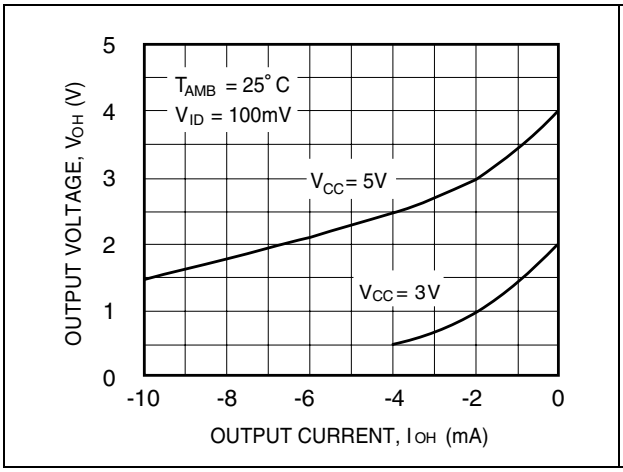


Figure 6. High level output voltage versus high level output current

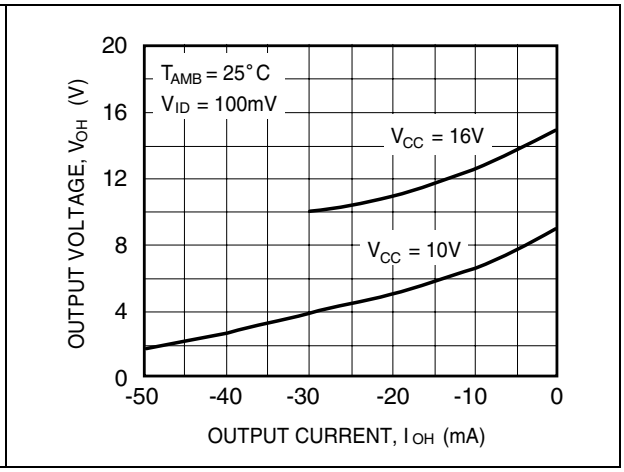


Figure 7. Low level output voltage versus low level output current

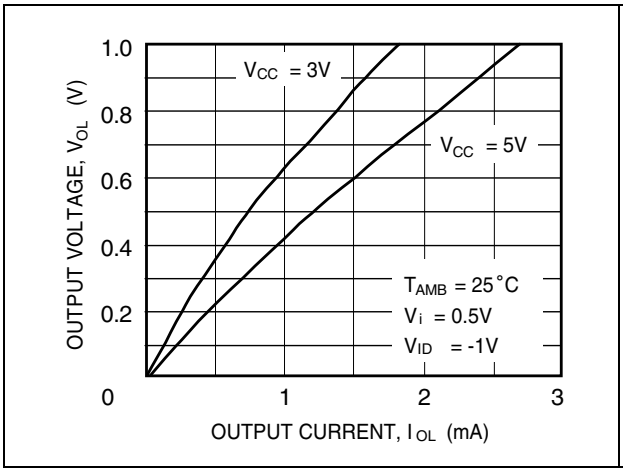


Figure 8. Low level output voltage versus low level output current

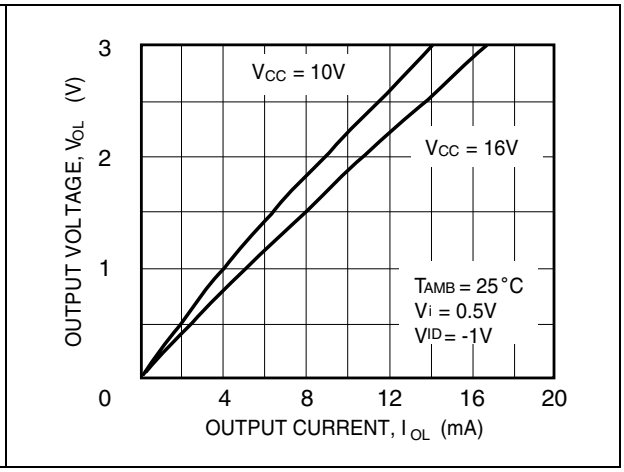


Figure 9. Open loop frequency response and phase shift

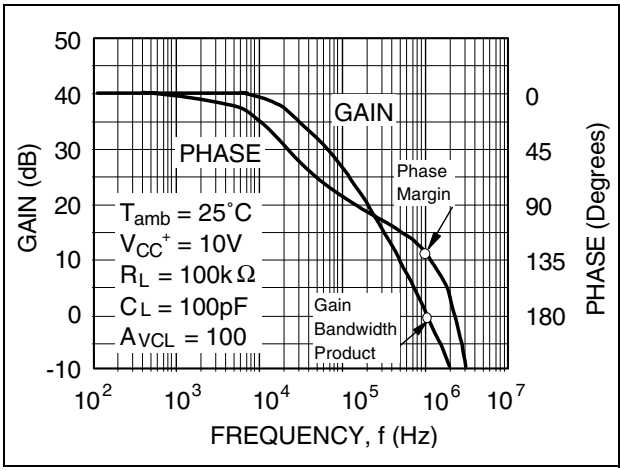


Figure 10. Gain bandwidth product versus supply voltage

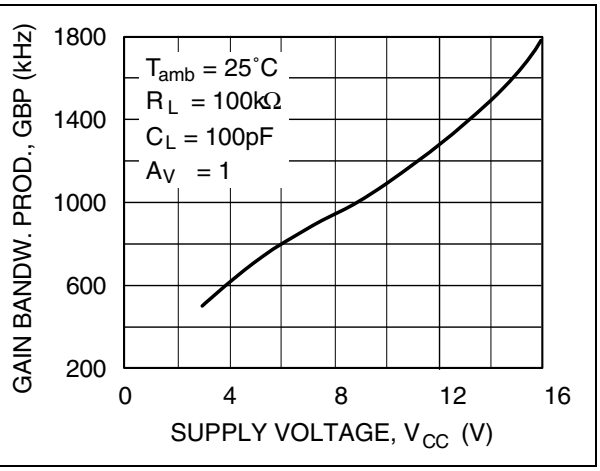


Figure 11. Phase margin versus supply voltage

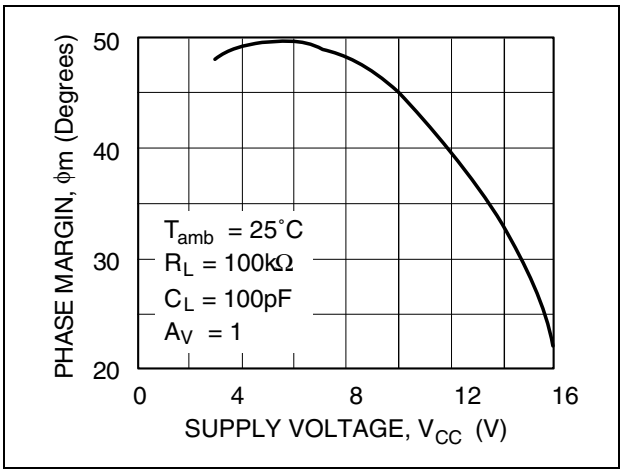


Figure 12. Phase margin versus capacitive load

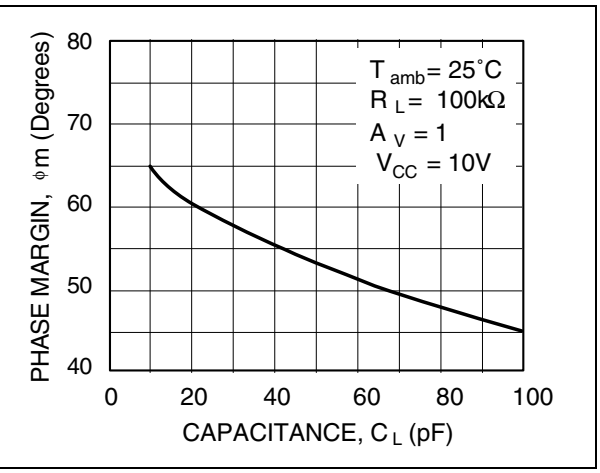


Figure 13. Slew rate versus supply voltage

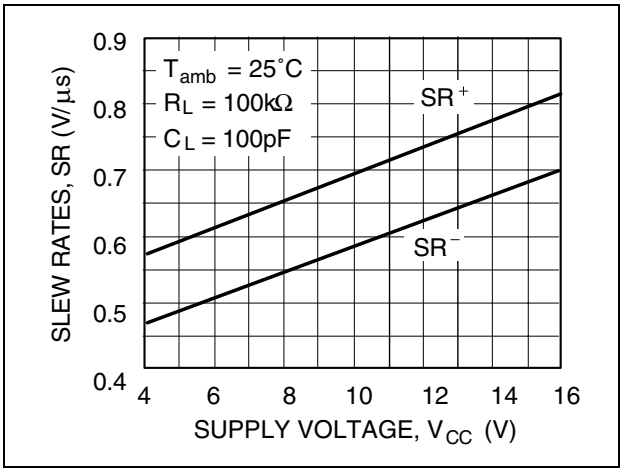
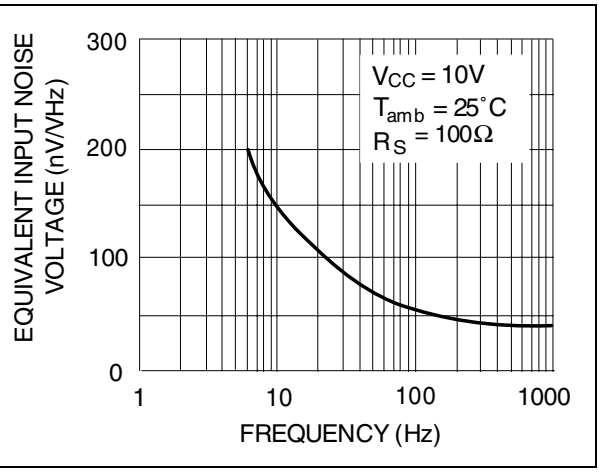


Figure 14. Input voltage noise versus frequency



4 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

4.1 DIP14 package information

Figure 15. DIP14 package mechanical drawing

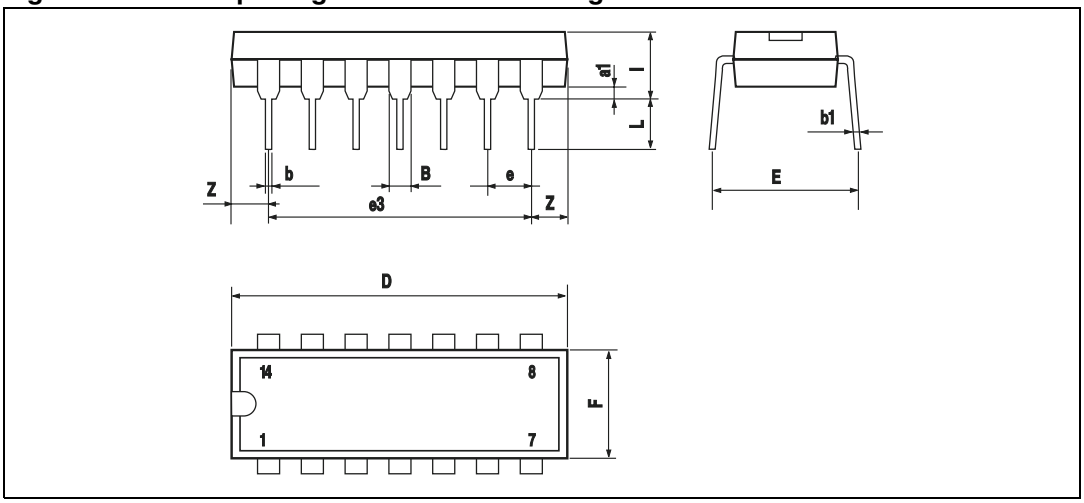


Table 4. DIP14 package mechanical data

Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

4.2 SO-14 package information

Figure 16. SO-14 package mechanical drawing

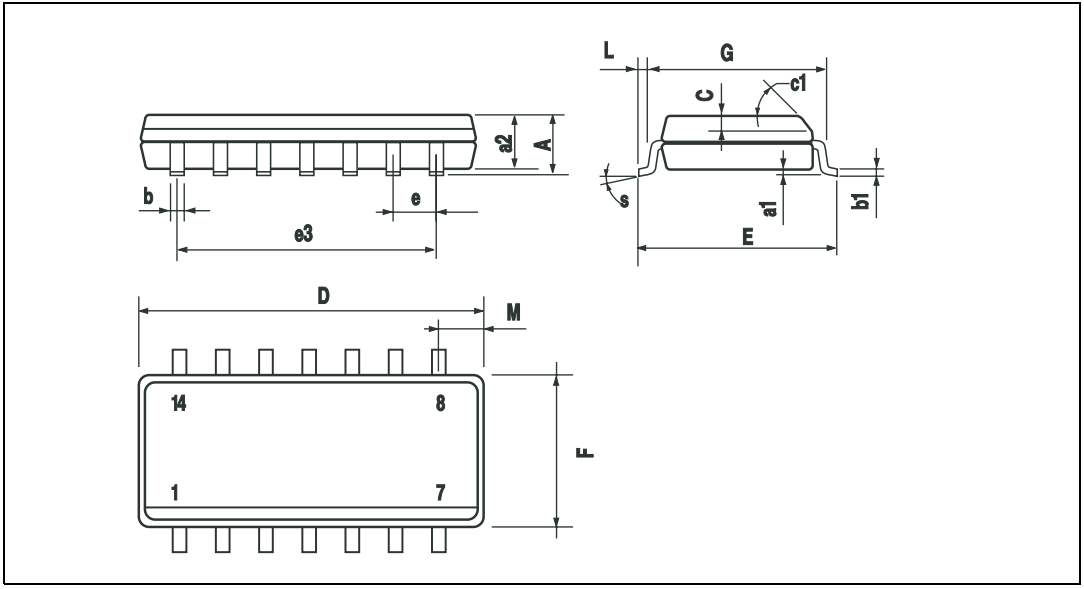


Table 5. SO-14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

4.3 TSSOP14 package information

Figure 17. TSSOP14 package mechanical drawing

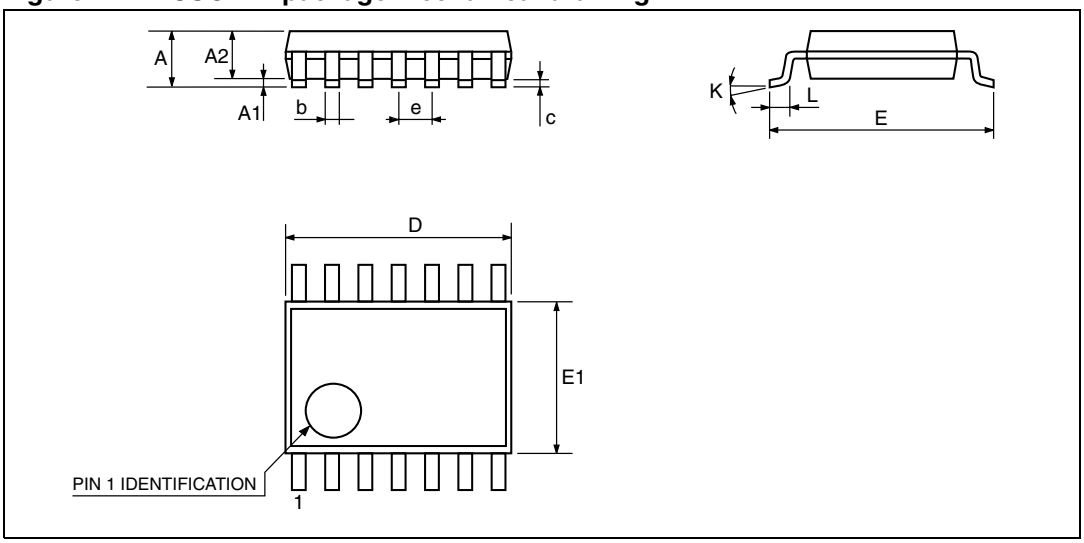


Figure 18. TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L1	0.45	0.60	0.75	0.018	0.024	0.030

5 Ordering information

Table 6. Order codes

Order code	Temperature range	Package	Packing	Marking
TS27M4CD TS27M4CDT	0°C, +70°C	SO-14	Tube or Tape & reel	27M4C
TS27M4ACD TS27M4ACDT				27M4AC
TS27M4CN TS27M4ACN		DIP14	Tube	TS27M4CN
				TS27M4ACN
TS27M4CPT TS27M4ACPT		TSSOP14	Tape & reel	27M4C
				27M4AC
TS27M4ID TS27M4IDT	-40°C, +125°C	SO-14	Tube or Tape & reel	27M4I
TS27M4AID TS27M4AIDT				27M4AI
TS27M4IN TS27M4AIN		DIP14	Tube	TS27M4IN
				TS27M4AIN
TS27M4IPT TS27M4AIPT		TSSOP14	Tape & reel	27M4I
				27M4AI
TS27M4MD TS27M4MDT	-55°C, +125°C	SO-14	Tube or Tape & reel	27M4M
TS27M4AM TS27M4AMDT				27M4AM
TS27M4MN TS27M4AMN		DIP14	Tube	TS27M4MN
				TS27M4AMN
TS27M4MPT TS27M4AMPT		TSSOP14	Tape & reel	27M4M
				27M4AM

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
07-Jan-2001	1	Initial release.
08-Sep-2008	2	Removed TS27M4B version of device. Added R_{thja}, R_{thjc}, and ESD parameters in *Table 1: Absolute maximum ratings (AMR)*. Expanded *Table 6: Order codes*. Updated document format.

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