72V, Parallelable, 4-Switch Buck-Boost Controller for GaN FETs and Si MOSFETs

FEATURES

- Wide V_{IN} Voltage Range: 5V to 72V
- Single Inductor Architecture Allows V_{IN} Above, Below, or Equal to Regulated V_{OUT}
- Synchronous Rectification: up to 99% Efficiency
- Compatible with GaN FETs and Si MOSFETs
- ±1% Output Voltage Accuracy: 1V ≤ V_{OUT} ≤ 72V
- DCR or R_{SENSE} Current Sensing
- Peak Current-Mode Control in Buck/Boost/Buck-Boost Mode
- Programmable Input or Output Current Regulation
- Continuously Programmable Dead Time (0 to 100ns)
- Phase-Lockable Frequency (150kHz to 1MHz)
- Multiphase/Multi-IC Parallel Operation
- V_{IN} Overvoltage Protection
- Selectable Continuous or Pulse-Skipping Mode Operation and Inductor Peak Current Limits
- 48-Lead, 7mm × 7mm LFCSP with Exposed Pad Package, IPC-9592 High-Voltage Spacing Compliant

APPLICATIONS

- Industrial and Telecom Systems
- Distributed DC Power or Battery Backup Systems

GENERAL DESCRIPTION

The LT7930 is a high-performance, buck-boost switching regulator controller that operates from an input voltage above, below, or equal to the output voltage. The constant-frequency, peak current mode architecture allows a phase-lockable switching frequency of up to 1MHz, while a programmable input or output current loop regulates the average input or output current for accurately supporting battery charging applications. With a wide 5V to 72V input and output range and seamless, low-noise transitions between operating regions, the LT7930 is ideal for 48V input systems.

The LT7930 features forced continuous mode (FCM)/ pulse-skipping mode operation. It supports multiphase/ multi-IC parallel operation for high-power applications. The LT7930 includes 5V optimized N-channel gate drivers to drive GaN FETs or NMOS FETs. Its dead time can be continuously programmed with an external resistor, allowing short dead time for GaN FETs or longer dead time for Si MOSFETs in order to maximize efficiency. The LT7930 also provides V_{IN} overvoltage protection, smart $EXTV_{CC}$ auxiliary supply, and programmable inductor peak current limit. A PGOOD pin indicates when the output is within 10% of its designed set point.

The LT7930 is packaged in a low-profile, 48-lead LFCSP that is compliant with the IPC-9592 high-voltage pin spacing standard.

TYPICAL APPLICATION

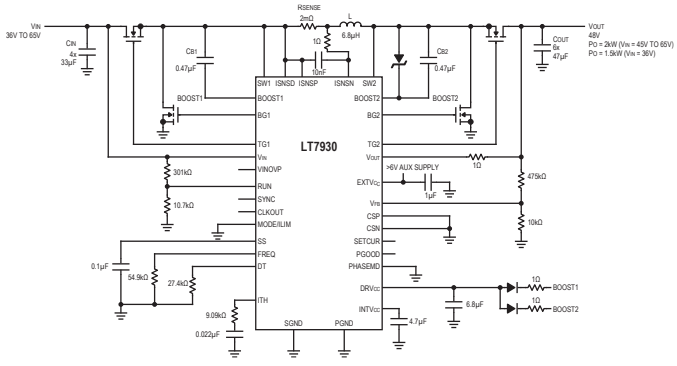

Figure 1. 36V_{IN} to 65V_{IN}, 48V_{OUT} Output Buck-Boost Converter

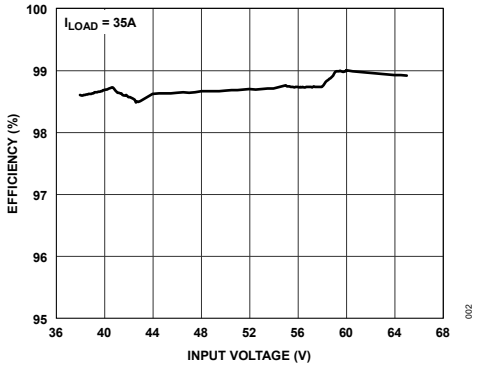

Figure 2. Efficiency vs. Input Voltage

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	7/26	Initial Release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are at T_A = 25°C, V_{IN} = 12V, RUN > 1.25V unless otherwise noted. (2))

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Bias Supply (V_{IN}, $EXTV_{CC}$)						
Bias Input Supply Operating Voltage Range	V_{IN}		5		72	V
Auxiliary Bias Voltage Operating Range	$EXTV_{CC}$		5		72	V
V_{IN} Supply Current (Shutdown Mode)	I_Q	V_{IN} = 5V, RUN = 0V, $EXTV_{CC}$ = 0V		70	100	µA
V_{IN} Supply Current (Standby Mode)	I_Q	V_{IN} = 5V, RUN = 0.9V, $EXTV_{CC}$ = 0V		3		mA
Controller Operation						
Output Voltage Operating Range	V_{OUT}		1		72	V
Regulated Feedback Voltage	V_{FB}	ITH = 1.2V (4), -40°C ≤ T_J ≤ +125°C	0.99	1.00	1.01	V
V_{FB} Pin Current	I_{VFB}	(4)		–50	–100	nA
Reference Voltage Line Regulation	$V_{REFLNREG}$	V_{IN} = 12V to 72V (4)		0.01	0.2	%
Output Voltage Load Regulation	$V_{LOADREG}$	Measure in servo loop, ΔITH voltage = 1.2V to 1.8V		0.05	0.2	%
		Measure in servo loop, ΔITH voltage = 1.2V to 0.6V		–0.05	–0.2	%
Error Amplifier Transconductance	G_M	ITH = 1.2V (4), sink/source = 10µA		2		mmho
DRV_{CC} Undervoltage Lockout	$UVLO_DRV_{CC}$	DRV_{CC} ramping down	3.3	3.7	4	V
DRV_{CC} Undervoltage Hysteresis	UVLO_DRV_HYS			0.45		V
$INTV_{CC}$ Undervoltage Lockout	$UVLO_INTV_{CC}$	$INTV_{CC}$ ramping down		3.5		V
$INTV_{CC}$ Undervoltage Hysteresis	UVLO_INTV_HYS			0.4		V
RUN Pin Threshold 1 (Shutdown to Standby)	V_{RUN}	V_{RUN} rising	0.3	0.57		V
RUN Pin Threshold 2 (Standby to on)	V_{RUN}	V_{RUN} rising	1.1	1.22	1.3	V
RUN Pin Source Current	I_{RUN}	V_{RUN} < 0.57V		1		µA
		0.57V < V_{RUN} < 1.2V		2		µA
		V_{RUN} > 1.2V		6		µA
VINOVP Pin Threshold	V_{VINOVP}	V_{VINOVP} rising	1.48	1.53	1.58	V
VINOVP Threshold Hysteresis	V_{VINOVP_HYS}			100		mV

(Specifications are at T_A = 25°C, V_{IN} = 12V, RUN > 1.25V unless otherwise noted. [2])

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Soft-Start (SS Pin) Source Current	I_{SS}			2.5		µA
Maximum Duty Cycle of Boost Mode (BG2)	DMAX_BG2			90		%
Inductor Current Sensing						
Maximum Inductor Peak Current-Sense Threshold	$V_{SENSE(ILMAX)}$	MODE/ILIM < $INTV_{CC}$/2, ITH = 2.025V, $V_{ISNSP} - V_{ISNSD}$ = 25mV, -40°C ≤ T_J ≤ +125°C	18	25	32	mV
		MODE/ILIM > $INTV_{CC}$/2, ITH = 2.025V, $V_{ISNSP} - V_{ISNSD}$ = 50mV, -40°C ≤ T_J ≤ +125°C	40	50	60	mV
		MODE/ILIM < $INTV_{CC}$/2, ITH = 2.025V, $V_{ISNSP} = V_{ISNSD}$, -40°C ≤ T_J ≤ +125°C	92	100	108	mV
		MODE/ILIM > $INTV_{CC}$/2, ITH = 2.025V, $V_{ISNSP} = V_{ISNSD}$, -40°C ≤ T_J ≤ +125°C	190	200	210	mV
ISNSD Pin Leakage Current	I_{ISNSD}			0	±0.1	µA
ISNSN Pin Leakage Current	I_{ISNSN}			0	±0.1	µA
Input/Output Average Current Regulation						
CSP Pin Input Current	I_{CSP}	$V_{CSP} = V_{CSN}$ > 5V, $V_{CSP} - V_{CSN}$ = 50mV		14	20	µA
CSN Pin Input Current	I_{CSN}	$V_{CSP} = V_{CSN}$ > 5V, $V_{CSP} - V_{CSN}$ = 50mV		14	20	µA
CSP/CSN Pin Current Mismatch	ΔI_{CS}	V_{CSP} = 12V, $V_{CSP} - V_{CSN}$ = 50mV		0.05	±1	µA
Maximum Average Current Limit	$V_{MAX(IAVG)}$	V_{CSP} = 12V, -40°C ≤ T_J ≤ +125°C	46.5	50	53	mV
SETCUR Pin Output Current	I_{SETCUR}		14	15	16	µA
DRV_{CC} and $INTV_{CC}$ Linear Regulators						
DRV_{CC} Regulation Voltage	V_{DRVCC}	V_{IN} = 12V, $EXTV_{CC}$ = 0V	4.9	5	5.1	V
		V_{IN} = 5V, $EXTV_{CC}$ = 12V	4.9	5	5.1	V
DRV_{CC} Voltage Load Regulation	V_{DRVCC_LREG}	$IDRV_{CC}$ = 0mA to 55mA, V_{IN} = 12V		1	2	%
$INTV_{CC}$ Regulation Voltage	V_{INTVCC}		4.4	4.5	4.6	V
Oscillator and Phase-Locked Loop						
FREQ Pin Output Current	I_{FREQ}		9	10	11	µA
Low Fixed Switching Frequency	$f_{SW(MIN)}$	V_{FREQ} = 0V		80		kHz

(Specifications are at T_A = 25°C, V_{IN} = 12V, RUN > 1.25V unless otherwise noted. (2))

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
High Fixed Switching Frequency	$f_{SW(MAX)}$	V_{FREQ} = 5V		1280		kHz
Synchronizable Frequency	f_{SW_SYNC}	SYNC = external clock	150		1000	kHz
SYNC Pin Input Threshold	V_{TH_SYNC}	SYNC pin rising		1.2	2	V
		SYNC pin falling	0.5	0.9		V
SYNC Pin Input Resistance to Ground	R_{SYNC}			500		kΩ
Clock Output High Voltage			4.3	4.5		V
Clock Output Low Voltage				0	0.2	V
Power Good						
PGOOD Trip Level, V_{FB} Respect to Set Regulated Voltage	V_{PGOOD}	V_{FB} ramping negative		–10		%
PGOOD Trip Level, V_{FB} with Respect to Set Regulated Voltage	V_{PGOOD}	V_{FB} ramping positive		10		%
PGOOD Open-Drain On-Resistance	R_{PGOOD}			55		Ω
PGOOD Leakage Current	I_{PGOOD}	V_{PGOOD} = 6V			±1	µA
Dead Time						
Gate Off to Gate On, R_{DT} = 20kΩ	$t_{D,20k\Omega}$	R_{DT} = 20kΩ, no load on gate driver	2	4	7	ns
Gate Off to Gate On, R_{DT} = 66kΩ	$t_{D,66k\Omega}$	R_{DT} = 66kΩ, no load on gate driver	35	40	45	ns
Gate Drivers						
Top Driver Pull-Up On-Resistance	R_{TG1}, R_{TG2}	BOOST – SW = 5V		3		Ω
Top Driver Pull-Down On-Resistance	R_{TG1}, R_{TG2}	BOOST – SW = 5V		1		Ω
Bottom Driver Pull-Up On-Resistance	R_{BG1}, R_{BG2}	DRV_{CC} = 5V		3.5		Ω
Bottom Driver Pull-Down On-Resistance	R_{BG1}, R_{BG2}	DRV_{CC} = 5V		1		Ω

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
Input and Output Voltage (V_{IN}, V_{OUT})	–0.3V to +75V
Topside Driver Voltages (BOOST1, BOOST2)	–0.3V to +80/85([11])V
Switch Voltages (SW1, SW2)	–5V to +75/80([11])V
(BOOST1 – SW1), (BOOST2 – SW2)	–0.3V to +8V
Inductor Current-Sense Voltages (ISNSP, ISNSN, ISNSD)	–5V to +75V
Input/Output Current-Sense Voltages (CSP, CSN)	–0.3V to +75V
$EXTV_{CC}$ Voltage	–0.3V to +75V
RUN Voltage	–0.3V to +12V
PGOOD Voltage	–0.3V to +6V
ITH, V_{FB} , DT Voltages	–0.3V to $INTV_{CC}$
PHASMD, SETCUR, SS Voltages	–0.3V to $INTV_{CC}$
FREQ, SYNC, CLKOUT Voltages	–0.3V to $INTV_{CC}$
MODE/ILIM, VINOVP Voltages	–0.3V to $INTV_{CC}$
DRV_{CC} Peak Current ([10])	100mA
TG1, BG1, TG2, BG2	[9]
Operating Junction Temperature Range ([2],[3])	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C

1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

2 The LT7930 is tested under pulsed load conditions such that $T_J \approx T_A$. The LT7930 is guaranteed to meet specifications from –40°C to +125°C junction temperature. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than +125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula: $T_J = T_A + (P_D \times \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

3 When $V_{IN} > EXTV_{CC}$ and $EXTV_{CC} > 4.8V$, V_{BIAS} supply current is transferred to the $EXTV_{CC}$ pin to reduce the total input supply quiescent current.

4 The LT7930 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}. The specifications at –40°C and +125°C are not tested in production and are assured by design, characterization, and correlation to production testing at other temperatures.

5 Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the *Applications Information* section.

6 Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

7 The minimum on-time condition is specified for an inductor peak-to-peak ripple current > 40% of $I_{L(MAX)}$ (see Minimum On-Time Considerations in the *Applications Information* section).

8 The LT7930 includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature is exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

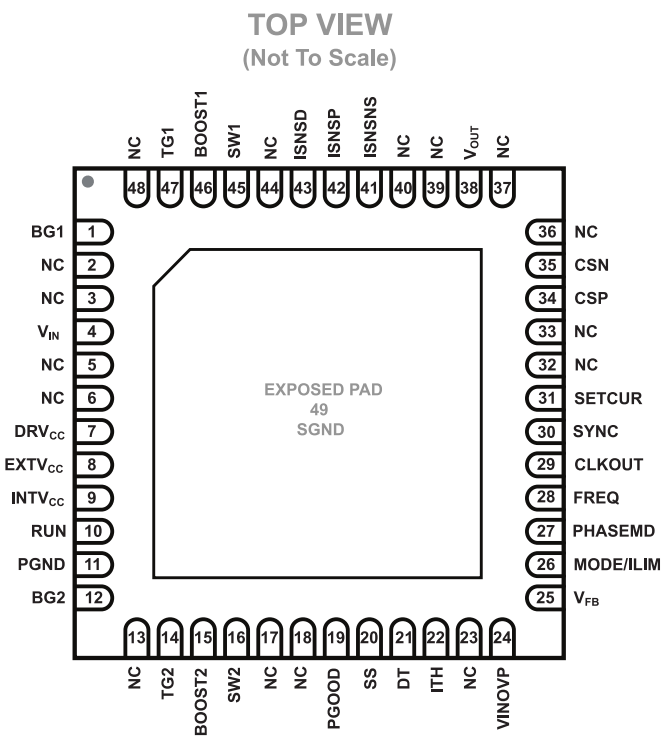
9 Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

10 Guaranteed by design.

11 SW1, SW2 absolute maximum voltage of 80V and BOOST1, BOOST2 absolute maximum voltage of 85V are guaranteed by design for transients less than 100ns.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

48 LFCSP



UK PACKAGE
48-LEAD (7mm × 7mm) LFCSP
IPC-9592 High Voltage Spacing Compliant
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 49) IS SGND, MUST BE SOLDERED TO PCB

Pin Descriptions

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1, 12	BG1, BG2	Bottom Gate Driver Outputs. These pins drive the gates of the bottom FETs between PGND and DRV_{CC}.
4	V_{IN}	Main IC Supply. Power input to the internal LDO connected to DRV_{CC}. Bypass this pin to PGND with a capacitor (0.1µF to 1µF) close to the pin.
7	DRV_{CC}	Gate Driver Current Supply LDO Output. The voltage on this pin is regulated to 5V from either V_{IN} or $EXTV_{CC}$ during normal operation. Bypass this pin to PGND with a low-ESR tantalum or ceramic capacitor with a minimum capacitance of 4.7µF and at least 8 times the sum of C_{BST1} and C_{BST2}.
8	$EXTV_{CC}$	External Power Input to an Internal LDO Connected to DRV_{CC}. When the voltage on this pin is greater than 4.8V and lower than the V_{IN} pin voltage,

PIN	NAME	DESCRIPTION
		this LDO bypasses the internal LDO powered from V_{IN}. Bypass this pin to PGND with a capacitor (0.1µF to 1µF) close to the pin.
9	$INTV_{CC}$	Internal 4.5V Regulator Output. The control circuits are powered from this voltage. Bypass this pin to SGND with a minimum of 4.7µF low-ESR tantalum or ceramic capacitor.
10	RUN	Enable Control Input. A voltage above 1.22V turns on the IC. There is a 2µA pull-up current on this pin. Once the RUN pin rises above the 1.22V threshold, the pull-up increases to 6µA.
11	PGND	Power Ground. Connect this pin closely to the sources of the bottom FETs and negative terminal of the V_{IN}, DRV_{CC}, $EXTV_{CC}$ bypass capacitor.
14, 47	TG2, TG1	Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to DRV_{CC} superimposed on the switching node voltages.
15, 46	BOOST2, BOOST1	Bootstrapped Supplies to the Top-Side Floating Drivers. Capacitors are connected between the BOOST and SW pins, and Schottky diodes are tied between the BOOST and DRV_{CC} pins. Voltage swing at the BOOST1 pin is from DRV_{CC} to (V_{IN} + DRV_{CC}). Voltage swing at the BOOST2 pin is from DRV_{CC} to (V_{OUT} + DRV_{CC}).
16, 45	SW2, SW1	Switch Node Connections. Normally connected to the inductor terminals. SW1 swings from a Schottky diode voltage drop below ground up to V_{IN}, and SW2 swings from a Schottky diode voltage drop below ground up to V_{OUT}. A bootstrap capacitor (0.1µF to 1µF) should be placed from each SW pin as close as possible to the corresponding BOOST pin.
19	PGOOD	Power-Good Indicator Output for the Regulated Output Voltage. Open-drain logic output that is pulled down to ground when the regulated output voltage exceeds the ±10% regulation window after the internal 30µs power bad mask timer expires.
20	SS	Soft-Start Input. The voltage ramp rate at this pin sets the output voltage ramp rate of the regulated voltage. A capacitor to ground accomplishes soft-start. This pin has a 2.5µA pull-up current.
21	DT	Dead-Time Programming. A resistor between this pin and SGND pin sets the dead time. See the *Programmable Dead Time (DT Pin)* section for more details.
22	ITH	Current Control Threshold and Error Amplifier Compensation Point. The current comparator's threshold varies with the ITH control voltage. The compensation network is from the ITH pin to SGND.
24	VINOVP	V_{IN} Overvoltage Protection. The controller stops switching when the voltage on this pin exceeds 1.53V and resumes switching when the voltage drops below 1.43V. Float or short this pin to SGND if not used.
25	V_{FB}	Output Voltage Sensing Error Amplifier Noninverting Input. This pin receives the remotely sensed feedback voltage from the external resistor divider across the output voltage.

PIN	NAME	DESCRIPTION
26	MODE/ILIM	FCM/Pulse-Skipping Mode and Inductor Current-Limit Programming. Tying this pin to GND or $INTV_{CC}$ enables FCM operation, otherwise the controller works in pulse-skipping mode. Tying this pin to a voltage lower than half of $INTV_{CC}$ enables the low current limit, while higher than half of $INTV_{CC}$ enables the high current limit. See the *Applications Information* section for details.
27	PHASMD	Phase Mode Programming. This pin sets the phase relationship between the internal oscillator clock and the output clock on the CLKOUT pin. Tying this pin to SGND sets 180° phase-shift, floating this pin sets 120° phase-shift, and tying this pin to $INTV_{CC}$ sets 90° phase-shift. See the *Applications Information* section for details.
28	FREQ	Frequency Setting. A resistor between this pin and SGND sets the switching frequency. This pin sources 10µA current.
29	CLKOUT	Clock Output. Use this pin to synchronize the switching frequency of multiple LT7930 ICs for parallel operations. Signal swings are from $INTV_{CC}$ to ground.
30	SYNC	Switching Frequency Synchronization. Applying an external clock between 150kHz and 1MHz causes the switching frequency to synchronize to the external clock. If SYNC is low, a resistor from the FREQ pin to SGND sets the default switching frequency. This pin has a 500kΩ internal resistor to ground.
31	SETCUR	Average Current Regulation. A resistor from this pin to SGND sets the maximum average input or output current sensed by the CSP and CSN pins. This pin sources 15µA current.
34, 35	CSP, CSN	Average Current Sensing. The positive/negative inputs of the internal rail-to-rail average current-sense amplifier (CSA).
38	V_{OUT}	Floating Driver Bias in Boost Mode. Supplies the bias current for the BOOST1 to SW1 driver circuitry when V_{OUT} is much higher than V_{IN}.
41	ISNSN	Negative Current-Sense Comparator Inputs. The negative input of the current comparator is normally connected to the DCR-sensing network.
42	ISNSP	Positive Current-Sense Comparator Inputs. This pin must be Kelvin-connected to the inductor on the switching node SW1.
43	ISNSD	DC Current-Sense Comparator Inputs. These inputs amplify the DC portion of the sensed current signal to the IC's current comparator. If no use in large DCR applications, short the ISNSD pin to the ISNSP pin locally. See the *Applications Information* section for details.
49	SGND	Exposed Pad Signal Ground. Must be soldered to the PCB ground for rated thermal performance. All small signal components, such as $INTV_{CC}$, SS, ITH, V_{FB}, and FREQ, should be connected here.
2, 3, 5, 6, 13, 17, 18, 23, 32, 33,	NC	No Connect. Always keep these pins floating. These pins are intentionally skipped to isolate adjacent pins.

PIN	NAME	DESCRIPTION
36, 37, 39, 40, 44, 48		

TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = +25°C, unless otherwise noted.)

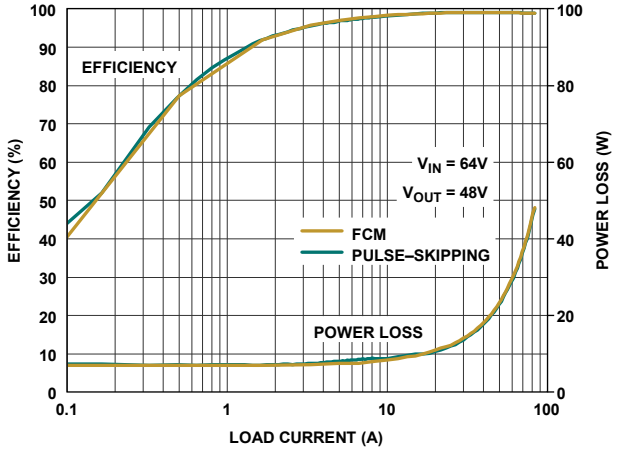


Figure 3. Efficiency and Power Loss vs. Load Current (2-Phase Buck Mode)

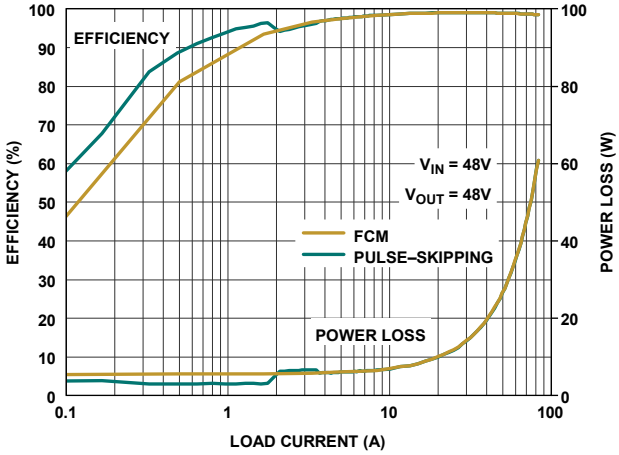


Figure 4. Efficiency and Power Loss vs. Load Current (2-Phase Buck-Boost Mode)

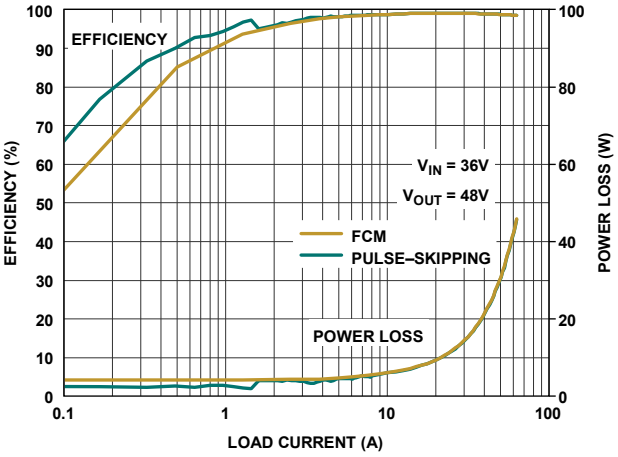


Figure 5. Efficiency and Power Loss vs. Load Current (2-Phase Boost Mode)

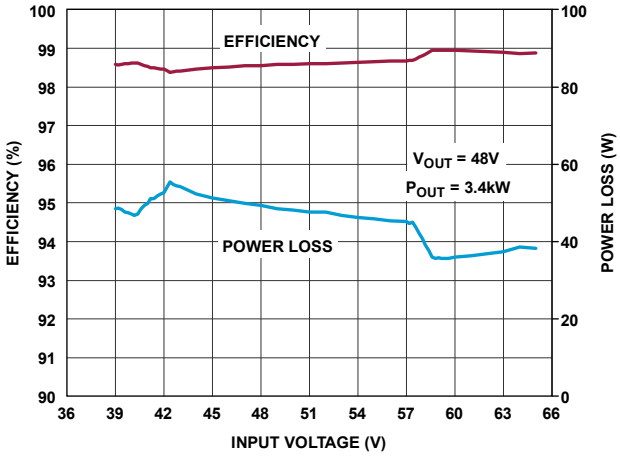


Figure 6. Efficiency and Power Loss vs. V_{IN} (2 Phase)

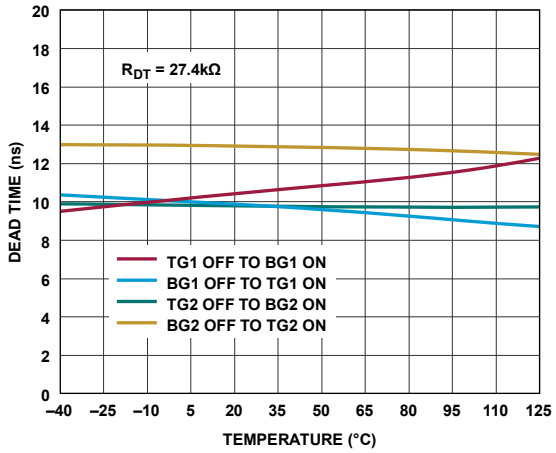


Figure 7. Dead Time vs. Temperature

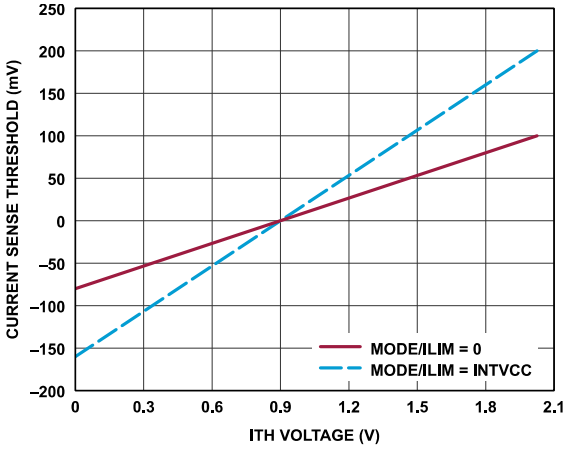


Figure 8. Current-Sense Threshold vs. ITH Voltage

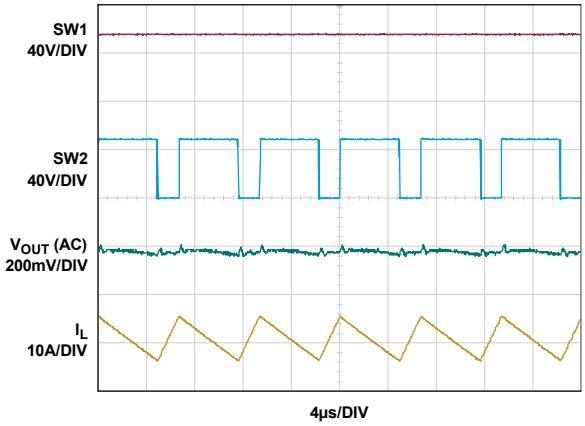


Figure 9. FCM Operation Boost Region ($36V_{IN}$, $48V_{OUT}$)

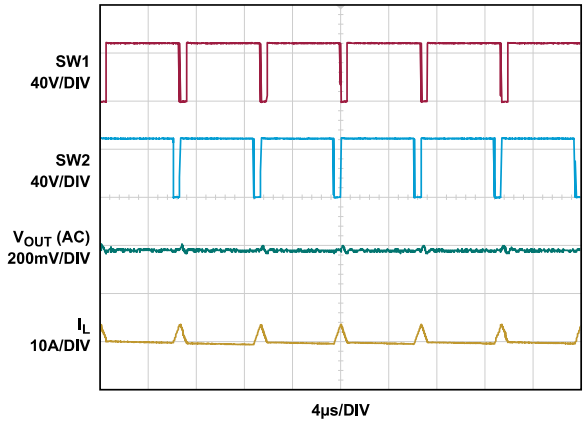


Figure 10. FCM Operation Buck-Boost Region ($48V_{IN}$, $48V_{OUT}$)

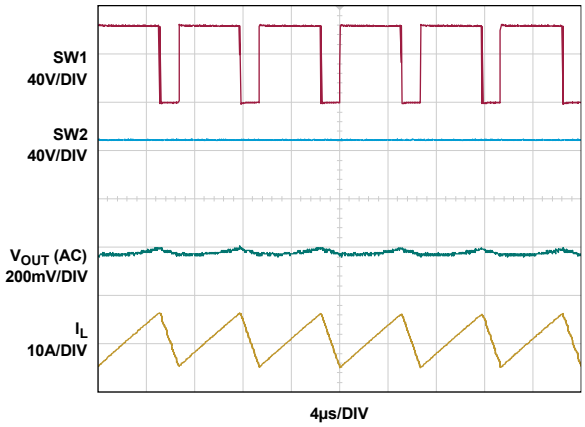


Figure 11. FCM Operation Buck Region ($64V_{IN}$, $48V_{OUT}$)

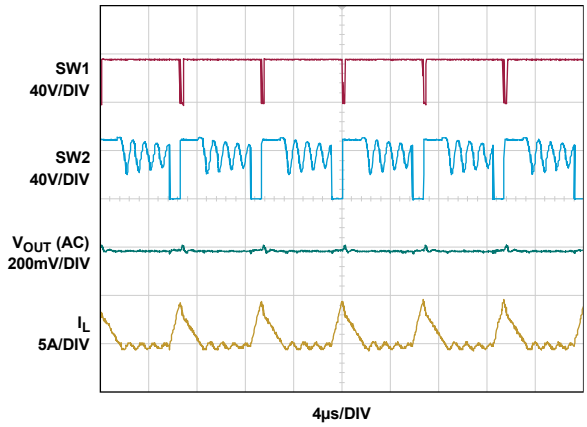


Figure 12. Pulse-Skipping Mode Waveforms with 500mA Load ($36V_{IN}$, $48V_{OUT}$)

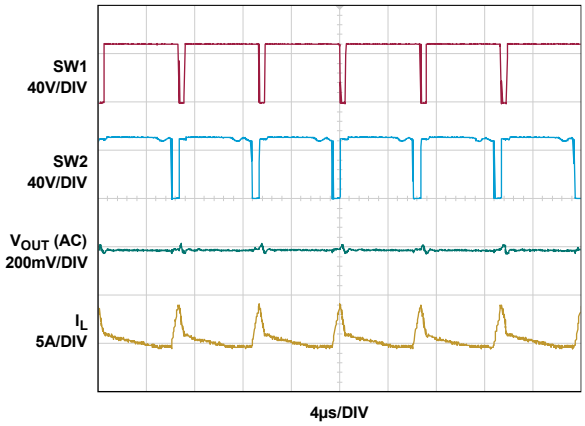


Figure 13. Pulse-Skipping Mode Waveforms with 500mA Load ($48V_{IN}$, $48V_{OUT}$)

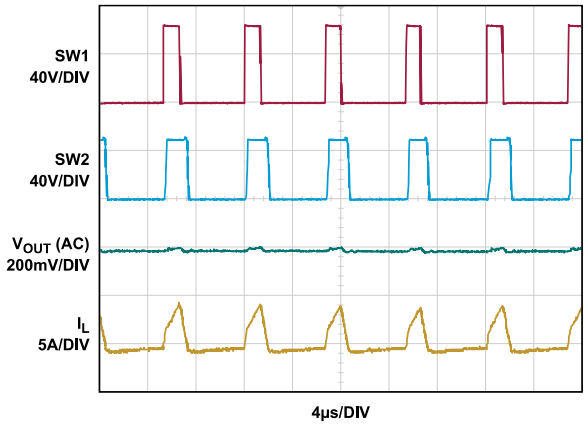


Figure 14. Pulse-Skipping Mode Waveforms with 500mA Load ($64V_{IN}$, $48V_{OUT}$)

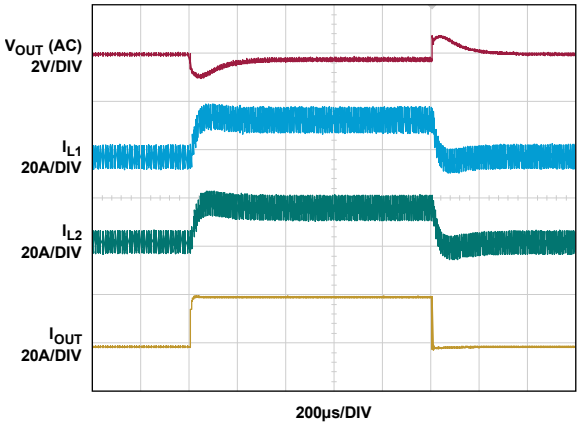


Figure 15. 2-Phase Parallel Operation Load Step ($36V_{IN}$, $48V_{OUT}$)

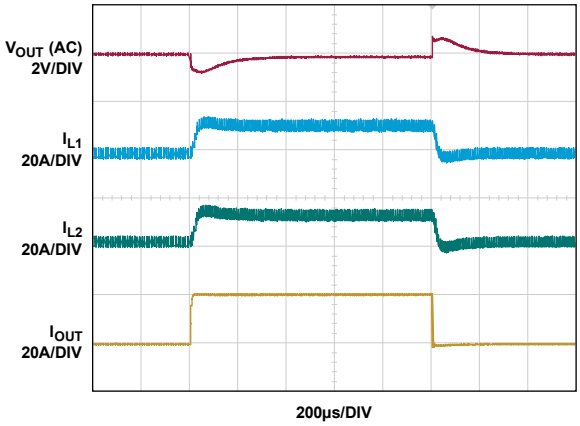


Figure 16. 2-Phase Parallel Operation Load Step ($48V_{IN}$, $48V_{OUT}$)

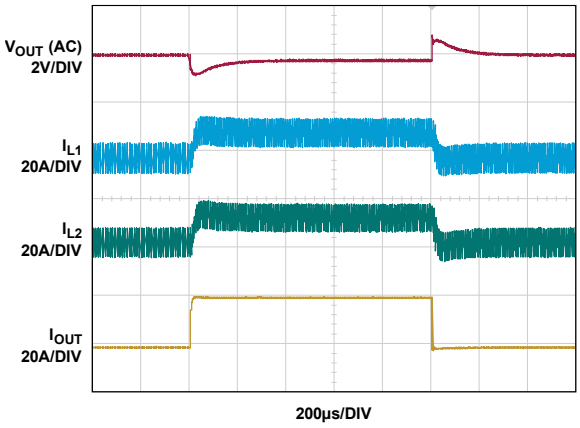


Figure 17. 2-Phase Parallel Operation Load Step ($64V_{IN}$, $48V_{OUT}$)

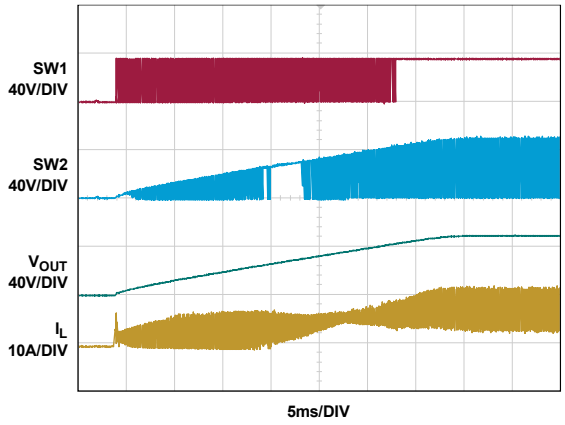


Figure 18. Boost Mode Startup with 10Ω Load ($36V_{IN}$ to $48V_{OUT}$)

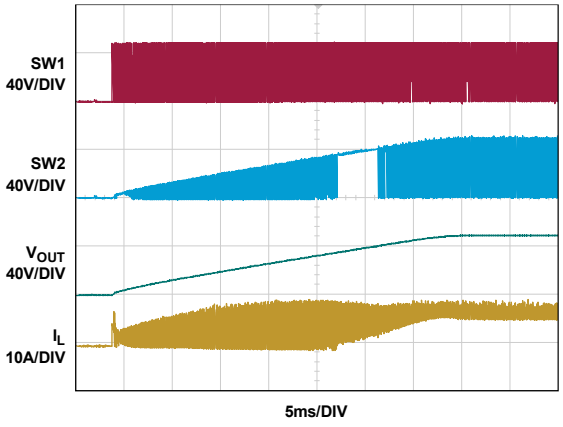


Figure 19. Buck-Boost Mode Startup with 10Ω Load ($48V_{IN}$ to $48V_{OUT}$)

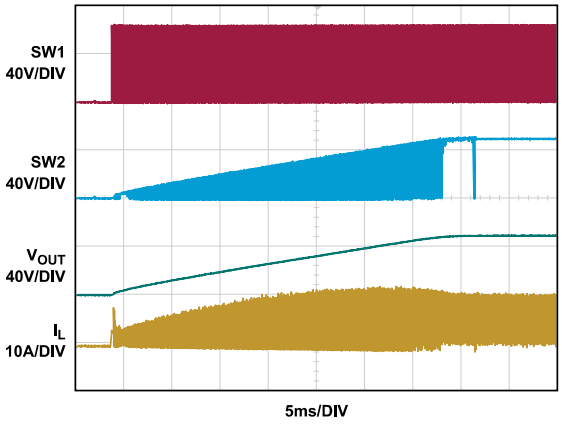
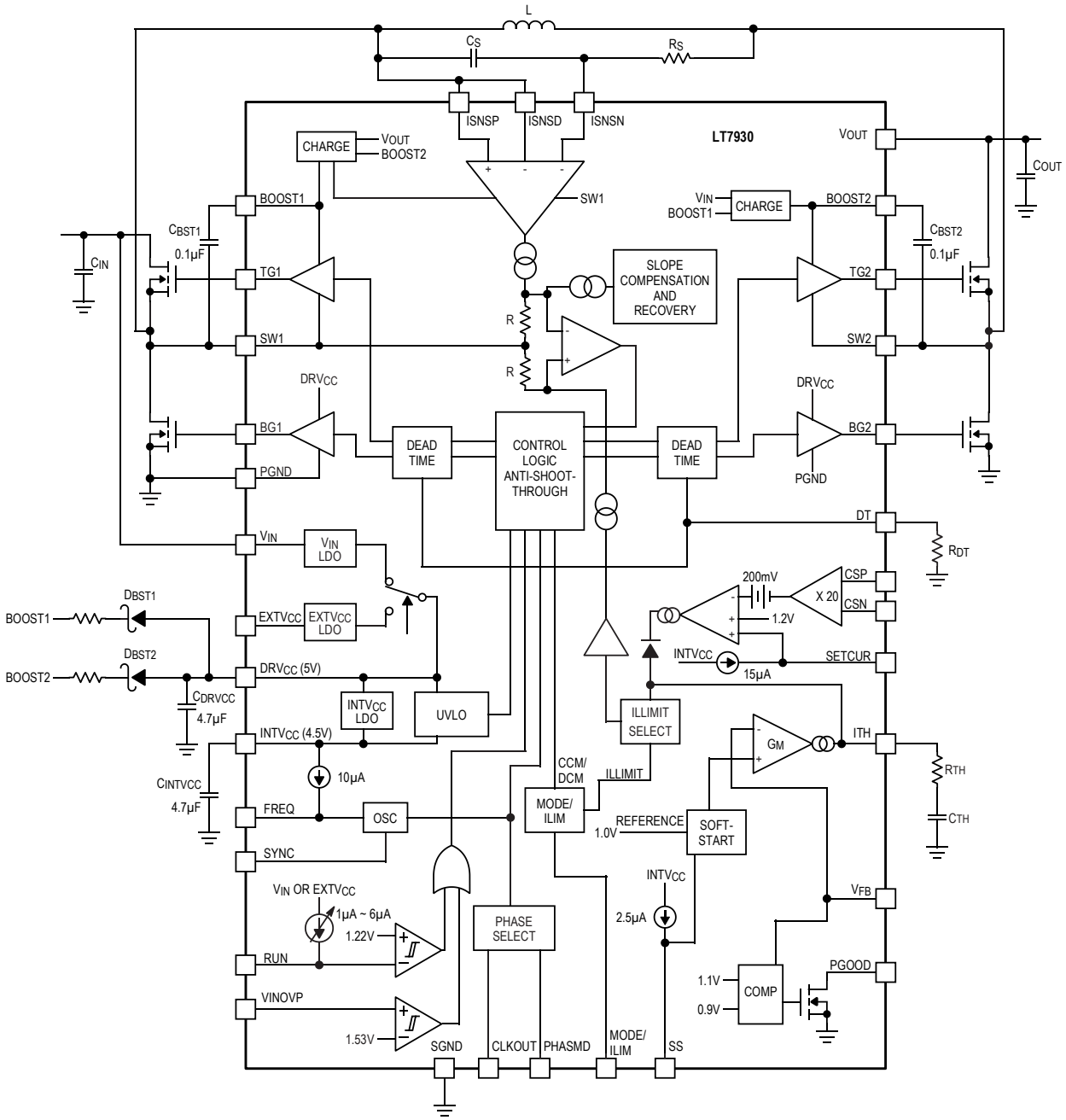


Figure 20. Buck Mode Startup with 10Ω Load ($64V_{IN}$ to $48V_{OUT}$)

BLOCK DIAGRAM



THEORY OF OPERATION

Main Control Loop

The LT7930 is a constant-frequency, peak current-mode controller for 4-switch buck-boost converters that can regulate an output voltage above, below, or equal to the input voltage. The Analog Devices-proprietary current-sensing and control architecture employs inductor DC resistance (DCR) for current sensing and closed-loop regulation. The inductor peak current is controlled by the voltage on the ITH pin, which is the output of the error amplifier (EA). The V_{FB} pin receives the voltage feedback signal and is compared with the internal 1.0V reference voltage by the EA. If the input or output average current regulation loop is implemented, the inductor current is controlled by either the output feedback voltage or the input/output average current.

DRV_{CC} Power

Power for the top and bottom FET drivers and most other internal circuitry is derived from the DRV_{CC} pin. When the $EXTV_{CC}$ supply is not used, an internal 5V linear regulator supplies DRV_{CC} power from V_{IN}. If $EXTV_{CC}$ is connected to an external voltage source such as the output of the buck-boost converter, another 5V linear regulator under $EXTV_{CC}$ may be enabled and supply DRV_{CC} power. The LT7930 internally chooses the V_{IN} linear regulator or $EXTV_{CC}$ linear regulator to supply DRV_{CC} power based on the operation mode and to supply voltages for minimizing IC power loss and reducing IC temperature. Either V_{IN} or $EXTV_{CC}$ can supply the IC separately. If one of the power supplies on V_{IN} or $EXTV_{CC}$ fails, the LT7930 can still operate normally with the other input supply on V_{IN} or $EXTV_{CC}$. Both V_{IN} and $EXTV_{CC}$ can withstand voltages as high as 72V.

Start-up and Shutdown Control (RUN Pin)

The LT7930 is in shutdown mode when the RUN pin is pulled down and lower than 0.5V. In shutdown mode, most internal circuitry is turned off, including the DRV_{CC}/$INTV_{CC}$ regulators, and the LT7930 consumes less than 100µA current. All of the driver outputs are actively low to turn off the external FETs. Releasing RUN allows an internal 1µA current to pull up this pin and enable the converter. When the RUN pin voltage is higher than 0.5V and lower than 1.22V, the LT7930 is in standby mode. The DRV_{CC}/$INTV_{CC}$ regulators and all of the internal circuitry are enabled, but output switching is disabled. After the RUN pin is higher than 1.22V, the LT7930 is in active mode and starts switching while regulating the output voltage. The RUN pin may be externally pulled up or driven directly by logic. Alternatively, the RUN pin can be controlled by a resistor-divider from V_{IN} to SGND to achieve programmable V_{IN} undervoltage lockout (UVLO). Customers may design the converter to start up at the preprogrammed V_{IN} voltage with different resistor-divider values. Do not exceed the absolute maximum rating of 12V on the RUN pin.

The startup of the converter's output (V_{OUT}) is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.0V internal reference, the LT7930 regulates the V_{FB} voltage to the SS voltage instead of the 1.0V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to SGND. An internal 2.5µA pull-up current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.0V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. During startup, the LT7930 operates in pulse-skipping mode to avoid the negative inductor current and output voltage discharging. When RUN is pulled low to disable the controller, or when DRV_{CC} is below the UVLO threshold of 3.7V, the SS pin is pulled low by an internal MOSFET. In UVLO, the controller is disabled and the external FETs are held off.

Power Switch Control

The simplified *Block Diagram* shows how the four power switches are connected to the inductor, V_{IN}, V_{OUT}, and GND. The LT7930 operates in the buck region ($V_{IN} >> V_{OUT}$), boost region ($V_{IN} << V_{OUT}$), and buck-boost region ($V_{IN} \approx V_{OUT}$)

without sensing the V_{IN} and V_{OUT} voltage. The power switches are properly controlled so that the transfer between regions is continuous and smooth.

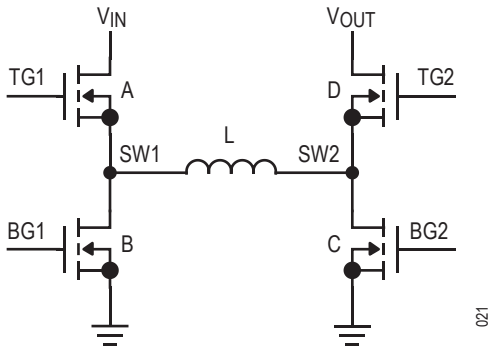


Figure 21. Simplified Diagram of the Output Switches

Buck Region (V_{IN} >> V_{OUT})

Switch D is always on, and switch C is always off in this region. Switches A and B alternate, behaving like a typical synchronous buck regulator. The LT7930 operates like a conventional buck controller with peak current-mode control. The inductor peak current is regulated and proportional to the voltage on the ITH pin. As the input voltage decreases and is close to the output voltage, the duty cycle of switch A in buck mode increases. Once the duty cycle reaches 83%, the LT7930 enters the buck-boost region as the input voltage decreases.

Buck–Boost Region (V_{IN} ≈ V_{OUT})

When V_{IN} is close to V_{OUT}, the controller enters the buck-boost region. To maintain peak current-mode control, the current comparator needs to be tripped each cycle by the inductor peak current. However, at V_{IN} = V_{OUT}, the inductor current is flat and has no peak to trip the current comparator in buck or boost mode operation. To create an inductor peak current, when the duty cycle is larger than 83% in buck mode operation and the current comparator has not been tripped, switches A and C are turned on to force the inductor current to ramp up quickly until the current comparator is tripped. The peak inductor current is still controlled by the voltage on the ITH pin with a cycle-by-cycle peak current limit. As the input voltage keeps decreasing and the buck mode duty cycle reaches 100%, the LT7930 enters boost mode naturally.

Boost Region (V_{IN} << V_{OUT})

Switch A is always on and synchronous switch B is always off in the boost region. Switches C and D alternate, behaving like a typical synchronous boost regulator. The LT7930 operates like a conventional peak current-mode control boost controller. In every cycle, switch C is turned on first; the inductor current is regulated and proportional to the voltage on the ITH pin with the same peak current limit as the buck mode. The maximum duty cycle of switch C in boost mode operation is around 90%. As a result, the maximum step-up ratio of the LT7930 in FCM mode is around 10.

Pulse-Skipping Mode and Light Load Current Operation (MODE/ILIM Pin)

The LT7930 can be set to enter pulse-skipping mode or FCM using the MODE/ILIM pin. To select forced continuous operation, tie the MODE/ILIM pin to SGND or $INTV_{CC}$. To select pulse-skipping mode, tie the MODE/ILIM pin to a voltage equivalent of 2/3 of $INTV_{CC}$ (e.g., a 10kΩ/20kΩ resistor-divider from $INTV_{CC}$ to SGND) or leave it floating. The MODE/ILIM pin is a multifunctional pin. It not only sets the operation mode but also programs the peak current limits. See *Table 4* for the MODE/ILIM pin setup.

Table 4. MODE/ILIM Pin Setup

MODE/ILIM PIN	CURRENT-SENSE THRESHOLD (ISNSD SHORT TO ISNSP)	OPERATION MODE
SGND	100mV	Forced continuous
Float	100mV	Pulse skipping
2/3 $INTV_{CC}$	200mV	Pulse skipping
$INTV_{CC}$	200mV	Forced continuous

When the LT7930 is in FCM, the light load operation is the same as the heavy load operation with a constant switching frequency, and the output voltage ripple is minimized. When the LT7930 enters pulse-skipping mode at light load conditions, the inductor current is not allowed to reverse, and the synchronous switch D is held off whenever reverse current on the inductor is detected. At very light loads, the current comparator may remain tripped for many cycles and force switches A and C to stay off for the same number of cycles (i.e., skipping pulses). In the buck-boost region, the LT7930 may switch several cycles and then keep skipping pulses for a longer time at light loads until the control loop pulls ITH high. The pulse-skipping mode decreases the switching frequency, thus improving efficiency. However, this may cause a larger output voltage ripple at light loads.

When the LT7930 is in pulse-skipping mode, a sufficiently light load can cause the inductor current to fall to zero. Once this happens, switch D is turned off for the remaining cycle along with switch C. During this interval, no switch is actively driving the SW2 node, allowing its voltage to ring. The minimum voltage reached during this ringing is limited by the reverse-conduction characteristics of switch C. For GaN FETs, their reverse conduction voltage is typically around 2V. If a GaN FET is used for switch C, the SW2 node can ring down to –2V, which may lead to overcharging of capacitor C_{BST2}. When the LT7930 is set to operate in pulse-skipping mode with GaN FETs, a Schottky diode should be placed in parallel with switch C to clamp the minimum SW2 voltage. This Schottky diode will absorb the SW2 node ringing energy when it rings negative. A 1A-rated Schottky diode is sufficient to use here.

If the LT7930 is instead set to enter FCM, then a 5V Zener diode across C_{BST2} is sufficient to clamp the capacitor voltage during the start-up pulse-skipping phase, ensuring a smooth transition into FCM afterward. These additional diodes are unnecessary when switch C is a Si MOSFET.

Output Overvoltage Operation

If the output voltage is higher than the value commanded by the V_{FB} resistor-divider, the LT7930 responds according to the mode and region of operation. In continuous conduction mode, the LT7930 sinks current into the input. If the input supply is capable of sinking current, the LT7930 allows the reverse inductor current to be sunk into the input. The maximum valley current of the reverse inductor current is approximately 80% of the maximum peak inductor current in the positive direction. In pulse-skipping mode, switching stops and the output is allowed to remain high.

Constant-Current Regulation (CSP/CSN/ SETCUR Pins)

The LT7930 provides a constant-current regulation loop for either input or output average current. A sensing resistor close to the input or output capacitor can be used to sense the input or output current. Because the input or output current may be a pulse current in the different operation regions, an RC filter must be applied on the CSP and CSN pins for average current sensing. When the voltage on the current-sensing resistor exceeds the programmed current limit, the voltage on the ITH pin is pulled low to decrease the inductor current and maintain the desired maximum input or output current. The current limit may be set by the voltage on the SETCUR pin from 0.2V to 1.2V corresponding to the linear 0mV to 50mV current limit on the sensing resistor. There is a 15µA current out of the SETCUR pin. If the SETCUR pin is floating or the SETCUR pin voltage is higher than 1.2V, the current limit is clamped at 50mV internally. The input current-limit function prevents the DC input source from overloading, while the output

current limit provides a building block for battery charger or LED driver applications. It can also serve as an extra current-limit protection for a constant-voltage regulation application. The input/output current-limit function has an operating voltage range of GND to the maximum operating voltage V_{OUT}/V_{IN} (72V).

Frequency Selection and Phase-Locked Loop (FREQ, SYNC, PHASMD, and CLKOUT Pins)

Switching frequency selection is a trade-off between efficiency and component size. Low-frequency operation increases efficiency by reducing FET switching losses, but requires larger inductance and/or capacitance to maintain a low output ripple voltage. The switching frequency of the LT7930's controllers can be selected using the FREQ pin. If the SYNC pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 80kHz to 1280kHz. Switching frequency is determined by the voltage on the FREQ pin. Because there is a precision 10µA current flowing out of the FREQ pin, the user can program the controller's switching frequency with a single resistor to SGND (e.g., the FREQ pin voltage is 1V with a 100kΩ resistor from the FREQ pin to SGND). The curve in *Figure 22* shows the relationship between the FREQ pin resistor and the switching frequency.

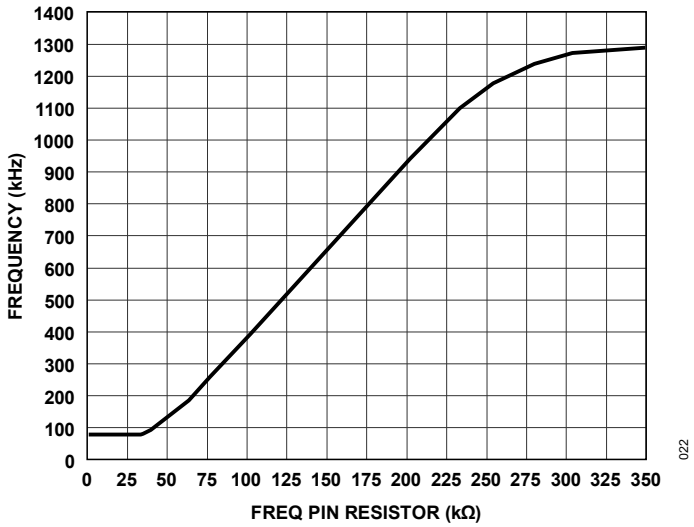


Figure 22. Relationship between Switching Frequency and FREQ Pin Resistor

A phase-locked loop (PLL) is integrated on the LT7930 to synchronize the internal oscillator to an external clock source driving the SYNC pin. The PLL is capable of locking to any frequency within the range of 150kHz to 1MHz. The frequency-setting resistor at the FREQ pin should always be present to set the controller's initial switching frequency before locking to the external clock or in any cases where the external clock is missing during the operation. The CLKOUT pin is a clock signal output with the same frequency as the internal oscillator with the phase shift programmed by the PHASMD pin. It may be used in multi-IC parallel applications by passing the clock signal of the first IC to the SYNC pin of the second IC for frequency synchronization. The phase shift can be programmed based on the values in *Table 5*.

Table 5. Phase-Shift Programming

PHASMD PIN	CLKOUT PHASE-SHIFT REFER TO THE INTERNAL OSCILLATOR
SGND	180°
Float	120°
$INTV_{CC}$	90°

Programmable Dead Time (DT Pin)

The LT7930 dead time can be adjusted with a resistor between the DT pin and SGND pin. The relationship between the DT pin resistor R_{DT} and dead time is shown in *Figure 23*. When the DT pin is open, dead time is clamped at around 320ns. When dead time is less than 20ns, it can be calculated from the following equation:

$$t_D = 0.8 \times (R_{DT} - 15)$$

where dead time is in ns and R_{DT} is in kΩ. Do not use R_{DT} less than 15kΩ.

Due to FET variations and PCB layout parasitics, to avoid shoot-through, a minimum 5ns dead time is recommended for typical GaN FET applications.

Due to the large reverse conduction voltage of GaN FETs, if dead time is set above 20ns, parallel Schottky diodes must be added to the bottom GaN FETs. Schottky diodes with a 3A current rating are sufficiently large to use here.

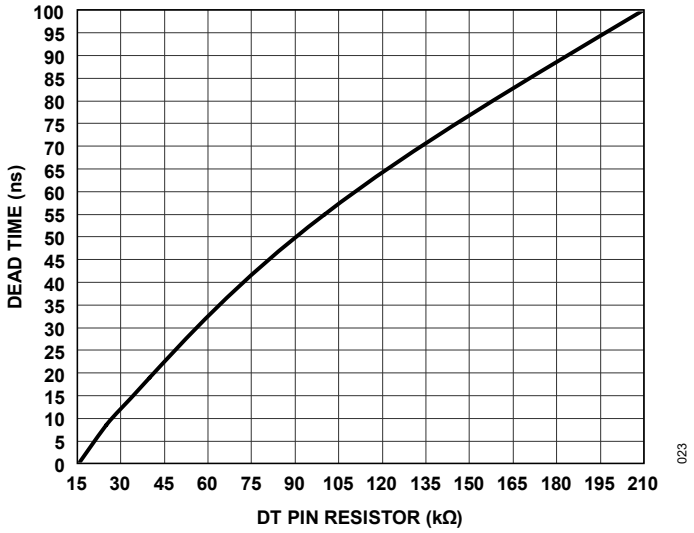


Figure 23. Dead Time vs. DT Pin Resistor

Power Good (PGOOD Pin)

The PGOOD pin is connected to the open-drain of an internal N-channel MOSFET. When V_{FB} is not within ±10% of the 1.0V reference voltage, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when RUN is below 1.22V or when the LT7930 is in the soft-start phase. There is an internal 30µs power good or bad mask when V_{FB} goes in or out of the ±10% window. The PGOOD pin can be pulled up by an external resistor to $INTV_{CC}$ or an external source of up to 6V.

V_{IN} Overvoltage Protection (VINOVP Pin)

The LT7930 offers programmable input overvoltage protection to protect the V_{IN} side from overvoltage conditions. The LT7930 has a comparator that monitors and compares the VINOVP pin voltage. When the VINOVP pin exceeds 1.53V, the controller enters standby mode, and the DRV_{CC}/$INTV_{CC}$ regulators and all of the internal circuitry are enabled, but no switching is happening. Once the pin voltage drops below 1.43V, the LT7930 enters active mode and resumes switching and regulating the output voltage. Float or short the VINOVP pin to SGND if this function is not used.

Short-Circuit Protection, Current Limit, and Current-Limit Foldback

The maximum peak current threshold of the controller is limited by a voltage clamp on the ITH pin. In normal operation, the ITH voltage varies from 0.9V to 2.025V corresponding to the peak inductor current-sensing voltage of 0mV to 100mV (MODE/ILIM tied to SGND and ISNSD tied to ISNSP). The LT7930 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 40% of its nominal output level, then the maximum sense voltage is progressively lowered from its maximum value to one-fifth of the maximum value. Foldback current limiting is disabled during soft-startup. Under short-circuit conditions, the LT7930 will limit the current by operating as a buck with very low duty cycles and by skipping cycles. In this situation, synchronous switch B dissipates most of the power (though less than in normal operation).

Compensation Loop (ITH Pin)

The LT7930 uses an internal transconductance error amplifier, the output of which (ITH) compensates the control loop. The external inductor, output capacitor, and compensation resistor and capacitor determine the loop stability. The compensation design is similar to the traditional buck or boost converter with peak current mode control. For a typical voltage regulator application, a 5kΩ resistor in series with a 10nF compensation capacitor on the ITH pin to SGND is adequate and a good starting point.

APPLICATIONS INFORMATION

The *Typical Applications* diagram is a basic LT7930 application circuit. See *Figure 31* for detailed external components. External component selection is driven by the load requirement and begins with the selection of the inductor value, DCR, and R_{SENSE}. Next, the power FETs are selected, followed by C_{IN} and C_{OUT}. This circuit can be configured for operation up to an input voltage of 72V.

Inductor Selection

The inductor selection and operating frequency are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values but with higher switching losses. The inductor value also has a direct effect on ripple current. Because the LT7930 is a constant-frequency peak current-mode controller, the inductor peak current is regulated and limited cycle by cycle. The inductor should be selected with a saturation current that is higher than the maximum peak current. The maximum output DC current in buck mode is the peak inductor current minus half of the ripple current. In boost mode, the maximum output DC current varies with duty cycle and ripple current. Too large of a ripple current reduces the maximum output current, and a smaller current ripple may lead to a small current-sense signal, which is more sensitive to switching noise. Typically, the inductor current ripple (ΔI_L) set to 30% to 60% of the maximum DC inductor current at the nominal input voltage is a good starting point. If the buck-boost converter only operates in buck mode and buck-boost mode, the maximum DC inductor current is approximately the maximum output load current. Otherwise, the maximum DC inductor current is the inductor current in boost mode with a minimum V_{IN} at the maximum load condition. It can be calculated as:

$$I_L = I_{LOAD(MAX)} \frac{V_{OUT}}{V_{OUT} - V_{IN}}$$

For high efficiency, choose an inductor with a low core loss, such as a ferrite. Also, the inductor should have as low of a DC resistance as possible to reduce I^2R losses. It must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core, or shielded bobbin inductor.

Current Sensing

The LT7930 is a peak current-mode controller that can be configured to use either inductor DC resistance (DCR) or external R_{SENSE} current sensing. The choice between the two current-sensing schemes is largely a design trade-off between cost, power consumption, and accuracy. DCR sensing is becoming popular because it saves on expensive current-sensing resistors and is more power efficient, especially in high-current applications. However, current-sensing resistors provide the more accurate current limits for the controller.

Inductor DCR Sensing

The LT7930 uses the inductor DCR for current sensing and closed-loop regulation. After selecting the inductance and saturation current, the DCR of the inductor also must be chosen properly to achieve the required output current and current limit. To sense the inductor current with a large DCR, the ISNSD pin may be shorted to the ISNSP pin to achieve 100mV or 200mV current-sense threshold limits. Choose the DCR of the inductor so that the peak current is less than the saturation current but higher than the maximum DC current plus the ripple current.

$$DCR \leq \frac{V_{SENSE(MAX)}}{I_{LOAD(MAX)} + \frac{\Delta I_L}{2}}$$

Filter components, especially capacitors, must be placed close to the LT7930, and the sense lines should run close together to a Kelvin connection underneath the current-sense element (*Figure 24*). In *Figure 25*, the external R1 x C1 time constant is chosen to be exactly equal to the L/DCR time constant; the voltage drop across the external capacitor is equal to the drop across the inductor DCR. C1 is typically selected to be in the range of 0.047µF to 0.47µF. For

example, for a 4.7µH/10mΩ inductor and C1 = 0.047µF, R1 should be L/(DCR x C1) = 10kΩ. The maximum peak inductor current is V_{SENSE}/DCR = (100mV or 200mV)/10mΩ = 10A or 20A, depending on the MODE/ ILIM pin setup. To further tune the current limit, another resistor may be paralleled with C1 to form a resistor-divider with R1 and scale the sensed voltage. Refer to the standard DCR setup in the buck controller data sheet (e.g., the LTC3855) for details.

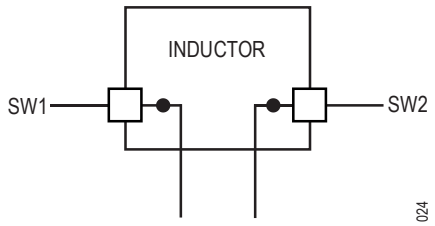


Figure 24. Sense Lines Placement with Inductor DCR

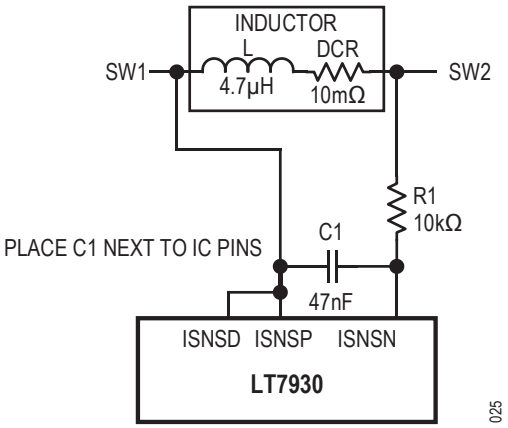


Figure 25. Inductor DCR Current Sensing

To properly size the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature. To ensure that the application delivers the full load current over the full operating temperature range, use the manufacturer's maximum value, usually given at +20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is +100°C. Consult the manufacturers' data sheets for detailed information.

To maintain a good signal-to-noise ratio (SNR) for the current-sense signal, it is suggested to have a minimum ΔV_{SENSE} larger than 10mV. For a DCR-sensing application, the minimum sensed ripple voltage ΔV_{SENSE} may be estimated by the following equation:

$$\Delta V_{SENSE} = DCR \times \Delta IL(MIN)$$

In high-current applications, a low-DCR inductor is preferred for higher efficiency. The LT7930 is designed to sense the low-DCR inductor current using an Analog Devices-proprietary sensing method without sacrificing the SNR. As shown in *Figure 26*, the low-DCR current sensing requires an additional RC filter and ISNSD pin.

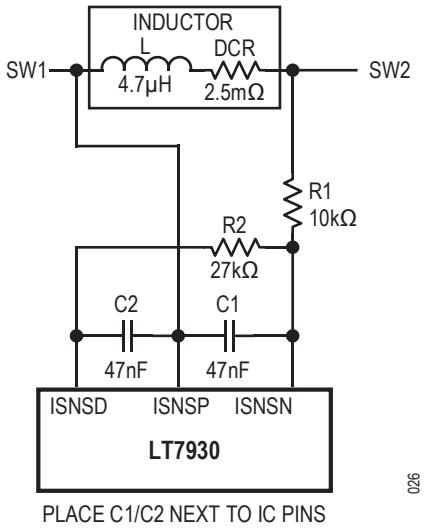


Figure 26. Small Inductor DCR Current Sensing

The external R1 x C1 time constant is chosen to be equal to the L/(4 x DCR) time constant. If the C1 = C2, then R2 = 3 x 0.9 x R1 = 2.7 x R1. For example, for a 4.7µH/2.5mΩ inductor and C1 = 0.047µF, R1 should be L/(4 x DCR x C1) = 10kΩ, and R2 should be 2.7 x R1 = 27kΩ. With this setup, the voltage drop on the inductor DCR is sensed and amplified four times larger inside the IC to be compared with 100mV or 200mV current threshold limits. Thus, the equivalent maximum current-sense voltage V_{SENSE} is limited to 100mV/4 = 25mV or 200mV/4 = 50mV, and the maximum inductor current is V_{SENSE}/DCR = 25mV/2.5mΩ = 10A if MODE/ILIM = 0. Note that, in this condition, the sensed ripple voltage is amplified to be four times larger, and the ΔV_{SENSE} may be estimated by the following equation:

$$\Delta V_{SENSE} = 4 \times DCR \times \Delta I_{L(MIN)}$$

DCR current sensing requires that the ISNSP pin is Kelvin-connected to the inductor's left terminal and shorted to SW1. The ISNSP pin and SW1 pin must be electrically shorted together.

External R_{SENSE} Current Sensing

Current sensing using an external sense resistor offers higher accuracy and a more linear measurement directly proportional to the current. It also provides the flexibility to select precise resistance values and tight tolerances, allowing consistent inductor current control, accurate current limiting, and effective current sharing, especially in multi-IC/multiphase systems. A typical sensing circuit using external R_{SENSE} is shown in *Figure 27*. R_{SENSE} is chosen based on the required output current. Similar to DCR sensing, to sense the inductor current with a large R_{SENSE}, the ISNSD pin may be shorted to the ISNSP pin to achieve 100mV or 200mV current-sense threshold limits. Choose R_{SENSE} so that the peak current is less than the saturation current, but higher than the maximum DC current plus the ripple current.

$$R_{SENSE} \leq \frac{V_{SENSE(MAX)}}{I_{LOAD(MAX)} + \frac{\Delta I_L}{2}}$$

To maintain a good SNR for the current-sense signal, it is suggested to have a minimum ΔV_{SENSE} larger than 10mV. For an external R_{SENSE} sensing application, the minimum sensed ripple voltage ΔV_{SENSE} may be estimated by the equation:

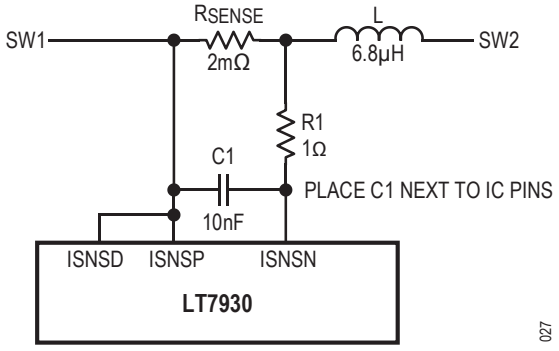


Figure 27. External R_{SENSE} Current Sensing

To reduce the effects of capacitive and inductive noise coupled into the current-sense comparator, a small RC filter can be placed near the IC. A typical filter consisting of a series 1Ω resistor and a parallel 10nF capacitor provides a good starting point. Increasing the filter size can help reduce the current comparator trip point jitter. However, increasing the filter size too much reduces the accuracy of the inductor current peak and zero-crossing detection.

For small R_{SENSE} applications, the ISNSD pin along with an additional RC filter can be used to amplify the sensed voltage without compromising the SNR. See the *Inductor DCR Sensing* section for filter design guidance and sensed voltage estimation with the ISNSD pin.

Similar to DCR current sensing, R_{SENSE} current sensing also requires the ISNSP pin to be Kelvin-connected to R_{SENSE} and shorted to SW1. The ISNSP pin and the SW1 pin must be electrically shorted together.

Set Output Voltage

The LT7930 output voltage is set by an external feedback resistive divider carefully placed across the output capacitor. The resultant feedback signal is compared to an internal precision 1.0V voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 1.0V \times \left(1 + \frac{R1}{R2}\right)$$

where R1 is connected to V_{OUT} and R2 is connected to SGND.

Program Average Input/Output Current Limit

As shown in *Figure 28* and *Figure 29*, the input/output average current-sense resistor R_{SENSE} should be placed between the V_{IN}/V_{OUT} bulk capacitor and the decoupling capacitor. A lowpass filter formed by R_F and C_F is recommended to reduce the switching noise and stabilize the current loop. Due to the same current on the CSP/CSN pins, the filter resistors R_F on CSP and CSN must be the same value. With the typical 100Ω resistors shown in the following figures, the value of capacitor C_F should be 1µF to 2.2µF to filter the pulsed input/output current at the switching frequency. The current loop's transfer function should approximate that of the voltage loop. The crossover frequency should be one-tenth of the switching frequency, and gain should decrease by 20dB/decade. Similar current and voltage loop transfer functions will ensure overall system stability.

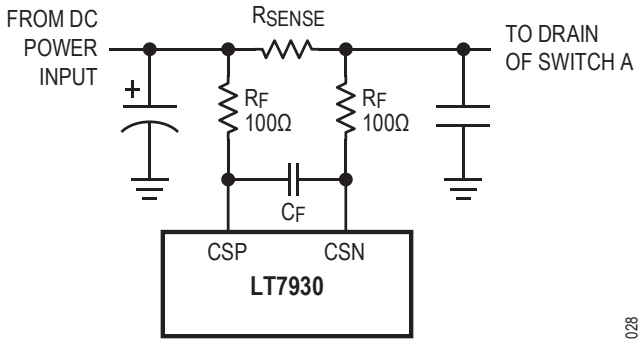


Figure 28. Programming Average Input Current Limit

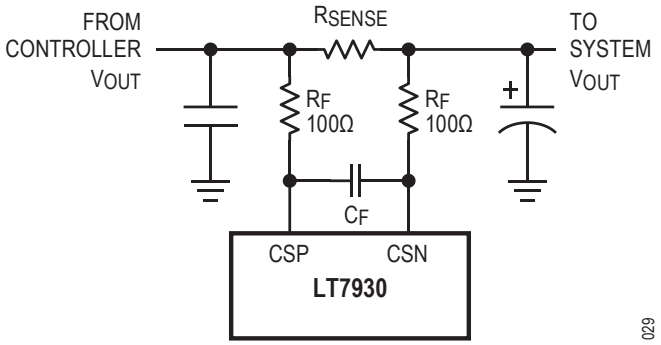


Figure 29. Programming Average Output Current Limit

The input/output current limit is set by the SETCUR pin linearly from 0.2V to 1.2V. The SETCUR pin voltage is internally clamped to 1.2V if the SETCUR pin voltage is higher than 1.2V. The sensed voltage between CSP and CSN is amplified by a factor of 20 internally with a 200mV offset. The resultant voltage is then compared with the voltage on the SETCUR pin. When the sensed voltage is higher than the SETCUR voltage, the ITH pin voltage is pulled low to decrease the inductor current and maintain the current loop regulation. Because the SETCUR pin voltage is internally clamped to 1.2V, the maximum sensed voltage between CSP and CSN is limited to (1.2V – 0.2V)/20 = 50mV.

If the input/output average current limit is not desired, the CSP and the CSN pins should be shorted together and tied to SGND, and the SETCUR pin should be tied to $INTV_{CC}$ or left floating.

C_{IN}/C_{OUT} Selection

In the boost region, input current is continuous. In the buck region, input current is discontinuous, and the selection of input capacitor C_{IN} is driven by the need to filter the input square-wave current. Use a low-ESR capacitor that is sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

$$I_{RMS} \approx I_{OUT(MAX)}OUT \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to derate the capacitor.

In the boost region, the discontinuous current shifts from input to output, so C_{OUT} must be capable of reducing the output voltage ripple. The effects of equivalent series resistance (ESR) and bulk capacitance must be considered

when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$RIPPLE_{(BOOST,CAP)} = I_{OUT(MAX)} \times \left(\frac{V_{OUT} - V_{IN(MIN)}}{C_{OUT} \times V_{OUT} \times f_{SW}}\right)$$

where C_{OUT} is the output capacitor and f_{SW} is the switching frequency.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{BOOST,ESR} = I_{OUT(MAX,BOOST)} \text{ x } ESR$$

In buck mode, V_{OUT} ripple is given by:

$$\Delta V_{OUT} \leq \Delta I_L \times \frac{ESR + 1}{8 \times f_{SW} \times C_{OUT}}$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current-handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface-mount packages. Ceramic capacitors have excellent low-ESR characteristics, but can have a high voltage coefficient. Capacitors are now available with low-ESR and high ripple current ratings, such as OS-CON and POSCAP.

Power FET Selection

As shown in *Figure 21*, the LT7930 requires four external GaN FETs or N-channel power MOSFETs: two for the top switches (switches A and D) and two for the bottom switches (switches B and C). Important parameters for the power FETs are the breakdown voltage ($V_{(BR)DSS}$/BV_{DSS}), threshold voltage ($V_{GS(TH)}$), on-resistance ($R_{DS(ON)}$), reverse transfer capacitance (C_{RSS}), and maximum drain current (I_D). For switches A and B on the input side, the breakdown voltage ($V_{(BR)DSS}$/BV_{DSS}) must be higher than the input voltage. For switches C and D on the output side, the breakdown voltage must be higher than the output voltage. The LT7930 FET driver voltage at the DRV_{CC} pin is 5V, which can drive logic-level FETs.

Note: Do not use FETs with a threshold voltage more than 3V ($V_{GS(TH)}$ > 3V).

In order to select the power FETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in the boost region, when it remains on all the time. Its maximum power dissipation at a maximum output current is given by:

$$P_{A,BOOST} = \left(\frac{I_{OUT(MAX)} \times V_{OUT}}{V_{IN}}\right)^2 \times \rho\tau \times R_{DS(ON)}$$

where ρτ is a normalization factor (unity at 25°C), accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C. For a maximum junction temperature of +125°C, using a value of ρτ = 1.5 is reasonable.

Switch B operates in the buck region as the synchronous rectifier. Its power dissipation at a maximum output current is given by:

$$P_{B,BUCK} = I_{OUT(MAX)}{}^2 \times \rho\tau \times R_{DS(ON)} \times \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

Switch C operates in the boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{C,BOOST} = I_{OUT(MAX)}{}^2 \times \rho\tau \times R_{DS(ON)} \times \frac{V_{OUT} - V_{IN}}{V_{IN}{}^2} + k \times I_{OUT(MAX)} \times C_{RSS} \times f \times \frac{V_{OUT}{}^3}{V_{IN}}$$

where C_{RSS} is usually specified by the FET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in the boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D,BOOST} = \frac{I_{OUT(MAX)} \times V_{OUT}{}^2}{V_{IN}} \times \rho\tau \times R_{DS(ON)} \times \frac{V_{IN}}{V_{OUT}}$$

For the same output voltage and current, switch A has the highest power dissipation and switch B has the lowest power dissipation unless a short occurs at the output. From a known power dissipation in the power FET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \text{ x } R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in the equation normally includes the $R_{TH(JC)}$ for the device thermal resistance from junction to case plus the thermal resistance from the case to the ambient temperature ($R_{TH(CA)}$). This value of T_J can then be compared to the original, assumed value that is used in the iterative calculation process.

Optional Schottky Diode (D_B, D_D) Selection

The optional Schottky diodes D_B (in parallel with switch B) and D_D (in parallel with switch D) conduct during the dead time between the conduction of the power FET switches. They are intended to prevent the body diode of the synchronous switches B and D from turning on and storing charge during dead time when using N-channel power MOSFETs and to prevent the significant loss that occurs due to reverse conduction during dead time when using GaN FETs. These diodes are effective in improving efficiency, especially when operating at higher switching frequencies. In particular, D_B significantly reduces reverse recovery current between switch B turn-off and switch A turn-on, and D_D significantly reduces reverse recovery current between switch D turn-off and switch-C turn-on. They improve converter efficiency and reduce switch voltage stress. In order for the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components are placed adjacently.

Top FET Driver Supply

In the *Block Diagram*, the external bootstrap capacitors C_{BST1} and C_{BST2} connected to the BOOST1 and BOOST2 pins supply the gate drive voltage for the topside FETs. When the top switch A turns on, the switch node SW1 rises to V_{IN} and the BOOST1 pin rises to approximately V_{IN} + DRV_{CC}. When the bottom switch B turns on, the switch node SW1 drops low and the boost capacitor C_{BST1} is charged through diode D_{BST1} from DRV_{CC}. When the top switch D turns on, the switch node SW2 rises to V_{OUT} and the BOOST2 pin rises to approximately V_{OUT} + DRV_{CC}. When the bottom switch C turns on, the switch node SW2 drops to low and the boost capacitor C_{BST2} is charged through diode D_{BST2} from DRV_{CC}.

If the bottom switch B is a GaN FET, which has a large reverse conduction voltage, then a resistor R_{BST1} needs to be added in series with diode D_{BST1}. R_{BST1} limits the C_{BST1} charging current during dead time when SW1 can drop very low and helps maintain the top driver supply voltage around 4.6V. Choosing 1Ω for R_{BST1} is adequate for typical GaN FET applications and a good starting point. Using larger R_{BST1} further limits the C_{BST1} charging current and lowers its voltage. Do not use R_{BST1} > 5Ω, as this may cause insufficient top driver supply voltage. R_{BST2} is picked with the same considerations as R_{BST1}.

The boost capacitors C_{BST1} and C_{BST2} must store about 100 times the gate charge that is required by the top switches A and D. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate. The low-leakage

Schottky diodes D_{BST1} and D_{BST2} must be able to handle the top driver current. Due to the large duty cycle and short on-time of BG1/BG2 when V_{IN} is close to V_{OUT}, the pulse current on D_{BST1} and D_{BST2} could be higher than 100mA. It is suggested that the current capability of D_{BST1} and D_{BST2} is higher than 100mA. The D_{BST1} reverse breakdown voltage must be greater than V_{IN}, and the D_{BST2} reverse breakdown voltage must be greater than V_{OUT}.

DRV_{CC} Regulators and $EXTV_{CC}$

The LT7930 features a P-channel MOSFET LDO that supplies power to DRV_{CC} from the V_{IN} supply. DRV_{CC} powers the gate drivers and most of the LT7930's internal circuitry. The linear regulator regulates the voltage at the DRV_{CC} pin to 5V when the V_{IN} voltage is greater than 5V. $EXTV_{CC}$ connects to DRV_{CC} through another P-channel MOSFET LDO and can also regulate the DRV_{CC} to 5V. The LT7930 internally chooses an efficient LDO between V_{IN} and $EXTV_{CC}$ to reduce IC temperature. Both LDOs can supply the driver current and must be bypassed to ground with a ceramic capacitor or low-ESR tantalum capacitor that has a minimum capacitance of 4.7µF and at least 8 times the sum of C_{BST1} and C_{BST2}. Good bypassing is needed to supply the high transient currents required by the FET gate drivers and the initial C_{BST} charging.

High input voltage applications in which large power FETs are being driven at high frequencies may cause the maximum junction temperature rating for the LT7930 to be exceeded. The DRV_{CC} current, which is dominated by the gate charge current, may be supplied by the linear regulator either from V_{IN} or from $EXTV_{CC}$. Power dissipation for the IC in this case is the highest and is equal to (V_{IN} or $EXTV_{CC}$) x I_{DRVCC}. The gate charge current is dependent on operating frequency, as discussed in the *Efficiency Considerations* section. The junction temperature can be estimated by using the equations given in Note 2 of the *Electrical Characteristics* table. For example, when the LT7930 DRV_{CC} current is 40mA from a 12V~60V V_{IN} supply and there is no $EXTV_{CC}$ supply, the worst-case junction temperature at room temperature can be calculated by:

$$T_J = 25°C + (40mA)(60V)(34°C/W) = 106.6°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode at a maximum V_{IN}. If the output voltage of the above example converter is 24V and it is connected to the $EXTV_{CC}$ pin, when the voltage applied to $EXTV_{CC}$ rises above 4.8V, the DRV_{CC} linear regulator from V_{IN} is turned off and the linear regulator from $EXTV_{CC}$ is turned on. Using $EXTV_{CC}$ allows the FET driver and control power to be derived from the LT7930's switching regulator output during normal operation and from the V_{IN} when the output is out of regulation (e.g., during startup or short circuit). Significant efficiency and thermal gains can be realized by powering $EXTV_{CC}$ from the 24V output, which reduces the junction temperature in the previous example from 106.6°C to 57.6°C:

$$TJ = 25°C + (40mA)(24V)(34°C/W) = 57.6°C$$

Powering $EXTV_{CC}$ from the output can also provide enough gate drive when V_{IN} drops below 5V. This allows a wider operating range for V_{IN} after the controller starts into regulation. If both input and output voltages are high voltages, such as 40V, an external low-voltage (8V~10V) bias supply is suggested to be used on the $EXTV_{CC}$ pin for better efficiency and thermal performance.

Undervoltage Lockout (UVLO)

The LT7930 provides two mechanisms to protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the DRV_{CC} voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when DRV_{CC} is below 3.7V. To prevent oscillation when there is a disturbance on DRV_{CC}, the UVLO comparator has 450mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor-divider from V_{IN} to turn on the IC when V_{IN} is high enough. An extra 4µA of current flows out of the RUN pin once its voltage passes 1.22V. One can program the hysteresis of the run comparator by adjusting the values of the resistor-divider. It is suggested to set the V_{IN} UVLO higher than 5V using the RUN pin for enough gate drive voltage.

In FCM mode, a sufficiently low V_{IN} (step-up ratio > 10) can cause switch C to reach its maximum duty cycle, which may result in a large negative inductor current flowing back to the input. To prevent this, set the V_{IN} UVLO above $\frac{V_{OUT}}{10}$ using the RUN pin to halt switching under this condition.

V_{IN} Overvoltage Protection

To adjust the rising input voltage overvoltage threshold, connect the external resistor voltage divider to the VINOVP pin as shown in *Figure 30*. Use the following equation to adjust the rising input overvoltage threshold.

$$V_{IN_OV} = V_{VINOVP} \times \left(1 + \frac{R3}{R4}\right)$$

Where V_{IN_OV} is the input supply voltage at which the controller enters the V_{IN} overvoltage condition and V_{VINOVP} is the VINOVP pin rising threshold (1.53V, typ).

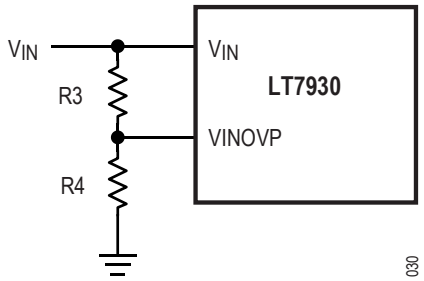


Figure 30. Adjustable Input Overvoltage Threshold

Soft Start-Up Function

When a capacitor is connected to the SS pin, a soft-start current of 2.5µA starts to charge the capacitor. A soft-start function is achieved by controlling the output ramp voltage according to the ramp rate on the SS pin. Current foldback is disabled during this phase to ensure smooth soft-start. When the chip is in the shutdown state with its RUN pin voltage below 1.22V, the SS pin is actively pulled to ground. The soft-start range is defined to be the voltage range from 0V to 1.0V on the SS pin. The total soft-start time can be calculated as:

$$t_{SOFT-START} = 1.0 \times \frac{C_{SS}}{2.5\mu A}$$

Regardless of the mode selected by the MODE/ILIM pin, the regulator always starts in pulse-skipping mode up to SS = 1.0V.

Fault Conditions: Current Limit and Current Foldback

The maximum inductor current is inherently limited in a current-mode controller by the maximum sense voltage. With 100mV current-limit setup (MODE/ILIM tied to ground and ISNSD shorted to ISNSP), the maximum sense voltage and inductor DCR determine the maximum allowed inductor peak current, which is:

$$I_{L(PEAK)} = \frac{100mV}{DCR}$$

To further limit current in the event of a short circuit to ground, the LT7930 includes foldback current limiting. If the output falls by more than 40%, then the maximum sense voltage is progressively lowered to about one-fifth of its full value.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuit produce losses, four main sources account for most of the losses in the LT7930 circuits.

- DC I^2R Losses. These arise from the resistances of the FETs, sensing resistor, inductor, and PC board traces and cause efficiency to drop at high output currents.
- FET Transition Loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends on the input voltage, load current, driver strength, and FET capacitance, among other factors.
- DRV_{CC} Current. This is the sum of the FET driver and control currents. This loss can be reduced by supplying DRV_{CC} current through the $EXTV_{CC}$ pin from a high-efficiency source, such as the output (if $5V < V_{OUT} \leq 20V$) or alternate low voltage supply if available.
- C_{IN} and C_{OUT} Loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck mode. The output capacitor has the more difficult job of filtering the large RMS output current in boost mode. Both C_{IN} and C_{OUT} are required to have low ESR to minimize AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.
- Other Losses. Optional Schottky diodes paralleled across switches B and D are responsible for conduction losses during dead time. Inductor core loss should also be considered. Switch C causes reverse recovery current loss in boost mode.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If one makes a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

Parallel Operations

For output loads that demand high current, multiple LT7930s can be paralleled and daisy-chained to run out of phase to provide more output current without increasing input and output voltage ripple. The SYNC pin allows the LT7930 to synchronize to the CLKOUT signal of another LT7930. The CLKOUT signal can be connected to the SYNC pin of the following LT7930 stage to line up both the frequency and the phase of the entire system. Tying the PHASMD pin to GND, floating, or $INTV_{CC}$ generates a phase difference (between SW1 and CLKOUT) of 180°, 120°, or 90° respectively for 2, 3, or 4 IC's operating in parallel.

Similar to other peak current-mode controllers, the LT7930 may be paralleled with natural cycle-by-cycle current sharing and no extra current sharing loop or stability issues. When designing parallel operations with multiple ICs, always start from the single LT7930 design and check the output current capability and load current transient stability. Then the LT7930 devices can be paralleled by making these connections.

- Tie all of the V_{FB} pins together.
- Tie all of the ITH pins together.
- Tie the inputs of all converters together.

- Tie the outputs of all converters together.
- Route one IC's CLKOUT to another IC's SYNC pin.

See the *Typical Applications* section for an example of a 2-phase parallel operation design.

The LT7930 may also be paralleled from different input voltages for a redundancy design. Just do not tie the SS and RUN pins of the LT7930s together, and each LT7930 can start up with different input voltages to supply current to a single output. Any one input voltage failure will not affect the output voltage regulation as long as the other input sources can supply enough load current. The peak inductor currents are still shared among all of the buck-boost converters by tying all of the ITH pins together. In the redundancy design, it is suggested that each LT7930 has its own compensation network and feedback resistor locally close to the pin, and then short the V_{FB} and ITH pins all together with PCB traces.

Design Example

As a design example for a buck-boost converter, assume $V_{IN(NOMINAL)}$ = 36V ~ 65V, V_{OUT} = 48V, I_{OUT} = 42A, and f_{SW} = 150kHz with a maximum ambient temperature = 60°C.

1. Set the frequency by referring to the FREQ pin resistor vs. frequency curve (see *Figure 22*); a 54.9kΩ resistor to GND will set the switching frequency to 150kHz.

2. Determine the inductor value. For an operating maximum input voltage of 65V, set the inductor ripple current to 30% of the DC current (12.6A) at this input voltage. This leads to an inductor value of:

$$L = \left(V_{IN(MAX)} - V_{OUT}\right) \times \frac{DT_S}{i_L} = (65V - 48V) \times 0.74 \times \frac{6.66\mu s}{12.6A} = 6.6\mu H$$

   The peak inductor current at $65V_{IN}$ is 48A.

   To achieve high efficiency, low-DCR inductors are preferred. This example uses a Wurth 7443640680 inductor (6.8µH/2.64mΩ) with a 55A-rated current. With an RC filter and the usage of an external R_{SENSE} of 2mΩ, we can set the peak sensed inductor current limit to 100mV. Then the peak inductor current is 100mV/2mΩ = 50A, which is less than the saturation current of the selected inductor.

   Next, the inductor current at a minimum input voltage should be examined. At V_{IN} = 36V and V_{OUT} = 48V, the converter is working as a boost converter. At V_{IN} = 36V, the maximum load that the converter can supply before hitting the peak inductor current limit is 31A. The peak inductor current with a 31A load current is 47A.

3. Set the output voltage. Select feedback resistors R1 and R2. If R2 is 10kΩ, R1 is:

$$R1 = \frac{V_{OUT} \times R2}{1.0} - R2$$

   Select R1 as 475kΩ. Both R1 and R2 should have a tolerance of no more than 1%.

4. Select FETs based on the maximum input and output voltages. Switches A and B connected to SW1 operate under the 65V (max) input voltage, so 100V-rated GaN FETs are selected. Switches C and D connected to SW2 operate under the 48V output voltage. The same 100V GaN FETs are selected for switches C and D as well. Similar to a buck or boost converter design, the low $R_{DS(ON)}$ FETs are preferred for low conduction losses. However, the switching loss may be high for low $R_{DS(ON)}$ FETs due to the large gate capacitance. The LT7930 can drive both GaN FETs and N-channel MOSFETs for users to select from a wide variety of power switches. In the design example, the EPC2361 GaN FETs are used. Bootstrap diodes should be able to handle the

maximum V_{IN}/V_{OUT} voltage with a higher than 100mA capability. BAT46WJ,115 Schottky diodes are selected for the TG1/TG2 drivers.

5. Set the dead time by referring to the Dead Time vs. DT Pin Resistor curve (see *Figure 23*); a 27.4kΩ resistor to GND will set the dead time to 10ns.

The RUN pin is used to set the input voltage UVLO. A 301kΩ/10.7kΩ resistor divider from V_{IN} to the RUN pin turns on the converter when V_{IN} is higher than 34V.

PC Board Layout Guidelines

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components. Refer to the evaluation kits, demo board layout, and demo manual for detailed examples.

- The ground plane layer should not have any traces and should be as close as possible to the layer with power FETs.
- Place C_{IN}, switch A, switch B in one compact area. Place C_{OUT}, switch C, and switch D in one compact area.
- Use immediate vias to connect the components (including the LT7930's SGND and PGND pins) to the ground plane. Use several large vias for each power component.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper reduces the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or GND).
- Segregate the signal and power grounds. All small signal components should return to the SGND pin, which is then tied to the PGND pin at one point.
- Place switch B and switch C as close to the controller as possible, keeping the PGND, BG, and SW traces short.
- Keep the high dv/dt SW1, SW2, BOOST1, BOOST2, TG1, and TG2 nodes away from sensitive small-signal nodes.
- The path formed by switch A, switch B, and the C_{IN} capacitor should have short leads and PCB trace lengths. The path formed by switch C, switch D, and the C_{OUT} capacitor also should have short leads and PCB trace lengths.
- The output capacitor (–) terminals should be connected as closely as possible to the (–) terminals of the input capacitor.
- Connect the top driver boost capacitor C_{BST1} closely to the BOOST1 and SW1 pins. Connect the top driver boost capacitor C_{BST2} closely to the BOOST2 and SW2 pins.
- Connect the C_{IN} input capacitors and C_{OUT} output capacitors closely to the power FETs. These capacitors carry the FET AC current in the boost and buck region.
- Connect the V_{FB} pin resistive dividers to the (+) terminals of C_{OUT} and signal ground. A small V_{FB} bypass capacitor may be connected closely to the LT7930 SGND pin. The R2 connection should not be along high current or noise paths, such as input capacitors.
- Route ISNSP and ISNSN leads together with minimum PCB trace spacing. ISNSP must be electrically connected to SW1 without any resistance. The filter capacitor between ISNSP and ISNSN should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the inductor/R_{SENSE}. If ISNSD is used, the filter capacitor on the ISNSD should also be placed close to the IC.

- Connect the ITH pin compensation network closely to the IC, between ITH and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the DRV_{CC} bypass capacitor closely to the IC, between the DRV_{CC} and the PGND pin. This capacitor carries the FET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the DRV_{CC} and PGND pins can help improve noise performance substantially.
- Minimize the trace capacitance from the CLKOUT pin to the SYNC pin for parallel operations. This is to ensure the clock signal edge is sharp and the phase relationship between the parallel controllers is accurate.

TYPICAL APPLICATIONS

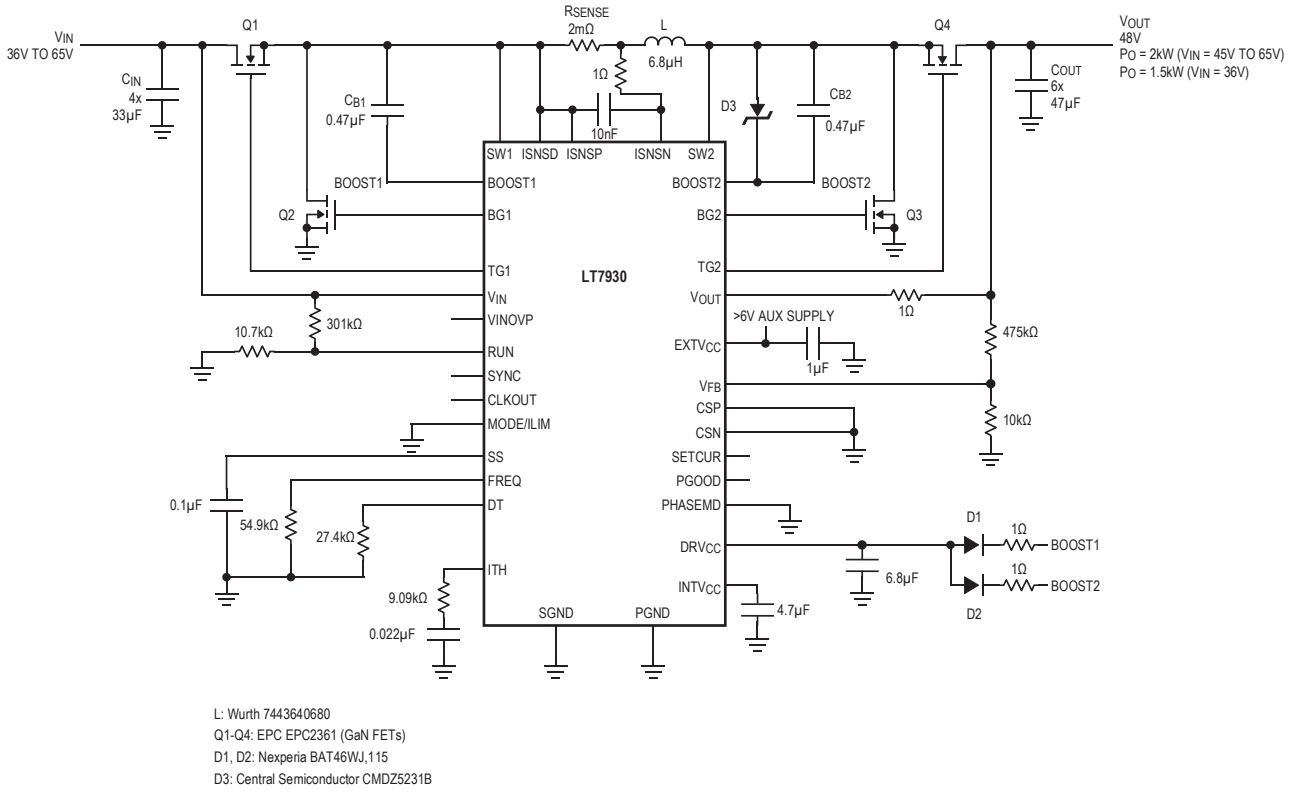


Figure 31. High-Efficiency, 150kHz, 36V to 65V Input, 48V$_{OUT}$ Output Buck-Boost Converter

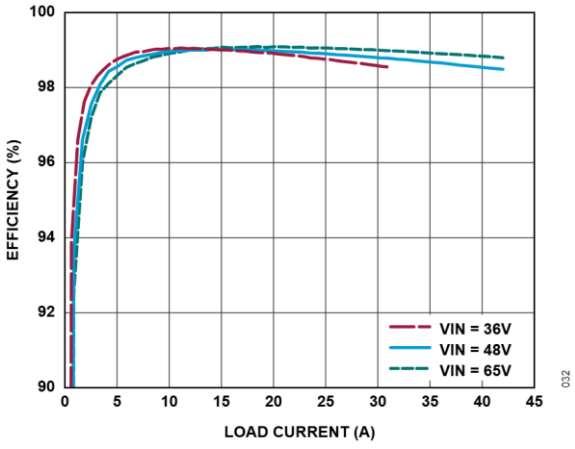


Figure 32. Efficiency vs. Load Current (150kHz)

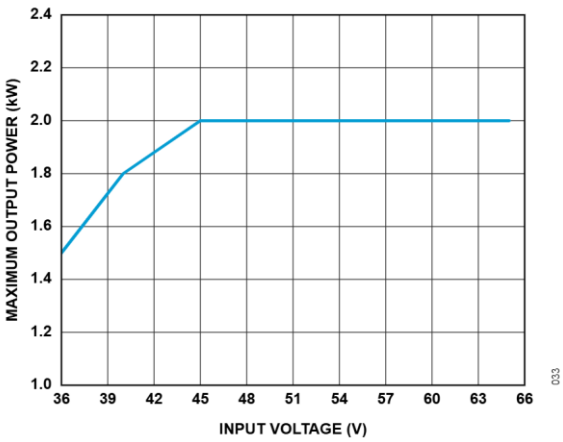
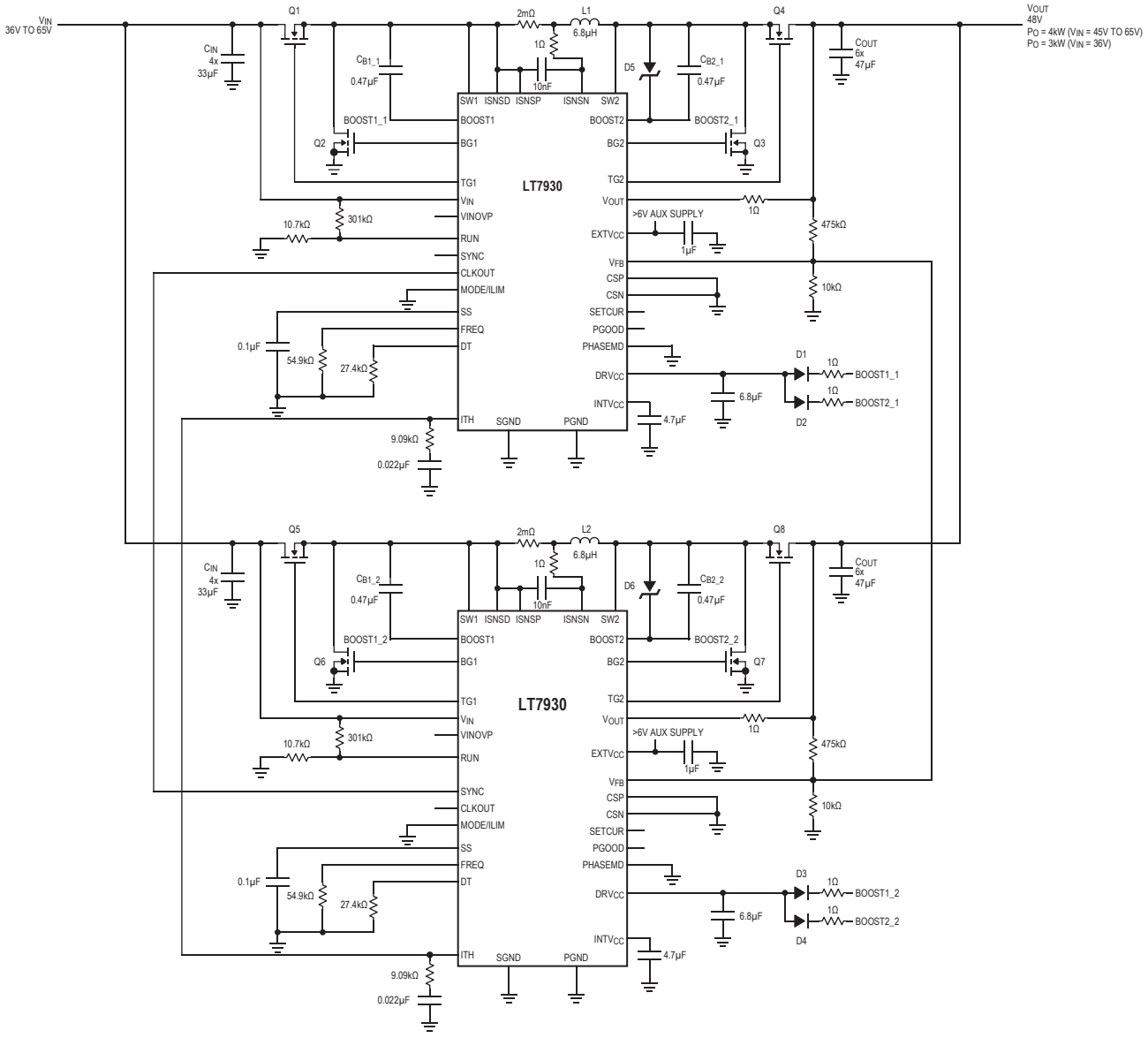
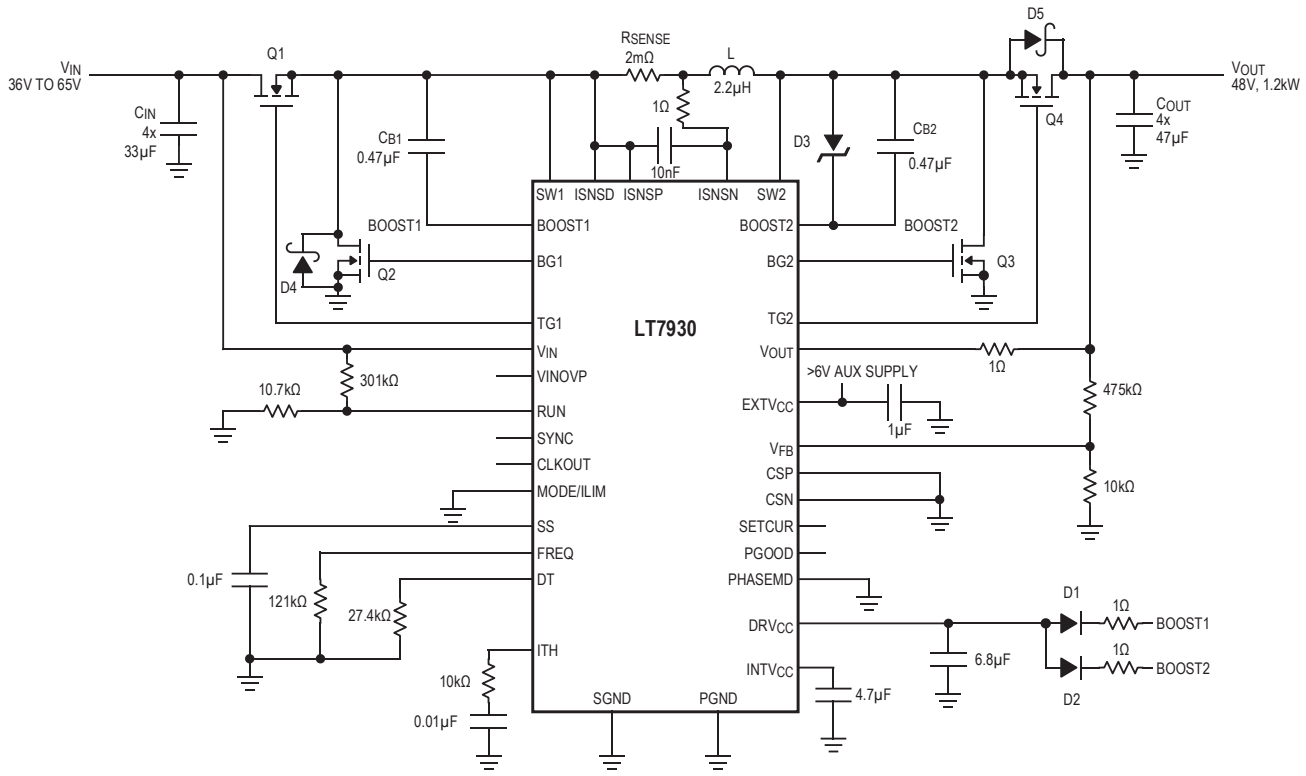


Figure 33. Maximum Output Power vs. Input Voltage



L1, L2: Wurth 7443640680
Q1-Q8: EPC EPC2361 (GaN FETs)
D1-D4: Nexperia BAT46WJ,115
D5, D6: Central Semiconductor CMDZ5231B

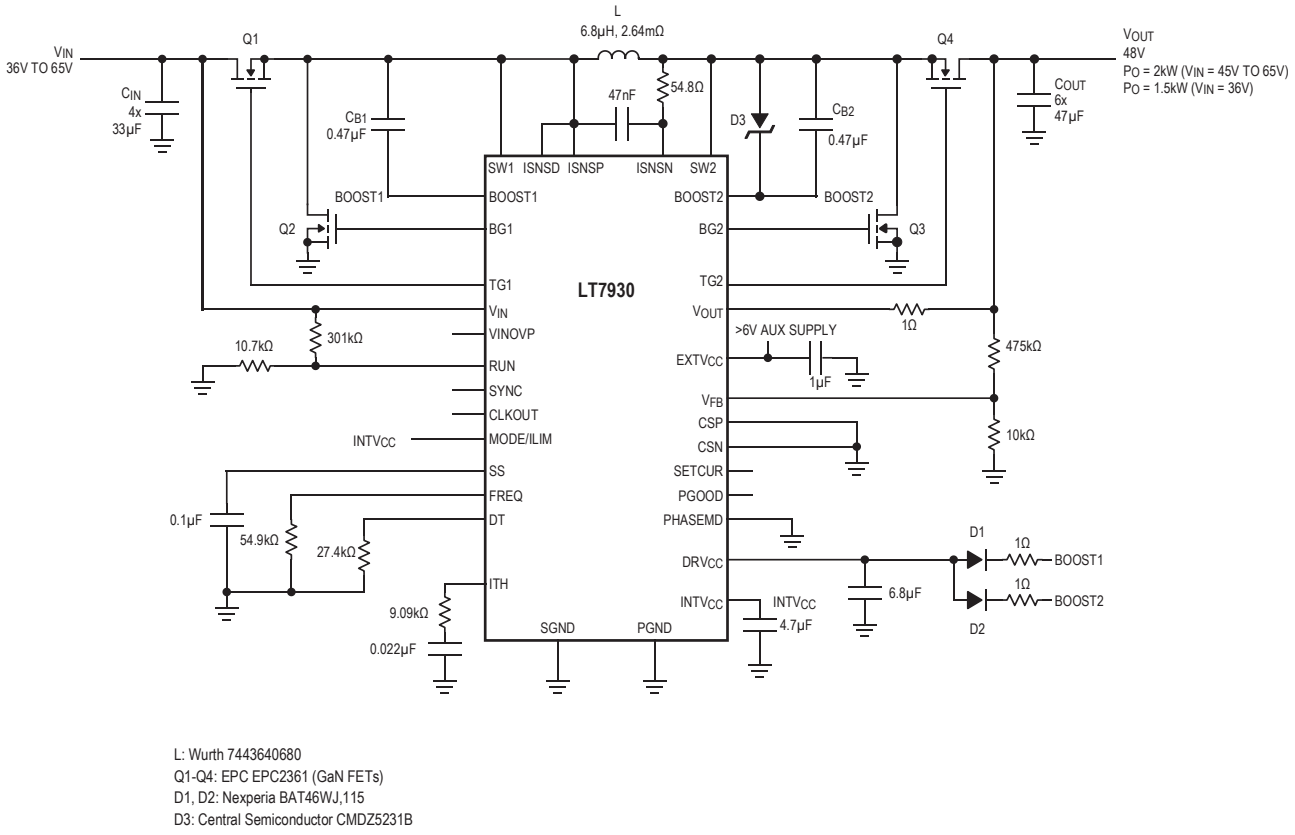
Figure 34. 2-Phase Operation, 150kHz, 48V_{OUT} Buck-Boost Converter



OPTIONAL SCHOTTKY DIODES ACROSS THE SYNCHRONOUS FETS (Q2, Q4) TO ACHIEVE HIGHER OUTPUT POWER WITH REDUCED DEAD TIME LOSS

L: Wurth 7443630220 OR Coilcraft XKL1510-182 (1.8µH)
Q1-Q4: EPC EPC2361 (GaN FETs)
D1, D2: Nexperia BAT46WJ,115
D3: Central Semiconductor CMDZ5231B
D4, D5: Nexperia PMEG100T030ELPEZ

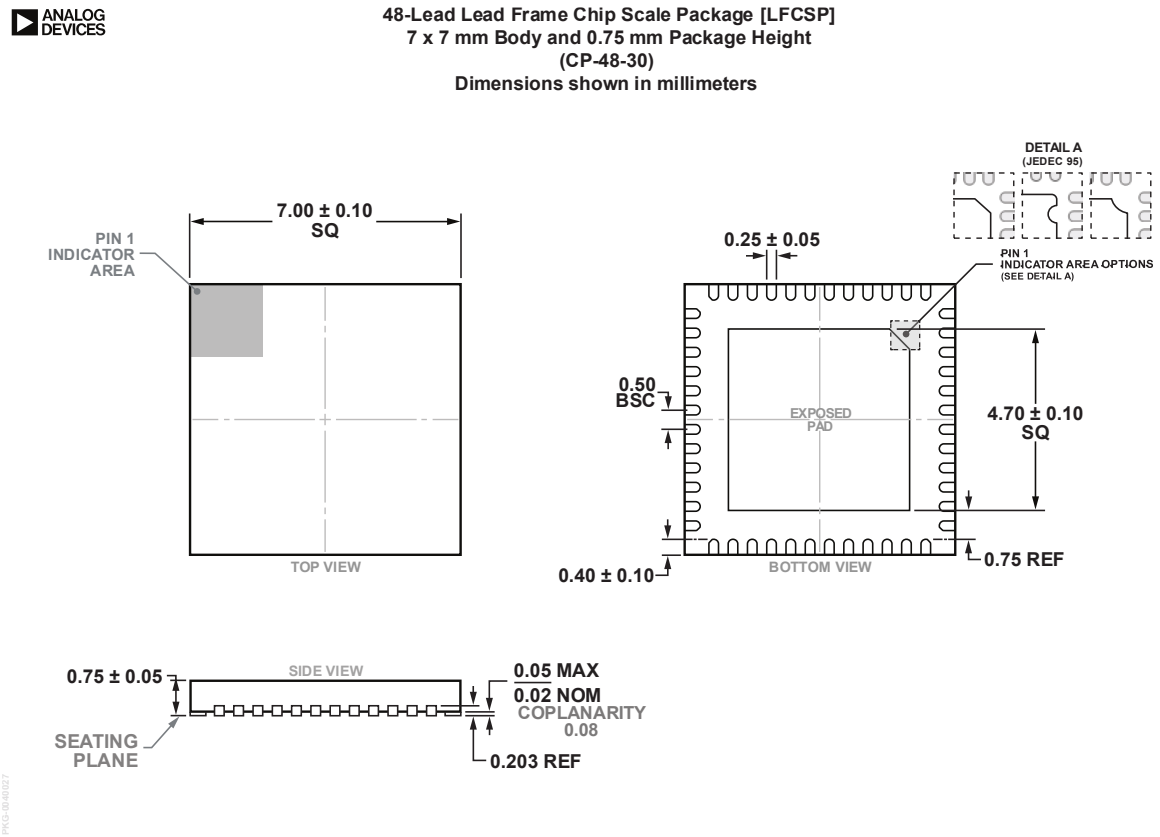
Figure 35. High-Efficiency, 500kHz, 36V to 65V Input, 48V_{OUT}/1.2kW Output Buck-Boost Converter



L: Wurth 7443640680
Q1-Q4: EPC EPC2361 (GaN FETs)
D1, D2: Nexperia BAT46WJ,115
D3: Central Semiconductor CMDZ5231B

Figure 36. High-Efficiency, 150kHz, 36V to 65V Input, 48V_{OUT} Output Buck-Boost Converter with Inductor DCR Current Sensing

PACKAGE DESCRIPTION



RECOMMENDED SOLDER PAD LAYOUT
(TOP VIEW)

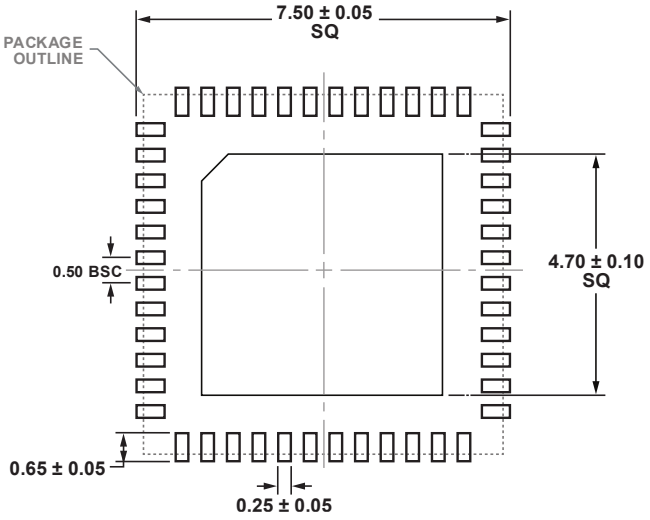


Figure 37. Package Drawing

ORDERING GUIDE

Table 6. Ordering Guide

LEAD-FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT7930AUK#PBF	LT7930AUK#TRPBF	LT7930	48-lead (7mm × 7mm) plastic LFCSP	–40°C to +125°C

Contact the factory for parts specified with wider operating temperature ranges.
**The temperature grade is identified by a label on the shipping container.*
Tape-and-reel specifications. Some packages are available in 500 unit reels through designated sales channels with a #TRMPBF suffix.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7878	70V Parallelable 4-Switch Buck-Boost Controller with Inductor DCR Current Sensing	5V ≤ V_{IN} ≤ 70V, 1V ≤ V_{OUT} ≤ 70V, up to 98% efficiency, peak current-mode control, drives logic level or STD threshold MOSFETs, 5mm × 5mm 32-lead QFN and 7mm × 7mm 48-lead LFCSP
LTC3789	High Efficiency, Synchronous, 4-Switch Buck-Boost Controller	4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 38V, up to 98% efficiency, current-mode control
LTC3779	150V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost Controller	4.5V ≤ V_{IN} ≤ 150V, 1.2V ≤ V_{OUT} ≤ 150V, up to 99% efficiency, drives logic level or STD threshold MOSFETs, 38-lead TSSOP
LTC3777	150V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost Controller plus Switching Bias Supply	4.5V ≤ V_{IN} ≤ 150V, 1.2V ≤ V_{OUT} ≤ 150V, up to 99% efficiency, drives logic level or STD threshold MOSFETs, 38-lead TSSOP
LT8705A	80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller	2.8V ≤ V_{IN} ≤ 80V, input and output current monitor, 5mm × 7mm 38-lead QFN and 38-lead TSSOP
LT8708	80V Bidirectional Synchronous 4-Switch Buck-Boost DC/DC Controller with Bidirectional Capability	2.8V (need EXTVCC > 6.4V) ≤ V_{IN} ≤ 80V, 1.3V ≤ V_{OUT} ≤ 80V, 5mm × 8mm 40-lead QFN
LTM8056	58V_{IN}, 48V_{OUT} Buck-Boost µModule (Power Module) Regulator	5V ≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 48V, adjustable input and output current limiting, 15mm × 15mm × 4.92mm BGA
LT8392	60V Synchronous 4-Switch Buck-Boost Controller with Spread Spectrum	3V ≤ V_{IN} ≤ 60V, 1.2V ≤ V_{OUT} ≤ 60V, I_Q = 2µA, 4mm × 5mm 28-lead QFN and 28-lead TSSOP
LTC7813	Low I_Q, 60V Synchronous Boost plus Buck Controller	4.5V (down to 2.2V after startup) ≤ V_{IN} ≤ 60V, boost V_{OUT} up to 60V, 0.8V ≤ buck V_{OUT} ≤ 60V, I_Q = 29µA, low-EMI and low input/output ripple, 5mm × 5mm 32-lead QFN

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