**TMC2211**

# 65V 2ARMS Smart Pin-Configurable Integrated Stepper Driver

## General Description

The TMC2211 is a high-performance stepper motor driver IC with configuration options through package pins and additional diagnostic outputs. It combines the industry's most advanced stepper motor driver based on the 256 microsteps, built-in indexer and two fully integrated 65V, 3.0AMAX H-bridges, plus non-dissipative integrated current sensing (ICS).

ADI-Trinamic's sophisticated StealthChop2 chopper ensures absolutely noiseless operation combined with maximum efficiency and best motor torque.

High integration, high energy efficiency, and a small form factor enable miniaturized and scalable systems for costeffective solutions. The complete solution reduces the learning curve to a minimum while giving best-in-class performance. The H-bridge field-effect transistors (FETs) have very low impedance, resulting in high driving efficiency and minimal heat generated. The typical total $R_{ON}$ (high side + low side) is 0.31Ω.

The maximum RMS current per H-bridge is 2A with $V_S$ = 24V and 1.7A with $V_S$ = 48V supply at room temperature, assuming a four-layer PCB.

Due to thermal restrictions, the applicable RMS current depends on environment temperature, duty cycle, and the thermal characteristics of the application (PCB ground planes, heatsink, ventilation).

The maximum full-scale current per H-bridge is IFS = 3.0AMAX and can be set by an external resistor connected to $I_{REF}$. This current is defined as the maximum current setting of the embedded current drive regulation circuit.

The maximum output current per H-Bridge is limited by the overcurrent protection (OCP) to a value safely above the peak current setting.

The non-dissipative ICS eliminates the bulky external power resistors, resulting in a dramatic space and power saving compared with mainstream applications based on external sense resistors, while providing the same overall accuracy.

The TMC2211 features extensive diagnostics and protections such as short protection/OCP, thermal shutdown, and undervoltage lockout (UVLO).

During thermal shutdown and UVLO events, the driver is disabled.

The TMC2211 is available in a small TQFN38 5mm x 7mm package with exposed pad.

## Applications

- Textile, Sewing Machines, Knitting Machines
- Lab and Factory Automation
- ID Printers/Card Printers
- Liquid Handling, Medical Applications
- Office Automation and Paper Handling
- POS, Massage Chairs
- ATM, Cash Recycler, Bill Validators, Cash Machines
- CCTV, Security
- Pumps and Valve Control
- Heliostat and Antenna Positioning
- Stage Lighting

## Benefits and Features

- Voltage Range: 4.5V to 65V DC
- Low $R_{ON}$ (HS + LS): 0.31Ω Typical (TA = 25°C)
- Current Ratings per H-Bridge (Typical at 25°C):
  - $2A_{RMS}$ (2.8A Sine Peak) at $V_S$ = 24V
  - $1.7A_{RMS}$ (2.4A Sine Peak) at $V_S$ = 48V
- Fully Integrated Lossless Current Sensing
- Step/Direction (S/D) Interface with MicroPlyer Step Interpolation
- Highest Resolution: 256 Microsteps per Full Step
- StealthChop2 Silent Motor Operation
- SpreadCycle Highly Dynamic Motor Control Chopper
- Full Protection and Diagnostics
- Overvoltage Protection Output
- Compact 5mm x 7mm TQFN38 Package

19-102100; Rev. 0; 01/26

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# TABLE OF CONTENTS

General Description ..... 1
Applications ..... 1
Benefits and Features ..... 1
Package Information ..... 6
Absolute Maximum Ratings ..... 6
Electrical Characteristics ..... 6
Pin Descriptions ..... 9
Pin Configurations ..... 10
Functional Diagrams ..... 11
Detailed Description ..... 12
Principles of Operation ..... 12
Pin-Configurable Step and Direction Driver ..... 12
Key Concepts ..... 13
StealthChop2 and SpreadCycle Driver ..... 13
Benefits ..... 13
Step/Direction Interface ..... 13
Timing ..... 13
MicroPlyer Step Interpolator and Standstill Detection ..... 14
Attention: MicroPlyer only works perfectly with a stable STEP frequency. ..... 15
Pin Configuration Options ..... 15
Attention: First operation with StealthChop2 can only be enabled during standstill to allow for tuning of the integrated current scaling algorithm. ..... 16
StealthChop2 ..... 16
Attention: ..... 16
SpreadCycle ..... 17
Integrated Current Sense ..... 18
Setting the Full-Scale Current Range ..... 18
Diagnostic Outputs ..... 19
Reset, Disable/Stop, and Power Down ..... 21
External Reset and Sleep Mode ..... 21
Protections and Driver Diagnostics ..... 21
Overcurrent Protection ..... 21
Thermal Protection and Shutdown ..... 21
Overvoltage Protection and OV Pin ..... 21
Short Protection (Short-to-GND and Short-to-VS) ..... 22
Undervoltage Lockout Protection ..... 22
Electrostatic Discharge (ESD) Protection ..... 23

Typical Application Circuits ..... 23
Standard Application Circuit ..... 23
High Motor Current TMC2211 ..... 23
Driver Protection and EME Circuitry ..... 24
Ordering Information ..... 25

## LIST OF FIGURES

Figure 1. Simplified Diagram ..... 11
Figure 2. Block Diagram ..... 12
Figure 3. STEP/DIR Signal Timing ..... 14
Figure 4. STEP/DIR Signal Input Filter Structure ..... 14
Figure 5. MicroPlyer Microstep Interpolation with Rising STEP Frequency (Example: 16 to 256) ..... 15
Figure 6. Typical Chopper Decay Phases ..... 17
Figure 7. SpreadCycle Chopper Scheme Showing Coil Current During a Chopper Cycle ..... 17
Figure 8. Diagnostic Outputs Configuration Options ..... 20
Figure 9. Index Signal Pulse at Positive Zero Transition of the Coil B Microstep Wave ..... 20
Figure 10. Brake Chopper Circuit Example ..... 22
Figure 11. Standard Application Circuit ..... 23
Figure 12. Simple ESD Enhancement ..... 24
Figure 13. Extended Motor Output Protection ..... 25

# LIST OF TABLES

Table 1. Microstep Resolution Configuration for the Step Input ..... 15
Table 2. Run Current (IRUN) Configuration ..... 15
Table 3. Digital Current Scale Configuration ..... 16
Table 4. Chopper Mode Selection ..... 16
Table 5. Hold Current (IHOLD) Reduction Configuration ..... 16
Table 6. StealthChop2 PWM Frequency ..... 16
Table 7. SpreadCycle Parameters ..... 17
Table 8. $I_{FS}$ Full-Scale Peak Range Settings (Example for $R_{REF}$ = 12kΩ) ..... 19
Table 9. $I_{FS}$ Full-Scale RMS Current in Ampere ($A_{RMS}$) Based on CFG3/CFG2 Pin Setting and Different $R_{REF}$ ..... 19
Table 10. Overcurrent Protection Thresholds Based on the Full-Scale Current Setting ..... 22

## Package Information

| TQFN38 5mm x 7mm | |
|---|---|
| Package Code | T3857+1C |
| Outline Number | 21-0172 |
| Land Pattern Number | 90-0076 |
| Thermal Resistance, Single Layer Board: | |
| Junction to Ambient ($\theta_{JA}$) | 38°C/W |
| Junction to Case ($\theta_{JC}$) | 1°C/W |
| Thermal Resistance, Four Layer Board: | |
| Junction to Ambient ($\theta_{JA}$) | 28°C/W |
| Junction to Case ($\theta_{JC}$) | 1°C/W |

For the latest package outline information and land patterns (footprints), go to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html.

## Absolute Maximum Ratings

$V_S$ to GND ..... -0.3V to 70V

$V_{DD1V8}$ to GND ..... -0.3V to Min. (2.2, $V_S$ + 0.3)V

AGND to GND ..... -0.3V to +0.3V

OUT1A, OUT2A, OUT1B, OUT2B ..... -0.3V to $V_S$ + 0.3V

$V_{CP}$ to GND ..... $V_S$ - 0.3V to Min. (74, $V_S$ + 6)V

CPO to GND ..... $V_S$ - 0.3V to $V_{CP}$ + 0.3V

CPI to GND ..... -0.3V to $V_S$ + 0.3V

SLEEPN to GND ..... -0.3V to $V_S$ + 0.3V

$I_{REF}$, AIN to GND ..... -0.3V to Min. (2.2, $V_{DD1V8}$ + 0.3)V

$V_{CC_IO}$ to GND ..... -0.3V to 6V

Logic Input/Output Voltage to GND ..... -0.3V to $V_{CC_IO}$ + 0.3V

OV to GND ..... -0.3V to 6V

Operating Temperature Range ..... -40°C to 125°C

Junction Temperature ..... +165°C

Storage Temperature Range ..... -65°C to +150°C

Soldering Temperature (Reflow) ..... +260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Electrical Characteristics

($V_S$ = 4.5V to 65V, $V_{CC_IO}$ = 2.2V to 5.5V = $R_{REF}$ from 12kΩ to 24kΩ. Typical values assume $T_A$ = 25ºC and $V_S$ = 48V. Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Supply Voltage Range | $V_S$ | | 4.5 | | 65 | V |
| Sleep Mode Current Consumption | IVS | V(SLEEPN) = 0 | | 4 | 25 | µA |
| Quiescent Current Consumption | IVS | V(SLEEPN) = 1, V(DRV_ENN) = 1 | | 3.5 | 6 | mA |
| 1.8V Regulator Output Voltage | VVDD | $V_S$ = 4.5V | | 1.8 | | V |

($V_S$ = 4.5V to 65V, $V_{CC_IO}$ = 2.2V to 5.5V = $R_{REF}$ from 12kΩ to 24kΩ. Typical values assume $T_A$ = 25ºC and $V_S$ = 48V. Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{DD}$ Current Limit | IV18LIM | | 20 | | | mA |
| Charge Pump Voltage | $V_{CP}$ | | | $V_S$ + 2.7 | | V |
| Logic I/O Supply Voltage Range | $V_{CC_IO}$ | | 2.2 | | 5.5 | V |
| Sleep Mode Current Consumption | IVCC_IO | V(SLEEPN) = 0 | | 5 | 10 | µA |
| Quiescent Current Consumption | IVCC_IO | V(SLEEPN) = 1 | | 35 | 60 | µA |
| **LOGIC LEVEL INPUTS-OUTPUTS** | | | | | | |
| Input Voltage Level - High | $V_{IH}$ | | 0.7 × $V_{CC_IO}$ | | | V |
| Input Voltage Level - Low | $V_{IL}$ | | | | 0.3 × $V_{CC_IO}$ | V |
| Input Hysteresis | $V_{HYS}$ | | | 0.15 × $V_{CC_IO}$ | | V |
| Internal Pullup/Pulldown Resistance | $R_{PULL}$ | To GND or to $V_{CC_IO}$ | 60 | 100 | 140 | kΩ |
| Input Leakage | InLeak | Inputs without pullup/pulldown resistance | -1 | | +1 | µA |
| Output Logic-Low Voltage | $V_{OL}$ | $I_{LOAD}$ = 5mA | | | 0.4 | V |
| Push-Pull Output LogicHigh Voltage | $V_{OH}$ | $I_{LOAD}$ = 5mA | $V_{CC_IO}$ – 0.4V | | | |
| Open-Drain Output Logic High Leakage Current | $I_{OH}$ | V(PIN) = 5.5V | -1 | | +1 | µA |
| SLEEPN Voltage Level High | $V_{IHSLEEPN}$ | | 0.9 | | | V |
| SLEEPN Voltage Level Low | $V_{ILSLEEPN}$ | | | | 0.6 | V |
| SLEEPN Pulldown Input Resistance | $R_{PDSLEEPN}$ | | 0.8 | 1.5 | | MΩ |
| **OUTPUT SPECIFICATIONS** | | | | | | |
| Output ON-Resistance Low Side | $R_{ONLS}$ | CFG3/CFG2 = 10 | | 0.15 | 0.3 | Ω |
| | | CFG3/CFG2 = 01 | | 0.21 | 0.4 | |
| Output ON-Resistance Low Side | $R_{ONLS}$ | CFG3/CFG2 = 00 | | 0.37 | 0.75 | Ω |
| Output ON-Resistance High Side | $R_{ONLS}$ | | | 0.16 | 0.3 | Ω |
| Output Leakage | $I_{LEAK}$ | | -10 | | +10 | µA |
| Output Slew Rate | SR | | | 400 | | V/µs |
| **PROTECTION CIRCUITS** | | | | | | |
| Overcurrent Protection Threshold | OCP | CFG3/CFG2 = 10 | 5.0 | | | A |
| | | CFG3/CFG2 = 01 | 3.33 | | | |
| | | CFG3/CFG2 = 00 | 1.67 | | | |
| Overcurrent Protection Blanking Time | TOCP | | 0.9 | 1.5 | 2.3 | µs |
| UVLO Threshold on $V_S$ | UVLO | $V_S$ falling | 3.75 | 3.9 | 4.05 | V |

($V_S$ = 4.5V to 65V, $V_{CC_IO}$ = 2.2V to 5.5V = $R_{REF}$ from 12kΩ to 24kΩ. Typical values assume $T_A$ = 25ºC and $V_S$ = 48V. Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| UVLO Threshold on $V_S$ Hysteris | UVLOHYS | | | 0.12 | | V |
| UVLO Threshold on $V_{CC_IO}$ | UVLO | $V_{CC_IO}$ falling | 0.9 | 1.5 | 1.95 | |
| $V_{CC_IO}$ UVLO Hysteresis | UVLOVCCH | | | 100 | | mV |
| Thermal Protection Threshold Temperature | TSD | | | 165 | | °C |
| Thermal Protection Temperature Hysteresis | | | | 20 | | °C |
| **CURRENT REGULATION** | | | | | | |
| $I_{REF}$ Pin Resistor Range | $R_{REF}$ | | 12 | | 60 | kΩ |
| $I_{REF}$ Output Voltage | $V_{REF}$ | | 0.882 | 0.9 | 0.918 | V |
| Full-Scale Current Constant | KIFS | IFS = 1A | | 11.75 | | A × kΩ |
| | | IFS = 2A | | 24 | | |
| | | IFS = 3A | | 36 | | |
| Regulation Accuracy | DITRIP1 | Output current from 7% to 100% FS, $R_{REF}$ = 12kΩ | -7 | | +7 | % |
| Phase-to-Phase Current Regulation Mismatch | $I_{MATCH}$ | Output currents from 7% to 100% FS, $R_{REF}$ = 12kΩ One Sigma | | 0.7 | | % |
| **FUNCTIONAL TIMINGS** | | | | | | |
| SLEEP Time | $t_{SLEEP}$ | SLEEPN = 0 to OUT_ three state | | | 50 | µs |
| Wake-Up Time from Sleep | $T_{WAKE}$ | SLEEPN = 1 to normal operation | | | 2.5 | ms |
| Enable Time | $T_{EN}$ | Time from DRV_ENN pin falling edge to driver on | | | 1.5 | µs |
| Disable Time | $T_{EN}$ | Time from DRV_ENN pin rising edge to driver off | | | 6 | µs |
| **CLOCK** | | | | | | |
| Internal Clock Frequency | $f_{CLK}$ | | 11.9 | 12.5 | 13.2 | MHz |
| **STEP/DIR TIMINGS** | | | | | | |
| Step Frequency | $f_{STEP}$ | | | | $f_{CLK}/8$ | |
| Fullstep Frequency | $f_{FS}$ | | | | $f_{CLK}/512$ | |
| STEP High Time | $t_{SH}$ | | $t_{CLK}$ + 20 | | | ns |
| STEP Low Time | $t_{SL}$ | | $t_{CLK}$ + 20 | | | ns |
| DIR to STEP Setup Time | $t_{SU}$ | | 20 | | | ns |
| DIR to STEP Hold Time | $T_H$ | | 20 | | | ns |

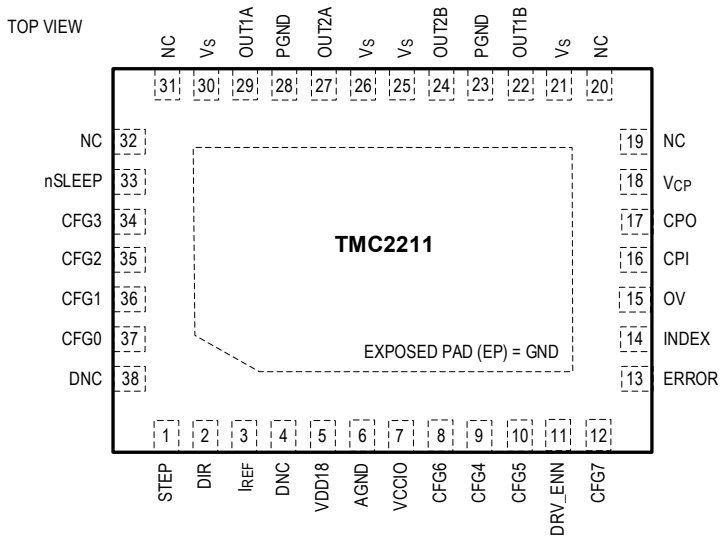
## Pin Descriptions

| PIN | NAME | FUNCTION | REF SUPPLY | Type |
|---|---|---|---|---|
| 6 | AGND | Analog Ground. Connect to ground plane. | | GND |
| 23, 28 | PGND | Power Ground. Connect to ground plane. | | GND |
| 21, 25, 26, 30 | $V_S$ | Motor Supply Voltage. Provide filtering capacity near pin with shortest loop to GND plane/exposed pad. | | Supply |
| 5 | $V_{DD1V8}$ | Output of Internal 1.8V Regulator. Attach 2.2µF or larger ceramic capacitor to AGND near to pin for best performance. | | Supply |
| 18 | $V_{CP}$ | Charge Pump Voltage. Tie to $V_S$ using 1.0µF capacitor. Connect positive end of capacitor close to $V_S$ pin to avoid inductive peaks. | | Analog Output |
| 7 | $V_{CC_IO}$ | Digital IO supply voltage provided from external source to define circuit IO level. Required for proper voltage level settings on output pins. | | Supply |
| 17 | CPO | Charge Pump Capacitor Output | | Analog Output |
| 16 | CPI | Charge Pump Capacitor Input. Tie to CPO using a VS-rated 22nF capacitor. | | Analog Output |
| 1 | STEP | Step input | VCC_IO | Digital Input |
| 2 | DIR | Direction input | VCC_IO | Digital Input |
| 34 | CFG3 | Configuration input, see Table 1 to Table 5 for details on the configuration options | VCC_IO | Digital Input (Pullup) |
| 35 | CFG2 | Configuration input, see Table 1 to Table 5 for details on the configuration options | VCC_IO | Digital Input (Pullup) |
| 36 | CFG1 | Configuration input, see Table 1 to Table 5 for details on the configuration options | VCC_IO | Digital Input (Pullup) |
| 37 | CFG0 | Configuration input, see Table 1 to Table 5 for details on the configuration options | VCC_IO | Digital Output |
| 3 | $I_{REF}$ | Analog Reference Current for Current Scaling. Provide external resistor to GND. | VDD_18 | Analog Input |
| 12 | CFG7 | Configuration input, see Table 1 to Table 5 for details on the configuration options | VCC_IO | Digital Input (Pulldown) |
| 9 | CFG4 | Configuration input, see Table 1 to Table 5 for details on the configuration options | VCC_IO | Digital Input (Pullup) |
| 10 | CFG5 | Configuration input, see Table 1 to Table 5 for details on the configuration options | VCC_IO | Digital Input (Pullup) |
| 8 | CFG6 | Configuration input, see Table 1 to Table 5 for details on the configuration options | VCC_IO | Digital Input (Pullup) |
| 11 | DRV_ENN | Enable Input. The power stage is switched off (all motor outputs floating) when this pin is driven to a high level. | VCC_IO | Digital Input (Pullup) |
| 13 | ERROR | Error output | VCC_IO | Digital Output (open drain) |
| 14 | INDEX | Open drain index pulse output indicating microstep 0 position of coil B. | VCC_IO | Digital Output |

| | | | | |
|---|---|---|---|---|
| | | | | (open drain) |
| 33 | nSLEEP | Low active power down input/reset input.<br>Apply a continuous low level to bring the device to sleep mode.<br>SLEEPN has an internal pulldown.<br>If not used, connect to $V_S$ or $V_{CC_IO}$ (this is a high voltage pin).<br>Once the IC returns from sleep mode/reset, it must be reconfigured before being used again.<br>While reconfiguring the IC, it is advised to still hold the bridge drivers disabled with DRV_ENN.<br>Do not use while at high motor velocity! | VS | Analog Input (Pulldown) |
| 24 | OUT2B | Motor Coil B Output 2 | VS | Analog Output |
| 22 | OUT1B | Motor Coil B Output 1 | VS | Analog Output |
| 27 | OUT2A | Motor Coil A Output 2 | VS | Analog Output |
| 29 | OUT1A | Motor Coil A Output 1 | VS | Analog Output |
| EP | GND | Exposed Die Pad. Connect the exposed die pad to a GND plane. Provide as many as possible vias for heat transfer to the GND plane. Serves as the GND pin for power stage and internal circuitry. | | GND |
| 19, 20, 31, 32 | N.C. | No Internal Connection. Leave this pin open or tie it to GND for improved cooling. | | N.C. |
| 15 | OV | Overvoltage Indicator Output (Open-Drain). Attach external MOSFET with load resistor to limit supply voltage >68.4V. External pullup resistor required.<br>Updated by ADC with $f_{CLK}/2048$. | VCC_IO | Digital Output (Open-Drain) |
| 4, 38 | DNC | Do not connect. This pin must remain unconnected. It may be used internally | | |

## Pin Configurations

**TMC2211 TQFN Pin Configuration**




**TQFN38**
**(5mm x 7mm)**

## Functional Diagrams

TMC2211

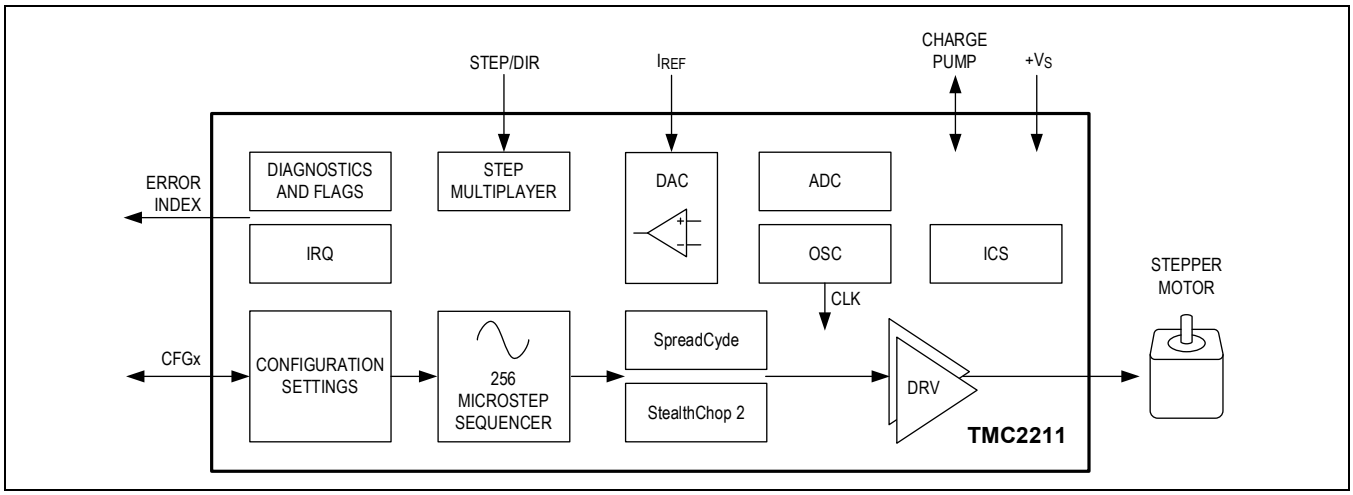



*Figure 1. Simplified Diagram*

# Detailed Description

## Principles of Operation

### Pin-Configurable Step and Direction Driver

The TMC2211 is a step and direction stepper motor driver with pin-configurable settings. Optional feedback signals (ERROR and INDEX) allow error detection and synchronization of motion, if required. The TMC2211 implements advanced features exclusive to ADI-Trinamic products. These features contribute toward greater precision, greater energy efficiency, higher reliability, and quieter and smoother motion.

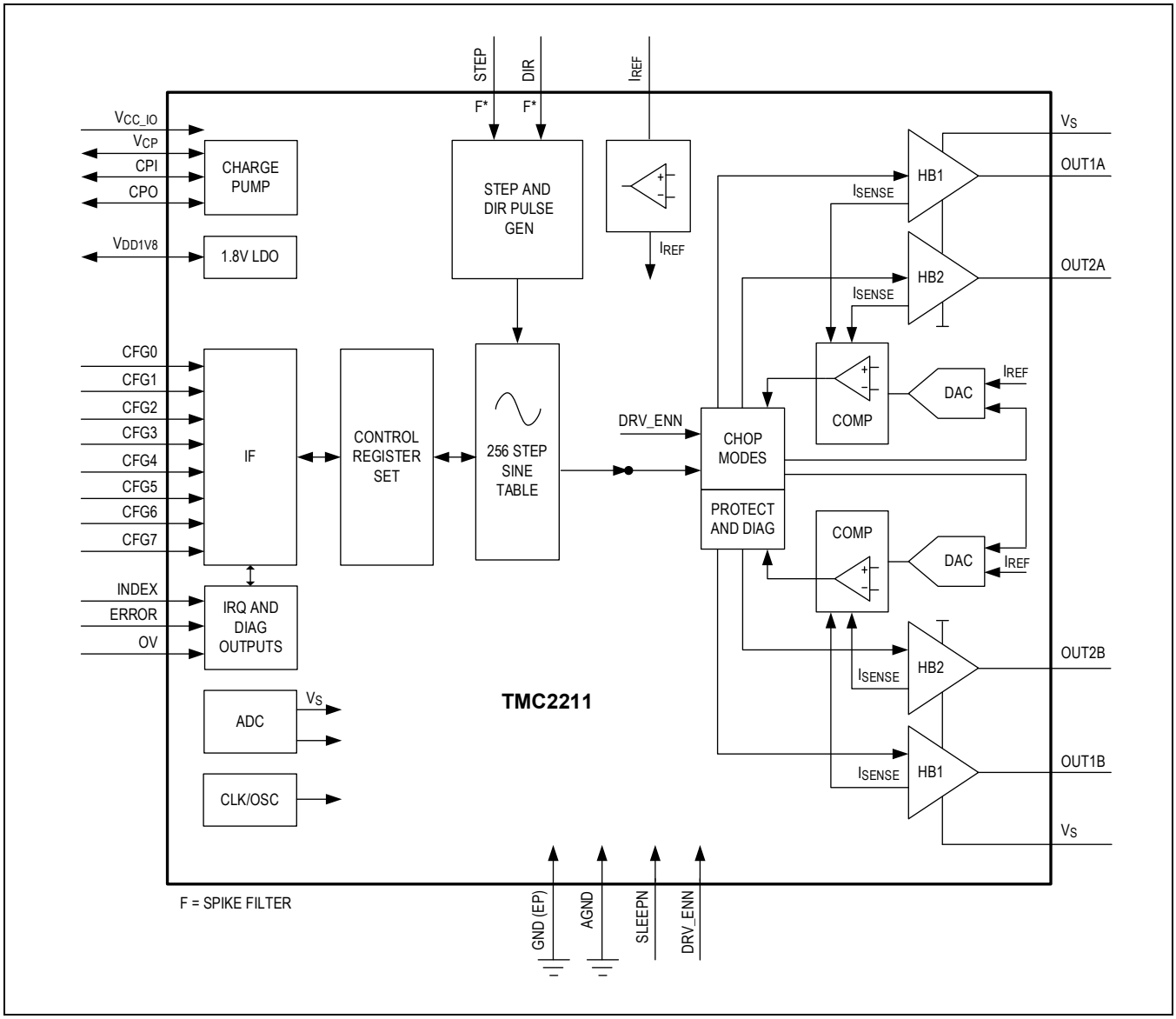



*Figure 2. Block Diagram*

### Key Concepts

The TMC2211 implements advanced features exclusive to ADI-Trinamic products. These features contribute toward greater precision, greater energy efficiency, higher reliability, smoother motion, and cooler operation in many stepper motor applications.

| | |
|---|---|
| StealthChop2 | No-noise, high-precision chopper algorithm for inaudible motion and inaudible standstill of the motor. Allows faster motor acceleration and deceleration than StealthChop and extends StealthChop to low standstill motor currents. |
| SpreadCycle | High-precision cycle-by-cycle current control for highest dynamic movements. |
| MicroPlyer | Microstep interpolator to run at full 256 microstepping with low resolution step input. |

In addition to these performance enhancements, ADI-Trinamic motor drivers offer safeguards to detect and protect against shorted outputs, output open-circuit and undervoltage conditions for enhancing safety and recovery from equipment malfunctions.

### StealthChop2 and SpreadCycle Driver

StealthChop2 is a voltage chopper-based principle. It guarantees the motor is absolutely quiet in standstill and in slow motion, except for the noise generated by ball bearings.

Unlike other voltage mode choppers, StealthChop2 does not require any configuration. It automatically learns the best settings during the first motion after power-up and further optimizes the settings in subsequent motions.

An initial homing sequence is sufficient for learning. StealthChop2 allows high motor dynamics by reacting at once to a change of motor velocity.

For highest velocity applications, SpreadCycle is an alternative option to StealthChop2. StealthChop2 and SpreadCycle may even be used in a combined configuration for the best of both worlds: StealthChop2 for no-noise standstill, silent, and smooth performance, SpreadCycle at higher velocity for high dynamics and highest peak velocity at low vibration.

SpreadCycle is an advanced cycle-by-cycle chopper mode. It offers smooth operation and good resonance dampening over a wide range of speed and load. The SpreadCycle chopper scheme automatically integrates and tunes fast decay cycles to guarantee smooth zero-crossing performance.

### Benefits

- Significantly improved microstepping with low-cost motors.
- Motor runs smooth and quiet.
- Absolutely no standby noise.
- Reduced mechanical resonance improves torque output.

## Step/Direction Interface

The STEP and DIR inputs provide a simple, standard interface compatible with many existing motion controllers. The MicroPlyer step pulse interpolator brings the smooth motor operation of high-resolution microstepping to applications originally designed for coarser stepping.

### Timing

*Figure 3* shows the timing parameters for the STEP and DIR signals. STEP and DIR are sampled and synchronized to the system clock. An internal analog filter of approximately 10ns removes glitches on the signals, such as those caused by long PCB traces. If the signal source is far from the chip, and especially if the signals are carried on cables, the signals should be filtered or transmitted differentially. See the *Electrical Characteristics* table for the specified timing parameters.

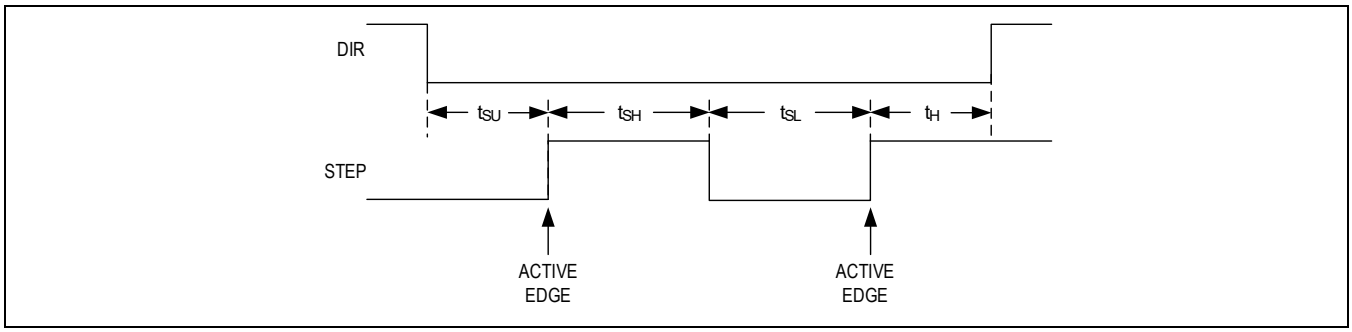



*Figure 3. STEP/DIR Signal Timing*

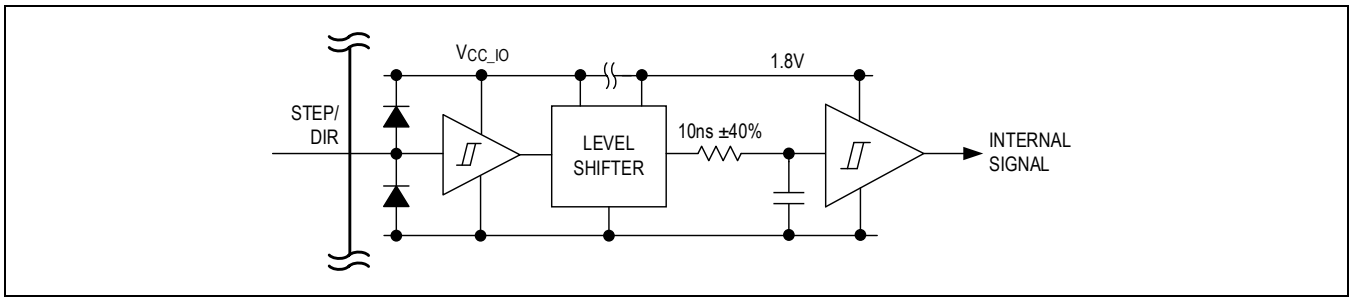



*Figure 4. STEP/DIR Signal Input Filter Structure*

### MicroPlyer Step Interpolator and Standstill Detection

For each active edge on STEP, MicroPlyer produces microsteps at 256x resolution. It interpolates the time in between the two step impulses at the step input based on the last step interval. This way, from four microsteps (64 microsteps to 256 microsteps interpolation) up to 32 microsteps (8 microstep input to 256 microsteps) are driven for a single-step pulse.

MicroPlyer is always enabled. The step rate for the interpolated two microsteps to 256 microsteps is determined by measuring the time interval of the previous step period and dividing it into up to 256 equal parts. The maximum time between two microsteps corresponds to 2^20 (roughly one million system clock cycles) for an even distribution of 256 microsteps. At 12.5MHz system clock frequency, this results in a minimum step input frequency of 12Hz for MicroPlyer operation. A lower step rate causes the detection of a standstill event. At this frequency, microsteps occur at a rate of (system clock frequency)/2^16 ~ 256Hz. When a standstill is detected, the driver automatically switches the motor to holding current IHOLD.

**Attention: MicroPlyer only works perfectly with a stable STEP frequency.**

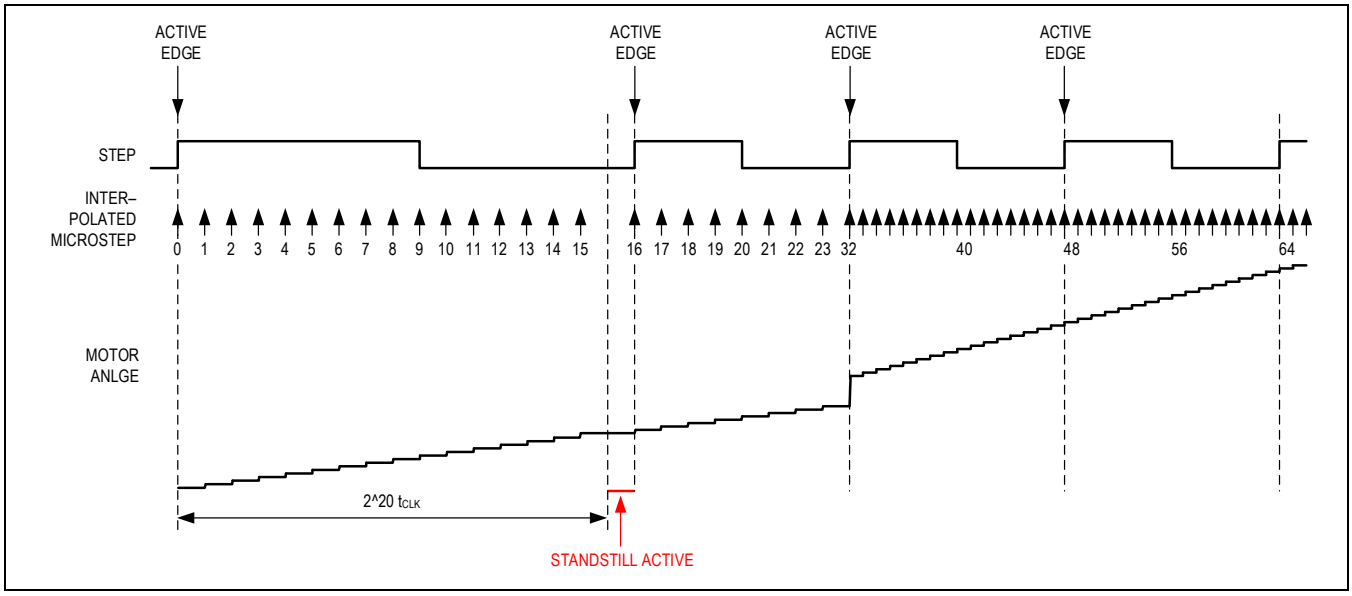



*Figure 5. MicroPlyer Microstep Interpolation with Rising STEP Frequency (Example: 16 to 256)*

The first STEP cycle is long enough to set the standstill bit stst in 0_This bit is cleared on the next STEP active edge. Then, the external STEP frequency increases. After one cycle at the higher rate, MicroPlyer adapts the interpolated microstep rate to the higher frequency. During the last cycle at the slower rate, MicroPlyer does not generate all 16 microsteps. So, there is a small jump in motor angle between the first and second cycles at the higher rate.

## Pin Configuration Options

The following settings can be adjusted using the CFGx pins:

### Table 1. Microstep Resolution Configuration for the Step Input

| CFG0/CFG1: CONFIGURATION OF MICROSTEP RESOLUTION FOR STEP INPUT | | |
|---|---|---|
| **CFG1** | **CFG0** | **MICROSTEP SETTING** |
| GND | GND | 8 microsteps |
| GND | VCC_IO | 16 microsteps |
| VCC_IO | GND | 32 microsteps |
| VCC_IO | VCC_IO | 64 microsteps |

### Table 2. Run Current (IRUN) Configuration

| CFG3/CFG2: CONFIGURATION OF RUN CURRENT IRUN (ALONG WITH $I_{REF}$ RESISTOR), DO NOT CHANGE DURING OPERATION | | |
|---|---|---|
| **CFG3** | **CFG2** | **CURRENT RANGE SETTING** |
| GND | GND | Current scaling = 1A peak |
| GND | VCC_IO | Current scaling = 2A peak |
| VCC_IO | GND | Current scaling = 3A peak |
| VCC_IO | VCC_IO | Not used (3A peak) |

## Table 3. Digital Current Scale Configuration

| CFG4: DIGITAL CURRENT SCALE (MAY BE CHANGED DURING OPERATION) | |
|---|---|
| **CFG4** | **CURRENT SCALE** |
| GND | I = 75% of full scale current IRUN |
| VCC_IO | I = 100% of full scale current IRUN |

## Table 4. Chopper Mode Selection

| CFG5: SELECTION OF CHOPPER MODE | |
|---|---|
| **CFG5** | **CHOPPER MODE** |
| GND | SpreadCycle operation |
| VCC_IO | StealthChop2 operation |

**Attention: First operation with StealthChop2 can only be enabled during standstill to allow for tuning of the integrated current scaling algorithm.**

## Table 5. Hold Current (IHOLD) Reduction Configuration

| CFG7/CFG6: CONFIGURATION OF HOLD CURRENT REDUCTION | | |
|---|---|---|
| **CFG7** | **CFG6** | **HOLD CURRENT REDUCTION** |
| GND | GND | No hold current reduction. IHOLD = IRUN |
| GND | VCC_IO | Reduction to 50%. IHOLD = 1/2 IRUN |
| VCC_IO | GND | Reduction to 25%. IHOLD = 1/4 IRUN |
| VCC_IO | VCC_IO | Reduction to 12.5%. IHOLD = 1/8 IRUN |

## Table 6. StealthChop2 PWM Frequency

| CLOCK FREQUENCY fCLK | PWM FREQUENCY fPWM = 2/1024 fCLK |
|---|---|
| 12.5 MHz (internal) | 24.4 kHz |

### StealthChop2

StealthChop2 is an extremely quiet mode of operation for stepper motors. It is based on a voltage mode PWM. In case of standstill and at low velocities, the motor is absolutely noiseless. Thus, StealthChop2 operated stepper motor applications are very suitable for indoor or home use. The motor operates absolutely free of vibration at low velocities. With StealthChop2, the motor current is applied by driving a certain effective voltage into the coil, using a voltage mode PWM. With the enhanced StealthChop2, the driver automatically adapts to the application for best performance. No more configuration is required.

To match the motor current to a certain level, the effective PWM voltage is scaled depending on the actual motor velocity. Several additional factors influence the required voltage level to drive the motor at the target current: the motor resistance, its back EMF (that is, directly proportional to its velocity), as well as the actual level of the supply voltage. The StealthChop2 PWM frequency depends on the internal clock frequency.

Be sure to allow the motor to rest for at least 100ms before starting a motion using StealthChop2. This allows the current regulation to set the initial motor current. For high-velocity use cases, SpreadCycle should be considered in combination with StealthChop2 by switching between the two modes using the pin CFG5. When switching between both modes, a small jerk might be visible because of a phase shift between voltage and current.

**Attention:** A motor stall, or abrupt stop of the motion during operation in StealthChop2 can trigger an overcurrent condition. Depending on the previous motor velocity, and on the coil resistance of the motor, it significantly increases motor current for 10ms to 100ms. With low velocities, where the back EMF is just a fraction of the supply voltage, there is no danger of triggering the short detection.

### SpreadCycle

While StealthChop2 is a voltage mode PWM-controlled chopper, SpreadCycle is a cycle-by-cycle current control chopper. Therefore, it can react extremely fast to changes in motor velocity or motor load. The currents through both motor coils are controlled using dedicated chopper circuits. The chopper circuits work independently of each other. *Figure 6* shows the different chopper phases. The dedicated sense resistor in *Figure 6* is only used for better explanation. The TMC2211 comes with fully internal current sensing.

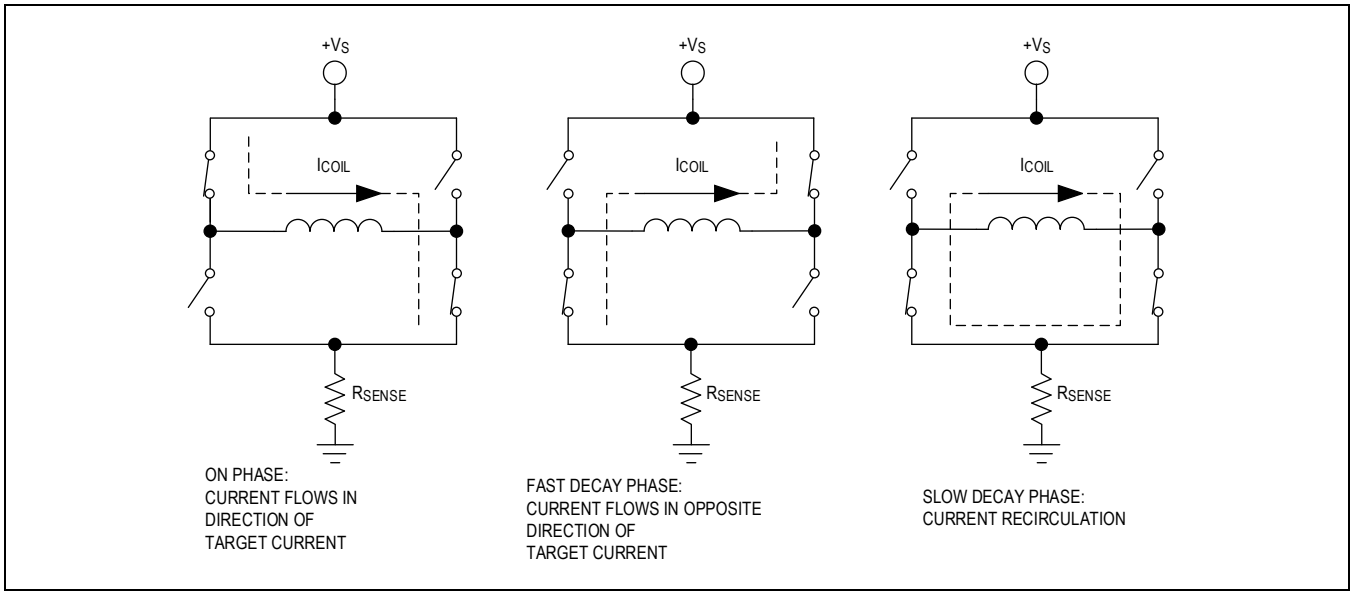



*Figure 6. Typical Chopper Decay Phases*

## Table 7. SpreadCycle Parameters

| PARAMETER | DESCRIPTION | SETTING |
|---|---|---|
| TOFF | The slow decay time (off time) is set to 120 $t_{CLK}$. | 120 $t_{CLK}$ |
| TBL | The comparator blank time safely covers the switching event and duration of the ringing on the RDS(ON) measurement. | 36 $t_{CLK}$ |

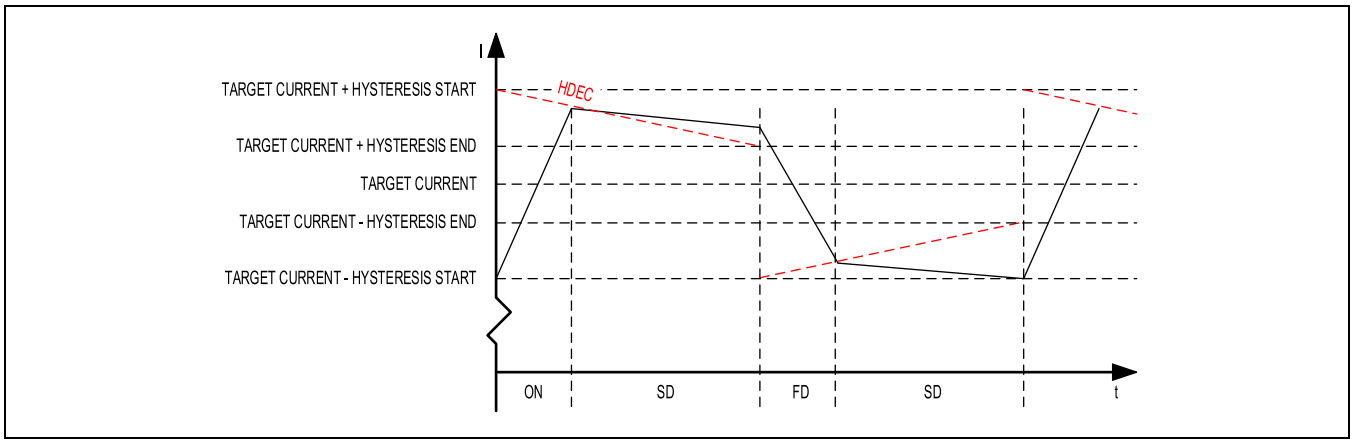



*Figure 7. SpreadCycle Chopper Scheme Showing Coil Current During a Chopper Cycle*

Although the current can be regulated using only on-phases (ON) and fast decay (FD) phase, insertion of the slow decay (SD) phase is important to reduce electrical losses and current ripple in the motor. The current comparator can measure coil current during phases when the current flows through exactly one low-side transistor, but not during the SD phase. So, the SD phase is terminated by a timer.The on-phase is terminated by the comparator when the current through the coil reaches the target current plus some hysteresis. The FD phase may be terminated by either the comparator or another timer.

When the coil current is switched, spikes in the RDS(ON)-based current measurement occur due to charging and discharging parasitic capacitance.

During this time, typically one or two microseconds, the current cannot be measured. Blanking is the time when the input to the comparator is masked to block these spikes.

The high-performance chopper algorithm called SpreadCycle cycles through four phases: on, slow decay, fast decay, and a second slow decay.

## Integrated Current Sense

Non-dissipative current sensing is integrated in the TMC2211 (ICS). This feature eliminates the bulky external power resistors, which are normally required with external current sensing. The ICS results in a dramatic space and power saving compared with mainstream applications based on the external sense resistor. For optimum performance, the ICS individually measures $R_{DS(ON)}$ for each of the power MOSFETs, considering individual MOSFET temperature to yield the best results.

### Setting the Full-Scale Current Range

The full-scale current IFS is a peak current setting. It is selected with an external reference resistor and the two configuration pins CFG2 and CFG3 (see also Table 2 in the **Pin Configuration Options** section).

Three different full-scale current ranges can be configured through the pins with the same reference resistor to adapt to different motor sizes and applications. This is needed to benefit from the best possible current control resolution.

Connect a reference resistor $R_{REF}$ from $I_{REF}$ to GND. Together with pins CFG3 and CFG2, the full-scale current range IFS is set based on the external resistor .

The following equation shows the full-scale current IFS as a function of the $R_{REF}$ shunt resistor connected to pin $I_{REF}$ and the configuration pin setting. The proportionality constant $K_{IFS}$ is defined by the CFG2 and CFG3 setting. The external resistor $R_{REF}$ can range between 12kΩ and 60kΩ.

$$I_{FS}\,(RMS) = \frac{K_{IFS}(CFG2, CFG3)}{RREF[k\Omega]} \times Cs \times \frac{248}{256} / \sqrt{2}$$

While motor running: $Cs = \frac{CFG4 \times 25 + 75}{100}$

While motor standstill: $Cs = \frac{\frac{CFG4 \times 25 + 75}{100}}{2^{(2*CFG7 + CFG6)}}$

This equation gives the RMS motor current per coil.

- CS is IRUN or IHOLD, respectively.
- 248/256 is the amplitude of the default microstep table.
- 1/SQRT(2) is the factor to calculate the RMS value for a sine wave shape.

## Table 8. $I_{FS}$ Full-Scale Peak Range Settings (Example for $R_{REF}$ = 12kΩ)

| CFG3/CFG2 | $K_{IFS}$ (A x kΩ) | MAX. FS SETTING (PEAK) | TYPICAL $R_{DS(ON)}$ (HS + LS) | NOTES |
|---|---|---|---|---|
| 1/1 | 36 | 3A | 0.31Ω | Optimized efficiency and extended operating range up to 3A (FS). |
| 1/0 | 36 | 3A | 0.31Ω | Optimized efficiency and extended operating range up to 3A (FS). |
| 0/1 | 24 | 2A | 0.37Ω | Reduced operating range up to 2AFS.<br>When high accuracy at lower current is required. |
| 0/0 (default) | 11.75 | 1A | 0.53Ω | Reduced operating range up to 1AFS.<br>When high accuracy at low current is required. |

*Table 9* is a matrix of different reference resistor values (at pin $I_{REF}$) versus the different pin configurations for the full-scale current. The resulting maximum RMS current is given in each cell.

## Table 9. $I_{FS}$ Full-Scale RMS Current in Ampere ($A_{RMS}$) Based on CFG3/CFG2 Pin Setting and Different $R_{REF}$

| $R_{REF}$ (kΩ) | MAX. FULL SCALE CURRENT ($A_{RMS}$) BASED ON CFG3/CFG2 PIN SETTING AND $K_{IFS}$ (A × kΩ) | | | |
|---|---|---|---|---|
| | CFG3/CFG2 = 1/1 | CFG3/CFG2 = 1/0 | CFG3/CFG2 = 0/1 | CFG3/CFG2 = 0/0 |
| | $K_{IFS}$ = 36 | $K_{IFS}$ = 36 | $K_{IFS}$ = 24 | $K_{IFS}$ = 11.75 |
| 12 | 2.05 | 2.05 | 1.37 | 0.67 |
| 15 | 1.65 | 1.65 | 1.09 | 0.53 |
| 18 | 1.37 | 1.37 | 0.91 | 0.45 |
| 22 | 1.12 | 1.12 | 0.75 | 0.37 |
| 27 | 0.91 | 0.91 | 0.61 | 0.30 |
| 33 | 0.75 | 0.75 | 0.49 | 0.24 |
| 39 | 0.63 | 0.63 | 0.43 | 0.20 |
| 47 | 0.52 | 0.52 | 0.35 | 0.17 |
| 56 | 0,44 | 0,44 | 0,29 | 0,15 |

### Diagnostic Outputs

Operation with an external motion controller often requires quick reaction to certain states of the stepper motor driver. Therefore, the diagnostic outputs ERROR and INDEX supply a fixed set of real-time information complementing the STEP/DIR interface.

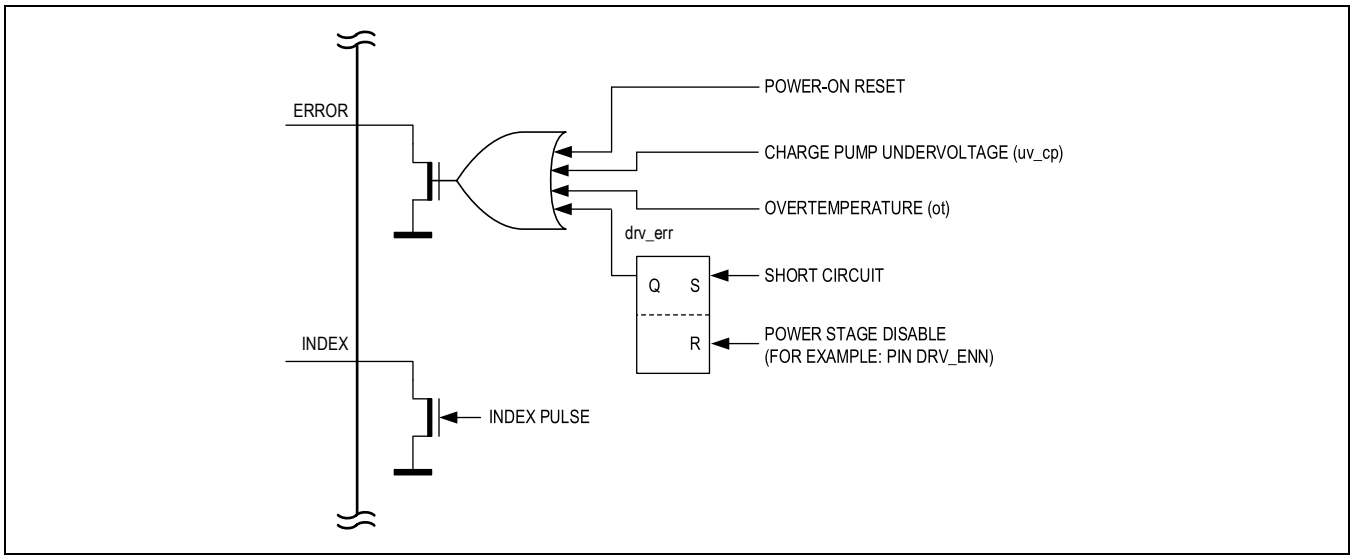



*Figure 8. Diagnostic Outputs Configuration Options*

ERROR shows any driver error that prevents the chip from operating. This is an open-drain output. To determine a reset of the driver, ERROR always shows a power-on reset condition by pulling low during a reset condition. An active INDEX output signals that the cosine curve of motor coil B is at its positive zero transition. The duration of the index pulse corresponds to the duration of the microstep. The index output allows precise detection of the microstep position within one electrical wave, that is, within a range of four fullsteps. With this, homing accuracy and reproducibility can be enhanced to microstep accuracy, even when using an inexpensive home switch. Thereby, the INDEX signal is a low active open-drain output. The active pulse is a low pulse.

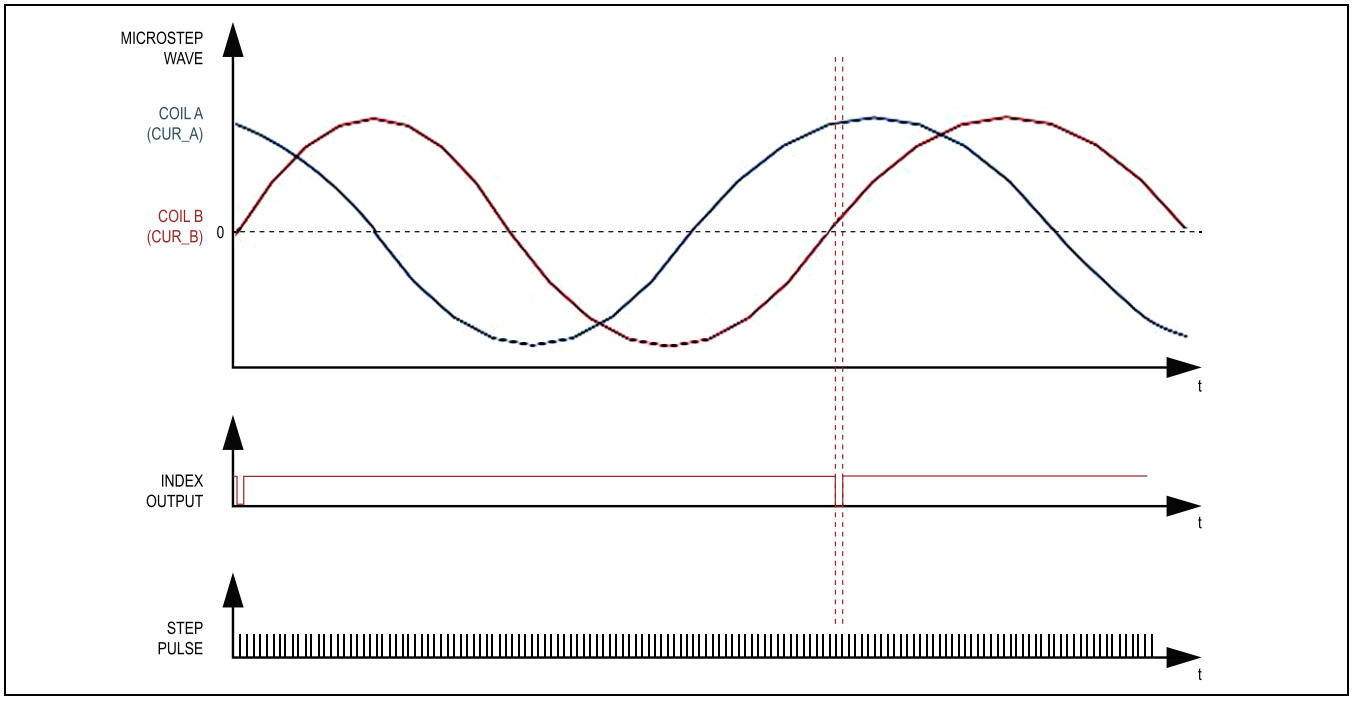



*Figure 9. Index Signal Pulse at Positive Zero Transition of the Coil B Microstep Wave*

## Reset, Disable/Stop, and Power Down

### External Reset and Sleep Mode

The reset and sleep mode are controlled with the SLEEPN pin.

A short pulse on SLEEPN with a duration >30µs results in a chip reset. Very short pulses of <30µs are filtered out and do not have an effect on the operation.

If SLEEPN is kept at GND, the IC goes into low power standby state (sleep mode). All internal supplies and bridge drivers are switched off.

After power-up or leaving sleep mode and reset condition, the configuration pins are read and internal registers set accordingly. Set DRV_ENN low to complete the power up cycle reset.

The wake-up time is given in the EC table.

If not used, connect to $V_S$ or $V_{CC_IO}$ (this is a high voltage pin). Driving the DRV_ENN pin high, the bridge drivers can be disabled and the motor is freewheeling.

Be careful using these pins during high motor velocity as energy fed back from the motor might damage the chip!

## Protections and Driver Diagnostics

### Overcurrent Protection

Overcurrent protection (OCP) protects the device against short circuits to the rails (supply voltage and ground) and between the outputs (OUT1A, OUT2A, OUT1B, OUT, and 2B).

The OCP threshold depends on the selected full-scale current range or see the *Electrical Characteristics* table for the respective threshold values.

The full-scale range is selected with CFG3/CFG2 pins (see Table 9)

If the output current is greater than the OCP threshold for longer than the deglitch time (blanking time), then an OCP event is detected.

When an OCP event is detected, the H-bridge is immediately disabled.

The short protection tries thrice before a fault on the ERROR pin is set and the bridge is continuously disabled.

The device is still alive and allows for configuration using pins.

To re-enable the power bridge, the DRV_ENN pin must be cycled.

### Thermal Protection and Shutdown

The TMC2211 has an internal thermal protection.

If the die temperature exceeds 165°C (typical value), a fault indication as a fault flag is raised and the driver is three-stated until the junction temperature drops below approximately 145°C (typical value). After that, the driver is re-enabled.

Heat is mainly generated by the motor driver stages, and at increased voltage, by the internal voltage regulator. Most critical situations, where the driver MOSFETs can be overheated, are avoided when enabling the short-to-GND protection. For many applications, the overtemperature prewarning indicates an abnormal operation situation and can be used to initiate user warning or power reduction measures like motor current reduction. The thermal shutdown is just an emergency measure and temperature rising to the shutdown level should be prevented by design.

### Overvoltage Protection and OV Pin

A stepper motor application can generate significant overvoltage, especially when the motor is quickly decelerated from a high velocity, or when the motor stalls.

This voltage is fed back to the supply rails by the driver output stage.

For typical NEMA17 or larger motors, and also for smaller motors with sufficient flywheel mass, the energy fed back can be substantial, so that the power capacitors and circuit consumption are not sufficient to keep the supply within its limits.

To protect the driver as well as connected circuitry, the TMC2211 has an overvoltage detection and protection mechanism.

The OV output allows attaching an NPN or MOSFET with a power resistor (brake resistor) to dump the excess energy into the resistor.

The transistor chops with approximately 3kHz to 4kHz (depending on the clock frequency) to keep the supply within the limits.

The supply voltage is permanently monitored with the internal ADC.

The upper level for the supply voltage is set to 68.4V.

The OV output pin shows the actual state of the overvoltage monitor.

As soon as and as long as $V_S$ > 68.4 V, the OV output pin changes to three-state/'Z'.

The OV output pin is an open-drain pin. *Figure 10* shows an example of a brake chopper circuit.

Take special care if the device is put into sleep mode (SLEEPN = LOW). In this case, OV is floating.

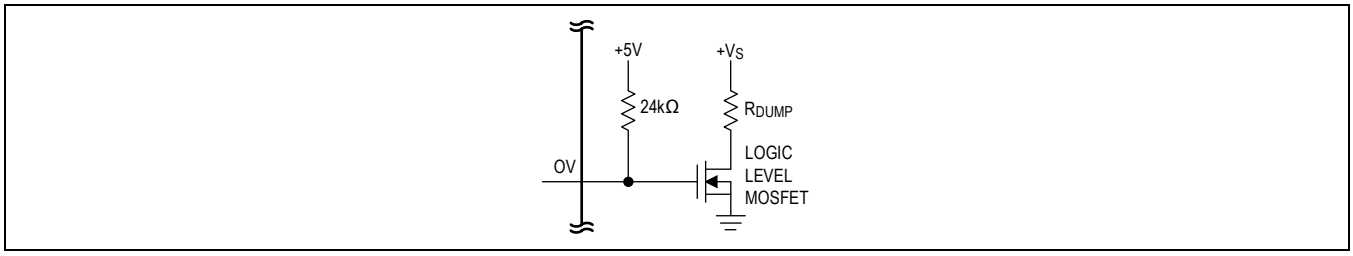



*Figure 10. Brake Chopper Circuit Example*

### Short Protection (Short-to-GND and Short-to-VS)

The TMC2211 power stages are protected against a short-circuit condition by an additional measurement of the current flowing through the high-side MOSFETs. This is important, as most short circuit conditions result from a motor cable insulation defect, for example, when touching the conducting parts connected to the system ground. The short detection is protected against spurious triggering, for example, by electrostatic discharges (ESD), by retrying thrice before switching off the motor.

Once a short condition is safely detected, the corresponding driver bridge is switched off, and the ERROR pin is active (no flags in register map). To restart the motor, intervene by disabling and re-enabling by toggling DRV_ENN. Note that the short-to-GND protection cannot protect the system and the power stages for all possible short events, as a short event is rather undefined and a complex network of external components may be involved. Therefore, short circuits should basically be avoided.

Depending on the full-scale current setting, the low-side short protection triggers at different overcurrent protection thresholds.

## Table 10. Overcurrent Protection Thresholds Based on the Full-Scale Current Setting

| FULL-SCALE CURRENT SETTING (CFG3/CFG2) | OVERCURRENT PROTECTION THRESHOLD [A] |
|---|---|
| 10 (and 11) | 5.0 |
| 01 | 3.33 |
| 00 | 1.67 |

### Undervoltage Lockout Protection

The TMC2211 features an UVLO protection for $V_S$, $V_{CC_IO}$, and the charge pump.

The UVLO condition on $V_S$ is triggered below 4.05V (max).

The UVLO condition on $V_{CC_IO}$ is triggered below 1.95V (max).

The UVLO condition on the charge pump is triggered in case of an error condition of the charge pump, for example, due to a wrong capacitor value.

During a $V_{CC_IO}$ UVLO, no communication with the IC is possible and the driver is disabled. The ERROR pin is active low (open-drain).

### Electrostatic Discharge (ESD) Protection

The chip has internal ESD protection on every pin.

The TMC2211 motor phase output pins are protected up to 8kV HBM in the application when using a bypass capacitor of at least 1µF on the positive voltage supply ($V_S$ pins).

This is not protection against the hot plugging of a motor.

## Typical Application Circuits

### Standard Application Circuit

The standard application circuit uses a minimum set of additional components. Use low ESR electrolytic capacitors to filter the power supply. The capacitors must cope with the current ripple caused by the chopper operation. A minimum capacity of 100µF at $V_S$ is recommended for best performance. The current ripple in the supply capacitors also depends on the power supply internal resistance and cable length. $V_{CC_IO}$ must be supplied from an external source, for example, a low drop 3.3V regulator.

Place all the filter capacitors as close as possible to the related IC pins. Use a solid common ground plane for all GND connections. Connect the $V_{DD1V8}$ filtering capacitor directly to the $V_{DD1V8}$ pin.

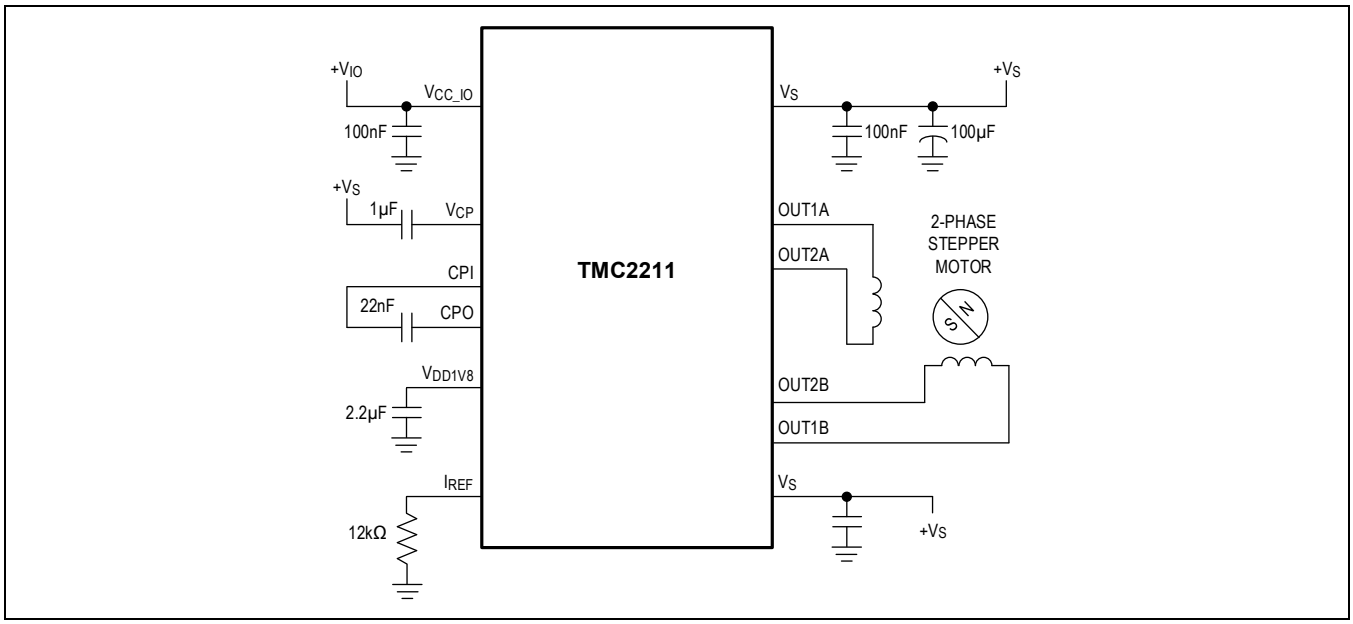



*Figure 11. Standard Application Circuit*

### High Motor Current

When operating at a high motor current, the driver power dissipation due to MOSFET switch-on resistance significantly heats up the driver. This power dissipation heats up the PCB cooling infrastructure also, if operated at an increased duty cycle. This in turn leads to a further increase of driver temperature. An increase of temperature by about 100°C increases MOSFET resistance by roughly 50%. This is a typical behavior of MOSFET switches. Therefore, under high duty cycle and high load conditions, thermal characteristics must be carefully considered, especially when increased environment temperatures are to be supported. See the **Package Information** for the thermal characteristics and online evaluation kit information for the layout example.

As a rule of thumb, thermal properties of the PCB design may become critical at supply voltages above 24V or with a motor current above $1.5A_{RMS}$ for increased periods of time. Note that the resistive power dissipation rises with the square of the motor current. On the other hand, this means that a small reduction of motor current significantly saves heat dissipation and energy.

### Driver Protection and EME Circuitry

Some applications have to cope with ESD events caused by motor operation or external influence. Despite ESD circuitry within the driver chips, ESD events occurring during operation can cause a reset or even a destruction of the motor driver, depending on their energy. Especially, plastic housings and belt drive systems tend to cause ESD events of several kV. It is best practice to avoid ESD events by attaching all conductive parts, especially the motors themselves to PCB ground, or to apply electrically conductive plastic parts. In addition, the driver can be protected up to a certain degree against ESD events or live plugging/pulling the motor, which also causes high voltages and high currents into the motor connector terminals.

A simple scheme uses capacitors at the driver outputs to reduce the dV/dt caused by ESD events. Larger capacitors bring more benefit concerning ESD suppression, but cause additional current flow in each chopper cycle, and thus, increase driver power dissipation, especially at high supply voltages. The values shown are example values (they might be varied between 100pF and 1nF). The capacitors also dampen high-frequency noise injected from the digital parts of the application PCB circuitry, and thus, reduce electromagnetic emission.

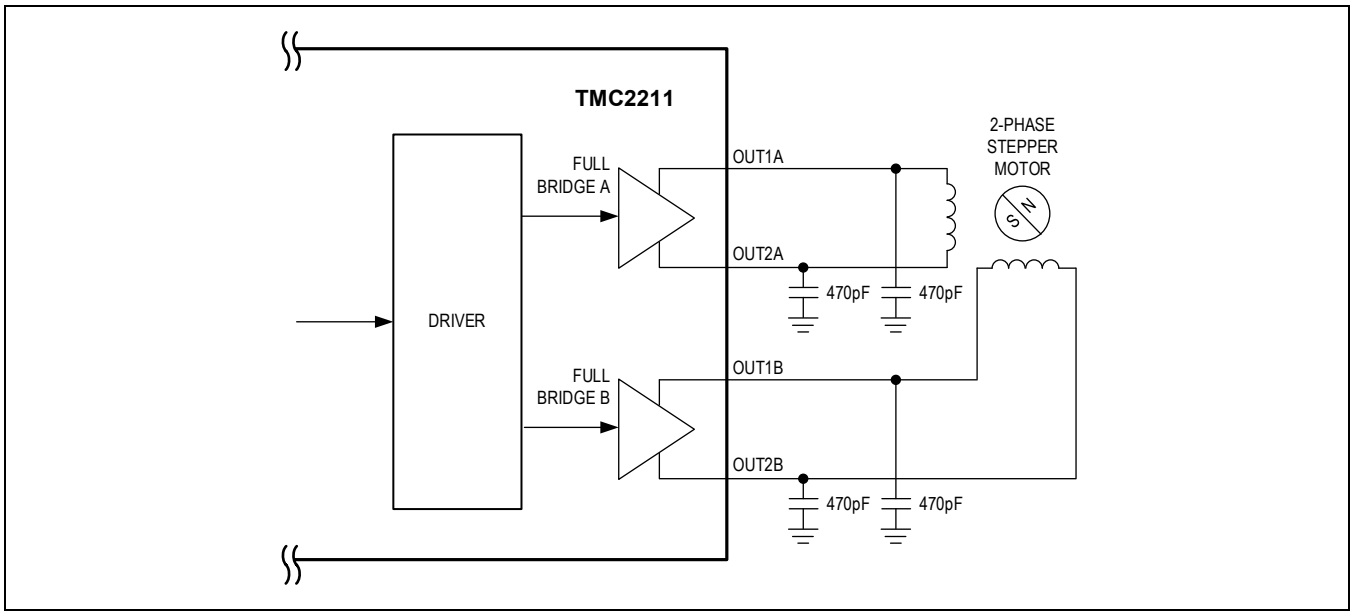



*Figure 12. Simple ESD Enhancement*

A more elaborate scheme uses LC filters to decouple the driver outputs from the motor connector. Varistors V1 and V2 between the coil terminals eliminate coil overvoltage caused by live plugging. Optionally, protect all outputs by a varistor (V1A, V1B, V2A, and V2B) against the ESD voltage. Fit the varistors to the supply voltage rating. The surface-mount device (SMD) inductivities conduct full motor coil current and must be selected accordingly.

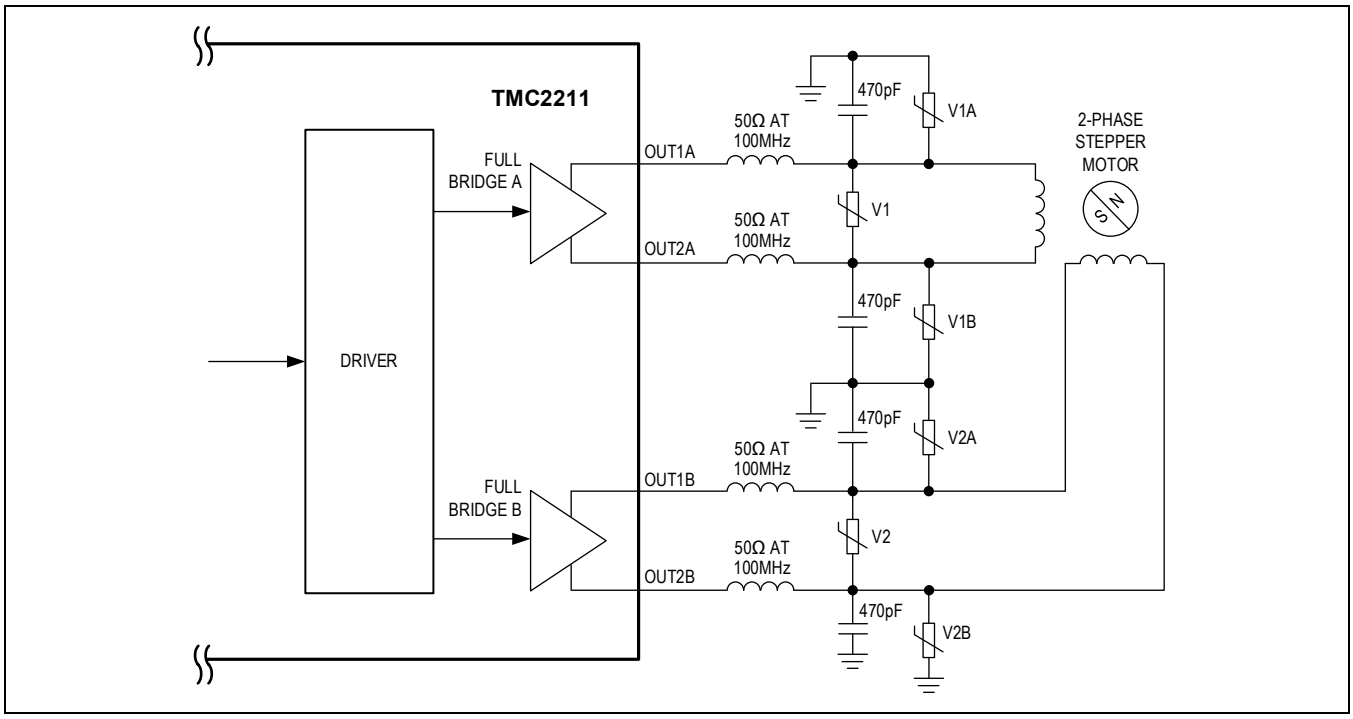



*Figure 13. Extended Motor Output Protection*

## Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PIN-PACKAGE |
|---|---|---|
| TMC2211ATU+ | -40°C to +125°C | 38 TQFN - 5mm x 7mm |
| TMC2211ATU+T | -40°C to +125°C | 38 TQFN - 5mm x 7mm |

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 01/26 | Initial release | — |

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