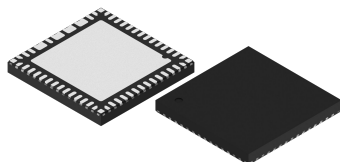


## Automotive power management IC for highly integrated processors



VFQFN56 + 4L  
8x8x0.9 mm

| Maturity status link      |
|---------------------------|
| <a href="#">SPSB100GS</a> |

| Device summary |
|----------------|
| SPSB100GSTR    |
| SPSB100GBSTR   |

### Features



- AEC-Q100 grade 1 qualified
- Two configurable (6.5 V, 5 V, 3.3 V) buck converters (up to 3.0 A) @ 2.4 MHz or 400 kHz
- One buck converter dedicated to the core power supply at 1.02V (up to 6 A) @ 2.4 MHz, with fine-tuning configurability from 0.99 V to 1.05 V
- Overcurrent detection and limitation for all bucks
- Integrated soft-start on buck stages
- Boost controller 6 - 9 V with a max current capability of 3.5 A @ 400 kHz, for sustaining permanently low battery conditions and deep cranking pulses with boost modes
- One 5 V voltage regulator (120 mA) for CAN-FD supply
- One configurable (5 V or 3.3 V) low drop voltage tracker of buck regulator (10 mA)
- One high-side driver for contact monitoring ( $R_{ON} = 55 \Omega$ ) with open-load and overcurrent diagnosis
- Dedicated interrupt pin for failure communication
- Device can operate in low-power mode
- Very low quiescent current in deep sleep state
- MCU reset generator
- Configurable window watchdog with an extended long open window up to 9 s, with maskable function and enable/disable function through NVM bits
- 1 CAN-FD transceiver (ISO 11898-2/2016 compliant), which can be deactivated via SPI, with local failure and bus failure diagnosis
- Device contains temperature warning and protection
- Thermal clusters
- A/D conversion of supply voltages and internal temperature sensors
- STMicroelectronics standard serial peripheral interface (32-bit / ST\_SPI) including 4-bit CRC
- One fail-safe output
- One input pin supporting static and dynamic error signal reporting
- Programmable periodic system wake-up feature
- Programmable periodic system wake-up feature extended up to 180 days (Very Long Duration Timer)
- Documentation available for customers that need support when dealing with ASIL requirements as per ISO26262

### Description

The **SPSB100GS** is a fully integrated automotive power management system IC, specifically designed for highly integrated application processors (e.g. Stellar G and P MCU families), offering low-power mode and high-current capability. The device comes with enhanced system power supply functionality and a CAN-FD physical communication layer (available only on the **SPSB100GS** version).

It combines three switch-mode power supplies together with two integrated linear voltage regulators. The device further integrates two wake-up inputs and advanced fail-safe functionalities. The device also embeds a Long Duration Timer up to 180 days.

The boost controller is intended to sustain cold cranking pulses, start-stop, and weak battery conditions.

Different combinations make it possible to supply the system microcontroller, the integrated CAN-FD transceiver (only for the SPSB100GS version), and external peripheral loads and sensors in several adjustable voltage and current ranges. The SPSB100GS and the SPSB100GBS are delivered out of STMicroelectronics factory with default values (rails, power-up and -down sequences) stored in the USER-NVM space as reported in System Supply Configuration 1, but can be also re-programmed by customers based on different application needs.

The STMicroelectronics standard SPI interface allows for control and diagnosis of the device and enables generic software development.

The device offers a set of features to support applications that need to fulfill functional safety requirements as defined by Automotive Safety Integrity Level (ASIL).

## 1 Block diagrams

Figure 1. SPSB100GS block diagram

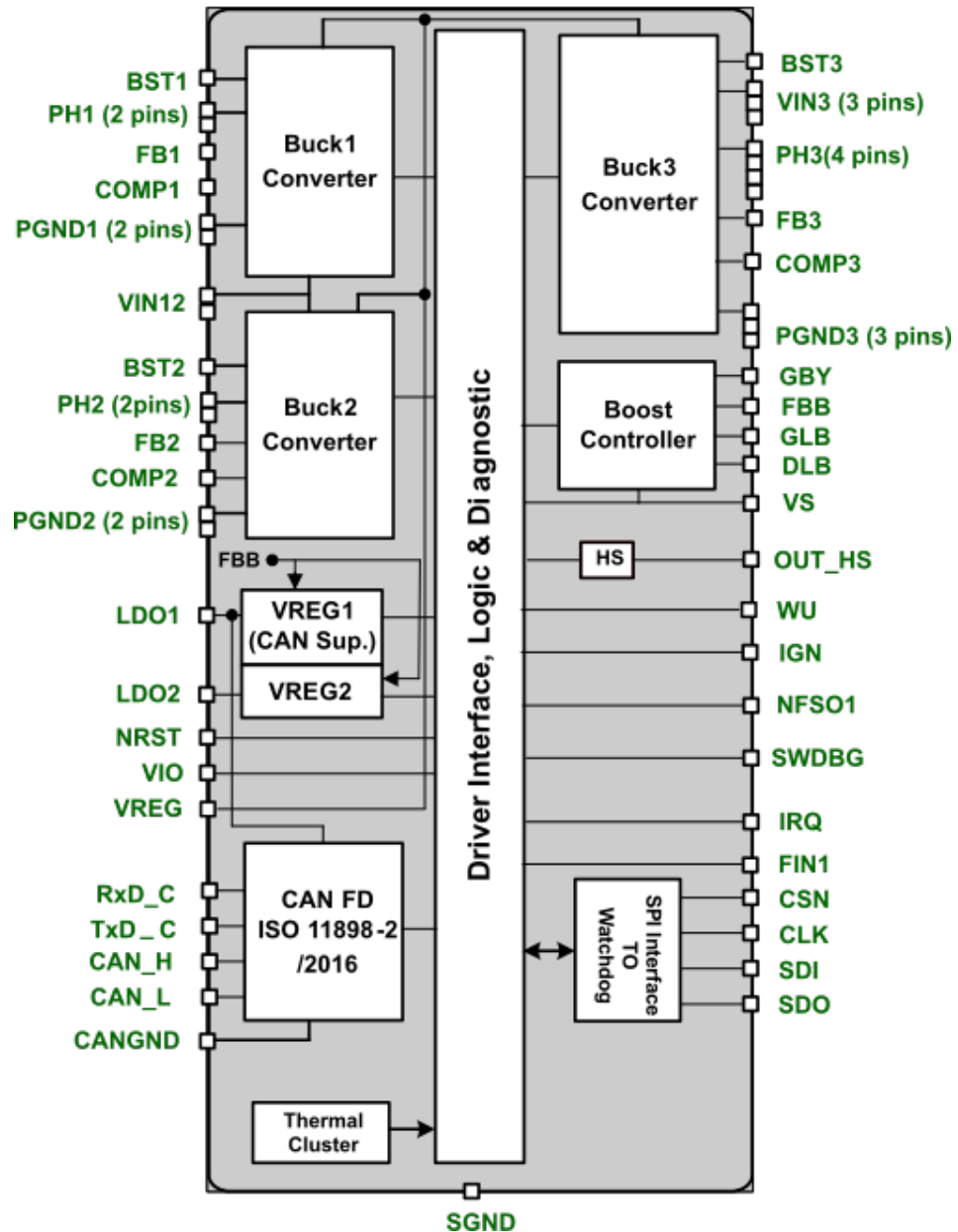
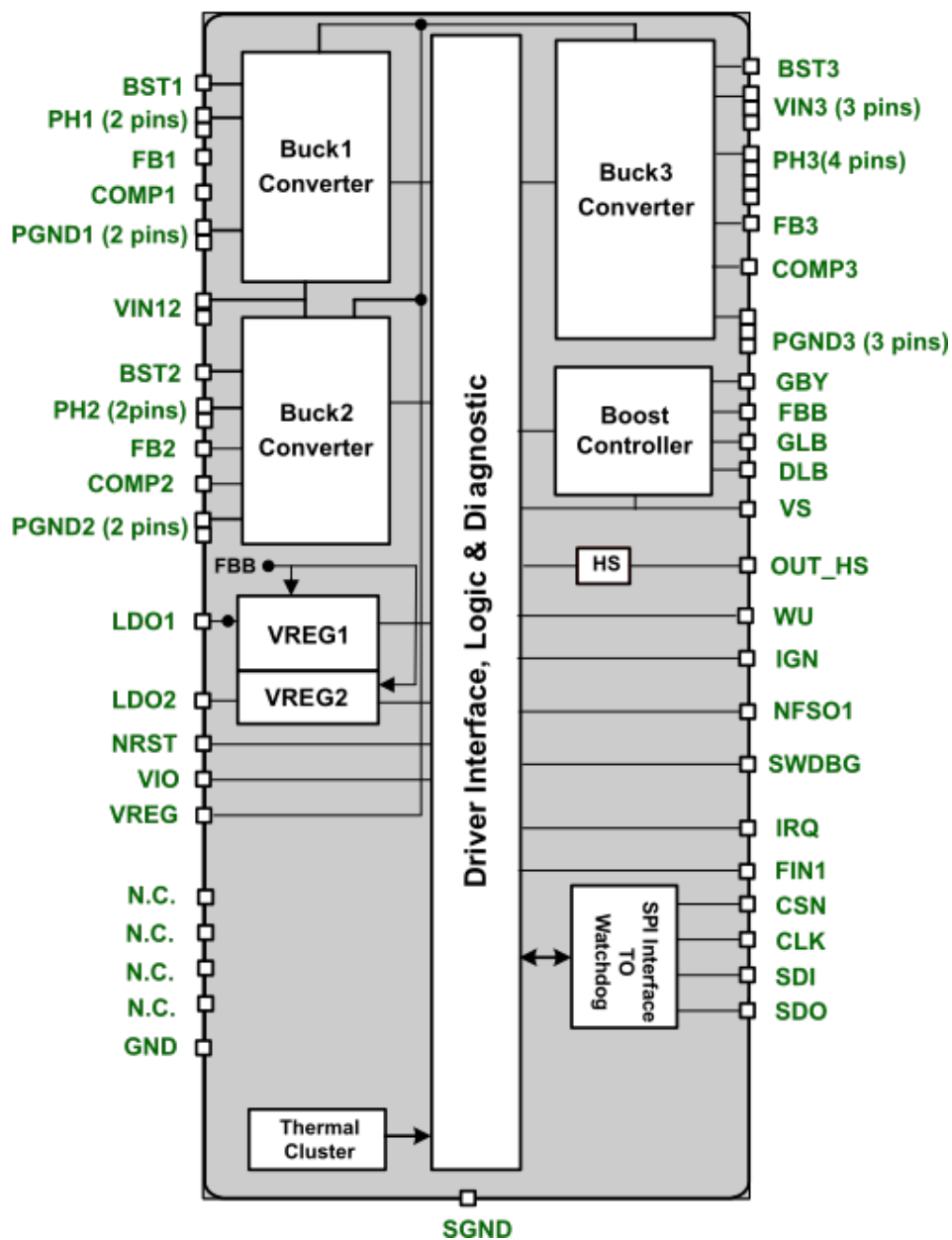


Figure 2. SPSB100GS block diagram



Prerelease product(s)

## 1.1 Pin description

Figure 3. SPSB100GS pin connection (top view)

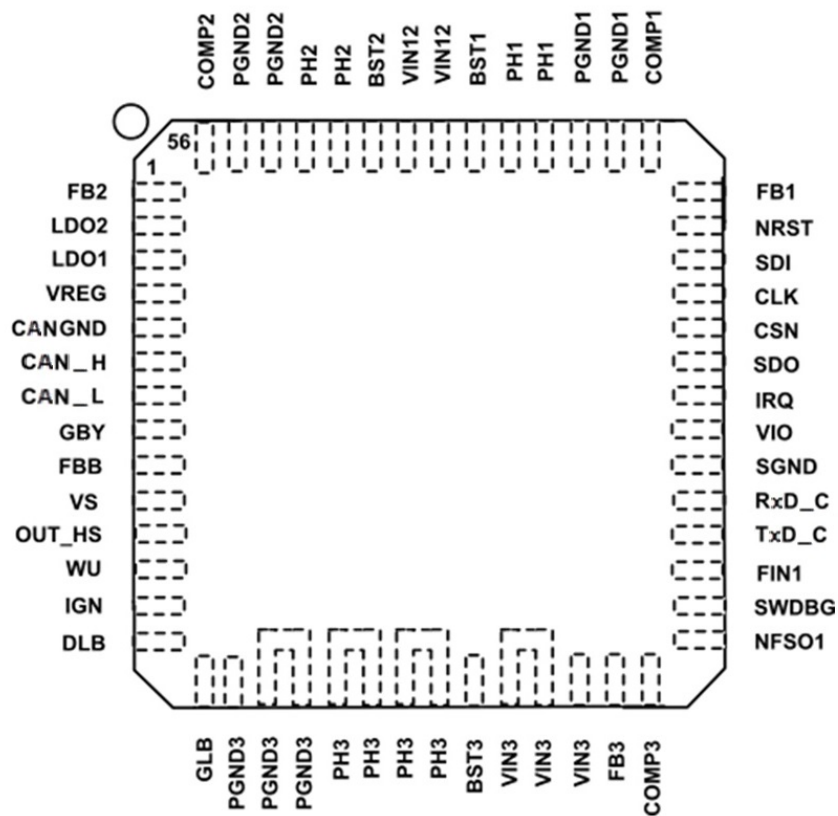
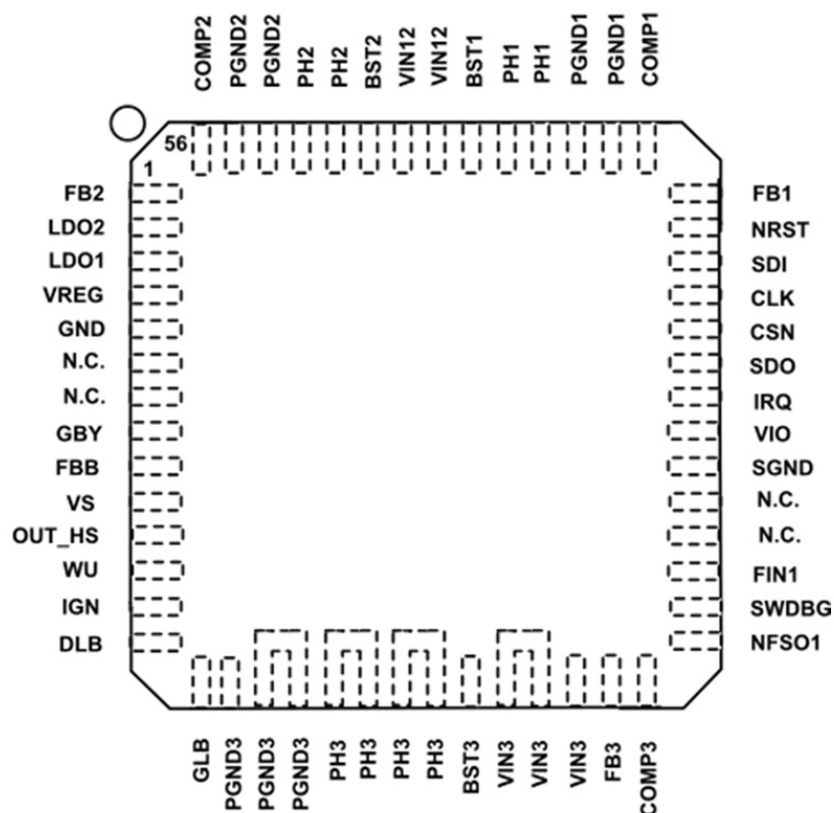


**Figure 4. SPSB100GBS pin connection (top view)**

**Table 1. Pin configuration**

| Pin number | Pin SPSB100GS | Pin SPSB100GBS      | Description                                                                    | I/O type |
|------------|---------------|---------------------|--------------------------------------------------------------------------------|----------|
| 1          | FB2           | FB2                 | BUCK2 feedback voltage (to internal voltage monitors)                          | I        |
| 2          | LDO2          | LDO2                | 5 V/3.3 V voltage regulator - tracker of buck output                           | O        |
| 3          | LDO1          | LDO1                | 5 V voltage regulator 1 output (for CAN-FD supply)                             | O        |
| 4          | VREG          | VREG                | Internal 3.3 V regulator output for buck bootstrap                             | O        |
| 5          | CANGND        | GND                 | CAN ground / Drain source monitoring ground                                    |          |
| 6          | CAN_H         | N.C. <sup>(1)</sup> | CAN high level voltage I/O                                                     | I/O      |
| 7          | CAN_L         | N.C. <sup>(1)</sup> | CAN low level voltage I/O                                                      | I/O      |
| 8          | GBY           | GBY                 | Gate driver of external MOS bypass BOOST                                       | O        |
| 9          | FBB           | FBB                 | BOOST feedback pin and supply for LDO1 & LDO2, OUT_HS, VREG, WU and IGN blocks | I        |
| 10         | VS            | VS                  | Sensing boost input                                                            | I        |
| 11         | OUT_HS        | OUT_HS              | High-side driver output to supply contacts                                     | O        |
| 12         | WU            | WU                  | Wake-up input for static or cyclic monitoring of external contact              | I        |

| Pin number | Pin SPSB100GS              | Pin SPSB100GBS             | Description                                                                                      | I/O type |
|------------|----------------------------|----------------------------|--------------------------------------------------------------------------------------------------|----------|
| 13         | IGN                        | IGN                        | Wake-up input for static or cyclic monitoring of external contact with KL15 feature              | I        |
| 14         | DLB                        | DLB                        | Drain monitoring of external low-side MOS of BOOST                                               | I        |
| 15         | GLB                        | GLB                        | Gate driver of external low-side MOS of BOOST                                                    | O        |
| 16         | PGND3                      | PGND3                      | BUCK3 power ground                                                                               |          |
| 17         | PGND3, 2 <sup>nd</sup> pin | PGND3, 2 <sup>nd</sup> pin | BUCK3 power ground                                                                               |          |
| 18         | PGND3, 3 <sup>rd</sup> pin | PGND3, 3 <sup>rd</sup> pin | BUCK3 power ground                                                                               |          |
| 19         | PH3                        | PH3                        | Switching node BUCK3                                                                             | I/O      |
| 20         | PH3, 2 <sup>nd</sup> pin   | PH3, 2 <sup>nd</sup> pin   | Switching node BUCK3                                                                             | O        |
| 21         | PH3, 3 <sup>rd</sup> pin   | PH3, 3 <sup>rd</sup> pin   | Switching node BUCK3                                                                             | O        |
| 22         | PH3, 4 <sup>th</sup> pin   | PH3, 4 <sup>th</sup> pin   | Switching node BUCK3                                                                             | O        |
| 23         | BST3                       | BST3                       | Boot-strap capacitor to supply BUCK3 high-side MOS gate-driver circuitry                         |          |
| 24         | VIN3                       | VIN3                       | Input voltage BUCK3                                                                              | I        |
| 25         | VIN3, 2 <sup>nd</sup> pin  | VIN3, 2 <sup>nd</sup> pin  | Input voltage BUCK3                                                                              | I        |
| 26         | VIN3, 3 <sup>rd</sup> pin  | VIN3, 3 <sup>rd</sup> pin  | Input voltage BUCK3                                                                              | I        |
| 27         | FB3                        | FB3                        | BUCK3 feedback voltage (to internal voltage monitors)                                            | I        |
| 28         | COMP3                      | COMP3                      | BUCK3 error amplifier compensation network                                                       |          |
| 29         | NFSO1                      | NFSO1                      | Fail safe output (active low, open drain)                                                        | O        |
| 30         | SWDBG                      | SWDBG                      | Debug input to deactivate the window watchdog (active high) and enter pin for NVM emulation mode | I        |
| 31         | FIN1                       | FIN1                       | FCCU sequence input                                                                              | I        |
| 32         | TxD_C                      | N.C. <sup>(1)</sup>        | CAN transmit data input                                                                          | I        |
| 33         | RxD_C                      | N.C. <sup>(1)</sup>        | CAN receive data output                                                                          | O        |
| 34         | SGND                       | SGND                       | Signal ground (analog and digital reference)                                                     |          |
| 35         | VIO                        | VIO                        | I/O power supply (3.3 V or 5 V)                                                                  | I        |
| 36         | IRQ                        | IRQ                        | Interrupt (open-drain)                                                                           | O        |
| 37         | SDO                        | SDO                        | SPI serial data output                                                                           | O        |
| 38         | CSN                        | CSN                        | SPI chip select not input                                                                        | I        |
| 39         | CLK                        | CLK                        | SPI serial clock input                                                                           | I        |
| 40         | SDI                        | SDI                        | SPI serial data Input                                                                            | I        |
| 41         | NRST                       | NRST                       | Reset output to microcontroller, internal pull-up (open-drain)                                   | O        |
| 42         | FB1                        | FB1                        | BUCK1 feedback voltage (to internal voltage monitors)                                            | I        |
| 43         | COMP1                      | COMP1                      | BUCK1 error amplifier compensation network                                                       |          |

| Pin number | Pin SPSB100GS              | Pin SPSB100GBS             | Description                                                             | I/O type |
|------------|----------------------------|----------------------------|-------------------------------------------------------------------------|----------|
| 44         | PGND1                      | PGND1                      | BUCK1 power ground                                                      |          |
| 45         | PGND1, 2 <sup>nd</sup> pin | PGND1, 2 <sup>nd</sup> pin | BUCK1 power ground                                                      |          |
| 46         | PH1                        | PH1                        | Switching node BUCK1                                                    | I/O      |
| 47         | PH1, 2 <sup>nd</sup> pin   | PH1, 2 <sup>nd</sup> pin   | Switching node BUCK1                                                    | O        |
| 48         | BST1                       | BST1                       | Bootstrap capacitor to supply BUCK1 high-side MOS gate-driver circuitry |          |
| 49         | VIN12                      | VIN12                      | Input voltage BUCK1 and BUCK2                                           | I        |
| 50         | VIN12                      | VIN12                      | Input voltage BUCK1 and BUCK2                                           | I        |
| 51         | BST2                       | BST2                       | Bootstrap capacitor to supply BUCK2 high-side MOS gate-driver circuitry |          |
| 52         | PH2                        | PH2                        | Switching node BUCK2                                                    | I/O      |
| 53         | PH2, 2 <sup>nd</sup> pin   | PH2, 2 <sup>nd</sup> pin   | Switching node BUCK2                                                    | O        |
| 54         | PGND2,                     | PGND2,                     | BUCK2 power ground                                                      |          |
| 55         | PGND2, 2 <sup>nd</sup> pin | PGND2, 2 <sup>nd</sup> pin | BUCK2 power ground                                                      |          |
| 56         | COMP2                      | COMP2                      | BUCK2 error amplifier compensation network                              |          |

1. For the SPSB100GBS version, it is recommended to connect the N.C. pins to ground.

## 2 Maximum ratings

### 2.1 Operating range

Within the operating range, the part operates as specified and without any parameter deviations. The device may not operate properly if maximum operating conditions are exceeded.

Once taken beyond the operative ratings and returned back to within the specified range, the part recovers with no damage or degradation.

Additional supply voltage and temperature conditions are given separately at the beginning of each electrical specification table.

All voltages are related to the potential at the CANGND pin internally connected to the substrate.

**Table 2. Operating conditions**

| Symbol                   | Parameter                    | Min. | Typ. | Max. | Unit |
|--------------------------|------------------------------|------|------|------|------|
| $V_S$ <sup>(1) (2)</sup> | Global                       | 3    |      | 29   | V    |
| $F_{BB}$                 | Boost output                 | 7.7  |      | 29   | V    |
| $V_{IN12}$               | Buck1 & Buck2 supply pin     | 7.7  |      | 29   | V    |
| $V_{IN3}$                | Buck3 supply pin             | 3    |      | 7    | V    |
| VIO                      | Digital interface supply pin | 3    |      | 5.5  | V    |

1.  $V_S$  operating range from 3 V up to 6 V is intended as a transitory time during cranking conditions.

2. The device is compatible to Jump start events up to 29 V maximum  $V_S$  voltage.

#### 2.1.1 Supply voltage ranges

All SPI communication, logic and oscillator parameters work down to  $V_S = V_{PORVS\_F}$  and are specified accordingly:

- SPI thresholds
- Oscillator frequency (delay times correctly elapsed)
- Internal register status correctly kept (reset at default values for  $V_S < V_{PORVS\_F}$ )
- Reset threshold correctly detected

### 2.2 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

All voltages are related to the potential at the substrate ground pin.

**Table 3. Absolute maximum ratings**

| Symbol        | Parameter                                                                | Condition                                          | Min. | Typ. | Max. | Unit |
|---------------|--------------------------------------------------------------------------|----------------------------------------------------|------|------|------|------|
| $V_{S\_LD}$   | DC supply voltage                                                        | Load dump 400 ms max.                              | -0.3 |      | 40   | V    |
| $V_{S\_rev}$  | DC supply voltage for reverse battery                                    | Reverse battery with limited current at max. 30 mA | -1.0 |      |      | V    |
| $V_{FBB\_LD}$ | Boost output voltage range<br>Supply for LDO1&2, OUT_HS, IGN & WU blocks | Load dump 400 ms max.                              | -0.3 |      | 40   | V    |
| $V_{GLB}$     | Boost gate driver voltage range                                          | $V_{GLB} < V_{FBB} + 0.3$ V                        | -0.3 |      | 13.4 | V    |
| $V_{DLB}$     | Boost external drain voltage range                                       |                                                    | -0.3 |      | 40   | V    |
| $V_{GBY}$     | Bypass gate driver voltage range                                         | $V_{GBY} < V_{FBB} + 0.3$ V                        | -0.3 |      | 40   | V    |

| Symbol                          | Parameter                                                            | Condition                                                           | Min. | Typ. | Max. | Unit |
|---------------------------------|----------------------------------------------------------------------|---------------------------------------------------------------------|------|------|------|------|
| V <sub>REG</sub>                | 3.3 V regulator output for bucks bootstrap                           |                                                                     | -0.3 |      | 4.6  | V    |
| V <sub>IN12_LD</sub>            | Buck1&2 input voltage range                                          | V <sub>IN12</sub> < V <sub>FBB</sub> + 0.3 V, load dump 400 ms max. | -0.3 |      | 40   | V    |
| V <sub>FB1</sub>                | Buck1 feedback voltage range                                         | V <sub>FB1</sub> < V <sub>FBB</sub> + 0.3 V                         | -0.3 |      | 20   | V    |
| V <sub>FB2</sub>                | Buck2 feedback voltage range                                         | V <sub>FB2</sub> < V <sub>FBB</sub> + 0.3 V                         | -0.3 |      | 20   | V    |
| V <sub>PH1</sub> <sup>(1)</sup> | Buck1 phase output voltage range                                     |                                                                     | -0.3 |      | 40   | V    |
| V <sub>PH2</sub> <sup>(1)</sup> | Buck2 phase output voltage range                                     |                                                                     | -0.3 |      | 40   | V    |
| V <sub>BST1</sub>               | Buck1 bootstrap voltage range                                        | V <sub>BST1</sub> < V <sub>PH1</sub> + 4.6 V                        | -0.3 |      | 40   | V    |
| V <sub>BST2</sub>               | Buck2 bootstrap voltage range                                        | V <sub>BST2</sub> < V <sub>PH2</sub> + 4.6 V                        | -0.3 |      | 40   | V    |
| V <sub>COMP1</sub>              | Buck1 compensation voltage range                                     |                                                                     | -0.3 |      | 4.6  | V    |
| V <sub>COMP2</sub>              | Buck2 compensation voltage range                                     |                                                                     | -0.3 |      | 4.6  | V    |
| V <sub>IN3</sub>                | Buck3 input voltage range                                            |                                                                     | -0.3 |      | 20   | V    |
| V <sub>FB3</sub>                | Buck3 feedback voltage range                                         |                                                                     | -0.3 |      | 20   | V    |
| V <sub>PH3</sub> <sup>(1)</sup> | Buck3 output phase voltage range                                     |                                                                     | -0.3 |      | 20   | V    |
| V <sub>BST3</sub>               | Buck3 bootstrap voltage range                                        | V <sub>BST3</sub> < V <sub>PH3</sub> + 4.6 V                        | -0.3 |      | 20   | V    |
| V <sub>COMP3</sub>              | Buck3 compensation voltage range                                     |                                                                     | -0.3 |      | 4.6  | V    |
| V <sub>LDO1</sub>               | Stabilized supply voltage 1                                          | V <sub>LDO1</sub> < V <sub>FBB</sub> + 0.3 V                        | -0.3 |      | 6.5  | V    |
| V <sub>LDO2</sub>               | Stabilized supply voltage 2                                          | V <sub>LDO2</sub> < V <sub>FBB</sub> + 0.3 V                        | -0.3 |      | 20   | V    |
| V <sub>IO</sub>                 | I/O supply voltage                                                   |                                                                     | -0.3 |      | 20   | V    |
| V <sub>SDI</sub>                | Logic input                                                          |                                                                     | -0.3 |      | 20   | V    |
| V <sub>CLK</sub>                | Logic input                                                          |                                                                     | -0.3 |      | 20   | V    |
| V <sub>CSN</sub>                | Logic input                                                          |                                                                     | -0.3 |      | 20   | V    |
| V <sub>SDO</sub>                | Logic output                                                         |                                                                     | -0.3 |      | 20   | V    |
| V <sub>RXD_C</sub>              | Logic output                                                         |                                                                     | -0.3 |      | 20   | V    |
| V <sub>NRST</sub>               | Open-drain output (with internal pull-up)                            |                                                                     | -0.3 |      | 20   | V    |
| V <sub>IRQ</sub>                | Open-drain output (with internal pull-up)                            |                                                                     | -0.3 |      | 20   | V    |
| V <sub>TXD_C</sub>              | Logic input                                                          |                                                                     | -0.3 |      | 20   | V    |
| V <sub>SWDBG</sub>              | Debug input pin voltage range                                        |                                                                     | -0.3 |      | 20   | V    |
| V <sub>FIN1</sub>               | FIN1 input voltage range                                             |                                                                     | -0.3 |      | 20   | V    |
| V <sub>NFSO1</sub>              | Open-drain output (without internal pull-up)                         |                                                                     | -0.3 |      | 40   | V    |
| V <sub>WU_LD</sub>              | DC WU input voltage                                                  | Load dump 400 ms max.                                               | -0.3 |      | 40   | V    |
| V <sub>IGN_LD</sub>             | DC IGN input voltage                                                 | Load dump 400 ms max.                                               | -0.3 |      | 40   | V    |
| I <sub>Input</sub>              | Current injection into FBB related input pins WU, IGN <sup>(2)</sup> |                                                                     | -20  |      | 20   | mA   |
| V <sub>CAN_H</sub>              | CAN bus I/O                                                          |                                                                     | -27  |      | 40   | V    |
| V <sub>CAN_L</sub>              | CAN bus I/O                                                          |                                                                     | -27  |      | 40   | V    |
| V <sub>OUT_HS</sub>             | Output voltage                                                       | V <sub>OUT_HS</sub> < F <sub>BB</sub> + 0.3 V                       | -0.3 |      | 40   | V    |
| I <sub>OUT_HS</sub>             | Current injection OUT_HS <sup>(2)</sup>                              |                                                                     | -20  |      | 20   | mA   |

| Symbol                 | Parameter                                                | Condition | Min.  | Typ. | Max. | Unit |
|------------------------|----------------------------------------------------------|-----------|-------|------|------|------|
| $I_{SGND}^{(3)}$       | Maximum current at SGND <sup>(3)</sup>                   |           | -1.25 |      | 1.25 | A    |
| $I_{VIN12}$            | Maximum current at VIN12 <sup>(3)</sup> (for each pin)   |           | -5    |      | 5    | A    |
| $I_{PGND1}, I_{PGND2}$ | Maximum current at PGND1&2 <sup>(3)</sup> (for each pin) |           | -5    |      | 5    | A    |
| $I_{PH1}, I_{PH2}$     | Maximum current at PH1&2 <sup>(3)</sup> (for each pin)   |           | -5    |      | 5    | A    |
| $I_{VIN3}$             | Maximum current at VIN3 <sup>(3)</sup> (for each pin)    |           | -5    |      | 5    | A    |
| $I_{PGND3}$            | Maximum current at PGND3 <sup>(3)</sup> (for each pin)   |           | -5    |      | 5    | A    |
| $I_{PH3}$              | Maximum current at PH3 <sup>(3)</sup> (for each pin)     |           | -5    |      | 5    | A    |
| $V_{PGND}$             | PGND versus CANGND                                       |           | -0.3  |      | 0.3  | V    |
| $V_{GND}$              | SGND versus CANGND                                       |           | -0.3  |      | 0.3  | V    |

1. Transients on this pin can be tolerated for a duration < 100 ns, not exceeding -3 V.
2. Guaranteed by design.
3. Values for the absolute maximum DC current through the bond wires. This value does not consider maximum power dissipation or other limits. Guaranteed by design.

## 2.3 ESD robustness

**Table 4. ESD protection**

| Symbol              | Parameter | Condition                                | Min.          | Typ. | Max.        | Unit |
|---------------------|-----------|------------------------------------------|---------------|------|-------------|------|
| Pins                | All pins  | HBM <sup>(1)</sup>                       | -2            |      | 2           | kV   |
| Power output pin    | OUT_HS    | HBM <sup>(2)</sup>                       | -4            |      | 4           | kV   |
| Transceiver         | CAN_H     | HBM <sup>(2)</sup>                       | -8            |      | 8           | kV   |
| Transceiver         | CAN_H     | Direct ESD <sup>(3)</sup>                | -6            |      | 6           | kV   |
| Transceiver         | CAN_L     | HBM <sup>(2)</sup>                       | -8            |      | 8           | kV   |
| Transceiver         | CAN_L     | Direct ESD <sup>(3)</sup>                | -6            |      | 6           | kV   |
| Pins <sup>(4)</sup> | All pins  | CDM (values for corner pins in brackets) | -500 / (-750) |      | 500 / (750) | V    |

1. HBM (Human Body Model, 100 pF, 1.5 kΩ) according to AEC-Q100-002.
2. HBM with all non-zapped pins grounded.
3. Direct ESD Test according to ISO 10605 (150 pF, 330 Ω) and IEC62228-3.
4. CDM (Charged Device Model) according to AEC-Q100-011.

## 2.4 Temperature ranges and thermal data

**Table 5. Temperature ranges and thermal data**

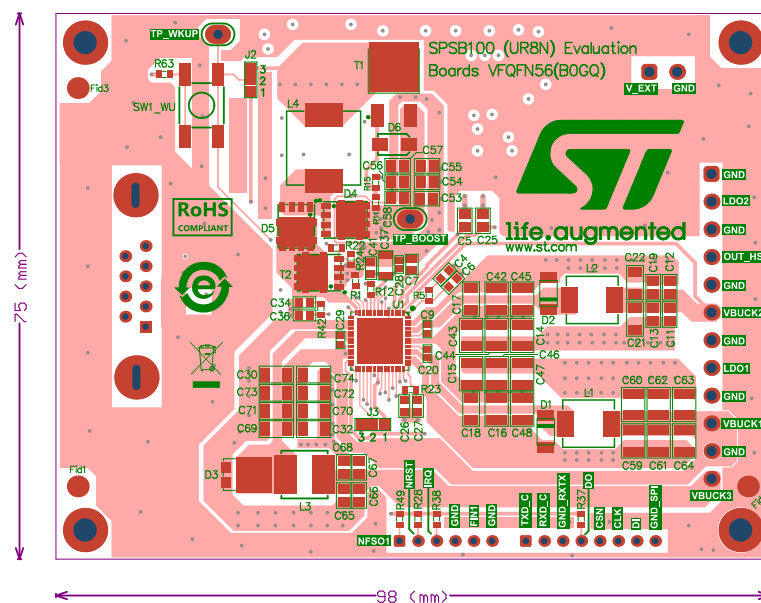
| Symbol    | Parameter                      | Condition | Min. | Typ. | Max. | Unit |
|-----------|--------------------------------|-----------|------|------|------|------|
| $T_{amb}$ | Operating temperature          |           | -40  | -    | 125  | °C   |
| $T_j$     | Operating junction temperature |           | -40  | -    | 175  | °C   |
| $T_{stg}$ | Storage temperature            |           | -55  | -    | 150  | °C   |

| Symbol           | Parameter                                                                                | Condition                   | Min. | Typ. | Max. | Unit |
|------------------|------------------------------------------------------------------------------------------|-----------------------------|------|------|------|------|
| $T_W$            | Thermal overtemperature warning threshold                                                |                             | 140  | -    | 160  | °C   |
| $T_{SD}$         | Thermal shut-down junction temperature                                                   |                             | 165  | -    | 185  | °C   |
| $T_{SDC}$        | Central thermal shut-down junction temperature                                           |                             | 175  | -    | 195  | °C   |
| $T_{SDhys}$      | Thermal shut-down temperature hysteresis                                                 |                             | 0    | 5    | 10   | °C   |
| $T_{F\_TJ}$      | Thermal warning/shut-down filter time                                                    | Covered by scan             | 60   | 75   | 90   | µs   |
| $T_{F\_TSDC}$    | Central thermal shut-down filter time                                                    | Covered by scan             | 25.6 | 32   | 38.4 | µs   |
| $R_{Th\_j-amb}$  | Thermal resistance junction-to-ambient                                                   | JEDEC 2s2p board (JESD51-7) | 25   |      |      | °C/W |
| $R_{Th\_j-Cbot}$ | Thermal resistance junction-to-Case bottom with uniform power dissipation on silicon die | JEDEC 2s2p board            | 0.5  |      |      | °C/W |

All parameters are guaranteed in the junction temperature range from -40 to +150 °C (unless otherwise specified). The device is still operational and functional up to 175 °C.

The SPSB100GS embeds a multitude of junctions housed in a relatively small piece of silicon. The devices contain, among all the described features, two voltage regulators (one of which can operate as a voltage tracker) and three buck converters with internal power stages and one high-side driver. For this reason, using the thermal impedance of a single junction (i.e. the voltage regulator or major power dissipation contributor) does not allow prediction of the thermal behavior of the whole device, and therefore it is not possible to assess whether a device is thermally suitable for a given activation profile and load characteristics. Thermal information is provided as temperature readings by different clusters located close to the most dissipative junctions. Some representative and realistic case thermal profiles are described below:

**Figure 5. VFQFN56+4L printed circuit board, 4 layers - top layer**



Two typical application scenarios related to system configuration 1 and differentiated based on the selected Buck1,2 frequencies are described below:

$V_{bat} = 16\text{ V}$ ,  $R_{thja} = 25^\circ\text{C/W}$ ,  $T_{jmax} = 170^\circ\text{C}$

#### Case A

- LDO1 (5 V): output load 100 mA
- LDO2 (5 V): output load 5 mA
- OUT\_HS:  $I_{LOAD} = 20$  mA
- Buck1 (3.3 V): output load 1 A at 400 kHz
- Buck2 (5.0 V): output load 1 A at 400 kHz
- Buck3 (1.02 V): output load 2 A at 2.4 MHz

**Case B**

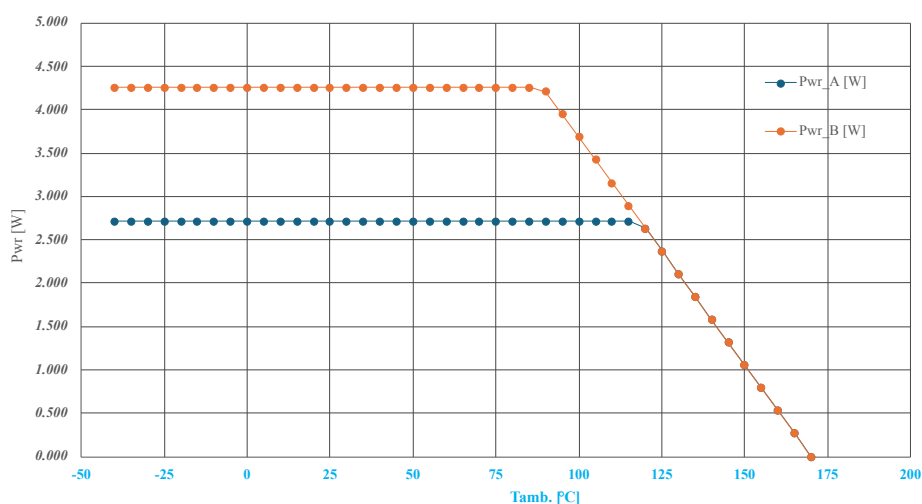
- LDO1 (5 V): output load 100 mA
- LDO2 (5 V): output load 5 mA
- OUT\_HS:  $I_{LOAD} = 20$  mA
- Buck1 (3.3 V): output load 1 A at 2.4 MHz
- Buck2 (5.0 V): output load 1 A at 2.4 MHz
- Buck3 (1.02 V): output load 2 A at 2.4 MHz

Note:

1. Buck3 load current is already considered in the power dissipation calculation, so 1 A is referred to Buck1 external load current.
2. Selecting the switching frequency at 2.4 MHz for Buck1 and Buck2 will lower the regulators efficiency. In applications where high output power requirements significantly affect total power dissipation, using a 400 kHz switching frequency for Buck1 and Buck2 is recommended to reduce global power losses and simplify the thermal management design.

The curves below illustrate the range of ambient temperature within which the total power dissipation for use cases A and B can be sustained. The ambient temperature at which the curves drop indicates the point where the maximum total power dissipation must be reduced to prevent activation of the over-temperature.

**Figure 6. Cases A and B power dissipation management vs. ambient temperature with Buck1 and Buck2 at 400 kHz and 2.4 MHz**



## 3 Functional description

### 3.1 Supply configurations

The battery supplies the boost controller.  $F_{BB}$ , the boost output, supplies internal regulated voltages of analog and digital blocks, the wake-up blocks, the OUT\_HS output, and fail-safe block. Buck1, Buck2, and Buck3 have independent supply pins in order to allow different supply configurations according to the application. Below, we describe the two main configurations where it is required to provide direct supply to the microcontroller core.

#### 3.1.1 System supply configuration 1

Figure 7. SPSB100GS direct supply of the microcontroller core

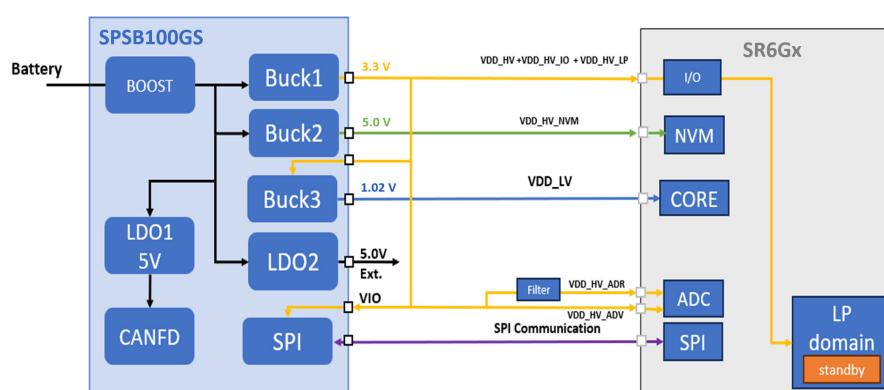
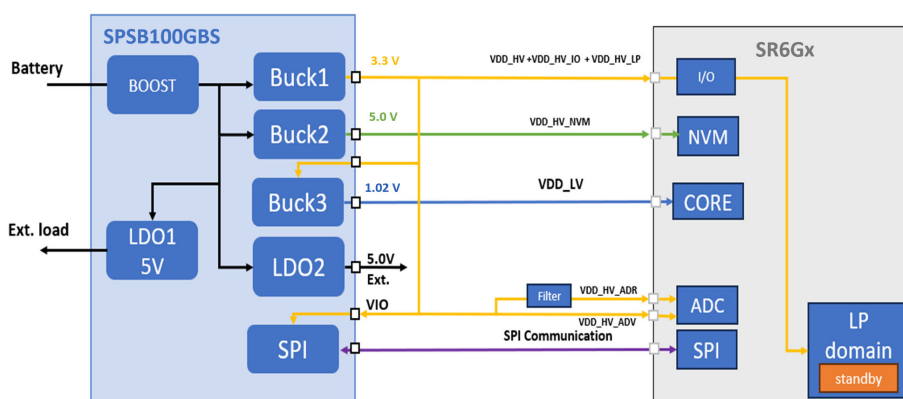


Figure 8. SPSB100GBS direct supply of the microcontroller core



In the above configurations, only differentiated for the SPSB100GS and SPSB100GBS (without transceiver), the Buck3 is supplied by Buck1 and is configured to provide a 1.02 V high-current supply to the MCU CORE. Buck1 and Buck2 are supplied by the boost and supply the 3.3 V and the 5 V. Boost always supplies LDO1 and LDO2, both providing 5 V.

For the configuration 1 default NVM settings refer to [Table 69](#).

The power-up and power-down sequence associated with this supply configuration are as follows:

Power-up sequence:

- Step 1: turn ON Buck1 at 3.3 V, wait PG (BUCK1\_PG\_OK flag)
- Step 2: turn ON Buck3 at 1.02 V, wait PG (BUCK3\_PG\_OK flag)
- Step 3: turn ON Buck2 at 5 V, wait PG (BUCK2\_PG\_OK flag)
- Step 4: turn ON LDO2 in tracker of Buck2, wait PG (LDO2\_PG\_OK flag)
- Step 5: turn ON LDO1, wait 0 ms
- Step 6: deassert NRST, wait 0 ms

Power-down sequence:

- Step 1: ASSERT NRST, wait 2 ms
- Step 2: turn OFF LDO2 and LDO1, wait 2 ms
- Step 3: turn OFF Buck3, wait 2 ms
- Step 4: turn OFF Buck1 and Buck2, wait 2ms
- Step 5: turn OFF VREG after 10ms

### 3.1.2 Digital interface supply: VIO

The VIO pin supplies the SPI interface as well as the IRQ, FIN1, NRST , RxD\_C, TxD\_C pins.

The VIO pin can be supplied from one of the SPSB100GS bucks, or from an external regulator.

Digital pin functionalities are guaranteed when  $V_{IO} > V_{VIO\_UV\_R}$  (VIO\_UV flag not raised).

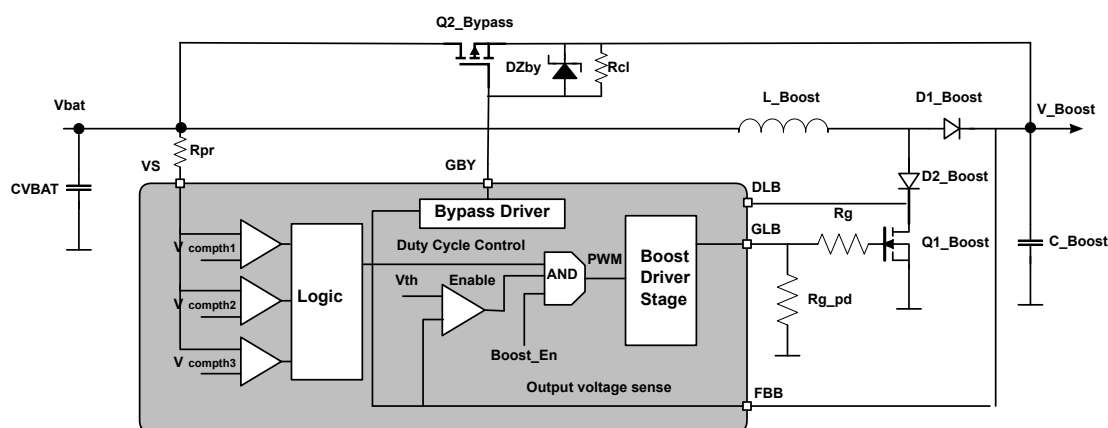
## 3.2 Boost controller

The boost, or step-up controller, generates an output voltage that supplies the SPSB100GS device and the buck converters only during a transitory time at power-up to reach a normal operating range (12 V battery range), or during low battery conditions, to sustain cranking.

In case the  $V_S$  voltage exceeds the  $V_{TH\_BYPASS\_Rx}$  threshold, the converter will be deactivated and battery supplies the buck converters via a separate bypass MOSFET: The Bypass will not be activated if the NRST is asserted.

The block diagram of the boost is shown in the figure below:

**Figure 9. Boost controller block diagram**



According to the sensed battery voltage on the VS pin ( $VS\_LOW$ ,  $VS\_MID$  and  $VS\_HIGH$  thresholds), the boost duty cycle is suitably adjusted ( $BOOST\_DC\_Max$  when  $VS$  voltage is between  $V_{PORVS\_F}$  and  $VS\_LOW$ ,  $BOOST\_DC\_High$  when  $VS$  is between  $VS\_LOW$  and  $VS\_MID$ ,  $BOOST\_DC\_Min$  when  $VS$  is between  $VS\_MID$  and  $VS\_HIGH$  and  $BOOST\_DC\_Low$  when  $VS$  is higher than  $VS\_HIGH$ ) in order to keep the output voltage quite above the selected thresholds.

The system is compliant with the newly defined "Cold Cranking Pulse" required by start-stop systems. Moreover, a suitable bypass MOSFET is driven when the BOOST is not switching, in order to bypass the inductor, minimizing overall losses during normal operation.

The boost and the bypass drivers can be switched OFF permanently by setting  $BOOST\_DIS=1$  and  $BYPASS\_DIS=1$  respectively in the USER\_NVM space.

If the BOOST function is used (BOOST\_DIS=0):

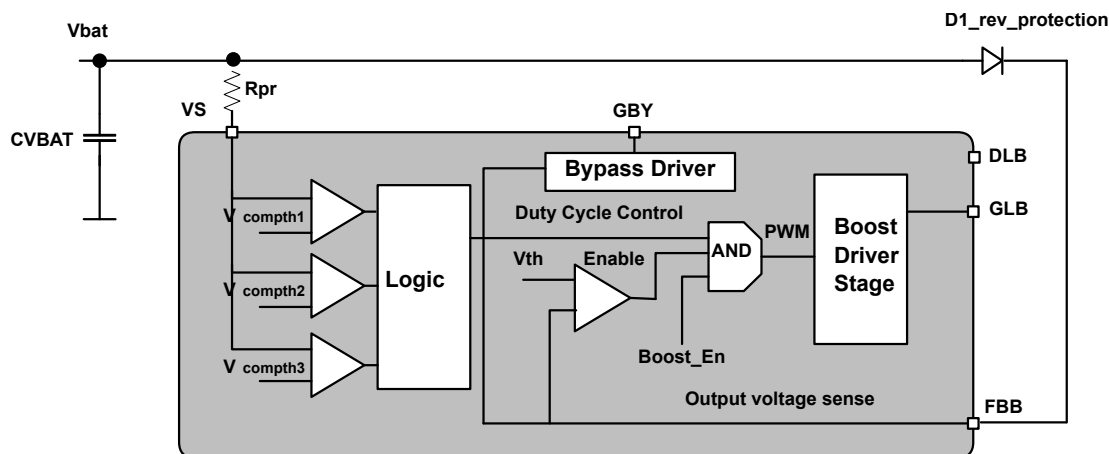
- at power-up, the bypass control is enabled when the state machine enters INIT state (after successful safety checks). If  $V_S > V_{TH\_BYPASS\_R}$ , the external bypass switch is turned on (BYPASS\_STATUS=1) while the boost PWM is stopped. When  $V_S < V_{TH\_BYPASS\_F}$ , the external switch is turned off (BYPASS\_STATUS=0) and boost switching is activated.
- in ACTIVE – FULL-POWER mode and in REC-1 state, when  $V_S > V_{TH\_BYPASS\_R}$ , the external bypass switch is turned on after  $t_{F\_BYPASS\_EN}$  timing (BYPASS\_STATUS=1) the boost PWM is stopped.  $FBB > V_{FBB\_REGx}$  thresholds. When  $V_S < V_{TH\_BYPASS\_F}$ , the bypass switch is turned off after  $t_{F\_BYPASS\_DIS}$  timing (BYPASS\_STATUS=0) and the boost switching is activated if  $FBB < V_{FBB\_REGx}$  thresholds.
- in ACTIVE – LOW-POWER mode, the BYPASS controller is disabled, turning the external switch (BYPASS\_STATUS=0) off: the consumption on the battery is limited to few mA so no dissipation issue is expected on the D1\_boost diode.
- in ACTIVE-LOW-POWER mode, the BOOST IP is disabled to reduce the overall SPSB100GS consumption. It is woken up when the monitored  $V_S$  goes below  $V_{TH\_BYPASS\_Fx}$  for the remaining active BUCK with duty cycle BOOST\_DC\_LP.
- In REC-2 or DEEP-SLEEP state, the boost is always OFF and the BYPASS controller is always disabled (BYPASS\_STATUS=0).

If the BOOST function is not used (USER-NVM BOOST\_DIS=1 or SPI bit BOOST\_OFF=1):

- at power-up, the bypass control is enabled, turning on the external switch (BYPASS\_STATUS=1), as soon as the state machine reaches the INIT state and following successful safety checks.
- in ACTIVE – FULL-POWER mode and in REC-1 state, the BYPASS switch is turned on whatever the  $V_S$  voltage (BYPASS\_STATUS = 1) and BOOST is switched OFF ( BOOST\_ENA\_STATUS = 0).
- In ACTIVE – LOW-POWER mode, DEEP-SLEEP or REC-2 state, the BYPASS controller is disabled, turning off the external switch (BYPASS\_STATUS = 0) and BOOST is switched OFF ( BOOST\_ENA\_STATUS = 0 ).

The block diagram of the device when boost is not used is shown in the figure below. Note that the D1\_rev\_protection diode is needed only if there is no reverse battery protection solution already implemented in the application.

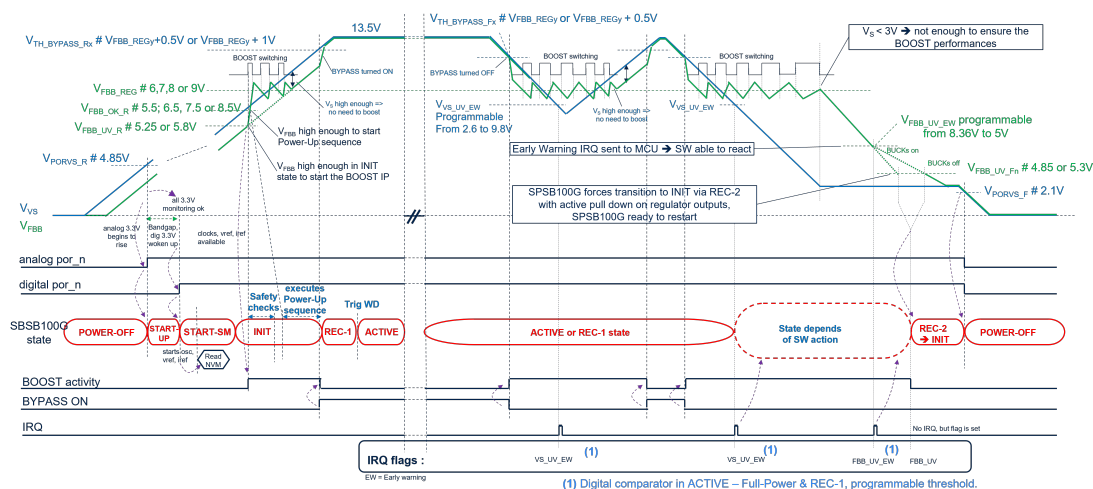
**Figure 10. Boost controller disabled block diagram**



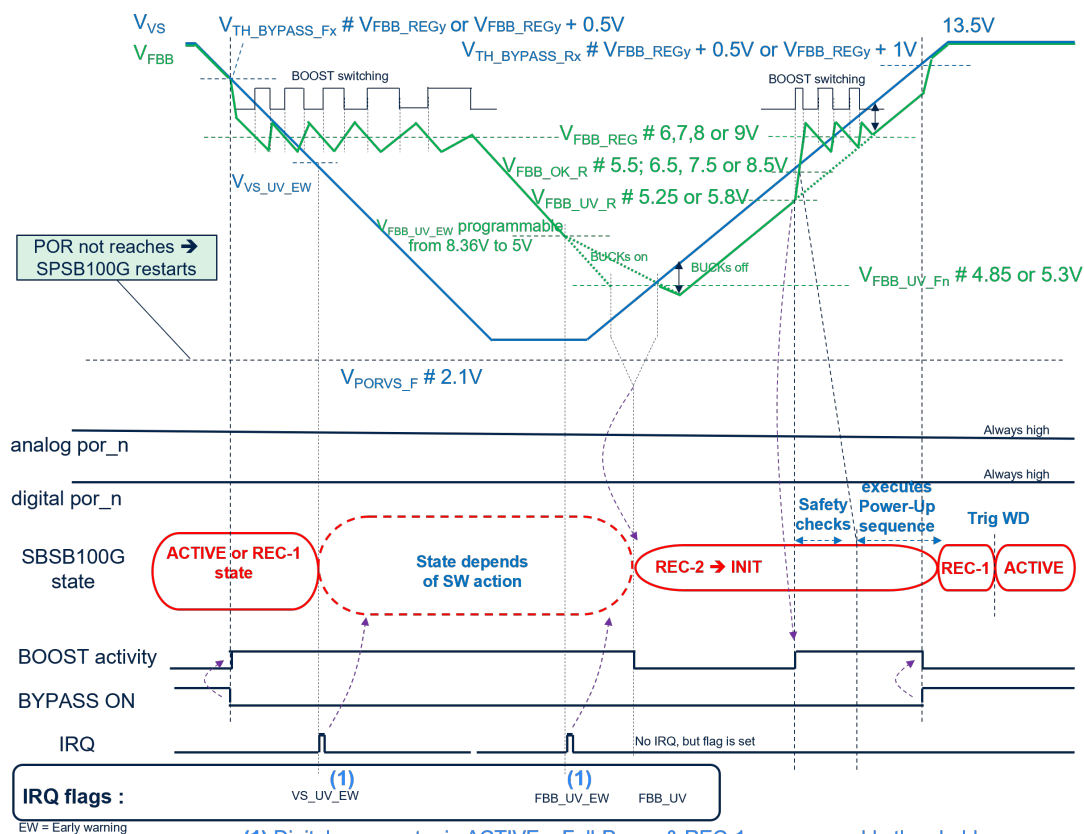
### 3.2.1 Power-up/down and voltage drop behavior

The boost role is crucial for SPSB100GS operation, so its behavior related to normal or accidental variations of the voltage supply should be clearly defined. The general behavior is described in the following figures.

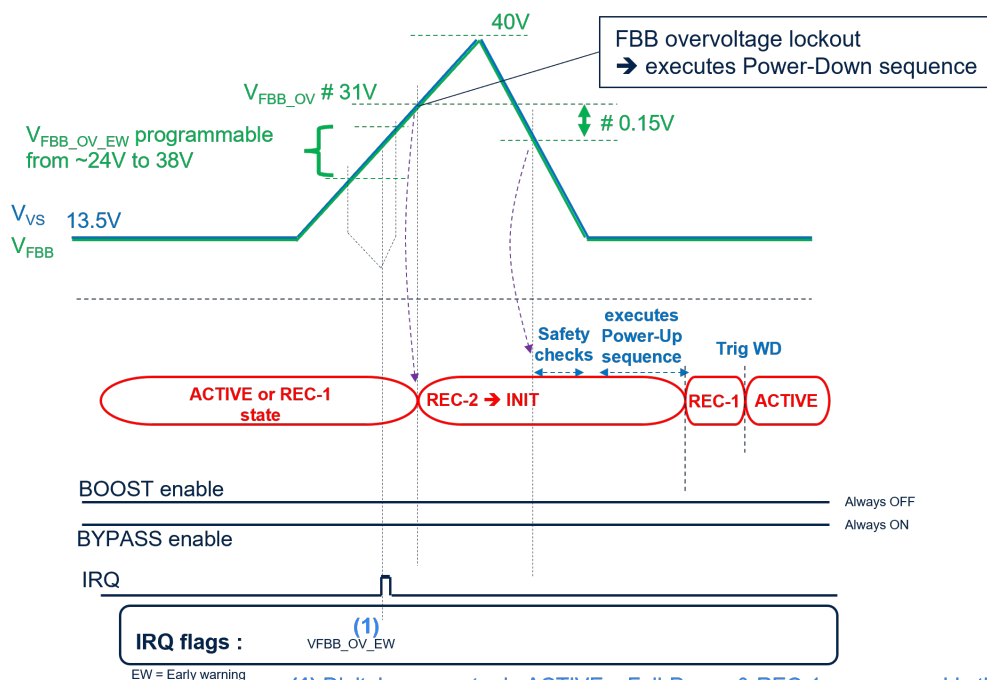
### Figure 11. Battery plug/unplug behavior



### Figure 12. Battery drop behavior



Overvoltage cases are not critical for the boost itself (bypass is ON) but for the regulators (Bucks, LDOs...) that are directly supplied. These are managed according to configured thresholds (through VFBB\_OV threshold) which trigger a power down sequence in any case. Power-up is initiated as long as the voltage decreases below the overvoltage FBB\_OV\_F.

**Figure 13. Behavior on battery over voltage**


(1) Digital comparator in ACTIVE – Full-Power & REC-1, programmable threshold.

Undervoltage cases are critical for the regulators (Bucks, LDOs...) that are directly supplied. These are managed according to configured thresholds (through  $V_{FBB\_UV\_F}$  threshold) which trigger a power-down sequence in any case. Undervoltage can be triggered based on FBB early warning thresholds. If  $FBB\_UV\_EW\_PD$  is set high, the power-down sequence is triggered at the threshold defined by the  $FBB\_UV\_EW\_TH[3:0]$  bits.

Power-up is initiated as long as the FBB voltage increases above the threshold  $V_{FBB\_OK\_Rx}$ .

### 3.2.2

#### Boost modes

It is possible to set two different boost modes for the SPSB100GS through U-NVM bits:

- Boost Cranking mode when U-NVM bit  $BOOST\_CRK\_ONLY = 1$ .
- Boost Normal mode when U-NVM bit  $BOOST\_CRK\_ONLY = 0$ .

For both modes, the following points apply:

- Flexibility on boost regulation level ( $V_{FBB\_REGx}$ ) can be set in the  $FBB\_REG\_LEVEL\_SEL[1:0]$  bit.
- Flexibility on comparator thresholds  $V_{TH\_BYPASS\_Rx}$  to enable and  $V_{TH\_BYPASS\_Fx}$  to disable the external bypass MOSFET can be set in the  $BYPASS\_OFFSET\_SEL$  and  $FBB\_REG\_LEVEL\_SEL[1:0]$  bits.
- Flexibility on FBB level ( $V_{FBB\_OK\_Rx}$ ) to execute the power-up sequence can be set in the  $FBB\_OK\_SEL[1:0]$  bits.
- Flexibility on FBB level ( $V_{FBB\_UV\_Rx}$ ) to start the boost can be set in the  $FBB\_UV\_LEVEL\_SEL$  bit.
- A programmable timer  $t_{boost\_crk\_tox}$  to disable the boost when  $V_S < V_{S\_SENSEx}$  can be set in the  $BOOST\_CRK\_TO[2:0]$  bits.
  - The timer can be disabled if  $BOOST\_CRK\_TO = '000'$ .
  - When the timer expires, the flag  $BOOST\_TIMER\_CNT\_END$  is set and generates an IRQ unless the  $MASK\_BOOST\_TIMER\_CNT\_END\_IRQ$  is set.
  - The bit  $BOOST\_CNT\_END$  can be used to stop the timer when it is running by setting this bit to 1. To relaunch the timer, a transition from 1 to 0 for the bit  $BOOST\_CNT\_END$  is required.

#### 3.2.2.1

##### Boost Cranking mode

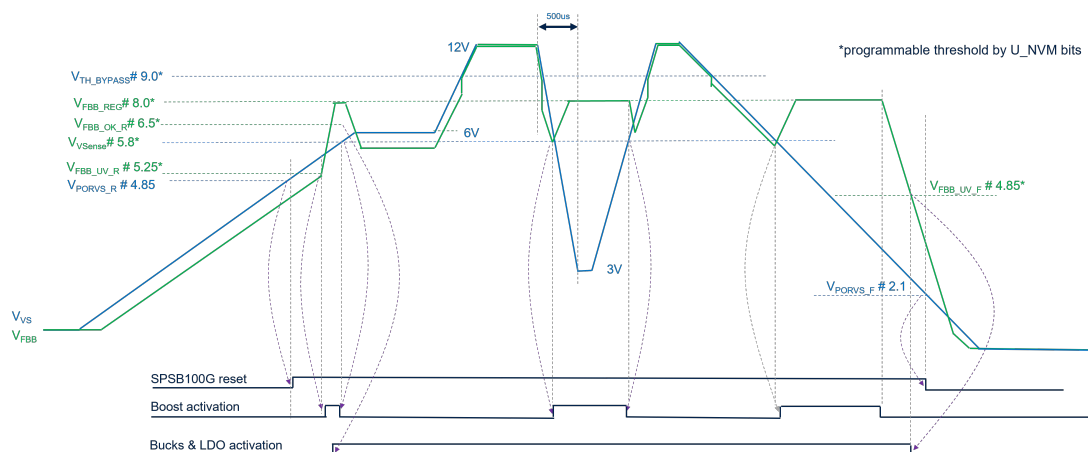
To activate the Boost Cranking mode, it is required to set it via the U-NVM bit  $BOOST\_CRK\_ONLY$  at "1".

This mode allows SPSB100GS to work as follows:

- Boost active for  $V_S < V_{S\_SENSEx}$  (managing potential cranking condition)
- Boost inactive for  $V_S \geq V_{S\_SENSEx}$

Where  $V_{SENSE}$  is a monitoring comparator that permits enabling/disabling boost, and is programmable in the U\_NVM bit  $VS\_SENSE\_LEVEL\_SEL[1:0]$  from 5.4 V to 5.85 V, with four steps of 150 mV.

**Figure 14. Boost Cranking mode**



**Note:** Buck1,2 output current capabilities are linked to input voltage applied. Please refer to current limitations curves reported in [Section 7.9: BUCK2 converter](#).

### 3.2.2.2 Boost Normal mode

To activate Boost normal mode, it is required to set it via the U-NVM bit  $BOOST\_CRK\_ONLY = 0$ .

**Figure 15. Boost Normal mode**

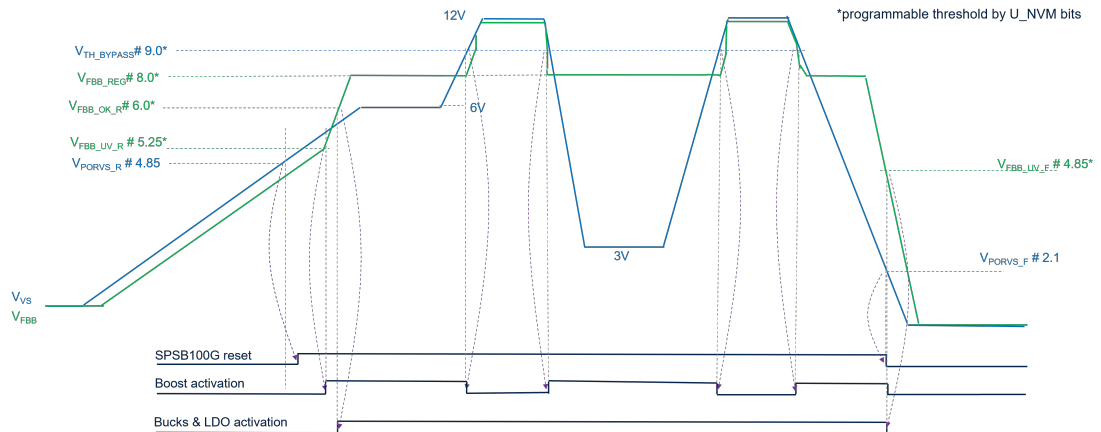
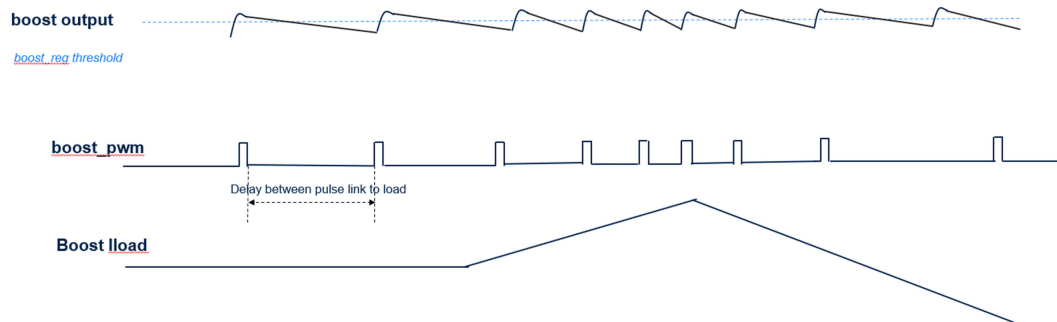


**Figure 16. Boost Normal mode - pulses with high/medium load**



### 3.3 Buck converters

#### 3.3.1 Buck1 converter

The Buck1 regulator is a synchronous converter compatible with battery level, with integrated power MOS. Stability compensation network is external.

Output voltages are programmable via the USER -NVM through the bit BUCK1\_PU\_VALUE.

The switching frequency can be selected either at 400 kHz or 2.4 MHz, by USER-NVM bit BUCK1\_FREQ. To limit emission in the audio bandwidth, refresh frequency can be forced at 25 kHz by USER-NVM bit BUCK1\_REFRESH\_FREQ set low (1 kHz when high). The drawback to this will be additional consumption in low-power mode.

The spread-spectrum feature is configurable via the SPI bit BUCK1\_SPREAD\_ENA (disabled by default).

Buck1 integrates a low-power mode (automatically set by LOW\_POWER\_SET in the SPI) which optimizes its efficiency in active low-power mode (Buck1 is a mandatory regulator in active low-power mode).

Buck1 can be disabled/enabled in active full power via the SPI bit VBUCK1\_ENA (only after SPI\_PROTECT\_ACCESS has been set). In active low-power mode, enabling Buck1 is not allowed.

The live bit VBUCK1\_ENA\_STATUS reflects the state of Buck1 output.

Note that after the first power-up, the control bit VBUCK1\_ENA needs to be aligned with live bit VBUCK1\_ENA\_STATUS.

In active full-power, the Buck1 converter provides the following diagnostics:

- UV detection to monitor the output voltage (flag is BUCK1\_UV). Buck1 is therefore switched off after tbuck1\_UV\_TO, except if SPI bit MASK\_BUCK1\_UV\_POWER\_OFF is set
- Undervoltage detection generates an IRQ, except if MASK\_BUCK1\_IRQ is set
- OV detection to monitor the output voltage (flag is BUCK1\_OV bit). Buck1 is therefore switched off after tbuck1\_OV\_TO. The status register bit BUCK1\_OV must be read and cleared before switching ON the regulator via the SPI bit VBUCK1\_ENA to allow a proper start-up (only when Buck1 is not critical for the MCU).
- Overvoltage detection generates an IRQ, except if MASK\_BUCK1\_IRQ is set.
- Power-good detection is used to signal Buck power-on success (flag is BUCK1\_PG\_OK bit) and IRQ is generated except if MASK\_BUCK1\_PG\_IRQ is set.
- If not, after TBUCK1\_PG\_TO timeout, Buck1 is switched off and the flag BUCK1\_PG\_TIMEOUT is set.
- Unsuccessful power-good detection generates an IRQ except if MASK\_BUCK1\_PG\_TIMEOUT\_IRQ is set.
- Configurable overcurrent protection through U-NVM BUCK1\_IPEAK (flag is BUCK1\_OC bit). Buck1 is therefore switched off after a time of tbuck1\_OC\_TO except if MASK\_BUCK1\_OC\_POWER\_OFF is set.
- Overcurrent detection generates an IRQ except if MASK\_BUCK1\_OC\_IRQ is set.
- Warning temperature detection by a local thermal sensor (flag is TW\_CL1).
- Warning temperature detection generates an IRQ except if MASK\_CL1\_TW\_IRQ is set.
- Overtemperature detection by a local thermal sensor (flag is TSD\_CL1, see also [Section 4.7](#)) and buck1 is switched off.
- Buck1 internal regulators detection (flag is BUCK1\_INT\_FAIL) and Buck1 is switched off.
- Internal fail generates an IRQ except if MASK\_BUCK1\_IRQ is set.
- After a fault detection (UV, OV, OC, FBLOSS, TSD\_CL1 or PG timeout), Buck1 can be re-enabled by setting BUCK1\_ENA = 0, followed by BUCK1\_ENA=1.
- Buck1 feedback (FB1) pin disconnection (flag is BUCK1\_FBLOSS). Buck1 is switched off.
- FB1 pin disconnection generates an IRQ except if MASK\_BUCK1\_IRQ is set.

In active low- power, the Buck1 converter provides the following diagnostics:

- UV detection to monitor the output voltage (flag is BUCK1\_UV). Buck1 is therefore switched off except if SPI bit MASK\_BUCK1\_UV\_POWER\_OFF is set.
- Undervoltage detection generates an IRQ except if MASK\_BUCK1\_IRQ is set.
- OV detection to monitor the output voltage (flag is BUCK1\_OV bit). Buck1 is therefore switched off.
- Overvoltage detection generates an IRQ except if MASK\_BUCK1\_IRQ is set.
- Overcurrent protection (flag is BUCK1\_OC bit). Buck1 is therefore switched off except if MASK\_BUCK1\_OC\_POWER\_OFF is set.
- Overcurrent detection generates an IRQ except if MASK\_BUCK1\_OC\_IRQ is set.
- Buck1 feedback (FB1) pin disconnection (flag is BUCK1\_UV). Buck1 is switched off.
- FB1 pin disconnection generates an IRQ except if MASK\_BUCK1\_IRQ is set.
- Overtemperature detection by the central thermal sensor (flag is TSD\_CL0, see also [Section 4.7](#)) and device power-down sequence is executed.

In ACTIVE and REC-1 states, when BUCK1\_REGFAIL\_GO\_REC is set at 1 in the USER-NVM, in case of PG timeout, OV, UV, INT\_FAIL, OC, FBLOSS, or TSD events, the device executes a power-down sequence, enters REC-2 state and makes an automatic retry. PG\_TIMEOUT, OV, UV, OC, INT\_FAIL, FBLOSS or TSD flags are not blocking a re-enable of the BUCK1.

According to a suitably configured output voltage, it can also be used to supply another buck. It is not recommended to use MASK\_BUCK1\_OC\_POWER\_OFF and MASK\_BUCK1\_UV\_POWER\_OFF at the same time.

### 3.3.2

#### Buck2 converter

The Buck2 converter is the same as the Buck1.

The Buck2 regulator is a synchronous converter compatible with battery level, with an integrated power MOS. Stability compensation network is external.

Output voltages are programmable via the USER -NVM through the bit BUCK2\_PU\_VALUE.

The switching frequency can be selected either at 400 kHz or 2.4 MHz, by USER-NVM BUCK2\_FREQ. To limit emission in the audio bandwidth, refresh frequency can be forced at 25 kHz by USER-NVM bit BUCK2\_REFRESH\_FREQ set low (1 kHz when high). The drawback to this will be additional consumption in low-power mode.

The spread-spectrum feature is configurable via the SPI bit BUCK2\_SPREAD\_ENA (disabled by default).

Buck2 integrates a low-power mode (automatically set by LOW\_POWER\_SET in the SPI) which optimize its efficiency in active low-power mode. (Buck2 can be optionally enabled in active low-power mode).

Buck2 can be disabled via the SPI bit VBUCK2\_ENA. (only after SPI\_PROTECT\_ACCESS has been set). In active low-power mode, enabling Buck2 is not allowed.

The live bit VBUCK2\_ENA\_STATUS reflects the state of Buck2 output.

Note that after the first power-up, the control bit VBUCK2\_ENA needs to be aligned with live bit VBUCK2\_ENA\_STATUS.

In active full-power, the Buck2 converter provides the following diagnostics:

- UV detection to monitor the output voltage (flag is BUCK2\_UV). Buck2 is therefore switched off after tbuck2\_UV\_TO except if SPI bit MASK\_BUCK2\_UV\_POWER\_OFF is set.
- Undervoltage detection generates an IRQ except if MASK\_BUCK2\_IRQ is set.
- OV detection to monitor the output voltage (flag is BUCK2\_OV bit). Buck2 is therefore switched off after tbuck2\_OV\_TO. Status register bit BUCK2\_OV must be read and cleared before switching ON the regulator via the SPI bit VBUCK2\_ENA to allow a proper start-up (only when Buck2 is not critical for the MCU).
- Overvoltage detection generates an IRQ except if MASK\_BUCK2\_IRQ is set.
- Power-good detection is used to signal Buck power-on success (flag is BUCK2\_PG\_OK bit) and IRQ is generated except if MASK\_BUCK2\_PG\_IRQ is set.
- If not, after TBUCK2\_PG\_TO timeout, Buck2 is switched off and the flag BUCK2\_PG\_TIMEOUT is set.
- Unsuccessful power-good detection generates an IRQ except if MASK\_BUCK2\_PG\_TIMEOUT\_IRQ is set.
- Configurable overcurrent protection through U-NVM BUCK2\_IPEAK (flag is BUCK2\_OC bit). Buck2 is therefore switched off after tbuck2\_OC\_TO except if MASK\_BUCK2\_OC\_POWER\_OFF is set.
- Overcurrent detection generates an IRQ except if MASK\_BUCK2\_OC\_IRQ is set.
- Warning temperature detection by a local thermal sensor (flag is TW\_CL2).
- Warning temperature detection generates an IRQ except if MASK\_CL2\_TW\_IRQ is set.
- Overtemperature detection by local thermal sensor (flag is TSD\_CL2, see also [Section 4.7](#)) and buck2 is switched off.
- Buck2 internal regulators detection (flag is BUCK2\_INT\_FAIL). Buck2 is switched off.
- Internal fail generates an IRQ except if MASK\_BUCK2\_IRQ is set.
- Buck2 feedback (FB2) pin disconnection (flag is BUCK2\_FBLOSS). Buck2 is switched off.
- FB2 pin disconnection generates an IRQ except if MASK\_BUCK2\_IRQ is set.
- After a fault detection (UV, OV, OC, FBLOSS, TSD\_CL2 or PG timeout), Buck2 can be re-enabled by setting BUCK2\_ENA = 0, followed by BUCK2\_ENA=1.

In active low-power, the Buck2 converter provides the following diagnostics:

- UV detection to monitor the output voltage (flag is BUCK2\_UV). Buck2 is therefore switched off except if SPI bit MASK\_BUCK2\_UV\_POWER\_OFF is set.
- Undervoltage detection generates an IRQ except if MASK\_BUCK2\_IRQ is set.
- OV detection to monitor the output voltage (flag is BUCK2\_OV bit) Buck2 is therefore switched off.
- Overvoltage detection generates an IRQ except if MASK\_BUCK2\_IRQ is set.
- Overcurrent protection (flag is BUCK2\_OC bit). Buck2 is therefore switched off except if MASK\_BUCK2\_OC\_POWER\_OFF is set.
- Overcurrent detection generates an IRQ except if MASK\_BUCK2\_OC\_IRQ is set.
- Buck2 feedback (FB2) pin disconnection (flag is BUCK2\_UV). Buck2 is switched off.
- FB2 pin disconnection generates an IRQ except if MASK\_BUCK2\_IRQ is set.
- Overtemperature detection by the central thermal sensor (flag is TSD\_CL0, see also [Section 4.7](#)) and device power-down sequence is executed.

In ACTIVE and REC-1 states, when BUCK2\_REGFAIL\_GO\_REC is set at 1 in the USER-NVM, in case of PG timeout, OV, UV, INT\_FAIL, OC, FBLOSS or TSD events, the device executes a power-down sequence, enters REC-2 state and makes an automatic retry. PG\_TIMEOUT, OV, UV, OC, INT\_FAIL, FBLOSS or TSD flags are not blocking a re-enable of the BUCK2.

It is not recommended to use MASK\_BUCK2\_OC\_POWER\_OFF and MASK\_BUCK2\_UV\_POWER\_OFF at the same time.

### 3.3.3

#### Buck3 converter

The Buck3 is a post-regulator and needs to be supplied by Buck1 or Buck2 through the VIN3 pin.

The Buck3 converter is similar to the Buck1 but with double current capability. Fine-tuning in steps of 10 mV is available by SPI (BUCK3\_FTUNE[2:0] control bits), covering a range from 0.99 V to 1.05 V.

Output voltage is usable via the USER-NVM bit BUCK3\_PU\_VALUE = 1.

The spread-spectrum feature is configurable via the SPI bit BUCK3\_SPREAD\_ENA (disabled by default).

To limit emission in the audio bandwidth, refresh frequency can be forced at 25 kHz by USER-NVM bit BUCK3\_REFRESH\_FREQ set low (1 kHz when high).

Buck3 can be disabled via the SPI bit VBUCK3\_ENA (only after SPI\_PROTECT\_ACCESS has been set). Buck3 must be disabled before entering active low-power mode and must not be enabled in this mode.

The live bit VBUCK3\_ENA\_STATUS reflects the state of BUCK3 output.

Note that after the first power-up, the control bit VBUCK3\_ENA needs to be aligned with live bit VBUCK3\_ENA\_STATUS.

The Buck3 converter provides the following diagnostics:

- UV detection to monitor the output voltage (flag is BUCK3\_UV). Buck3 is therefore switched off after tbuck3\_UV\_TO except if SPI bit MASK\_BUCK3\_UV\_POWER\_OFF is set
- Undervoltage detection generates an IRQ except if MASK\_BUCK3\_IRQ is set
- OV detection to monitor the output voltage (flag is BUCK3\_OV bit). Buck3 is therefore switched off after tbuck3\_OV\_TO. Status register bit BUCK3\_OV must be read and cleared before switching ON the regulator via the SPI bit VBUCK3\_ENA to allow a proper start-up (only when Buck3 is not critical for the MCU).
- Overvoltage detection generates an IRQ except if MASK\_BUCK3\_IRQ is set.
- Power-good detection is used to signal Buck power-on success (flag is BUCK3\_PG\_OK bit) and IRQ is generated except if MASK\_BUCK3\_PG\_IRQ is set.
- If not, after TBUCK3\_PG\_TO timeout, Buck3 is switched off and the flag BUCK3\_PG\_TIMEOUT is set.
- Unsuccessful power-good detection generates an IRQ except if MASK\_BUCK3\_PG\_TIMEOUT\_IRQ is set.
- Configurable overcurrent protection through U-NVM BUCK3\_IPEAK (flag is BUCK3\_OC bit). Buck3 is therefore switched off after tbuck3\_OC\_TO except if MASK\_BUCK3\_OC\_POWER\_OFF is set.
- Overcurrent detection generates an IRQ except if MASK\_BUCK3\_OC\_IRQ.
- Warning temperature detection by a local thermal sensor(flag is TW\_CL3).
- Warning temperature detection generates an IRQ except if MASK\_CL3\_TW\_IRQ is set.
- Overtemperature detection by a local thermal sensor (flag is TSD\_CL3, see also [Section 4.7](#)) and Buck3 is switched off.
- Buck3 internal regulators detection (flag is BUCK3\_INT\_FAIL). Buck3 is switched off.
- Internal fail generates an IRQ except if MASK\_BUCK3\_IRQ is set.
- After a fault detection (UV, OV, OC, INT\_FAIL, TSD\_CL3 or PG timeout), Buck3 can be re-enabled by setting BUCK3\_ENA = 0, followed by BUCK3\_ENA=1.
- In ACTIVE and REC-1 states, when BUCK3\_REGFAIL\_GO\_REC is set at 1 in the USER-NVM, in case of PG timeout, OV, UV, OC, INT\_FAIL or TSD events, the device executes a power-down sequence, enters REC-2 state and makes an automatic retry. PG\_TIMEOUT, OV, UV, OC, INT\_FAIL or TSD flags are not blocking a re-enable of the BUCK3.

It is not recommended to use MASK\_BUCK3\_OC\_POWER\_OFF and MASK\_BUCK3\_UV\_POWER\_OFF at the same time.

## 3.4 Linear voltage regulators

### 3.4.1 LDO1

The LDO1 is dedicated to supplying the CAN-FD in ACTIVE state or to supplying external loads (only for the SPSB100GBS). It is supplied by the FBB pin. LDO1 has a 5 V output and a 120 mA current capability. It can be enabled/disabled through the LDO1\_ENA control bit (only after SPI\_PROTECT\_ACCESS has been set). The voltage regulator is protected against undervoltage (flag is LDO1\_UV) and LDO1 is therefore switched off. The undervoltage detection generates an IRQ except if it is masked with MASK\_LDO1\_IRQ. The live bit LDO1\_ENA\_STATUS reflects the state of LDO1 output.

**Note:** *Note that, after the first-power up, it is necessary the control bit LDO1\_ENA needs to be aligned with live bit LDO1\_ENA\_STATUS.*

- Power-good is used to signal LDO1 power-on success (flag is LDO1\_PG\_OK bit).
- If not, after T<sub>LDO1\_PG\_TO</sub> timeout, LDO1 is switched off and flag LDO1\_PG\_TIMEOUT is set.
- Power-on success generates an IRQ except if it is masked with MASK\_LDO1\_PG\_IRQ.
- Unsuccessful power-good detection generates an IRQ except if MASK\_LDO1\_PG\_TIMEOUT\_IRQ is set.
- After a fault detection (UV or PG timeout), LDO1 can be re-enabled by setting LDO1\_ENA = 0, followed by LDO1\_ENA=1, Fail flags are not blocking to re-enable the LDO1.

The output voltage is stable for ceramic load capacitors C<sub>LDO1</sub> > 1 µF.

Warning temperature detection by a local thermal sensor (flag is TW\_CL0).

Warning temperature detection generates an IRQ except if MASK\_CL0\_TW\_IRQ is set.

In case the device temperature exceeds the TSD\_CL0 threshold, the device executes a power-down sequence before entering REC-2 state.

### 3.4.2 LDO2

The SPSB100GS embeds one low-dropout tracking regulator designed to provide an output voltage that closely tracks the bucks' reference at +/-10 mV while delivering up to 10 mA on the LDO2 output pin. The LDO2 voltage tracker is supplied by the FBB pin.

The LDO2\_ENA SPI bit is used to enable/disable this LDO (only after SPI\_PROTECT\_ACCESS has been set). LDO2 must be disabled before entering ACTIVE low-power mode, and must not be enabled in this mode.

LDO2 can be configured by means of the USER-NVM LDO2\_TRK bits to track one of Buck1, Buck2 or Buck3, if related output voltages are 5 V or 3.3 V (see Table 6).

**Table 6. Voltage regulators configuration**

| Tracking configuration | LDO2_TRK[0,1] USER-NVM configuration bits | Selected voltage source | Source output voltage | LDO2 behavior          |
|------------------------|-------------------------------------------|-------------------------|-----------------------|------------------------|
| 1                      | 00                                        | Buck1                   | 3.3 V or 5 V          | Tracks Buck1           |
|                        |                                           |                         | 6.5 V                 | OFF what ever LDO2_ENA |
| 2                      | 01                                        | Buck2                   | 3.3 V or 5 V          | Tracks Buck2           |
|                        |                                           |                         | 6.5 V                 | OFF what ever LDO2_ENA |
| 3                      | 1x                                        | Buck3                   | 1.02 V                | OFF what ever LDO2_ENA |
|                        |                                           |                         | 3.3 V                 | Tracks Buck3           |

LDO2 is supplied by the FBB pin.

The tracking regulator provides the following diagnostics:

- The live bit LDO2\_ENA\_STATUS reflects the state of LDO2 output.

**Note:** *Note that, after the first-power up, it is necessary the control bit LDO2\_ENA needs to be aligned with live bit LDO2\_ENA\_STATUS.*

- Overvoltage detection to monitor the output voltage (flag is LDO2\_OV bit) and LDO2 is therefore switched off.
- Overvoltage detection generates an IRQ except if MASK\_LDO2\_IRQ is set.
- Undervoltage detection (flag is LDO2\_UV bit) and LDO2 is therefore switched off.
- Undervoltage detection generates an IRQ except if MASK\_LDO2\_IRQ is set.
- Power-good is used to signal LDO2 power-on success (flag is LDO2\_PG\_OK bit).
- If not, after  $T_{LDO2\_PG\_TO}$  timeout, LDO2 is switched off and flag LDO2\_PG\_TIMEOUT is set.
- The power-on success generates an IRQ, except if it is masked with MASK\_LDO2\_PG\_IRQ.
- Unsuccessful power-good detection generates an IRQ except if MASK\_LDO2\_PG\_TIMEOUT\_IRQ is set.
- Warning temperature detection by a local thermal sensor (flag is TW\_CL4).
- Warning temperature detection generates an IRQ except if MASK\_CL4\_TW\_IRQ is set.
- Overtemperature detection by a local thermal sensor (flag is TSD\_CL4, see also [Section 4.7](#)) and LDO2 is switched off.
- After a fault detection (UV, OV, TSD\_CL4 or PG timeout), LDO2 can be re-enabled by setting LDO2\_ENA = 0, followed by LDO2\_ENA=1, Fail flags are not blocking to re-enable the LDO2.
- LDO2 is switched off if a fault on the tracked regulator is detected.
- In active and REC-1 states, when LDO2\_REGFAIL\_GO\_REC is set at 1 in the USER-NVM, in case of PG timeout, OV, UV, or TSD events, the device executes a power-down sequence, enters REC-2 state, and makes an automatic retry.

### 3.5

## Operating modes

The device can work in a normal operation mode (ACTIVE state - FULL-POWER mode) or in a reduced operation mode (ACTIVE state - LOW-POWER mode).

The transition between FULL-POWER and LOW-POWER mode is managed via an SPI command (LOW\_POWER\_SET control bit, only after SPI\_PROTECT\_ACCESS has been set).

In ACTIVE state, the device is fully controllable and configurable through the SPI.

Moreover, a DEEP-SLEEP state is available in order to minimize current consumption during not-operating time frames via the SPI command DO\_POWER\_DOWN (only after SPI\_PROTECT\_ACCESS has been set). Status bits DEEP-SLEEP\_FROM\_DO\_POWER\_DOWN will be set at "01" if transitioning from ACTIVE state, or "1x" if transition from REC-1 state.

DEEP-SLEEP\_FROM\_DO\_POWER\_DOWN can be cleared via the CLR\_DEEP\_SLEEP\_FROM\_DO\_POWER\_DOWN bit.

The table below shows the availability and operational behavior of regulators and functions across different operating modes. In some modes, a regulator can be actively turned ON or OFF, allowing dynamic control. In other modes, the regulator remains permanently OFF and cannot be enabled.

**Table 7. Regulators and functions availability by operating modes**

| Regulators                | FULL-POWER            | LOW-POWER             | DEEP-SLEEP            |
|---------------------------|-----------------------|-----------------------|-----------------------|
| BOOST                     | ON/OFF <sup>(1)</sup> | ON/OFF <sup>(1)</sup> | OFF                   |
| Buck 1                    | ON/OFF <sup>(2)</sup> | ON/OFF <sup>(3)</sup> | OFF                   |
| Buck 2                    | ON/OFF <sup>(2)</sup> | ON/OFF <sup>(3)</sup> | OFF                   |
| Buck 3                    | ON/OFF <sup>(2)</sup> | OFF                   | OFF                   |
| LDO 1                     | ON/OFF <sup>(2)</sup> | ON/OFF <sup>(3)</sup> | OFF                   |
| LDO 2                     | ON/OFF <sup>(2)</sup> | OFF                   | OFF                   |
| <b>Wake up mechanisms</b> | <b>FULL-POWER</b>     | <b>LOW-POWER</b>      | <b>DEEP-SLEEP</b>     |
| WU, IGN                   | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> |
| LDT                       | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> |
| CAN                       | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> |
| OUT_HS cyclic             | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> |
| <b>Others</b>             | <b>FULL-POWER</b>     | <b>LOW-POWER</b>      | <b>DEEP-SLEEP</b>     |
| NFSO                      | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> | OFF <sup>(4)</sup>    |
| NRST                      | ON                    | ON                    | OFF                   |
| IRQ                       | ON                    | ON                    | OFF                   |
| FCCU                      | ON/OFF <sup>(3)</sup> | OFF                   | OFF                   |
| CAN FD                    | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> | OFF                   |
| OUT_HS                    | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> | ON/OFF <sup>(3)</sup> |
| ADC                       | ON                    | OFF                   | OFF                   |
| TSDC                      | ON                    | ON                    | OFF                   |
| TSD                       | ON                    | OFF                   | OFF                   |
| SPI                       | ON                    | ON                    | ON/OFF                |
| Watchdog                  | ON/OFF <sup>(5)</sup> | ON/OFF <sup>(3)</sup> | OFF                   |
| BYPASS                    | ON/OFF <sup>(1)</sup> | OFF                   | OFF                   |

1. ON/OFF depends on battery voltage level. Can be set OFF by NVM/SPI.
2. ON if included in the Power-ON sequence by NVM or by SPI programming.
3. SPI programmable.
4. Can be set High or low by NVM.
5. ON/OFF by NVM.

### 3.5.1 Wake-up from DEEP-SLEEP to ACTIVE state

A wake-up from DEEP-SLEEP state will transit the device to the INIT state, as described in [Section 3.6.3](#)

To avoid disabling all wake-up capability, a hard protection is implemented: the SPI writing to disable the last wake-up possibility defined in [Table 8](#) is not taken into account and a status register bit SPI\_ALL\_WAKEUP\_DISABLE is set, and generates an IRQ except if MASK\_SPI\_ERROR\_IRQ is set.

Current consumption in DEEP-SLEEP mode is calculated as  $I_{VS\_DP}$  + wake-up current consumption contributions.

This can be initiated by one or more of the following events:

### Table 8. Wake up events description

| Wake up source                | Description                                                       | Flag       |
|-------------------------------|-------------------------------------------------------------------|------------|
| CAN bus activity              | Can be configured by SPI (CAN_WU_ENA bit)                         | CAN_WAKE   |
| Level change of wake-up (WU)  | Can be configured by SPI (WU_ENA bit)                             | WU_WAKE    |
| Level change of wake-up (IGN) | Can be configured by SPI (IGN_ENA bit)                            | IGN_WAKE   |
| Cyclic monitoring (WU)        | Can be configured by SPI (WU_FILT bit with<br>TIMER_ENA=1)        | WU_WAKE    |
| Cyclic monitoring (IGN)       | Can be configured by SPI (IGN_FILT bit with<br>TIMER_ENA=1)       | IGN_WAKE   |
| Timer                         | Can be configured by SPI (TIMER_WAKE_ENA bit with<br>TIMER_ENA=1) | TIMER_WAKE |
| Long duration timer           | Can be configured by SPI (LDT_MODE bit with<br>LDT_ENA=1)         | LDT_WAKE   |

### 3.5.2 Wake-up events in ACTIVE mode

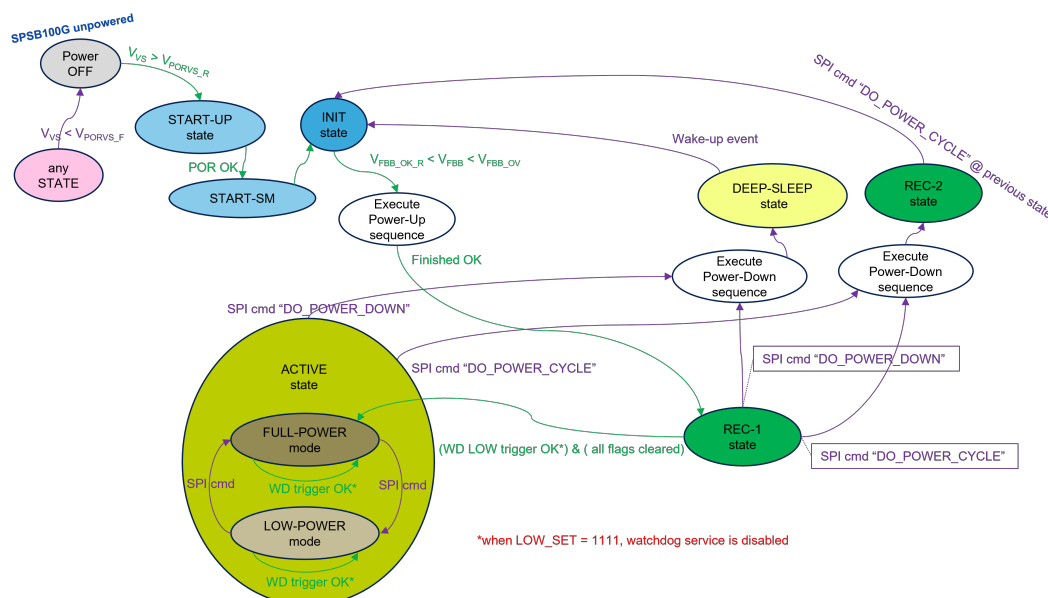
All enabled wake-up events described in [Table 8](#) in ACTIVE mode are signaled to the microcontroller by an interrupt request on the IRQ pin.

### 3.6 Functional overview - state machine

To make the reading easier, the state machine description has been split into three parts. First, the state diagram is presented with the normal transitions (Section 3.6.1), then transitions resulting in a fault event detection are shown (Section 3.6.2), and finally the full state machine is described and states and transitions detailed (Section 3.6.3).

### 3.6.1 State machine without fault transitions

**Figure 17. State machine without fault transitions**



Until the voltage on the VS pin reaches  $V_{PORVS\_R}$  for the first time, the device is in POWER-OFF state. After that, the device transitions to the START-UP state, where internal power supplies are established. Then, a core logic reset is released and the START-SM state is reached, where oscillators start and the NVM is read and checked. Refer to Chapter [Section 3.8](#) for details on the USER-NVM space programming.

After start-up completion, the device reaches the INIT state, where a digital BIST is ran, and when the FBB voltage reaches  $V_{FBB\_OK\_R}$ , the device executes a power-up sequence, which turns ON all regulators as per application requirements stored in the USER-NVM space. The sequence includes the NRST pin deassertion to high level and, at the same time, the start of the watchdog long open window. See the power-up sequence description in [Section 3.7.1](#) for details. After the power-up sequence, the device enters the REC-1 state: The SPSB100GS is waiting for the MCU to boot up and triggers the watchdog, except if  $LOW\_SET[3:0] = 1111$ , before expiration of the watchdog long open window timeout. After a valid trigger of the watchdog during its long open window timeout, the device enters ACTIVE state in FULL-POWER mode. In the ACTIVE state, the device is fully controllable by SPI. The MCU can configure SPSB100GS features as per application needs to optimize ECU performances and global power consumption. In particular, some regulators can be switched OFF by SPI and the SPSB100GS can be set to LOW-POWER mode, to reduce ECU power consumption while delivering the strict minimum power supply and supervision to the MCU. Later, the MCU can reconfigure the SPSB100GS in FULL-POWER mode by SPI.

In ACTIVE state, the MCU can also request a power cycle from the SPSB100GS: a power-down sequence is then executed, followed by digital BIST in INIT state, before executing a power-up sequence. In ACTIVE state, the MCU can also request a power-down from the SPSB100GS: a power-down sequence is then executed, and DEEP-SLEEP state is reached. It is left upon a wake-up event. Wake-up event sensitivity is programmable by SPI in ACTIVE state, and includes cyclic sensing of the WU pin with cyclic powering of OUT\_HS, edge and level detection on IGN, and CAN wake-up frame detection.

## 3.6.2 State machine focusing on fault transitions

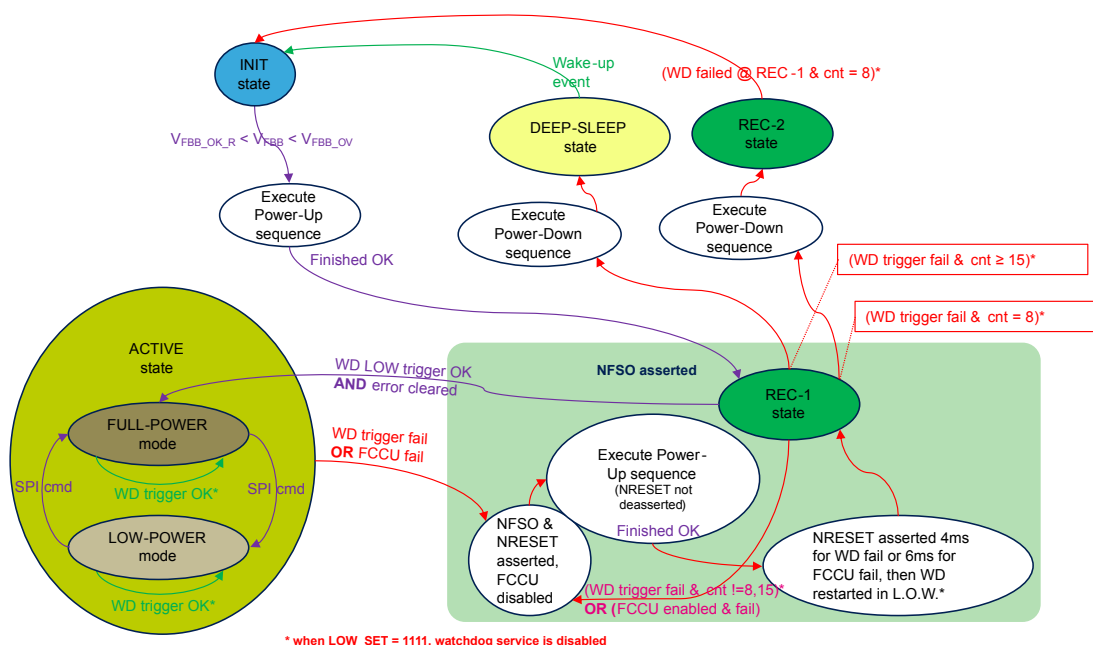
### 3.6.2.1 NVM fault management

NVM fault management is explained in [Section 3.8.1](#).

### 3.6.2.2 Watchdog triggering and FCCU monitor fault management

The watchdog is launched during the power-up sequence when the NRST pin is deasserted high, starting with a long open window timeout. After the power-up sequence, the SPSB100GS reaches REC-1 state, which is dedicated to watchdog and FCCU monitor fault management.

**Figure 18. State machine details with watchdog and FCCU monitor fault management**



While in REC-1 state, a read and clear of error flags and a proper triggering of the watchdog in long open window timeout initiates a transition to ACTIVE state.

If the watchdog is triggered without clearing all flags, then the device remains in REC-1 state and the watchdog has to be triggered within the default window.

In ACTIVE state, the watchdog runs with normal window timings. Proper trigger of the watchdog maintains the SPSB100GS in ACTIVE state, while a failure in the watchdog service or a fault detected on the FCCU monitor will:

- increment the watchdog fault counter (only due to watchdog fail)
- assert NRST pin low
- disable and reset the FCCU monitor
- initiate a power-up sequence: This is mandatory to power regulators that may have been switched off SPI.
- disable the BYPASS external MOSFET

Then, the NRST pin remains asserted for  $t_{NRST\_WDR}$  (in case of watchdog trigger fault), or  $t_{NRST\_FCCU}$  (in case of FCCU monitor fault). Before being released, the watchdog starts a long open window and the SPSB100GS reaches REC-1 state.

In case of successive faults in servicing the watchdog in long open window, the watchdog fault counter is incremented, a power-up sequence is run, a  $t_{NRST\_WDR}$  NRST pulse is generated, and a long open window is restarted.

If the watchdog is properly served during the long open window, then the watchdog fault counter is reset and the SPSB100GS enters ACTIVE state.

8 successive watchdog faults will force the SPSB100GS to initiate a power cycle through the REC-2 and INIT states. In case of 15 successive watchdog faults, the SPSB100GS enters DEEP-SLEEP state.

The FCCU monitor is disabled and its configuration reset after the first watchdog fault. The FCCU monitor can be reconfigured and enabled through SPI in REC-1 or ACTIVE state.

### 3.6.2.3

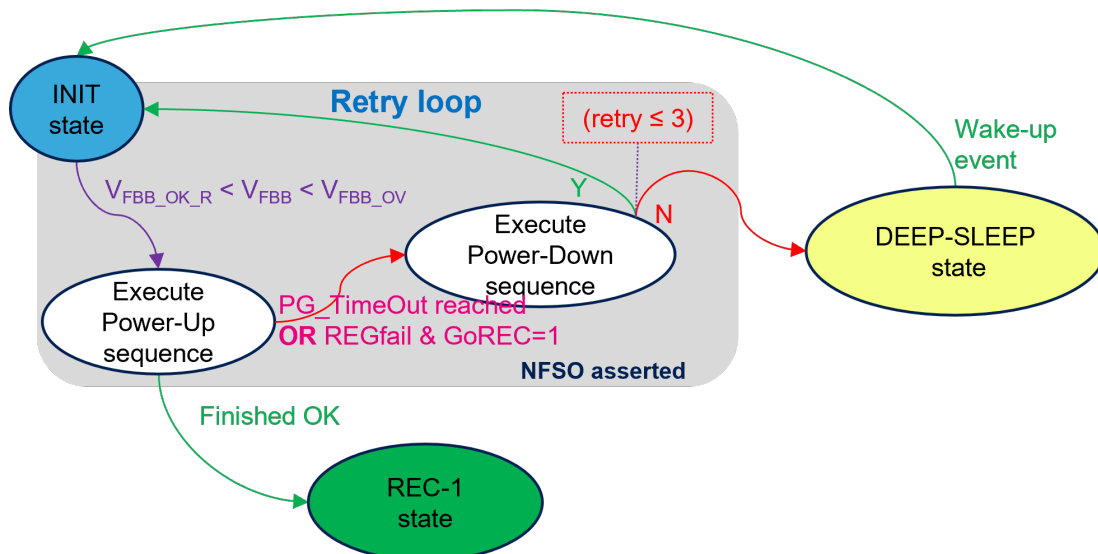
#### Power-up fault management

The power-up sequence can be programmed to wait for the power-good signal of any of the turned-on regulators (see the power-up sequence description in Section 3.7.1 for details). In such a case, a timeout counter is run. It is longer than the maximum rising time of the SPSB100GS regulators.

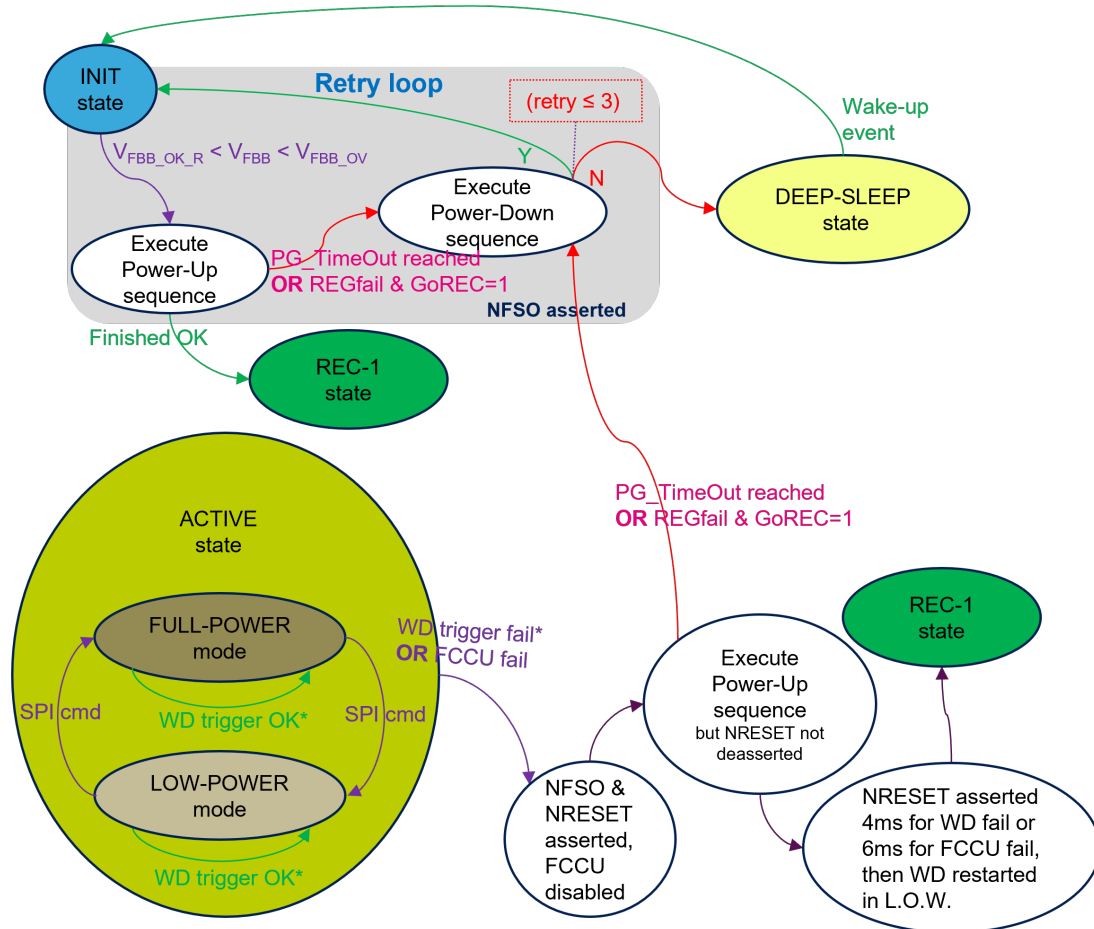
If the timeout elapses, the SPSB100GS executes a power-down sequence, the power-up retry counter POWUP\_RETRY\_CNT is incremented, and the SPSB100GS retries 4 times to power-up the regulators (POWUP\_RETRY\_CNT counter can be cleared by CLR\_POWUP\_RETRY\_COUNT bit). If 4 successive faults occur and the PU\_LOOP\_FOR\_EVER bit is not set, then the SPSB100GS enters DEEP-SLEEP state, clears the POWUP\_RETRY\_CNT and generates a status register flag FORCED\_SLEEP\_POWUP. If PU\_LOOP\_FOR\_EVER bit is set, the SPSB100GS will retry to power-up forever.

The same retry loop applies if a fault on a regulator is detected during the power-up sequence, and the regulator has its REGFAIL\_GO\_REC configuration bit set to 1. See Section 3.6.2.5 for details.

**Figure 19. State machine details on power-up fault (1)**



The behavior is similar if the power-up sequence timeout is reached when the sequence is executed after a watchdog fault or an FCCU monitor fault detection as shown in the following figure.

**Figure 20. State machine details on power-up fault (2)**


### 3.6.2.4

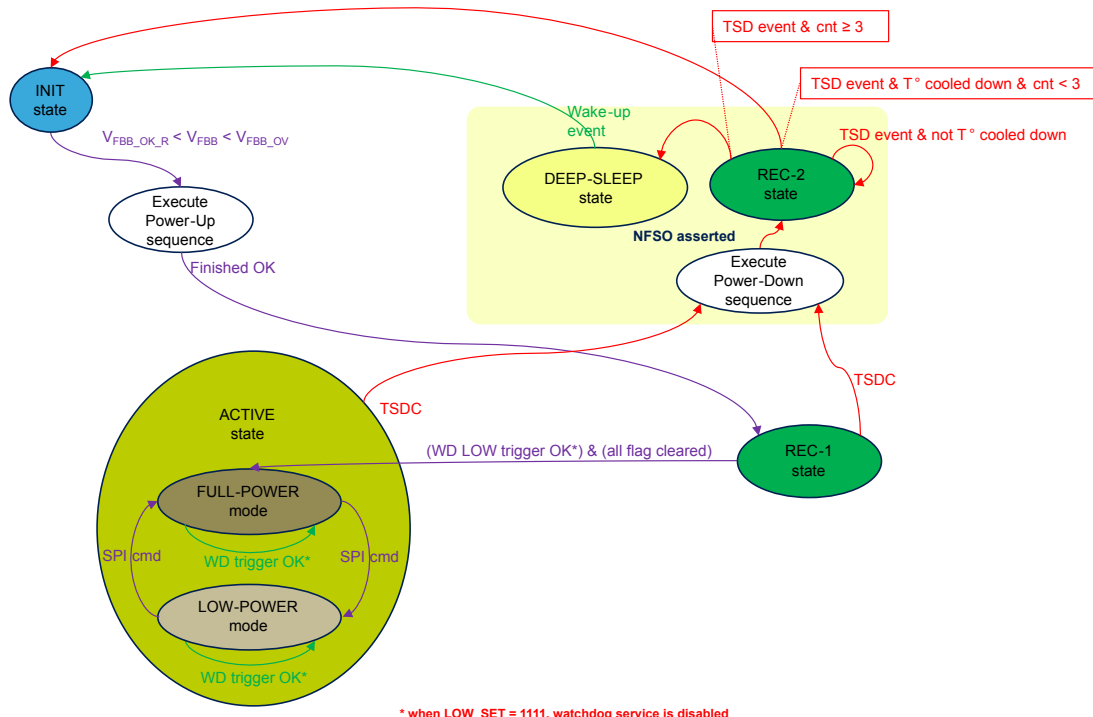
#### Central thermal sensor fault management

The central thermal sensor plays a major role in protecting the whole device. This sensor is monitoring the temperature of the SPSB100GS core. If the SPSB100GS core temperature exceeds the  $T_{SDC}$  threshold, a power-down sequence is run, and the SPSB100GS enters REC-2 state.

In REC-2 state, all regulators are OFF and the TSD event counter **TSD\_CNT\_FAIL** is incremented. After the temperature cools down, if **TSD\_CNT\_FAIL** is less than 3, then SPSB100GS transits to INIT state and initiates a power-up sequence. If not, then the SPSB100GS transits to DEEP-SLEEP state until a wake-up event and generates a status register flag **FORCED\_SLEEP\_TSD**.

The TSD event counter, **TSD\_CNT\_FAIL**, is readable via the SPI and can be cleared by **CLR\_TSD\_CNT\_FAIL** bit. This counter is incremented after a TSD event on any of the clusters.

### Figure 21. State machine details on TSDC fault



### 3.6.2.5

### Regulator fault management

Each SPSB100GS regulator has the following monitors:

- Temperature sensor with a warning threshold (TW) and a shut-down threshold (TSD)
- Undervoltage comparator (UV)
- Overvoltage comparator (OV) except for LDO1
- Power-good comparator (PG\_TIMEOUT)
- Overcurrent comparator (OC) on Bucks
- Internal regulator comparator (INT\_FAIL) on Bucks
- FB pin disconnection (FBLOSS for Buck1 and Buck2)

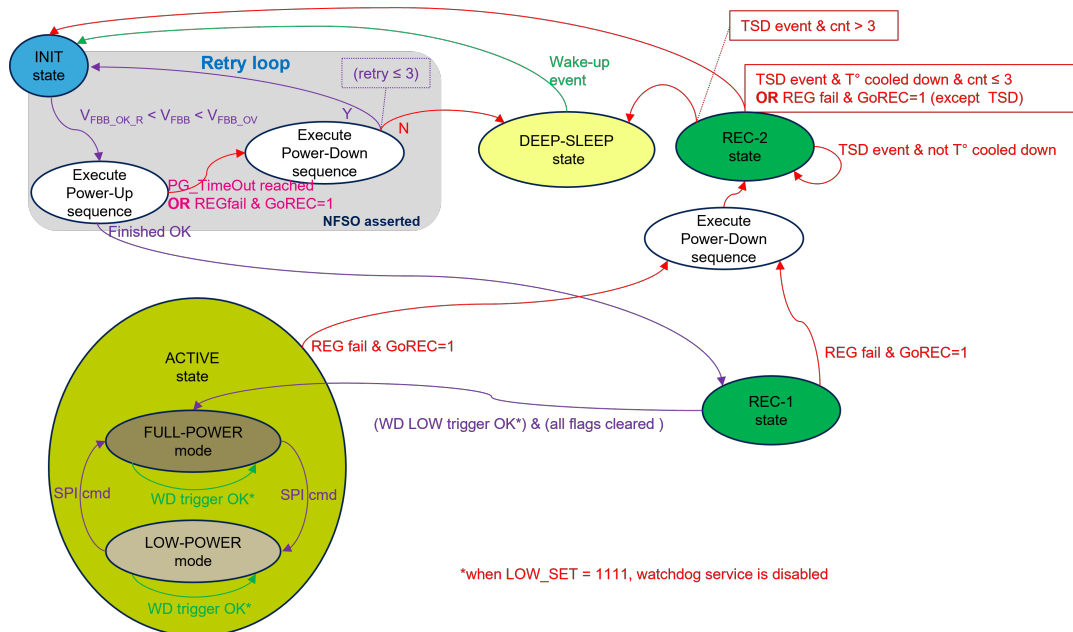
The user can decide how the SPSB100GS shall react on an event of those monitors. This is done through the USER-NVM bit REGFAIL\_GO\_REC for each of them.

A TW event sets the associated flag and generate an interruption, while the reaction to a TSD, UV, PG TIMEOUT, OC, INT\_FAIL, FBLOSS and OV event depends on the regulator REGFAIL\_GO\_REC bit.

When REGFAIL\_GO\_REC is set to '1', a fault detected on regulator TSD, UV, PG\_TIMEOUT, OC, INT\_FAIL, FBLOSS and OV monitors initiates a power-down sequence, then the state machine transitions to INIT state and runs a power-up sequence. If a fault is detected, then the retry sequence described in [Section 3.6.2.3](#) is executed. In case of TSD, the SPSB100GS reaction is the same as for a TSDC event described in [Section 3.6.2.4](#).

A fault event counter REG\_FAIL\_CNT is incremented when a power-down sequence is initiated by a regulator fault event. When the counter reaches 3, the SPSB100GS transitions to DEEP-SLEEP state, where the counter is reset and the SPI flag FORCED\_SLEEP\_REGFAIL is set. REG\_FAIL\_CNT is clearable by SPI bit CLR REG FAIL CNT.

Figure 22. Regulator fault reaction with REGFAIL\_GO\_REC = 1

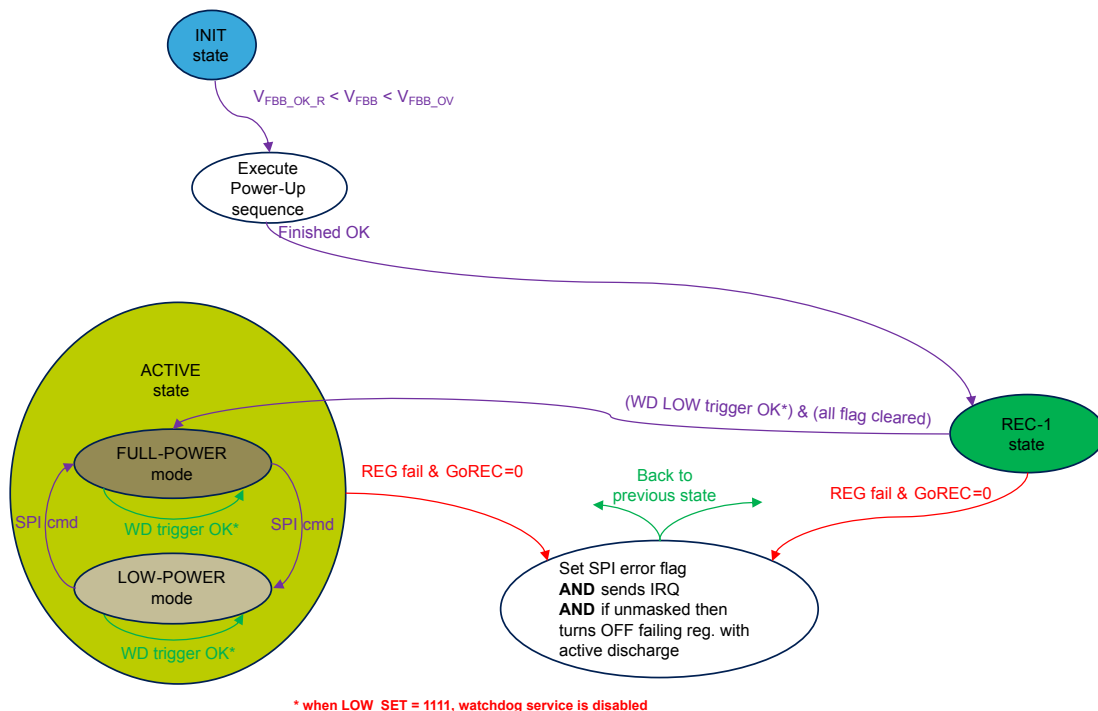


When REGFAIL\_GO\_REC is reset to '0', a fault detected on regulator, TSD, UV, OC, INT\_FAIL, FBLOSS and OV monitors will:

- Set the associated flag
- Send an interruption. The interruption can be masked for UV, OC, INT\_FAIL, FBLOSS and OV and TW, not for TSD.
- Switch the regulator OFF if the action is not masked. Action of UV and OC is maskable, while an INT\_FAIL, FBLOSS, OV and TSD event always switches the regulator OFF. TW event never switches the regulator OFF.

The state machine does not change its state if REGFAIL\_GO\_REC is reset to '0'.

Figure 23. Regulator fault reaction with REGFAIL\_GO\_REC = 0

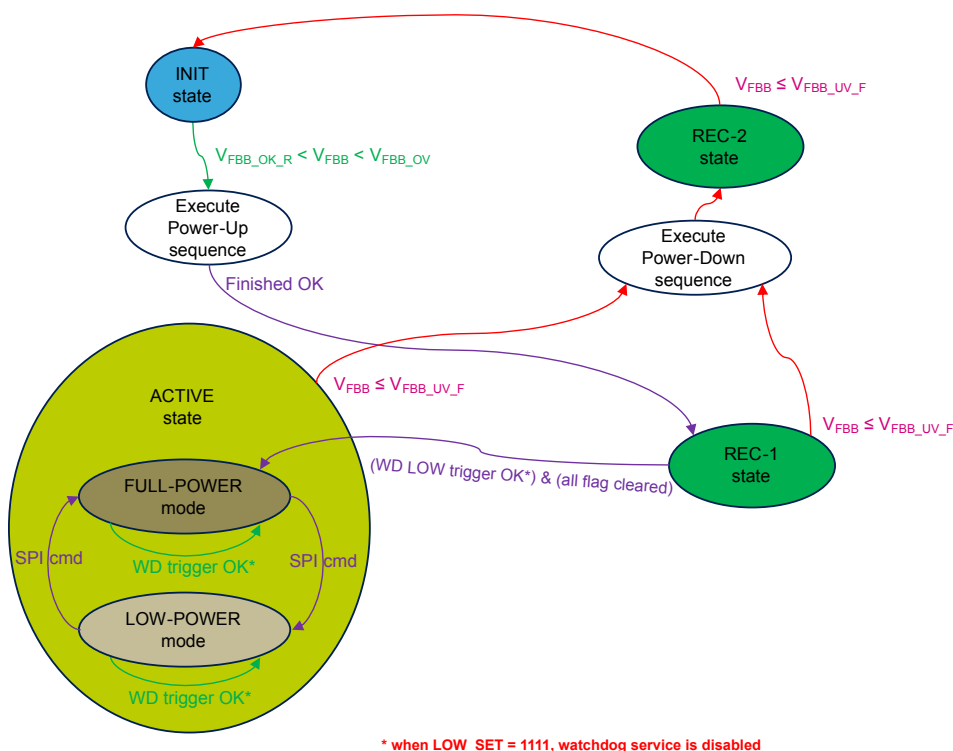


### 3.6.2.6

#### FBB voltage drop management

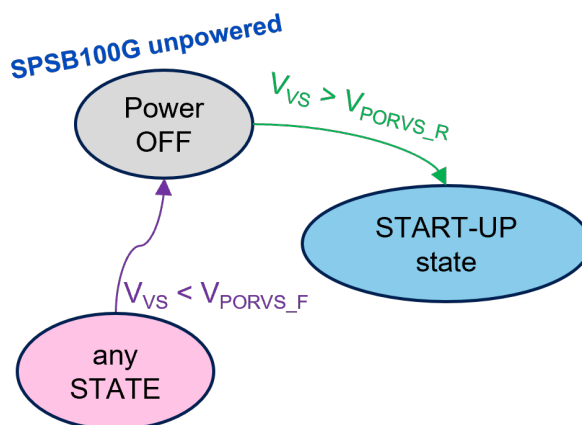
The SPSB100GS monitors the voltage on the FBB pin. The state machine reacts in case the FBB pin voltage drops below the  $V_{FBB\_UV\_F}$  threshold by executing a power-down sequence and transitioning to REC-2 then INIT state. In INIT state, the SPSB100GS restarts when the FBB pin voltage rises above  $V_{FBB\_OK\_R}$ .

Figure 24. FBB pin voltage fault reaction



In case the VS pin voltage drops below  $V_{PORVS\_F}$ , a hard reset of the SPSB100GS is generated independently of the SPSB100GS's current state, the POWER-OFF state is forced. The SPSB100GS starts up again after the VS pin voltage rises above  $V_{PORVS\_R}$ .

Figure 25. VS pin voltage fault reaction

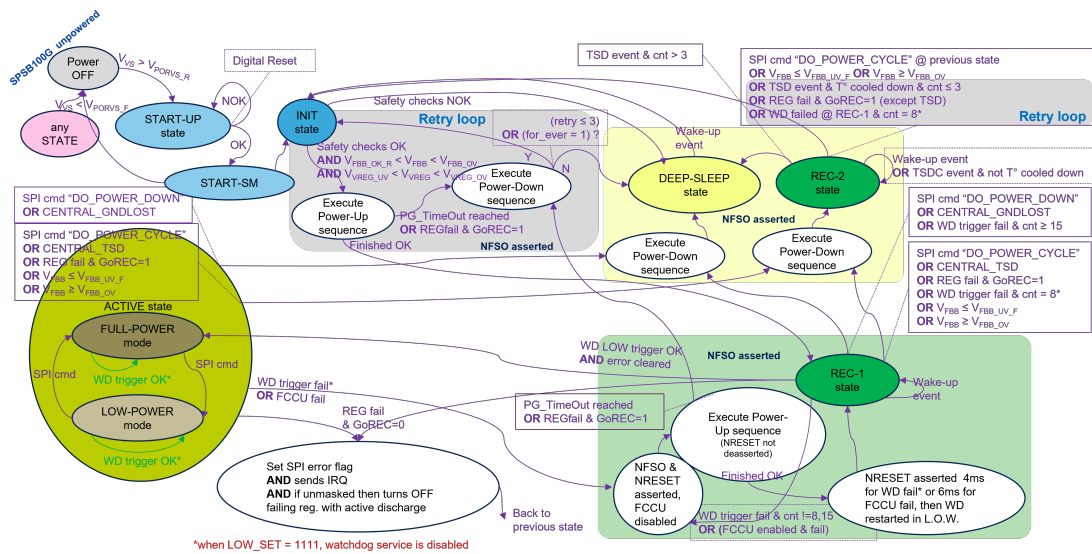


### 3.6.3

#### States and transitions description

The following figure shows the entire state machine.

**Figure 26. State machine**



SPSB100GS states can be read by status register bits DEV\_STATE.

### 3.6.3.1 Power-OFF state

Power-OFF state is the default state when the SPSB100GS is not powered.

This state is entered unconditionally when the VS pin voltage drops below  $V_{PORVS\_F}$ .

### 3.6.3.2 START-UP state

START-UP state is entered from Power-OFF state when the VS pin voltage reaches  $V_{PORVS\_R}$ .

In this state, internal power supplies are established, and the digital core reset is released.

SPSB100GS transitions to START-SM state.

### 3.6.3.3 START-SM state

START-SM state is entered after START-UP completion when the digital core reset is released.

In this state, oscillators start and the main state machine is executed. It is possible to enter USER-NVM programming mode, refer to [Section 3.8](#) for details.

When USER-NVM programming mode is not entered, the SPSB100GS transitions automatically from START-SM to INIT state.

### 3.6.3.4 INIT state

INIT state is entered

- after completion of START-SM state and the NVM is loaded without error
- from DEEP-SLEEP state upon a wake-up event
- from REC-2 state when
- MCU sent the SPI command DO\_POWER\_CYCLE (only after SPI\_PROTECT\_ACCESS has been set) in ACTIVE or REC-1 state
- FBB pin voltage is below  $V_{FBB\_UV\_F}$  and VS pin voltage above  $V_{PORVS\_F}$
- Once thermal sensors detected a TSD event, the chip temperature has cooled down and the TSD counter has not reached 3
- A fault has been detected on a critical regulator output voltage ( $REGFAIL\_GO\_REC=1$ )
- 8 successive watchdog trigger faults have been detected
- In case a fault has been detected during the power-up sequence and the power-up retry counter does not reach 3, or LOOP\_FOR\_EVER bit is set to 1

In the INIT state, when the FBB pin voltage rises above  $V_{FBB\_OK\_R}$  (the minimum voltage allowing the SPSB100GS to power up), the SPSB100GS executes the digital BIST before initiating a power-up sequence.

### 3.6.3.5 **ACTIVE state**

ACTIVE state is the state reached after a successful power-up sequence, after the MCU has performed a read & clear of SPI error flags in RECOVERY-1 state, and triggered the watchdog in long open window timeout.

In ACTIVE state, the SPSB100GS can be configured in FULL-POWER or LOW-POWER modes.

In both modes, the MCU can configure the watchdog timings and control the NFSO1 pin through the SPI.

Reaction to fault detection is independent of the POWER modes.

#### 3.6.3.5.1 **FULL-POWER mode**

FULL-POWER mode is the default mode when entering ACTIVE state from RECOVERY-1 state.

In FULL-POWER mode, all features of the SPSB100GS are accessible and configurable by SPI registers, in particular the MCU can switch some regulators OFF to optimize ECU power consumption.

In FULL-POWER mode, regulator monitors are active and analog & digital BIST can be run on demand by the MCU, as described in [Section 4.15](#) and [Section 4.16](#). Watchdog is running and must be served, except if  $LOW\_SET = 1111$ . The NFSO1 pin is controllable by SPI register.

#### 3.6.3.5.2 **LOW-POWER mode**

LOW-POWER mode is accessible by SPI in ACTIVE state from FULL-POWER mode. In this mode the SPSB100GS power consumption is reduced by:

- Turning OFF low-level hardware monitors
- Turning OFF the redundant voltage and current bias blocks
- Turning OFF NVM run time checks
- Turning OFF the ADC
- Analog and digital BIST shall not be executed on demand

In LOW-POWER mode

- The watchdog is running and must be served (except if  $WD\_LP\_ENA$  is set at 0), its timing is configurable to further reduce power consumption
- Central thermal monitoring is active
- If Buck1 and/or Buck2 and/or LDO1 is/are kept ON in a low-power setting, then OV and UV monitoring are active. See [Section 6](#) for functional safety details.
- Other regulators must be turn OFF before to enter in LOW-POWER mode

The MCU can decide to leave this mode by SPI command and return to FULL-POWER mode.

In LOW-POWER mode, the VIO must be supplied and SPSB100GS offers three possibilities:

- All regulators are turned OFF: In this case, VIO must be supplied by an external regulator
- Only Buck1 is kept ON in its low-power configuration. Buck1, or an external regulator, is used to supply VIO
- Buck1 and 2 are kept ON in their low-power configuration. Buck1 or 2, or an external regulator, is used to supply VIO.

#### 3.6.3.5.3 **Transitions between FULL-POWER and LOW-POWER modes**

Transitions between the two modes are the responsibility of the MCU.

To transition to LOW-POWER mode, the following sequence must be performed by the MCU:

- Assert low NFSO1 output (optional)
- Reconfigure watchdog timing (optional)
- Disable watchdog by setting WD\_LP\_ENA = 0 (optional)
- Turn off FCCU monitoring feature
- Turn OFF Buck3 and LDO2 regulators
- Buck1 and/or Buck2 can be kept ON if one of it is used to supply VIO
- LDO1 can be kept ON to allow CAN-FD transceiver to transmit (optional)
- Configure wake-up sources and IRQ generation (optional)

Until this step, the SPSB100GS is still in FULL-POWER mode, but with tuned settings.

- Set SPI bit LOW\_POWER\_SET to 1 (only after SPI\_PROTECT\_ACCESS has been set)

This last action sets the SPSB100GS in LOW-POWER mode, and the SPSB100GS generates an interruption to confirm the proper transition to LOW-POWER mode (except if MASK\_LP\_READY\_IRQ is set) and sets status bit LP\_READY.

To transit from LOW-POWER to FULL-POWER mode, the following sequence must be performed by the MCU:

- Clear SPI bit LOW\_POWER\_SET to 0 (only after SPI\_PROTECT\_ACCESS has been set)

This first action sets the SPSB100GS in FULL-POWER mode, the SPSB100GS generates an interruption to confirm the proper transition to FULL-POWER mode and sets status bit FP\_READY. The MCU must wait for this confirmation before continuing, then:

- Turn ON other regulator(s) as per application needs
- Reconfigure watchdog timing to satisfy functional safety requirements (optional)
- Turn ON FCCU monitoring feature
- Trigger watchdog during LOW
- Configure wake-up sources and IRQ generation (optional)
- De-assert NFSO1 output

The low-level hardware monitoring is turned back ON when SPI bit LOW\_POWER\_SET is cleared. If a hardware fault is detected, the SPSB100GS transitions asynchronously to DEEP-SLEEP state.

LOW\_POWER\_SET, FP\_READY and LP\_READY are not automatically cleared in case of transition due to hard fail.

### 3.6.3.6

#### **REC-1 state**

The SPSB100GS enters REC-1 state in two cases

- from INIT state after the power-up sequence ended successfully
- from ACTIVE state after a WD trigger issue or a FCCU fault is detected

When entering REC-1 state

- NFSO1 output is asserted low
- FCCU monitoring is turned OFF
- WD starts a LOW, except if LOW\_SET = 1111

In this state all voltage regulators are set according the power-up sequence settings stored in the USER-NVM. If any of the voltage regulators configured in the power-up sequence were switched off in ACTIVE state through the SPI, they are enabled upon entering REC-1 state.

The transition from REC-1 to ACTIVE state is started after the MCU has read and cleared error flags (if any, see [Section 9.8](#)) and triggered the WD in LOW.

In REC-1 state, the MCU cannot de-assert NFSO1 output. Further WD trigger fault will generate a NRST low pulse of  $t_{NRST\_WDR}$ . See the Watchdog paragraph for further details ([Section 3.10](#)). If FCCU is enabled by the MCU and an FCCU fault is detected, then the SPSB100GS remains in REC-1 state and generates an NRST low pulse of  $t_{NRST\_FCCU}$ . See the FIN1 paragraph for details ([Section 3.11](#)).

### 3.6.3.7

#### **REC-2 state**

The SPSB100GS enters REC-2 state from ACTIVE state and generates status register bit FSM\_TO\_REC2 = 0 in case of:

- DO\_POWER\_CYCLE SPI command (only after SPI\_PROTECT\_ACCESS has been set)
- The temperature of the central sensor exceeds the  $T_{SDC}$  threshold
- A fault on one of the regulators occurs, and its REGFAIL\_GO\_REC configuration bit is set to 1
- The FBB pin voltage falls below  $V_{FBB\_UV\_Fx}$  (  $x=1$  or  $2$  ) or above  $V_{FBB\_OV}$

The SPSB100GS enters REC-2 state from ACTIVE state and generates status register bit REC2\_FROM\_DO\_POWER\_CYCLE = 01 in case of DO\_POWER\_CYCLE SPI command (only after SPI\_PROTECT\_ACCESS has been set). REC2\_FROM\_DO\_POWER\_CYCLE can be cleared by CLR\_REC2\_FROM\_DO\_POWER\_CYCLE bit.

The SPSB100GS enters REC-2 state from REC-1 state and generates status register bit FSM\_TO\_REC2 = 1 in case of:

- DO\_POWER\_CYCLE SPI command (only after SPI\_PROTECT\_ACCESS has been set)
- The temperature of the central sensor surpassed the  $T_{SDC}$  threshold
- A fault on one of the regulators occurred and its REGFAIL\_GO\_REC configuration bit is set to 1
- 8 consecutive WD trigger faults
- The FBB pin voltage falls below  $V_{FBB\_UV\_Fx}$  (  $x=1$  or  $2$  ) or above  $V_{FBB\_OV}$

The SPSB100GS enters REC-2 state from REC-1 state and generates status register bit REC2\_FROM\_DO\_POWER\_CYCLE = 1X in case of DO\_POWER\_CYCLE SPI command (only after SPI\_PROTECT\_ACCESS has been set). REC2\_FROM\_DO\_POWER\_CYCLE can be cleared by CLR\_REC2\_FROM\_DO\_POWER\_CYCLE bit.

When entering REC-2 state

- the NFSO1 output is asserted low
- FCCU monitoring is turned OFF
- NRST is asserted low and regulators are turned off according to the programmed power-down sequence
- In case of a TSD event, the TSD counter is incremented and the SPSB100GS waits for the temperature to cool down

From REC-2 state, the SPSB100GS transitions to DEEP-SLEEP state for unrecoverable faults, or to INIT state to power up again.

### 3.6.3.8

#### **DEEP-SLEEP state - Unrecoverable faults**

The SPSB100GS enters DEEP-SLEEP state from ACTIVE - FULL-POWER state in case of:

- DO\_POWER\_DOWN SPI command (only after SPI\_PROTECT\_ACCESS has been set)
- Power ground lost

The SPSB100GS enters DEEP-SLEEP state from REC-1 state in case of:

- DO\_POWER\_DOWN SPI command (only after SPI\_PROTECT\_ACCESS has been set)
- Power ground lost
- 15 consecutive WD trigger faults

The SPSB100GS enters DEEP-SLEEP state from REC-2 state in case of:

- The temperature of one sensor surpassed the TSD threshold and TSD counter (TSD\_CNT\_FAIL) reached 3
- The counter of regulator (REG\_FAIL\_CNT) fail events reached 3

When entering DEEP-SLEEP state from ACTIVE or REC-1 states

- the NFSO1 output is asserted low
- FCCU monitoring is turned OFF
- NRST is asserted low and regulators are turned off according to the programmed power-down sequence

The SPSB100GS remains in DEEP-SLEEP state until a wake-up event occurs. The design of the SPSB100GS has been optimized to offer very low power consumption while being wake-able by external events.

DEEP-SLEEP state is also entered

- in case of HW low-level error, refer to [Section 4.8](#) for details
- from INIT state in case of safety check error, refer to [Section 4.17](#) for details
- in case of repeated power-up fault (refer to chapter [Section 3.6.2.3](#))

## 3.7 Power-up and power-down sequence

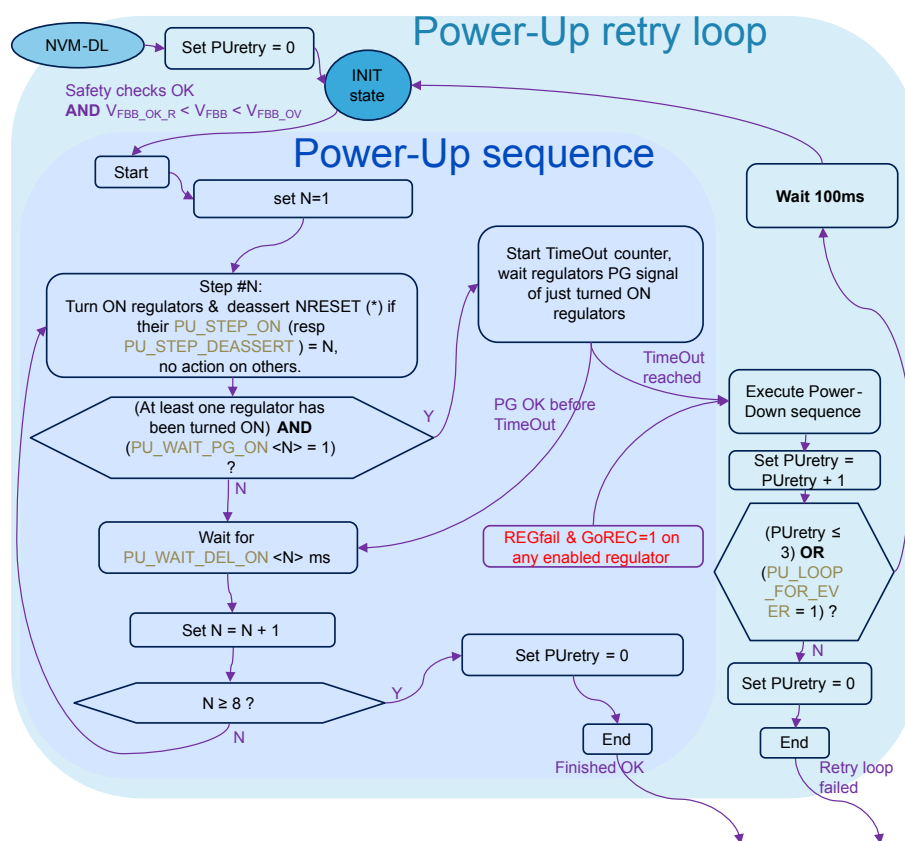
The power-up and power-down sequences turn all the regulators ON and OFF automatically. The sequences are executed by the device state machine as described in [Section 3.6](#) and are fully programmable through the USER-NVM space to cover a broad range of applications.

The sequences control Buck1, 2, 3 and LDO1, 2 regulators, together with the NRST pin.

### 3.7.1 Power-up sequence

The power-up sequence consists of 7 steps as described below.

**Figure 27. Power-up sequence**



Each of Buck1, 2, 3, and LDO1, 2 can be turned ON with USER-NVM bits BUCK1\_PU\_STEP\_ENA, BUCK2\_PU\_STEP\_ENA, BUCK3\_PU\_STEP\_ENA, LDO1\_PU\_STEP\_ENA, LDO2\_PU\_STEP\_ENA at any step from 1 to 7. None, or more than one, regulator can be turned ON at any step.

The NRST pin can be deasserted at any step from 1 to 7, with USER-NVM bits NRESET\_PU\_STEP\_DEASSERT independently of regulators setting. Note that the watchdog timeout starts at the step where NRST is deasserted.

After a regulator has been turned ON at step N, the sequence offers the possibility to wait for power-good signal with USER-NVM bits PU\_WAIT\_PG\_ENA\_X (X equal to steps from 1 to 7):

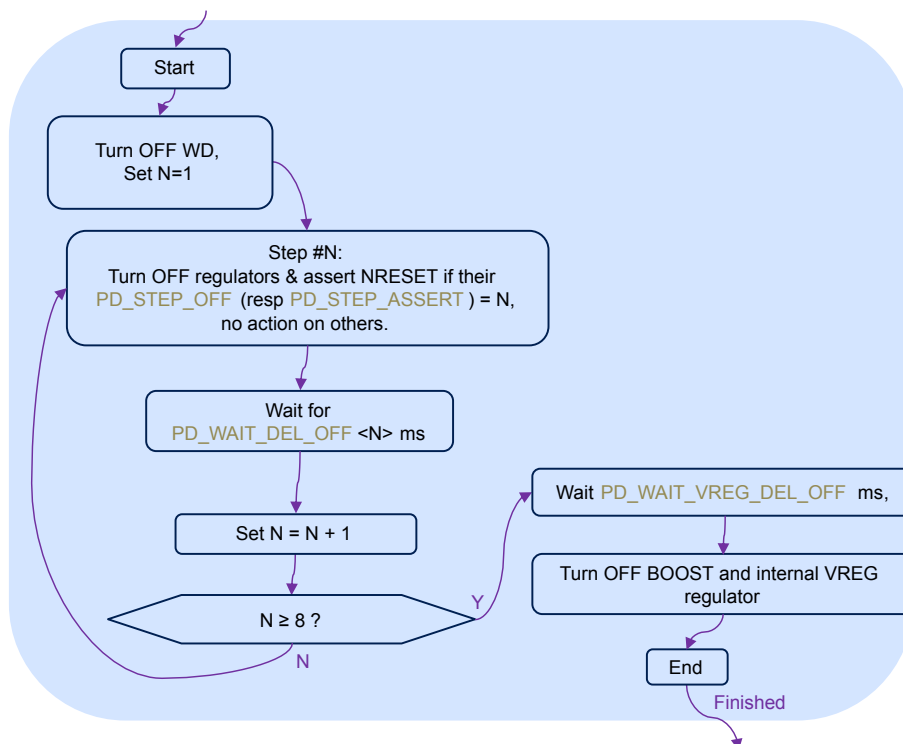
- If this option is selected, then the device waits for PG signal of all regulators turned ON at step N. A timeout is used to detect a fault; if the timeout expires, a power-down sequence is executed and a retry procedure is started as described in [Section 3.6.2.3](#).
- If not, or when the PG level is reached, the sequence is paused for a programmable delay with USER-NVM bits PU\_WAIT\_DEL\_ENA\_X (X equal to steps from 1 to 7) before proceeding to the next step.

While the sequence executes, any regulator fault is managed as per its REGFAIL\_GO\_REC setting as described in [Section 3.6.2.5](#).

### 3.7.2 Power-down sequence

The power-down sequence consists of 7 steps as described below.

**Figure 28. Power-down sequence**



Each of Buck1, 2, 3, and LDO1, 2 can be turned OFF with USER-NVM bits BUCK1\_PD\_STEP\_OFF, BUCK2\_PD\_STEP\_OFF, BUCK3\_PD\_STEP\_OFF, LDO1\_PD\_STEP\_OFF, LDO2\_PD\_STEP\_OFF at any step from 1 to 7. None, or more than one regulator can be turned OFF at any step.

The NRST pin can be asserted at any step from 1 to 7 with USER-NVM bits NRESET\_PD\_STEP\_ASSERT, independently of regulator settings. Note that the watchdog is stopped before step 1.

After a regulator has been turned OFF at step N, the sequence offers the possibility to wait for a programmable delay with USER-NVM bits PD\_WAIT\_DEL\_OFF\_X (X equal to steps from 1 to 7).

When the sequence ends, an extra delay can be programmed before turning OFF the BOOST and internal VREG with USER-NVM bits PD\_WAIT\_VREG\_DEL\_OFF.

## 3.8 User NVM modification procedure

The SPSB100GS integrates a Non-Volatile Memory (NVM) to store ST factory trim data and customer personalization data. Trim data are stored in the ST-NVM space, while customer data are stored in the USER-NVM space.

The SPSB100GS is delivered out of ST factory with default values stored in the USER-NVM space. Default values ensure proper behavior of the application with a SR6x microcontroller, as in the Configuration 1 shown in Figure 7. Details of default power-up and -down settings can be found in [Section 3.1.1](#).

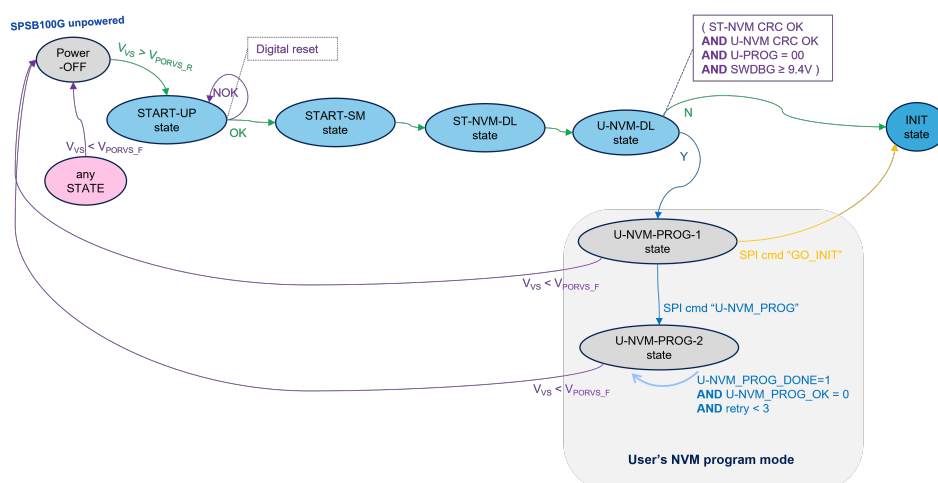
The customer has the option to reprogram the USER-NVM space only once, or use the default values stored by ST.

The U\_NVM\_RELEASE<15:0> bits in the USER-NVM space can be used to store a USER-NVM configuration release. The default value is 1d.

The following figure illustrates how to program the NVM. The following color code is used to indicate the offered possibilities:

- Green: The SPSB100GS starts up with valid data stored in the ST-NVM and USER-NVM (USER-NVM previously programmed by ST or by the customer)
- Blue: The SPSB100 enters the USER-NVM programming procedure
- Orange: The USER-NVM emulation feature is used

**Figure 29. NVM programming procedure**



### 3.8.1 Start-up with valid NVM data and NVM faults management

The ST-NVM data are read in the ST-NVM-DL state, then the USER-NVM data are read in the U-NVM\_DL state. If the conditions to enter the USER-NVM modification procedure are not met, the state machine proceeds to INIT state where further safety checks will be performed.

### 3.8.2 USER-NVM emulation procedure

It is possible to emulate the USER-NVM content using the data stored in the RAM image.

This can only be done when the USER-NVM has not been programmed by the user.

To do so, force the voltage on the SWDBG higher than  $V_{NVM\_EMU\_H}$  (20 V max), before plugging in the power supply, to enter the USER-NVM modification mode. The modification mode is entered after current ST- and U-NVM data have been read and their CRC checked.

First, the state machine enters the USER-NVM-PROG-1 state. In this state, the user must supply  $V_{IO}$  externally (3.3 or 5.0 V).

At this stage, the SWDBG pin can be released and does not have to be maintained higher than  $V_{NVM\_EMU\_H}$ . The user can then modify the USER-NVM RAM through SPI access and the U\_NVM SPI registers from DCR10 up to DCR28 can be written.

When completed, the user can set the GO\_INIT through SPI access. This results in the state machine transitioning to the INIT state.

It is forbidden to enable regulators in the USER-NVM-PROG-1 state.

The USER-NVM emulated values are lost if the power supply at the VS pin is below  $V_{PORVS\_R}$ .

During emulation mode, the values of the U\_NVM\_CRC0 and U\_NVM\_CRC1 bits in DCR17 and DCR25 are not considered by the device.

In USER-NVM emulation mode, the runtime check of the USER-NVM is disabled. For this reason, the USER-NVM emulation mode shall be used for debug purposes only.

### 3.8.3 USER-NVM programming procedure

The user can emulate the USER-NVM as many times as they want, as long as the USER-NVM is not programmed by the user. Once programmed by the user, the USER-NVM cannot be emulated and the device proceeds with valid data stored in the USER-NVM.

To program the USER-NVM, it is necessary to first emulate the USER-NVM with the desired configuration. During this emulation for programming, the user must perform at least a write to DCR17 and DCR25 with any value corresponding to their need. This is necessary to initiate some bits that will be used to allow proper programming. The USER-NVM uses NVM CRC to check that NVM content is correct, but during programming, the user does not have to take care of this because the correct CRC will be calculated by the SPSB100GS from emulated data and will be programmed with emulated data.

Then, instead of the GO\_INIT bit set through SPI access, the user must set the U-NVM\_PROG bit (only after SPI\_PROTECT\_ACCESS has been set). This starts the USER-NVM programming and sets the device to USER-NVM-PROG-2 state.

When the USER-NVM programming is completed, the status bit NVM\_PROG\_DONE is set. The user can read this status bit through SPI access. When this bit is set, the user can read the NVM\_PROG\_OK status bit to verify that the USER-NVM programming has been completed correctly, because the USER-NVM programming is followed by the USER-NVM verification.

If the USER-NVM programming has failed and the NVM\_PROG\_OK status bit is low when the NVM\_PROG\_DONE status bit is set, the user may request a new programming by setting the U-NVM\_PROG control bit to "0" (only after SPI\_PROTECT\_ACCESS has been set) then setting again this bit to "1". This operation can be done twice, so there is a maximum programming possibility of three times. If at the end of three USER\_NVM programming requests, NVM\_PROG\_OK is still low when NVM\_PROG\_DONE is high, the chip cannot be programmed anymore and cannot start correctly. In this case, any new programming request will be ignored.

After a valid USER-NVM programming procedure, the U\_NVM SPI registers from DCR10 to DCR28 can only be readable.

### 3.8.4 Loading USER-NVM data into RAM image

To program the USER-NVM, it is necessary to load the data (CRC included) into a dedicated portion of the RAM. This is done automatically by the state machine.

## 3.9 Wake-up inputs: IGN and WU

### 3.9.1 Standard wake-up functionality

Both inputs can be configured as wake-up sources (through the IGN\_ENA and WU\_ENA control bits). In particular, the IGN input can be used as a wake-up source connected to ignition (KL15) via a resistor.

The voltage can also be read back via SPI through 10-bit ADC monitoring (IGN[9..0] bits, in addition to WU[9..0] ones).

In case WU, or IGN, is directly connected to battery line, the input must be protected by a series resistance of typical 1 kΩ to sustain reverse battery condition.

Each wake-up input is sensitive to any level transition (rising and falling edge) and can be configured for static or cyclic monitoring of the input voltage level by suitable setting of WU\_FILT and IGN\_FILT bits, which allows to choose between static or cyclic monitoring with a timer. When the configuration of a timer is changed, the timer is automatically restarted using the new configuration.

For static contact monitoring, a filter time of  $t_{WU\_stat}$ ,  $t_{IGN\_stat}$  is implemented. The filter is started when the input voltage crosses the specified thresholds  $V_{WUthp}$ ,  $V_{IGNthp}$  (both thresholds are linked to the  $V_{FBB}$  level). The wake-up status bits (WU\_WAKE and IGN\_WAKE bits) are set only if this threshold is exceeded for longer than  $t_{WU\_stat}$ ,  $t_{IGN\_stat}$ .

Cyclic contact monitoring instead allows for periodical (not threshold dependent) activation of the wake-up input to read the status of the external contact. The periodical activation is driven by a timer whose settings (on-time and period) can be configured through the T1\_PER[2..0] and T1\_ENA[2..0] bits.

The input signal is filtered with a filter time of  $t_{WU\_cyc}$  ( $t_{IGN\_cyc}$ ) after a delay (80% of the configured timer on-time). A wake-up is processed if the status has changed from the previous cycle. Therefore, the wake-up status WU\_WAKE and IGN\_WAKE bits are set only if the status during a subsequent on-time is different, after the configured delay and  $t_{WU\_cyc}$  ( $t_{IGN\_cyc}$ ). This can be done only if WU\_CONFIG and IGN\_CONFIG are configured as wake-up inputs.

In ACTIVE LOW-POWER or DEEP-SLEEP modes, the WU and IGN inputs are configurable with an internal pull-up or pull-down current source according to the WU\_PU and IGN\_PU SPI bits set up.

In ACTIVE FULL-POWER mode, the inputs have an internal pull-down resistor (RWU\_act) and the input status can be read by WU\_STATE and IGN\_STATE. This can be done only if WU\_CONFIG and IGN\_CONFIG are configured as wake-up inputs and if WU\_ENA and IGN\_ENA are set high.

The output OUT\_HS can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the wake-up input.

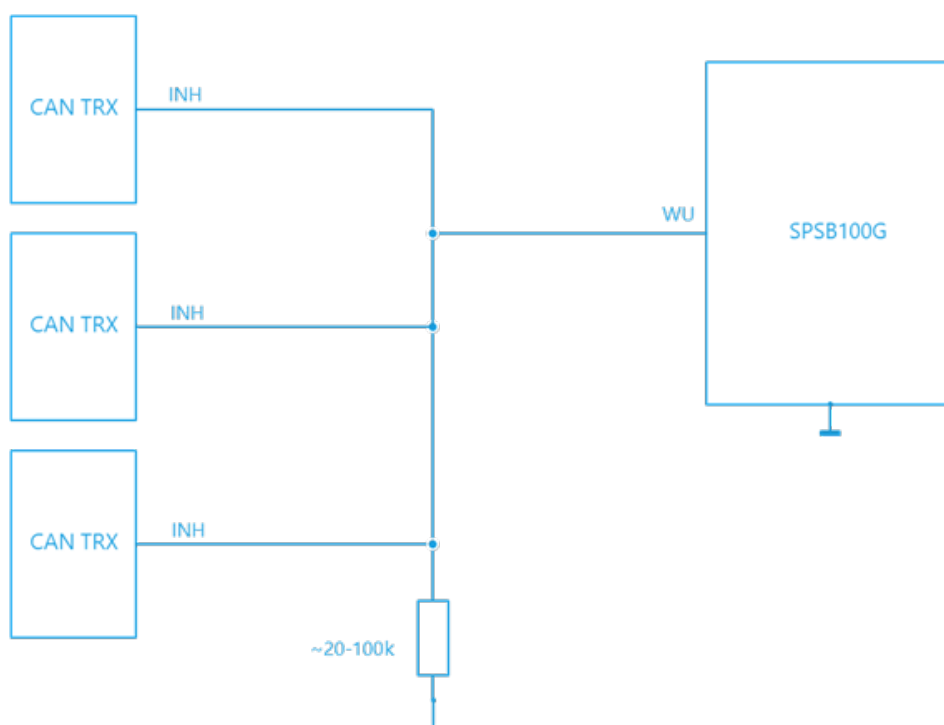
If WU\_ENA = 1 and WU\_CONFIG = 1, the wake-up capability and the voltage measurement through ADC are both activated on the WU pin.

If IGN\_ENA = 1 and IGN\_CONFIG = 1, the wake-up capability and the voltage measurement through ADC are both activated on the IGN pin.

### 3.9.2 Extended wake-up functionality

It is possible to inhibit the DEEP-SLEEP transition by using the WAKEUP\_GO\_TO\_DEEP\_SLEEP\_INH bit. For example, when the SPSB100GS is woken up by external transceivers as shown below:

**Figure 30. Wake-up functionality**



To activate this extended wake-up functionality for the SPSB100GS, the bit WAKEUP\_GO\_TO\_DEEP\_SLEEP\_INH must be set to "1". In this case, the request via the DCR bit DO\_POWER\_DOWN to transition to DEEP-SLEEP mode will be considered only if no wake-up events occur before the execution of the power-down sequence. In case a valid wake-up sources is detected, the SPSB100GS inhibits the transition to DEEP-SLEEP state and the SPSB100GS remains in ACTIVE state.

**Note:** *Extended wake-up functionality is intended to force the MCU to take into account all wake-up events before requesting the power-down sequence.*

**Note:** *Extended wake-up capability can set device in infinite retry loop if MCU is not able to clear a potential wake up flag after the 15 watchdog fails.*

### 3.10 Configurable time-out window watchdog

During normal operation, the watchdog monitors the microcontroller within a programmable trigger cycle (see Figure 65 and Figure 66).

After a power-up sequence, the watchdog starts with a long open window  $t_{LW}$ . The watchdog allows the microcontroller to run its own setup, and then to start the window watchdog by setting WD\_TRIG=1.

The long open window ( $t_{LW}$ ) is configurable via the USER-NVM through the bits LOW\_SET [3..0].

Subsequently, the microcontroller has to serve the watchdog by alternating the watchdog trigger bit within the safe trigger area  $T_{SWX}$  (see Figure 65). The trigger time is configurable via SPI.

A correct watchdog trigger signal will immediately start the next cycle.

A watchdog trig will not take into account if the NRST pin is low.

If LOW\_SET [3..0] is set at "1111", the long open window is set to an infinite duration. In this case, if the application does not require a watchdog, the microcontroller must not trigger the watchdog. So, the device will transition from REC-1 to ACTIVE FULL-POWER after a read and clearing of error flags. If the watchdog is triggered even with LOW\_SET [3..0] set to "1111", the watchdog starts with the default window and then has to be served. Note that in the case of LOW\_SET = 1111, so in case the watchdog service is disabled, it must be considered in the safety analysis based on FIT calculation, as described in the Safety Manual.

The watchdog trigger time can be configured by setting the WD\_TIME [3..0] bits (only after SPI\_PROTECT\_ACCESS has been set) and the default value is 0001 (window 2). The change of watchdog window timing through WD\_TIME in the SPI registers cannot be done when the watchdog is in long open window counting.

The microcontroller can read the LOW\_STATUS bit to ascertain if the watchdog is in long open window phase (when LOW\_STATUS is high) or in normal window (when LOW\_STATUS is low). When in the long open window phase, the LOW\_STATUS bit is high even if the watchdog is in infinite long open window. When not in infinite long open window, if FSM is in ACTIVE\_HP or ACTIVE\_LP state, the LOW\_STATUS is low and watchdog counts in normal window. When LOW\_STATUS is high, the current watchdog LOW is given by LOW\_SET[3:0]. When LOW\_STATUS is low, the current watchdog window is given by WD\_TIME\_STATUS[3:0]. During REC-1 FSM state, WD\_TIME[3:0] cannot be written because the watchdog is counting in a long open window.

In case of WD\_FAIL or FCCU\_FAIL, the watchdog starts in a long open window when NRST rises. In this case, the watchdog trig bit is automatically cleared. So, the microcontroller can trigger the watchdog with a WD\_TRIG bit high.

The new value of WD\_TIME is loaded into the watchdog module on the next trig event after the SPI configuration. The following watchdog cycle uses the new programmed value.

This means that when a watchdog is running on a current window, to change the window, the microcontroller must:

1. write the new watchdog window in WD\_TIME(3-0)
2. trig the watchdog in the current window.

Doing this, the watchdog restarts using the new window.

It is possible to disable the watchdog in ACTIVE – LOW-POWER mode only through the WD\_LP\_ENA bit set to "0" (only after SPI\_PROTECT\_ACCESS has been set). If WD\_LP\_ENA is set high again during ACTIVE - LOW-POWER mode, the watchdog will stay disabled and will restart with a long open window after the transition from ACTIVE-LP to ACTIVE-FP.

**Note:** Using WD\_LP\_ENA = 0 can mask a MCU issue during LOW-POWER mode.

Fault conditions can be detected through the following bits:

- The status bit WD\_ENA\_ECHO indicates that the watchdog is running when high. The status bit WD\_ENA\_ECHO\_ERROR indicates a watchdog echo error and generates an IRQ. This error can be masked by MASK\_WD\_ENA\_ECHO\_ERROR\_IRQ. In case of watchdog fail, a flag WDFAIL is set and the watchdog fail counter WDFAIL\_CNT is incremented up to 15 consecutive watchdog trig faults. After 15 consecutive watchdog trig faults, the bit FORCED\_SLEEP\_WDFAIL is set and the device will reach the DEEP-SLEEP state.

**Note:** The bit FORCED\_SLEEP\_WDFAIL will be set even if the device will not transition to DEEP-SLEEP, in case WAKEUP\_GO\_TO\_DEEP\_SLEEP\_INH is used. See chapter [Section 3.9.2](#).

- WDFAIL\_CNT can be reset by the CLR\_WDFAIL\_CNT bit.
- The microcontroller can ascertain the current state of the watchdog by reading WD\_TIMER\_STATE = 00, WD trig is a too early window trig, WD\_TIMER\_STATE = 01, WD trig is in valid window trig.

**Note:** A delay of 120  $\mu$ s should be added after WD\_TIMER\_STATE reaches 1 to guarantee a valid window when WD\_TIME setting = 0x00, 0x01, 0x02, 0x09 to 0x0F and a delay of 1.2 ms when WD\_TIME setting = 0x03 to 0x08.

Watchdog mask function:

In the ACTIVE state, it is possible to temporarily mask the watchdog fail effect by masking the NRST via SPI, setting WD\_NRST\_MASK = 1 (only after SPI\_PROTECT\_ACCESS has been set). In this case, the NRST is still asserted high during the eight successive watchdog trig faults.

After a power cycle, the WD\_NRST\_MASK is cleared to "0" (default value). If WD\_NRST\_MASK = 0, the NRST happens normally in case of WDG fail.

The following steps manage the watchdog mask function for the MCU bootloader:

1. Before going to the bootloader, the MCU needs to deactivate FCCU and read the status register to make sure no fccu\_fail is present.
2. MCU sets WD\_Nrst\_MASK=1 and enters the bootloader to reflash software or to do other operations.
3. After exiting the bootloader, the MCU has to make three consecutive WD\_TRIG: 1 - 0 - 1.
4. It will reset the WD internal counter whatever the state of the WD, as a wd\_fail will occur (sending trigs at 1 in RESET state ensures the reset of the counter).
5. Wait at least 100 ms (the NRST duration) to ensure being in the long open window.
6. The MCU can read LOW\_STATUS to be sure of being in LOW (optional).
7. Unmask NRST: WD\_Nrst\_MASK=0.
8. Start feeding WD with trig at '1' as needed in LOW.

### 3.11 FIN1 input

SPSB100GS integrates an MCU fault monitoring called FCCU. FCCU block can be configured to detect error reported by the MCU through FIN1 input. Two error reporting protocols are available: static and dynamic protocols.

#### 3.11.1 Static protocol

In this protocol MCU signals its own errors to SPSB100GS by driving FIN1 input pin at low or high level. MCU shall configure the SPSB100GS FCCU block as following:

- FCCU\_PROTOCOL shall be reset to 0
- FCCU\_STATIC\_ERROR shall be reset to 0 if MCU signals error driving FIN1 low, or set to 1 if MCU signals error driving FIN1 high
- MCU shall drive FIN1
- FCCU\_ENA shall be set at 1 to enable the monitoring feature (only after SPI\_PROTECT\_ACCESS has been set)

#### 3.11.2 Dynamic protocol

In this protocol, the MCU signals its own error to SPSB100GS by increasing the period, or half period, of the toggling signal sent to FIN1 input.

The FCCU block shall be programmed to monitor the half period of the toggling signal received on FIN1. The FCCU block is made of a counter clocked by a 400 kHz clock derived from the main oscillator, the counter is reset at each transition on FIN1 input. If the counter overflows, an error is signaled.

The counter overflow threshold is programmed on FCCU\_COUNTER<12:0> (only after SPI\_PROTECT\_ACCESS has been set). The oscillator accuracy shall be considered to calculate the value of this threshold, the following formula can be used:

$$\text{FCCU\_COUNTER} > \text{FIN1\_half\_period} * (400 \text{ kHz} + \text{main oscillator accuracy})$$

Example: with an MCU toggling signal at 4 882.8 Hz (min) with 50% of duty cycle, and 20% accuracy of SPSB100GS oscillator

$$\text{FCCU\_COUNTER} > (204.8 / 2) \mu\text{s} * (400 \text{ kHz} * 1.2) = 49.15, \text{ gives FCCU\_COUNTER} = 50 \text{ at minimum}$$

The MCU shall configure the SPSB100GS FCCU block as follows:

- FCCU\_PROTOCOL shall be set to 1
- FCCU\_STATIC\_ERROR can be used to configure an internal pull-up (set to 1) or an internal pull-down (reset to 0) on FIN1 input
- FCCU\_COUNTER shall be loaded to the overflow threshold (only after SPI\_PROTECT\_ACCESS has been set)
- MCU shall drive FIN1 with the proper toggling signal
- FCCU\_ENA shall be set at 1 to enable the monitoring feature (only after SPI\_PROTECT\_ACCESS has been set)

Each time a transisiton is detected on FIN1 input, the register FCCU\_LAST\_STABLE<12:0> is loaded with the last value of the FCCU counter. The MCU can read back this value through SPI.

### 3.11.3 Reaction on error

When an error is detected by the MCU fault monitoring, the NRST pin is asserted low, the status bit FCCUFAIL shall be set, the state machine reacts as described in Chapter Section 3.6.2.2. The live status bit FIN1\_STATE shows the current state of the FIN1 input.

To properly restart FCCU block after a FCCUFAIL detection, MCU has to write FCCU\_ENA=0, clear FCCUFAIL flag and re enable the monitoring by setting FCCU\_ENA=1.

The live bit FCCU\_ENA\_STATUS reflect the state of FCCU block.

## 3.12 High-side output OUT\_HS

In ACTIVE, FULL-POWER or LOW-POWER modes, and in DEEP-SLEEP states, the high-side driver output OUT\_HS can be configured for supplying external loads or contacts.

The High-side output can either be controlled:

- Permanently ON (OUTHHS\_[1..0] = 01)
- Permanently OFF (OUTHHS\_[1..0] = 00)
- Through an Internal Timer (OUTHHS\_[1..0] = 1x).

In timer mode configuration (when TIMER\_ENA= 1) the activation period can be configured through the bits T1\_PER [2..0] in the following range {10, 20, 50, 100, 200, 500, 1000, 2000 ms}.

On-time is configurable through bits T1\_ENA[1..0] in the following range {0.1, 0.3, 1, 10, 20 ms}.

In case the wake-up Inputs WU and IGN are configured in cyclic sense mode (WU\_FILT=1, IGN\_FILT=1), the capture of their input state is synchronized with the high-side timer mode:

- A switched ON delay time tDON\_OUT\_HS is applied after the high-side is turned ON
- A switched OFF delay time tDOFF\_OUT\_HS is applied after the high-side is turned OFF
- A fixed filter time of tWU\_cyc is applied after blanking time has elapsed before refreshing the WU\_WAKE or IGN\_WAKE.
- In case of status change detection between the previous and the new captured state, the status bits WU\_WAKE and IGN\_WAKE will be set in status register. Depending on the dedicated settings applied on each wake-up input, wake-up detection could wake up the SPSB100GS and/or generate an IRQ.

In case of overcurrent, detection is done by OUTHHS\_OC bit, OUTHHS driver is switched off after filter time toc\_out\_hs and an IRQ is generated except if MASK\_OUTHHS\_IRQ is set.

After an OC detection, OUTHHS can be re-enabled by clearing status bit OUTHHS\_OC.

In case of open load, detection is done by OUTHHS\_OL bit, an IRQ is generated except if MASK\_OUTHHS\_IRQ is set.

The live bit OUTHHS\_ENA\_STATUS reflects the state of OUTHHS output.

**Note:** *The high-side driver OUT\_HS is intended to drive resistive loads only. Therefore, only limited energy ( $E < 1 \text{ mJ}$ ) can be dissipated by the internal ESD diodes in freewheeling condition. For inductive loads ( $L > 100 \mu\text{H}$ ), an external freewheeling diode connected between GND and the OUT\_HS pin is required.*

## 3.13 Fail-safe output - NFSO1

The NFSO1 is asserted low when a fault event is detected. The objective of this pin is to drive an electrical safe circuitry independent from the MCU to deactivate the whole system and set the ECU to a protected and known state.

The NFSO1 pin is an open-drain output. An external pull-up resistor must be connected to VIO or VBAT.

The NFSO1 pin is controlled by an asynchronous OR of

- asynchronous supervisor of internal voltage reference. When a difference between the main and monitoring voltage reference is detected, the NFSO1 pin is asserted low
- synchronous monitor of main oscillator. When an oscillator frequency drift or a stuck-at condition is detected, the NFSO1 pin is asserted low
- when a watchdog or FCCU fail occurs, the NFSO1 pin is asserted low
- the SPI control bit NFSO\_ASSERT\_LOW writing effect is considered only in ACTIVE - FULL-POWER mode (only after SPI\_PROTECT\_ACCESS has been set)
  - NFSO\_ASSERT\_LOW = 1: pin is asserted low
  - NFSO\_ASSERT\_LOW = 0: pin is in high impedance. Its level is defined by external pull-up

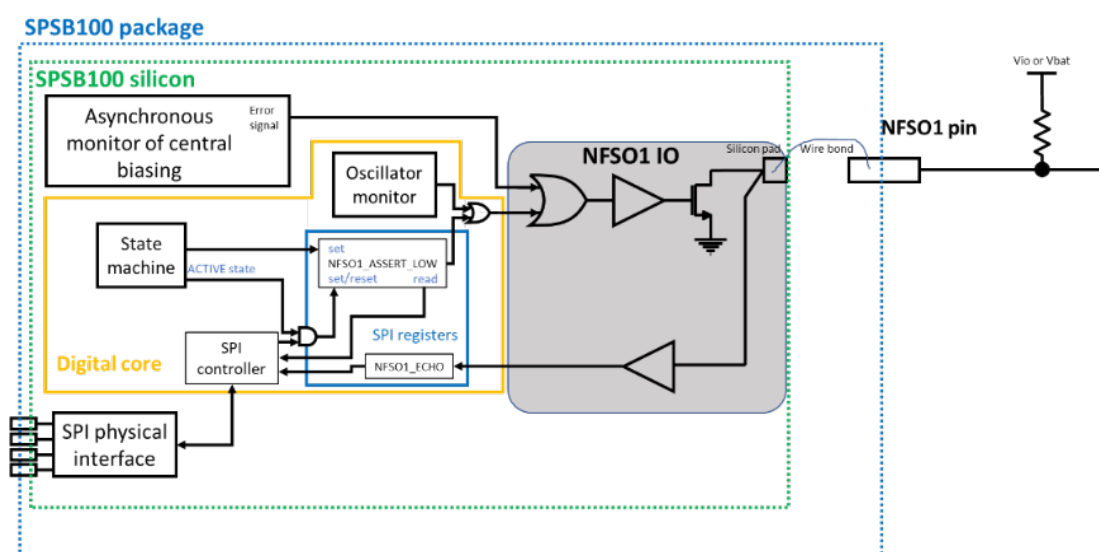
To avoid extra current drain consumption in DEEP-SLEEP due to the external pull-up on the NFSO1 pin, the default state can be selected via the user-NVM bit NFSO\_STATE\_IN\_DEEP\_SLEEP. When NFSO\_STATE\_IN\_DEEP\_SLEEP = 0, the NFSO1 pin is asserted (low), instead when NFSO\_STATE\_IN\_DEEP\_SLEEP = 1, the NFSO1 in deasserted (high) in DEEP-SLEEP.

The state machine can only set NFSO\_ASSERT\_LOW to 1, while the MCU can set, reset and read it, making the NFSO1 pin fully controllable by the MCU in ACTIVE state.

The SPI bit NFSO1\_ECHO is sensing the NFSO1 state on its silicon pad:

- NFSO1\_ECHO = 0: NFSO1 output pad is asserted low
- NFSO1\_ECHO = 1: The NFSO1 output pad is pulled up by external circuitry

Figure 31. NFSO1 implementation details



After a battery plug, after each power-up sequence, during a power-down sequence, or in INIT, REC-1, REC-2, DEEP-SLEEP states, the NFSO1 pin is asserted low. This is ensured by the state machine that sets the SPI bit NFSO\_ASSERT\_LOW to 1. In ACTIVE state, the MCU can decide to release the NFSO1 pin through the SPI when the application is ready to start.

**Note:** that NFSO1 reaction on fault is masked to avoid to react due to an ABIST request. This implementation generates a false NFSO\_ECHO\_ERROR flag in case of an ABIST request is done before asserting NFSO high (by SPI command writing NFSO\_ASSERT\_LOW = 0).

Figure 32. NFSO1 output pin behavior at battery plug

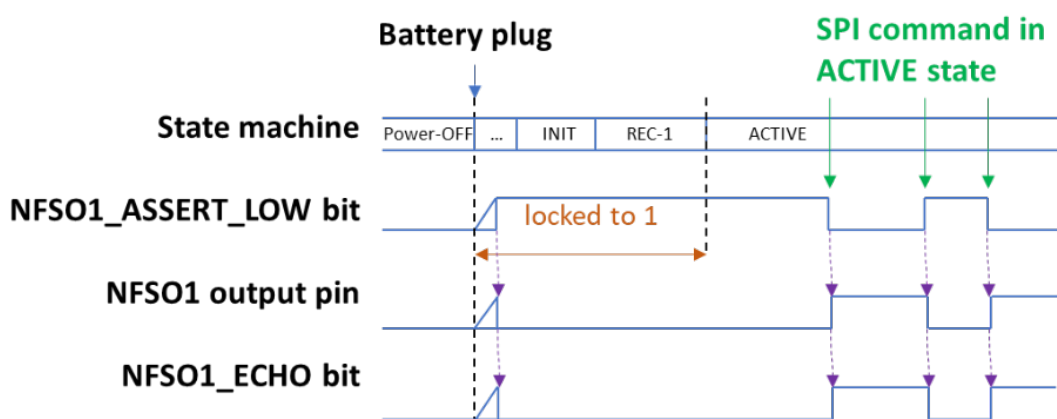
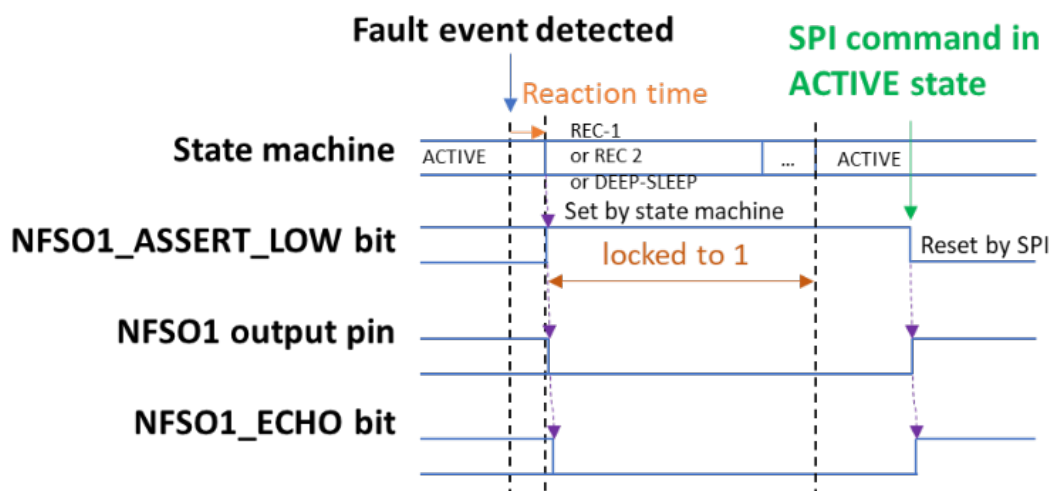


**Figure 33. NFSO1 output pin behavior after a failure is detected**


### 3.14 Interrupt - IRQ

The IRQ pin is an open-drain with an internal pull-up for echo generation. An external pull-up to  $V_{IO}$  level close to the MCU is strongly recommended. The IRQ pin is set low if any of the following events occur, as shown in the table below.

**Table 9. IRQ events**

| SPI status bit name | IRQ generated               | IRQ SPI mask name         |
|---------------------|-----------------------------|---------------------------|
| ABIST_COMPLETE      | Y                           | not maskable              |
| LBIST_COMPLETE      | Y                           | not maskable              |
| BOOST_IN_LP         | Y                           | MASK_BOOST_IN_LP_IRQ      |
| BOOST_VDSMON_ERROR  | Y                           | MASK_BOOST_VDSMON_IRQ     |
| BUCK1_OC            | Y if BUCK1_REGFAIL_GO_REC=0 | MASK_BUCK1_OC_IRQ         |
| BUCK1_OV            | Y if BUCK1_REGFAIL_GO_REC=0 | MASK_BUCK1_IRQ            |
| BUCK1_FB            | Y if BUCK1_REGFAIL_GO_REC=0 | MASK_BUCK1_IRQ            |
| BUCK1_PG_OK         | Y                           | MASK_BUCK1_PG_IRQ         |
| BUCK1_PG_TIMEOUT    | Y                           | MASK_BUCK1_PG_TIMEOUT_IRQ |
| BUCK1_UV            | Y if BUCK1_REGFAIL_GO_REC=0 | MASK_BUCK1_IRQ            |
| BUCK2_OC            | Y if BUCK2_REGFAIL_GO_REC=0 | MASK_BUCK2_OC_IRQ         |
| BUCK2_OV            | Y if BUCK2_REGFAIL_GO_REC=0 | MASK_BUCK2_IRQ            |
| BUCK2_FB            | Y if BUCK2_REGFAIL_GO_REC=0 | MASK_BUCK2_IRQ            |
| BUCK2_PG_OK         | Y                           | MASK_BUCK2_PG_IRQ         |
| BUCK2_PG_TIMEOUT    | Y                           | MASK_BUCK2_PG_TIMEOUT_IRQ |
| BUCK2_UV            | Y if BUCK2_REGFAIL_GO_REC=0 | MASK_BUCK2_IRQ            |
| BUCK3_OC            | Y if BUCK3_REGFAIL_GO_REC=0 | MASK_BUCK3_OC_IRQ         |
| BUCK3_OV            | Y if BUCK3_REGFAIL_GO_REC=0 | MASK_BUCK3_IRQ            |
| BUCK3_PG_OK         | Y                           | MASK_BUCK3_PG_IRQ         |
| BUCK3_PG_TIMEOUT    | Y                           | MASK_BUCK3_PG_TIMEOUT_IRQ |
| BUCK3_UV            | Y if BUCK3_REGFAIL_GO_REC=0 | MASK_BUCK3_IRQ            |
| BUCK1_INT_FAIL      | Y if BUCK1_REGFAIL_GO_REC=0 | MASK_BUCK1_IRQ            |

| SPI status bit name    | IRQ generated               | IRQ SPI mask name            |
|------------------------|-----------------------------|------------------------------|
| BUCK2_INT_FAIL         | Y if BUCK2_REGFAIL_GO_REC=0 | MASK_BUCK2_IRQ               |
| BUCK3_INT_FAIL         | Y if BUCK3_REGFAIL_GO_REC=0 | MASK_BUCK3_IRQ               |
| BYPASS_VDSMON_ERROR    | Y                           | MASK_BYPASS_VDSMON_IRQ       |
| NFSO1_ECHO_ERROR       | Y                           | MASK_NFSO1_ECHO_ERROR_IRQ    |
| FBB_OV                 | Y                           | MASK_FBB_OV_IRQ              |
| FBB_OV_EW              | Y                           | MASK_FBB_OV_EW_IRQ           |
| FBB_UV                 | Y                           | MASK_FBB_UV_IRQ              |
| FBB_UV_EW              | Y                           | MASK_FBB_UV_EW_IRQ           |
| FCCU_ENA_ECHO_ERROR    | Y                           | MASK_FCCU_ENA_ECHO_ERROR_IRQ |
| IRQ_REQUEST            | Y                           | not maskable                 |
| LDO1_PG_OK             | Y                           | MASK_LDO1_PG_IRQ             |
| LDO1_PG_TIMEOUT        | Y                           | MASK_LDO1_PG_TIMEOUT_IRQ     |
| LDO1_UV                | Y                           | MASK_LDO1_IRQ                |
| LDO2_OV                | Y                           | MASK_LDO2_IRQ                |
| LDO2_PG_OK             | Y                           | MASK_LDO2_PG_IRQ             |
| LDO2_PG_TIMEOUT        | Y                           | MASK_LDO2_PG_TIMEOUT_IRQ     |
| LDO2_UV                | Y                           | MASK_LDO2_IRQ                |
| NVM_PROG_DONE          | Y                           | not maskable                 |
| OUTHS_OC               | Y                           | MASK_OUTHS_IRQ               |
| OUTHS_OL               | Y                           | MASK_OUTHS_IRQ               |
| SPI_ALL_WAKEUP_DISABLE | Y                           | MASK_SPI_ERROR_IRQ           |
| SPI_REG_COMP_ERROR     | Y                           | MASK_SPI_ERROR_IRQ           |
| SPI_CLK_CNT            | Y                           | MASK_SPI_ERROR_IRQ           |
| SPI_CRC_ERR            | Y                           | MASK_SPI_ERROR_IRQ           |
| SPI_CSN_TIMEOUT        | Y                           | MASK_SPI_ERROR_IRQ           |
| SPI_LBISTED            | Y                           | MASK_SPI_ERROR_IRQ           |
| SPI_SDI_STUCK_HIGH     | Y                           | MASK_SPI_ERROR_IRQ           |
| SPI_SDI_STUCK_LOW      | Y                           | MASK_SPI_ERROR_IRQ           |
| SPI_STATUS_WRT         | Y                           | MASK_SPI_ERROR_IRQ           |
| SPI_UNDEF_ADD          | Y                           | MASK_SPI_ERROR_IRQ           |
| VS_UV_EW               | Y                           | MASK_VS_EW_IRQ               |
| TSD_CL1                | Y if BUCK1_REGFAIL_GO_REC=0 | not maskable                 |
| TSD_CL2                | Y if BUCK2_REGFAIL_GO_REC=0 | not maskable                 |
| TSD_CL3                | Y if BUCK3_REGFAIL_GO_REC=0 | not maskable                 |
| TSD_CL4                | Y if LDO2_REGFAIL_GO_REC=0  | not maskable                 |
| TW_CL0                 | Y                           | MASK_CL0_TW_IRQ              |
| TW_CL1                 | Y                           | MASK_CL1_TW_IRQ              |
| TW_CL2                 | Y                           | MASK_CL2_TW_IRQ              |
| TW_CL3                 | Y                           | MASK_CL3_TW_IRQ              |
| TW_CL4                 | Y                           | MASK_CL4_TW_IRQ              |
| IGN_WAKE               | Y                           | IGN_ENA=0                    |

| SPI status bit name | IRQ generated | IRQ SPI mask name          |
|---------------------|---------------|----------------------------|
| TIMER_WAKE          | Y             | TIMER_WAKE_ENA=0           |
| WU_WAKE             | Y             | WU_ENA=0                   |
| SWDBG_VIO           | Y             | MASK_SWDBG_VIO_IRQ         |
| WD_ENA_ECHO_ERROR   | Y             | MASK_WD_ENA_ECHO_ERROR_IRQ |
| FP_READY            | Y             | not maskable               |
| LBIST_STOPPED       |               | not maskable               |
| LP_READY            | Y             | MASK_LP_READY_IRQ          |

Interrupt is an NOR of all information, except if some masks are set. A read & clear of all set flags is needed to allow the IRQ pin to be set high.

The interrupt output pin indicates:

- warnings and errors which must be reported to the MCU
- Confirms a requested action from the MCU

### 3.15 Reset output - NRST

The NRST pin is an open-drain with an internal pull-up for echo generation. An external pull-up to  $V_{IO}$  level close to the MCU is strongly recommended.

The aim of the NRST output is to drive the MCU NRST input pin.

The NRST is released after a proper power-up sequence before reaching the REC-1 state, and is asserted low after  $t_{NRST\_rt}$ , in case of error as described in [Section 3.6.3](#).

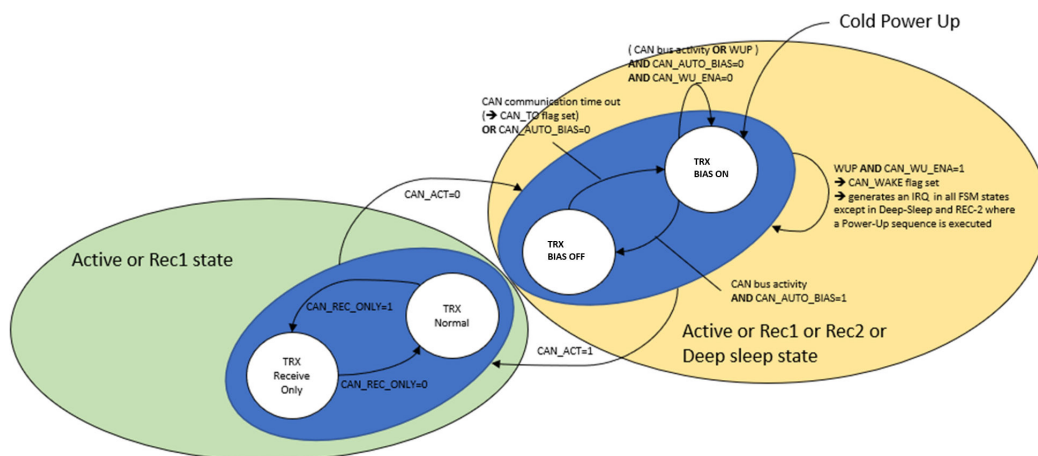
### 3.16 CAN FD bus transceiver (only for SPSB100GS)

#### 3.16.1 Features

- ISO 11898-2:2016 compliant
- CAN-FD cell has been designed according to IEC 62228-3
- Listen mode (transmitter disabled)
- Supported bitrates of at least 2 Mb/s for operation (5 Mb/s max bit rate)
- Function range from -27 V to +40 V DC at CAN pins
- GND disconnection fail-safe at module level
- GND shift operation at system level
- Microcontroller interface with CMOS compatible I/O pins
- ESD and transient immunity according to IEC 62215-3 and ISO 10605 per IEC 62228-3 standard
- Matched output slopes and propagation delay

### 3.16.2 CAN transceiver operating modes

Figure 34. Transceiver state diagram



#### TRX BIAS modes

After power-on reset ( $V_S > V_{PORVS\_R}$ ), the CAN transceiver is disabled and is by default in TRX BIAS OFF. The RxD\_C pin is kept at high level (recessive state) in REC-1 and ACTIVE states.

There is no automatic state transition into TRX Normal mode after a detection of a CAN wake-up signal (WUP).

CAN TRX BIAS mode includes two possible submodes: BIAS ON and BIAS OFF depending on the  $CAN\_AUTO\_BIAS$  bit (compliant with ISO 11898-2:2016). In BIAS ON,  $CAN\_H$  is set at  $V_{CANHrec}$  level and  $CAN\_L$  level is set at  $V_{CANLrec}$  level.

In TRX BIAS ON, if  $CAN\_AUTO\_BIAS$  is set at "1" and there has been no activity on the bus for a time longer than  $t_{silence}$ , then the bus lines are biased towards 0 V and the flag  $CAN\_TO$  is set. An IRQ is generated except if  $MASK\_CAN\_IRQ$  is set to "1".

The live bit  $CAN\_AUTO\_BIAS\_STATUS$  reflects the state of CAN auto biasing.

#### TRX normal mode

The transceiver can be enabled by setting  $CAN\_ACT = 1$ .

The live bit  $CAN\_ACT\_STATUS$  reflect the state of the CAN transceiver.

Full functionality of the CAN-FD transceiver is available (transmitter and receiver) in ACTIVE and REC-1 states. The voltage biasing is automatically enabled.

#### TRX Receive Only mode

In TRX Normal mode it is possible to disable the CAN transmitter by setting the  $CAN\_REC\_ONLY$  bit. In this mode, it is possible to listen to the bus but not send to it. The receiver termination network is still activated in this mode.

### 3.16.3 CAN error handling

The device provides the following five error handling features.

The CAN transmitter is disabled automatically in case of the following errors:

- Dominant TxD\_C timeout
- CAN permanent recessive
- RxD\_C permanent recessive
- Thermal shutdown on  $Th\_CL0$
- Undervoltage on LDO1

The CAN receiver is not disabled in case of any failure condition.

#### Dominant TxD\_C time out

If TxD\_C is in dominant state (low) for  $t > t_{dom}(TxD\_C)$ , the transmitter will be disabled, the status bit will be latched and can be read and optionally cleared by SPI (CAN\_TXD\_DOM bit). An IRQ is generated except if MASK\_CAN\_IRQ is set at "1". The transmitter remains disabled until the status register is cleared.

#### **CAN Bus Permanent Recessive**

If TxD\_C changes to dominant (low) state but CAN bus does not follow for four times, the transmitter will be disabled, the status bit will be latched and can be read and optionally cleared by SPI (CAN\_PERM\_REC bit). An IRQ is generated except if MASK\_CAN\_IRQ is set at "1". The transmitter remains disabled until the status register is cleared.

#### **CAN Permanent Dominant**

If the bus state is dominant for  $t > t_{CAN}$ , a permanent dominant status will be detected. The status bit will be latched and can be read and optionally cleared by SPI (CAN\_PERM\_DOM bit). An IRQ is generated except if MASK\_CAN\_IRQ is set at "1". The transmitter will not be disabled.

#### **RxD\_C Permanent Recessive**

If RxD\_C pin is clamped to recessive (high) state, the controller is not able to recognize a bus dominant state and could start messages at any time, which results in disturbing the overall bus communication.

Therefore, if RxD\_C does not follow TxD\_C for four times, the transmitter will be disabled. The status bit will be latched and can be read and optionally cleared by SPI (CAN\_RXD\_REC bit). An IRQ is generated except if MASK\_CAN\_IRQ is set at "1". The transmitter remains disabled until the status register is cleared.

#### **Thermal shut-down detection on cluster TSD\_CL0**

If Th\_CL0 temperature sensor exceeds the shut-down threshold, then the transmitter is disabled, the status bit is latched and can be read and optionally cleared by SPI (TSD\_CL0 bit). The transmitter remains disabled until the status register is cleared.

#### **LDO1 undervoltage**

If LDO1 output voltage decreases below the LDO1\_UV threshold, the transmitter is disabled. The status bit is latched and can be read and optionally cleared by SPI (LDO1\_UV bit). The transmitter remains disabled until LDO1 is re-enabled.

#### **CAN supply low**

If LDO1 output voltage decreases below CAN\_SUP\_LOW threshold for  $t > t_{VCANSUPLOW}$ , the status bit is latched and can be read and optionally cleared by SPI (CAN\_SUP\_LOW bit). An IRQ is generated except if MASK\_CAN\_IRQ is set at "1". The transmitter will not be disabled. CAN\_SUP\_LOW monitoring is enabled when CAN\_ACT = 1.

### **3.16.4**

#### **Wake-up by CAN**

If CAN\_WU\_ENA is set at "1", and the CAN transceiver is in one of TRX bias modes, then the CAN-Receiver is able to detect a wake-up pattern (WUP) and generate a CAN\_WAKE flag.

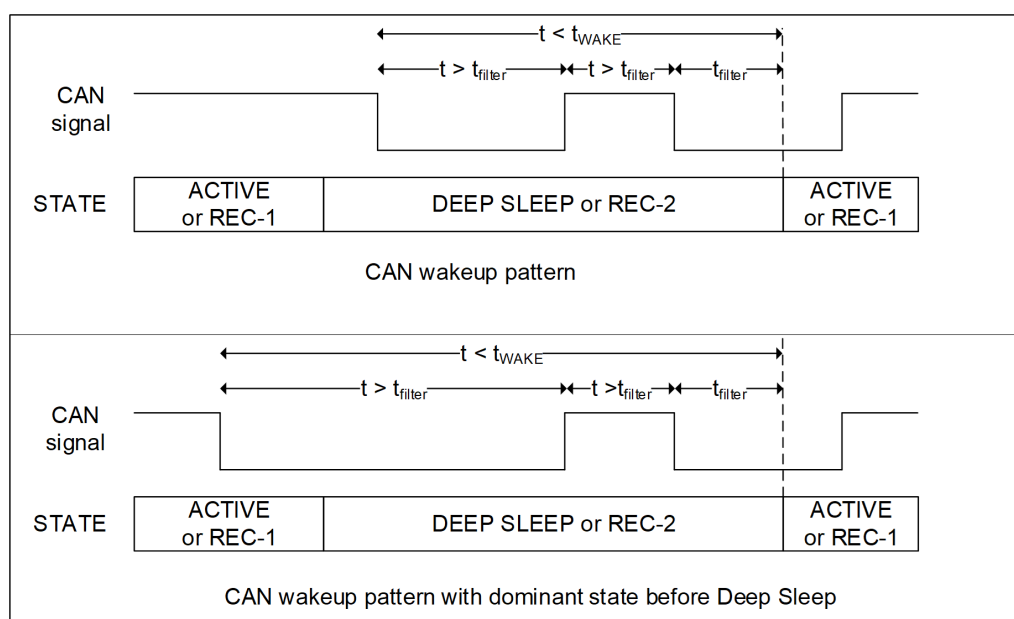
If such a pattern is detected (see [Figure 35](#)) and:

- If the device is in DEEP-SLEEP or REC-2 states, then a wake-up event is generated and CAN\_WAKE flag set
- If the device is in ACTIVE or REC-1 states, then an IRQ is generated and CAN\_WAKE flag is set

The CAN wake-up pattern (WUP) is defined (see Figure 35) by:

- a series of two consecutive dominant pulses, where each of them must be longer than  $t_{\text{filter}}$ .
- the distance between the two dominant pulses must be longer than  $t_{\text{filter}}$ .
- the two dominant pulses must occur within a time frame of  $t_{\text{wake}}$ .
- the wake-up event occurs when the duration of the second pulse becomes longer than  $t_{\text{filter}}$ .

**Figure 35. CAN wake-up capabilities**



### 3.16.5 CAN looping mode

If the CAN\_LOOP\_ENA (configuration register) is set, the TxD\_C input is mapped directly to the RxD\_C pin. This mode can be used in combination with the TRX Receive-only mode, to run diagnosis for the CAN protocol handler of the microcontroller.

### 3.16.6 Complete disabling of CAN transceiver

For those applications in which it is not requested, it is possible to completely disable the CAN transceiver by SPI. In this case, CAN\_WU\_ENA, CAN\_ACT and CAN\_AUTO\_BIAS must be cleared.

A further minimization of current consumption can be achieved by switching off LDO1, which internally supplies the transceiver. In this case, the protected bit LDO1\_ENA can be set to 0 only after SPI\_PROTECT\_ACCESS has been set.

## 3.17 10-bit ADC

In ACTIVE – FULL-POWER mode and REC-1 state, the voltage signals VS, FBB, WU, IGN, TH\_CL0, TH\_CL1, TH\_CL2, TH\_CL3, and TH\_CL4 are read out sequentially. Related bit names in the status register are VS[0..9], FBB[0..9], WU[0..9], IGN[0..9], TEMP\_CL0[0..9], TEMP\_CL1[0..9], TEMP\_CL2[0..9], TEMP\_CL3[0..9] and TEMP\_CL4[0..9].

The voltage signals are multiplexed to an ADC. The ADC is realized as a 10-bit SAR. Each channel is converted with a conversion time  $t_{\text{con}}$ , therefore an update of the ADC value is available every  $t_{\text{con}} * 13$ .

The voltage measurement on VS, FBB, WU and IGN can be calculated from the binary coded register value using the following formula:

$$\text{Decimal code} = (\text{Vin} / \text{LSB}_V) - 1$$

The temperature measurement on TEMP\_CL0-4 can be calculated from the binary coded register value using the following formula:

$$\text{Decimal code} = [(355 - T_j) / \text{LSB}_T] - 1$$

### 3.18 SW-Debug mode

The SW-Debug mode is intended for SW development. In SW-Debug mode, the watchdog is not started and consequently does not monitor proper watchdog trig.

To set the device in SW-DEBUG mode, the SWDBG pin must be shorted to VIO before a power-up sequence (cold-start or wake-up from DEEP-SLEEP). With such a setting, the device executes the power-up sequence and, instead of reaching REC-1 state, the device transits to SWDBG state.

In SWDBG state the timeout  $t_{\text{SWDBG\_TO}}$  is launch.

The timeout is used to prevent the system to be stuck in SWDBG state:

If the timeout expires, then SW-Debug mode entry is canceled. The device transits to REC-1 state and starts the watchdog with a long open window. The status register bit SWDBG\_VIO is set, an IRQ (maskable by MASK\_SWDBG\_VIO\_IRQ) is generated to indicate that the SWDBG pin is shorted to VIO.

If the short to VIO is removed before timeout expiration, then the device transitions to REC-1 state, and the watchdog is disabled. To transition to ACTIVE - FULL-POWER mode, the SW must clear error flags and set WD\_TRIG. This is the only access to WD\_TRIG that the SW must handle in SW-Debug mode.

Any further voltage attachment to the SWDBG pin at VIO is ignored, until the next SPSB100GS power-up sequence. This helps to protect against unwanted SW-Debug mode entry and enables possible sharing of this pin with other functions.

Once the SW-Debug mode is established, it persists until terminated via SPI command SWDBG\_EXIT or until the next power-on reset (battery unplug and replug). If terminated by SPI command, the watchdog starts immediately with a long open window.

The state of the SWDBG pin can be monitored by the live bit SWDBG\_STATE.

In the final application, it is possible to detect the hardware fault "SWDBG shorted to VIO" using the following procedure.

After the MCU boot-up, the SW shall read the SPSB100GS state. The expected state is REC-1. If the SWDBG pin is faultily shorted to VIO, then the device reaches SWDBG state.

In such a case it is possible to kill the timeout by setting the KILL\_SWDBG\_TIMEOUT control bit: the device transits to REC-1 state, the watchdog is enabled disregarding the SWDBG pin voltage.

This feature is useful to prevent an increase in the start-up time when the hardware fault "SWDBG shorted to VIO" is present.

Note: The purpose of SW-Debug mode is to develop software. This mode must not be used in the final application.

### 3.19 VREG

The VREG is dedicated to generating the bootstrap voltage for the Bucks in ACTIVE and REC-1 states. It is supplied by the FBB pin in ACTIVE - FULL-POWER and in ACTIVE - LOW-POWER.

VREG has a 3.3 V output.

VREG cannot be used to supply external blocks.

The voltage regulator is protected against undervoltage. If the VREG output voltage goes below  $V_{\text{VREG\_UV}}$  for a delay longer than  $t_{\text{VREG\_UV}}$ , flag INT\_REG\_UV is set and the device will execute a power-down sequence to enter DEEP-SLEEP state.

The voltage regulator is protected against overvoltage. If the VREG output voltage goes above  $V_{\text{VREG\_OV}}$  for a delay longer than  $t_{\text{VREG\_OV}}$ , flag INT\_REG\_OV is set and the device will execute a power-down sequence to enter DEEP-SLEEP state.

The voltage regulator is protected against a short to ground during INIT state. If the VREG output voltage is not able to reach  $V_{\text{VREG\_UV}}$  after  $t_{\text{VREG\_stup}}$ , flag INT\_REG\_UV is set and the device will make a transition to DEEP-SLEEP state.

Current limitation  $I_{\text{VREG\_CCmax}}$  of the regulator ensures fast charge of the external decoupling capacitor.

The output voltage is stable for ceramic load capacitors, see  $C_{\text{VREG}}$  in the [Table 62](#).

Warning temperature detection is managed by a local thermal sensor (flag is TW\_CL0).

Warning temperature detection generates an IRQ except if MASK\_CL0\_TW\_IRQ is set.

In case the device temperature exceeds the TSD\_CL0 threshold, the device executes a power-down sequence before entering REC-2 state.

### 3.20 Long duration timer (LDT)

The SPSB100GS has embedded a timer that allows to wake up the device after a set period (if configured as a wake-up source by SPI, bit LDT\_MODE) or to ascertain the time since the last power-down.

The configuration as a wake-up source can be done if SPI LDT\_CNT\_ENA = '0'.

LDT\_MODE, LDT\_CNT\_THR[4:0], LDT\_CNT\_THR\_MSB\_POS[4:0] thresholds can be set, otherwise the configuration is locked.

The threshold configuration is done by two 5-bit registers:

- LDT\_CNT\_THR[4:0]: configure LDT threshold (locked when LDT\_CNT\_ENA =1)
- LDT\_CNT\_THR\_MSB\_POS[4:0]: select LDT threshold MSB position from 23 to 4 (bigger or smaller values are clamped) (locked when LDT\_CNT\_ENA =1)

Starting from the theoretical requested threshold (THEO\_LDT\_CNT\_THR):

- $LDT\_CNT\_THR\_MSB\_POS = INT(LN(THEO\_LDT\_CNT\_THR) / LN(2))$ 
  - INT() = Integer part of
  - LN() = Natural logarithm of
  - $LN(X) / LN(2)$  corresponds to the logarithm in base 2 of X.  $LN(2) = 0.693$
- $LDT\_CNT\_THR = INT((THEO\_LDT\_CNT\_THR / (2^{(LDT\_CNT\_THR\_MSB\_POS - 4)} + 0.5))$
- If, in some use cases, LDT\_CNT\_THR is higher than 31, LDT\_CNT\_THR must be clamped at 31

Example for a duration of 15 days:

- $THEO\_LDT\_CNT\_THR = 1,296,000 \text{ seconds} = 15 \times 24 \times 3600 \text{ seconds}$
- $LDT\_CNT\_THR\_MSB\_POS = INT(LN(THEO\_LDT\_CNT\_THR) / LN(2)) = 20$
- $LDT\_CNT\_THR = INT((THEO\_LDT\_CNT\_THR / (2^{(LDT\_CNT\_THR\_MSB\_POS - 4)} + 0.5)) = 20$
- So,
  - LDT\_CNT\_THR\_MSB\_POS = 20
  - LDT\_CNT\_THR = 20
  - LDT counts for 1,310,720 seconds. So, an error of 4.1 hours over 15 days = an error of 1.1%

The LDT (long duration timer) is a 24-bit timer that can be enabled or disabled by SPI bits LDT\_ENA and LDT\_CNT\_ENA. When the LDT is enabled, the live status bit LDT\_RUNNING is set high until the timer expires.

In the DEEP-SLEEP state all analog and digital blocks of the SPSB100GS are OFF except for the LDT counter when it is enabled.

To exit the DEEP-SLEEP state, two different cases can be considered:

- the LDT wake-up threshold value is reached
- another wake-up source is detected

In the first case, the MCU can read flag LDT\_WAKE by SPI, SPSB100GS leaves the DEEP-SLEEP state starting a power-on sequence.

In the second case, if the device is woken up by another wake-up source, the MCU can read wake-up flags by SPI and can read time elapsed since last LDT activation. To obtain a stable value, long duration timer elapsed time has to be latched by setting CR bit LDT\_TIMER\_READ\_ENA high and the counted value is written in a read-only register LDT\_TIMER\_VALUE[23:0].

Elapsed time is counted as soon the LDT\_ENA = 1 and LDT\_CNT\_ENA = 1. For example, if the MCU wants to measure the elapsed time value from the last DEEP-SLEEP, the MCU has to activate LDT by writing '1' in the LDT\_ENA and LDT\_CNT\_ENA, and then initiate a power-down cycle.

In case the MCU needs to stop the counter, it must set LDT\_CNT\_ENA = 0. In any case, the status of the counter is held inside the status register (LDT\_TIMER\_VALUE[23:0]). The counter is reset as soon as LDT\_CNT\_ENA is set to '1'.

The LDT\_DEBUG bit could be set to '1' to speed up the counter by a factor of 100x for debug purposes (10 ms steps, instead of 1 s).

## 4 Protection, diagnosis and monitoring signals

### 4.1 Supply monitoring

#### 4.1.1 VS pin

The battery line is monitored through the VS pin.

The VS input voltage is monitored through analog comparators and the ADC:

- VS input voltage can be read back by SPI access, by VS[9..0].
- The ADC is used to detect early undervoltage warnings (flagged by VS\_UV\_EW bit).

The thresholds are programmable by SPI (VS\_UV\_EW\_TH[4..0]) and an interrupt is issued when thresholds are crossed except if MASK\_VS\_EW\_IRQ is set.

#### 4.1.2 FBB pin

The FBB input voltage is monitored through analog comparators and the ADC:

- An analog comparator is used to detect over- and undervoltages. The reaction to a FBB voltage fault is described in [Section 3.6.2.6](#).
- An analog comparator is used to detect overvoltage. Flag is FBB\_OV and generates an IRQ except if MASK\_FBB\_OV\_IRQ is set. State machine executes a power-down sequence to enter REC-2.
- An analog comparator is used to detect undervoltage. Flag is FBB\_UV and generates an IRQ except if MASK\_FBB\_UV\_IRQ is set. State machine executes a power-down sequence to enter REC-2.
- The ADC is used to detect overvoltage early warnings (flagged by FBB\_OV\_EW bit).
- The ADC is used to detect undervoltage early warnings (flagged by FBB\_UV\_EW bit).
- The thresholds are programmable by SPI (FBB\_OV\_EW\_TH[3..0]) and an interrupt is issued when thresholds are crossed except if MASK\_FBB\_OV\_EW\_IRQ is set.
- The thresholds are programmable by SPI (FBB\_UV\_EW\_TH[3..0]) and an interrupt is issued when thresholds are crossed, except if MASK\_FBB\_UV\_EW\_IRQ is set.
- The result of ADC conversion is also readable back via SPI, by FBB[9..0]

#### 4.1.3 VIO pin

The VIO voltage is monitored through an analog comparator and digital communication is blocked if VIO voltage is below  $V_{VIO\_UV}$  threshold for a delay longer than  $T_{F\_VIO\_UV}$  (flag is VIO\_UV bit).

### 4.2 Regulators output voltage protection

The Buck1, 2, 3 and LDO2 outputs are monitored through analog comparators to detect over- and undervoltages. (through BUCKx\_UV, BUCKx\_OV, LDO2\_UV and LDO2\_OV bits). The reaction to a fault is described in [Section 3.6.2.5](#). In addition, LDO2 is also turned OFF when the tracked regulator is turned OFF in reaction to a fault.

When a regulator is turned ON, by SPI or power-up sequence, a short to ground is detected if the output voltage does not reach the power-good threshold in the timeout period (BUCKx\_PG\_TIMEOUT bit), in such a case the regulator is switched OFF.

In addition, when turned ON through the SPI, an interrupt is generated as soon as their output voltage reaches the power-good threshold (BUCKx\_PG and LDO2\_PG bits).

Latent fault detection of OV, UV, PG analog comparators is ensured by Analog-BIST.

Latent fault of regulator monitor digital controller is ensured by Digital-BIST.

### 4.3 Boost and bypass $V_{ds}$ monitoring

The BOOST driver includes a comparator to monitor the voltage drop across the boost external transistor. The voltage is monitored between the DLB and CANGND pins.

The monitor issues a fault (whose threshold is set by BOOST\_DSMON\_TH[2..0] bits) if the monitored voltage is above the programmed threshold for five consecutive periods of the BOOST PWM signal.

When a fault is detected (flag is BOOST\_VDSMON\_ERROR), an interrupt is sent on the IRQ pin (except if it is masked by MASK\_BOOST\_VDSMON\_IRQ) and the boost external transistor is permanently turned OFF. MCU shall read and clear the status flag to turn the boost driver back ON.

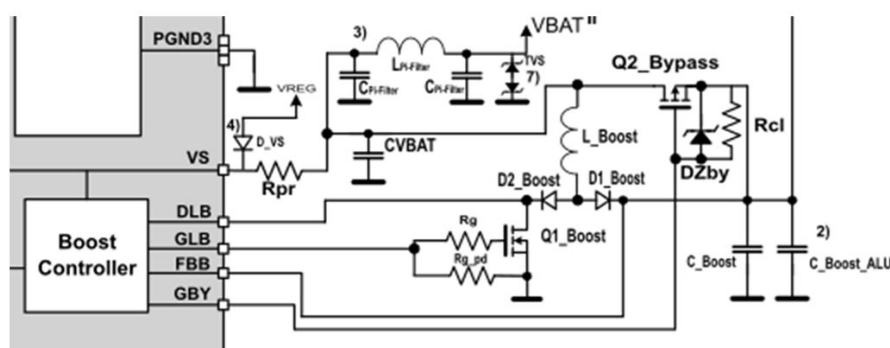
The BYPASS driver includes a comparator to monitor the voltage across the bypass external transistor. this comparator is enabled as soon as BYPASS is switched ON with a digital blanking time,  $t_{B\_BYPASS\_VDSM}$ . The voltage is monitored between the VS and FBB pins.

The monitor issues a fault if the monitored voltage is above the programmed threshold (BYPASS\_DSMON\_TH[2..0] bits) for a delay longer than  $t_{F\_BYPASS\_VDSM}$ .

When a fault is detected (flag is `BYPASS_VDSMON_ERROR`), an interrupt is sent on the `IRQ` pin (except if it is masked by `MASK_BYPASS_VDSMON_IRQ`), the `BYPASS` external transistor is switched off.

Latent fault detection of comparators is ensured by Analog-BIST.

**Figure 36. Boost and bypass  $V_{ds}$  monitoring (extracted by application scheme)**



#### 4.4 Boost activity monitoring

In ACTIVE – FULL-POWER and in REC-1 states, the BOOST activity can be monitored by the deactivation of the bypass with the live bit BYPASS STATUS = 0.

In ACTIVE – LOW-POWER state, a flag BOOST\_IN\_LP is set and an interrupt is generated though the IRQ pin (except if it is masked by MASK\_BOOST\_IN\_LP\_IRQ) when the BOOST starts to switch.

In other states the BOOST is disabled.

#### 4.5 WU and IGN monitoring

WU and IGN voltages can be measured through the ADC and values read back via SPI (WU[9..0] and IGN[9..0]).

## 4.6 Ground pin monitoring

Analog comparators are cross-monitoring the voltage on the three ground pads CAN-GND (bonded to CANGND pin), Analog-GND and Digital-GND (both bonded to SGND pin).

If at least one ground pad is electrically disconnected from the PCB ground plane with a level above  $V_{\text{Gnd\_Loss\_th}}$ , then a ground loss is detected (GNDLOSS) after  $t_{\text{Gnd\_Loss\_Filter}}$  and the reaction is described in [Section 4.8](#).

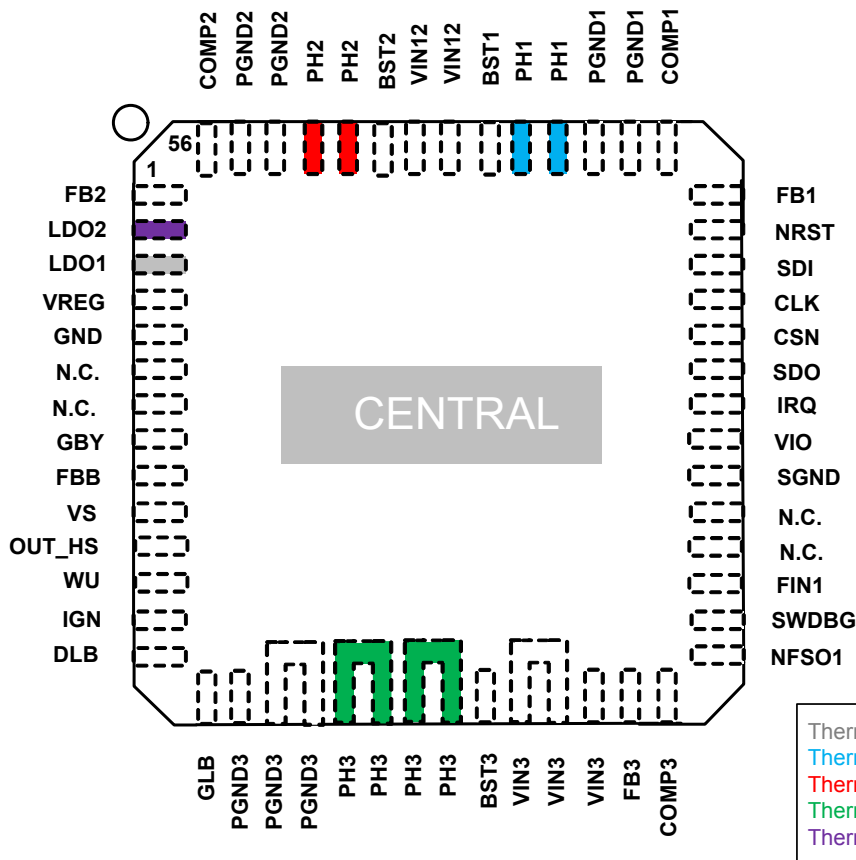
Latent fault detection of ground comparators is ensured by Analog-BIST.

## 4.7 Temperature monitoring

In order to provide advanced on-chip temperature control, the power outputs are grouped in clusters with dedicated thermal sensors. The sensors are suitably located on the device.

If the temperature of a cluster reaches the thermal warning threshold, then a dedicated status flag (TW\_CLx bit) is set and an interrupt is issued.

If the temperature of a cluster reaches the thermal shutdown threshold, then a dedicated status flag is set, the outputs assigned to that cluster are shut down and depending on their configuration bit REGFAIL\_GO\_REC all outputs are shut down or not as described in [Section 3.6.2.5](#).

**Figure 37. Thermal cluster identification**

**Table 10. Thermal cluster definition**

| Th_CL0               | Th_CL1                 | Th_CL2                 | Th_CL3                 | Th_CL4                 |
|----------------------|------------------------|------------------------|------------------------|------------------------|
| LDO1, central        | BUCK1                  | BUCK2                  | BUCK3                  | LDO2                   |
| TW digitally managed | TW and TSD             | TW and TSD             | TW and TSD             | TW and TSD             |
| TSDC analog managed  | Both digitally managed | Both digitally managed | Both digitally managed | Both digitally managed |

Cluster temperatures are converted through the ADC and readable by SPI (through TEMP\_CLx[9..0] bits), only in ACTIVE - FULL-POWER mode

**Note:** In DEEP-SLEEP state, all clusters are disabled.

**Note:** In ACTIVE - LOW-POWER state, all clusters are disabled, except Th\_CL0 to detect TSDC.

Thermal clusters are monitored through the ADC. Central thermal clusters T<sub>SDC</sub> is ensured by an analog comparator.

Latent fault detection of TSDC thermal comparator is covered by an Analog-BIST.

Latent fault detection of thermal monitor and ADC digital controllers are covered by a Digital-BIST.

## 4.8 HW low-level monitors

The SPSB100GS integrates asynchronous monitors of low-level blocks in ACTIVE - FULL-POWER mode and REC-1 state:

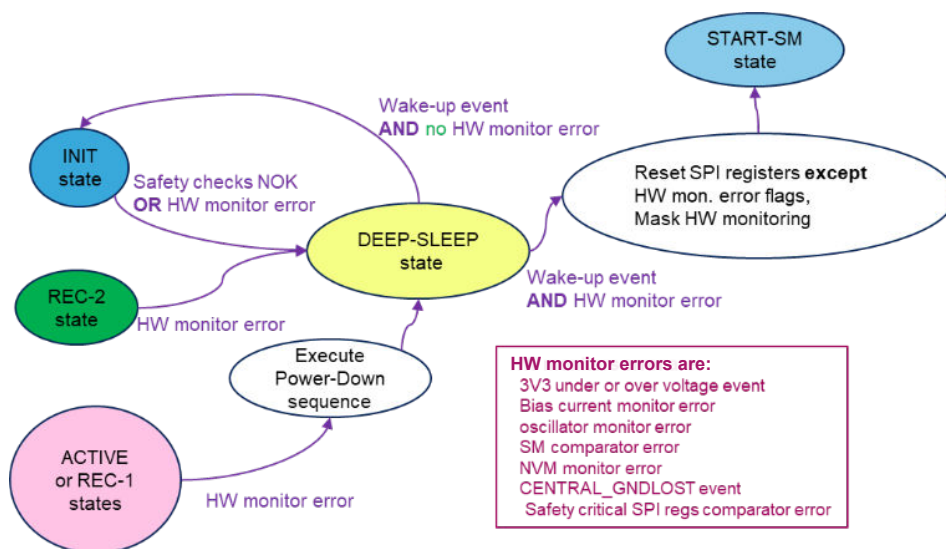
- voltage differences between main and monitoring digital and analog power supplies (INT\_REG\_UV, INT\_REG\_OV bits).
- current differences between main and monitoring current sources (CURRENT\_MISMATCH bit).

and synchronous monitors of

- frequency difference between main and redundant oscillators (OSC\_ERROR bit).
- state Machine's state by comparison of main and redundant state machine(FSM\_COMP\_ERROR bit).
- NVM data by
  - comparison of NVM data and redundant registers (NVM\_COMP\_ERROR bit).
  - CRC check at NVM download (NVM\_CRC\_ERROR bit).
- Safety critical SPI registers by comparison of main and redundant registers (SPI\_REG\_COMP\_ERROR bit generates an IRQ except if MASK\_SPI\_ERROR\_IRQ is set).
- Ground loss connection by cross-checking ground domains (GNDLOSS bit).

A fault detected by low-level monitors triggers a power-down sequence and the SPSB100GS reaches the DEEP-SLEEP state. In such a situation, after a wake-up event (except for OSC\_ERROR where the SPSB100GS will restart automatically if oscillators recover their frequencies), all SPI registers are reset except HW low-level monitor flags and the SPSB100GS transitions to START-SM state.

**Figure 38. SPSB100GS HW low-level monitors**



## 4.9 Communication interface

The SPI communication protocol embeds the following safety mechanisms:

- A 4-bit CRC SPI\_CRC\_ERR is set in case of error detected, and an IRQ is generated except if MASK\_SPI\_ERROR\_IRQ is set.
- Clock monitor: During communication (CSN low phase), a clock monitor counts the valid CLK edges. If the CLK edges do not correlate with the SPI data length then SPI\_CLK\_CNT is set, an IRQ is generated except if MASK\_SPI\_ERROR\_IRQ is set, the actual communication is rejected.
- CLK phase check: To verify that the CLK phase of the SPI master is set correctly, a special device information register is implemented. When reading this register (Address: 20H), the data must be 55H. In case AAH is read, the CPHA setting of the SPI master is wrong and proper communication cannot be guaranteed.
- CSN timeout: If CSN is set low for  $t > t_{CSNfail}$ , then the frame is rejected and SDO is released to tri-state (SPI\_CSN\_TIMEOUT is set). An IRQ is generated except if MASK\_SPI\_ERROR\_IRQ is set.
- SDI stuck at high detection: An SPI frame consisting of all bits '1' is detected as failure and will be rejected, SPI\_SDI\_STUCK\_HIGH is set and an IRQ is generated except if MASK\_SPI\_ERROR\_IRQ is set.
- SDI stuck at low detection: An SPI frame consisting of all bits '0' is detected as failure and will be rejected, SPI\_SDI\_STUCK\_LOW is set and an IRQ is generated except if MASK\_SPI\_ERROR\_IRQ is set.
- SDO stuck: The Global Status Byte (GSB) is transmitted within every SPI frame; the definition of the GSB guarantees that a content of all '1' or all '0' is not possible; therefore, the microcontroller can identify if the SDO signal is stuck at a high or low level.
- Functional safety-relevant configuration registers are locked by a dedicated bit SPI\_PROTECT\_ACCESS. A first SPI command must be sent to un-protect the functional safety-relevant registers, then a further SPI command is sent to modify those configuration registers.
- SPI undefined address access is detected by a dedicated bit SPI\_UNDEF\_ADD. An IRQ is generated except if MASK\_SPI\_ERROR\_IRQ is set.
- SPI unwanted write access on a status register is detected by a dedicated bit SPI\_STATUS\_WRT. An IRQ is generated except if MASK\_SPI\_ERROR\_IRQ is set.
- SPI unwanted access during LBIST test is detected and SPI\_LBISTED is set. An IRQ is generated except if MASK\_SPI\_ERROR\_IRQ is set. In this case, the SPI frame is rejected.
- Functional safety-relevant configuration registers are duplicated and a runtime comparison mechanism checks the coherency of their data. In case of error, the reaction is described in chapter [Section 4.8](#).

Latent fault detection of SPI digital handler, functional safety redundant configuration register, and comparison mechanism are covered by a Digital-BIST.

## 4.10 IRQ pin monitoring

To check that the IRQ line is properly connected to the MCU, an IRQ can be sent to the MCU through an SPI request.

When the MCU sets the SPI bit IRQ\_REQUEST, an interrupt is generated on the IRQ pin.

The MCU can verify that the IRQ has been sent correctly by checking the IRQ\_SENT status bit. The IRQ pin shall be set high after read & clear of the IRQ\_SENT flag.

To detect IRQ stuck high fault, the device embeds

- an echo signal of the IRQ pin: IRQ\_ECHO live bit in the status register.
- an echo error detection mechanism: IRQ\_ECHO\_ERROR status bit is set if the device detects an IRQ\_ECHO high signal when the IRQ pin is asserted low after a filter time  $T_{IRQ\_ECHO\_FILT}$ .

## 4.11 NRST pin monitoring

To detect an NRST stuck high fault, the device embeds

- an echo signal of the NRST pin: NRST\_ECHO live bit in status register.
- an echo error detection mechanism: NRST\_ECHO\_ERROR status bit is set if the device detects an NRST\_ECHO high signal when the NRST pin is asserted low after a filter time  $T_{NRST\_ECHO\_FILT}$ .

## 4.12 NFSO1 pin monitoring

To detect an NFSO1 stuck high fault, the device embeds:

- an echo signal of the NFSO1 pin: NFSO1\_ECHO live bit in status register.
- an echo error detection mechanism: NFSO1\_ECHO\_ERROR status bit is set if the device detects an NFSO1\_ECHO high signal when the NFSO1 pin is asserted low, after a filter time  $T_{NFSO\_ECHO\_FILT}$  and an interrupt is sent to the IRQ pin, except if MASK\_NFSO1\_ECHO\_ERROR\_IRQ is set.

#### 4.13 Watchdog block monitoring

To detect an improper turn-OFF of the watchdog feature, the device embeds:

- An echo signal of the watchdog block enable signal: WD\_ENA\_ECHO live bit in the status register.
- An echo error detection mechanism: WD\_ENA\_ECHO\_ERROR status bit is set if the device detects that the watchdog block is turned OFF while the device is not in SW-Debug mode, and an interrupt is sent to the IRQ pin, except if MASK\_WD\_ENA\_ECHO\_ERROR\_IRQ is set.

#### 4.14 FCCU block monitoring

To detect an improper turn OFF of the FCCU monitor feature, the device embeds

- an echo signal of the FCCU monitor block enable signal: FCCU\_ENA\_ECHO live bit in status register.
- an echo error detection mechanism: FCCU\_ENA\_ECHO\_ERROR status bit is set if the device detects that the FCCU monitor block is turn OFF in ACTIVE state, when FCCU\_ENA has been set and an interrupt is sent to the IRQ pin, except if MASK\_FCCU\_ENA\_ECHO\_ERROR\_IRQ is set.

#### 4.15 Analog BIST

ABIST is performed on SPI request.

ABIST is not run on blocks that are turned OFF. The MCU shall ensure the proper turn-on of a block when its ABIST is expected to be run.

ABIST covers latent fault detection of:

- OV, UV, PG analog comparators.
- Internal voltage and current supplies monitor.
- Central thermal monitor.
- BOOST and BYPASS VDS monitors.

ABIST must be run only in ACTIVE - FULL-POWER mode by the MCU through the SPI, after any regulator enable request waiting for PG flag (e.g. after ACTIVE-LP to ACTIVE-FP transition). The MCU shall write the ABIST bit to request its execution (only after SPI\_PROTECT\_ACCESS has been set).

After  $T_{ABIST}$ , ABIST is finished, the status bit ABIST\_COMPLETE is set and an interrupt is sent to IRQ pin.

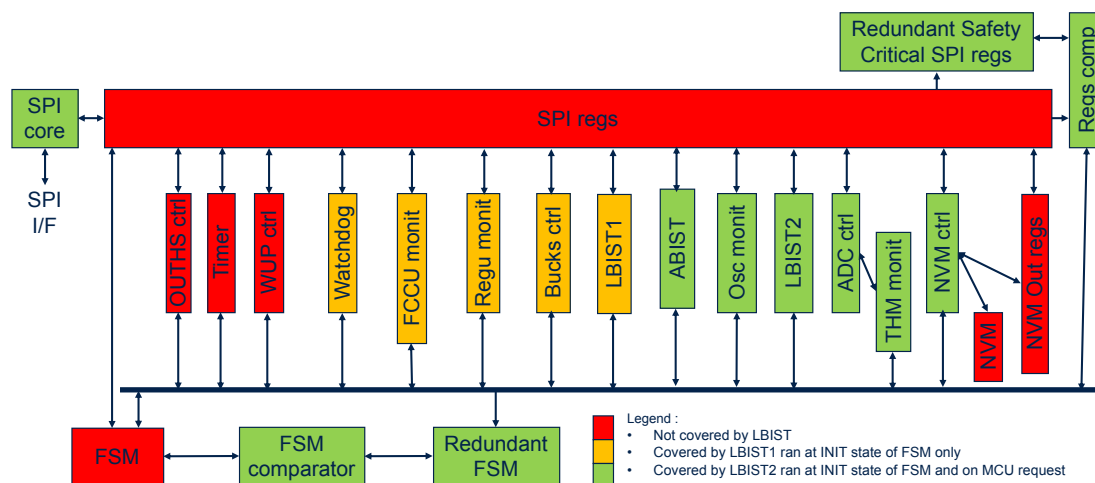
ABIST\_ERROR is set in case an error is detected.

For boost VDSM monitoring, to avoid a false ABIST error, a status bit ABIST\_BOOST\_IGNORED will be set at 1 if the ABIST request is made during boost PWM activity.

#### 4.16 Logic BIST

The SPSB100GS integrates two logic BIST:

- LBIST1 is performed in INIT state only
- LBIST2 is performed in INIT state and on SPI request

**Figure 39. Logic BIST**


LBIST2 must be run only in ACTIVE - FULL-POWER mode by the MCU through the SPI. The MCU shall write the LBIST bit to request its execution (only after SPI\_PROTECT\_ACCESS has been set).

**Note:** *LBIST2 must be run in a time window from 4.5 to 5.2 ms after a request to transit from ACTIVE-LOW-POWER to ACTIVE-FULL-POWER. If LBIST2 is requested outside this time window, a random fault can occur and send the device in DEEP\_SLEEP due to a wrong NVM\_COMP\_ERROR flag.*

After  $T_{LBIST}$ , the LBIST2 is finished, the status bit LBIST\_COMPLETE is set and an interrupt is sent to the IRQ pin.

LBIST\_ERROR\_1 is set in case an LBIST2 error is detected.

SPSB100GS does not take any action in case an LBIST2 error is detected. It is the duty of the MCU to properly react to a signaled error.

An LBIST error detected in INIT state is considered as a safety check error, see Chapter [Section 4.17](#).

Fault management while LBIST is executed:

- When LBIST2 is executed on demand in ACTIVE - FULL-POWER, the faults (UV, OV, TSD...) processed by the blocks under LBIST2 are not masked. If a fault occurs, the LBIST2 is stopped, the status bit LBIST\_STOPPED is set, an IRQ is generated, and the fault is processed by the SPSB100GS with appropriate reaction.
- An SPI access is considered as a fault: the SPI command is disregarded and the fault is handled as described above.
- As a consequence, the watchdog window must be properly set before requesting an LBIST2 execution to allow the LBIST2 to complete before the next watchdog trig through the SPI.

## 4.17 Safety checks

In the INIT state, the following safety checks are performed:

- digital LBIST
- ground pin monitor.
- NVM checks: CRC and U-PROG value.

In case of error, the state machine transitions to DEEP-SLEEP, where the device can be woken up to INIT state, where safety checks are run again.

## 4.18 NVM integrity monitor

To detect an improper turn OFF of NVM monitor feature, the device embeds a live bit NVM\_COMPARE\_ENA\_STATUS to check NVM monitor block enable signal. This status bit is valid only in ACTIVE - FULL-POWER mode. The reaction of the NVM monitor feature in case of error is described in [Section 4.8](#).

## 5 Serial peripheral interface (SPI)

A 32-bit SPI is used for bidirectional communication with the microcontroller.

The microcontroller SPI peripheral shall be configured with CPOL = 0 and CPHA = 0. SDI input data is sampled by the CLK rising edge, and SDO output data is updated on the CLK falling edge.

This device is not limited to a microcontroller with a built-in SPI peripheral, but three CMOS-compatible output pins and one input pin may be used to communicate with the device. A fault condition can be detected by setting CSN to low. In such a condition, the SDO pin reflects the global error flag GSBN of the device.

- **Chip select not (CSN)**  
The CSN input pin is used to select the serial interface of this device. When CSN is high, the output pin SDO is in a high impedance state. CSN low activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame. If CSN is low for  $t > t_{CSNfail}$ , the SDO output will be switched back to high impedance to avoid blocking the signal line and allow other SPI nodes to drive the bus.
- **Serial data in (SDI)**  
The SDI input pin is used to transfer data into the device. The data applied to SDI are sampled at the rising edge of the CLK signal and shifted into an internal 32-bit shift register. At the rising edge of the CSN signal, the content of the shift register is transferred to the data input register. The writing to the selected data input register is enabled if exactly 32 bits are transmitted within one communication frame (that is, CSN low). If more or fewer clock pulses are counted within one frame, the complete frame is ignored and an SPI error is signaled. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame. Due to this safety functionality, daisy-chaining of the SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.
- **Serial data out (SDO)**  
The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global error flag GSBN. The first rising edge of the CLK input after a high-to-low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out. As SDO is in high impedance when CSN is high, it is possible to link several SPI target devices that respect this rule with a dedicated CSN line for each SPI target.
- **Serial clock (CLK)**  
The CLK input is used to synchronize the input and output bit streams. The data input (SDI) is sampled at the rising edge of the CLK and the data output SDO is updated on the falling edge of the CLK signal.

### 5.1 ST SPI

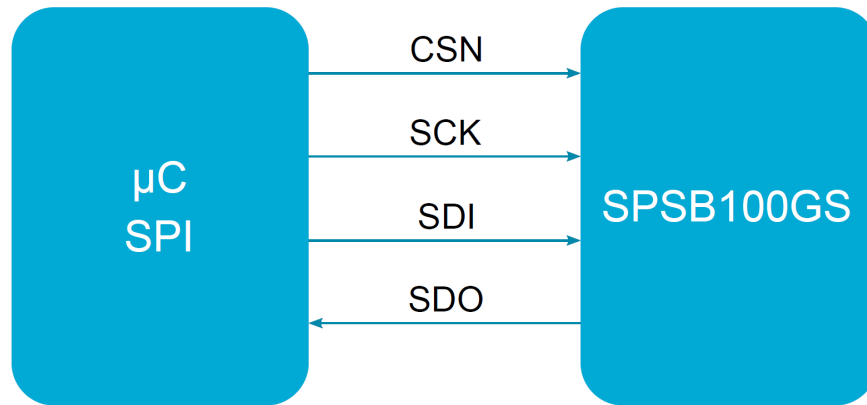
The ST-SPI is a standard used in ST Automotive ASSP devices.

This chapter describes the SPI protocol. It defines a common structure of the communication frames and defines specific addresses for product and status information.

The ST-SPI allows usage of generic software to operate the devices while maintaining the required flexibility to adapt them to the individual functionality of a particular product. In addition, safety mechanisms are implemented to protect the communication from external influences and incorrect or unwanted usage.

### 5.1.1 Physical Layer

Figure 40. SPI pin description



## 5.2 Signal description

### Chip select not (CSN)

The communication interface is deselected when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame has been sent. At CSN falling and rising edges, the serial clock (CLK) has to be logically low. The serial data out (SDO) is in high impedance when CSN is high or a communication timeout is detected.

### Serial clock (CLK)

CLK provides the clock of the SPI. Data present at serial data input (SDI) are latched on the rising edge of the serial clock (CLK) into the internal shift registers, while on the falling edge data from the internal shift registers are shifted out to serial data out (SDO).

### Serial data input (SDI)

This input is used to serially transfer data into the device. Data is latched on the rising edge of the serial clock (CLK).

### Serial data output (SDO)

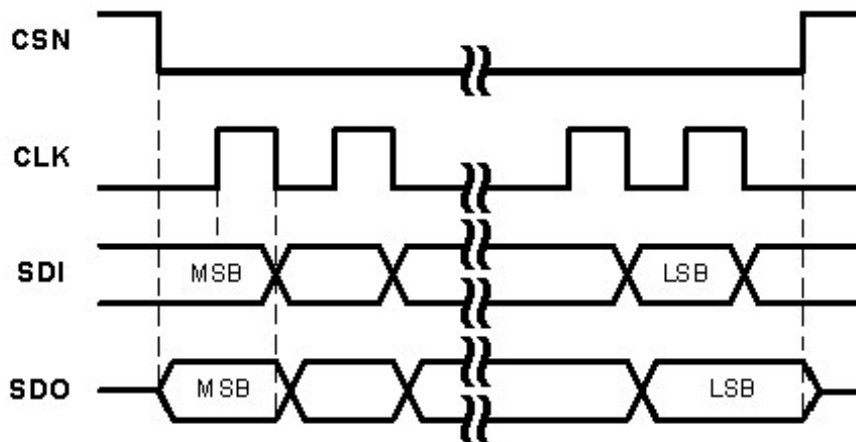
This output signal is used to serially transfer data out of the device. Data is shifted out on the falling edge of the serial clock (CLK).

### 5.2.1 Clock and data characteristics

The ST-SPI can be driven by a microcontroller with its SPI peripheral running in the following modes:

- CPOL = 0
- CPHA = 0

Figure 41. SPI signal description



The communication frame starts with the falling edge of the CSN (communication start). CLK has to be low. The SDI data is then latched at all following CLK rising edge into the internal shift registers.

After communication start, the SDO leaves the high impedance state and presents the MSB of the data shifted out to the SDO. At all following CLK falling edge, data is shifted out through the internal shift registers to SDO.

The communication frame is finished with the rising edge of CSN. If a valid communication took place, the requested operation according to the operating code is performed.

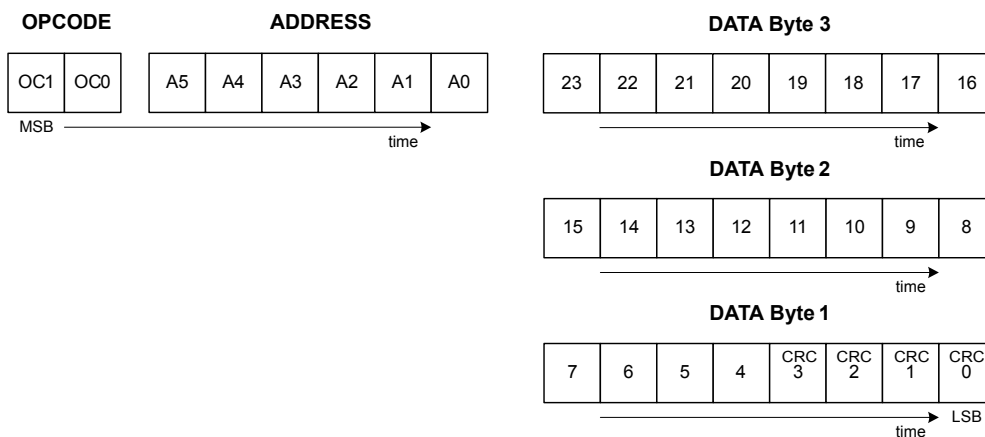
## 5.2.2

### Communication protocol

#### SDI frame

The device data-in frame consists of 32 bits (OpCode (2 bits) + address (6 bits) + data (20 bits) + CRC (4 bits)). The first two received bits (MSB, MSB-1) contain the operation code which indicates the instruction to be performed. The following 6 bits (MSB-2 to MSB-7) represent the address on which the operation is performed. The subsequent bytes contain the payload.

Figure 42. SDI frame



#### Operation code

The operating code is used to distinguish among different access modes to the registers of the target device.

Table 11. Operation codes

| OC1 | OC0 | Description     |
|-----|-----|-----------------|
| 0   | 0   | Write operation |

| OC1 | OC0 | Description              |
|-----|-----|--------------------------|
| 0   | 1   | Read operation           |
| 1   | 0   | Read and clear operation |
| 1   | 1   | Read device information  |

A **Write operation** leads to a modification of the addressed data by the payload if a write access is allowed (for example, control register, valid data). Besides this, a shift out of the content (data present at *communication start*) of the same register is performed.

A **Read operation** shifts out the data present in the addressed register at *communication start*. The SDI payload data is ignored and internal data will not be modified. Burst read cannot be performed. Even if the first 8 bits of SDO are sent during read device information, the chip must receive a full frame with CRC on SDI, otherwise a SPI\_CLK\_CNT and a SPI\_CRC\_ERR will be set generating a SPIE.

A **Read and clear operation** will lead to clearing of addressed status bits. The bits to be cleared are defined first by address, second by payload data bits set to '1'. Besides this, a shift out of the content (data present at *communication start*) of the same register is performed.

Note:

*Status registers which change status during communication could be cleared by the actual Read and clear operation and are neither reported in actual communication nor in the following communications. To avoid a loss of any reported status, it is recommended to clear status registers which have been read in the previous communication (selective bitwise clear).*

#### Advanced Operation Code

A 'clear all status registers' command is performed when an OpCode '10' at address b'111111 is performed.

#### Data-In payload

The *payload* (data bits) is the data transferred to the device within every SPI communication. The *payload* always follows the OpCode and the address bits.

For write access, the *payload* represents the new data written to the addressed register. For *Read and clear* operations, the *payload* defines which bits of the addressed status register will be cleared. In case of a '1' at the corresponding bit position, the bit will be cleared.

For a *Read operation*, the SDI *payload* is not used. For functional safety reasons, it is recommended to set the unused *payload* to '0'.

#### SDO frame

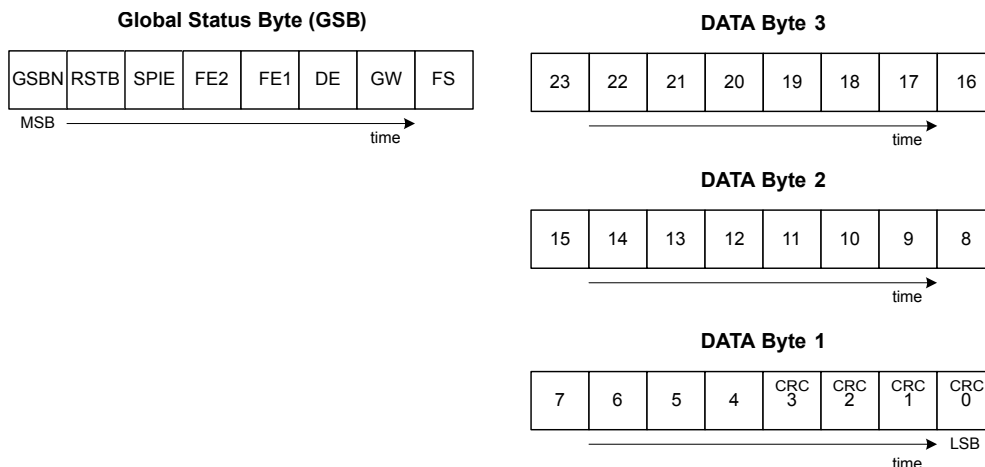
The data-out frame consists of 32 bits (GSB + data bits + CRC).

The first eight transmitted bits contain device related status information (GSB) and are latched into the shift register at the time of the *communication start*. These 8 bits are transmitted at every SPI transaction.

The subsequent bytes contain the payload data together with the four LSB bits containing CRC and are latched into the shift register with 32 falling clock edges for the total SPI frame.

This could lead to an inconsistency in data between the GSB and *payload* due to different shift register load times. However, no unwanted status register clear should appear, as status information should just be cleared with a dedicated bit clear after.

Figure 43. SDO frame



### Global Status Byte (GSB)

Bits 0 to 5 represent a logical OR combination of bits located in the status registers. Therefore, no direct Read and clear can be performed on these bits inside the GSB.

Table 12. Global status byte

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| GSBN  | RSTB  | SPIE  | RES   | FE1   | DE    | GW    | FS    |

- Global status bit not (GSBN)**  
 The GSBN is a logical NOR combination of bit 0 to bit 6. This bit can also be used as a *global status flag* without starting a complete communication frame as it is present directly after pulling CSN low. OUTHS open load can be masked in GSBN by setting bit MASK\_OL\_GSB. Global warning can be masked in GSBN by setting bit MASK\_GW\_GSB.
- Reset bit (RSTB)**  
 The RSTB indicates an SPSB100GS reset. In case this bit is set, all internal control and status registers are set to default. The RSTB bit is cleared after a *Read and clear* of the VPOR bit in the *status registers* which caused the reset event.
- SPI error (SPIE)**
- Functional error 1 (FE1)**  
 The FE1 is a logical OR combination of errors coming from functional blocks.
- Device error (DE)**  
 The DE is a logical OR combination of errors related to device-specific blocks.
- Global warning (GW)**  
 The GW is a logical OR combination of warning flags (for example, thermal warning). Thermal warning can be masked in GW by setting bit MASK\_TW\_GW.
- Fail-safe (FS)**  
 The FS bit indicates that the device was forced into a safe state due to mistreatment or critical internal errors (for example, watchdog failure, voltage regulator failure).

### Data-Out payload

The data-out *payload* (20 data bits + 4 CRC bits) is the data transferred from the target device within every SPI communication to the controller device.

### 5.2.3 Address definition

**Table 13. RAM and ROM address range**

| Operation code |     |                                                             |
|----------------|-----|-------------------------------------------------------------|
| OC1            | OC0 | Description                                                 |
| 0              | 0   | Write operation, allowed for RAM control registers          |
| 0              | 1   | Read operation, allowed for RAM status or control registers |
| 1              | 0   | Read and clear operation, allowed for RAM status registers  |
| 1              | 1   | Read device information in ROM registers                    |

**Table 14. RAM address**

| RAM address | Description         | Access |
|-------------|---------------------|--------|
| 3FH         | Special OpCode      | R/W    |
| ...         | -                   | -      |
| 32H         | Status register 18  | R/C    |
| ...         | ...                 | -      |
| 22H         | Status register 2   | R/C    |
| 21H         | Status register 1   | R/C    |
| ...         | ...                 | -      |
| 1CH         | Control register 28 | R/W    |
| ...         | ...                 | -      |
| 02H         | Control register 2  | R/W    |
| 01H         | Control register 1  | R/W    |
| 00H         | Reserved            | -      |

**Table 15. ROM address**

| RAM address | Description     | Access |
|-------------|-----------------|--------|
| ...         | -               | -      |
| 3EH         | <GSB Options>   | R      |
| ...         | -               | -      |
| 20H         | <SPI CPHA test> | R      |
| ...         | -               | -      |
| 15H         | <WD bit pos. 3> | R      |
| 14H         | <WD bit pos. 2> | R      |
| 13H         | <WD bit pos. 1> | R      |
| 12H         | <WD Type 2>     | R      |
| 11H         | <WD Type 1>     | R      |
| 10H         | <SPI mode>      | R      |
| ...         | -               | -      |
| 0AH         | <Silicon Ver.>  | R      |
| ...         | -               | -      |
| 05H         | <Device No.4>   | R      |

| RAM address | Description     | Access |
|-------------|-----------------|--------|
| 04H         | <Device No.3>   | R      |
| 03H         | <Device No.2>   | R      |
| 02H         | <Device No.1>   | R      |
| 01H         | <Device Family> | R      |
| 00H         | <Company Code>  | R      |

### Device information registers

The *device information registers* can be read by using the OpCode '11'. After shifting out the GSB, the 8-bit wide payload will be transmitted. By reading *device information registers*, a communication width of 32 bits can be used. After shifting out the GSB followed by the 8-bit wide payload, a series of '0' is shifted out at the SDO.

**Table 16. Information registers map**

| ROM address | Description     | Access | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0                                                        |
|-------------|-----------------|--------|-------|-------|-------|-------|-------|-------|-------|--------------------------------------------------------------|
| ...         |                 |        |       |       |       |       |       |       |       |                                                              |
| 3EH         | <GSB Options>   | R      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0                                                            |
| ...         |                 |        |       |       |       |       |       |       |       |                                                              |
| 20H         | <SPI CPHA test> | R      | 0     | 1     | 0     | 1     | 0     | 1     | 0     | 1                                                            |
| ...         |                 |        |       |       |       |       |       |       |       |                                                              |
| 15H         | <WD bit pos. 3> | R      |       |       |       |       |       |       |       | 00H                                                          |
| 14H         | <WD bit pos. 2> | R      |       |       |       |       |       |       |       | C0H                                                          |
| 13H         | <WD bit pos. 1> | R      |       |       |       |       |       |       |       | 44H                                                          |
| 12H         | <WD Type 2>     | R      |       |       |       |       |       |       |       | 91H                                                          |
| 11H         | <WD Type 1>     | R      |       |       |       |       |       |       |       | Watchdog long open window<br>(refers to watchdog definition) |
| 10H         | <SPI mode>      | R      |       |       |       |       |       |       |       | 32H                                                          |
| ...         |                 |        |       |       |       |       |       |       |       |                                                              |
| 0AH         | <Silicon Ver.>  | R      |       |       |       |       |       |       |       | Major revision      Minor revision                           |
| ...         |                 |        |       |       |       |       |       |       |       |                                                              |
| 06H         | <Device No.5>   | R      |       |       |       |       |       |       |       | 00H: <b>SPSB100GS</b><br>01H: <b>SPSB100GBS</b>              |
| 05H         | <Device No.4>   | R      |       |       |       |       |       |       |       | 47H                                                          |
| 04H         | <Device No.3>   | R      |       |       |       |       |       |       |       | 39H                                                          |
| 03H         | <Device No.2>   | R      |       |       |       |       |       |       |       | 52H                                                          |
| 02H         | <Device No.1>   | R      |       |       |       |       |       |       |       | 55H                                                          |
| 01H         | <Device Family> | R      |       |       |       |       |       |       |       | 01H                                                          |
| 00H         | <Company Code>  | R      |       |       |       |       |       |       |       | 00H                                                          |

### Device identification registers

These registers represent a unique signature to identify the device and silicon version.

<Company Code>: 00H (STMicroelectronics)

<Device Family>: 01H (BCD power management)

<Device No. 1>: 55H (ASCII code for U)

<Device No. 2>: 52H (ASCII code for R)

<Device No. 3>: 39H (ASCII code for 9)  
<Device No. 4>: 47H (ASCII code for G)  
<Device No. 5>: 00H: SPSB100GS 01H SPSB100GBS

#### SPI modes

By reading out the <SPI mode> register, general information on SPI usage of the *device application registers* can be obtained.

**Table 17. SPI mode register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| BR    | FL2   | FL1   | FL0   | SPI8  | 0     | S1    | S0    |
| 0     | 0     | 1     | 1     | 0     | 0     | 1     | 0     |

<SPI Mode>: 32H (no burst mode available, 32 bits, CRC used)

#### CRC

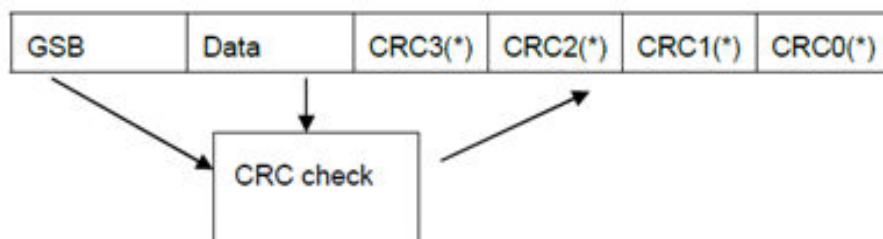
##### SDI:

The CRC check is performed on the complete communication frame using the polynomial  $(X^4 + X + 1)$ .  
The frame is valid only if the result of the CRC check is equal to '0'. If not, the frame is rejected and a SPIE bit is set.

##### SDO:

CRC is calculated on GSB and data (not considering the last 4 CRC bits) and the 4 bit result is saved in Data LSB\_3 to Data LSB\_0.

**Figure 44. CRC check**



Exceptions:

The CRC field is not inserted when device information is read in ROM registers.

#### Watchdog definition

(see also Chapter [Section 3.10](#))

Watchdog default settings can be read out via the device information registers.

**Table 18. WD type/timing**

|             | Bit 7 | Bit 6 | Bit 5                             | Bit 4 | Bit 3 | Bit 2                 | Bit 1 | Bit 0 |
|-------------|-------|-------|-----------------------------------|-------|-------|-----------------------|-------|-------|
| <WD Type 1> | 0     | 1     | x                                 | x     | x     | x                     | x     | x     |
|             |       |       | Watchdog Long Open Window WT[5:0] |       |       |                       |       |       |
| <WD Type 2> | 1     | 0     | 0                                 | 1     | 0     | 0                     | 0     | 1     |
|             |       |       | Open Window OW[2:0]               |       |       | Closed Window CW[2:0] |       |       |

<WD Type 1>: Long Open Window: reflects the value of LOW\_SET(1:0) bits of the USER-NVM

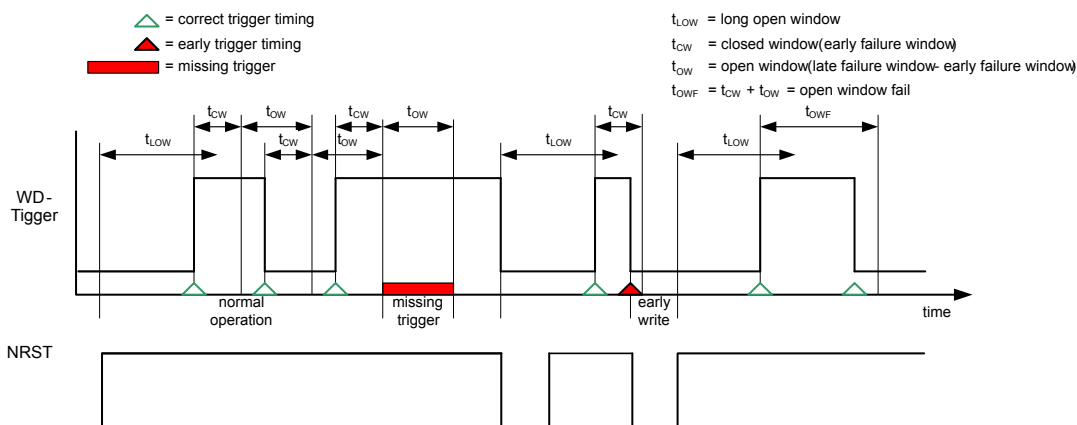
<WD Type 2>:91H; (Open Window: 10 ms, Closed Window: 5 ms)

<WD Type 1> indicates the Long Open Window duration. On this byte, bits 5 and 4 are zero and bits 3 to 0 come from LOW\_SET(3-0) USER-NVM bits. Refer to Section 7.11 describing the Long Open Window durations according to LOW\_SET(3-0) from USER-NVM.

<WD Type 2> describes the default timing of the window watchdog.

The binary value of CW[2:0] multiplied by 5 ms defines the typical Closed Window time ( $t_{CW}$ ) and OW[2:0] multiplied by 5 ms defines the typical Open Window time ( $t_{OW}$ ). See the figure below with  $t_{CW} = t_{EFW}$  and  $t_{OW} = t_{LFW} - t_{EFW}$

Figure 45. Window watchdog operation



The watchdog trigger bit location is defined by the <WD bit pos. X> registers.

Table 19. WD bit position

|                                                         | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| <WD bit pos. 1>                                         | 0     | 1     | 0     | 0     | 0     | 1     | 0     | 0     |
| Defines the register addresses of the WD trigger bit(s) |       |       |       |       |       |       |       |       |
| <WD bit pos. 2>                                         | 1     | 1     | 0     | 0     | 0     | 0     | 0     | 0     |
| Defines the binary bit position                         |       |       |       |       |       |       |       |       |

<WD bit pos 1>: 44H; watchdog trigger bit located at address 04H (DCR4)

<WD bit pos 2>: C0H; watchdog trigger bit location is bit 0

<WD bit pos 3>: 00H

#### Device Application Registers (RAM)

The device application registers are all registers accessible using the OpCode '00', '01' and '10'.

## 6 Functional safety concept

The device is designed to offer a set of features to support applications that need to fulfill functional safety requirements as defined by ASIL classification in ISO26262-2018. The IC is developed for different applications, hence can be considered an SEooC (safety element out of context) as defined in the normative. Analysis of the IC's capability to reach the required safety level should be made at system level under the user's responsibility.

### 6.1 Safety requirements

SPSB100GS must fulfill safety requirements for temperature, output current, output voltage, and system operation as in the following tables based on MCU modes.

**Table 20. Relation between MCU and SPSB100GS modes**

| MCU         | SPSB100GS         | FSR          | ASIL |
|-------------|-------------------|--------------|------|
| RUN         | Active FULL-POWER | FSR-FP-x     | D    |
| Smart-Power | Active FULL-POWER | FSR-LP-x     | B    |
|             | Active LOW-POWER  | FSR-LP-x     | B    |
| Stand-By    | Active LOW-POWER  | FSR-LP-1/5/6 | B    |

#### 6.1.1 SPSB100GS in active full-power mode

**Figure 46. PMIC is in active full-power mode**

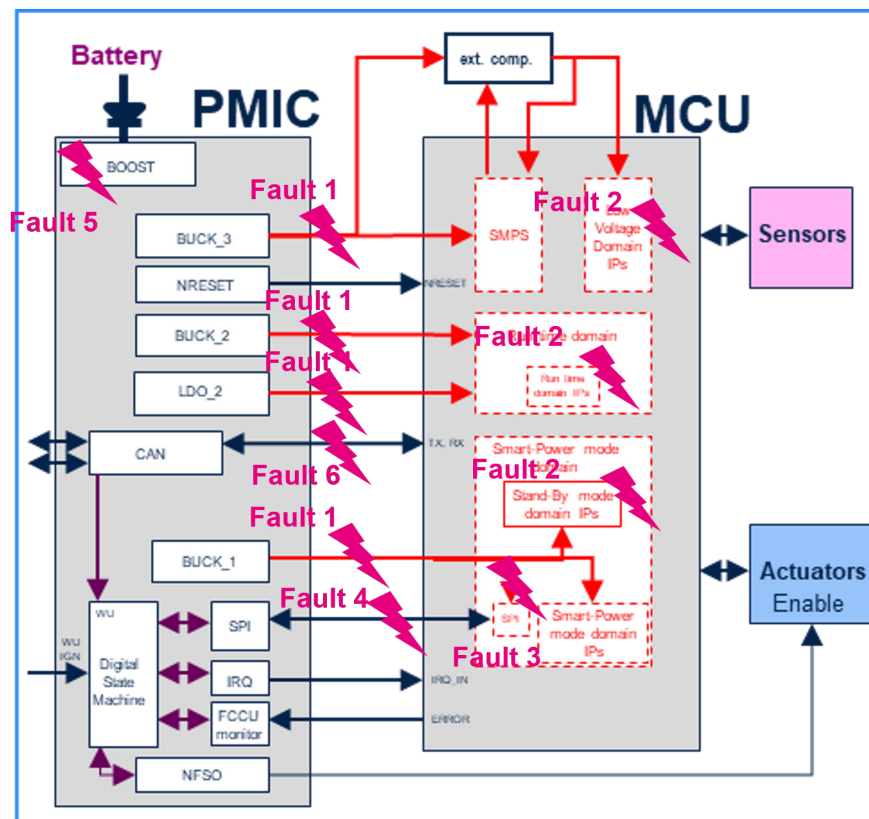


**Table 21. Safety requirement list while SPSB100GS in active full-power mode**

| ID    | Description                                                                                                                                                                                    | Safety state                                                                      |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|
| TSR-1 | Regulator, defined as non-critical supply rail, shall provide configured output voltage, above defined UV threshold and below defined OV threshold.                                            | The PMIC shall power down failing rail(s) and shall send an interrupt to the MCU. |
| TSR-2 | Regulator, defined as critical supply rail, shall provide configured output voltage, above defined UV threshold and below defined OV threshold.                                                | The PMIC shall power down all rails and shall latch NFSO1 output low.             |
| TSR-3 | PMIC shall monitor the error pin used by the MCU to indicate a hardware error and assert NRST/NFSO1 as per specification.                                                                      | NA (safety mechanism).                                                            |
| TSR-4 | PMIC shall monitor if the MCU misses or wrongly triggers window watchdog and assert NRST/NFSO1 as per specification.                                                                           | NA (safety mechanism).                                                            |
| TSR-5 | PMIC shall monitor BOOST/ BYPASS external transistors power dissipation and, if max. temperature is exceeded, shall turn off BOOST/BYPASS transistors and report the failure to the MCU (IRQ). | NA (safety mechanism).                                                            |

**Note:** More details about functional safety can be found in the device safety manual, provided only upon customer request.

### 6.1.2 SPSB100GS in active low-power mode

**Figure 47. PMIC is in active low-power mode**

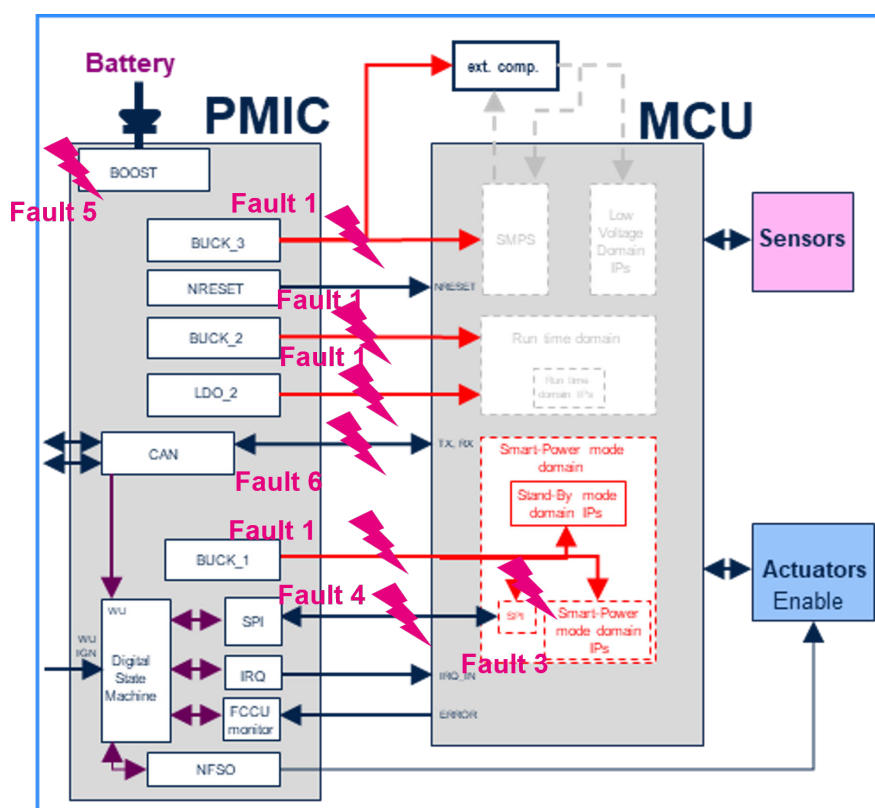


**Table 22. Safety requirement list while SPSB100GS in active low-power mode**

| ID      | Description                                                                                                                                                                                    | Safe state                                                                    |
|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
| TSRLP-1 | Regulator, defined as non-critical supply rail, shall provide configured output voltage, above defined UV threshold and below defined OV threshold.                                            | The PMIC shall power down failing rail(s) and shall send an interrupt to MCU. |
| TSRLP-2 | Regulator, defined as critical supply rail, shall provide configured output voltage, above defined UV threshold and below defined OV threshold.                                                | The PMIC shall power down all rails and shall latch NFSO1 output low.         |
| TSRLP-4 | PMIC shall monitor if the MCU misses or wrongly triggers window watchdog and assert NRST/NFSO1 as per specification.                                                                           | NA (safety mechanism).                                                        |
| TSRLP-5 | PMIC shall monitor BOOST/ BYPASS external transistors power dissipation and, if max. temperature is exceeded, shall turn off BOOST/BYPASS transistors and report the failure to the MCU (IRQ). | NA (safety mechanism).                                                        |
| TSRLP-6 | PMIC shall latch NFSO1 low when the PMIC is in Low-Power mode, REC-1,-2 or DEEP-SLEEP state.                                                                                                   | NA (safety mechanism).                                                        |

**Note:** More details about functional safety can be found in the device safety manual, provided only upon customer request.

### 6.1.3 Independent from MCU mode

The following figure shows the CAN behavior, regardless of the MCU mode.

**Figure 48. Independent from MCU mode**

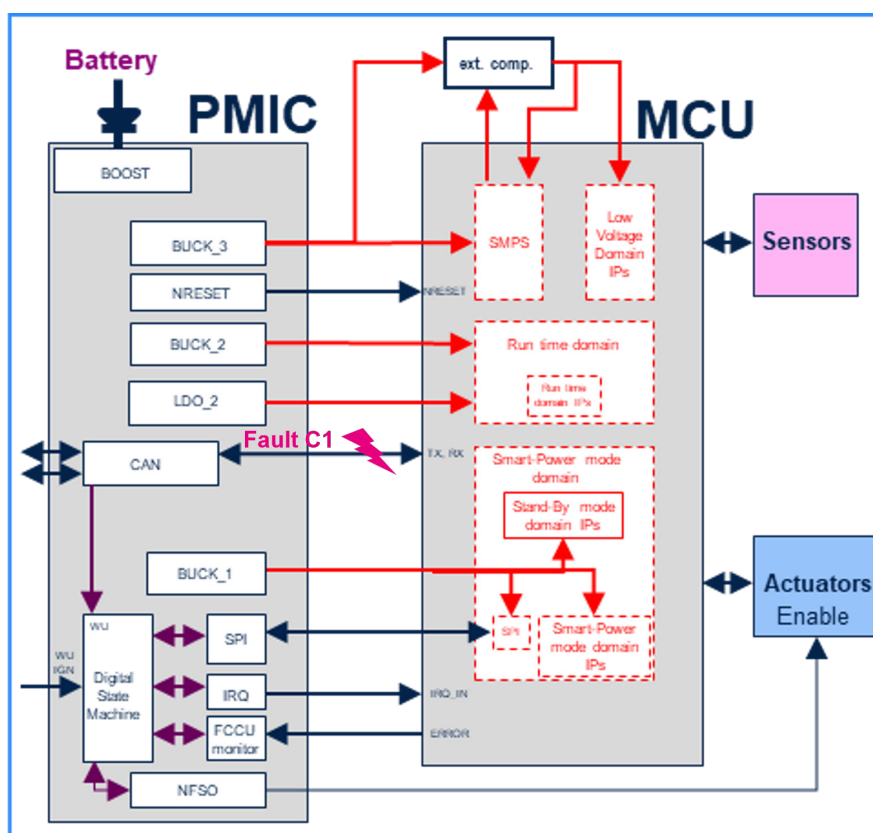


**Table 23. Safety requirement list independent of MCU mode**

| ID    | Description                                         |                                                                                                                                                                |
|-------|-----------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TSR-7 | Device shall guarantee CAN interface functionality. | <p>Overtemperature condition: Device transitions to REC-2 state, then INIT state and powers up the rails.</p> <p>Other conditions: device state unchanged.</p> |

*Note:* More details about functional safety can be found in the device safety manual, provided only upon customer request.

## 6.2 Safety mechanisms

Safety mechanisms implemented in the SPSB100GS are described in [Section 5](#). More details about functional safety can be found in the device safety manual, provided only upon customer request.

## 7 Electrical characteristics

### 7.1 Supply monitoring

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  
 $3\text{ V} < V_S < 29\text{ V}$ ,  $6\text{ V} \leq V_{FBB} \leq 29\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 24. Supply and supply monitoring**

| Symbol                | Parameter                                       | Condition                                                                                         | Min.  | Typ.  | Max.  | Unit          |
|-----------------------|-------------------------------------------------|---------------------------------------------------------------------------------------------------|-------|-------|-------|---------------|
| $V_{FBB\_OK\_R1}$     | VFBB OK rising threshold                        | $FBB\_OK\_SEL<1:0>=00$                                                                            | 5.2   | 5.5   | 5.8   | V             |
| $V_{FBB\_OK\_F1}$     | VFBB OK falling threshold                       | $FBB\_OK\_SEL<1:0>=00$                                                                            | 4.7   | 5.0   | 5.3   | V             |
| $V_{FBB\_OK\_R2}$     | VFBB OK rising threshold                        | $FBB\_OK\_SEL<1:0>=01$                                                                            | 6.2   | 6.5   | 6.8   | V             |
| $V_{FBB\_OK\_F2}$     | VFBB OK falling threshold                       | $FBB\_OK\_SEL<1:0>=01$                                                                            | 5.7   | 6.0   | 6.3   | V             |
| $V_{FBB\_OK\_R3}$     | VFBB OK rising threshold                        | $FBB\_OK\_SEL<1:0>=10$                                                                            | 7.1   | 7.5   | 7.9   | V             |
| $V_{FBB\_OK\_F3}$     | VFBB OK falling threshold                       | $FBB\_OK\_SEL<1:0>=10$                                                                            | 6.6   | 7.0   | 7.4   | V             |
| $V_{FBB\_OK\_R4}$     | VFBB OK rising threshold                        | $FBB\_OK\_SEL<1:0>=11$                                                                            | 8.1   | 8.5   | 8.9   | V             |
| $V_{FBB\_OK\_F4}$     | VFBB OK falling threshold                       | $FBB\_OK\_SEL<1:0>=11$                                                                            | 7.6   | 8.0   | 8.4   | V             |
| $V_{FBB\_OK\_HYS}$    | VFBB OK hysteresis                              |                                                                                                   | 0.44  | 0.55  | 0.65  | V             |
| $T_{F\_FBB\_OK}$      | Digital filter time on FBB OK                   | Covered by SCAN                                                                                   | 12    | 15    | 22    | $\mu\text{s}$ |
| $V_{FBB\_OV}$         | VFBB overvoltage threshold                      | $V_{FBB}$ increasing                                                                              | 29    | 31    | 33    | V             |
| $V_{FBB\_OV\_HYS}$    | VFBB overvoltage hysteresis                     |                                                                                                   | 0.1   | 0.15  | 0.25  | V             |
| $T_{F\_FBB\_OV}$      | Digital filter time on FBB overvoltage          | Covered by SCAN                                                                                   | 12    | 15    | 22    | $\mu\text{s}$ |
| $V_{FBB\_OV\_EW}$     | VFBB overvoltage early warning threshold        | $FBB\_OV\_EW\_TH=[0\dots3]$ step = 1 V. Covered by SCAN                                           | 24    |       | 38    | V             |
| $V_{FBB\_UV\_EW\_TH}$ | VFBB undervoltage early warning range           | $FBB\_UV\_EW\_TH=[0\dots3]$ step = 0.24 V. Covered by SCAN                                        | 5     |       | 8.36  | V             |
| $V_{VS\_UV\_EW\_TH}$  | VS undervoltage early warning range             | $VS\_UV\_EW\_TH=[0\dots4]$ step = 0.24 V. Covered by SCAN                                         | 2.6   |       | 9.8   | V             |
| $V_{VIO\_UV\_R}$      | VIO undervoltage rising VIO voltage             |                                                                                                   | 2.75  | 2.9   | 3.10  | V             |
| $V_{VIO\_UV\_F}$      | On a falling VIO voltage                        |                                                                                                   | 2.7   | 2.85  | 3.05  | V             |
| $V_{VIO\_UV\_HYS}$    | Hysteresis VIO monitoring                       |                                                                                                   | 0.005 | 0.035 | 0.065 | V             |
| $T_{F\_VIO\_UV}$      | Digital filter time on comparator output        | Covered by SCAN                                                                                   | 12    | 15    | 22    | $\mu\text{s}$ |
| $I_{V(Act)}^{(1)}$    | Current consumption in ACTIVE – FULL-POWER mode | $V_S = 13.5\text{ V}$ ; Buck1,2,3 ON; LDO1, LDO2 ON; no load on regulator; Buck1,2_freq = 400 kHz |       | 25    | 40    | mA            |

| Symbol                    | Parameter                                                            | Condition                                                                                                                                                                                                                                                                     | Min. | Typ. | Max. | Unit          |
|---------------------------|----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{VS\_LP1}^{(1)}$       | Current consumption in ACTIVE - LOW-POWER mode                       | $V_S = 13.5\text{ V}$ ; Buck1 ON in LP<br>BUCK1_REFRESH_FREQ = 1; Buck2,3 OFF;<br>LDO1,2 OFF; Buck1 load = 5 mA; $V_{OUT\_BUCK1} = 3.3\text{ V}$ ; Buck1_freq = 400 kHz, IRQ and NFSO high                                                                                    |      | 2    | 3.2  | mA            |
| $I_{VS\_LP2}^{(1)}$       | Current consumption in ACTIVE - LOW-POWER mode                       | $V_S = 13.5\text{ V}$ ; Buck1 ON in LP<br>BUCK1_REFRESH_FREQ = 1; Buck2,3 OFF;<br>LDO1,2 OFF; Buck1 load = 50 $\mu\text{A}$ ; $V_{OUT\_BUCK1} = 3.3\text{ V}$ ; watchdog, OUT_HS, cyclic sense, cyclic wake-up, no SPI communication; Buck2_freq = 400 kHz, IRQ and NFSO high |      | 300  | 600  | $\mu\text{A}$ |
| $I_{VS\_DP}$              | Current consumption in DEEP-SLEEP mode <sup>(2) (3)</sup>            | $V_S = 13.5\text{ V}$ ; Buck1,2,3 OFF; LDO1,2 OFF;<br>OUT_HS, cyclic sense, cyclic wake-up, NFSO high, $T_a = 0\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$                                                                                                          |      | 20   | 40   | $\mu\text{A}$ |
| $I_{VS\_DP\_T}$           | Current consumption in DEEP-SLEEP mode <sup>(2)</sup>                | $V_S = 13.5\text{ V}$ ; Buck1,2,3 OFF; LDO1,2 OFF;<br>OUT_HS, cyclic sense, cyclic wake-up, NFSO high, full temperature range                                                                                                                                                 |      |      | 55   | $\mu\text{A}$ |
| $I_{QCW}$                 | Current consumption adder for cyclic wake-up                         | $V_S = 13.5\text{ V}$ ; in ACTIVE-LOW-POWER mode or DEEP-SLEEP state                                                                                                                                                                                                          |      | 60   | 90   | $\mu\text{A}$ |
| $I_{QCS}$                 | Current consumption adder for cyclic sense                           | $V_S = 13.5\text{ V}$ ; in ACTIVE-LOW-POWER mode or DEEP-SLEEP state. $T_{period} = 50\text{ ms}$ , $T_{on} = 100\text{ }\mu\text{s}$                                                                                                                                         |      | 60   | 90   | $\mu\text{A}$ |
| $I_{QCAN}^{(3)}$          | Quiescent current adder for CAN wake up or CAN autobiasing activated | $V_S = 13.5\text{ V}$ ; in ACTIVE-LOW-POWER mode or DEEP-SLEEP state                                                                                                                                                                                                          |      | 7    | 13   | $\mu\text{A}$ |
| $I_{QOUT\_HS}^{(3)}$      | Additional bias quiescent current for switched ON OUT_HS             | $V_S = 13.5\text{ V}$ ; in ACTIVE-LOW-POWER mode or DEEP-SLEEP state<br>No Load                                                                                                                                                                                               |      | 140  | 220  | $\mu\text{A}$ |
| $I_{VS\_BUCK2\_LP}^{(3)}$ | Additional bias quiescent current for Buck2 in LOW-POWER mode        | $V_S = 13.5\text{ V}$ ; Buck2 ON in LP<br>BUCK2_REFRESH_FREQ = 1; $V_{OUT} = 5\text{ V}$<br>No Load                                                                                                                                                                           |      | 90   | 400  | $\mu\text{A}$ |
| $I_{VS\_DP\_LDT}$         | Additional current consumption for VLDT                              | $V_S = 13.5\text{ V}$                                                                                                                                                                                                                                                         |      |      | 55   | $\mu\text{A}$ |

1. Verified by bench measurements. Performances verified in applicative conditions.
2. Current consumption in DEEP-SLEEP mode is calculated as  $I_{VS\_DP}$  + wake-up current consumption contributions.
3. Guaranteed by design.

## 7.2 Power ground loss monitoring

**Table 25. Power ground loss monitoring**

| Symbol                      | Parameter               | Condition | Min. | Typ. | Max. | Unit          |
|-----------------------------|-------------------------|-----------|------|------|------|---------------|
| $V_{Gnd\_Loss\_th}$         | Ground loss threshold   |           | 150  | 300  | 470  | mV            |
| $t_{Gnd\_Loss\_FILT}^{(1)}$ | Ground loss filter time |           | 12   | 15   | 22   | $\mu\text{s}$ |

1. Digital implementation guaranteed by SCAN test.

The ground loss protection parameter depends mainly on the implementation. This monitor measures a ground shift between the CANGND and SGND pins.

## 7.3 Oscillator

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

$6\text{ V} \leq V_{\text{FBB}} \leq 29\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 26. Oscillator**

| Symbol                     | Parameter             | Condition | Min.  | Typ. | Max.  | Unit |
|----------------------------|-----------------------|-----------|-------|------|-------|------|
| $F_{\text{CLK800K}}$       | Oscillation frequency |           | 640   | 800  | 960   | kHz  |
| $F_{\text{CLK33M6\_MAIN}}$ | Oscillation frequency |           | 26.88 | 33.6 | 40.32 | MHz  |
| $F_{\text{CLK33M6\_MON}}$  | Oscillation frequency |           | 26.88 | 33.6 | 40.32 | MHz  |

## 7.4 Power-on reset

All outputs open;  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 27. Power-on reset**

| Symbol                      | Parameter                   | Condition | Min. | Typ. | Max. | Unit |
|-----------------------------|-----------------------------|-----------|------|------|------|------|
| $V_{\text{PORVS\_R}}$       | $V_S$ POR rising threshold  |           | 4.5  | 4.85 | 5.2  | V    |
| $V_{\text{PORVS\_F}}^{(1)}$ | $V_S$ POR falling threshold |           | 1.9  | 2.1  | 2.3  | V    |
| $V_{\text{PORVS\_HYS}}$     | $V_S$ POR hysteresis        |           | 2.5  | 2.75 | 3    | V    |

1. This threshold is valid if  $V_S$  had already reached  $V_{\text{PORVS\_R(max)}}$  previously.

## 7.5 LDO1 voltage regulator

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

$6\text{ V} \leq V_{\text{FBB}} \leq 29\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 28. LDO1**

| Symbol                          | Parameter                                                       | Condition                                                                                                            | Min. | Typ. | Max. | Unit          |
|---------------------------------|-----------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $V_{\text{LDO1}}$               | Output voltage tolerance.<br>Including line and load regulation | $I_{\text{LOAD}} = 100\text{ }\mu\text{A}$ to $120\text{ mA}$<br>$6.0\text{ V} \leq V_{\text{FBB}} \leq 29\text{ V}$ | 4.9  | 5.0  | 5.15 | V             |
| $V_{\text{LDO1\_PG}}^{(1)}$     | Power-good rising threshold                                     | $V_{\text{LDO1}}$ increasing                                                                                         | 4.6  | 4.8  | 4.9  | V             |
| $V_{\text{LDO1\_UV}}$           | Undervoltage falling threshold                                  | $V_{\text{LDO1}}$ decreasing                                                                                         | 3.8  | 4.0  | 4.2  | V             |
| $t_{\text{LDO1\_PG\_TO}}^{(2)}$ | LDO1 timeout for power-good                                     |                                                                                                                      | 4.8  | 6    | 7.5  | ms            |
| $t_{\text{LDO1\_UV}}^{(2)}$     | Undervoltage filter time                                        |                                                                                                                      | 12   | 15   | 22   | $\mu\text{s}$ |
| $V_{\text{LDO1\_DP}}$           | Drop-out voltage                                                | $I_{\text{LOAD}} = 120\text{ mA}$                                                                                    | -    | -    | 0.8  | V             |
| $I_{\text{LDO1\_Cmax}}$         | Short circuit output current (to GND)                           | Current limitation                                                                                                   | 130  | 175  | 250  | mA            |
| $C_{\text{LDO1}}^{(3)}$         | Load capacitor 1                                                | Ceramic ( $\pm 20\%$ )                                                                                               | 1    | -    | 10   | $\mu\text{F}$ |

1. No overlap with  $V_{\text{LDO1}}$  regulation level by production test.

2. Digital implementation guaranteed by SCAN test.

3. Nominal capacitor value required for stability of the regulator. Tested with  $1\text{ }\mu\text{F}$  ceramic ( $\pm 20\%$ ). Capacitor must be located close to the regulator output pin. A  $2.2\text{ }\mu\text{F}$  capacitor value is recommended to minimize the DPI (Direct Power Injection) stress in the application.

## 7.6 LDO2 voltage regulator

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

$6\text{ V} \leq V_{\text{FBB}} \leq 29\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

The same parameter values apply in both 5 V and 3.3 V conditions unless otherwise specified.

**Table 29. LDO2**

| Symbol                           | Parameter                             | Condition                                                                                                                                            | Min.             | Typ.  | Max.              | Unit          |
|----------------------------------|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-------|-------------------|---------------|
| $V_{\text{LDO2\_5}}$             | Output voltage                        | $V_{\text{FBB}} \geq 6.0\text{ V}$                                                                                                                   | 4.9              | 5.0   | 5.15              | V             |
| $V_{\text{LDO2\_33}}$            | Output voltage                        | $V_{\text{FBB}} \geq 6.0\text{ V}$                                                                                                                   | 3.23             | 3.3   | 3.399             | V             |
| $V_{\text{LDO2\_ACC\_25}}^{(1)}$ | Output voltage tracking accuracy      | $I_{\text{LOAD}} = 100\text{ }\mu\text{A}$ to $5\text{ mA}$<br>$V_{\text{FBB}} = 8\text{ V}$ to $18\text{ V}$<br>$T_j = 25\text{ }^{\circ}\text{C}$  | -10              | -     | 10                | mV            |
| $V_{\text{LDO2\_ACC\_130}}$      | Output voltage tracking accuracy      | $I_{\text{LOAD}} = 100\text{ }\mu\text{A}$ to $5\text{ mA}$<br>$V_{\text{FBB}} = 8\text{ V}$ to $18\text{ V}$<br>$T_j = 130\text{ }^{\circ}\text{C}$ | -20              | -     | 20                | mV            |
| $V_{\text{LDO2\_OV}}$            | Overvoltage threshold for LDO2        |                                                                                                                                                      | 105              | 108.5 | 112               | %             |
| $t_{\text{LDO2\_OV}}^{(2)}$      | LDO2 overvoltage filter time          |                                                                                                                                                      | 12               | 15    | 22                | $\mu\text{s}$ |
| $V_{\text{LDO2\_PG}}$            | Power-good voltage threshold for LDO2 |                                                                                                                                                      | 91.5             | 95    | 98.5              | %             |
| $V_{\text{LDO2\_UV}}$            | Undervoltage threshold for LDO2       |                                                                                                                                                      | 88               | 91.5  | 95                | %             |
| $t_{\text{LDO2\_UV}}^{(2)}$      | LDO2 undervoltage filter time         |                                                                                                                                                      | 12               | 15    | 22                | $\mu\text{s}$ |
| $t_{\text{LDO2\_PG\_TO}}^{(2)}$  | LDO2 timeout for power-good           |                                                                                                                                                      | 4.8              | 6     | 7.5               | ms            |
| $V_{\text{LDO2\_DP}}$            | Drop-out voltage                      | $I_{\text{LOAD}} = 10\text{ mA}$                                                                                                                     | -                | 0.5   | 1.0               | V             |
| $R_{\text{PD\_OFF\_Ido2}}$       | Pull down resistor in Off             | $V_{\text{out}} = 3.3\text{ V}$                                                                                                                      | 110              | 150   | 180               | $\Omega$      |
| $I_{\text{LDO2\_CCmax}}$         | Short-circuit output current (to GND) | Current limitation                                                                                                                                   | 15               | 30    | 45                | mA            |
| $C_{\text{LDO2}}$                | Load capacitor 1                      | Ceramic ( $\pm 20\%$ )                                                                                                                               | 1 <sup>(3)</sup> | -     | 10 <sup>(1)</sup> | $\mu\text{F}$ |

1. Guaranteed by design.

2. Digital implementation guaranteed by SCAN test.

3. Nominal capacitor value required for stability of the regulator. Tested with  $1\text{ }\mu\text{F}$  ceramic ( $\pm 20\%$ ). Capacitor must be located close to the regulator output pin. A  $2.2\text{ }\mu\text{F}$  capacitor value is recommended to minimize the DPI (Direct power Injection) stress in the application.

## 7.7 Boost controller

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

$3\text{ V} \leq V_{\text{S}} \leq 29\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 30. Boost controller**

| Symbol                   | Parameter                     | Condition                                                                                          | Min. | Typ. | Max. | Unit |
|--------------------------|-------------------------------|----------------------------------------------------------------------------------------------------|------|------|------|------|
| $V_{\text{FBB\_UV\_R1}}$ | BOOST rising enable threshold | $\text{FBB\_UV\_LEVEL\_SEL} = 0$<br>Input voltage required on initial start-up to enable the boost | 5.0  | 5.25 | 5.5  | V    |

| Symbol                               | Parameter                                                  | Condition                                                                              | Min. | Typ. | Max. | Unit |
|--------------------------------------|------------------------------------------------------------|----------------------------------------------------------------------------------------|------|------|------|------|
| V <sub>FBB_UV_F1</sub>               | BOOST falling disable threshold                            | FBB_UV_LEVEL_SEL = 0<br>Power-down threshold                                           | 4.6  | 4.85 | 5.1  | V    |
| V <sub>FBB_UV_R2</sub>               | BOOST rising enable threshold                              | FBB_UV_LEVEL_SEL = 1<br>Input voltage required on initial start-up to enable the boost | 5.55 | 5.8  | 6.05 | V    |
| V <sub>FBB_UV_F2</sub>               | BOOST falling disable threshold                            | FBB_UV_LEVEL_SEL = 1<br>Power-down threshold                                           | 5.05 | 5.3  | 5.55 | V    |
| V <sub>FBB_UV_HYS</sub>              | Boost enable hysteresis                                    |                                                                                        | 0.35 | 0.45 | 0.55 | V    |
| T <sub>F_FBB_UV</sub> <sup>(1)</sup> | Digital filter time on FBB POR                             |                                                                                        | 12   | 15   | 22   | µs   |
| V <sub>FBB_REG1</sub>                | V <sub>FBB</sub> regulation threshold                      | FBB_REG_LEVEL_SEL<1:0> = 00                                                            | 5.8  | 6.0  | 6.2  | V    |
| V <sub>FBB_REG2</sub>                | V <sub>FBB</sub> regulation threshold                      | FBB_REG_LEVEL_SEL<1:0> = 01                                                            | 6.8  | 7.0  | 7.2  | V    |
| V <sub>FBB_REG3</sub>                | V <sub>FBB</sub> regulation threshold                      | FBB_REG_LEVEL_SEL<1:0> = 10                                                            | 7.75 | 8.0  | 8.25 | V    |
| V <sub>FBB_REG4</sub>                | V <sub>FBB</sub> regulation threshold                      | FBB_REG_LEVEL_SEL<1:0> = 11                                                            | 8.75 | 9.0  | 9.25 | V    |
| V <sub>S_SENSE1</sub>                | V <sub>S_SENSE</sub> threshold                             | VS_SENSE_LEVEL_SEL<1:0> = 00                                                           | 5.25 | 5.4  | 5.55 | V    |
| V <sub>S_SENSE2</sub>                | V <sub>S_SENSE</sub> threshold                             | VS_SENSE_LEVEL_SEL<1:0> = 01                                                           | 5.4  | 5.55 | 5.7  | V    |
| V <sub>S_SENSE3</sub>                | V <sub>S_SENSE</sub> threshold                             | VS_SENSE_LEVEL_SEL<1:0> = 10                                                           | 5.55 | 5.7  | 5.85 | V    |
| V <sub>S_SENSE4</sub>                | V <sub>S_SENSE</sub> threshold                             | VS_SENSE_LEVEL_SEL<1:0> = 11                                                           | 5.7  | 5.85 | 6.0  | V    |
| V <sub>S_SENSE_HYS</sub>             | V <sub>S_SENSE</sub> hysteresis                            |                                                                                        | 10   | 50   | 100  | mV   |
| F <sub>sw_BOOST</sub>                | Switching frequency                                        | Guaranteed by SCAN                                                                     | 320  | 400  | 480  | kHz  |
| Boost_DC_Max <sup>(1)</sup>          | Boost duty cycle Max                                       | 0V < VS < VS <sub>LOW</sub><br>TON=63 cycles of 33.6 MHz main clk                      | 34   | 75   | 83   | %    |
| Boost_DC_High <sup>(1)</sup>         | Boost duty cycle high                                      | VS <sub>LOW</sub> < VS < VS <sub>MID</sub><br>TON=55 cycles of 33.6 MHz main clk       | 30   | 65.5 | 73   | %    |
| Boost_DC_Low <sup>(1)</sup>          | Boost duty cycle Low                                       | VS <sub>MID</sub> < VS < VS <sub>HIGH</sub><br>TON=46 cycles of 33.6MHz main clk       | 25   | 54.8 | 61   | %    |
| Boost_DC_Min <sup>(1)</sup>          | Boost duty cycle min                                       | VS <sub>HIGH</sub> < VS<br>TON=38 cycles of 33.6MHz main clk                           | 21   | 45.2 | 50   | %    |
| Boost_DC_LP <sup>(1)</sup>           | Boost duty cycle in LOW-POWER mode                         | VS <sub>HIGH</sub> < VS<br>TON= 2 cycles of 800kHz                                     | 27   | 50.0 | 66   | %    |
| VS <sub>Low_R</sub>                  | VS comparator threshold<br>VS <sub>Low</sub><br>Rising     |                                                                                        | 4.25 | 4.5  | 4.75 | V    |
| VS <sub>Low_F</sub>                  | VS comparator threshold<br>VS <sub>Low</sub><br>Falling    |                                                                                        | 3.75 | 4.0  | 4.25 | V    |
| VS <sub>Low_HYS</sub>                | VS comparator threshold<br>VS <sub>Low</sub><br>Hysteresis |                                                                                        | 0.4  | 0.5  | 0.6  | V    |
| VS <sub>Mid_R</sub>                  | VS comparator threshold<br>VS <sub>Mid</sub><br>Rising     |                                                                                        | 5.7  | 6.0  | 6.3  | V    |
| VS <sub>Mid_F</sub>                  | VS comparator threshold<br>VS <sub>Mid</sub><br>Falling    |                                                                                        | 5.2  | 5.5  | 5.8  | V    |

| Symbol                                | Parameter                                                           | Condition                                                                                                                        | Min. | Typ. | Max. | Unit |
|---------------------------------------|---------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| VS_Mid_HYS                            | VS comparator threshold<br>VS_Mid<br>Hysteresis                     |                                                                                                                                  | 0.4  | 0.5  | 0.6  | V    |
| VS_High_R                             | VS comparator threshold<br>VS_High<br>Rising                        |                                                                                                                                  | 7.1  | 7.5  | 7.9  | V    |
| VS_High_F                             | VS comparator threshold<br>VS_High<br>Falling                       |                                                                                                                                  | 6.6  | 7    | 7.4  | V    |
| VS_High_HYS                           | VS comparator threshold<br>VS_High hysteresis                       |                                                                                                                                  | 0.4  | 0.5  | 0.6  | V    |
| V <sub>Boost_rip</sub> <sup>(2)</sup> | Boost Voltage_ripple                                                | Ripple @ 20 kHz<br><br>All characteristics of all blocks supplied by FBB guaranteed with external components defined in Table 65 |      |      | 2.5  | Vpp  |
| I <sub>Boost</sub> <sup>(2)</sup>     | Boost current capability in full power mode                         | guaranteed with external components defined in Table 65                                                                          | 3.5  |      |      | A    |
| I <sub>Boost_LP</sub> <sup>(2)</sup>  | Boost current capability in LOW-POWER mode                          | guaranteed with external components defined in Table 65                                                                          | 0.2  |      |      | A    |
| I <sub>Boost_LS_sink1</sub>           | LS driver sink current                                              | VFBB= VGLB = 8.5V                                                                                                                | 70   | 100  | 130  | mA   |
| I <sub>Boost_HS_source1</sub>         | HS driver source current                                            | VFBB=8.5V VGLB = 0V                                                                                                              | 70   | 100  | 130  | mA   |
| I <sub>Boost_LS_sink2</sub>           | LS driver sink current                                              | VFBB=8.5V VGLB = 0.5V                                                                                                            | 20   | 35   | 55   | mA   |
| I <sub>Boost_HS_source2</sub>         | HS driver source current                                            | VFBB=8.5V VGLB = 8V                                                                                                              | 10   | 25   | 45   | mA   |
| R <sub>Boost_gate_pull-down</sub>     | Resistive gate pull-down                                            | BOOST_DIS=1                                                                                                                      | 3    | 5    | 8    | kΩ   |
| I <sub>VS_stdby</sub>                 | Current leakage on VS pin in stdby                                  |                                                                                                                                  |      |      | 2    | μA   |
| I <sub>VS_Sense</sub>                 | Sink current in VS active mode                                      |                                                                                                                                  | 120  | 180  | 250  | μA   |
| V <sub>BOOST_VDSM1</sub>              | Boost drain-source rising threshold voltage                         | BOOST_DSMON_TH=000                                                                                                               | 220  | 250  | 280  | mV   |
| V <sub>BOOST_VDSM2</sub>              | Boost drain-source rising threshold voltage                         | BOOST_DSMON_TH=001                                                                                                               | 400  | 450  | 500  | mV   |
| V <sub>BOOST_VDSM3</sub>              | Boost drain-source rising threshold voltage                         | BOOST_DSMON_TH =010                                                                                                              | 580  | 650  | 710  | mV   |
| V <sub>BOOST_VDSM4</sub>              | Boost drain-source rising threshold voltage                         | BOOST_DSMON_TH =011                                                                                                              | 770  | 850  | 930  | mV   |
| V <sub>BOOST_VDSM5</sub>              | Boost drain-source rising threshold voltage                         | BOOST_DSMON_TH =100                                                                                                              | 1.0  | 1.1  | 1.2  | V    |
| V <sub>BOOST_VDSM6</sub>              | Boost drain-source rising threshold voltage                         | BOOST_DSMON_TH =101                                                                                                              | 1.15 | 1.3  | 1.45 | V    |
| V <sub>BOOST_VDSM7</sub>              | Boost drain-source rising threshold voltage                         | BOOST_DSMON_TH =110                                                                                                              | 1.35 | 1.5  | 1.65 | V    |
| V <sub>BOOST_VDSM8</sub>              | Boost drain-source rising threshold voltage                         | BOOST_DSMON_TH =111                                                                                                              | 1.53 | 1.7  | 1.87 | V    |
| V <sub>BOOST_VDSM_HYS_H</sub>         | Boost drain-source threshold voltage hysteresis for high VDSM codes | BOOST_DSMON_TH =1xx                                                                                                              | 75   | 100  | 125  | mV   |
| V <sub>BOOST_VDSM_HYS_L</sub>         | Boost drain-source threshold voltage hysteresis for Low VDSM codes  | BOOST_DSMON_TH =0xx                                                                                                              | 25   | 50   | 75   | mV   |

| Symbol                     | Parameter                                                                    | Condition                                             | Min. | Typ. | Max.  | Unit    |
|----------------------------|------------------------------------------------------------------------------|-------------------------------------------------------|------|------|-------|---------|
| $V_{TH\_BYPASS\_R1}$       | Bypass external MOSFET enable comparator rising threshold, rising $V_{VS}$   | BYPASS_OFFSET_SEL = 0 and FBB_REG_LEVEL_SEL<1:0> = 00 | 6.3  | 6.5  | 6.7   | V       |
| $V_{TH\_BYPASS\_F1}$       | Bypass external MOSFET disable comparator falling threshold, rising $V_{VS}$ | BYPASS_OFFSET_SEL = 0 and FBB_REG_LEVEL_SEL<1:0> = 00 | 5.8  | 6.0  | 6.2   | V       |
| $V_{TH\_BYPASS\_R2}$       | Bypass external MOSFET enable comparator rising threshold, rising $V_{VS}$   | BYPASS_OFFSET_SEL = 1 and FBB_REG_LEVEL_SEL<1:0> = 00 | 6.8  | 7.0  | 7.2   | V       |
| $V_{TH\_BYPASS\_F2}$       | Bypass external MOSFET disable comparator falling threshold, rising $V_{VS}$ | BYPASS_OFFSET_SEL = 1 and FBB_REG_LEVEL_SEL<1:0> = 00 | 6.3  | 6.5  | 6.7   | V       |
| $V_{TH\_BYPASS\_R3}$       | Bypass external MOSFET enable comparator rising threshold, rising $V_{VS}$   | BYPASS_OFFSET_SEL = 0 and FBB_REG_LEVEL_SEL<1:0> = 01 | 7.3  | 7.5  | 7.7   | V       |
| $V_{TH\_BYPASS\_F3}$       | Bypass external MOSFET disable comparator falling threshold, rising $V_{VS}$ | BYPASS_OFFSET_SEL = 0 and FBB_REG_LEVEL_SEL<1:0> = 01 | 6.8  | 7.0  | 7.2   | V       |
| $V_{TH\_BYPASS\_R4}$       | Bypass external MOSFET enable comparator rising threshold, rising $V_{VS}$   | BYPASS_OFFSET_SEL = 1 and FBB_REG_LEVEL_SEL<1:0> = 01 | 7.75 | 8.0  | 8.25  | V       |
| $V_{TH\_BYPASS\_F4}$       | Bypass external MOSFET disable comparator falling threshold, rising $V_{VS}$ | BYPASS_OFFSET_SEL = 1 and FBB_REG_LEVEL_SEL<1:0> = 01 | 7.3  | 7.5  | 7.7   | V       |
| $V_{TH\_BYPASS\_R5}$       | Bypass external MOSFET enable comparator rising threshold, rising $V_{VS}$   | BYPASS_OFFSET_SEL = 0 and FBB_REG_LEVEL_SEL<1:0> = 10 | 8.25 | 8.5  | 8.75  | V       |
| $V_{TH\_BYPASS\_F5}$       | Bypass external MOSFET disable comparator falling threshold, rising $V_{VS}$ | BYPASS_OFFSET_SEL = 0 and FBB_REG_LEVEL_SEL<1:0> = 10 | 7.75 | 8.0  | 8.25  | V       |
| $V_{TH\_BYPASS\_R6}$       | Bypass external MOSFET enable comparator rising threshold, rising $V_{VS}$   | BYPASS_OFFSET_SEL = 1 and FBB_REG_LEVEL_SEL<1:0> = 10 | 8.75 | 9.0  | 9.25  | V       |
| $V_{TH\_BYPASS\_F6}$       | Bypass external MOSFET disable comparator falling threshold, rising $V_{VS}$ | BYPASS_OFFSET_SEL = 1 and FBB_REG_LEVEL_SEL<1:0> = 10 | 8.25 | 8.5  | 8.75  | V       |
| $V_{TH\_BYPASS\_R7}$       | Bypass external MOSFET enable comparator rising threshold, rising $V_{VS}$   | BYPASS_OFFSET_SEL = 0 and FBB_REG_LEVEL_SEL<1:0> = 11 | 9.25 | 9.5  | 9.75  | V       |
| $V_{TH\_BYPASS\_F7}$       | Bypass external MOSFET disable comparator falling threshold, rising $V_{VS}$ | BYPASS_OFFSET_SEL = 0 and FBB_REG_LEVEL_SEL<1:0> = 11 | 8.75 | 9.0  | 9.25  | V       |
| $V_{TH\_BYPASS\_R8}$       | Bypass external MOSFET enable comparator rising threshold, rising $V_{VS}$   | BYPASS_OFFSET_SEL = 1 and FBB_REG_LEVEL_SEL<1:0> = 11 | 9.75 | 10.0 | 10.25 | V       |
| $V_{TH\_BYPASS\_F8}$       | Bypass external MOSFET disable comparator falling threshold, rising $V_{VS}$ | BYPASS_OFFSET_SEL = 1 and FBB_REG_LEVEL_SEL<1:0> = 11 | 9.25 | 9.5  | 9.75  | V       |
| $T_{F\_BYPASS\_EN}^{(1)}$  | Digital filter time on bypass external MOSFET enable comparator output       |                                                       | 12   | 15   | 22    | $\mu s$ |
| $T_{F\_BYPASS\_DIS}^{(1)}$ | Digital filter time on bypass external MOSFET disable comparator output      |                                                       | 0    | 0.24 | 0.4   | $\mu s$ |

| Symbol                                    | Parameter                                            | Condition                              | Min. | Typ. | Max. | Unit |
|-------------------------------------------|------------------------------------------------------|----------------------------------------|------|------|------|------|
| V <sub>BYPASS_VDSM1</sub>                 | Bypass drain-source rising threshold voltage         | BYPASS_DSMON_TH =000                   | 75   | 125  | 175  | mV   |
| V <sub>BYPASS_VDSM2</sub>                 | Bypass drain-source rising threshold voltage         | BYPASS_DSMON_TH =001                   | 125  | 165  | 225  | mV   |
| V <sub>BYPASS_VDSM3</sub>                 | Bypass drain-source rising threshold voltage         | BYPASS_DSMON_TH =010                   | 175  | 225  | 275  | mV   |
| V <sub>BYPASS_VDSM4</sub>                 | Bypass drain-source rising threshold voltage         | BYPASS_DSMON_TH =011                   | 225  | 275  | 325  | mV   |
| V <sub>BYPASS_VDSM5</sub>                 | Bypass drain-source rising threshold voltage         | BYPASS_DSMON_TH =100                   | 275  | 325  | 375  | mV   |
| V <sub>BYPASS_VDSM6</sub>                 | Bypass drain-source rising threshold voltage         | BYPASS_DSMON_TH =101                   | 325  | 375  | 425  | mV   |
| V <sub>BYPASS_VDSM7</sub>                 | Bypass drain-source rising threshold voltage         | BYPASS_DSMON_TH =110                   | 375  | 425  | 475  | mV   |
| V <sub>BYPASS_VDSM8</sub>                 | Bypass drain-source rising threshold voltage         | BYPASS_DSMON_TH=111                    | 425  | 475  | 525  | mV   |
| V <sub>BYPASS_VDSM_HYS</sub>              | Bypass drain-source threshold voltage hysteresis     | BYPASS_DSMON_TH =xxx                   | 25   | 50   | 75   | mV   |
| T <sub>F_BYPASS_VDSM</sub> <sup>(1)</sup> | Digital filter time on bypass drain-source threshold |                                        | 12   | 15   | 22   | µs   |
| T <sub>B_BYPASS_VDSM</sub> <sup>(1)</sup> | Blanking time on bypass drain-source comparator      |                                        | 90   | 110  | 142  | µs   |
| R <sub>bypass_gate_discharge</sub>        | Bypass gate discharge resistor                       | FBB-GBY = 2 V FBB=7 and GBY=5 turn OFF | 100  | 220  | 600  | Ω    |
| I <sub>bypass_gate_charge</sub>           | Bypass gate charge current                           | GBY=5V FBB=13.5V                       | 0.4  | 1.2  | 2    | mA   |
| t <sub>boost_crk_to1</sub> <sup>(1)</sup> | Boost timeout 1                                      | BOOST_CRK_TO = 001                     | 0.4  | 0.5  | 0.6  | s    |
| t <sub>boost_crk_to2</sub> <sup>(1)</sup> | Boost timeout 2                                      | BOOST_CRK_TO = 010                     | 0.8  | 1    | 1.2  | s    |
| t <sub>boost_crk_to3</sub> <sup>(1)</sup> | Boost timeout 3                                      | BOOST_CRK_TO = 011                     | 1.6  | 2    | 2.4  | s    |
| t <sub>boost_crk_to4</sub> <sup>(1)</sup> | Boost timeout 4                                      | BOOST_CRK_TO = 100                     | 3.2  | 4    | 4.8  | s    |
| t <sub>boost_crk_to5</sub> <sup>(1)</sup> | Boost timeout 5                                      | BOOST_CRK_TO = 101                     | 4.8  | 6    | 7.2  | s    |
| t <sub>boost_crk_to6</sub> <sup>(1)</sup> | Boost timeout 6                                      | BOOST_CRK_TO = 110                     | 6.4  | 8    | 9.6  | s    |
| t <sub>boost_crk_to7</sub> <sup>(1)</sup> | Boost timeout 7                                      | BOOST_CRK_TO = 111                     | 8    | 10   | 12   | s    |

1. Digital implementation guaranteed by SCAN test.
2. Guaranteed by design.

## 7.8 BUCK1 converter

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

$8.5\text{ V} \leq V_{IN12} \leq 29\text{ V}$ ,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 31. Buck 1 converter**

| Symbol                       | Parameter                                               | Condition                                                                                                                                                            | Min   | Typ   | Max   | Unit          |
|------------------------------|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|---------------|
| $V_{IN12\_H}$                | Input voltage range                                     | $V_{out\_buck1} = 6.5\text{ V}$<br>(see Figure 59)                                                                                                                   | 8.7   | 14    | 29    | V             |
| $V_{IN12\_M}$                | Input voltage range                                     | $V_{out\_buck1} = 5\text{ V}$<br>(see Figure 58)                                                                                                                     | 7     | 14    | 29    | V             |
| $V_{IN12\_L}$                | Input voltage range                                     | $V_{out\_buck1} = 3.3\text{ V}$<br>(see Figure 57)                                                                                                                   | 5.2   | 14    | 29    | V             |
| $V_{out\_buck1\_33}^{(1)}$   | Output voltage                                          | BUCK1_PU_VALUE=00<br>Transients and ripple not included, $V_{IN12} = 8.5\text{ V}$ to $16\text{ V}$ , $I_{LOAD} = 50\text{ mA}$ to $1.5\text{ A}$<br>Freq. = 400 kHz | 3.23  | 3.3   | 3.399 | V             |
| $V_{out\_buck1\_5}^{(1)}$    | Output voltage                                          | BUCK1_PU_VALUE=01<br>Transients and ripple not included, $V_{IN12} = 8.5\text{ V}$ to $16\text{ V}$ , $I_{LOAD} = 50\text{ mA}$ to $1.5\text{ A}$<br>Freq. = 400 kHz | 4.9   | 5     | 5.15  | V             |
| $V_{out\_buck1\_65}^{(1)}$   | Output voltage                                          | BUCK1_PU_VALUE=1x<br>Transients and ripple not included, $V_{IN12} = 9.2\text{ V}$ to $16\text{ V}$ , $I_{LOAD} = 50\text{ mA}$ to $1.5\text{ A}$<br>Freq. = 400 kHz | 6.37  | 6.5   | 6.695 | V             |
| $V_{out\_UV\_buck1\_err}$    | Output undervoltage threshold monitor range             |                                                                                                                                                                      | 86    | 90    | 94    | %             |
| $V_{out\_PG\_buck1}$         | Output power-good threshold monitor range               |                                                                                                                                                                      | 88    | 92    | 96    | %             |
| $V_{out\_OV\_buck1\_err}$    | Output overvoltage threshold monitor range              |                                                                                                                                                                      | 103   | 107   | 111   | %             |
| $t_{buck1\_PG\_TO}^{(2)}$    | Output power-good timeout                               |                                                                                                                                                                      | 4.8   | 6     | 7.5   | ms            |
| $t_{buck1\_UV\_TO}^{(2)}$    | $V_{OUT}$ undervoltage time-out filter                  |                                                                                                                                                                      | 25    | 30    | 41    | $\mu\text{s}$ |
| $t_{buck1\_OV\_TO}^{(2)}$    | $V_{OUT}$ overvoltage time-out filter                   |                                                                                                                                                                      | 25    | 30    | 41    | $\mu\text{s}$ |
| $R_{DS(on)\_HS\_buck1\_25}$  | HS Switch ON resistance @ 1.5 A                         | $V_{IN12} = 14\text{ V}$ , $T_J = 25\text{ }^{\circ}\text{C}$                                                                                                        |       | 0.095 | 0.12  | $\Omega$      |
| $R_{DS(on)\_HS\_buck1\_130}$ | HS switch ON resistance @ 1.5 A                         | $V_{IN12} = 14\text{ V}$ , $T_J = 130\text{ }^{\circ}\text{C}$                                                                                                       |       |       | 0.165 | $\Omega$      |
| $R_{DS(on)\_LS\_buck1\_25}$  | LS switch ON resistance @ 1.5 A                         | $V_{IN12} = 14\text{ V}$ , $T_J = 25\text{ }^{\circ}\text{C}$                                                                                                        |       | 0.095 | 0.12  | $\Omega$      |
| $R_{DS(on)\_LS\_buck1\_130}$ | LS switch ON resistance @ 1.5 A                         | $V_{IN12} = 14\text{ V}$ , $T_J = 130\text{ }^{\circ}\text{C}$                                                                                                       |       |       | 0.165 | $\Omega$      |
| $I_{limit\_buck1\_000}$      | Peak switching current limit @ $V_{IN12} = 14\text{ V}$ | BUCK1_IPEAK=000                                                                                                                                                      | 1.7   | 2     | 2.3   | A             |
| $I_{limit\_buck1\_001}$      | Peak switching current limit @ $V_{IN12} = 14\text{ V}$ | BUCK1_IPEAK=001                                                                                                                                                      | 2.125 | 2.5   | 2.875 | A             |

| Symbol                                  | Parameter                                                  | Condition                                                                                                                                                                                       | Min   | Typ  | Max   | Unit |
|-----------------------------------------|------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|------|
| $I_{\text{limit\_buck1\_010}}$          | Peak switching current limit @ VIN12 = 14 V                | BUCK1_IPEAK=010                                                                                                                                                                                 | 2.55  | 3    | 3.45  | A    |
| $I_{\text{limit\_buck1\_011}}$          | Peak switching current limit @ VIN12 = 14 V                | BUCK1_IPEAK=011                                                                                                                                                                                 | 2.975 | 3.5  | 4.025 | A    |
| $I_{\text{limit\_buck1\_100}}$          | Peak switching current limit @ VIN12 = 14 V                | BUCK1_IPEAK=100                                                                                                                                                                                 | 3.2   | 4    | 4.6   | A    |
| $I_{\text{limit\_buck1\_101}}$          | Peak switching current limit @ VIN12 = 14 V                | BUCK1_IPEAK=101                                                                                                                                                                                 | 3.5   | 4.5  | 5.175 | A    |
| $I_{\text{limit\_buck1\_11X}}$          | Peak switching current limit @ VIN12 = 14 V                | BUCK1_IPEAK=11X                                                                                                                                                                                 | 3.75  | 5    | 5.75  | A    |
| $t_{\text{buck1\_OC\_TO}}^{(2)}$        | Overcurrent filter time                                    |                                                                                                                                                                                                 | 125   | 150  | 200   | μs   |
| $T_{\text{softstart\_buck1\_00}}^{(3)}$ | Soft-start time slope when start-up                        | BUCK1_SS_VALUE=00                                                                                                                                                                               | 9.9   | 16.5 | 23.1  | V/ms |
| $T_{\text{softstart\_buck1\_01}}^{(3)}$ | Soft start time slope when start-up                        | BUCK1_SS_VALUE=01                                                                                                                                                                               | 4.95  | 8.25 | 11.9  | V/ms |
| $T_{\text{softstart\_buck1\_10}}^{(1)}$ | Soft start time slope when start-up                        | BUCK1_SS_VALUE=10                                                                                                                                                                               | 1.98  | 3.3  | 4.62  | V/ms |
| $T_{\text{softstart\_buck1\_11}}^{(3)}$ | Soft start time slope when start-up                        | BUCK1_SS_VALUE=11                                                                                                                                                                               | 0.99  | 1.65 | 2.31  | V/ms |
| $F_{\text{sw\_buck1\_0}}$               | Switching frequency                                        | BUCK1_FREQ=0                                                                                                                                                                                    | 2.0   | 2.4  | 2.8   | MHz  |
| $F_{\text{sw\_buck1\_1}}$               | Switching frequency                                        | BUCK1_FREQ=1                                                                                                                                                                                    | 333   | 400  | 470   | kHz  |
| $F_{\text{spread\_buck1\_24}}^{(3)}$    | Spread-spectrum range (enable/disable by BUCK1_SPREAD_ENA) | $F_{\text{sw\_buck1}} = 2.4 \text{ MHz}$                                                                                                                                                        | -30   |      | +30   | %    |
| $F_{\text{spread\_buck1\_04}}^{(3)}$    | Spread spectrum range (Enable/disable by BUCK1_SPREAD_ENA) | $F_{\text{sw\_buck1}} = 400 \text{ kHz}$                                                                                                                                                        | -30   |      | +30   | %    |
| RPD_OFF_buck1                           | Pull-down resistor in Off                                  | $V_{\text{OUT}} = 3.3 \text{ V}$                                                                                                                                                                | 55    | 70   | 90    | Ω    |
| $I_{\text{buck1\_LP}}$                  | Output current in LOW-POWER mode                           | $V_{\text{IN12}} = 14 \text{ V}$                                                                                                                                                                |       |      | 100   | mA   |
| $V_{\text{buck1\_LP\_00}}$              | Output voltage in LOW-POWER mode                           | BUCK1_PU_VALUE= 00<br>Line/Load transients not included<br>Ripple included<br>$V_{\text{IN12}} = 8.5 \text{ V to } 16 \text{ V}$ , $I_{\text{LOAD}} = 50 \mu\text{A to } I_{\text{Buck1\_LP}}$  | 3.15  | 3.3  | 3.45  | V    |
| $V_{\text{buck1\_LP\_01}}$              | Output voltage in LOW-POWER mode                           | BUCK1_PU_VALUE = 01<br>Line/Load transients not included<br>Ripple included<br>$V_{\text{IN12}} = 8.5 \text{ V to } 16 \text{ V}$ , $I_{\text{LOAD}} = 50 \mu\text{A to } I_{\text{Buck1\_LP}}$ | 4.75  | 5    | 5.25  | V    |
| $V_{\text{buck1\_LP\_1X}}$              | Output voltage in LOW-POWER mode                           | BUCK1_PU_VALUE = 1x<br>Line/Load transients not included<br>Ripple included<br>$V_{\text{IN12}} = 8.5 \text{ V to } 16 \text{ V}$ , $I_{\text{LOAD}} = 50 \mu\text{A to } I_{\text{Buck1\_LP}}$ | 6.22  | 6.5  | 6.78  | V    |
| $I_{\text{sw\_limit\_buck1\_LP}}$       | Peak current limit in LP mode                              |                                                                                                                                                                                                 | 900   | 1250 | 1500  | mA   |
| $V_{\text{out\_UV\_buck1\_LP\_33}}$     | Output undervoltage threshold monitor in LP mode           | $V_{\text{OUT}} = 3.3 \text{ V}$                                                                                                                                                                | 2.75  | 2.9  | 3.05  | V    |

| Symbol                           | Parameter                                        | Condition                                     | Min  | Typ  | Max  | Unit     |
|----------------------------------|--------------------------------------------------|-----------------------------------------------|------|------|------|----------|
| $V_{out\_UV\_buck1\_LP\_5}$      | Output undervoltage threshold monitor in LP mode | $V_{OUT} = 5\text{ V}$                        | 4.15 | 4.35 | 4.65 | V        |
| $V_{out\_UV\_buck1\_LP\_65}$     | Output undervoltage threshold monitor in LP mode | $V_{OUT} = 6.5\text{ V}$                      | 5.45 | 5.65 | 5.85 | V        |
| $V_{out\_OV\_buck1\_LP\_33}$     | Output overvoltage threshold monitor in LP mode  | $V_{out} = 3.3\text{ V}$                      | 3.55 | 3.7  | 3.89 | V        |
| $V_{out\_OV\_buck1\_LP\_5}$      | Output overvoltage threshold monitor in LP mode  | $V_{out} = 5\text{ V}$                        | 5.4  | 5.65 | 5.85 | V        |
| $V_{out\_OV\_buck1\_LP\_65}$     | Output overvoltage threshold monitor in LP mode  | $V_{out} = 6.5\text{ V}$                      | 6.9  | 7.2  | 7.5  | V        |
| $R_{DS(on)\_HS\_buck1\_LP\_25}$  | HS switch ON resistance @ 0.1 A                  | $V_{IN12} = 14\text{ V}, T_J = 25\text{ °C}$  |      | 0.72 | 0.9  | $\Omega$ |
| $R_{DS(on)\_HS\_buck1\_LP\_130}$ | HS switch ON resistance @ 0.1 A                  | $V_{IN12} = 14\text{ V}, T_J = 130\text{ °C}$ |      |      | 1.3  | $\Omega$ |
| $R_{DS(on)\_LS\_buck1\_LP\_25}$  | LS switch ON resistance @ 0.1 A                  | $V_{IN12} = 14\text{ V}, T_J = 25\text{ °C}$  |      | 0.2  | 0.3  | $\Omega$ |
| $R_{DS(on)\_LS\_buck1\_LP\_130}$ | LS switch ON resistance @ 0.1A                   | $V_{IN12} = 14\text{ V}, T_J = 130\text{ °C}$ |      |      | 0.4  | $\Omega$ |

1. Verified by bench measurements. Performances verified in applicative conditions. Tested in static load conditions ( $I_{LOAD} = 150\text{ mA}$ ) at 400 kHz and 2.4 MHz.
2. Digital implementation guaranteed by SCAN test.
3. Guaranteed by design.

## 7.9 BUCK2 converter

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

$8.5\text{ V} \leq V_{IN12} \leq 29\text{ V}$ ,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Buck2 shares the same input as Buck1.

**Table 32. Buck2 converter**

| Symbol                       | Parameter                                               | Condition                                                                                                                                                                     | Min.  | Typ.  | Max.  | Unit          |
|------------------------------|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|---------------|
| $V_{IN12\_H}$                | Input voltage range                                     | $V_{out\_buck1} = 6.5\text{ V}$<br>(see Figure 59)                                                                                                                            | 8.7   | 14    | 29    | V             |
| $V_{IN12\_M}$                | Input voltage range                                     | $V_{out\_buck1} = 5\text{ V}$<br>(see Figure 58)                                                                                                                              | 7     | 14    | 29    | V             |
| $V_{IN12\_L}$                | Input voltage range                                     | $V_{out\_buck1} = 3.3\text{ V}$<br>(see Figure 57)                                                                                                                            | 5.2   | 14    | 29    | V             |
| $V_{out\_buck2\_33}^{(1)}$   | Output voltage                                          | BUCK2_PU_VALUE=00<br>Transients and ripple not included, $V_{IN12} = 8.5\text{ V}$ to $16\text{ V}$ , $I_{LOAD} = 50\text{ mA}$ to $1.5\text{ A}$<br>Freq. = $400\text{ kHz}$ | 3.23  | 3.3   | 3.399 | V             |
| $V_{out\_buck2\_5}^{(1)}$    | Output voltage                                          | BUCK2_PU_VALUE=01<br>Transients and ripple not included, $V_{IN12} = 8.5\text{ V}$ to $16\text{ V}$ , $I_{LOAD} = 50\text{ mA}$ to $1.5\text{ A}$<br>Freq. = $400\text{ kHz}$ | 4.9   | 5     | 5.15  | V             |
| $V_{out\_buck2\_65}^{(1)}$   | Output voltage                                          | BUCK2_PU_VALUE=1x<br>Transients and ripple not included, $V_{IN12} = 9.2\text{ V}$ to $16\text{ V}$ , $I_{LOAD} = 50\text{ mA}$ to $1.5\text{ A}$<br>Freq. = $400\text{ kHz}$ | 6.37  | 6.5   | 6.695 | V             |
| $V_{out\_UV\_buck2\_err}$    | Output undervoltage threshold monitor range             |                                                                                                                                                                               | 86    | 90    | 94    | %             |
| $V_{out\_PG\_buck2}$         | Output power-good threshold monitor range               |                                                                                                                                                                               | 88    | 92    | 96    | %             |
| $V_{out\_OV\_buck2\_err}$    | Output overvoltage threshold monitor range              |                                                                                                                                                                               | 103   | 107   | 111   | %             |
| $t_{buck2\_PG\_TO}^{(2)}$    | Output power-good timeout                               |                                                                                                                                                                               | 4.8   | 6     | 7.5   | ms            |
| $t_{buck2\_UV\_TO}^{(2)}$    | $V_{OUT}$ undervoltage time-out filter                  |                                                                                                                                                                               | 25    | 30    | 41    | $\mu\text{s}$ |
| $t_{buck2\_OV\_TO}^{(2)}$    | $V_{OUT}$ overvoltage time-out filter                   |                                                                                                                                                                               | 25    | 30    | 41    | $\mu\text{s}$ |
| $R_{DS(on)\_HS\_buck2\_25}$  | HS switch ON resistance @ $1.5\text{ A}$                | $V_{IN12} = 14\text{ V}$ , $T_J = 25\text{ }^{\circ}\text{C}$                                                                                                                 |       | 0.095 | 0.12  | $\Omega$      |
| $R_{DS(on)\_HS\_buck2\_130}$ | HS switch ON resistance @ $1.5\text{ A}$                | $V_{IN12} = 14\text{ V}$ , $T_J = 130\text{ }^{\circ}\text{C}$                                                                                                                |       |       | 0.165 | $\Omega$      |
| $R_{DS(on)\_LS\_buck2\_25}$  | LS switch ON resistance @ $1.5\text{ A}$                | $V_{IN12} = 14\text{ V}$ , $T_J = 25\text{ }^{\circ}\text{C}$                                                                                                                 |       | 0.095 | 0.12  | $\Omega$      |
| $R_{DS(on)\_LS\_buck2\_130}$ | LS switch ON resistance @ $1.5\text{ A}$                | $V_{IN12} = 14\text{ V}$ , $T_J = 130\text{ }^{\circ}\text{C}$                                                                                                                |       |       | 0.165 | $\Omega$      |
| $I_{limit\_buck2\_000}$      | Peak switching current limit @ $V_{IN12} = 14\text{ V}$ | BUCK2_IPEAK=000                                                                                                                                                               | 1.7   | 2     | 2.3   | A             |
| $I_{limit\_buck2\_001}$      | Peak switching current limit @ $V_{IN12} = 14\text{ V}$ | BUCK2_IPEAK=001                                                                                                                                                               | 2.125 | 2.5   | 2.875 | A             |

| Symbol                           | Parameter                                                  | Condition                                                                                                                        | Min.  | Typ. | Max.  | Unit |
|----------------------------------|------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|------|
| $I_{limit\_buck2\_010}$          | Peak switching current limit @ VIN12 = 14 V                | BUCK2_IPEAK=010                                                                                                                  | 2.55  | 3    | 3.45  | A    |
| $I_{limit\_buck2\_011}$          | Peak switching current limit @ VIN12 = 14 V                | BUCK2_IPEAK=011                                                                                                                  | 2.975 | 3.5  | 4.025 | A    |
| $I_{limit\_buck2\_100}$          | Peak switching current limit @ VIN12 = 14 V                | BUCK2_IPEAK=100                                                                                                                  | 3.2   | 4    | 4.6   | A    |
| $I_{limit\_buck2\_101}$          | Peak switching current limit @ VIN12 = 14 V                | BUCK2_IPEAK=101                                                                                                                  | 3.5   | 4.5  | 5.175 | A    |
| $I_{limit\_buck2\_11x}$          | Peak switching current limit @ VIN12 = 14 V                | BUCK2_IPEAK=11X                                                                                                                  | 3.75  | 5    | 5.75  | A    |
| $t_{buck2\_OC\_TO}^{(2)}$        | Overcurrent filter time                                    |                                                                                                                                  | 125   | 150  | 200   | μs   |
| $T_{softstart\_buck2\_00}^{(3)}$ | Soft start time slope when start-up                        | BUCK2_SS_VALUE=00                                                                                                                | 9.9   | 16.5 | 23.1  | V/ms |
| $T_{softstart\_buck2\_01}^{(3)}$ | Soft-start time slope when start-up                        | BUCK2_SS_VALUE=01                                                                                                                | 4.95  | 8.25 | 11.9  | V/ms |
| $T_{softstart\_buck2\_10}^{(3)}$ | Soft-start time slope when start-up                        | BUCK2_SS_VALUE=10                                                                                                                | 1.98  | 3.3  | 4.62  | V/ms |
| $T_{softstart\_buck2\_11}^{(3)}$ | Soft start time slope when start-up                        | BUCK2_SS_VALUE=11                                                                                                                | 0.99  | 1.65 | 2.31  | V/ms |
| $F_{sw\_buck2\_0}$               | Switching frequency                                        | BUCK2_FREQ=0                                                                                                                     | 2.0   | 2.4  | 2.8   | MHz  |
| $F_{sw\_buck2\_1}$               | Switching frequency                                        | BUCK2_FREQ=1                                                                                                                     | 333   | 400  | 470   | kHz  |
| $F_{spread\_buck2\_24}^{(3)}$    | Spread spectrum range (Enable/disable by BUCK2_SPREAD_ENA) | Fsw_buck2 = 2.4 MHz                                                                                                              | -30   |      | +30   | %    |
| $F_{spread\_buck2\_04(1)}$       | Spread spectrum range (Enable/disable by BUCK2_SPREAD_ENA) | Fsw_buck2 = 400 kHz                                                                                                              | -30   |      | +30   | %    |
| $\Phi_{buck2}^{(3)(2)}$          | Phase shift to BUCK1                                       |                                                                                                                                  |       | 225  |       | deg  |
| $RPD\_OFF\_buck2$                | Pull down resistor in Off                                  | Vout = 3.3 V                                                                                                                     | 55    | 70   | 90    | Ω    |
| $I_{buck2\_LP}$                  | Output current in LOW-POWER mode                           | VIN12 = 14 V                                                                                                                     |       |      | 100   | mA   |
| $V_{buck2\_LP\_00}$              | Output voltage in LOW-POWER mode                           | BUCK2_PU_VALUE= 00<br>Line/Load transients not included<br>Ripple included<br>VIN12 = 8.5 V to 16 V, Iload = 50 μA to IBuck2_LP  | 3.15  | 3.3  | 3.45  | V    |
| $V_{buck2\_LP\_01}$              | Output voltage in LOW-POWER mode                           | BUCK2_PU_VALUE = 01<br>Line/Load transients not included<br>Ripple included<br>VIN12 = 8.5 V to 16 V, Iload = 50 μA to IBuck2_LP | 4.75  | 5    | 5.25  | V    |
| $V_{buck2\_LP\_1X}$              | Output voltage in LOW-POWER mode                           | BUCK2_PU_VALUE = 1x<br>Line/Load transients not included<br>Ripple included<br>VIN12 = 8.5 V to 16 V, ILOAD = 50 μA to IBuck2_LP | 6.22  | 6.5  | 6.78  | V    |
| $I_{sw\_limit\_buck2\_LP}$       | Peak current limit in LP mode                              |                                                                                                                                  | 900   | 1250 | 1500  | mA   |

| Symbol                            | Parameter                                        | Condition                                                      | Min. | Typ. | Max. | Unit     |
|-----------------------------------|--------------------------------------------------|----------------------------------------------------------------|------|------|------|----------|
| $V_{out\_UV\_buck2\_LP\_33}$      | Output undervoltage threshold monitor in LP mode | $V_{OUT} = 3.3\text{ V}$                                       | 2.75 | 2.9  | 3.05 | V        |
| $V_{out\_UV\_buck2\_LP\_5}$       | Output undervoltage threshold monitor in LP mode | $V_{OUT} = 5\text{ V}$                                         | 4.15 | 4.35 | 4.65 | V        |
| $V_{out\_UV\_buck2\_LP\_65}$      | Output undervoltage threshold monitor in LP mode | $V_{OUT} = 6.5\text{ V}$                                       | 5.45 | 5.65 | 5.85 | V        |
| $V_{out\_OV\_buck2\_LP\_33}$      | Output overvoltage threshold monitor in LP mode  | $V_{OUT} = 3.3\text{ V}$                                       | 3.55 | 3.7  | 3.89 | V        |
| $V_{out\_OV\_buck2\_LP\_5}$       | Output overvoltage threshold monitor in LP mode  | $V_{OUT} = 5\text{ V}$                                         | 5.4  | 5.65 | 5.85 | V        |
| $V_{out\_OV\_buck2\_LP\_65}$      | Output overvoltage threshold monitor in LP mode  | $V_{OUT} = 6.5\text{ V}$                                       | 6.9  | 7.2  | 7.5  | V        |
| $R_{DS(on)}_{HS\_buck2\_LP\_25}$  | HS switch ON resistance @ 0.1 A                  | $V_{IN12} = 14\text{ V}$ , $T_J = 25\text{ }^{\circ}\text{C}$  |      | 0.72 | 0.9  | $\Omega$ |
| $R_{DS(on)}_{HS\_buck2\_LP\_130}$ | HS switch ON resistance @ 0.1 A                  | $V_{IN12} = 14\text{ V}$ , $T_J = 130\text{ }^{\circ}\text{C}$ |      |      | 1.3  | $\Omega$ |
| $R_{DS(on)}_{LS\_buck2\_LP\_25}$  | LS switch ON resistance @ 0.1 A                  | $V_{IN12} = 14\text{ V}$ , $T_J = 25\text{ }^{\circ}\text{C}$  |      | 0.25 | 0.3  | $\Omega$ |
| $R_{DS(on)}_{LS\_buck2\_LP\_130}$ | LS switch ON resistance @ 0.1 A                  | $V_{IN12} = 14\text{ V}$ , $T_J = 130\text{ }^{\circ}\text{C}$ |      |      | 0.4  | $\Omega$ |

1. Verified by bench measurements. Performances verified in applicative conditions. Tested in static load conditions ( $I_{LOAD} = 150\text{ mA}$ ) at 400 kHz and 2.4 MHz.
2. Digital implementation guaranteed by SCAN test.
3. Guaranteed by design.

Below are the efficiency curves for BUCK1 and BUCK2:

**Figure 49. Efficiency @ 400 kHz VIN 14.00 V**

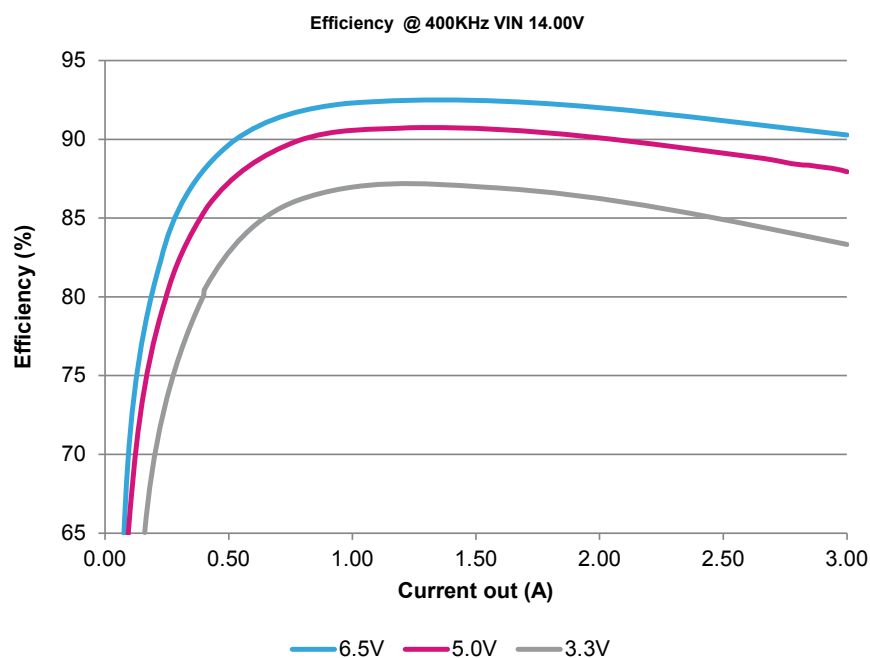
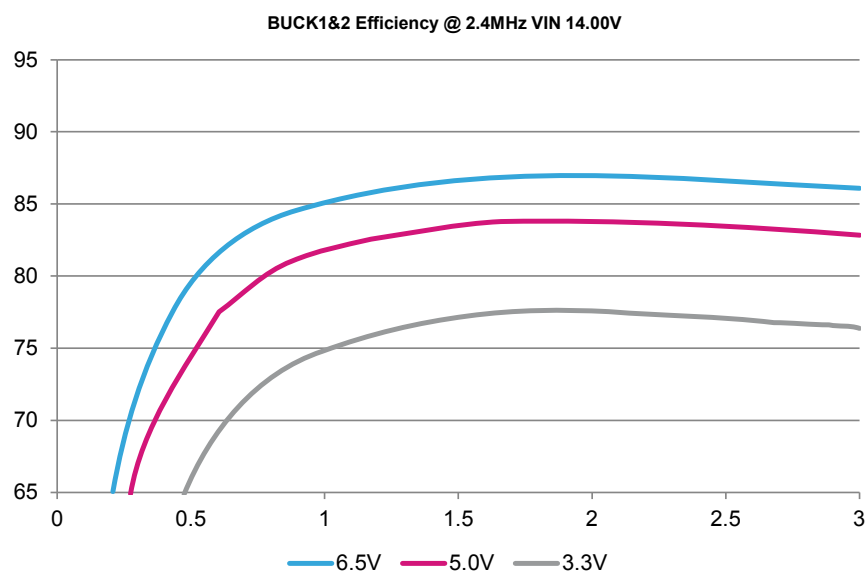


**Figure 50. BUCK1&2 Efficiency @ 2.4 MHz VIN 14.00 V**



Prerelease product(s)

See below the load and line transient curves for Buck1, 2:

**Figure 51.  $I_{LOAD}$  transient 0.05 A to 1.5 A in 50  $\mu$ s**

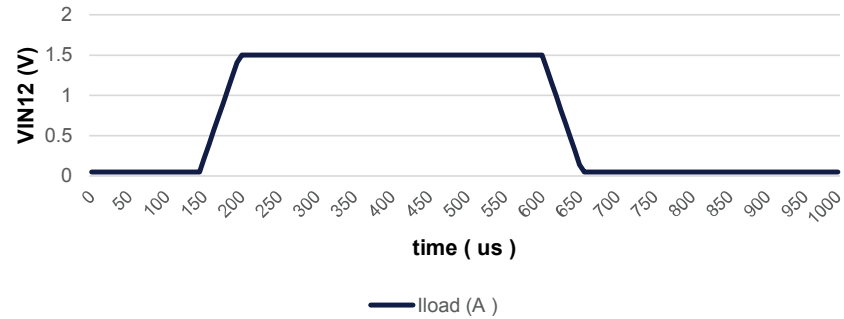


**Figure 52. Buck1&2 @ 400 kHz**

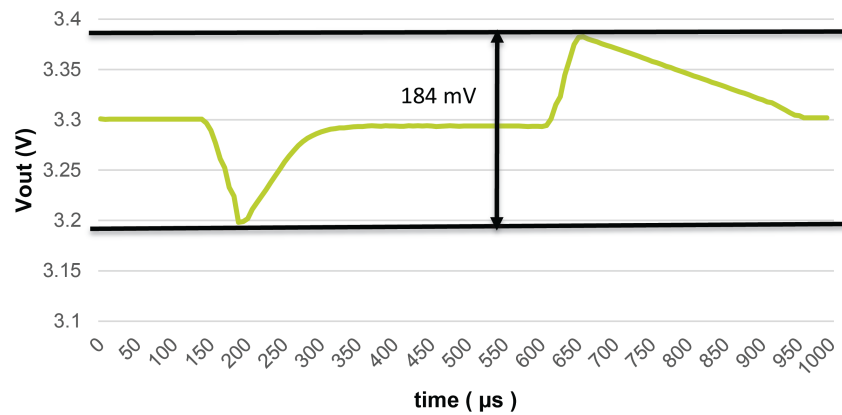


**Figure 53. Buck1&2 @ 2.4 MHz**

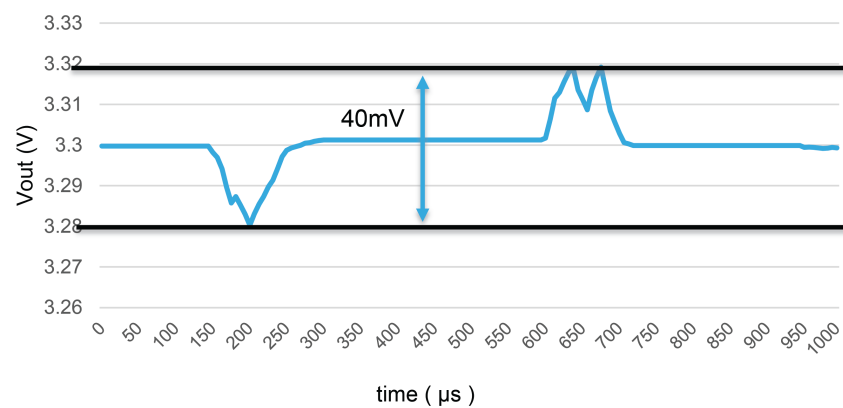


**Figure 54. Line transient 8 V to 16 V in 200  $\mu$ s**

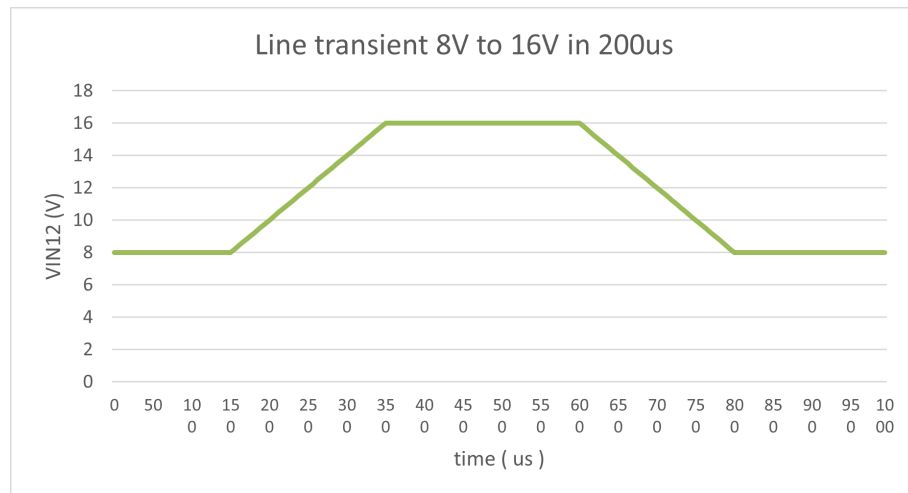


**Figure 55. Buck1&2 @ 400 kHz**

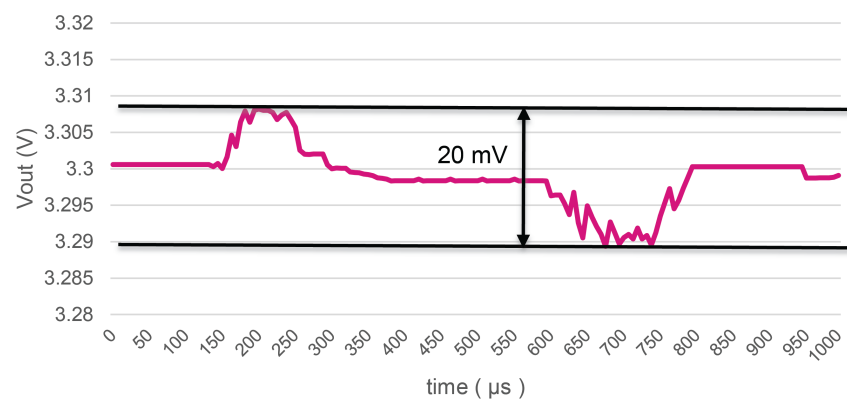
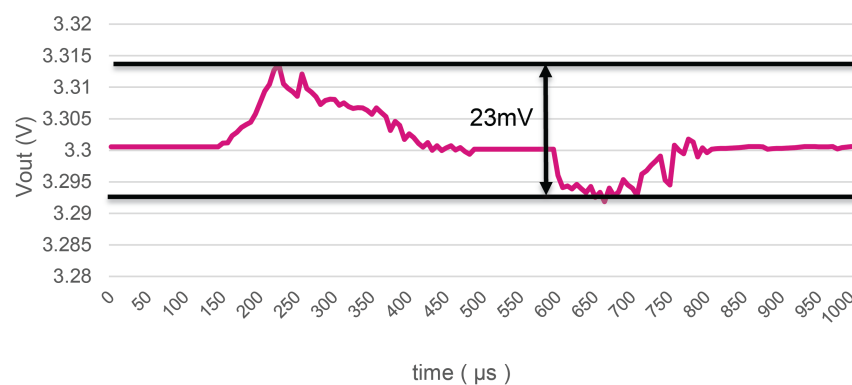


**Figure 56. Buck1&2 @ 2.4 MHz**



See below the current limitation curves for Buck1, 2 based on different input voltages:

**Figure 57. Current limitation curves of Buck1, 2 for  $V_{out}$  3.3 V**

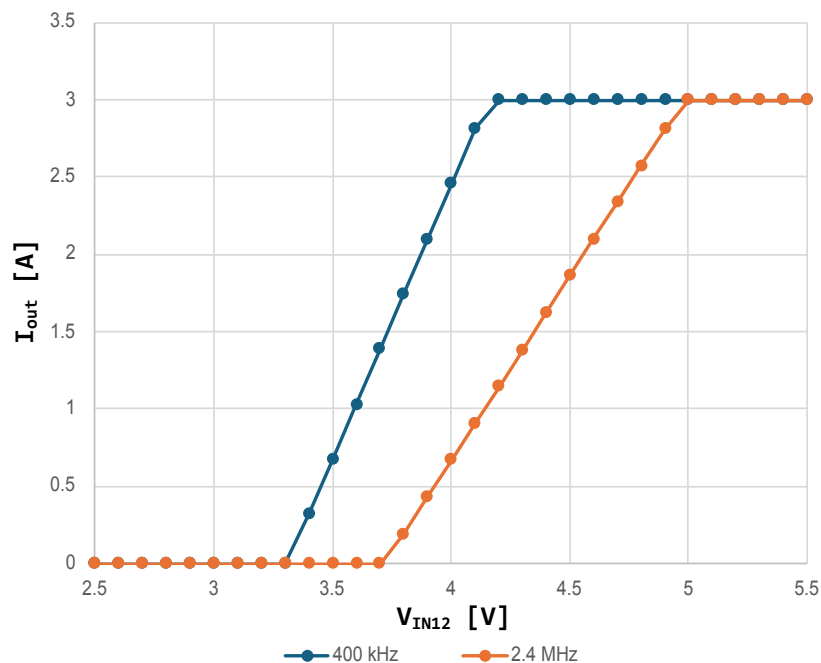


**Figure 58. Current limitation curves of Buck1, 2 for  $V_{out}$  5 V**

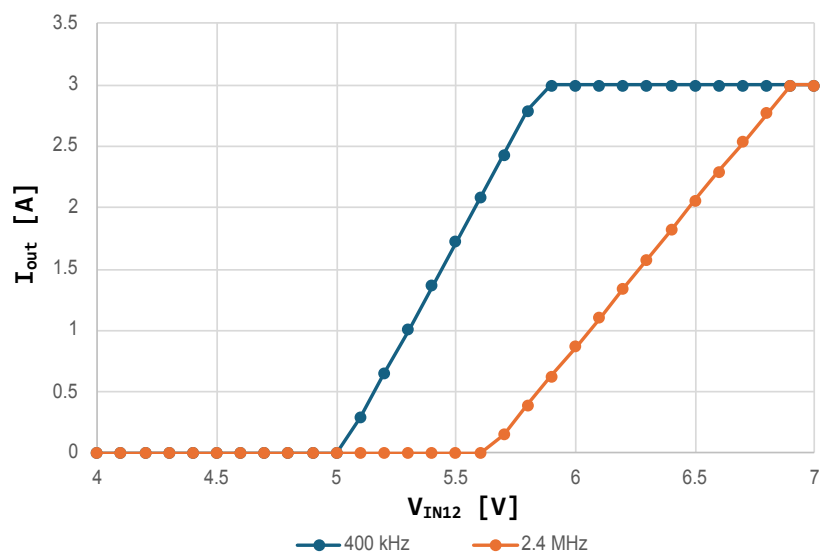
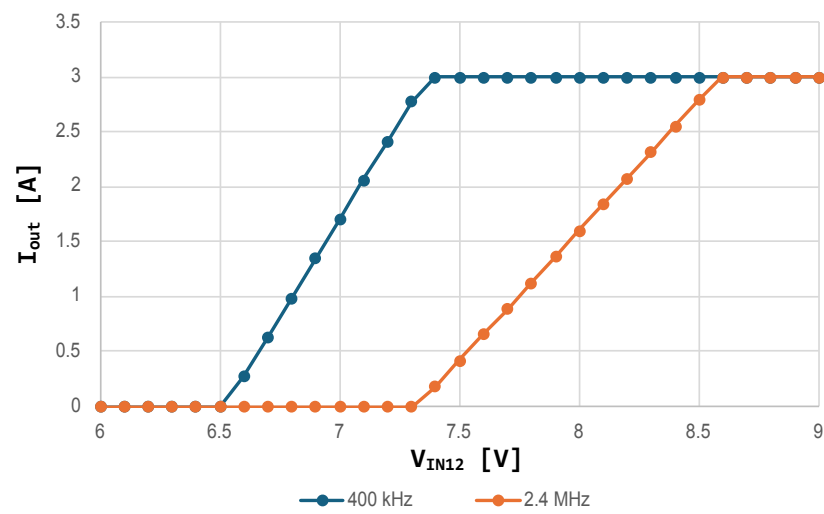


**Figure 59. Current limitation curves of Buck1, 2 for  $V_{out}$  6.5 V**



## 7.10 BUCK3 converter

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

$3\text{ V} \leq V_{\text{IN}3} \leq 5.25\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 33. BUCK3 converter**

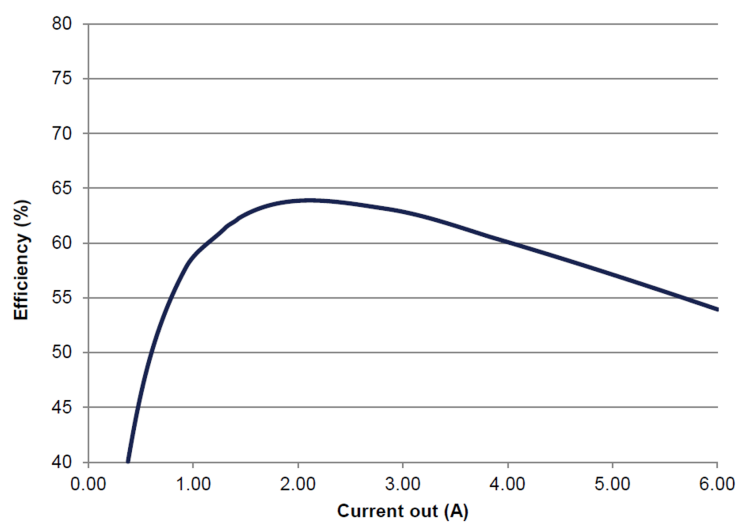
| Symbol                                          | Parameter                                                  | Condition                                                                                                                                       | Min   | Typ  | Max   | Unit          |
|-------------------------------------------------|------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|---------------|
| $V_{\text{in}3\_L}$ <sup>(1) (2)</sup>          | Input voltage range                                        |                                                                                                                                                 | 3     | -    | 5.25  | V             |
| $V_{\text{out\_buck3\_11X}}$ <sup>(1) (2)</sup> | Output voltage                                             | BUCK3_PU_VALUE = 1<br>BUCK3_FTUNE = 11X<br>$V_{\text{IN}3} = 3\text{ V}$ to $5.25\text{ V}$<br>$I_{\text{LOAD}} = 50\text{ mA}$ to $3\text{ A}$ | 0.955 | 0.99 | 1.025 | V             |
| $V_{\text{out\_buck3\_101}}$ <sup>(1) (2)</sup> | Output voltage                                             | BUCK3_PU_VALUE = 1<br>BUCK3_FTUNE = 101<br>$V_{\text{IN}3} = 3\text{ V}$ to $5.25\text{ V}$<br>$I_{\text{LOAD}} = 50\text{ mA}$ to $3\text{ A}$ | 0.965 | 1.0  | 1.035 | V             |
| $V_{\text{out\_buck3\_100}}$ <sup>(1) (2)</sup> | Output voltage                                             | BUCK3_PU_VALUE = 1<br>BUCK3_FTUNE = 100<br>$V_{\text{IN}3} = 3\text{ V}$ to $5.25\text{ V}$<br>$I_{\text{LOAD}} = 50\text{ mA}$ to $3\text{ A}$ | 0.975 | 1.01 | 1.045 | V             |
| $V_{\text{out\_buck3\_000}}$ <sup>(1) (2)</sup> | Output voltage                                             | BUCK3_PU_VALUE = 1<br>BUCK3_FTUNE = 000<br>$V_{\text{IN}3} = 3\text{ V}$ to $5.25\text{ V}$<br>$I_{\text{LOAD}} = 50\text{ mA}$ to $3\text{ A}$ | 0.985 | 1.02 | 1.055 | V             |
| $V_{\text{out\_buck3\_001}}$ <sup>(1) (2)</sup> | Output voltage                                             | BUCK3_PU_VALUE = 1<br>BUCK3_FTUNE = 001<br>$V_{\text{IN}3} = 3\text{ V}$ to $5.25\text{ V}$<br>$I_{\text{LOAD}} = 50\text{ mA}$ to $3\text{ A}$ | 0.995 | 1.03 | 1.065 | V             |
| $V_{\text{out\_buck3\_010}}$ <sup>(1) (2)</sup> | Output voltage                                             | BUCK3_PU_VALUE = 1<br>BUCK3_FTUNE = 010<br>$V_{\text{IN}3} = 3\text{ V}$ to $5.25\text{ V}$<br>$I_{\text{LOAD}} = 50\text{ mA}$ to $3\text{ A}$ | 1.005 | 1.04 | 1.075 | V             |
| $V_{\text{out\_buck3\_011}}$ <sup>(1) (2)</sup> | Output voltage                                             | BUCK3_PU_VALUE = 1<br>BUCK3_FTUNE = 011<br>$V_{\text{IN}3} = 3\text{ V}$ to $5.25\text{ V}$<br>$I_{\text{LOAD}} = 50\text{ mA}$ to $3\text{ A}$ | 1.015 | 1.05 | 1.085 | V             |
| $V_{\text{out\_UV\_buck3}}$                     | Output undervoltage threshold monitor range for fine-tune  | BUCK3_PU_VALUE = 1                                                                                                                              | 0.84  | -    | 0.94  | V             |
| $V_{\text{out\_PG\_buck3\_FT}}$                 | Output power-good threshold monitor range for fine-tune    | BUCK3_PU_VALUE = 1                                                                                                                              | 0.86  | -    | 0.955 | V             |
| $V_{\text{out\_OV\_buck3\_FT}}$                 | Output overvoltage threshold monitor range for fine-tuning | BUCK3_PU_VALUE = 1                                                                                                                              | 1.085 | -    | 1.165 | V             |
| $t_{\text{buck3\_PG\_TO}}$ <sup>(3)</sup>       | Output power-good timeout                                  |                                                                                                                                                 | 4.8   | 6    | 7.5   | ms            |
| $t_{\text{buck3\_UV\_TO}}$ <sup>(3)</sup>       | $V_{\text{OUT}}$ undervoltage timeout filter               |                                                                                                                                                 | 25    | 30   | 41    | $\mu\text{s}$ |

| Symbol                                                    | Parameter                                   | Condition                                                                       | Min   | Typ  | Max   | Unit          |
|-----------------------------------------------------------|---------------------------------------------|---------------------------------------------------------------------------------|-------|------|-------|---------------|
| $t_{\text{buck3\_OV\_TO}}$ <sup>(3)</sup>                 | $V_{\text{OUT}}$ overvoltage timeout filter |                                                                                 | 25    | 30   | 41    | $\mu\text{s}$ |
| $R_{\text{DS(on)}}_{\text{HS\_buck3\_25}}$ <sup>(2)</sup> | HS switch ON resistance at 3 A              | $V_{\text{IN3}} = 5 \text{ V}$<br>$T_{\text{J}} = 25 \text{ }^{\circ}\text{C}$  | -     | 0.04 | 0.08  | $\Omega$      |
| $R_{\text{DS(on)}}_{\text{HS\_buck3\_130}}$               | HS switch ON resistance at 3 A              | $V_{\text{IN3}} = 5 \text{ V}$<br>$T_{\text{J}} = 130 \text{ }^{\circ}\text{C}$ | -     | -    | 0.1   | $\Omega$      |
| $R_{\text{DS(on)}}_{\text{LS\_buck3\_25}}$                | LS switch ON resistance at 3 A              | $V_{\text{IN3}} = 5 \text{ V}$<br>$T_{\text{J}} = 25 \text{ }^{\circ}\text{C}$  | -     | 0.04 | 0.08  | $\Omega$      |
| $R_{\text{DS(on)}}_{\text{LS\_buck3\_130}}$               |                                             | $V_{\text{IN3}} = 5 \text{ V}$<br>$T_{\text{J}} = 130 \text{ }^{\circ}\text{C}$ | -     | -    | 0.1   | $\Omega$      |
| $I_{\text{limit\_buck3\_00}}$                             | Peak switching current limit                | BUCK3_IPEAK = 00                                                                | 3.4   | 4    | 4.6   | A             |
| $I_{\text{limit\_buck3\_01}}$                             | Peak switching current limit                | BUCK3_IPEAK = 01                                                                | 4.25  | 5    | 5.75  | A             |
| $I_{\text{limit\_buck3\_10}}$                             | Peak switching current limit                | BUCK3_IPEAK = 10                                                                | 5.1   | 6    | 6.9   | A             |
| $I_{\text{limit\_buck3\_11}}$                             | Peak switching current limit                | BUCK3_IPEAK = 11                                                                | 6.1   | 7    | 8.05  | A             |
| $t_{\text{buck3\_OC\_TO}}$ <sup>(3)</sup>                 | Overcurrent filter time                     |                                                                                 | 125   | 150  | 200   | $\mu\text{s}$ |
| $T_{\text{softstart\_buck3\_00}}$ <sup>(1)</sup>          | Soft-start time slope when start-up         | BUCK3_SS_VALUE = 00                                                             | 5.28  | 8.7  | 12.32 | V/ms          |
| $T_{\text{softstart\_buck3\_01}}$ <sup>(1)</sup>          | Soft-start time slope when start-up         | BUCK3_SS_VALUE = 01                                                             | 2.64  | 4.35 | 6.16  | V/ms          |
| $T_{\text{softstart\_buck3\_10}}$ <sup>(1)</sup>          | Soft-start time slope when start-up         | BUCK3_SS_VALUE = 10                                                             | 1.08  | 1.75 | 2.52  | V/ms          |
| $T_{\text{softstart\_buck3\_11}}$ <sup>(1)</sup>          | Soft-start time slope when start-up         | BUCK3_SS_VALUE = 11                                                             | 0.552 | 0.87 | 1.288 | V/ms          |
| $F_{\text{sw\_buck3}}$                                    | Switching frequency                         |                                                                                 | 2.0   | 2.4  | 2.8   | MHz           |
| $F_{\text{spread\_buck3}}$ <sup>(1)</sup>                 | Spread-spectrum range                       |                                                                                 | -30   | -    | +30   | %             |
| $\text{PHI\_buck3}$ <sup>(1)(3)</sup>                     | Phase shift to Buck1                        |                                                                                 | 200   | 250  | 300   | deg           |
| $\text{RPD\_OFF\_Buck3}$                                  | Pull-down resistor Off                      | $V_{\text{out}} = 3.3 \text{ V}$                                                | 105   | 130  | 180   | $\Omega$      |

1. *Guaranteed by design.*
2. *Verified by bench measurements. Performances verified in applicative conditions. Tested in static LOAD conditions ( $I_{\text{LOAD}} = 150 \text{ mA}$ ).*
3. *Digital implementation guaranteed by SCAN test.*

Below are the efficiency curves for Buck3:

**Figure 60. Buck3 efficiency at 1.02 V and VIN 3.30 V**



See below the load and line transient curves for Buck3:

**Figure 61.**  $I_{LOAD}$  transient 0.05 A to 3.0 A in 50  $\mu$ s

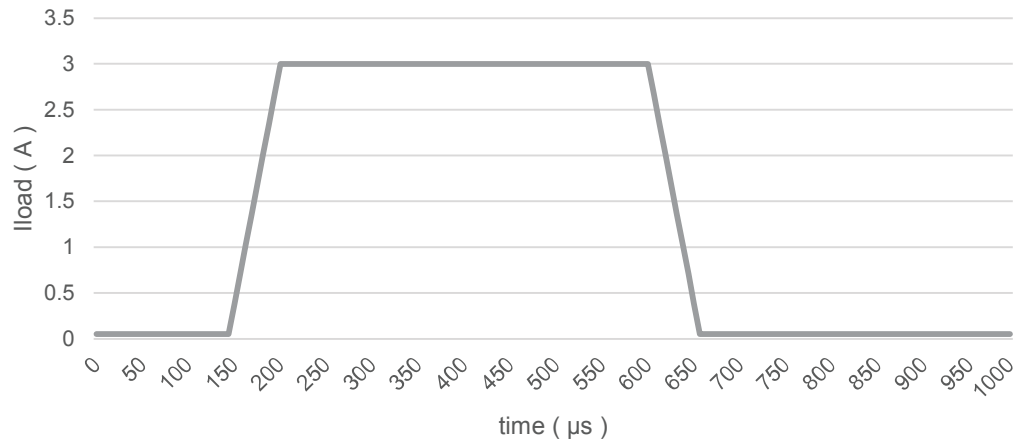


**Figure 62.** Buck3

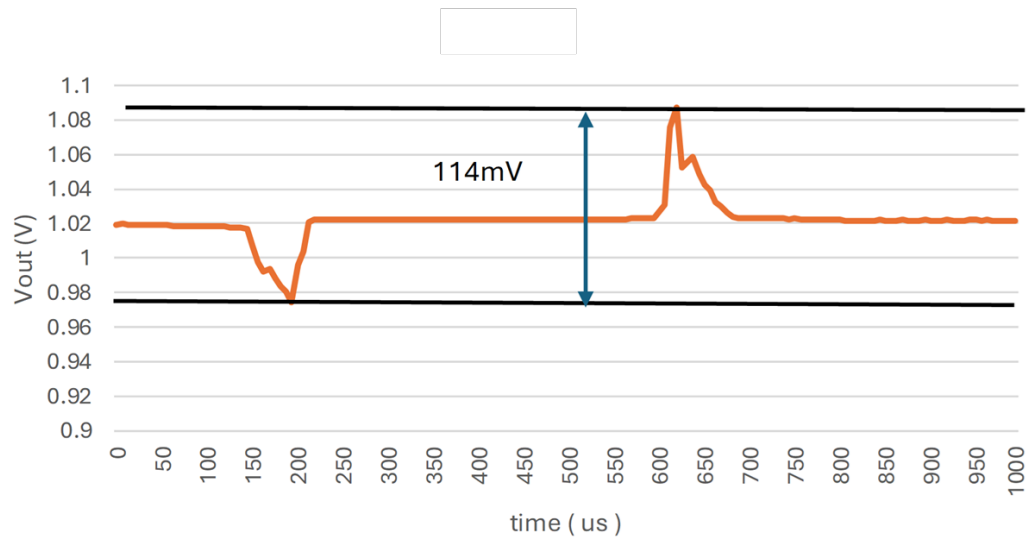


**Figure 63. Line transient from 3 V to 5.5 V in 200  $\mu$ s**

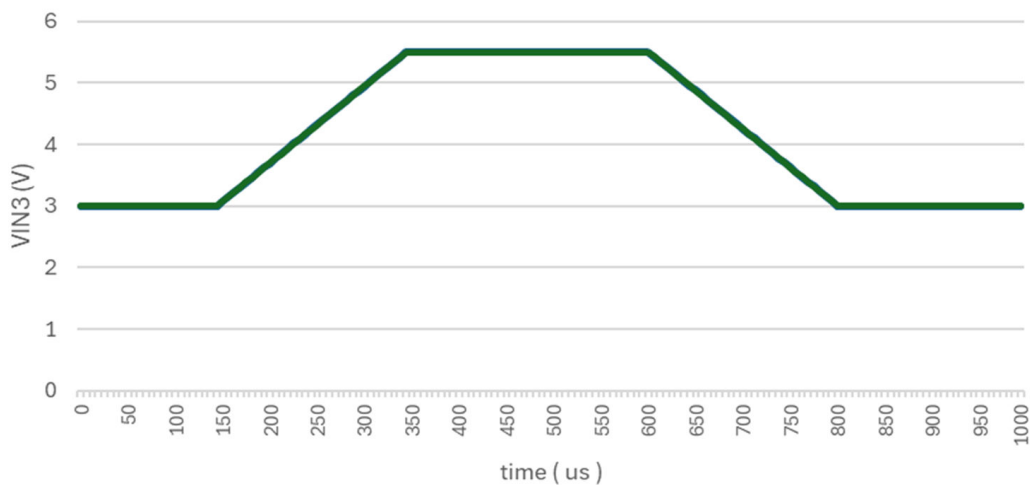
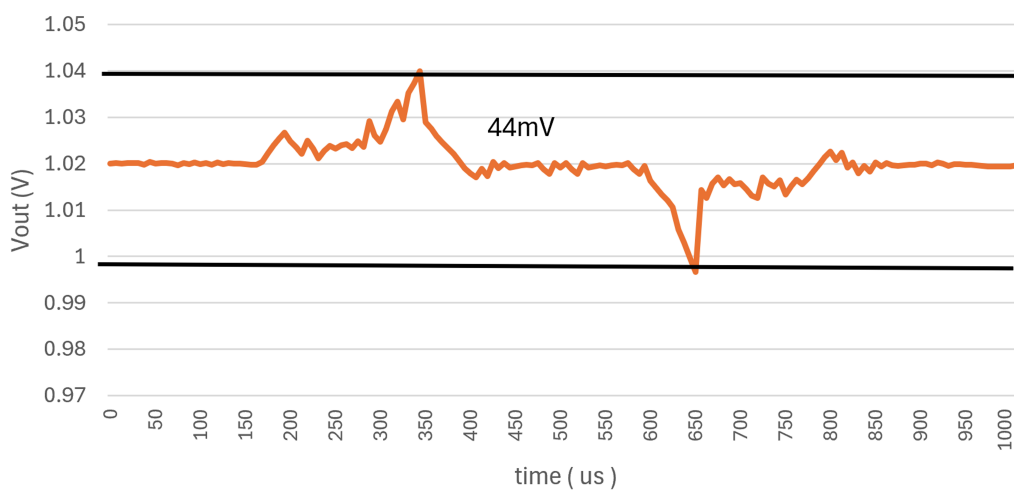


**Figure 64. Buck3**



## 7.11

### Watchdog

6.0 V ≤ V<sub>FBB</sub> ≤ 29 V, T<sub>j</sub> = -40 °C to 150 °C, unless otherwise specified.

All watchdog timings are covered by SCAN test.

**Table 34. Watchdog**

| Symbol                           | Parameter              | Condition                      | Min.  | Typ.     | Max.  | Unit |
|----------------------------------|------------------------|--------------------------------|-------|----------|-------|------|
| t <sub>LW1</sub> <sup>(1)</sup>  | Long open window 1     | LOW_SET <3:0> : 0000           | -     | -        | 319   | ms   |
| t <sub>LW2</sub> <sup>(1)</sup>  | Long open window 2     | LOW_SET <3:0> : 0001           | -     | -        | 479   | ms   |
| t <sub>LW3</sub> <sup>(1)</sup>  | Long open window 3     | LOW_SET <3:0> : 0010           | -     | -        | 638   | ms   |
| t <sub>LW4</sub> <sup>(1)</sup>  | Long open window 4     | LOW_SET <3:0> : 0011           | -     | -        | 1025  | ms   |
| t <sub>LW5</sub> <sup>(1)</sup>  | Long open window 5     | LOW_SET <3:0> : 0100           | -     | -        | 115   | ms   |
| t <sub>LW6</sub> <sup>(1)</sup>  | Long open window 6     | LOW_SET <3:0> : 0101           | -     | -        | 159   | ms   |
| t <sub>LW7</sub> <sup>(1)</sup>  | Long open window 7     | LOW_SET <3:0> : 0110           | -     | -        | 230   | ms   |
| t <sub>LW8</sub> <sup>(1)</sup>  | Long open window 8     | LOW_SET <3:0> : 0111           | -     | -        | 460   | ms   |
| t <sub>LW12</sub> <sup>(1)</sup> | Long open window 12    | LOW_SET <3:0> : 1000-1011      | -     | -        | 2300  | ms   |
| t <sub>LW13</sub> <sup>(1)</sup> | Long open window 13    | LOW_SET <3:0> : 1100           | -     | -        | 4600  | ms   |
| t <sub>LW14</sub> <sup>(1)</sup> | Long open window 14    | LOW_SET <3:0> : 1101           | -     | -        | 6900  | ms   |
| t <sub>LW15</sub> <sup>(1)</sup> | Long open window 15    | LOW_SET <3:0> : 1110           | -     | -        | 9200  | ms   |
| t <sub>LW16</sub>                | Long open window 16    | LOW_SET <3:0> : 1111           | -     | Infinite | -     | -    |
| T <sub>EFW1</sub>                | Early failure window 1 | WD_TIME = 0000                 | -     | -        | 2.8   | ms   |
| T <sub>LFW1</sub>                | Late failure window 1  | WD_TIME = 0000                 | 10    | -        | -     | ms   |
| T <sub>SW1</sub>                 | Safe window 1          | WD_TIME = 0000                 | 4.5   | -        | 5.4   | ms   |
| T <sub>EFW2</sub>                | Early failure window 2 | WD_TIME = 0001 (default value) | -     | -        | 5.3   | ms   |
| T <sub>LFW2</sub>                | Late failure window 2  | WD_TIME = 0001 (default value) | 20    | -        | -     | ms   |
| T <sub>SW2</sub>                 | Safe window 2          | WD_TIME = 0001 (default value) | 8.4   | -        | 11.5  | ms   |
| T <sub>EFW3</sub>                | Early failure window 3 | WD_TIME = 0010                 | -     | -        | 17.3  | ms   |
| T <sub>LFW3</sub>                | Late failure window 3  | WD_TIME = 0010                 | 50    | -        | -     | ms   |
| T <sub>SW3</sub>                 | Safe window 3          | WD_TIME = 0010                 | 27.1  | -        | 31.5  | ms   |
| T <sub>EFW4</sub>                | Early failure window 4 | WD_TIME = 0011                 | -     | -        | 31.5  | ms   |
| T <sub>LFW4</sub>                | Late failure window 4  | WD_TIME = 0011                 | 90    | -        | -     | ms   |
| T <sub>SW4</sub>                 | Safe window 4          | WD_TIME = 0011                 | 50.4  | -        | 56.8  | ms   |
| T <sub>EFW5</sub>                | Early failure window 5 | WD_TIME = 0100                 | -     | -        | 96.2  | ms   |
| T <sub>LFW5</sub>                | Late failure window 5  | WD_TIME = 0100                 | 250   | -        | -     | ms   |
| T <sub>SW5</sub>                 | Safe window 5          | WD_TIME = 0100                 | 151.1 | -        | 159.3 | ms   |
| T <sub>EFW6</sub>                | Early failure window 6 | WD_TIME = 0101                 | -     | -        | 197.1 | ms   |
| T <sub>LFW6</sub>                | Late failure window 6  | WD_TIME = 0101                 | 500   | -        | -     | ms   |
| T <sub>SW6</sub>                 | Safe window 6          | WD_TIME = 0101                 | 308.4 | -        | 319.3 | ms   |
| T <sub>EFW7</sub>                | Early failure window 7 | WD_TIME = 0110                 | -     | -        | 299.6 | ms   |
| T <sub>LFW7</sub>                | Late failure window 7  | WD_TIME = 0110                 | 750   | -        | -     | ms   |

| Symbol      | Parameter               | Condition           | Min.  | Typ. | Max.   | Unit |
|-------------|-------------------------|---------------------|-------|------|--------|------|
| $T_{SW7}$   | Safe window 7           | WD_TIME = 0110      | 468.1 | -    | 479.4  | ms   |
| $T_{EFW8}$  | Early failure window 8  | WD_TIME = 0111      | -     | -    | 402.1  | ms   |
| $T_{LFW8}$  | Late failure window 8   | WD_TIME = 0111      | 1000  | -    | -      | ms   |
| $T_{SW8}$   | Safe window 8           | WD_TIME = 0111      | 627.8 | -    | 638.7  | ms   |
| $T_{EFW9}$  | Early failure window 9  | WD_TIME = 1000      | -     | -    | 630.8  | ms   |
| $T_{LFW9}$  | Late failure window 9   | WD_TIME = 1000      | 1600  | -    | -      | ms   |
| $T_{SW9}$   | Safe window 9           | WD_TIME = 1000      | 984   | -    | 1025.1 | ms   |
| $T_{EFW10}$ | Early failure window 10 | WD_TIME = 1001-1111 | -     | -    | 3.2    | ms   |
| $T_{LFW10}$ | Late failure window 10  | WD_TIME = 1001-1111 | 78    | -    | -      | ms   |
| $T_{SW10}$  | Safe window 10          | WD_TIME = 1001-1111 | 5     | -    | 50     | ms   |

1.  $t_{LWn}$  defines the maximum timing to guarantee that a NRESET pulse will not be generated.

**Figure 65. Watchdog early, late and safe windows**

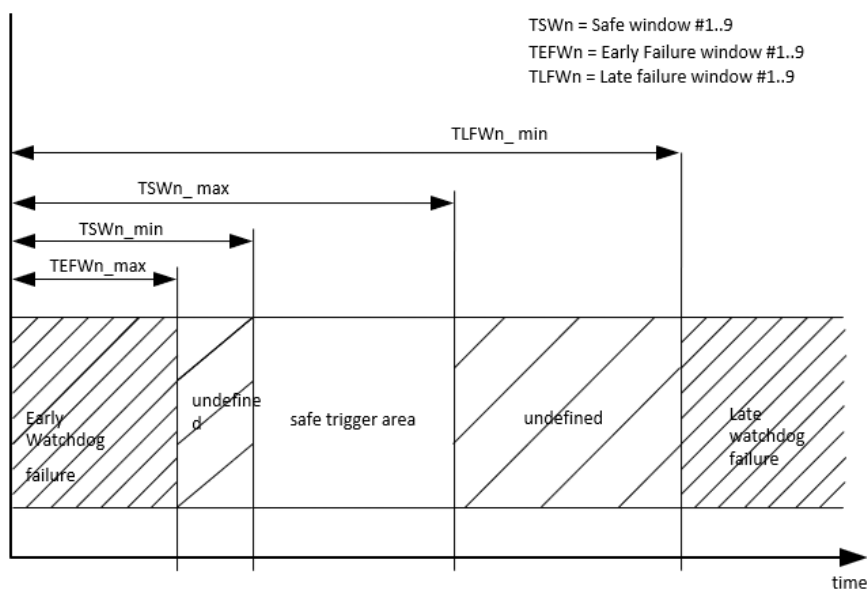
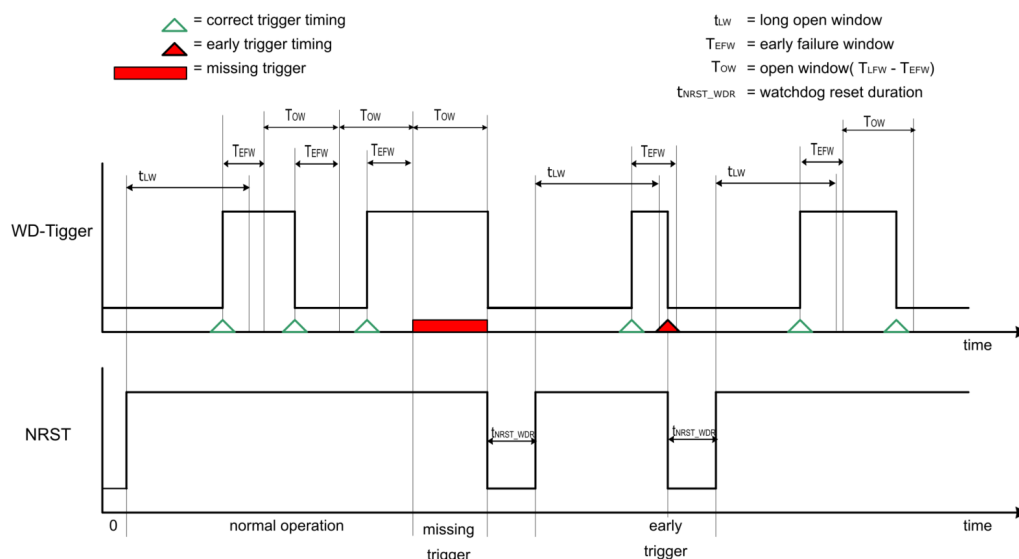


**Figure 66. Watchdog timing**


## 7.12 High-side output OUT\_HS

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_{FBB} \leq 29\text{ V}$ ;  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 35. High side Output OUT\_HS**

| Symbol                       | Parameter                                | Condition                                                                                                                | Min  | Typ | Max | Unit             |
|------------------------------|------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|------|-----|-----|------------------|
| $r_{ON\_OUT\_HS\_25}$        | Static drain source On-resistance        | $V_{FBB} = 13.5\text{ V}$ , $I_{LOAD} = -15\text{ mA}$ , $T_{amb} = +25\text{ }^{\circ}\text{C}$                         |      | 55  | 80  | $\Omega$         |
| $r_{ON\_OUT\_HS\_130}$       | Static drain source On-resistance        | $V_{FBB} = 13.5\text{ V}$ , $I_{LOAD} = -15\text{ mA}$ , $T_{amb} = +130\text{ }^{\circ}\text{C}$                        |      |     | 130 | $\Omega$         |
| $I_{OC\_OUT\_HS}$            | Overcurrent threshold                    | $V_{FBB} = 13.5\text{ V}$                                                                                                | 25   | 33  | 40  | mA               |
| $t_{OC\_OUT\_HS}^{(1)}$      | Overcurrent filter time                  |                                                                                                                          | 16   | 28  | 40  | $\mu\text{s}$    |
| $t_{BLK\_OC\_OUT\_HS}^{(1)}$ | Blanking time of over-current            | In case of short at enable (to be added to filter time for the minimum $t_{ON}$ )                                        | 32   | 46  | 60  | $\mu\text{s}$    |
| $I_{OLD\_OUT\_HS}$           | Open-load detection current              | $V_{FBB} = 13.5\text{ V}$                                                                                                | 0.25 | 0.7 | 1.3 | mA               |
| $t_{OLD\_OUT\_HS}^{(1)}$     | Open-load detection time                 |                                                                                                                          | 45   | 70  | 95  | $\mu\text{s}$    |
| $dV_{OUT\_HS}/dt$            | Slew rate                                | $V_{FBB} = 13.5\text{ V}$ , $R_{load} = 620\text{ }\Omega$ , $C_{load} = 47\text{ nF}$ , from 20% to 80 %                | 0.05 | 0.8 | 2   | V/ $\mu\text{s}$ |
| $t_{DON\_OUT\_HS}$           | Switch ON delay time                     | $V_{FBB} = 13.5\text{ V}$ , (from CSN rising 50% to OUT 80 %) $R_{load} = 620\text{ }\Omega$ , $C_{load} = 47\text{ nF}$ | 5    | 20  | 40  | $\mu\text{s}$    |
| $t_{DOFF\_OUT\_HS}$          | Switch OFF delay time                    | $V_{FBB} = 13.5\text{ V}$ ; (from CSN rising 50% to OUT 20 %) $R_{load} = 620\text{ }\Omega$ ; $C_{load} = 47\text{ nF}$ | 10   | 60  | 100 | $\mu\text{s}$    |
| $I_{QLH\_OUT\_HS\_LP}$       | Switched-off output Current in LOW-POWER | $V_{OUT\_HS} = 0\text{ V}$ ; ACTIVE - LOW-POWER or DEEP-SLEEP modes                                                      | -5   |     |     | $\mu\text{A}$    |
| $I_{QLH\_OUT\_HS\_FP}$       | Switched-off output                      | $V_{OUT\_HS} = 0\text{ V}$ ;                                                                                             | -10  |     |     | $\mu\text{A}$    |

| Symbol | Parameter             | Condition                | Min | Typ | Max | Unit |
|--------|-----------------------|--------------------------|-----|-----|-----|------|
|        | Current in FULL-POWER | ACTIVE - FULL-POWER mode |     |     |     |      |

1. Digital implementation guaranteed by SCAN test.

### 7.13 NFSO1 fail-safe output

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  
 $6.0\text{ V} \leq V_{\text{FBB}} \leq 40\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 36. Low side outputs**

| Symbol                        | Parameter                 | Condition                        | Min | Typ | Max | Unit             |
|-------------------------------|---------------------------|----------------------------------|-----|-----|-----|------------------|
| $V_{\text{NFSO1\_L}}$         | Output low level          | $I_{\text{NFSO1}} = 4\text{ mA}$ | -   | -   | 0.5 | V                |
| $I_{\text{NFSO1\_LK}}$        | Tristate leakage current  | $V_{\text{NFSO1}} = 40\text{ V}$ | -   | -   | 10  | $\mu\text{A}$    |
| $t_{\text{NFSO1\_rt}}$        | Detection reaction time   |                                  | -   | -   | 200 | $\mu\text{s}$    |
| $R_{\text{NFSO1\_PU}}$        | External pull-up resistor |                                  | -   | 30  | -   | $\text{k}\Omega$ |
| $t_{\text{NFSO\_ECHO\_FILT}}$ | Echo error filter time    | On falling edge                  | 91  | 100 | 150 | $\mu\text{s}$    |

## 7.14 Wake-up inputs (WU, IGN)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

$6.0\text{ V} \leq V_{FBB} \leq 29\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 37. Wake-up Inputs**

| Symbol                | Parameter                                                 | Condition                                                                                                                                 | Min. | Typ. | Max. | Unit          |
|-----------------------|-----------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $V_{WUthp}$           | Wake-up falling edge threshold voltage                    | $V_{thp\ min} = V_{FBB} * 0.4$<br>$V_{thp\ typ} = V_{FBB} * 0.45$<br>$V_{thp\ max} = V_{FBB} * 0.5$<br>Value for $V_{FBB} = 14\text{ V}$  | 5.6  | 6.3  | 7    | V             |
| $V_{IGNthp}$          | Wake-up falling edge threshold voltage                    | $V_{thp\ min} = V_{FBB} * 0.4$<br>$V_{thp\ typ} = V_{FBB} * 0.45$<br>$V_{thp\ max} = V_{FBB} * 0.5$<br>Value for $V_{FBB} = 14\text{ V}$  | 5.6  | 6.3  | 7    | V             |
| $V_{WUthn}$           | Wake-up rising edge threshold voltage                     | $V_{thp\ min} = V_{FBB} * 0.5$<br>$V_{thp\ typ} = V_{FBB} * 0.55$<br>$V_{thp\ max} = V_{FBB} * 0.6$<br>Value for $V_{FBB} = 14\text{ V}$  | 7    | 7.7  | 8.4  | V             |
| $V_{IGNthn}$          | Wake-up rising edge threshold voltage                     | $V_{thp\ min} = V_{FBB} * 0.5$<br>$V_{thp\ typ} = V_{FBB} * 0.55$<br>$V_{thp\ max} = V_{FBB} * 0.6$<br>Value for $V_{FBB} = 14\text{ V}$  | 7    | 7.7  | 8.4  | V             |
| $V_{HYST\_WU}$        | Hysteresis                                                | $V_{thp\ min} = V_{FBB} * 0.05$<br>$V_{thp\ typ} = V_{FBB} * 0.1$<br>$V_{thp\ max} = V_{FBB} * 0.15$<br>Value for $V_{FBB} = 14\text{ V}$ | 0.7  | 1.4  | 2.1  | V             |
| $V_{HYST\_IGN}$       | Hysteresis                                                | $V_{thp\ min} = V_{FBB} * 0.05$<br>$V_{thp\ typ} = V_{FBB} * 0.1$<br>$V_{thp\ max} = V_{FBB} * 0.15$<br>Value for $V_{FBB} = 14\text{ V}$ | 0.7  | 1.4  | 2.1  | V             |
| $t_{WU\_stat}^{(1)}$  | Static wake filter time                                   |                                                                                                                                           | 50   | 64   | 85   | $\mu\text{s}$ |
| $t_{IGN\_stat}^{(1)}$ | Static wake filter time                                   |                                                                                                                                           | 50   | 64   | 85   | $\mu\text{s}$ |
| $I_{WU\_stdby}$       | Input current in DEEP-SLEEP or ACTIVE LOW-POWER mode      | $V_{WU} < 1\text{ V}$<br>or $V_{WU} > (V_{FBB} - 1.5\text{ V})$<br>$WU\_ENA = 0$                                                          | -    | -    | 3    | $\mu\text{A}$ |
| $I_{IGN\_stdby}$      | Input current in DEEP-SLEEP or ACTIVE LOW-POWER mode      | $V_{IGN} < 1\text{ V}$<br>or $V_{IGN} > (V_{FBB} - 1.5\text{ V})$<br>$IGN\_ENA = 0$                                                       | -    | -    | 3    | $\mu\text{A}$ |
| $I_{WU\_stdby\_PD}$   | Pull-down current in DEEP-SLEEP or ACTIVE LOW-POWER modes | $V_{WU} < 1\text{ V}$<br>or $V_{WU} > (V_S - 1.5\text{ V})$<br>$WU\_ENA = 1$                                                              | 5    | 20   | 60   | $\mu\text{A}$ |

| Symbol               | Parameter                                                                                                    | Condition                                                                       | Min. | Typ. | Max. | Unit             |
|----------------------|--------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------|------|------|------|------------------|
| $I_{WU\_stdby\_PU}$  | Pull-up current in DEEP-SLEEP or ACTIVE LOW-POWER modes                                                      | $V_{WU} < 1\text{ V}$<br>or $V_{WU} > (V_S - 1.5\text{ V})$<br>$WU\_ENA = 1$    | -60  | -20  | -5   | $\mu\text{A}$    |
| $I_{IGN\_stdby\_PD}$ | Pull-down current in DEEP-SLEEP or ACTIVE LOW-POWER modes                                                    | $V_{IGN} < 1\text{ V}$<br>or $V_{IGN} > (V_S - 1.5\text{ V})$<br>$IGN\_ENA = 1$ | 5    | 20   | 60   | $\mu\text{A}$    |
| $I_{IGN\_stdby\_PU}$ | Pull-up current in DEEP-SLEEP or ACTIVE LOW-POWER modes                                                      | $V_{WU} < 1\text{ V}$<br>or $V_{WU} > (V_S - 1.5\text{ V})$<br>$WU\_ENA = 1$    | -60  | -20  | -5   | $\mu\text{A}$    |
| $R_{WU\_act}$        | Input resistor to GND in ACTIVE mode and in DEEP-SLEEP or ACTIVE LOW-POWER mode during wake-up input sensing |                                                                                 | 80   | 180  | 300  | $\text{k}\Omega$ |
| $R_{IGN\_act}$       | Input resistor to GND in ACTIVE mode and in DEEP-SLEEP or ACTIVE LOW-POWER mode during wake-up input sensing |                                                                                 | 80   | 180  | 300  | $\text{k}\Omega$ |
| $t_{WU\_cyc}^{(1)}$  | Cyclic wake filter time                                                                                      |                                                                                 | 12   | 16   | 29   | $\mu\text{s}$    |
| $t_{IGN\_cyc}^{(1)}$ | Cyclic wake filter time                                                                                      |                                                                                 | 12   | 16   | 29   | $\mu\text{s}$    |

1. Digital implementation guaranteed by SCAN test.

## 7.15 CAN FD transceiver (only for SPSB100GS)

ISO 11898-2:2016 compliant

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  $6\text{ V} < V_{FBB} < 29\text{ V}$ ;  $4.8\text{ V} < V_{LDO1} < 5.2\text{ V}$ ;  $3\text{ V} < V_{IO} < 5.5\text{ V}$ ;  $T_{junction} = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

$-12\text{ V} \leq (CANH + CANL) / 2 \leq 12\text{ V}$

**Table 38. CAN communication operating range**

| Symbol                 | Parameter                                                         | Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Min. | Typ. | Max. | Unit |
|------------------------|-------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $V_{FBB\_Transmitter}$ | Supply voltage operating range for CAN transmitter <sup>(1)</sup> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 6    |      | 29   | V    |
| $V_{FBB\_Receiver}$    | Supply voltage operating range for CAN receiver                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 6    |      | 29   | V    |
| $V_{CANSUPlow}$        | CAN supply low voltage flag                                       | $V_{LDO1}$ decreasing                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 4.1  | 4.3  | 4.5  | V    |
| $V_{CANHL,CM}$         | Common-mode bus voltage $(V_{CANH} + V_{CANL}) / 2$               | Measured with respect to the ground of each CAN transceiver                                                                                                                                                                                                                                                                                                                                                                                                                                             | -12  |      | 12   | V    |
| $I_{TRCV}$             | Transceiver current consumption during normal mode                | ACTIVE mode: $R_L = 50\text{ }\Omega \dots 65\text{ }\Omega$ ; 70% $V_{RxD\_C}$ (rising) - 30% $V_{RxD\_C}$ (falling); $CRxD\_C = 15\text{ pF}$ ; $TxD\_C$ rise and fall time = 10 ns (10% - 90%, 90% - 10%); Test signal to be applied on the TXD input of the implementation is a square wave signal with a positive duty cycle of 1/6, and a period of six times the nominal recessive bit width. Rectangular pulse signal $TTxD\_C = 6 * TBIT^{(2)}$ , high pulse $1 * TBIT$ , low pulse $5 * TBIT$ |      |      | 120  | mA   |
| $I_{TRCV\_short}$      | Transceiver current consumption during output short               | $R_L = 50\text{ }\Omega$ to $65\text{ }\Omega$ ; $V_{CANH} = -3\text{ V}$ or $V_{CANL} = 40\text{ V}$                                                                                                                                                                                                                                                                                                                                                                                                   |      |      | 120  | mA   |

| Symbol           | Parameter                                                               | Condition                                                             | Min. | Typ. | Max. | Unit    |
|------------------|-------------------------------------------------------------------------|-----------------------------------------------------------------------|------|------|------|---------|
| $I_{TRCVLPbias}$ | Transceiver current consumption; biasing active                         | $R_L = 50\ \Omega$ to $65\ \Omega$ ;<br>$V_{TxD\_C} = V_{TXDCHIGH}$ ; |      | 400  | 600  | $\mu A$ |
| $I_{TRCVLP}$     | Transceiver current consumption during LOW-POWER mode; biasing inactive | $R_L = 50\ \Omega$ to $65\ \Omega$ ;<br>$V_{TxD\_C} = V_{TXDCHIGH}$ ; |      |      | 50   | $\mu A$ |
| BR               | Supported bitrates                                                      | Supported bitrates at which all requirements are fulfilled            |      |      | 5    | Mb/s    |

- At  $V_{FBB} < V_{FBB\_Transmitter(min)}$  the transceiver shall enter high impedance state.
- The bit time  $T_{BIT}$  is the nominal bit time at a given bit rate ( $T_{BIT} = 1/BR$ ). E.g.: At  $BR = 2\text{Mb/s} \Rightarrow T_{BIT} = 500\text{ ns}$ .

**Table 39. CAN transmit data input: TxD\_C pin**

| Symbol          | Parameter                     | Condition       | Min | Typ  | Max | Unit       |
|-----------------|-------------------------------|-----------------|-----|------|-----|------------|
| $V_{TXDCLOW}$   | Input voltage dominant level  | ACTIVE mode     | 1.0 | 1.45 | 2.0 | V          |
| $V_{TXDCHIGH}$  | Input voltage recessive level | ACTIVE mode     | 1.2 | 1.85 | 2.3 | V          |
| $V_{TXDCHYS}$   | $V_{TXDCHIGH} - V_{TXDCLOW}$  | ACTIVE mode     | 0.2 | 0.4  | 0.7 | V          |
| $R_{TXDCPU}$    | TxD_C pull-up resistor        | ACTIVE mode     | 20  | 50   | 110 | k $\Omega$ |
| $t_{dom}(TXDC)$ | TxD_C dominant timeout        | Covered by SCAN | 0.8 | 2    | 5   | ms         |

**Table 40. CAN Receive Data Output: Pin RxD\_C**

| Symbol         | Parameter                      | Condition                                                         | Min | Typ | Max | Unit |
|----------------|--------------------------------|-------------------------------------------------------------------|-----|-----|-----|------|
| $V_{RXDCLOW}$  | Output voltage dominant level  | ACTIVE mode, $I_{RxD\_C} = 2\text{ mA}$                           | 0   | 0.2 | 0.5 | V    |
| $V_{RXDCHIGH}$ | Output voltage recessive level | ACTIVE mode, $I_{RxD\_C} = -2\text{ mA}$<br>$V_{IO} = 5\text{ V}$ | 4.5 | 4.8 | 5.0 | V    |
| $t_{r,RXDC}$   | RxD_C rise time                | $C_L = 15\text{ pF}$ ;<br>30% - 70% $V_{RxD\_C}$ <sup>(1)</sup>   | 0   |     | 25  | ns   |
| $t_{f,RXDC}$   | RxD_C fall time                | $C_L = 15\text{ pF}$ ;<br>70% - 30% $V_{RxD\_C}$ <sup>(1)</sup>   | 0   |     | 25  | ns   |

- Guaranteed by design.

**Table 41. CAN transmitter dominant output characteristics**

| Symbol          | Parameter                                                                                     | Condition                                                          | Min  | Typ | Max  | Unit |
|-----------------|-----------------------------------------------------------------------------------------------|--------------------------------------------------------------------|------|-----|------|------|
| $V_{CANHdom}$   | Single-ended CANH voltage level in dominant state                                             | $V_{TxD\_C} = V_{TXDCLOW}$ ; $R_L = 50\ \Omega$ to $65\ \Omega$    | 2.75 | 3.5 | 4.5  | V    |
| $V_{CANLdom}$   | Single-ended CANL voltage level in dominant state                                             | $V_{TxD\_C} = V_{TXDCLOW}$ ;<br>$R_L = 50\ \Omega$ to $65\ \Omega$ | 0.5  | 1.5 | 2.25 | V    |
| $V_{DIFF,dom}$  | Differential output voltage in dominant state: $V_{CANHdom} - V_{CANLdom}$                    | $V_{TxD\_C} = V_{TXDCLOW}$ ;<br>$R_L = 50\ \Omega$ to $65\ \Omega$ | 1.5  | 2.0 | 3    | V    |
| $V_{DIFF\_Arb}$ | Differential output voltage in dominant state during arbitration: $V_{CANHdom} - V_{CANLdom}$ | $V_{TxD\_C} = V_{TXDCLOW}$ ; $R_L = 2240\ \Omega$                  | 1.5  |     | 5    | V    |

| Symbol                     | Parameter                                                                                                                      | Condition                                                                                                          | Min  | Typ | Max | Unit |
|----------------------------|--------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|------|-----|-----|------|
| $V_{DIFF,dom\_ext}$        | Differential output voltage in dominant state in extended bus load range: $V_{CANHdom} - V_{CANLdom}$                          | $V_{TxD\_C} = V_{TXDCLOW}$ ; $R_L = 45\ \Omega$ to $70\ \Omega$                                                    | 1.4  |     | 3.3 | V    |
| $V_{DIFF,domVsLow}$        | Differential output voltage in dominant state: $V_{CANHdom} - V_{CANLdom}$ at low $V_S$                                        | $V_{TxD\_C} = V_{TXDCLOW}$ ; $R_L = 50\ \Omega$ to $65\ \Omega$ ; $3\ V < V_S$ and $6\ V < V_{FBB}$ <sup>(1)</sup> | 1.35 |     | 3   | V    |
| $V_{DIFF,dom\_ext\_VsLow}$ | Differential output voltage in dominant state: $V_{CANHdom} - V_{CANLdom}$ with $45\ \Omega$ to $70\ \Omega$ load at low $V_S$ | $V_{TxD\_C} = V_{TXDCLOW}$ ; $R_L = 45$ to $70\ \Omega$ ; $3\ V < V_S$ and $6\ V < V_{FBB}$ <sup>(1)</sup>         | 1.25 |     | 3.3 | V    |
| $V_{SYM}$                  | Driver symmetry <sup>(2)</sup><br>$V_{SYM} = (V_{CANH} + V_{CANL}) / V_{LDO1}$<br>$V_{LDO1} = 5\ V$                            | $R_L = 60\ \Omega \pm 1\%$ ; $f_{TXDC} = 1\ MHz$ ;<br>$C_{SPLIT} = 4.7\ nF$ (+-5%)                                 | 0.9  | 1   | 1.1 |      |
| $I_{OCANH,dom}(-3V)$       | CANH output current in dominant state                                                                                          | $V_{TxD\_C} = V_{TXDCLOW}$ ;<br>$V_{CANH} = -3\ V$ to $18\ V$                                                      | -115 |     | 115 | mA   |
| $I_{OCANL,dom}(18V)$       | CANL output current in dominant state                                                                                          | $V_{TxD\_C} = V_{TXDCLOW}$ ; $V_{CANL} = -3\ V$ to $18\ V$                                                         | -115 |     | 115 | mA   |
| $I_{OCANH,dom}(40V)$       | CANH output current in dominant state                                                                                          | $V_{TxD\_C} = V_{TXDCLOW}$ ; $V_{CANH} = 40\ V$ ; $V_S = 40\ V$                                                    | 0    |     | 15  | mA   |
| $I_{OCANL,dom}(40V)$       | CANL output current in dominant state                                                                                          | $V_{TxD\_C} = V_{TXDCLOW}$ ; $V_{CANL} = 40\ V$ ; $V_S = 40\ V$                                                    | 0    |     | 115 | mA   |

- $V_S$  at device pin after reverse battery protection, while application is supplied with 6 V. Operating condition has to be adapted if a higher voltage drop occurs in the application.
- Measurement equipment input load  $< 20\ pF$ ,  $> 1\ M\Omega$ .

**Table 42. CAN transmitter recessive output characteristics, normal and LP mode bias active**

| Symbol            | Parameter                                                                     | Condition                             | Min | Typ | Max | Unit |
|-------------------|-------------------------------------------------------------------------------|---------------------------------------|-----|-----|-----|------|
| $V_{CANHrec}$     | CANH voltage level in recessive state                                         | $V_{TxD\_C} = V_{TXDCHIGH}$ ; No load | 2   | 2.5 | 3   | V    |
| $V_{CANLrec}$     | CANL voltage level in recessive state                                         | $V_{TxD\_C} = V_{TXDCHIGH}$ ; No load | 2   | 2.5 | 3   | V    |
| $V_{DIFF,recOUT}$ | Differential output voltage in recessive state<br>$V_{CANHrec} - V_{CANLrec}$ | $V_{TxD\_C} = V_{TXDCHIGH}$ ; No load | -50 |     | 50  | mV   |

**Note:** CAN normal mode: tested in TRX normal state while the device is in ACTIVE mode.

**Table 43. CAN transmitter recessive output characteristics, LP mode bias inactive**

| Symbol              | Parameter                                                                     | Condition                             | Min  | Typ | Max | Unit |
|---------------------|-------------------------------------------------------------------------------|---------------------------------------|------|-----|-----|------|
| $V_{CANHrecLP}$     | CANH voltage level in recessive state                                         | $V_{TxD\_C} = V_{TXDCHIGH}$ ; No load | -0.1 | 0   | 0.1 | V    |
| $V_{CANLrecLP}$     | CANL voltage level in recessive state                                         | $V_{TxD\_C} = V_{TXDCHIGH}$ ; No load | -0.1 | 0   | 0.1 | V    |
| $V_{DIFF,recOUTLP}$ | Differential output voltage in recessive state<br>$V_{CANHrec} - V_{CANLrec}$ | $V_{TxD\_C} = V_{TXDCHIGH}$ ; No load | -200 |     | 200 | mV   |

**Table 44. CAN receiver input characteristics during CAN normal and LP mode bias active**

| Symbol           | Parameter                                                           | Condition                                                                                        | Min | Typ | Max | Unit |
|------------------|---------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $V_{THdom}$      | Differential receiver threshold voltage recessive to dominant state | $-12\text{ V} \leq V_{CANH} \leq 12\text{ V}$ ; $12\text{ V} \leq V_{CANL} \leq 12\text{ V}$     | 0.5 |     | 0.9 | V    |
| $V_{dom\_range}$ | Differential dominant input level voltage range                     | $-12\text{ V} \leq V_{CANH} \leq 12\text{ V}$ ;<br>$-12\text{ V} \leq V_{CANL} \leq 12\text{ V}$ | 0.9 |     | 10  | V    |
| $V_{THrec}$      | Differential receiver threshold voltage dominant to recessive state | $12\text{ V} \leq V_{CANH} \leq 12\text{ V}$ ;<br>$-12\text{ V} \leq V_{CANL} \leq 12\text{ V}$  | 0.5 |     | 0.9 | V    |
| $V_{rec\_range}$ | Differential recessive input level voltage range                    | $-12\text{ V} \leq V_{CANH} \leq 12\text{ V}$ ;<br>$-12\text{ V} \leq V_{CANL} \leq 12\text{ V}$ | -5  |     | 0.5 | V    |

**Note:** CAN normal mode: tested in TRX normal state while the device is in ACTIVE mode.

**Table 45. CAN receiver input characteristics during CAN LOW-POWER mode, biasing inactive**

| Symbol               | Parameter                                                           | Condition                                       | Min  | Typ | Max  | Unit |
|----------------------|---------------------------------------------------------------------|-------------------------------------------------|------|-----|------|------|
| $V_{THdomLP}$        | Differential receiver threshold voltage recessive to dominant state | $12\text{ V} \leq V_{CANH} \leq 12\text{ V}$ ;  | 0.4  |     | 1.15 | V    |
|                      |                                                                     | $-12\text{ V} \leq V_{CANL} \leq 12\text{ V}$   |      |     |      |      |
| $V_{dom\_range\_LP}$ | Differential dominant input level voltage range                     | $-12\text{ V} \leq V_{CANH} \leq 12\text{ V}$ ; | 1.15 |     | 10   | V    |
|                      |                                                                     | $-12\text{ V} \leq V_{CANL} \leq 12\text{ V}$   |      |     |      |      |
| $V_{THrecLP}$        | Differential receiver threshold voltage dominant to recessive state | $12\text{ V} \leq V_{CANH} \leq 12\text{ V}$ ;  | 0.4  |     | 1.15 | V    |
|                      |                                                                     | $-12\text{ V} \leq V_{CANL} \leq 12\text{ V}$   |      |     |      |      |
| $V_{rec\_range\_LP}$ | Differential recessive input level voltage range                    | $V \leq V_{CANH} \leq 12\text{ V}$ ;            | -5   |     | 0.4  | V    |
|                      |                                                                     | $-12\text{ V} \leq V_{CANL} \leq 12\text{ V}$   |      |     |      |      |

**Note:** CAN LOW-POWER mode, biasing inactive: tested in CAN TRX STDBY (bias off) state while the device is in ACTIVE-FULL-POWER mode, in ACTIVE-LOW-POWER mode or in DEEP-SLEEP mode.

**Table 46. CAN receiver input resistance and capacitance**

| Symbol           | Parameter                                        | Condition                                                                                                                                                                                          | Min   | Typ | Max  | Unit       |
|------------------|--------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|------|------------|
| $R_{diff}$       | Differential internal resistance                 | $V_{TXD\_C} = V_{TXDCHIGH}$ ; No Load<br>$R_{diff} = R_{CANH} + R_{CANL}$<br>$-2,0\text{ V} \leq V_{CANH} \leq +7,0\text{ V}$ ;<br>$-2,0\text{ V} \leq V_{CANL} \leq +7,0\text{ V}$ <sup>(1)</sup> | 12    |     | 100  | k $\Omega$ |
| $R_{CANH, CANL}$ | Single-ended internal resistance                 | $V_{TXD\_C} = V_{TXDCHIGH}$ ; No load<br>$-2,0\text{ V} \leq V_{CANH} \leq +7,0\text{ V}$ ;<br>$-2,0\text{ V} \leq V_{CANL} \leq +7,0\text{ V}$ <sup>(1)</sup>                                     | 6     |     | 50   | k $\Omega$ |
| $m_R$            | Internal resistance matching<br>$R_{CANH, CANL}$ | Biasing active; $V_{TXD\_C} = V_{TXDCHIGH}$ ; no load;<br>$m_R = 2 \times (R_{CAN\_H} - R_{CAN\_L}) / (R_{CAN\_H} + R_{CAN\_L})$                                                                   | -0.03 |     | 0.03 |            |

1. Voltage range is taken from ISO CD 16845-2 (high-speed medium access unit - Conformance test plan).

Note: CAN normal and LOW-POWER mode, biasing active: tested in TRX normal and CAN TRX STDBY (bias on) state while the device is in ACTIVE and LOW-POWER mode.

**Table 47. CAN Transceiver delay**

| Symbol                                           | Parameter                                                          | Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Min | Typ  | Max  | Unit |
|--------------------------------------------------|--------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|------|
| $t_{LOOP,hl}$                                    | Loop delay TxD_C to RxD_C (High to Low)                            | $5.5\text{ V} < V_{FBB} < 18\text{ V}$ ; $R_L = 60\ \Omega \pm 1\%$ ; $C_L = 100\text{ pF}$ ; $30\% V_{TXD\_C} - 30\% V_{RXD\_C}$ ; TxD_C fall time = 10 ns (90% - 10%); $C_{RXD\_C} = 15\text{ pF}$                                                                                                                                                                                                                                                                                                                               |     |      | 255  | ns   |
| $t_{LOOP,lh}$                                    | Loop delay TxD_C to RxD_C (Low to High)                            | $5.5\text{ V} < V_{FBB} < 18\text{ V}$ ; $R_L = 60\ \Omega \pm 1\%$ ; $C_L = 100\text{ pF}$ ; $70\% V_{TXD} - 70\% V_{RXD\_C}$ ; TxD_C rise time = 10 ns (10% - 90%); $C_{RXD\_C} = 15\text{ pF}$                                                                                                                                                                                                                                                                                                                                  |     |      | 255  | ns   |
| $t_{LOOP150,hl}$                                 | Loop delay TxD_C to RxD_C (High to Low) with 150 $\Omega$ bus load | $5.5\text{ V} < V_{FBB} < 18\text{ V}$ ; $R_L = 150\ \Omega$ ; $C_L = 100\text{ pF}$ ; $30\%$ ; $V_{TXD\_C} 30\% V_{RXD\_C}$ ; TxD_C fall time = 10 ns (90% - 10%); $C_{RXD\_C} = 15\text{ pF}$                                                                                                                                                                                                                                                                                                                                    |     |      | 255  | ns   |
| $t_{LOOP150,lh}$                                 | Loop delay TxD_C to RxD_C (Low to High) with 150 $\Omega$ bus load | $5.5\text{ V} V_{FBB} < 18\text{ V}$ ; $R_L = 150\ \Omega$ ; $C_L = 100\text{ pF}$ ; $70\% V_{TXD} - 70\% V_{RXD\_C}$ ; TxD_C rise time = 10 ns (10% - 90%); $C_{RXD\_C} = 15\text{ pF}$                                                                                                                                                                                                                                                                                                                                           |     |      | 255  | ns   |
| $T_{Bit(RXD)} \leq 1\text{ Mb/s}$ <sup>(1)</sup> | Recessive bit symmetry at RxD_C                                    | $5.5\text{ V} < V_{FBB} < 18\text{ V}$ ; $R_L = 60\ \Omega \pm 1\%$ ; $70\% V_{RXD\_C}$ (rising) - $30\% V_{TXD\_C}$ (falling); $C_L = 100\text{ pF}$ ; $C_{RXD\_C} = 15\text{ pF}$ ; TXD rise and fall time = 10 ns (10% - 90%, 90% - 10%); Test signal to be applied on the TXD input of the implementation is a square wave signal with a positive duty cycle of 1/6, and a period of six times the nominal recessive bit width. Rectangular pulse signal $T_{TXD\_C} = 6000\text{ ns}$ , high pulse 1000 ns, low pulse 5000 ns | 900 | 1000 | 1050 | ns   |
| $T_{Bit(RXD)}_{150\Omega} \leq 1\text{ Mb/s}$    | Recessive bit symmetry at RxD_C                                    | $R_L = 150\ \Omega$ ; other conditions as $T_{Bit(RXD)} \leq 1\text{ Mb/s}$ ; value may be obtained by characterization only.                                                                                                                                                                                                                                                                                                                                                                                                      | 800 |      | 1050 | ns   |

| Symbol                                              | Parameter                                                                                            | Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Min | Typ  | Max  | Unit          |
|-----------------------------------------------------|------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|---------------|
| $T_{\text{Bit(RXD)}} \leq 2\text{Mb/s}$             | Recessive bit symmetry at RxD_C                                                                      | Conditions as $T_{\text{Bit(RXD)}} \leq 1\text{Mb/s}$ . Rectangular pulse signal $T_{\text{TXD\_C}} = 3000\text{ ns}$ , high pulse 500 ns, low pulse 2500 ns                                                                                                                                                                                                                                                                                                                                                                                                     | 400 | 500  | 550  | ns            |
| $T_{\text{Bit(RXD)}_{150\Omega} \leq 2\text{Mb/s}}$ | Recessive bit symmetry at RxD_C                                                                      | $R_L = 150\ \Omega$ ; other conditions as $T_{\text{Bit(RXD)}} \leq 1\text{Mb/s}$ ; value may be obtained by characterization only.                                                                                                                                                                                                                                                                                                                                                                                                                              | 300 |      | 550  | ns            |
| $T_{\text{Bit(RXD)}} \leq 5\text{Mb/s}$             | Recessive bit symmetry at RxD_C                                                                      | Conditions as $T_{\text{Bit(RXD)}} \leq 1\text{Mb/s}$ . Rectangular pulse signal $T_{\text{TXD\_C}} = 1200\text{ ns}$ , high pulse 200 ns, low pulse 1000 ns                                                                                                                                                                                                                                                                                                                                                                                                     | 120 | 200  | 220  | ns            |
| $T_{\text{Bit(BUS)}} \leq 1\text{Mb/s}$             | Recessive bit symmetry at CAN-Bus                                                                    | $5.5\text{ V} < V_{\text{FBB}} < 18\text{ V}$ ; $R_L = 60\ \Omega \pm 1\%$ ; $V_{\text{DIFF}}: 0.5\text{ V (falling)} - 0.9\text{ V (rising)}$ ; $C_L = 100\text{ pF}$ ; $C_{\text{RXD\_C}} = 15\text{ pF}$ ; TXD rise and fall time = 10 ns (10% - 90%, 90% - 10%); Test signal to be applied on the TXD input of the implementation is a square wave signal with a positive duty cycle of 1/6 and a period of six times the nominal recessive bit width. Rectangular pulse signal $T_{\text{TXD\_C}} = 6000\text{ ns}$ , high pulse 1000 ns, low pulse 5000 ns | 935 | 1000 | 1030 | ns            |
| $T_{\text{Bit(BUS)}} \leq 2\text{Mb/s}$             | Recessive bit symmetry at CAN-Bus                                                                    | Conditions as $T_{\text{Bit(BUS)}} \leq 1\text{Mb/s}$ . Rectangular pulse signal $T_{\text{TXD\_C}} = 3000\text{ ns}$ , high pulse 500 ns, low pulse 2500 ns                                                                                                                                                                                                                                                                                                                                                                                                     | 435 | 500  | 530  | ns            |
| $T_{\text{Bit(BUS)}} \leq 5\text{Mb/s}$             | Recessive bit symmetry at CAN-Bus                                                                    | Conditions as $T_{\text{Bit(BUS)}} \leq 1\text{ Mb/s}$ . Rectangular pulse signal $T_{\text{TXD\_C}} = 1200\text{ ns}$ , high pulse 200 ns, low pulse 1000 ns                                                                                                                                                                                                                                                                                                                                                                                                    | 155 | 200  | 210  | ns            |
| $\Delta t_{\text{REC}} \leq 2\text{Mb/s}$           | Receiver Timing Symmetry ( $T_{\text{Bit(RXD)}} - T_{\text{Bit(BUS)}}$ )                             | $5.5\text{ V} < V_{\text{FBB}} < 18\text{ V}$ ; $R_L = 60\ \Omega \pm 1\%$ ; $C_L = 100\text{ pF}$ ; $C_{\text{RXD\_C}} = 15\text{ pF}$ ; Rectangular pulse signal $T_{\text{TXD\_C}} = 3000\text{ ns}$ , high pulse 500 ns, low pulse 2500 ns                                                                                                                                                                                                                                                                                                                   | -65 |      | 40   | ns            |
| $\Delta t_{\text{REC}} \leq 5\text{Mb/s}$           | Receiver timing symmetry ( $T_{\text{Bit(RXD)}} - T_{\text{Bit(BUS)}}$ )                             | $5.5\text{ V} < V_{\text{FBB}} < 18\text{ V}$ ; $R_L = 60\ \Omega \pm 1\%$ ; $C_L = 100\text{ pF}$ ; $C_{\text{RXD\_C}} = 15\text{ pF}$ ; Rectangular pulse signal $T_{\text{TXD\_C}} = 1200\text{ ns}$ , high pulse 200 ns, low pulse 1000 ns                                                                                                                                                                                                                                                                                                                   | -45 |      | 15   | ns            |
| $t_{\text{CAN}}^{(2)}$                              | CAN permanent dominant timeout                                                                       | Covered by SCAN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 580 | 700  | 1000 | $\mu\text{s}$ |
| $t_{\text{VCANSUPlow}}$                             | CAN_SUP_LOW filter time                                                                              | Covered by SCAN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 12  | 15   | 22   | $\mu\text{s}$ |
| $t_{\text{WUP\_DEEP\_SLEEP}}$                       | Time between WUP <sup>(3)</sup> in DEEP-SLEEP mode, on the CAN bus until start of power-up sequence. | Wake-up pattern up to first regulator ON in power-up sequence config1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 15  | 20   | 30   | ms            |

1.  $T_{\text{bit(RxD\_C)}}$  for the highest supported data rate has to be specified (1 Mb/s, 2Mb/s or 5 Mb/s).

2. At the expiration of this filter time a flag is set.

3. Time starts with the end of last dominant phase of the WUP.

**Table 48. Maximum leakage currents on CANH and CANL, unpowered**

| Symbol                         | Parameter                  | Condition                                                                                                                                                                                                                                                                                                  | Min | Typ | Max | Unit          |
|--------------------------------|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| $I_{\text{Leakage, CANH,105}}$ | Input leakage current CANH | Unpowered device; $V_{\text{CANH}} = 5\text{ V}$ ; $V_{\text{CANL}} = 5\text{ V}$ ; $V_{\text{FBB}} < V_{\text{FBB\_Transmitter(min)}}$ ; $V_{\text{FBB}}$ , $V_{\text{LDO1}}^{(1)}$ connected via $0\ \Omega$ to GND<br><br>$V_{\text{FBB}}$ , $V_{\text{LDO1}}$ connected via $47\text{ k}\Omega$ to GND | -10 |     | 10  | $\mu\text{A}$ |

| Symbol                          | Parameter                  | Condition                                                                                                                                                                                                                                                                                                                                              | Min | Typ | Max | Unit          |
|---------------------------------|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
|                                 |                            | $T_j = -40$ to $105\text{ }^{\circ}\text{C}$                                                                                                                                                                                                                                                                                                           |     |     |     |               |
| $I_{\text{Leakage, CANH, 130}}$ | Input leakage current CANH | Unpowered device; $V_{\text{CANH}} = 5\text{ V}$ ; $V_{\text{CANL}} = 5\text{ V}$ ; $V_{\text{FBB}} < V_{\text{FBB\_Transmitter(min)}}$ ;<br>$V_{\text{FBB}}$ , $V_{\text{LDO1}}^{(1)}$ connected via $0\text{ }\Omega$ to GND<br>$V_{\text{FBB}}$ , $V_{\text{LDO1}}$ connected via $47\text{ k}\Omega$ to GND<br>$T_j = 130\text{ }^{\circ}\text{C}$ | -10 |     | 10  | $\mu\text{A}$ |
| $I_{\text{Leakage, CANL, 105}}$ | Input leakage current CANL | Unpowered device;<br>$V_{\text{CANH}} = 5\text{ V}$ ; $V_{\text{CANL}} = 5\text{ V}$ ; $V_{\text{FBB}} < V_{\text{FBB\_Transmitter(min)}}$ ;<br>$V_{\text{FBB}}$ , $V_{\text{LDO1}}^{(2)}$ connected via $0\text{ }\Omega$ to GND<br>$T_j = -40$ to $105\text{ }^{\circ}\text{C}$                                                                      | -10 |     | 10  | $\mu\text{A}$ |
| $I_{\text{Leakage, CANL, 130}}$ | Input leakage current CANL | Unpowered device;<br>$V_{\text{CANH}} = 5\text{ V}$ ; $V_{\text{CANL}} = 5\text{ V}$ ; $V_{\text{FBB}} < V_{\text{FBB\_Transmitter(min)}}$ ;<br>$V_{\text{FBB}}$ , $V_{\text{LDO1}}^{(2)}$ connected via $0\text{ }\Omega$ to GND<br>$T_j = 130\text{ }^{\circ}\text{C}$                                                                               | -10 |     | 10  | $\mu\text{A}$ |

1. Related to the external supply pin of the CAN-transceiver. If the transceiver supply is generated entirely inside of the device, the parameter is measured with respect to the supply of the device.
2. Related to the external supply pin of the CAN transceiver. If the transceiver supply is generated entirely inside of the device, the parameter is measured with respect to the supply of the device; if the transceiver is supplied by its own supply pin, this pin has to fulfill this specification as well as the supply that is used to generate the transceiver voltage in case it is on the same device.

**Table 49. Biasing control timings**

| Symbol                     | Parameter                | Condition | Min | Typ | Max  | Unit          |
|----------------------------|--------------------------|-----------|-----|-----|------|---------------|
| $t_{\text{filter}}$        | CAN activity filter time |           | 0.5 |     | 1.8  | $\mu\text{s}$ |
| $t_{\text{wake}}^{(1)}$    | Wake-up timeout          |           | 0.8 | 1   | 5    | ms            |
| $t_{\text{Silence}}^{(1)}$ | CAN timeout              |           | 600 | 700 | 1200 | ms            |
| $T_{\text{Bias}}$          | CAN bias reaction time   |           |     |     | 250  | $\mu\text{s}$ |

1. Digital implementation guaranteed by SCAN test.

## 7.16 SPI

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  
 $3\text{ V} \leq V_{\text{IO}} \leq 5.5\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 50. Input: CSN**

| Symbol                | Parameter                               | Condition                       | Min | Typ | Max | Unit       |
|-----------------------|-----------------------------------------|---------------------------------|-----|-----|-----|------------|
| $V_{\text{CSN\_L}}$   | Input voltage low threshold             |                                 | 1.0 | -   | -   | V          |
| $V_{\text{CSN\_H}}$   | Input voltage high threshold            |                                 | -   | -   | 2.3 | V          |
| $V_{\text{CSN\_HYS}}$ | $V_{\text{CSN\_H}} - V_{\text{CSN\_L}}$ |                                 | 0.2 | 0.4 | -   | V          |
| $R_{\text{CSN\_PU}}$  | CSN pull-up resistor                    | $V = 1.0\text{ V}$              | 13  | 29  | 55  | k $\Omega$ |
| $C_{\text{CSN}}$      |                                         | $0\text{ V} < V < 5.3\text{ V}$ | -   | 10  | 15  | pF         |

**Table 51. Inputs: CLK, SDI**

| Symbol                         | Parameter                               | Condition                          | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------------|------------------------------------|-----|-----|-----|------|
| V <sub>CLK_L</sub>             | CLK input low threshold                 |                                    | 1.0 | -   | -   | V    |
| V <sub>SDI_L</sub>             | SDI input low threshold                 |                                    | 1.0 | -   | -   | V    |
| V <sub>CLK_H</sub>             | CLK input high threshold                |                                    | -   | -   | 2.3 | V    |
| V <sub>SDI_H</sub>             | SDI input high threshold                |                                    | -   | -   | 2.3 | V    |
| V <sub>CLK_HYS</sub>           | CLK input hysteresis                    |                                    | 0.2 | -   | -   | V    |
| V <sub>SDI_HYS</sub>           | SDI input hysteresis                    |                                    | 0.2 | -   | -   | V    |
| I <sub>CLK</sub>               | CLK pull-down current at input          | V <sub>CLK</sub> = 1.0 V           | 5   | 20  | 60  | μA   |
| I <sub>SDI</sub>               | SDI pull-down current at input          | V <sub>SDI</sub> = 1.0 V           | 5   | 20  | 60  | μA   |
| C <sub>in</sub> <sup>(1)</sup> | Input capacitance at input CLK, and SDI | 0 V < V <sub>CLK,SDI</sub> < 5.3 V | -   | 10  | 15  | pF   |
| f <sub>CLK</sub>               | SPI input frequency at CLK              |                                    | -   | -   | 6   | MHz  |

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

**Table 52. SDI, CLK and CSN timing**

| Symbol                           | Parameter                                                                   | Condition | Min   | Typ | Max | Unit |
|----------------------------------|-----------------------------------------------------------------------------|-----------|-------|-----|-----|------|
| t <sub>CLK</sub>                 | Clock period                                                                |           | 166   | -   | -   | ns   |
| t <sub>CLK_H</sub>               | Clock high time                                                             |           | 58    | -   | -   | ns   |
| t <sub>CLK_L</sub>               | Clock low time                                                              |           | 58    | -   | -   | ns   |
| t <sub>set_CSN</sub>             | CSN setup time, CSN low before rising edge of CLK in ACTIVE FULL-POWER mode |           | 150   | -   | -   | ns   |
| t <sub>set_CSN_LP</sub>          | CSN setup time, CSN low before rising edge of CLK in ACTIVE LOW-POWER mode  |           | 10000 | -   | -   | ns   |
| t <sub>set_CLK</sub>             | CLK setup time, CLK high before rising edge of CSN                          |           | 150   | -   | -   | ns   |
| t <sub>set_SDI</sub>             | SDI setup time                                                              |           | 25    | -   | -   | ns   |
| t <sub>hold_SDI</sub>            | SDI hold time                                                               |           | 25    | -   | -   | ns   |
| t <sub>r_in</sub> <sup>(1)</sup> | Rise time of input signal SDI, CLK, CSN                                     |           | -     | -   | 25  | ns   |
| t <sub>f_in</sub> <sup>(1)</sup> | Fall time of input signal SDI, CLK, CSN                                     |           | -     | -   | 25  | ns   |

1. Guaranteed by design.

**Table 53. Output: SDO**

| Symbol              | Parameter                | Condition                                                           | Min | Typ | Max | Unit |
|---------------------|--------------------------|---------------------------------------------------------------------|-----|-----|-----|------|
| V <sub>SDO_L</sub>  | Output low level         | V <sub>IO</sub> = 5.0 V<br>I <sub>SDO</sub> = +4 mA                 | -   | -   | 0.5 | V    |
| V <sub>SDO_H</sub>  | Output high level        | V <sub>IO</sub> = 5.0 V<br>I <sub>SDO</sub> = -4 mA                 | 4.5 | -   | -   | V    |
| I <sub>SDO_LK</sub> | Tristate leakage current | V <sub>IO</sub> = 5.0 V<br>0 V < V <sub>SDO</sub> < V <sub>IO</sub> | -10 | -   | 10  | μA   |

**Table 54. SDO timing (see Figure 69 SPI input timing)**

| Symbol                       | Parameter                                          | Condition                                                                               | Min | Typ | Max | Unit |
|------------------------------|----------------------------------------------------|-----------------------------------------------------------------------------------------|-----|-----|-----|------|
| $t_{r\_SDO}^{(1)}$           | SDO rise time                                      | $C_L = 50\text{ pF}$<br>$I_{load} = -4\text{ mA}$<br>20% to 80%                         |     | -   | 25  | ns   |
| $t_{f\_SDO}^{(1)}$           | SDO fall time                                      | $C_L = 50\text{ pF}$<br>$I_{load} = 4\text{ mA}$<br>20% to 80%                          |     | -   | 25  | ns   |
| $t_{en\_SDO\_tri\_L}^{(1)}$  | SDO enable time from high impedance to low level   | $C_L = 50\text{ pF}$<br>$I_{load} = 4\text{ mA}$<br>Pull-up load to $V_{IO}$            |     | 50  | 100 | ns   |
| $t_{dis\_SDO\_tri\_L}^{(1)}$ | SDO disable time from low level to high impedance  | $C_L = 50\text{ pF}$<br>$I_{load} = 4\text{ mA}$<br>Pull-up load to $V_{IO}$            |     | 50  | 100 | ns   |
| $t_{en\_SDO\_tri\_H}^{(1)}$  | SDO enable time from high impedance to high level  | $C_L = 50\text{ pF}$<br>$I_{load} = -4\text{ mA}$<br>Pull-down load to GND              |     | 50  | 100 | ns   |
| $t_{dis\_SDO\_H\_tri}^{(1)}$ | SDO disable time from high level to high impedance | $C_L = 50\text{ pF}$<br>$I_{load} = -4\text{ mA}$                                       |     | 50  | 100 | ns   |
| $t_{d\_SDO}^{(1)}$           | SDO delay time                                     | $V_{SDO} < 0.2 \cdot V_{IO}$<br>or $V_{SDO} > 0.8 \cdot V_{IO}$<br>$C_L = 50\text{ pF}$ |     | 30  | 60  | ns   |

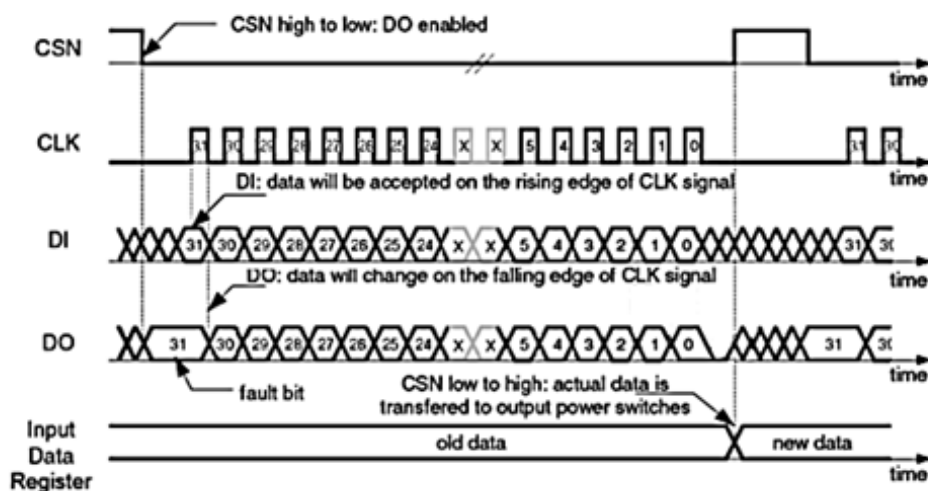
1. Guaranteed by design.

**Table 55. CSN timing (see Figure 71 SPI CSN - Output Timing)**

| Symbol                       | Parameter                              | Condition                                 | Min | Typ | Max | Unit          |
|------------------------------|----------------------------------------|-------------------------------------------|-----|-----|-----|---------------|
| $t_{CSN\_HI,min\_act}^{(1)}$ | Minimum CSN high time, ACTIVE mode     | Transfer of SPI-command to input register | 0.5 | -   | -   | $\mu\text{s}$ |
| $t_{CSN\_HI,min\_lp}^{(1)}$  | Minimum CSN high time, LOW-POWER modes | Transfer of SPI-command to input register | 5   | -   | -   | $\mu\text{s}$ |
| $t_{CSNfail}^{(1)}$          | CSN low timeout                        |                                           | 20  | 35  | 50  | ms            |

1. Covered by scan.

Figure 67. SPI - Transfer timing diagram



The SPI can be driven by a microcontroller with its SPI peripheral running in the following modes:

- CPOL = 0
- CPHA = 0

For this mode input data is sampled by the low-to-high transition of the clock CLK, and output data is changed from the high-to-low transition of CLK.

Figure 68. SPI - Input timing

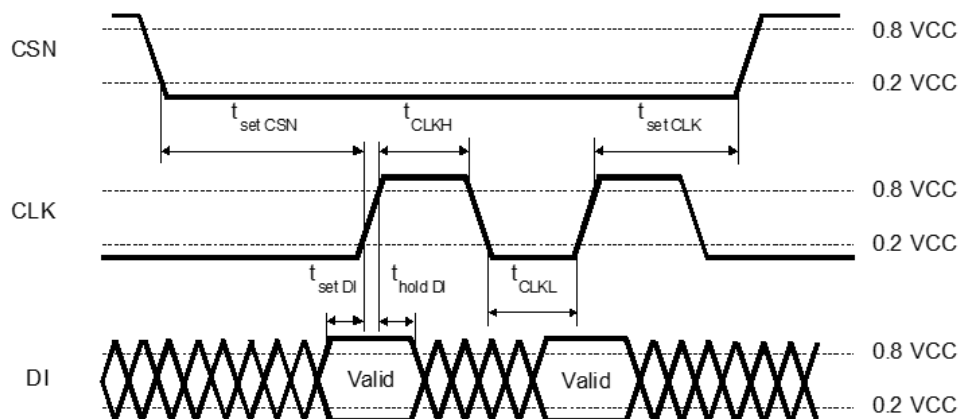
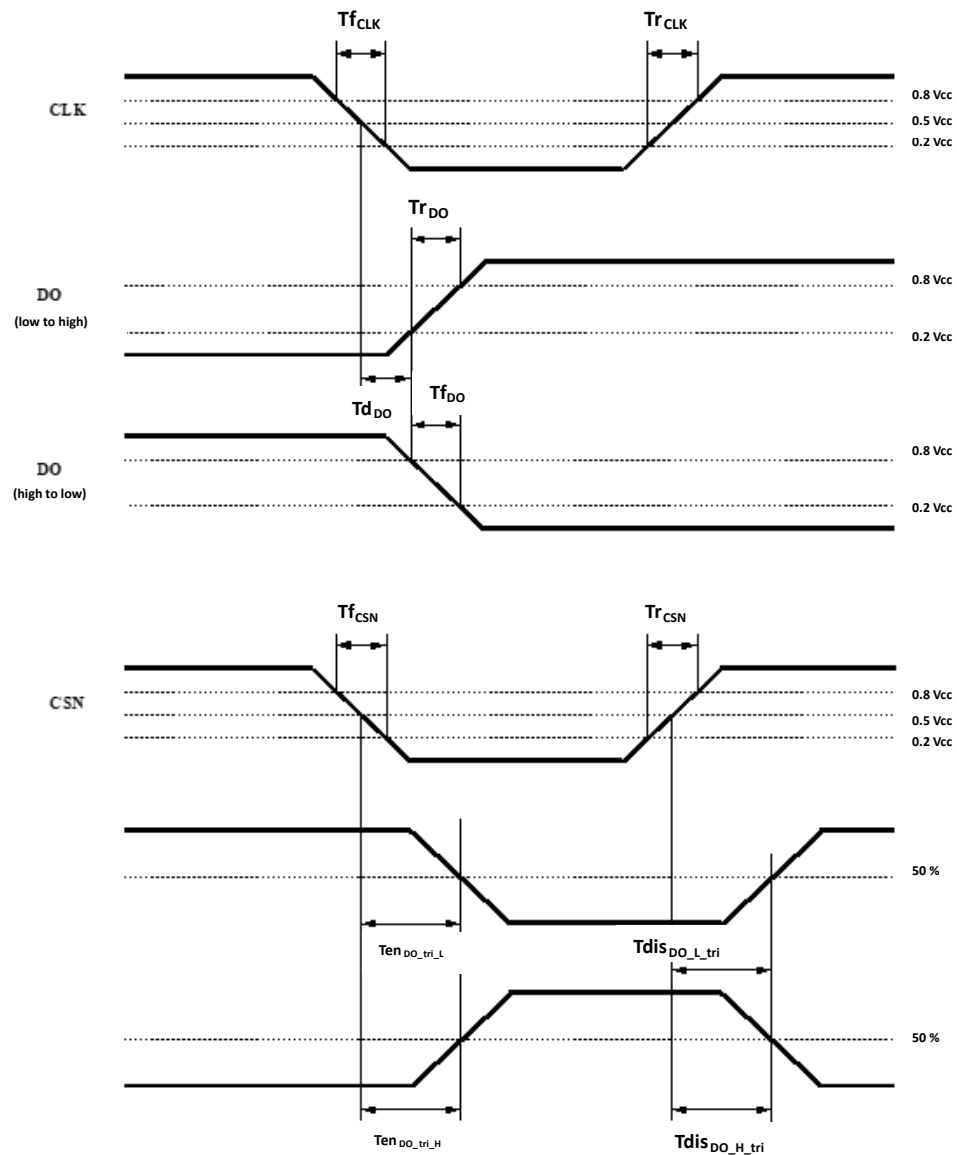
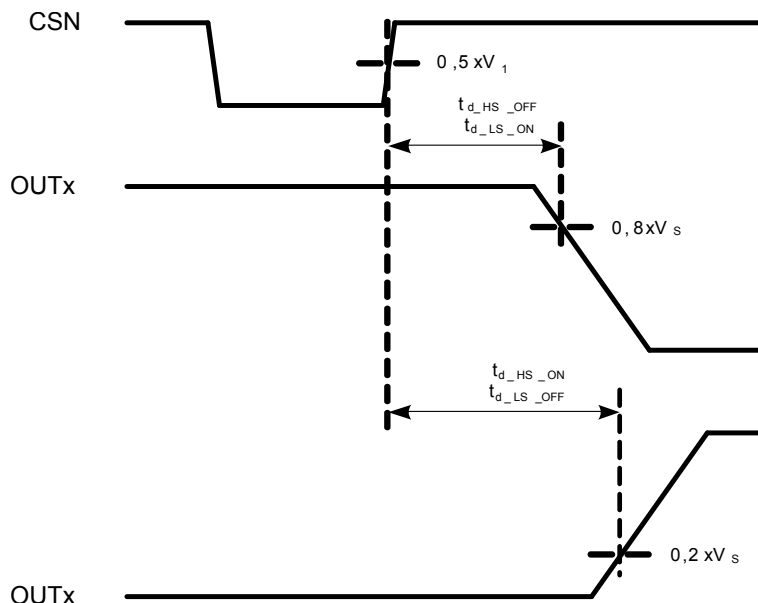
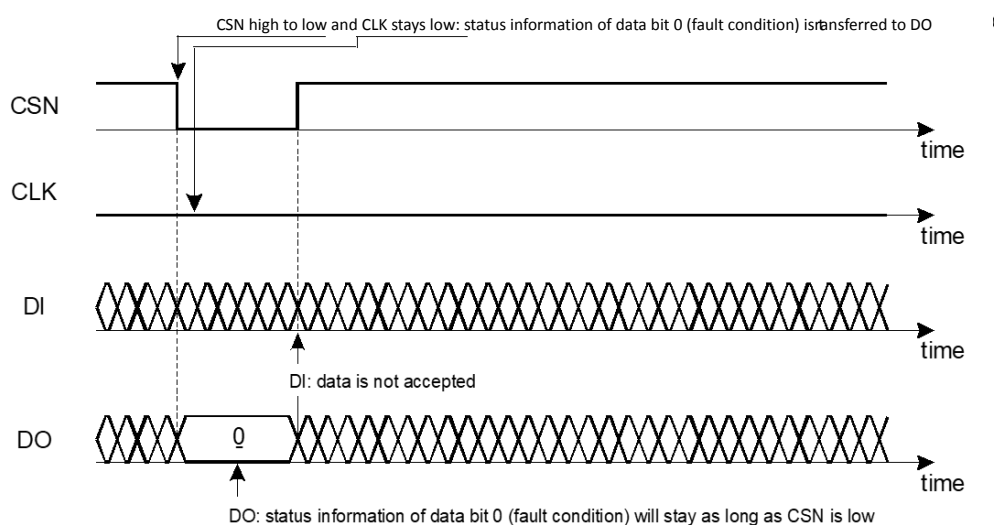


**Figure 69. SPI - Output timing**



Prerelease product(s)

**Figure 70. SPI CSN - Output timing**

**Figure 71. SPI - CSN low-to-high transition and global status bit access**


## 7.17 SWDBG input

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  
 $3\text{ V} \leq V_{\text{FBB}} \leq 20\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ .

**Table 56. SWDBG input**

| Symbol                       | Parameter                                         | Condition                                    | Min | Typ | Max  | Unit       |
|------------------------------|---------------------------------------------------|----------------------------------------------|-----|-----|------|------------|
| $V_{\text{SWDBG\_L}}$        | Input voltage low threshold                       |                                              | 1.0 | -   | -    | V          |
| $V_{\text{SWDBG\_H}}$        | Input voltage high threshold for watchdog disable |                                              | -   | -   | 2.3  | V          |
| $V_{\text{SWDBG\_HYS}}$      | Input hysteresis                                  |                                              | 0.2 | -   | -    | V          |
| $t_{\text{SWDBG\_TO}}^{(1)}$ | Software-debug timeout                            |                                              | 8.3 | 10  | 12.6 | s          |
| $R_{\text{SWDBG\_PD}}$       | Pull-down resistor                                | $V_{\text{SWDBG}} = 6\text{ to }20\text{ V}$ | 13  | 29  | 55   | k $\Omega$ |
| $V_{\text{NVM\_EMU\_L}}$     | Input low threshold for NVM emulation exit        |                                              | 6.1 | -   | -    | V          |

| Symbol                            | Parameter                                                    | Condition | Min | Typ | Max | Unit |
|-----------------------------------|--------------------------------------------------------------|-----------|-----|-----|-----|------|
| V <sub>NVM_EMU_H</sub>            | Input voltage high threshold for transition to NVM emulation |           | -   | -   | 9.4 | V    |
| V <sub>NVM_EMU_HYS</sub>          | Input hysteresis for NVM emulation                           |           | 0.3 | -   | -   | V    |
| C <sub>SWDBG</sub> <sup>(2)</sup> | SWDBG input capacitance                                      |           | -   | -   | 15  | pF   |

1. Digital implementation guaranteed by SCAN test.

2. Guaranteed by design.

## 7.18 ADC characteristics

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6.0 V ≤ V<sub>FBB</sub> ≤ 29 V, T<sub>j</sub> = -40 °C to 150 °C.

**Table 57. ADC characteristics**

| Symbol                | Parameter                                  | Condition                                              | Min   | Typ   | Max   | Unit |
|-----------------------|--------------------------------------------|--------------------------------------------------------|-------|-------|-------|------|
| t <sub>con</sub>      | Conversion time for 1 channel              | Tested by scan                                         | 2.49  | 3     | 3.51  | μs   |
| t <sub>con_2ADC</sub> | Conversion time between 2 ADC measurements | Tested by scan                                         | 32.3  | 39    | 45.6  | μs   |
| f <sub>ADC</sub>      | Clock frequency                            | Tested by scan                                         | 6.72  | 8.4   | 10.08 | MHz  |
| Acc <sup>(1)</sup>    | Accuracy                                   | Voltage divider+reference                              | -2    | -     | 2     | %    |
| Acc22                 | Accuracy                                   | Overall accuracy for WU input: V <sub>WU</sub> = 22 V  | -3    | -     | 3     | %    |
| Acc18                 | Accuracy                                   | Overall accuracy for WU input: V <sub>WU</sub> = 18 V  | -3.5  | -     | 3.5   | %    |
| Acc6                  | Accuracy                                   | Overall accuracy for WU input: V <sub>WU</sub> = 6 V   | -8    | -     | 8     | %    |
| Acc4                  | Accuracy                                   | Overall accuracy for WU input: V <sub>WU</sub> = 4.5 V | -10   | -     | 10    | %    |
| IE <sub>I</sub>       | Integral linearity error                   |                                                        | -     | 4     | 6     | LSB  |
| IE <sub>D</sub>       | Differential linearity error               |                                                        | -     | 2     | 4     | LSB  |
| V <sub>AINVS</sub>    | Conversion voltage range (WU and IGN)      |                                                        | 1     | -     | 40    | V    |
| LSB <sub>T</sub>      | Thermal LSB                                |                                                        | 0.471 | 0.496 | 0.521 | °C   |
| LSB <sub>V</sub>      | Voltage LSB (WU, IGN, VS and FBB)          |                                                        | 38    | 40    | 42    | mV   |

1. Guaranteed by design.

## 7.19 IRQ interrupt

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

3.0 V ≤ V<sub>IO</sub> ≤ 5.5 V, T<sub>j</sub> = -40 °C to 150 °C.

**Table 58. Interrupt output**

| Symbol                                | Parameter                              | Condition                                           | Min | Typ | Max | Unit |
|---------------------------------------|----------------------------------------|-----------------------------------------------------|-----|-----|-----|------|
| V <sub>IRQ_L</sub>                    | Output low level                       | I <sub>IRQ</sub> = +4 mA                            | -   | -   | 0.5 | V    |
| I <sub>IRQ_LK</sub>                   | Leakage current                        | V <sub>IRQ</sub> = 20 V<br>V <sub>IO</sub> = 3.3 V  | -   | -   | 100 | μA   |
| I <sub>IRQ_LK_5V</sub>                | Leakage current when IRQ is disabled   | V <sub>IRQ</sub> = 5.0 V<br>V <sub>IO</sub> = 5.0 V | -   | -   | 1   | μA   |
| R <sub>IRQ_PU</sub>                   | IRQ internal pull-up resistor for echo | V <sub>IRQ</sub> = 1 V                              | 13  | 29  | 55  | kΩ   |
| t <sub>IRQ_react</sub> <sup>(1)</sup> | Interrupt reaction time                |                                                     | -   | -   | 40  | μs   |

| Symbol                       | Parameter                  | Condition | Min | Typ | Max | Unit          |
|------------------------------|----------------------------|-----------|-----|-----|-----|---------------|
| $t_{\text{IRQ\_ECHO\_FILT}}$ | IRQ echo error filter time |           | 91  | 100 | 150 | $\mu\text{s}$ |

1. Guaranteed by SCAN.

## 7.20

### FIN1 input

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  
 $3.0\text{ V} \leq V_{\text{IO}} \leq 5.5\text{ V}$ ,  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 59. FIN1 input**

| Symbol                  | Parameter                                | Condition                                                                                                    | Min | Typ | Max | Unit       |
|-------------------------|------------------------------------------|--------------------------------------------------------------------------------------------------------------|-----|-----|-----|------------|
| $V_{\text{FIN1\_L}}$    | Input voltage low threshold              |                                                                                                              | 1.0 | -   | -   | V          |
| $V_{\text{FIN1\_H}}$    | Input voltage high threshold             |                                                                                                              | -   | -   | 2.3 | V          |
| $V_{\text{FIN1\_HYS}}$  | Input voltage hysteresis                 |                                                                                                              | 0.2 | -   | -   | V          |
| $R_{\text{FIN1\_PU}}$   | FIN1 pull-up resistor to $V_{\text{IO}}$ | $V_{\text{IO}} = 5.0\text{ V}$<br>$V_{\text{FIN1}} = 1.0\text{ V}$<br>Defined by CR<br>FCCU_STATIC_ERROR bit | 13  | 29  | 55  | k $\Omega$ |
| $R_{\text{FIN1\_PD}}$   | FIN1 pull-down resistor to GND           | $V_{\text{IO}} = 5.0\text{ V}$<br>$V_{\text{FIN1}} = 1.0\text{ V}$<br>Defined by CR<br>FCCU_STATIC_ERROR bit | 13  | 29  | 55  | k $\Omega$ |
| $C_{\text{FIN1}}^{(1)}$ | FIN1 input capacitance                   |                                                                                                              | -   | -   | 15  | pF         |

1. Guaranteed by design.

## 7.21

### Timer

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  
 $6.0\text{ V} \leq V_{\text{FBB}} \leq 29\text{ V}$ ,  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ , unless otherwise specified.  
All timer timings are covered by SCAN.

**Table 60. Timer values**

| Symbol           | Parameter     | Condition                          | Min  | Typ | Max  | Unit |
|------------------|---------------|------------------------------------|------|-----|------|------|
| $t_{\text{ON1}}$ | Timer on-time | $T1\_ENA = 000$<br>(default value) | 0.08 | 0.1 | 0.14 | ms   |
| $t_{\text{ON2}}$ | Timer on-time | $T1\_ENA = 001$                    | 0.25 | 0.3 | 0.39 | ms   |
| $t_{\text{ON3}}$ | Timer on-time | $T1\_ENA = 010$                    | 0.83 | 1   | 1.27 | ms   |
| $t_{\text{ON4}}$ | Timer on-time | $T1\_ENA = 011$                    | 8.3  | 10  | 12.5 | ms   |
| $t_{\text{ON5}}$ | Timer on-time | $T1\_ENA = 1xx$                    | 16.6 | 20  | 25   | ms   |
| T1               | Timer period  | $T1\_PER = 000$<br>(default value) | 8.3  | 10  | 12.5 | ms   |
| T2               | Timer period  | $T1\_PER = 001$                    | 16.6 | 20  | 25   | ms   |
| T3               | Timer period  | $T1\_PER = 010$                    | 41.6 | 50  | 62.5 | ms   |
| T4               | Timer period  | $T1\_PER = 011$                    | 83   | 100 | 125  | ms   |
| T5               | Timer period  | $T1\_PER = 100$                    | 166  | 200 | 250  | ms   |

| Symbol | Parameter    | Condition    | Min  | Typ  | Max  | Unit |
|--------|--------------|--------------|------|------|------|------|
| T6     | Timer period | T1_PER = 101 | 416  | 500  | 625  | ms   |
| T7     | Timer period | T1_PER = 110 | 830  | 1000 | 1250 | ms   |
| T8     | Timer period | T1_PER = 110 | 1660 | 2000 | 2500 | ms   |

## 7.22 Reset output (NRST)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  
 $3.0\text{ V} \leq V_{IO} \leq 5.5\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 61. Reset output**

| Symbol                      | Parameter                               | Condition                                             | Min | Typ | Max | Unit          |
|-----------------------------|-----------------------------------------|-------------------------------------------------------|-----|-----|-----|---------------|
| $V_{NRST\_L}$               | Output low level                        | $I_{NRST} = +4\text{ mA}$                             | -   | -   | 0.5 | V             |
| $I_{NRST\_LK}$              | Leakage current                         | $V_{NRST} = 20.0\text{ V}$<br>$V_{IO} = 3.3\text{ V}$ | -   | -   | 100 | $\mu\text{A}$ |
| $I_{NRST\_LK\_5V}$          | Leakage current when NRST is disabled   | $V_{NRST} = 5.0\text{ V}$<br>$V_{IO} = 5.0\text{ V}$  | -   | -   | 1   | $\mu\text{A}$ |
| $R_{NRST\_PU}$              | NRST internal pull-up resistor for echo | $V_{NRST} = 1.0\text{ V}$                             | 13  | 29  | 55  | k $\Omega$    |
| $t_{NRST\_WDR}^{(1)}$       | Low pulse duration time                 | In case of WD error                                   | 3.2 | -   | -   | ms            |
| $t_{NRST\_FCCU}^{(1)}$      | Low pulse duration time                 | In case of FCCU error                                 | 4.8 | -   | -   | ms            |
| $t_{NRST\_ECHO\_FLT}^{(1)}$ | NRST echo error filter time             |                                                       | 91  | 100 | 150 | $\mu\text{s}$ |

1. Guaranteed by SCAN.

## 7.23 VREG voltage regulator

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  
 $6\text{ V} \leq V_{FBB} \leq 29\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 62. VREG**

| Symbol               | Parameter                                  | Condition                                          | Min  | Typ | Max | Unit          |
|----------------------|--------------------------------------------|----------------------------------------------------|------|-----|-----|---------------|
| $V_{VREG}$           | Output voltage                             | In active-Full power<br>$I_{load} = 120\text{ mA}$ | 3.2  | 3.4 | 3.6 | V             |
| $V_{VREG\_LP}$       | Output voltage                             | In active-Low power<br>$I_{load} = 15\text{ mA}$   | 3.2  | 3.4 | 3.6 | V             |
| $V_{VREG\_OV}$       | Overvoltage threshold for $V_{REG}$        |                                                    | 3.45 | 3.6 | 3.8 | V             |
| $V_{VREG\_OV\_LP}$   | Overvoltage threshold for $V_{REG}$ in LP  |                                                    | 3.45 | 3.6 | 3.8 | V             |
| $t_{VREG\_OV}$       | $V_{REG}$ overvoltage filter time          |                                                    | 12   | 15  | 22  | $\mu\text{s}$ |
| $V_{VREG\_UV}$       | Undervoltage threshold for $V_{REG}$       |                                                    | 2.7  | 2.9 | 3.1 | V             |
| $V_{VREG\_UV\_LP}$   | Undervoltage threshold for $V_{REG}$ in LP |                                                    | 2.7  | 2.9 | 3.1 | V             |
| $t_{VREG\_UV}^{(1)}$ | $V_{REG}$ undervoltage filter time         |                                                    | 12   | 15  | 22  | $\mu\text{s}$ |

| Symbol                 | Parameter                                        | Condition                               | Min | Typ | Max  | Unit    |
|------------------------|--------------------------------------------------|-----------------------------------------|-----|-----|------|---------|
| $t_{VREG\_stup}^{(1)}$ | $V_{REG}$ max start-up delay time for power-good |                                         | 1.6 | 2   | 2.51 | ms      |
| $I_{VREG\_CCmax}$      | Short-circuit output current (to GND)            | Current limitation in active-full power | 125 | 260 | 380  | mA      |
| $C_{VREG}^{(2)}$       | Load capacitor                                   | Ceramic                                 | 3   | 4.7 | 10   | $\mu F$ |

1. Digital implementation guaranteed by SCAN test.
2. Nominal capacitor value required for stability of the regulator. Tested with 4.7  $\mu F$  ceramic ( $\pm 20\%$ ). Capacitor must be located close to the regulator output pin.

## 7.24 BIST timing

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  $6 V \leq V_{FBB} \leq 29 V$ ,  $T_j = -40^\circ C$  to  $150^\circ C$ , unless otherwise specified.

**Table 63. BIST timing**

| Symbol      | Parameter                     | Condition       | Min  | Typ  | Max  | Unit    |
|-------------|-------------------------------|-----------------|------|------|------|---------|
| $T_{LBIST}$ | Logical BIST execution timing | Covered by SCAN | 12.1 | 14.6 | 18.3 | ms      |
| $T_{ABIST}$ | Analog BIST execution timing  | Covered by SCAN | 83   | 100  | 188  | $\mu s$ |

## 7.25 Long duration timer

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6 V < V_{FBB} < 29 V$ ;  $T_j = -40^\circ C$  to  $150^\circ C$ , unless otherwise specified.

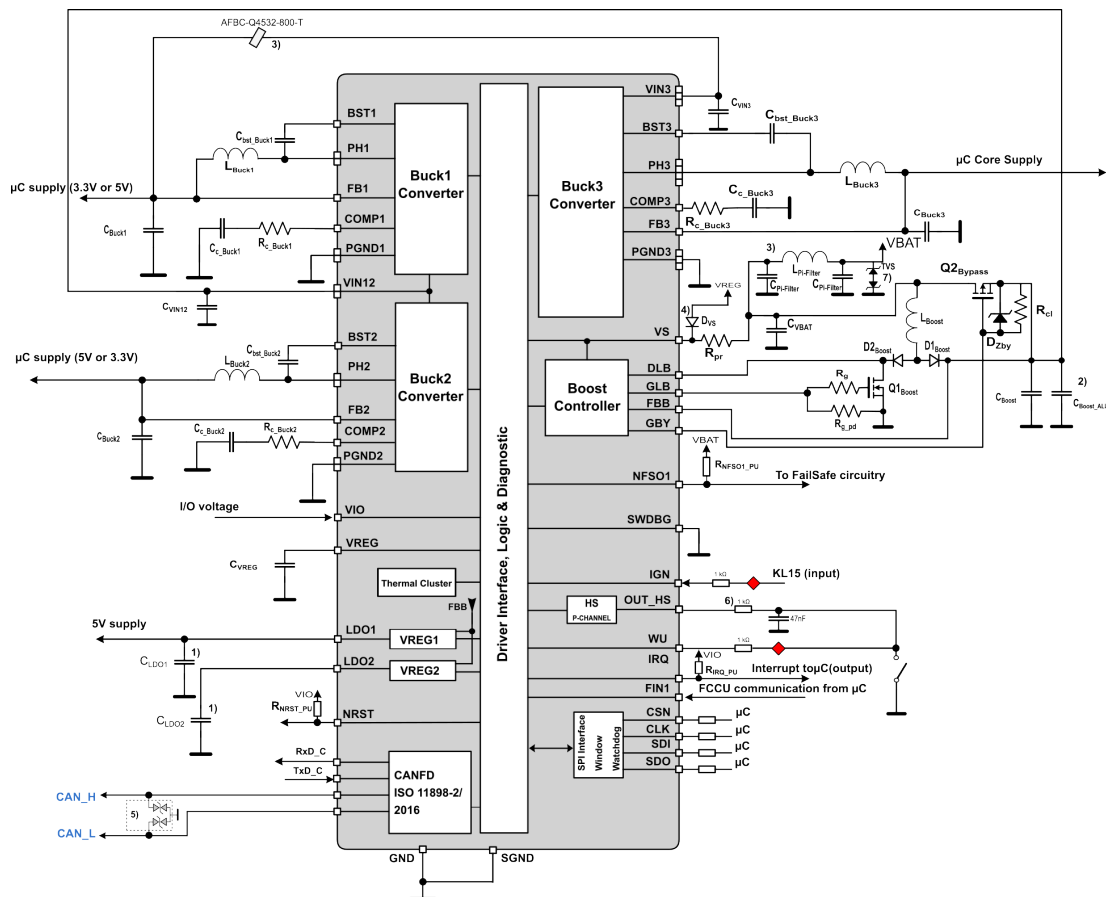
**Table 64. Timer values**

| Symbol            | Parameter                           | Condition | Min  | Typ | Max  | Unit |
|-------------------|-------------------------------------|-----------|------|-----|------|------|
| $VLD_{RES}^{(1)}$ | Very long duration timer resolution |           | 0.85 | 1   | 1.15 | s    |
| $LDT\_CNT^{(1)}$  | Long duration timer - counter       |           | 153  | 180 | 213  | days |

1. Covered by SCAN.

## 8 Application circuit

**Figure 72. Typical application circuit for SPSB100GS**



- 1) For EMC optimization purposes, capacitance could be redimensioned (2.2 µF recommended)  
 2) Optional to improve ripple on boost voltage  
 3) Only needed for EMC performances  
 4) Only needed to pass IAV-G brief interruptions test  
 5) ST ESDCAN04-2BWY is needed only for SAE J2962-2 compliance  
 6) Minimum serial resistor of 50 ohms is required on OUT\_HS to sustain E-17 test  
 7) TVS is needed to sustain ISO pulses

ESD Protection for ECU pins



### 8.1 External recommended components

**Table 65. External components (referred to pictures in the related sections)**

| Component         | Block/Usage              | Min | Typ | Max | Unit | Note                                                                                                            |
|-------------------|--------------------------|-----|-----|-----|------|-----------------------------------------------------------------------------------------------------------------|
| $C_{VBAT}^{(1)}$  | Capacitance at $V_{bat}$ | 40  | 50  | -   | µF   | ESR: < 15 mΩ<br>Capacitance change or temperature coefficient: <  22% <br>Rated voltage: > 40 VDC<br>X7R<br>SMD |
| $C_{Boost}^{(1)}$ | Capacitance at FBB       | 70  | 100 | 130 | µF   | ESR: < 15 mΩ<br>Capacitance change or temperature coefficient: <  22% <br>Rated voltage: > 40 VDC               |

| Component                                                                                                         | Block/Usage                                                           | Min  | Typ | Max  | Unit | Note                                                                                                                                                                                             |
|-------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------|------|-----|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                   |                                                                       |      |     |      |      | X7R<br>SMD                                                                                                                                                                                       |
| C <sub>Boost_ALU</sub> <sup>(1)</sup><br><sub>(2)</sub>                                                           | Option ALU capacitance at FBB                                         | 150  | 220 | 330  | μF   | ESR: < 30 mΩ<br>Capacitance change or temperature coefficient: <  32% <br>Rated voltage: > 40 VDC<br>AL ELEC CAP<br>SMD                                                                          |
| Q1 <sub>Boost</sub>                                                                                               | Low-side boost converter external MOSFET                              | -    | -   | -    | -    | R <sub>DS(ON)</sub> : < 10 mΩ<br>V <sub>(BR)DSS</sub> : > 40 V<br>V <sub>GS</sub> : ±20 V<br>I <sub>D</sub> (continuous): > 20 A<br>I <sub>D</sub> (pulse): > 40 A<br>V <sub>GS_TH</sub> : < 3 V |
| D1 <sub>Boost</sub><br>D2 <sub>Boost</sub>                                                                        | External Schottky diodes                                              | -    | -   | -    | -    | Schottky diodes<br>I <sub>F(AV)</sub> : > 25 A<br>V <sub>RRM</sub> : > 40 V<br>V <sub>F(max)</sub> : < 0.7 V                                                                                     |
| L <sub>Boost</sub>                                                                                                | BOOST inductance                                                      | 0.8  | 1   | 1.2  | μH   | DCR: < 10 mΩ<br>I <sub>sat</sub> : > 20 A<br>Derating < 40%                                                                                                                                      |
| R <sub>pr</sub>                                                                                                   | Resistor for VS pin protection                                        | 0.95 | 1   | 1.05 | kΩ   | -                                                                                                                                                                                                |
| R <sub>g</sub>                                                                                                    | Serial gate resistor of Q1 <sub>Boost</sub>                           | 2.09 | 2.2 | 2.31 | Ω    | -                                                                                                                                                                                                |
| R <sub>g_pd</sub>                                                                                                 | Pull-down resistor of Q1 <sub>Boost</sub> gate                        | 95   | 100 | 105  | kΩ   | -                                                                                                                                                                                                |
| Q2 <sub>Bypass</sub>                                                                                              | Bypass external MOSFET                                                | -    | -   | -    | -    | R <sub>DS(ON)</sub> : < 10 mΩ<br>V <sub>(BR)DSS</sub> : > 40 V<br>V <sub>GS</sub> : ±20 V<br>I <sub>D</sub> (continuous): > 20 A<br>I <sub>D</sub> (pulse): > 40 A<br>V <sub>GS_TH</sub> : < 3 V |
| D <sub>Zby</sub>                                                                                                  | Zener diode to clamp V <sub>GS</sub> of Q2 bypass                     | -    | -   | -    | -    | Voltage clamp = 18 V                                                                                                                                                                             |
| R <sub>cl</sub>                                                                                                   | Discharge resistor to short V <sub>GS</sub> of Q2 bypass in OFF STATE | 20.9 | 22  | 23.1 | kΩ   | -                                                                                                                                                                                                |
| C <sub>Buck1_24</sub> <sup>(1)</sup><br>C <sub>Buck2_24</sub> <sup>(1)</sup><br>C <sub>Buck3</sub> <sup>(1)</sup> | Output capacitor at 2.4 MHz<br>T = 27 °C                              | 17   | 22  | 27   | μF   | ESR: < 15 mΩ<br>Rated voltage: > 10 VDC<br>X7R<br>SMD                                                                                                                                            |
| L <sub>Buck1_24</sub><br>L <sub>Buck2_24</sub>                                                                    | Output inductor at 2.4 MHz                                            | 2.2  | 3.3 | 4    | μH   | R <sub>dc</sub> : < 25 mΩ<br>I <sub>sat</sub> > 6.2 A<br>SRF > 15 MHz<br>SMD                                                                                                                     |

| Component                                                                    | Block/Usage                                   | Min   | Typ | Max   | Unit | Note                                                                                                    |
|------------------------------------------------------------------------------|-----------------------------------------------|-------|-----|-------|------|---------------------------------------------------------------------------------------------------------|
| C <sub>bst_Buck1</sub><br>C <sub>bst_Buck2</sub>                             | Bootstrap capacitor                           | 37.6  | 47  | 56.4  | nF   | -                                                                                                       |
| C <sub>bst_Buck3</sub>                                                       | Bootstrap capacitor                           | 80    | 100 | 120   | nF   | -                                                                                                       |
| L <sub>Buck3</sub>                                                           | Output inductor<br>I <sub>out</sub> = 4.3 A   | 2.2   | 3.3 | 4     | μH   | R <sub>dc</sub> : < 15 mΩ<br>I <sub>sat</sub> > 10 A<br>SRF > 15 MHz<br>SMD<br>Choice: XAL6030-332ME    |
| C <sub>c_Buck1_24</sub><br>C <sub>c_Buck2_24</sub>                           | Compensation network capacitor at F = 2.4 MHz | 1.2   | 1.5 | 1.8   | nF   | -                                                                                                       |
| C <sub>c_Buck3</sub>                                                         | Compensation network capacitor                | 3.76  | 4.7 | 5.64  | nF   | -                                                                                                       |
| R <sub>c_Buck1_24</sub><br>R <sub>c_Buck2_24</sub>                           | Compensation network resistor at F = 2.4 MHz  | 14.25 | 15  | 15.75 | kΩ   | -                                                                                                       |
| R <sub>c_Buck3</sub>                                                         | Compensation network resistor                 | 0.95  | 1   | 1.05  | kΩ   | -                                                                                                       |
| C <sub>Buck1_04</sub> <sup>(1)</sup><br>C <sub>Buck2_04</sub> <sup>(1)</sup> | Output capacitor at 400 kHz<br>T = 27 °C      | 33    | 47  | 56    | μF   | ESR: < 15 mΩ<br>Rated voltage: > 10 VDC<br>X7R                                                          |
| L <sub>Buck1_04</sub><br>L <sub>Buck2_04</sub>                               | Output inductor at 400 kHz                    | 11    | 15  | 18    | μH   | R <sub>dc</sub> : < 40 mΩ<br>I <sub>sat</sub> > 6.2 A<br>SRF > 4 MHz<br>SMD<br>Choice: SPM6545VT-150M-D |
| C <sub>c_Buck1_04</sub><br>C <sub>c_Buck2_04</sub>                           | Compensation network capacitor at F = 400 kHz | 8     | 10  | 12    | nF   | -                                                                                                       |
| R <sub>c_Buck1_04</sub><br>R <sub>c_Buck2_04</sub>                           | Compensation network resistor at F = 400 kHz  | 4.84  | 5.1 | 5.35  | kΩ   | -                                                                                                       |
| C <sub>VREG</sub> <sup>(1)</sup>                                             | VREG output capacitor                         | 3     | 4.7 | 10    | μF   | max ESR < 0.1 Ω<br>Rated voltage > 5 V<br>X7R                                                           |
| C <sub>LDO1</sub>                                                            | LDO1 output capacitor                         | 1.0   | 2.2 | 10    | μF   | -                                                                                                       |
| C <sub>LDO2</sub> <sup>(1)</sup>                                             | LDO2 output capacitor                         | 1.0   | 2.2 | 10    | μF   | -                                                                                                       |
| R <sub>NFSO1_PU</sub>                                                        | Pull-up resistor to V <sub>bat</sub>          | 28.5  | 30  | 31.5  | kΩ   | -                                                                                                       |
| R <sub>IRQ_PU</sub>                                                          | Pull-up resistor to V <sub>IO</sub>           | 28.5  | 30  | 31.5  | kΩ   | -                                                                                                       |
| R <sub>NRST_PU</sub>                                                         | Pull-up resistor to V <sub>IO</sub>           | 28.5  | 30  | 31.5  | kΩ   | -                                                                                                       |
| C <sub>VIN12</sub> <sup>(1)</sup>                                            | Buck1, 2 input capacitors                     | 38    | 47  | 56    | μF   | ESR < 15 mΩ<br>Rated voltage: > 40 VDC<br>X7R                                                           |
| C <sub>VIN3</sub> <sup>(1)</sup>                                             | Buck3 input capacitor                         | 38    | 47  | 56    | μF   | ESR < 15 mΩ<br>Rated voltage: > 10 VDC<br>X7R                                                           |

| Component              | Block/Usage           | Min | Typ     | Max | Unit | Note                                                                                                      |
|------------------------|-----------------------|-----|---------|-----|------|-----------------------------------------------------------------------------------------------------------|
| D <sub>VS</sub>        | VS pin Schottky diode |     |         |     |      | STPS140ZY                                                                                                 |
| C <sub>Pi-Filter</sub> | Pi-Filter capacitor   |     | 4 x 4.7 |     | μF   | 4 x 4.7 μF capacitors in parallel are recommended to reduce ESR. 50 V voltage rating with 10% tolerance   |
| L <sub>Pi-Filter</sub> | Pi-Filter inductor    |     | 220     |     | nH   | R <sub>dc</sub> < 5 mΩ<br>I <sub>sat</sub> > 20 A<br>SRF > 300 MHz<br>Choice: 7447798022 Wurth Elektronik |

1. Capacitance to be dimensioned, for example, according to voltage drop out requirements. In order to reduce the ESR it is recommended to use more capacitors in parallel.
2. Minimum capacitor value needed to cover VW8000 E-07b test.

## 8.2 External components calculation

### 8.2.1 Buck1 and Buck2 inductor

The value of the output inductor is usually calculated to satisfy the peak-to-peak ripple current requirement. For the best compromise of cost, size and performance, it is suggested to keep the inductor current ripple between 20% and 40% of maximum load current.

For example, if:

$$\Delta I_L = I_{\text{Ripple}} = 0.3 I_{OUT(MAX)} \quad (1)$$

Where  $I_{OUT(MAX)}$  is the maximum output current, then the inductor value can be estimated by the following equation:

$$L > \frac{1}{f_{SW} \times \Delta I_L} \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (2)$$

where  $f_{SW}$  is the switching frequency and  $V_{IN(max)}$  is the maximum input voltage.

The peak current flowing in the inductor is:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \quad (3)$$

If the inductor value decreases, the peak current increases. The peak current has to be lower than the current limit of the device. The inductor should have a saturation current higher than the device current limit.

**Note:** In order to meet slope compensation, L needs to meet the following equation:

$$L > \frac{1}{2} \times \frac{V_{OUT}}{I_{\text{slope}}} \quad (4)$$

With  $I_{\text{slope}} = 650 \text{ mA} \times f_{SW}$ .

### 8.2.2 Buck3 inductor

The value of the output inductor is usually calculated to satisfy the peak-to-peak ripple current requirement. For the best compromise of cost, size and performance, it is suggested to keep the inductor current ripple between 20% and 40% of maximum load current.

For example, if:

$$\Delta I_L = I_{\text{Ripple}} = 0.3 I_{OUT(MAX)} \quad (5)$$

where  $I_{OUT(MAX)}$  is the maximum output current, then the inductor value can be estimated by the following equation:

$$L > \frac{1}{f_{SW} \times \Delta I_L} \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (6)$$

where  $f_{SW}$  is the switching frequency and  $V_{IN(max)}$  is the maximum input voltage.

The peak current flowing in the inductor is:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \quad (7)$$

If the inductor value decreases, the peak current increases. The peak current has to be lower than the current limit of the device. The inductor should have a saturation current higher than the device current limit.

**Note:** *In order to meet slope compensation, L needs to meet the following equation:*

$$L > \frac{1}{2} \times \frac{V_{OUT}}{I_{slope}} \quad (8)$$

With  $I_{slope} = 325 \text{ mA} \times f_{SW}$ .

## 9 SPI registers

### 9.1 Global Status Byte GSB

**Table 66. Global Status Byte GSB**

| Global Status Byte GSB     |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                        |                        |              |                |           |
|----------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------------------------|--------------|----------------|-----------|
| Bit 31                     | Bit 30             | Bit 29                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Bit 28                 | Bit 27                 | Bit 26       | Bit 25         | Bit 24    |
| 1 (R)                      | 0 (R)              | 0 (R)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 0 (R)                  | 0 (R)                  | 0 (R)        | 0 (R)          | 0 (R)     |
| GSBN                       | RSTB               | SPIE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | FE2                    | FE1                    | DE           | GW             | FS        |
| Global Status Bit Inverted | Reset              | SPI Error                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Functional Error Bit 2 | Functional Error Bit 1 | Device Error | Global Warning | Fail-Safe |
| Bit                        | Name               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                        |                        |              |                |           |
| 31                         | GSBN               | <b>Global Status Bit Inverted</b><br>The GSBN is a logical NOR combination of GSB Bits 24 to 30 (1)<br>This bit can also be used as global status flag without starting a complete communication frame as it is present at SDO directly after pulling CSN low. 0: error detected (one or several GSB bits from 24 to 30 are set)<br>1: no error detected (default after power-on)<br>Specific fault detection may be masked in the configuration registers 0x3F. A masked fault detection will still be reported in the GSB by the related fault flag, however it is not reflected in the GSBN (see Chapter <a href="#">Section 5.2.2</a> for masks). |                        |                        |              |                |           |
| 30                         | RSTB               | <b>Reset</b><br>The RSTB indicates that the NRESET output has been asserted low, this flag is set in case of<br>- power-down sequence<br>0: no reset signal has been generated (default) 1: Reset signal has been generated<br>RSTB is cleared by a Read and clear command to all bits in status register 1 causing the reset event.                                                                                                                                                                                                                                                                                                                  |                        |                        |              |                |           |
| 29                         | SPIE <sup>2)</sup> | <b>SPI Error Bit</b><br>The SPIE indicates errors related to a wrong SPI communication.<br>- SPI_SDI_STUCK_HIGH (SR4 - 0x24)<br>- SPI_SDI_STUCK_LOW (SR4 - 0x24)<br>- SPI_CSN_TIMEOUT (SR4 - 0x24)<br>- SPI_CRC_ERR (SR4 - 0x24)<br>- SPI_UNDEF_ADD (SR4 - 0x24)<br>- SPI_STATUS_WRT (SR4 - 0x24)<br>- SPI_CLK_CNT (SR4 - 0x24)<br>- SPI_LBISTED (SR4 - 0x24)<br>0: no error (default)<br>1: error detected                                                                                                                                                                                                                                           |                        |                        |              |                |           |
| 28                         | FE2                | <b>Functional Error Bit 2</b><br>The FE2 is a logical OR combination of errors related to the CAN transceiver.<br>- CAN_RXD_REC (SR2 - 0x22)<br>- CAN_PERM_REC (SR2 - 0x22)<br>- CAN_PERM_DOM (SR2 - 0x22)<br>- CAN_TXD_DOM (SR2 - 0x22)<br>0: no error (default) 1: error detected                                                                                                                                                                                                                                                                                                                                                                   |                        |                        |              |                |           |

| Global Status Byte GSB |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |        |        |        |        |        |
|------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|--------|
| Bit 31                 | Bit 30           | Bit 29                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Bit 28 | Bit 27 | Bit 26 | Bit 25 | Bit 24 |
|                        |                  | FE2 is cleared by a Read and clear command to all related bits in status registers 2 and 12.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |        |        |        |        |        |
| 27                     | FE1              | <b>Functional Error Bit 1</b><br>The FE1 is a logical OR combination of errors coming from functional blocks.<br>– OUTHS_OC (SR2 - 0x22)<br>– OUTHS_OL (SR2 - 0x22)<br>– BUCK1_UV (SR1 - 0x21)<br>– BUCK2_UV (SR1 - 0x21)<br>– BUCK3_UV (SR1 - 0x21)<br>– BUCK1_OV (SR1 - 0x21)<br>– BUCK2_OV (SR1 - 0x21)<br>– BUCK3_OV (SR1 - 0x21)<br>– BUCK1_OC (SR1 - 0x21)<br>– BUCK2_OC (SR1 - 0x21)<br>– BUCK3_OC (SR1 - 0x21)<br>– LDO2_UV (SR1 - 0x21)<br>– LDO2_OV (SR1 - 0x21)<br>BUCKX_PG_TIMEOUT from SPI request (SR1 - 0x21)<br>LDO2_PG_TIMEOUT from SPI request (SR1 - 0x21)<br>0: no error (default) 1: error detected<br>FE1 is cleared by a Read and clear command to all related bits in status registers 1 and 2 |        |        |        |        |        |
| 26                     | DE               | <b>Device Error Bit</b><br>DE is a logical OR combination of global errors related to the device.<br>– FBB_OV (SR2 - 0x22)<br>– FBB_UV (SR2 - 0x22)<br>– VIO_UV (SR2 - 0x22)<br>– TSD_CLx (SR2 - 0x22)<br>– WD_ENA_ECHO_ERROR (SR2 - 0x22)<br>– FCCU_ENA_ECHO_ERROR (SR2 - 0x22)<br>– NFSO1_ECHO_ERROR (SR2 - 0x22)<br>– IRQ_ECHO_ERROR (SR2 - 0x22)<br>– NRST_ECHO_ERROR (SR2 - 0x22)<br>0: no error (default) 1: error detected<br>DE is cleared by a Read & Clear command to all related bits in status registers 2                                                                                                                                                                                                 |        |        |        |        |        |
| 25                     | GW <sup>2)</sup> | <b>Global Warning Bit</b><br>GW is a logical OR combination of warning flags. Warning bits do not lead to any device state change or switch-off of functions.<br>– FBB_UV_EW (SR4 - 0x24)<br>– FBB_OV_EW (SR4 - 0x24)<br>– VS_UV_EW (SR4 - 0x24)<br>– CAN_SUP_LOW (SR4 - 0x24)<br>– TW_CLx (SR4 - 0x24)<br>0: no error (default) 1: error detected<br>GW is cleared by a Read and clear command to all related bits in status register 2,4                                                                                                                                                                                                                                                                             |        |        |        |        |        |
| 24                     | FS               | <b>Fail Safe</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |        |        |        |        |        |

| Global Status Byte GSB |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |        |        |        |        |        |
|------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|--------|
| Bit 31                 | Bit 30 | Bit 29                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Bit 28 | Bit 27 | Bit 26 | Bit 25 | Bit 24 |
|                        |        | <p>The FS bit indicates the device was forced into DEEP-SLEEP, REC-1 or -2 state due to the following fault conditions:</p> <ul style="list-style-type: none"> <li>- FCCUFAIL (SR3 - 0x23)</li> <li>- WDFAIL (SR3 - 0x23)</li> <li>- FORCED_SLEEP_TSD (SR3 - 0x23)</li> <li>- FORCED_SLEEP_POWUP (SR5 - 0x25)</li> <li>- GNDLOSS (SR3 - 0x23)</li> <li>INT_REG_UV (SR3 - 0x23)</li> <li>INT_REG_OV (SR3 - 0x23)</li> <li>CURRENT_MISMATCH (SR3 - 0x23)</li> <li>OSC_ERROR (SR3 - 0x23)</li> <li>LBIST_ERROR (SR3 - 0x23) <sup>(1)</sup></li> <li>NVM_COMP_ERROR (SR3 - 0x23)</li> <li>NVM_CRC_ERROR (SR3 - 0x23)</li> <li>SPI_REG_COMP_ERROR (SR3 - 0x23)</li> <li>FSM_COMP_ERROR (SR3 - 0x23)</li> </ul> <p>All control registers are set to default</p> <p>control registers are blocked for WRITE access except the following bits:</p> <ul style="list-style-type: none"> <li>- error flags</li> <li>- wakeup settings</li> <li>- timer setting</li> </ul> <p>1: Fail Safe active</p> <p>FS is cleared by a Read and clear command to all related bits in status register SR3 and SR5</p> |        |        |        |        |        |

1. Only after a DO\_POWER\_CYCLE.

## 9.2 Control register overview

**Table 67. Control register overview**

| bit              | 31   | 30                 | 29                           | 28                                | 27                      | 26                   | 25                        | 24                    | Mode               |
|------------------|------|--------------------|------------------------------|-----------------------------------|-------------------------|----------------------|---------------------------|-----------------------|--------------------|
| OpCode + Address | OC1  | OC2                | A5                           | A4                                | A3                      | A2                   | A1                        | A0                    | R/W                |
| Control Register |      |                    |                              |                                   |                         |                      |                           |                       |                    |
| Addr.            | bits | 23                 | 22                           | 21                                | 20                      | 19                   | 18                        | 17                    | 16                 |
|                  |      | 15                 | 14                           | 13                                | 12                      | 11                   | 10                        | 9                     | 8                  |
|                  |      | 7                  | 6                            | 5                                 | 4                       | CRC 3                | CRC 2                     | CRC 1                 | CRC 0              |
| 0x00             | MSB  | reserved           |                              |                                   |                         |                      |                           |                       |                    |
|                  |      | reserved           |                              |                                   |                         |                      |                           |                       |                    |
|                  | LSB  | reserved           |                              |                                   |                         |                      |                           |                       |                    |
| 0x01             | MSB  | RES                | RES                          | RES                               | RES                     | RES                  | WD_NRST_MASK              | WD_TIME_3             | WD_TIME_2          |
|                  |      | WD_TIME_1          | WD_TIME_0                    | VBUCK3_ENA                        | VBUCK2_ENA              | VBUCK1_ENA           | LDO1_ENA                  | LDO2_ENA              | LOW_POWER_SET      |
|                  | LSB  | WD_LP_ENA          | DO_POWER_DOWN                | U-NVM_PROG                        | DO_POWER_CYCLE          | CRC 3                | CRC 2                     | CRC 1                 | CRC 0              |
| 0x02             | MSB  | RES                | RES                          | NFSO_ASSERT_LOW                   | LBIST                   | ABIST                | RES                       | FCCU_COUNT_ER_12      | FCCU_COUNT_ER_11   |
|                  |      | FCCU_COUNT_ER_10   | FCCU_COUNT_ER_9              | FCCU_COUNT_ER_8                   | FCCU_COUNT_ER_7         | FCCU_COUNT_ER_6      | FCCU_COUNT_ER_5           | FCCU_COUNT_ER_4       | FCCU_COUNT_ER_3    |
|                  | LSB  | FCCU_COUNT_ER_2    | FCCU_COUNT_ER_1              | FCCU_COUNT_ER_0                   | FCCU_ENA                | CRC 3                | CRC 2                     | CRC 1                 | CRC 0              |
| 0x03             | MSB  | RES                | RES                          | BUCK3_SPREAD_ENA                  | BUCK2_SPREAD_ENA        | BUCK1_SPREAD_ENA     | CLR_WDFAIL_CNT            | RES                   | BUCK3_FTUNE_2      |
|                  |      | BUCK3_FTUNE_1      | BUCK3_FTUNE_0                | BOOST_OFF                         | FBB_OV_EW_TH_3          | FBB_OV_EW_TH_2       | FBB_OV_EW_TH_1            | FBB_OV_EW_TH_0        | FBB_UV_EW_TH_3     |
|                  | LSB  | FBB_UV_EW_TH_2     | FBB_UV_EW_TH_1               | FBB_UV_EW_TH_0                    | SPI_PROTECT_ACCESS      | CRC 3                | CRC 2                     | CRC 1                 | CRC 0              |
| 0x04             | MSB  | RES                | BOOST_DSMON_TH_2             | BOOST_DSMON_TH_1                  | BOOST_DSMON_TH_0        | SWDBG_EXIT           | VS_UV_EW_TH_4             | VS_UV_EW_TH_3         | VS_UV_EW_TH_2      |
|                  |      | VS_UV_EW_TH_1      | VS_UV_EW_TH_0                | FCCU_PROTOCOL                     | FCCU_STATIC_ERROR       | OUTHS_1              | OUTHS_0                   | BYPASS_DSMON_TH_2     | BYPASS_DSMON_TH_1  |
|                  | LSB  | BYPASS_DSMON_TH_0  | CLR_REG_FAIL_CNT             | KILL_SWDBG_TIMEOUT                | WD_TRIG                 | CRC 3                | CRC 2                     | CRC 1                 | CRC 0              |
| 0x05             | MSB  | RES                | CLR_REC2_FROM_DO_POWER_CYCLE | CLR_DEEP_SLEEP_FROM_DO_POWER_DOWN | CLR_POWERUP_RETRY_COUNT | T1_ENA_2             | T1_ENA_1                  | T1_ENA_0              | T1_PER_2           |
|                  |      | T1_PER_1           | T1_PER_0                     | TIMER_WAKE_ENA                    | IGN_CONFIG              | IGN_FILT             | IGN_ENA                   | IGN_PU                | WU_CONFIG          |
|                  | LSB  | WU_ENA             | WU_PU                        | WU_FILT                           | TIMER_ENA               | CRC 3                | CRC 2                     | CRC 1                 | CRC 0              |
| 0x06             | MSB  | RES                | MASK_BUCK3_PG_TIMEOUT_IRQ    | MASK_BUCK3_OC_IRQ                 | MASK_BUCK3_PG_IRQ       | MASK_BUCK3_IRQ       | MASK_BUCK2_PG_TIMEOUT_IRQ | MASK_BUCK2_OC_IRQ     | MASK_BUCK2_PG_IRQ  |
|                  |      | MASK_BUCK2_IRQ     | MASK_BUCK1_PG_TIMEOUT_IRQ    | MASK_BUCK1_OC_IRQ                 | MASK_BUCK1_PG_IRQ       | MASK_BUCK1_IRQ       | MASK_FBB_OV_IRQ           | MASK_FBB_UV_IRQ       | MASK_FBB_OV_EW_IRQ |
|                  | LSB  | MASK_FBB_UV_EW_IRQ | MASK_LDO2_PG_IRQ             | MASK_LDO2_PG_TIMEOUT_IRQ          | MASK_LDO2_IRQ           | CRC 3                | CRC 2                     | CRC 1                 | CRC 0              |
| 0x07             | MSB  | RES                | MASK_LDO1_PG_IRQ             | MASK_LDO1_PG_TIMEOUT_IRQ          | MASK_LDO1_IRQ           | MASK_BOOST_IN_LP_IRQ | MASK_BYPASS_VDSMON_IRQ    | MASK_BOOST_VDSMON_IRQ | IRQ_REQUEST        |
|                  |      | MASK_VS_EW_IRQ     | MASK_CAN_IRQ                 | MASK_CL4_TW_IRQ                   | MASK_CL3_TW_IRQ         | MASK_CL2_TW_IRQ      | MASK_CL1_TW_IRQ           | MASK_CL0_TW_IRQ       | MASK_OUTHS_IRQ     |



|      |       |     |                                 |                                  |                                    |                                     |                                 |                                      |                                 |                                 |     |
|------|-------|-----|---------------------------------|----------------------------------|------------------------------------|-------------------------------------|---------------------------------|--------------------------------------|---------------------------------|---------------------------------|-----|
| 0x07 | DCR 7 | LSB | MASK_SPI_ER<br>ROR_IRQ          | MASK_NFSO1<br>_ECHO_ERR<br>R_IRQ | MASK_WD_EN<br>A_ECHO_ERR<br>OR_IRQ | MASK_FCCU<br>ENA_ECHO_E<br>RROR_IRQ | CRC 3                           | CRC 2                                | CRC 1                           | CRC 0                           | R/W |
| 0x08 | DCR 8 | MSB | RES                             | MASK_SWDBG<br>_VIO_IRQ           | MASK_LP_REA<br>DY_IRQ              | CLR_TSD_CNT<br>_FAIL                | MASK_BUCK3<br>_OC_POWER_<br>OFF | MASK_BUCK2<br>_OC_POWER_<br>OFF      | MASK_BUCK1<br>_OC_POWER_<br>OFF | MASK_BUCK3<br>_UV_POWER_<br>OFF | R/W |
|      |       |     | MASK_BUCK2<br>_UV_POWER_<br>OFF | MASK_BUCK1<br>_UV_POWER_<br>OFF  | MASK_TW_GW                         | MASK_OL_GS<br>B                     | MASK_FE2_GS<br>B                | MASK_GW_GS<br>B                      | CAN_ACT                         | CAN_AUTO_BI<br>AS               |     |
|      |       | LSB | CAN_LOOP_E<br>NA                | CAN_REC_ON<br>LY                 | CAN_WU_ENA                         | GO_INIT                             | CRC 3                           | CRC 2                                | CRC 1                           | CRC 0                           |     |
| 0x09 | DCR 9 | MSB | RES                             | LDT_TIMER_R<br>EAD_ENA           | RES                                | BOOST_CNT_<br>END                   | RES                             | MASK_BOOST<br>_TIMER_CNT_<br>END_IRQ | LDT_CNT_THR<br>_4               | LDT_CNT_THR<br>_3               | R/W |
|      |       |     | LDT_CNT_THR<br>_2               | LDT_CNT_THR<br>_1                | LDT_CNT_THR<br>_0                  | LDT_CNT_THR<br>_MSB_POS_4           | LDT_CNT_THR<br>_MSB_POS_3       | LDT_CNT_THR<br>_MSB_POS_2            | LDT_CNT_THR<br>_MSB_POS_1       | LDT_CNT_THR<br>_MSB_POS_0       |     |
|      |       | LSB | LDT_DEBUG                       | LDT_MODE                         | LDT_ENA                            | LDT_CNT_ENA                         | CRC 3                           | CRC 2                                | CRC 1                           | CRC 0                           |     |

### 9.3 U\_NVM register overview

**Table 68. U\_NVM Register Overview**

| bit              |       |      | 31                               | 30                              | 29                                | 28                                | 27                                | 26                      | 25                      | 24                              | Mode |
|------------------|-------|------|----------------------------------|---------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-------------------------|-------------------------|---------------------------------|------|
| OpCode + Address |       |      | OC1                              | OC2                             | A5                                | A4                                | A3                                | A2                      | A1                      | A0                              | R/W  |
| U_NVM Register   |       |      |                                  |                                 |                                   |                                   |                                   |                         |                         |                                 |      |
| Addr             |       | bits | 23                               | 22                              | 21                                | 20                                | 19                                | 18                      | 17                      | 16                              |      |
|                  |       |      | 15                               | 14                              | 13                                | 12                                | 11                                | 10                      | 9                       | 8                               |      |
|                  |       |      | 7                                | 6                               | 5                                 | 4                                 | CRC 3                             | CRC 2                   | CRC 1                   | CRC 0                           |      |
| 0x0A             | DCR10 | MSB  | RES                              | RES                             | RES                               | RES                               | BUCK1_FREQ                        | BUCK1_PU_V<br>ALUE_1    | BUCK1_PU_V<br>ALUE_0    | BUCK1_PU_S<br>TEP_ENA_2         | R/W  |
|                  |       |      | BUCK1_PU_S<br>TEP_ENA_1          | BUCK1_PU_S<br>TEP_ENA_0         | BUCK1_PD_S<br>TEP_OFF_2           | BUCK1_PD_S<br>TEP_OFF_1           | BUCK1_PD_S<br>TEP_OFF_0           | BUCK1_IPEAK<br>_2       | BUCK1_IPEAK<br>_1       | BUCK1_IPEAK<br>_0               |      |
|                  |       | LSB  | BUCK1_REGF<br>AIL_GO_REC         | BUCK1_SS_V<br>ALUE_1            | BUCK1_SS_V<br>ALUE_0              | BUCK1_REFR<br>ESH_FREQ            | CRC 3                             | CRC 2                   | CRC 1                   | CRC 0                           |      |
| 0x0B             | DCR11 | MSB  | RES                              | RES                             | RES                               | RES                               | BUCK2_FREQ                        | BUCK2_PU_V<br>ALUE_1    | BUCK2_PU_V<br>ALUE_0    | BUCK2_PU_S<br>TEP_ENA_2         | R/W  |
|                  |       |      | BUCK2_PU_S<br>TEP_ENA_1          | BUCK2_PU_S<br>TEP_ENA_0         | BUCK2_PD_S<br>TEP_OFF_2           | BUCK2_PD_S<br>TEP_OFF_1           | BUCK2_PD_S<br>TEP_OFF_0           | BUCK2_IPEAK<br>_2       | BUCK2_IPEAK<br>_1       | BUCK2_IPEAK<br>_0               |      |
|                  |       | LSB  | BUCK2_REGF<br>AIL_GO_REC         | BUCK2_SS_V<br>ALUE_1            | BUCK2_SS_V<br>ALUE_0              | BUCK2_REFR<br>ESH_FREQ            | CRC 3                             | CRC 2                   | CRC 1                   | CRC 0                           |      |
| 0x0C             | DCR12 | MSB  | RES                              | RES                             | RES                               | RES                               | BYPASS_DIS                        | RES                     | RES                     | BUCK3_PU_V<br>ALUE              | R/W  |
|                  |       |      | BUCK3_PU_S<br>TEP_ENA_2          | BUCK3_PU_S<br>TEP_ENA_1         | BUCK3_PU_S<br>TEP_ENA_0           | BUCK3_PD_S<br>TEP_OFF_2           | BUCK3_PD_S<br>TEP_OFF_1           | BUCK3_PD_S<br>TEP_OFF_0 | BUCK3_IPEAK<br>_1       | BUCK3_IPEAK<br>_0               |      |
|                  |       | LSB  | BUCK3_REGF<br>AIL_GO_REC         | BUCK3_SS_V<br>ALUE_1            | BUCK3_SS_V<br>ALUE_0              | BUCK3_REFR<br>ESH_FREQ            | CRC 3                             | CRC 2                   | CRC 1                   | CRC 0                           |      |
| 0x0D             | DCR13 | MSB  | RES                              | RES                             | RES                               | RES                               | U_NVM_D_15                        | U_NVM_D_14              | U_NVM_D_13              | U_NVM_D_12                      | R/W  |
|                  |       |      | U_NVM_D_11                       | U_NVM_D_10                      | U_NVM_D_9                         | U_NVM_D_8                         | U_NVM_D_7                         | U_NVM_D_6               | U_NVM_D_5               | U_NVM_D_4                       |      |
|                  |       | LSB  | U_NVM_D_3                        | U_NVM_D_2                       | U_NVM_D_1                         | U_NVM_D_0                         | CRC 3                             | CRC 2                   | CRC 1                   | CRC 0                           |      |
| 0x0E             | DCR14 | MSB  | RES                              | RES                             | RES                               | RES                               | PU_LOOP_FO<br>R_EVER              | LDO2_REGFAI<br>L_GO_REC | LDO2_TRK_1              | LDO2_TRK_0                      | R/W  |
|                  |       |      | LDO2_PD_ST<br>EP_OFF_2           | LDO2_PD_ST<br>EP_OFF_1          | LDO2_PD_ST<br>EP_OFF_0            | LDO2_PU_ST<br>EP_ENA_2            | LDO2_PU_ST<br>EP_ENA_1            | LDO2_PU_ST<br>EP_ENA_0  | LDO1_PD_ST<br>EP_OFF_2  | LDO1_PD_ST<br>EP_OFF_1          |      |
|                  |       | LSB  | LDO1_PD_ST<br>EP_OFF_0           | LDO1_PU_ST<br>EP_ENA_2          | LDO1_PU_ST<br>EP_ENA_1            | LDO1_PU_ST<br>EP_ENA_0            | CRC 3                             | CRC 2                   | CRC 1                   | CRC 0                           |      |
| 0x0F             | DCR15 | MSB  | RES                              | RES                             | RES                               | RES                               | U_NVM_F_15                        | U_NVM_F_14              | PU_WAIT_DE<br>L_ENA_7_1 | PU_WAIT_DE<br>L_ENA_7_0         | R/W  |
|                  |       |      | PU_WAIT_DE<br>L_ENA_6_1          | PU_WAIT_DE<br>L_ENA_6_0         | PU_WAIT_DE<br>L_ENA_5_1           | PU_WAIT_DE<br>L_ENA_5_0           | PU_WAIT_DE<br>L_ENA_4_1           | PU_WAIT_DE<br>L_ENA_4_0 | PU_WAIT_DE<br>L_ENA_3_1 | PU_WAIT_DE<br>L_ENA_3_0         |      |
|                  |       | LSB  | PU_WAIT_DE<br>L_ENA_2_1          | PU_WAIT_DE<br>L_ENA_2_0         | PU_WAIT_DE<br>L_ENA_1_1           | PU_WAIT_DE<br>L_ENA_1_0           | CRC 3                             | CRC 2                   | CRC 1                   | CRC 0                           |      |
| 0x10             | DCR16 | MSB  | RES                              | RES                             | RES                               | RES                               | U_NVM_G_15                        | U_NVM_G_14              | U_NVM_G_13              | NRESET_PD_<br>STEP_ASSER<br>T_2 | R/W  |
|                  |       |      | NRESET_PD_<br>STEP_ASSER<br>T_1  | NRESET_PD_<br>STEP_ASSER<br>T_0 | NRESET_PU_<br>STEP_DEASS<br>ERT_2 | NRESET_PU_<br>STEP_DEASS<br>ERT_1 | NRESET_PU_<br>STEP_DEASS<br>ERT_0 | PU_WAIT_PG<br>_ENA_7    | PU_WAIT_PG<br>_ENA_6    | PU_WAIT_PG<br>_ENA_5            |      |
|                  |       | LSB  | PU_WAIT_PG<br>_ENA_4             | PU_WAIT_PG<br>_ENA_3            | PU_WAIT_PG<br>_ENA_2              | PU_WAIT_PG<br>_ENA_1              | CRC 3                             | CRC 2                   | CRC 1                   | CRC 0                           |      |
| 0x11             | DCR17 | MSB  | RES                              | RES                             | RES                               | RES                               | U_NVM_CRC0<br>_7                  | U_NVM_CRC0<br>_6        | U_NVM_CRC0<br>_5        | U_NVM_CRC0<br>_4                | R/W  |
|                  |       |      | U_NVM_CRC0<br>_3                 | U_NVM_CRC0<br>_2                | U_NVM_CRC0<br>_1                  | U_NVM_CRC0<br>_0                  | U_PROG0_1                         | U_PROG0_0               | U_NVM_H_5               | U_NVM_H_4                       |      |
|                  |       | LSB  | NFSO_STATE<br>_IN_DEEP_SL<br>EEP | U_NVM_H_2                       | U_NVM_H_1                         | BOOST_DIS                         | CRC 3                             | CRC 2                   | CRC 1                   | CRC 0                           |      |

|      |       |     |                         |                                |                         |                         |                            |                            |                          |                          |     |
|------|-------|-----|-------------------------|--------------------------------|-------------------------|-------------------------|----------------------------|----------------------------|--------------------------|--------------------------|-----|
| 0x12 | DCR18 | MSB | RES                     | RES                            | RES                     | RES                     | PD_WAIT_VR<br>EG_DEL_OFF_1 | PD_WAIT_VR<br>EG_DEL_OFF_0 | PD_WAIT_DE<br>L_OFF_7_1  | PD_WAIT_DE<br>L_OFF_7_0  | R/W |
|      |       |     | PD_WAIT_DE<br>L_OFF_6_1 | PD_WAIT_DE<br>L_OFF_6_0        | PD_WAIT_DE<br>L_OFF_5_1 | PD_WAIT_DE<br>L_OFF_5_0 | PD_WAIT_DE<br>L_OFF_4_1    | PD_WAIT_DE<br>L_OFF_4_0    | PD_WAIT_DE<br>L_OFF_3_1  | PD_WAIT_DE<br>L_OFF_3_0  |     |
|      |       | LSB | PD_WAIT_DE<br>L_OFF_2_1 | PD_WAIT_DE<br>L_OFF_2_0        | PD_WAIT_DE<br>L_OFF_1_1 | PD_WAIT_DE<br>L_OFF_1_0 | CRC 3                      | CRC 2                      | CRC 1                    | CRC 0                    |     |
| 0x13 | DCR19 | MSB | RES                     | RES                            | RES                     | RES                     | U_NVM_RELE<br>ASE_15       | U_NVM_RELE<br>ASE_14       | U_NVM_RELE<br>ASE_13     | U_NVM_RELE<br>ASE_12     | R/W |
|      |       |     | U_NVM_RELE<br>ASE_11    | U_NVM_RELE<br>ASE_10           | U_NVM_RELE<br>ASE_9     | U_NVM_RELE<br>ASE_8     | U_NVM_RELE<br>ASE_7        | U_NVM_RELE<br>ASE_6        | U_NVM_RELE<br>ASE_5      | U_NVM_RELE<br>ASE_4      |     |
|      |       | LSB | U_NVM_RELE<br>ASE_3     | U_NVM_RELE<br>ASE_2            | U_NVM_RELE<br>ASE_1     | U_NVM_RELE<br>ASE_0     | CRC 3                      | CRC 2                      | CRC 1                    | CRC 0                    |     |
| 0x14 | DCR20 | MSB | RES                     | RES                            | RES                     | RES                     | FBB_OK_SEL_1               | FBB_OK_SEL_0               | BYPASS_OFF<br>SET_SEL    | FBB_REG_LE<br>VEL_SEL_1  | R/W |
|      |       |     | FBB_REG_LE<br>VEL_SEL_0 | WAKEUP_GO<br>TO_DEEP_SLEEP_INH | BOOST_CRK_TO_2          | BOOST_CRK_TO_1          | BOOST_CRK_TO_0             | BOOST_CRK_ONLY             | VS_SENSE_L<br>EVEL_SEL_1 | VS_SENSE_L<br>EVEL_SEL_0 |     |
|      |       | LSB | LOW_SET_3               | LOW_SET_2                      | LOW_SET_1               | LOW_SET_0               | CRC 3                      | CRC 2                      | CRC 1                    | CRC 0                    |     |
| 0x15 | DCR21 | MSB | RES                     | RES                            | RES                     | RES                     | U_NVM_L_15                 | U_NVM_L_14                 | U_NVM_L_13               | U_NVM_L_12               | R/W |
|      |       |     | U_NVM_L_11              | U_NVM_L_10                     | U_NVM_L_9               | U_NVM_L_8               | U_NVM_L_7                  | U_NVM_L_6                  | U_NVM_L_5                | U_NVM_L_4                |     |
|      |       | LSB | RES                     | RES                            | FBB_UV_EW_PD            | FBB_UV_LEV<br>EL_SEL    | CRC 3                      | CRC 2                      | CRC 1                    | CRC 0                    |     |
| 0x16 | DCR22 | MSB | RES                     | RES                            | RES                     | RES                     | U_NVM_M_15                 | U_NVM_M_14                 | U_NVM_M_13               | U_NVM_M_12               | R/W |
|      |       |     | U_NVM_M_11              | U_NVM_M_10                     | U_NVM_M_9               | U_NVM_M_8               | U_NVM_M_7                  | U_NVM_M_6                  | U_NVM_M_5                | U_NVM_M_4                |     |
|      |       | LSB | U_NVM_M_3               | U_NVM_M_2                      | U_NVM_M_1               | U_NVM_M_0               | CRC 3                      | CRC 2                      | CRC 1                    | CRC 0                    |     |
| 0x17 | DCR23 | MSB | RES                     | RES                            | RES                     | RES                     | U_NVM_N_15                 | U_NVM_N_14                 | U_NVM_N_13               | U_NVM_N_12               | R/W |
|      |       |     | U_NVM_N_11              | U_NVM_N_10                     | U_NVM_N_9               | U_NVM_N_8               | U_NVM_N_7                  | U_NVM_N_6                  | U_NVM_N_5                | U_NVM_N_4                |     |
|      |       | LSB | U_NVM_N_3               | U_NVM_N_2                      | U_NVM_N_1               | U_NVM_N_0               | CRC 3                      | CRC 2                      | CRC 1                    | CRC 0                    |     |
| 0x18 | DCR24 | MSB | RES                     | RES                            | RES                     | RES                     | U_NVM_O_15                 | U_NVM_O_14                 | U_NVM_O_13               | U_NVM_O_12               | R/W |
|      |       |     | U_NVM_O_11              | U_NVM_O_10                     | U_NVM_O_9               | U_NVM_O_8               | U_NVM_O_7                  | U_NVM_O_6                  | U_NVM_O_5                | U_NVM_O_4                |     |
|      |       | LSB | U_NVM_O_3               | U_NVM_O_2                      | U_NVM_O_1               | U_NVM_O_0               | CRC 3                      | CRC 2                      | CRC 1                    | CRC 0                    |     |
| 0x19 | DCR25 | MSB | RES                     | RES                            | RES                     | RES                     | U_NVM_CRC1_7               | U_NVM_CRC1_6               | U_NVM_CRC1_5             | U_NVM_CRC1_4             | R/W |
|      |       |     | U_NVM_CRC1_3            | U_NVM_CRC1_2                   | U_NVM_CRC1_1            | U_NVM_CRC1_0            | U_PROG1_1                  | U_PROG1_0                  | U_NVM_P_5                | U_NVM_P_4                |     |
|      |       | LSB | U_NVM_P_3               | U_NVM_P_2                      | U_NVM_P_1               | U_NVM_P_0               | CRC 3                      | CRC 2                      | CRC 1                    | CRC 0                    |     |

**Table 69. USER\_NVM setting used for configuration1**

| NVM Sector   | Bit Number | Field Name           | Configuration 1 | Comment                                   |
|--------------|------------|----------------------|-----------------|-------------------------------------------|
| DCR10 (0x0A) | 0          | BUCK1_REFRESH_FREQ   | 1               | Buck1 refresh frequency at 1 kHz          |
|              | 1          | BUCK1_SS_VALUE[0]    | 1               | Buck1 soft-start at 8.25 V/ms             |
|              | 2          | BUCK1_SS_VALUE[1]    | 0               |                                           |
|              | 3          | BUCK1_REGFAIL_GO_REC | 1               | Buck1 defined as critical for application |
|              | 4          | BUCK1_IPEAK[0]       | 0               | Buck1 peak limitation current @ 5.0 A     |
|              | 5          | BUCK1_IPEAK[1]       | 1               |                                           |
|              | 6          | BUCK1_IPEAK[2]       | 1               |                                           |
|              | 7          | BUCK1_PD_STEP_OFF[0] | 1               | Buck1 turn-off at step 4                  |
|              | 8          | BUCK1_PD_STEP_OFF[1] | 1               |                                           |
|              | 9          | BUCK1_PD_STEP_OFF[2] | 0               |                                           |
|              | 10         | BUCK1_PU_STEP_ENA[0] | 1               | Buck1 turn-on at step 1                   |
|              | 11         | BUCK1_PU_STEP_ENA[1] | 0               |                                           |

| NVM Sector   | Bit Number | Field Name           | Configuration 1 | Comment                                       |
|--------------|------------|----------------------|-----------------|-----------------------------------------------|
| DCR10 (0x0A) | 12         | BUCK1_PU_STEP_ENA[2] | 0               | Buck1 turn-on at step 1                       |
|              | 13         | BUCK1_PU_VALUE[0]    | 0               | Buck1 voltage setting at 3.3 V                |
|              | 14         | BUCK1_PU_VALUE[1]    | 0               |                                               |
|              | 15         | BUCK1_FREQ           | 1               | Buck1 switching frequency at 400 kHz          |
| DCR11 (0x0B) | 0          | BUCK2_REFRESH_FREQ   | 1               | Buck2 refresh frequency at 1 kHz              |
|              | 1          | BUCK2_SS_VALUE[0]    | 1               | Buck2 soft-start at 8.25 V/ms                 |
|              | 2          | BUCK2_SS_VALUE[1]    | 0               |                                               |
|              | 3          | BUCK2_REGFAIL_GO_REC | 0               | Buck2 defined as not critical for application |
|              | 4          | BUCK2_IPEAK[0]       | 0               | Buck2 peak limitation current @ 4.0 A         |
|              | 5          | BUCK2_IPEAK[1]       | 0               |                                               |
|              | 6          | BUCK2_IPEAK[2]       | 1               |                                               |
|              | 7          | BUCK2_PD_STEP_OFF[0] | 1               | Buck2 turn-off at step 4                      |
|              | 8          | BUCK2_PD_STEP_OFF[1] | 1               |                                               |
|              | 9          | BUCK2_PD_STEP_OFF[2] | 0               |                                               |
|              | 10         | BUCK2_PU_STEP_ENA[0] | 1               | Buck2 turn-on at step 3                       |
|              | 11         | BUCK2_PU_STEP_ENA[1] | 1               |                                               |
|              | 12         | BUCK2_PU_STEP_ENA[2] | 0               |                                               |
|              | 13         | BUCK2_PU_VALUE[0]    | 1               | Buck2 voltage setting at 5.0 V                |
|              | 14         | BUCK2_PU_VALUE[1]    | 0               |                                               |
|              | 15         | BUCK2_FREQ           | 1               | Buck2 switching frequency at 400 kHz          |
| DCR12 (0x0C) | 0          | BUCK3_REFRESH_FREQ   | 1               | Buck3 refresh frequency at 1 kHz              |
|              | 1          | BUCK3_SS_VALUE[0]    | 1               | Buck3 soft-start at 0.87 V/ms                 |
|              | 2          | BUCK3_SS_VALUE[1]    | 1               |                                               |
|              | 3          | BUCK3_REGFAIL_GO_REC | 1               | Buck3 defined as critical for application     |
|              | 4          | BUCK3_IPEAK[0]       | 1               | Buck3 peak limitation current @ 7.0 A         |
|              | 5          | BUCK3_IPEAK[1]       | 1               |                                               |
|              | 6          | BUCK3_PD_STEP_OFF[0] | 0               | Buck3 turn-off at step 3                      |
|              | 7          | BUCK3_PD_STEP_OFF[1] | 1               |                                               |
|              | 8          | BUCK3_PD_STEP_OFF[2] | 0               |                                               |
|              | 9          | BUCK3_PU_STEP_ENA[0] | 0               | Buck3 turn-on at step 2                       |
|              | 10         | BUCK3_PU_STEP_ENA[1] | 1               |                                               |
|              | 11         | BUCK3_PU_STEP_ENA[2] | 0               |                                               |
|              | 12         | BUCK3_PU_VALUE       | 1               | Buck3 voltage setting at 1.02 V               |
|              | 13         | U_NVM_C[13]          | 0               |                                               |
|              | 14         | U_NVM_C[14]          | 0               |                                               |
|              | 15         | BYPASS_DIS           | 0               | Bypass not disabled                           |
| DCR13 (0x0D) | 0          | U_NVM_D[0]           | 0               |                                               |
|              | 1          | U_NVM_D[1]           | 0               |                                               |
|              | 2          | U_NVM_D[2]           | 0               |                                               |
|              | 3          | U_NVM_D[3]           | 0               |                                               |
|              | 4          | U_NVM_D[4]           | 0               |                                               |

| NVM Sector   | Bit Number | Field Name           | Configuration 1 | Comment                                      |
|--------------|------------|----------------------|-----------------|----------------------------------------------|
| DCR13 (0x0D) | 5          | U_NVM_D[5]           | 0               |                                              |
|              | 6          | U_NVM_D[6]           | 0               |                                              |
|              | 7          | U_NVM_D[7]           | 0               |                                              |
|              | 8          | U_NVM_D[8]           | 0               |                                              |
|              | 9          | U_NVM_D[9]           | 0               |                                              |
|              | 10         | U_NVM_D[10]          | 0               |                                              |
|              | 11         | U_NVM_D[11]          | 0               |                                              |
|              | 12         | U_NVM_D[12]          | 0               |                                              |
|              | 13         | U_NVM_D[13]          | 0               |                                              |
|              | 14         | U_NVM_D[14]          | 0               |                                              |
|              | 15         | U_NVM_D[15]          | 0               |                                              |
| DCR14 (0x0E) | 0          | LDO1_PU_STEP_ENA[0]  | 1               | LDO1 turn-on at step 5                       |
|              | 1          | LDO1_PU_STEP_ENA[1]  | 0               |                                              |
|              | 2          | LDO1_PU_STEP_ENA[2]  | 1               |                                              |
|              | 3          | LDO1_PD_STEP_OFF[0]  | 1               | LDO1 turn-off at step 2                      |
|              | 4          | LDO1_PD_STEP_OFF[1]  | 0               |                                              |
|              | 5          | LDO1_PD_STEP_OFF[2]  | 0               |                                              |
|              | 6          | LDO2_PU_STEP_ENA[0]  | 0               | LDO2 turn-on at step 4                       |
|              | 7          | LDO2_PU_STEP_ENA[1]  | 0               |                                              |
|              | 8          | LDO2_PU_STEP_ENA[2]  | 1               |                                              |
|              | 9          | LDO2_PD_STEP_OFF[0]  | 1               | LDO2 turn-off at step 2                      |
|              | 10         | LDO2_PD_STEP_OFF[1]  | 0               |                                              |
|              | 11         | LDO2_PD_STEP_OFF[2]  | 0               |                                              |
|              | 12         | LDO2_TRK[0]          | 1               | LDO2 tracker of Buck2                        |
|              | 13         | LDO2_TRK[1]          | 0               |                                              |
|              | 14         | LDO2_REGFAIL_GO_REC  | 0               | LDO2 defined as not critical for application |
|              | 15         | PU_LOOP_FOR_EVER     | 0               | Power-up sequence not set at infinite retry  |
| DCR15 (0x0F) | 0          | PU_WAIT_DEL_ENA_1[0] | 0               | Power-up delay at step 1 equal to 0 ms       |
|              | 1          | PU_WAIT_DEL_ENA_1[1] | 0               |                                              |
|              | 2          | PU_WAIT_DEL_ENA_2[0] | 0               | Power-up delay at step 2 equal to 0 ms       |
|              | 3          | PU_WAIT_DEL_ENA_2[1] | 0               |                                              |
|              | 4          | PU_WAIT_DEL_ENA_3[0] | 0               | Power-up delay at step 3 equal to 0 ms       |
|              | 5          | PU_WAIT_DEL_ENA_3[1] | 0               |                                              |
|              | 6          | PU_WAIT_DEL_ENA_4[0] | 0               | Power-up delay at step 4 equal to 0 ms       |
|              | 7          | PU_WAIT_DEL_ENA_4[1] | 0               |                                              |
|              | 8          | PU_WAIT_DEL_ENA_5[0] | 0               | Power-up delay at step 5 equal to 0 ms       |
|              | 9          | PU_WAIT_DEL_ENA_5[1] | 0               |                                              |
|              | 10         | PU_WAIT_DEL_ENA_6[0] | 0               | Power-up delay at step 6 equal to 0 ms       |
|              | 11         | PU_WAIT_DEL_ENA_6[1] | 0               |                                              |
|              | 12         | PU_WAIT_DEL_ENA_7[0] | 0               | Power-up delay at step 7 equal to 0 ms       |
|              | 13         | PU_WAIT_DEL_ENA_7[1] | 0               |                                              |

| NVM Sector   | Bit Number | Field Name                 | Configuration 1 | Comment                                                    |
|--------------|------------|----------------------------|-----------------|------------------------------------------------------------|
| DCR15 (0x0F) | 14         | U_NVM_F[14]                | 0               |                                                            |
|              | 15         | U_NVM_F[15]                | 0               |                                                            |
| DCR16 (0x10) | 0          | PU_WAIT_PG_ENA[1]          | 1               | at power-up step 1, wait for power-good signal             |
|              | 1          | PU_WAIT_PG_ENA[2]          | 1               | at power-up step 2, wait for power-good signal             |
|              | 2          | PU_WAIT_PG_ENA[3]          | 1               | at power-up step 3, wait for power-good signal             |
|              | 3          | PU_WAIT_PG_ENA[4]          | 1               | at power-up step 4, wait for power-good signal             |
|              | 4          | PU_WAIT_PG_ENA[5]          | 0               | at power-up step 5, no wait for power-good signal          |
|              | 5          | PU_WAIT_PG_ENA[6]          | 0               | at power-up step 6, no wait for power-good signal          |
|              | 6          | PU_WAIT_PG_ENA[7]          | 0               | at power-up step 7, no wait for power-good signal          |
|              | 7          | NRESET_PU_STEP_DEASSERT[0] | 0               | NRESET deassertion at step 7 at power-up                   |
|              | 8          | NRESET_PU_STEP_DEASSERT[1] | 1               |                                                            |
|              | 9          | NRESET_PU_STEP_DEASSERT[2] | 1               |                                                            |
|              | 10         | NRESET_PD_STEP_ASSERT[0]   | 0               | NRESET assertion at step 1 at power-down                   |
|              | 11         | NRESET_PD_STEP_ASSERT[1]   | 0               |                                                            |
|              | 12         | NRESET_PD_STEP_ASSERT[2]   | 0               |                                                            |
|              | 13         | U_NVM_G[13]                | 0               |                                                            |
|              | 14         | U_NVM_G[14]                | 0               |                                                            |
|              | 15         | U_NVM_G[15]                | 0               |                                                            |
| DCR17 (0x11) | 0          | BOOST_DIS                  | 0               | Boost is not disabled and depends on BOOST_OFF control bit |
|              | 1          | U_NVM_H[1]                 | 0               |                                                            |
|              | 2          | U_NVM_H[2]                 | 0               |                                                            |
|              | 3          | NFSO_STATE_IN_DEEP_SLEEP   | 1               | NFSO pin will be high when FSM in DEEP-SLEEP state         |
|              | 4          | U_NVM_H[4]                 | 0               |                                                            |
|              | 5          | U_NVM_H[5]                 | 0               |                                                            |
|              | 6          | U_PROG0[0]                 | 0               |                                                            |
|              | 7          | U_PROG0[1]                 | 0               |                                                            |
|              | 8          | U_NVM_CRC0[0]              | X               |                                                            |
|              | 9          | U_NVM_CRC0[1]              | X               |                                                            |
|              | 10         | U_NVM_CRC0[2]              | X               |                                                            |
|              | 11         | U_NVM_CRC0[3]              | X               |                                                            |
|              | 12         | U_NVM_CRC0[4]              | X               |                                                            |
|              | 13         | U_NVM_CRC0[5]              | X               |                                                            |
|              | 14         | U_NVM_CRC0[6]              | X               |                                                            |
|              | 15         | U_NVM_CRC0[7]              | X               |                                                            |
| DCR18 (0x12) | 0          | PD_WAIT_DEL_OFF_1[0]       | 1               | Power-down delay at step 1 equal to 2 ms                   |
|              | 1          | PD_WAIT_DEL_OFF_1[1]       | 0               |                                                            |
|              | 2          | PD_WAIT_DEL_OFF_2[0]       | 1               | Power-down delay at step 2 equal to 2 ms                   |
|              | 3          | PD_WAIT_DEL_OFF_2[1]       | 0               |                                                            |

| NVM Sector   | Bit Number | Field Name                  | Configuration 1 | Comment                                                                       |
|--------------|------------|-----------------------------|-----------------|-------------------------------------------------------------------------------|
| DCR18 (0x12) | 4          | PD_WAIT_DEL_OFF_3[0]        | 1               | Power-down delay at step 3 equal to 2 ms                                      |
|              | 5          | PD_WAIT_DEL_OFF_3[1]        | 0               |                                                                               |
|              | 6          | PD_WAIT_DEL_OFF_4[0]        | 1               | Power-down delay at step 4 equal to 2 ms                                      |
|              | 7          | PD_WAIT_DEL_OFF_4[1]        | 0               |                                                                               |
|              | 8          | PD_WAIT_DEL_OFF_5[0]        | 1               | Power-down delay at step 5 equal to 2 ms                                      |
|              | 9          | PD_WAIT_DEL_OFF_5[1]        | 0               |                                                                               |
|              | 10         | PD_WAIT_DEL_OFF_6[0]        | 1               | Power-down delay at step 6 equal to 2 ms                                      |
|              | 11         | PD_WAIT_DEL_OFF_6[1]        | 0               |                                                                               |
|              | 12         | PD_WAIT_DEL_OFF_7[0]        | 1               | Power-down delay at step 7 equal to 2 ms                                      |
|              | 13         | PD_WAIT_DEL_OFF_7[1]        | 0               |                                                                               |
|              | 14         | PD_WAIT_VREG_DEL_OFF[0]     | 0               | Power-down delay for VREG equal to 10 ms after the end of power-down sequence |
|              | 15         | PD_WAIT_VREG_DEL_OFF[1]     | 1               |                                                                               |
| DCR19 (0x13) | 0          | U_NVM_RELEASE[0]            | 1               | NVM release 1                                                                 |
|              | 1          | U_NVM_RELEASE[1]            | 0               |                                                                               |
|              | 2          | U_NVM_RELEASE[2]            | 0               |                                                                               |
|              | 3          | U_NVM_RELEASE[3]            | 0               |                                                                               |
|              | 4          | U_NVM_RELEASE[4]            | 0               |                                                                               |
|              | 5          | U_NVM_RELEASE[5]            | 0               |                                                                               |
|              | 6          | U_NVM_RELEASE[6]            | 0               |                                                                               |
|              | 7          | U_NVM_RELEASE[7]            | 0               |                                                                               |
|              | 8          | U_NVM_RELEASE[8]            | 0               |                                                                               |
|              | 9          | U_NVM_RELEASE[9]            | 0               |                                                                               |
|              | 10         | U_NVM_RELEASE[10]           | 0               |                                                                               |
|              | 11         | U_NVM_RELEASE[11]           | 0               |                                                                               |
|              | 12         | U_NVM_RELEASE[12]           | 0               |                                                                               |
|              | 13         | U_NVM_RELEASE[13]           | 0               |                                                                               |
|              | 14         | U_NVM_RELEASE[14]           | 0               |                                                                               |
|              | 15         | U_NVM_RELEASE[15]           | 0               |                                                                               |
| DCR20 (0x14) | 0          | LOW_SET[0]                  | 0               | Long Open Window duration at 319 ms                                           |
|              | 1          | LOW_SET[1]                  | 0               |                                                                               |
|              | 2          | LOW_SET[2]                  | 0               |                                                                               |
|              | 3          | LOW_SET[3]                  | 0               |                                                                               |
|              | 4          | VS_SENSE_LEVEL_SEL[0]       | 1               | VS_SENSE threshold set at 5.85 V                                              |
|              | 5          | VS_SENSE_LEVEL_SEL[1]       | 1               |                                                                               |
|              | 6          | BOOST_CRK_ONLY              | 0               | Boost not working only below VS_SENSE_LEVEL_SEL threshold                     |
|              | 7          | BOOST_CRK_TO[0]             | 0               | No timeout on Boost when VS below VS_SENSE_LEVEL_SEL threshold                |
|              | 8          | BOOST_CRK_TO[1]             | 0               |                                                                               |
|              | 9          | BOOST_CRK_TO[2]             | 0               |                                                                               |
|              | 10         | WAKEUP_GO_TO_DEEP_SLEEP_INH | 1               | Go to DEEP-SLEEP inhibition if a wake-up flag is present                      |
|              | 11         | FBB_REG_LEVEL_SEL[0]        | 1               | FBB regulation level set at 9 V                                               |

| NVM Sector   | Bit Number | Field Name           | Configuration 1 | Comment                                               |
|--------------|------------|----------------------|-----------------|-------------------------------------------------------|
| DCR20 (0x14) | 12         | FBB_REG_LEVEL_SEL[1] | 1               | FBB regulation level set at 9 V                       |
|              | 13         | BYPASS_OFFSET_SEL    | 1               | BYPASS offset set at FBB_REG_LEVEL + 1.0 V = 10 V     |
|              | 14         | FBB_OK_SEL[0]        | 0               | FBB_OK threshold set at 7.5 V                         |
|              | 15         | FBB_OK_SEL[1]        | 1               |                                                       |
| DCR21 (0x15) | 0          | FBB_UV_LEVEL_SEL     | 0               | FBB_UV threshold set at 5.25 V                        |
|              | 1          | FBB_UV_EW_PD         | 0               | Power-down sequence not linked to FBB_UV_EW threshold |
|              | 2          | U_NVM_L[2]           | 0               |                                                       |
|              | 3          | U_NVM_L[3]           | 0               |                                                       |
|              | 4          | U_NVM_L[4]           | 0               |                                                       |
|              | 5          | U_NVM_L[5]           | 0               |                                                       |
|              | 6          | U_NVM_L[6]           | 0               |                                                       |
|              | 7          | U_NVM_L[7]           | 0               |                                                       |
|              | 8          | U_NVM_L[8]           | 0               |                                                       |
|              | 9          | U_NVM_L[9]           | 0               |                                                       |
|              | 10         | U_NVM_L[10]          | 0               |                                                       |
|              | 11         | U_NVM_L[11]          | 0               |                                                       |
|              | 12         | U_NVM_L[12]          | 0               |                                                       |
|              | 13         | U_NVM_L[13]          | 0               |                                                       |
|              | 14         | U_NVM_L[14]          | 0               |                                                       |
|              | 15         | U_NVM_L[15]          | 0               |                                                       |

## 9.4 Status register overview

**Table 70. Status register overview**

| bit             |      |      | 31                     | 30                         | 29                                 | 28                                 | 27                      | 26                     | 25                                          | 24                                          | Mode |
|-----------------|------|------|------------------------|----------------------------|------------------------------------|------------------------------------|-------------------------|------------------------|---------------------------------------------|---------------------------------------------|------|
| Global Status   |      |      | GSBN                   | RSTB                       | SPIE                               | FE2                                | FE1                     | DE                     | GW                                          | FS                                          | R    |
| Status Register |      |      |                        |                            |                                    |                                    |                         |                        |                                             |                                             |      |
| Addr.           |      | bits | 23                     | 22                         | 21                                 | 20                                 | 19                      | 18                     | 17                                          | 16                                          |      |
|                 |      |      | 15                     | 14                         | 13                                 | 12                                 | 11                      | 10                     | 9                                           | 8                                           |      |
|                 |      |      | 7                      | 6                          | 5                                  | 4                                  | CRC 3                   | CRC 2                  | CRC 1                                       | CRC 0                                       |      |
| 0x21            | DSR1 | MSB  | RES                    | BOOST_TIME<br>R_CNT_END    | FORCED_SLE<br>EP_WDFAIL            | BUCK3_OC                           | BUCK3_OV                | BUCK3_UV               | BUCK3_PG_TI<br>MEOUT                        | BUCK2_OC                                    | R    |
|                 |      |      | BUCK2_OV               | BUCK2_UV                   | BUCK2_PG_TI<br>MEOUT               | BUCK1_OC                           | BUCK1_OV                | BUCK1_UV               | BUCK1_PG_TI<br>MEOUT                        | LDO2_PG_TIM<br>EOUT                         |      |
|                 |      | LSB  | LDO2_UV                | LDO2_OV                    | LDO1_PG_TIM<br>EOUT                | LDO1_UV                            | CRC 3                   | CRC 2                  | CRC 1                                       | CRC 0                                       |      |
| 0x22            | DSR2 | MSB  | RES                    | OUTHS_OL                   | OUTHS_OC                           | BOOST_IN_LP                        | BYPASS_VDS<br>MON_ERROR | BOOST_VDSM<br>ON_ERROR | FBB_OV                                      | FBB_UV                                      | R    |
|                 |      |      | IRQ_ECHO_E<br>RROR     | FCCU_ENA_E<br>CHO_ERROR    | NFSO1_ECHO<br>_ERROR               | WD_ENA_ECH<br>O_ERROR              | NRST_ECHO_<br>ERROR     | VIO_UV                 | TSD_CL4                                     | TSD_CL3                                     |      |
|                 |      | LSB  | TSD_CL2                | TSD_CL1                    | TSD_CL0                            | TSD                                | CRC 3                   | CRC 2                  | CRC 1                                       | CRC 0                                       |      |
| 0x23            | DSR3 | MSB  | RES                    | LBIST_STOPP<br>ED          | BUCK3_INT_F<br>AIL                 | BUCK2_INT_F<br>AIL                 | BUCK1_INT_F<br>AIL      | LBIST_ERROR<br>_1      | LBIST_ERROR<br>_0                           | ABIST_ERRO<br>R                             | R    |
|                 |      |      | CURRENT_MI<br>SMATCH   | FORCED_SLE<br>EP_TSD       | FCCUFAIL                           | WDFAIL                             | INT_REG_UV              | INT_REG_OV             | NVM_COMP_<br>ERROR                          | NVM_CRC_ER<br>ROR                           |      |
|                 |      | LSB  | GNDLOSS                | OSC_ERROR                  | SPI_REG_CO<br>MP_ERROR             | FSM_COMP_E<br>RROR                 | CRC 3                   | CRC 2                  | CRC 1                                       | CRC 0                                       |      |
| 0x24            | DSR4 | MSB  | RES                    | SPI_ALL_WAK<br>EUP_DISABLE | SPI_CLK_CNT                        | SPI_CSN_TIM<br>EOUT                | SPI_CRC_ER<br>R         | SPI_SDI_STU<br>CK_HIGH | SPI_SDI_STU<br>CK_LOW                       | SPI_UNDEF_A<br>DD                           | R    |
|                 |      |      | SPI_STATUS_<br>WRT     | SPI_LBISTED                | FBB_OV_EW                          | FBB_UV_EW                          | VS_UV_EW                | CAN_SUP_LO<br>W        | TW_CL4                                      | TW_CL3                                      |      |
|                 |      | LSB  | TW_CL2                 | TW_CL1                     | TW_CL0                             | TW                                 | CRC 3                   | CRC 2                  | CRC 1                                       | CRC 0                                       |      |
| 0x25            | DSR5 | MSB  | RES                    | FP_READY                   | RES                                | BOOST_ENA_<br>STATUS               | BYPASS_STAT<br>US       | BUCK3_PG_O<br>K        | BUCK2_PG_O<br>K                             | BUCK1_PG_O<br>K                             | R    |
|                 |      |      | DEV_STATE_5            | DEV_STATE_4                | DEV_STATE_3                        | DEV_STATE_2                        | DEV_STATE_1             | DEV_STATE_0            | DEEP-<br>SLEEP_FROM<br>_DO_POWER_<br>DOWN_1 | DEEP-<br>SLEEP_FROM<br>_DO_POWER_<br>DOWN_0 |      |
|                 |      | LSB  | FORCED_SLE<br>EP_POWUP | FSM_TO_REC<br>2            | REC2_FROM_<br>DO_POWER_<br>CYCLE_1 | REC2_FROM_<br>DO_POWER_<br>CYCLE_0 | CRC 3                   | CRC 2                  | CRC 1                                       | CRC 0                                       |      |
| 0x26            | DSR6 | MSB  | RES                    | LP_READY                   | SWDBG_VIO                          | SWDBG_STAT<br>E                    | CAN_TO                  | CAN_RXD_RE<br>C        | CAN_PERM_R<br>EC                            | CAN_PERM_D<br>OM                            | R    |
|                 |      |      | CAN_TXD_DO<br>M        | FIN1_STATE                 | IGN_STATE                          | WU_STATE                           | IGN_WAKE                | WU_WAKE                | CAN_WAKE                                    | TIMER_WAKE                                  |      |
|                 |      | LSB  | IRQ_ECHO               | NRST_ECHO                  | IRQ_SENT                           | NFSO1_ECHO                         | CRC 3                   | CRC 2                  | CRC 1                                       | CRC 0                                       |      |
| 0x27            | DSR7 | MSB  | RES                    | VPOR                       | LDO1_PG_OK                         | LDO2_ENA_S<br>TATUS                | LDO2_PG_OK              | FCCU_ENA_E<br>CHO      | WD_ENA_ECH<br>O                             | WD_TIMER_S<br>TATE_1                        | R    |
|                 |      |      | WD_TIMER_S<br>TATE_0   | WDFAIL_CNT_<br>3           | WDFAIL_CNT_<br>2                   | WDFAIL_CNT_<br>1                   | WDFAIL_CNT_<br>0        | TSD_CNT_FAI<br>L_1     | TSD_CNT_FAI<br>L_0                          | POWUP_RET<br>RY_CNT_1                       |      |
|                 |      | LSB  | POWUP_RET<br>RY_CNT_0  | RES                        | NVM_PROG_<br>OK                    | NVM_PROG_<br>DONE                  | CRC 3                   | CRC 2                  | CRC 1                                       | CRC 0                                       |      |
| 0x28            | DSR8 | MSB  | RES                    | FCCU_LAST_<br>STABLE_12    | FCCU_LAST_<br>STABLE_11            | FCCU_LAST_<br>STABLE_10            | FCCU_LAST_<br>STABLE_9  | FCCU_LAST_<br>STABLE_8 | FCCU_LAST_<br>STABLE_7                      | FCCU_LAST_<br>STABLE_6                      | R    |
|                 |      |      | FCCU_LAST_<br>STABLE_5 | FCCU_LAST_<br>STABLE_4     | FCCU_LAST_<br>STABLE_3             | FCCU_LAST_<br>STABLE_2             | FCCU_LAST_<br>STABLE_1  | FCCU_LAST_<br>STABLE_0 | FORCED_SLE<br>EP_REGFAIL                    | REG_FAIL_CN<br>T_1                          |      |
|                 |      | LSB  | REG_FAIL_CN<br>T_0     | ABIST_BOOST<br>_IGNORED    | LBIST_COMPL<br>ETE                 | ABIST_COMP<br>LETE                 | CRC 3                   | CRC 2                  | CRC 1                                       | CRC 0                                       |      |



|      |       |     |            |            |            |            |            |            |            |            |   |
|------|-------|-----|------------|------------|------------|------------|------------|------------|------------|------------|---|
| 0x29 | DSR9  | MSB | RES        | RES        | RES        | RES        | RES        | RES        | RES        | RES        | R |
|      |       |     | RES        | RES        | TEMP_CL0_9 | TEMP_CL0_8 | TEMP_CL0_7 | TEMP_CL0_6 | TEMP_CL0_5 | TEMP_CL0_4 |   |
|      |       | LSB | TEMP_CL0_3 | TEMP_CL0_2 | TEMP_CL0_1 | TEMP_CL0_0 | CRC 3      | CRC 2      | CRC 1      | CRC 0      |   |
| 0x2A | DSR10 | MSB | RES        | RES        | RES        | RES        | RES        | RES        | RES        | RES        | R |
|      |       |     | RES        | RES        | TEMP_CL1_9 | TEMP_CL1_8 | TEMP_CL1_7 | TEMP_CL1_6 | TEMP_CL1_5 | TEMP_CL1_4 |   |
|      |       | LSB | TEMP_CL1_3 | TEMP_CL1_2 | TEMP_CL1_1 | TEMP_CL1_0 | CRC 3      | CRC 2      | CRC 1      | CRC 0      |   |
| 0x2B | DSR11 | MSB | RES        | RES        | RES        | RES        | RES        | RES        | RES        | RES        | R |
|      |       |     | RES        | RES        | TEMP_CL2_9 | TEMP_CL2_8 | TEMP_CL2_7 | TEMP_CL2_6 | TEMP_CL2_5 | TEMP_CL2_4 |   |
|      |       | LSB | TEMP_CL2_3 | TEMP_CL2_2 | TEMP_CL2_1 | TEMP_CL2_0 | CRC 3      | CRC 2      | CRC 1      | CRC 0      |   |

|      |       |     |            |            |            |            |            |            |            |            |   |
|------|-------|-----|------------|------------|------------|------------|------------|------------|------------|------------|---|
| 0x2C | DSR12 | MSB | RES        | RES        | RES        | RES        | RES        | RES        | RES        | RES        | R |
|      |       |     | RES        | RES        | TEMP_CL3_9 | TEMP_CL3_8 | TEMP_CL3_7 | TEMP_CL3_6 | TEMP_CL3_5 | TEMP_CL3_4 |   |
|      |       | LSB | TEMP_CL3_3 | TEMP_CL3_2 | TEMP_CL3_1 | TEMP_CL3_0 | CRC 3      | CRC 2      | CRC 1      | CRC 0      |   |
| 0x2D | DSR13 | MSB | RES        | RES        | RES        | RES        | RES        | RES        | RES        | RES        | R |
|      |       |     | RES        | RES        | TEMP_CL4_9 | TEMP_CL4_8 | TEMP_CL4_7 | TEMP_CL4_6 | TEMP_CL4_5 | TEMP_CL4_4 |   |
|      |       | LSB | TEMP_CL4_3 | TEMP_CL4_2 | TEMP_CL4_1 | TEMP_CL4_0 | CRC 3      | CRC 2      | CRC 1      | CRC 0      |   |
| 0x2E | DSR14 | MSB | RES        | RES        | RES        | RES        | RES        | RES        | RES        | RES        | R |
|      |       |     | RES        | RES        | VS_9       | VS_8       | VS_7       | VS_6       | VS_5       | VS_4       |   |
|      |       | LSB | VS_3       | VS_2       | VS_1       | VS_0       | CRC 3      | CRC 2      | CRC 1      | CRC 0      |   |

|      |       |     |                        |                        |                        |                          |                        |                                |                        |                        |   |
|------|-------|-----|------------------------|------------------------|------------------------|--------------------------|------------------------|--------------------------------|------------------------|------------------------|---|
| 0x2F | DSR15 | MSB | RES                    | RES                    | RES                    | RES                      | RES                    | RES                            | RES                    | RES                    | R |
|      |       |     | RES                    | RES                    | WU_9                   | WU_8                     | WU_7                   | WU_6                           | WU_5                   | WU_4                   |   |
|      |       | LSB | WU_3                   | WU_2                   | WU_1                   | WU_0                     | CRC 3                  | CRC 2                          | CRC 1                  | CRC 0                  |   |
| 0x30 | DSR16 | MSB | RES                    | RES                    | RES                    | RES                      | RES                    | RES                            | RES                    | RES                    | R |
|      |       |     | RES                    | RES                    | IGN_9                  | IGN_8                    | IGN_7                  | IGN_6                          | IGN_5                  | IGN_4                  |   |
|      |       | LSB | IGN_3                  | IGN_2                  | IGN_1                  | IGN_0                    | CRC 3                  | CRC 2                          | CRC 1                  | CRC 0                  |   |
| 0x31 | DSR17 | MSB | RES                    | RES                    | RES                    | RES                      | RES                    | RES                            | RES                    | RES                    | R |
|      |       |     | RES                    | RES                    | FBB_9                  | FBB_8                    | FBB_7                  | FBB_6                          | FBB_5                  | FBB_4                  |   |
|      |       | LSB | FBB_3                  | FBB_2                  | FBB_1                  | FBB_0                    | CRC 3                  | CRC 2                          | CRC 1                  | CRC 0                  |   |
| 0x32 | DSR18 | MSB | RES                    | RES                    | RES                    | BUCK2_FBLO<br>SS         | BUCK1_FBLO<br>SS       | NVM_COMPA<br>RE_ENA_STAT<br>US | WD_TIME_ST<br>ATUS_3   | WD_TIME_ST<br>ATUS_2   | R |
|      |       |     | WD_TIME_ST<br>ATUS_1   | WD_TIME_ST<br>ATUS_0   | VBUCK3_ENA<br>_STATUS  | VBUCK2_ENA<br>_STATUS    | VBUCK1_ENA<br>_STATUS  | LDO1_ENA_S<br>TATUS            | OUTHS_ENA_<br>STATUS   | LOW_STATUS             |   |
|      |       | LSB | BOOST_ENA_<br>STATUS   | FCCU_ENA_S<br>TATUS    | CAN_ACT_ST<br>ATUS     | CAN_AUTO_BI<br>AS_STATUS | CRC 3                  | CRC 2                          | CRC 1                  | CRC 0                  |   |
| 0x33 | DSR19 | MSB | RES                    | LDT_TIMER_V<br>ALUE_23 | LDT_TIMER_V<br>ALUE_22 | LDT_TIMER_V<br>ALUE_21   | LDT_TIMER_V<br>ALUE_20 | LDT_TIMER_V<br>ALUE_19         | LDT_TIMER_V<br>ALUE_18 | LDT_TIMER_V<br>ALUE_17 | R |
|      |       |     | LDT_TIMER_V<br>ALUE_16 | LDT_TIMER_V<br>ALUE_15 | LDT_TIMER_V<br>ALUE_14 | LDT_TIMER_V<br>ALUE_13   | LDT_TIMER_V<br>ALUE_12 | LDT_TIMER_V<br>ALUE_11         | LDT_TIMER_V<br>ALUE_10 | LDT_TIMER_V<br>ALUE_9  |   |
|      |       | LSB | LDT_TIMER_V<br>ALUE_8  | LDT_TIMER_V<br>ALUE_7  | LDT_TIMER_V<br>ALUE_6  | LDT_TIMER_V<br>ALUE_5    | CRC 3                  | CRC 2                          | CRC 1                  | CRC 0                  |   |
| 0x34 | DSR20 | MSB | RES                    | LDT_TIMER_V<br>ALUE_4  | LDT_TIMER_V<br>ALUE_3  | LDT_TIMER_V<br>ALUE_2    | LDT_TIMER_V<br>ALUE_1  | LDT_TIMER_V<br>ALUE_0          | LDT_WAKE               | LDT_RUNNIN<br>G        | R |
|      |       |     | RES                    | RES                    | RES                    | RES                      | RES                    | RES                            | RES                    | RES                    |   |
|      |       | LSB | RES                    | RES                    | RES                    | RES                      | CRC 3                  | CRC 2                          | CRC 1                  | CRC 0                  |   |

## 9.5 Control registers

The first row of each of the following DCRx tables lists the register default values after power-up, as follows:

- 0 (R/W): Read/Write register with a default value of "0".
- 1 (R/W): Read/Write register with a default value of "1".
- - (R0): Reserved bits that always read as "0" and shall not be used.
- - (R): Read-only register

**Table 71. DCR1 (0x01) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19   | Bit 18                                      | Bit 17                             | Bit 16                             |
|----------|----------|----------|----------|----------|---------------------------------------------|------------------------------------|------------------------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | 0 (R/W)                                     | 0 (R/W)                            | 0 (R/W)                            |
| RES      | RES      | RES      | RES      | RES      | WD_NRST_MASK                                | WD_TIME_3                          | WD_TIME_2                          |
| Reserved | Reserved | Reserved | Reserved | Reserved | NRST pulses masked in case of watchdog fail | Watchdog trigger time <sub>3</sub> | Watchdog trigger time <sub>2</sub> |

**Table 72. DCR1 (0x01) MSB description**

| Bit | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES          | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 22  | RES          | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 21  | RES          | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 20  | RES          | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19  | RES          | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 18  | WD_NRST_MASK | NRST pulses mask in case of watchdog fail:<br>1 : NRST mask is enabled<br>0 : NRST mask is disabled<br>protected by SPI_PROTECT_ACCESS bit                                                                                                                                                                                                                                                                                 |
| 17  | WD_TIME_3    | Watchdog trigger time<br>0000: Window 1<br>0001: Window 2 (default window once WD kick)<br>0010: Window 3<br>0011: Window 4<br>0100: Window 5<br>0101: Window 6<br>0110: Window 7<br>0111: Window 8<br>1000: Window 9<br>1001-1110: Window 10 → 5-50 ms window<br>1111: Stop watchdog<br>The modified WD trigger time is valid after the next WD trig (CSN transition low-to-high) protected by the SPI_PROTECT_ACCESS bit |
| 16  | WD_TIME_2    |                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 73. DCR1 (0x01)**

| Bit 15    | Bit 14    | Bit 13     | Bit 12     | Bit 11     | Bit 10   | Bit 9    | Bit 8         |
|-----------|-----------|------------|------------|------------|----------|----------|---------------|
| 0 (R/W)   | 1 (R/W)   | 0 (R/W)    | 0 (R/W)    | 0 (R/W)    | 0 (R/W)  | 0 (R/W)  | 0 (R/W)       |
| WD_TIME_1 | WD_TIME_0 | VBUCK3_ENA | VBUCK2_ENA | VBUCK1_ENA | LDO1_ENA | LDO2_ENA | LOW_POWER_SET |

| Bit 15                  | Bit 14                  | Bit 13           | Bit 12           | Bit 11           | Bit 10          | Bit 9           | Bit 8              |
|-------------------------|-------------------------|------------------|------------------|------------------|-----------------|-----------------|--------------------|
| Watchdog trigger time 1 | Watchdog trigger time 0 | Buck3 enable bit | Buck2 enable bit | Buck1 enable bit | LDO1 enable bit | LDO2 enable bit | Set LOW-POWER mode |

**Table 74. DCR1 (0x01) description**

| Bit | Name          | Description                                                                                                                                                                                                                                                                                           |
|-----|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | WD_TIME_1     |                                                                                                                                                                                                                                                                                                       |
| 14  | WD_TIME_0     |                                                                                                                                                                                                                                                                                                       |
| 13  | VBUCK3_ENA    | Buck3 enable bit (default value link to start-up sequence setting)<br>1: Enable<br>Protected by SPI_PROTECT_ACCESS bit<br>0: Disabled<br>Note that, after the first power-up, it is necessary to align the live bit associated in DSR18 (VBUCK3_ENA_STATUS) with the current value associated in DCR1 |
| 12  | VBUCK2_ENA    | Buck2 enable bit (default value link to start-up sequence setting)<br>1: Enable<br>Protected by SPI_PROTECT_ACCESS bit<br>0: Disabled<br>Note that, after the first power-up, it is necessary to align the live bit associated in DSR18 (VBUCK2_ENA_STATUS) with the current value associated in DCR1 |
| 11  | VBUCK1_ENA    | Buck1 enable bit (default value link to start-up sequence setting)<br>1: Enable<br>Protected by SPI_PROTECT_ACCESS bit<br>0: Disabled<br>Note that, after the first power-up, it is necessary to align the live bit associated in DSR18 (VBUCK1_ENA_STATUS) with the current value associated in DCR1 |
| 10  | LDO1_ENA      | LDO1 enable bit (default value link to start up sequence setting)<br>1: Enable<br>0: Disabled<br>Protected by SPI_PROTECT_ACCESS bit<br>Note that, after the first power-up, it is necessary to align the live bit associated in DSR18 (LDO1_ENA_STATUS) with the current value associated in DCR1    |
| 9   | LDO2_ENA      | LDO2 enable bit (default value link to start up sequence setting)<br>1: Enable<br>0: Disabled<br>Protected by SPI_PROTECT_ACCESS bit<br>Note that, after the first power-up, it is necessary to align the live bit associated in DSR18 (LDO2_ENA_STATUS) with the current value associated in DCR1    |
| 8   | LOW_POWER_SET | Set LOW-POWER mode<br>1: Go to LOW-POWER<br>0: Back to FULL-POWER<br>Protected by SPI_PROTECT_ACCESS bit                                                                                                                                                                                              |

**Table 75. DCR1 (0x01) LSB**

| Bit 7   | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1   | Bit 0   |
|---------|---------|---------|---------|---------|---------|---------|---------|
| 1 (R/W) | 0 (R/W) | 0 (R/W) | 0 (R/W) | 0 (R/W) | 0 (R/W) | 0 (R/W) | 0 (R/W) |

| Bit 7                                 | Bit 6                   | Bit 5                | Bit 4           | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------------------------|-------------------------|----------------------|-----------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| WD_LP_ENA                             | DO_POWER_DOWN           | U-NVM_PROG           | DO_POWER_CYCLE  | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Watchdog in LOW-POWER mode enable bit | Power-down sequence bit | User NVM program bit | Power cycle bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 76. DCR1 (0x01) LSB description**

| Bit | Name           | Description                                                                                                                                                                                                 |
|-----|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | WD_LP_ENA      | 1: Watchdog is enabled in LOW-POWER mode (default)<br>0: Watchdog is disabled in LOW-POWER mode<br>Is taken into account as soon the LOW_POWER_SET bit is set to "1"<br>Protected by SPI_PROTECT_ACCESS bit |
| 6   | DO_POWER_DOWN  | Bit is reset after entry in DEEP-SLEEP state<br>This bit is automatically cleared and always read low<br>1: Execute power-down sequence<br>0: No action (default)<br>Protected by SPI_PROTECT_ACCESS bit    |
| 5   | U-NVM_PROG     | 1: start user NVM program<br>0: No action<br>Protected by SPI_PROTECT_ACCESS bit                                                                                                                            |
| 4   | DO_POWER_CYCLE | 1: execute power down sequence followed by power up sequence (power cycle)<br>0: no action<br>This bit is automatically cleared and always read low<br>Protected by SPI_PROTECT_ACCESS bit                  |
| 3   | CRC 3          |                                                                                                                                                                                                             |
| 2   | CRC 2          |                                                                                                                                                                                                             |
| 1   | CRC 1          |                                                                                                                                                                                                             |
| 0   | CRC 0          |                                                                                                                                                                                                             |

**Table 77. DCR2 (0x02) MSB**

| Bit 23   | Bit 22   | Bit 21          | Bit 20                   | Bit 19                  | Bit 18   | Bit 17              | Bit 16              |
|----------|----------|-----------------|--------------------------|-------------------------|----------|---------------------|---------------------|
| -(R0)    | -(R0)    | 1 (R/W)         | 0 (R/W)                  | 0 (R/W)                 | -(R0)    | 0 (R/W)             | 0 (R/W)             |
| RES      | RES      | NFSO_ASSERT_LOW | LBIST                    | ABIST                   | RES      | FCCU_COUNTER_12     | FCCU_COUNTER_11     |
| Reserved | Reserved | NFSO low bit    | Logical BIST request bit | Analog BIST request bit | Reserved | FCCU counter bit 12 | FCCU counter bit 11 |

**Table 78. DCR2 (0x02) MSB description**

| Bit | Name            | Description                                                                   |
|-----|-----------------|-------------------------------------------------------------------------------|
| 23  | RES             | Reserved                                                                      |
| 22  | RES             | Reserved                                                                      |
| 21  | NFSO_ASSERT_LOW | Force NFSO pin low<br>Protected by SPI_PROTECT_ACCESS bit                     |
| 20  | LBIST           | Logical BIST request<br>This bit is automatically cleared and always read low |

| Bit | Name            | Description                                                                                                         |
|-----|-----------------|---------------------------------------------------------------------------------------------------------------------|
|     |                 | Protected by SPI_PROTECT_ACCESS bit                                                                                 |
| 19  | ABIST           | Analog BIST request<br>This bit is automatically cleared and always read low<br>Protected by SPI_PROTECT_ACCESS bit |
| 18  | RES             | Reserved                                                                                                            |
| 17  | FCCU_COUNTER_12 | FCCU counter value selection<br>Protected by SPI_PROTECT_ACCESS bit                                                 |
| 16  | FCCU_COUNTER_11 |                                                                                                                     |

**Table 79. DCR2 (0x02)**

| Bit 15              | Bit 14             | Bit 13             | Bit 12             | Bit 11             | Bit 10             | Bit 9              | Bit 8              |
|---------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| 0 (R/W)             | 0 (R/W)            | 0 (R/W)            | 0 (R/W)            | 0 (R/W)            | 0 (R/W)            | 0 (R/W)            | 0 (R/W)            |
| FCCU_COUNTER_10     | FCCU_COUNTER_9     | FCCU_COUNTER_8     | FCCU_COUNTER_7     | FCCU_COUNTER_6     | FCCU_COUNTER_5     | FCCU_COUNTER_4     | FCCU_COUNTER_3     |
| FCCU counter bit 10 | FCCU counter bit 9 | FCCU counter bit 8 | FCCU counter bit 7 | FCCU counter bit 6 | FCCU counter bit 5 | FCCU counter bit 4 | FCCU counter bit 3 |

**Table 80. DCR2 (0x02) description**

| Bit | Name            | Description |
|-----|-----------------|-------------|
| 15  | FCCU_COUNTER_10 |             |
| 14  | FCCU_COUNTER_9  |             |
| 13  | FCCU_COUNTER_8  |             |
| 12  | FCCU_COUNTER_7  |             |
| 11  | FCCU_COUNTER_6  |             |
| 10  | FCCU_COUNTER_5  |             |
| 9   | FCCU_COUNTER_4  |             |
| 8   | FCCU_COUNTER_3  |             |

**Table 81. DCR2 (0x02) LSB**

| Bit 7              | Bit 6              | Bit 5              | Bit 4                   | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|--------------------|--------------------|--------------------|-------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R/W)            | 0 (R/W)            | 0 (R/W)            | 0 (R/W)                 | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          |
| FCCU_COUNTER_2     | FCCU_COUNTER_1     | FCCU_COUNTER_0     | FCCU_ENA                | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| FCCU counter bit 2 | FCCU counter bit 1 | FCCU counter bit 0 | FCCU monitor enable bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 82. DCR2 (0x02) LSB description**

| Bit | Name           | Description                                                                                                                          |
|-----|----------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 7   | FCCU_COUNTER_2 |                                                                                                                                      |
| 6   | FCCU_COUNTER_1 |                                                                                                                                      |
| 5   | FCCU_COUNTER_0 |                                                                                                                                      |
| 4   | FCCU_ENA       | Enable FCCU monitor<br>1: Enabled<br>0: Disabled (pull-up/-down defined by FCCU_STATIC_ERROR)<br>Protected by SPI_PROTECT_ACCESS bit |
| 3   | CRC 3          |                                                                                                                                      |

| Bit | Name  | Description |
|-----|-------|-------------|
| 2   | CRC 2 |             |
| 1   | CRC 1 |             |
| 0   | CRC 0 |             |

**Table 83. DCR3 (0x03) MSB**

| Bit 23   | Bit 22   | Bit 21                  | Bit 20                  | Bit 19                  | Bit 18                | Bit 17   | Bit 16                |
|----------|----------|-------------------------|-------------------------|-------------------------|-----------------------|----------|-----------------------|
| -(R0)    | -(R0)    | 0 (R/W)                 | 0 (R/W)                 | 0 (R/W)                 | 0 (R/W)               | -(R0)    | 0 (R/W)               |
| RES      | RES      | BUCK3_SPREAD_ENA        | BUCK2_SPREAD_ENA        | BUCK1_SPREAD_ENA        | CLR_WDFAIL_CNT        | RES      | BUCK3_FTUNE_2         |
| Reserved | Reserved | Buck3 spread enable bit | Buck2 spread enable bit | Buck1 spread enable bit | Clear WDFAIL_CNT bits | reserved | Buck3 fine-tune bit 2 |

**Table 84. DCR3 (0x03) MSB description**

| Bit | Name             | Description                                                       |
|-----|------------------|-------------------------------------------------------------------|
| 23  | RES              | Reserved                                                          |
| 22  | RES              | Reserved                                                          |
| 21  | BUCK3_SPREAD_ENA | Frequency spread selection<br>1: Enabled<br>0: Disabled (default) |
| 20  | BUCK2_SPREAD_ENA | Frequency spread selection<br>1: Enabled<br>0: Disabled (default) |
| 19  | BUCK1_SPREAD_ENA | Frequency spread selection<br>1: Enabled<br>0: Disabled (default) |
| 18  | CLR_WDFAIL_CNT   | Clear WDFAIL_CNT to 0<br>This bit is always read low              |
| 17  | RES              | Reserved                                                          |
| 16  | BUCK3_FTUNE_2    |                                                                   |

**Table 85. DCR3 (0x03)**

| Bit 15                | Bit 14                | Bit 13            | Bit 12                                        | Bit 11                                        | Bit 10                                        | Bit 9                                         | Bit 8                                          |
|-----------------------|-----------------------|-------------------|-----------------------------------------------|-----------------------------------------------|-----------------------------------------------|-----------------------------------------------|------------------------------------------------|
| 0 (R/W)               | 0 (R/W)               | 0 (R/W)           | 0 (R/W)                                       | 0 (R/W)                                       | 0 (R/W)                                       | 0 (R/W)                                       | 0 (R/W)                                        |
| BUCK3_FTUNE_1         | BUCK3_FTUNE_0         | BOOST_OFF         | FBB_OV_EW_TH_3                                | FBB_OV_EW_TH_2                                | FBB_OV_EW_TH_1                                | FBB_OV_EW_TH_0                                | FBB_UV_EW_TH_3                                 |
| Buck3 fine-tune bit 1 | Buck3 fine-tune bit 0 | BOOST disable bit | FBB overvoltage early warning threshold bit 3 | FBB overvoltage early warning threshold bit 2 | FBB overvoltage early warning threshold bit 1 | FBB overvoltage early warning threshold bit 0 | FBB undervoltage early warning threshold bit 3 |

**Table 86. DCR3 (0x03) description**

| Bit | Name          | Description                                                                      |
|-----|---------------|----------------------------------------------------------------------------------|
| 15  | BUCK3_FTUNE_1 |                                                                                  |
| 14  | BUCK3_FTUNE_0 | 11x: 0.99 V<br>101: 1.0 V<br>100: 1.01 V<br>000: 1.02 V (default)<br>001: 1.03 V |

| Bit | Name           | Description                                                                                                                                                                                                                                                       |
|-----|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                | 010: 1.04 V<br>011: 1.05 V                                                                                                                                                                                                                                        |
| 13  | BOOST_OFF      | Boost disable<br>1: Boost is disabled<br>0: Boost feature defined by BOOST_DIS U-NVM bit (default)                                                                                                                                                                |
| 12  | FBB_OV_EW_TH_3 | FBB overvoltage early warning threshold<br>At FBB > FBB_OV_EW_TH, an interrupt is generated on the IRQ pin and the status bit FBB_OV_EW in SR4 is set (in active mode)<br>0000: (default) feature deactivated<br>0001: 24 V<br>... (1 V step)<br>1111: 38 V       |
| 11  | FBB_OV_EW_TH_2 |                                                                                                                                                                                                                                                                   |
| 10  | FBB_OV_EW_TH_1 |                                                                                                                                                                                                                                                                   |
| 9   | FBB_OV_EW_TH_0 |                                                                                                                                                                                                                                                                   |
| 8   | FBB_UV_EW_TH_3 | FBB undervoltage early warning threshold.<br>At FBB < FBB_UV_EW_TH, an interrupt is generated on the IRQ pin and the status bit FBB_UV_EW in SR4 is set (in active mode)<br>0000: (default) feature deactivated<br>0001: 5 V<br>... (0.24 V step)<br>1111: 8.36 V |

**Table 87. DCR3 (0x03) LSB**

| Bit 7                                          | Bit 6                                          | Bit 5                                          | Bit 4                  | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|------------------------------------------------|------------------------------------------------|------------------------------------------------|------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R/W)                                        | 0 (R/W)                                        | 0 (R/W)                                        | 0 (R/W)                | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          |
| FBB_UV_EW_TH_2                                 | FBB_UV_EW_TH_1                                 | FBB_UV_EW_TH_0                                 | SPI_PROTECT_ACCESS     | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| FBB undervoltage early warning threshold bit 2 | FBB undervoltage early warning threshold bit 1 | FBB undervoltage early warning threshold bit 0 | SPI protect access bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 88. DCR3 (0x03) LSB description**

| Bit | Name               | Description                                                                                                                                                                                                                              |
|-----|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | FBB_UV_EW_TH_2     |                                                                                                                                                                                                                                          |
| 6   | FBB_UV_EW_TH_1     |                                                                                                                                                                                                                                          |
| 5   | FBB_UV_EW_TH_0     |                                                                                                                                                                                                                                          |
| 4   | SPI_PROTECT_ACCESS | 1: Allows write access to protected SPI bits on next write SPI frame<br>This bit is automatically cleared on the next write SPI frame but can be read high before the next write SPI frame<br>0: Access to protected SPI bits is blocked |
| 3   | CRC 3              |                                                                                                                                                                                                                                          |
| 2   | CRC 2              |                                                                                                                                                                                                                                          |
| 1   | CRC 1              |                                                                                                                                                                                                                                          |
| 0   | CRC 0              |                                                                                                                                                                                                                                          |

**Table 89. DCR4 (0x04) MSB**

| Bit 23   | Bit 22                        | Bit 21                        | Bit 20                        | Bit 19                  | Bit 18                                                    | Bit 17                                                    | Bit 16                                                    |
|----------|-------------------------------|-------------------------------|-------------------------------|-------------------------|-----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|
| - (R0)   | 1 (R/W)                       | 0 (R/W)                       | 0 (R/W)                       | 0 (R/W)                 | 0 (R/W)                                                   | 0 (R/W)                                                   | 0 (R/W)                                                   |
| RES      | BOOST_DSMON_TH_2              | BOOST_DSMON_TH_1              | BOOST_DSMON_TH_0              | SWDBG_EXIT              | VS_UV_EW_TH_4                                             | VS_UV_EW_TH_3                                             | VS_UV_EW_TH_2                                             |
| Reserved | BOOST monitor threshold bit 2 | BOOST monitor threshold bit 1 | BOOST monitor threshold bit 0 | Software debug exit bit | V <sub>S</sub> undervoltage early warning threshold bit 4 | V <sub>S</sub> undervoltage early warning threshold bit 3 | V <sub>S</sub> undervoltage early warning threshold bit 2 |

**Table 90. DCR4 (0x04) MSB description**

| Bit | Name             | Description                                                                                                                                                                                                                                                                           |
|-----|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES              | Reserved                                                                                                                                                                                                                                                                              |
| 22  | BOOST_DSMON_TH_2 | Control BOOST_VDMON_TH :<br>000 : 0.25 V<br>001 : 0.45 V<br>010 : 0.65 V<br>011 : 0.85 V<br>100 : 1.1 V<br>101 : 1.3 V<br>110 : 1.5 V<br>111 : 1.7 V                                                                                                                                  |
| 21  | BOOST_DSMON_TH_1 |                                                                                                                                                                                                                                                                                       |
| 20  | BOOST_DSMON_TH_0 |                                                                                                                                                                                                                                                                                       |
| 19  | SWDBG_EXIT       | This bit is active in software debug mode<br>1: Forces the device to exit software debug mode<br>Watchdog restarts with a LOW<br>0: No action (default)                                                                                                                               |
| 18  | VS_UV_EW_TH_4    | V <sub>S</sub> undervoltage early warning threshold<br>At V <sub>S</sub> < VS_EW_TH, an interrupt is generated on the IRQ pin and the status bit VS_UV_EW in SR4 is set (in active mode)<br>00000: Feature deactivated (default)<br>00001: 2.6 V<br>... (0.24 V step)<br>11111: 9.8 V |
| 17  | VS_UV_EW_TH_3    |                                                                                                                                                                                                                                                                                       |
| 16  | VS_UV_EW_TH_2    |                                                                                                                                                                                                                                                                                       |

**Table 91. DCR4 (0x04)**

| Bit 15                                                    | Bit 14                                                    | Bit 13            | Bit 12                | Bit 11                    | Bit 10                    | Bit 9                          | Bit 8                          |
|-----------------------------------------------------------|-----------------------------------------------------------|-------------------|-----------------------|---------------------------|---------------------------|--------------------------------|--------------------------------|
| 0 (R/W)                                                   | 0 (R/W)                                                   | 0 (R/W)           | 0 (R/W)               | 0 (R/W)                   | 0 (R/W)                   | 1 (R/W)                        | 0 (R/W)                        |
| VS_UV_EW_TH_1                                             | VS_UV_EW_TH_0                                             | FCCU_PROTOCOL     | FCCU_STATIC_ERROR     | OUTHS_1                   | OUTHS_0                   | BYPASS_DSMON_TH_2              | BYPASS_DSMON_TH_1              |
| V <sub>S</sub> undervoltage early warning threshold bit 1 | V <sub>S</sub> undervoltage early warning threshold bit 0 | FCCU protocol bit | FCCU static error bit | OUTHS configuration bit 1 | OUTHS configuration bit 0 | BYPASS monitor threshold bit 2 | BYPASS monitor threshold bit 1 |

**Table 92. DCR4 (0x04) description**

| Bit | Name              | Description                                                                                                                                                                         |
|-----|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | VS_UV_EW_TH_1     |                                                                                                                                                                                     |
| 14  | VS_UV_EW_TH_0     |                                                                                                                                                                                     |
| 13  | FCCU_PROTOCOL     | 1: Toggle (pull-up/-down defined by FCCU_STATIC_ERROR)<br>0: Static (error state defined by FCCU_STATIC_ERROR)                                                                      |
| 12  | FCCU_STATIC_ERROR | 1: Error when FIN1 = 1 (→ pull-up active)<br>0: Error when FIN1 = 0 (→ pull-down active)                                                                                            |
| 11  | OUTHS_1           | OUTHS configuration bits<br>00: Off (default)<br>01: On<br>1x: Timer 1                                                                                                              |
| 10  | OUTHS_0           |                                                                                                                                                                                     |
| 9   | BYPASS_DSMON_TH_2 | Configuration of Bypass Drain Source monitoring threshold :<br>000: 125 mV<br>001: 175 mV<br>010: 225 mV<br>011: 275 mV<br>100: 325 mV<br>101: 375 mV<br>110: 425 mV<br>111: 475 mV |
| 8   | BYPASS_DSMON_TH_1 |                                                                                                                                                                                     |

**Table 93. DCR4 (0x04) LSB**

| Bit 7                          | Bit 6                   | Bit 5                           | Bit 4                | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|--------------------------------|-------------------------|---------------------------------|----------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R/W)                        | 0 (R/W)                 | 0 (R/W)                         | 0 (R/W)              | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          |
| BYPASS_DSMON_TH_0              | CLR_REG_FAIL_CNT        | KILL_SWDBG_TIMEOUT              | WD_TRIG              | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| BYPASS monitor threshold bit 0 | Clear REG_FAIL_CNT bits | Kill software debug timeout bit | Watchdog trigger bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 94. DCR4 (0x04) LSB description**

| Bit | Name               | Description                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | BYPASS_DSMON_TH_0  |                                                                                                                                                                                                                                                                                                                                                                                                 |
| 6   | CLR_REG_FAIL_CNT   | Clear REG_FAIL_CNT to 0<br>This bit is always read low                                                                                                                                                                                                                                                                                                                                          |
| 5   | KILL_SWDBG_TIMEOUT | Kill the 10 s timeout that runs when the SWDBG pin is shorted to VIO at start-up. With this bit at '1', the timeout is killed → the state machine exits the SWDBG state and transitions to REC-1 and the watchdog is started with a LOW. SWDBG state is then NOT entered. This feature allows the MCU to take control in case of hardware fault without waiting for the 10 s timeout to elapse. |
| 4   | WD_TRIG            | Watchdog trig alternatively with 0 and 1. First trig has to be with 1<br>Watchdog trig alternatively with 0 and 1                                                                                                                                                                                                                                                                               |
| 3   | CRC 3              |                                                                                                                                                                                                                                                                                                                                                                                                 |
| 2   | CRC 2              |                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1   | CRC 1              |                                                                                                                                                                                                                                                                                                                                                                                                 |

| Bit | Name  | Description |
|-----|-------|-------------|
| 0   | CRC 0 |             |

**Table 95. DCR5 (0x05) MSB**

| Bit 23   | Bit 22                             | Bit 21                                  | Bit 20                      | Bit 19               | Bit 18               | Bit 17               | Bit 16               |
|----------|------------------------------------|-----------------------------------------|-----------------------------|----------------------|----------------------|----------------------|----------------------|
| -(R0)    | 0 (R/W)                            | 0 (R/W)                                 | 0 (R/W)                     | 0 (R/W)              | 0 (R/W)              | 0 (R/W)              | 0 (R/W)              |
| RES      | CLR_REC2_FROM_DO_POWER_CYCLE       | CLR_DEEP_SLEEP_FROM_DO_POWER_DOWN       | CLR_POWUP_RETRY_COUNT       | T1_ENA_2             | T1_ENA_1             | T1_ENA_0             | T1_PER_2             |
| Reserved | Clear REC2_FROM_DO_POWER_CYCLE bit | Clear DEEP_SLEEP_FROM_DO_POWER_DOWN bit | Clear POWUP_RETRY_COUNT bit | Timer 1 enable bit 2 | Timer 1 enable bit 1 | Timer 1 enable bit 0 | Timer 1 period bit 2 |

**Table 96. DCR5 (0x05) MSB description**

| Bit | Name                              | Description                                                                                                                                                                                                          |
|-----|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES                               | Reserved                                                                                                                                                                                                             |
| 22  | CLR_REC2_FROM_DO_POWER_CYCLE      | Clear REC2_FROM_DO_POWER_CYCLE to 0<br>This bit is always read low                                                                                                                                                   |
| 21  | CLR_DEEP_SLEEP_FROM_DO_POWER_DOWN | Clear DEEP-SLEEP_FROM_DO_POWER_DOWN to 0<br>This bit is always read low                                                                                                                                              |
| 20  | CLR_POWUP_RETRY_COUNT             | Clear POWUP_RETRY_CNT to 0<br>This bit is always read low                                                                                                                                                            |
| 19  | T1_ENA_2                          | Configuration of timer 1 ON duration<br>000: t <sub>ON1</sub> - 0.1 ms (default)<br>001: t <sub>ON2</sub> - 0.3 ms<br>010: t <sub>ON3</sub> - 1 ms<br>011: t <sub>ON4</sub> - 10 ms<br>1xx: t <sub>ON5</sub> - 20 ms |
| 18  | T1_ENA_1                          |                                                                                                                                                                                                                      |
| 17  | T1_ENA_0                          |                                                                                                                                                                                                                      |
| 16  | T1_PER_2                          | Configuration of timer 1 period<br>000: T1 - 10 ms (default)<br>001: T2 - 20 ms<br>010: T3 - 50 ms<br>011: T4 - 100 ms<br>100: T5 - 200 ms<br>101: T6 - 500 ms<br>110: T7 - 1000 ms<br>111: T8 - 2000 ms             |

**Table 97. DCR5 (0x05)**

| Bit 15               | Bit 14               | Bit 13                   | Bit 12                | Bit 11                       | Bit 10         | Bit 9                               | Bit 8                     |
|----------------------|----------------------|--------------------------|-----------------------|------------------------------|----------------|-------------------------------------|---------------------------|
| 0 (R/W)              | 0 (R/W)              | 0 (R/W)                  | 0 (R/W)               | 0 (R/W)                      | 1 (R/W)        | 0 (R/W)                             | 0 (R/W)                   |
| T1_PER_1             | T1_PER_0             | TIMER_WAKE_ENA           | IGN_CONFIG            | IGN_FILT                     | IGN_ENA        | IGN_PU                              | WU_CONFIG                 |
| Timer 1 period bit 1 | Timer 1 period bit 0 | Timer wake-up enable bit | IGN configuration bit | IGN filter configuration bit | IGN enable bit | IGN pull-up/-down configuration bit | Wake-up configuration bit |

**Table 98. DCR5 (0x05) description**

| Bit | Name           | Description                                                                                                                                                                                                              |
|-----|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | T1_PER_1       |                                                                                                                                                                                                                          |
| 14  | T1_PER_0       |                                                                                                                                                                                                                          |
| 13  | TIMER_WAKE_ENA | Timer wake-up enable<br>1: Wake after timer period<br>0: No timer wake-up capability                                                                                                                                     |
| 12  | IGN_CONFIG     | Configuration of input pin IGN input configured as wake-up input<br>1: IGN voltage measurement enabled<br>0: IGN configured as wake-up input (default)                                                                   |
| 11  | IGN_FILT       | IGN filter configuration bits<br>1: IGN input monitored in cyclic mode with Timer1 (filter time: tIGN_cyc, blanking time 80% of timer ON time)<br>0: IGN input monitored in static mode (filter time tGN_stat) (default) |
| 10  | IGN_ENA        | IGN input enable:<br>1: Device wake-up capability by IGN pin enabled (default)<br>0: No wake-up possible by IGN pin                                                                                                      |
| 9   | IGN_PU         | IGN Pull-up/-down configuration<br>1: PULL-UP<br>0: PULL-DOWN                                                                                                                                                            |
| 8   | WU_CONFIG      | Configuration of input pin WU input configured as wake-up input<br>1: WU voltage measurement enabled<br>0: WU configured as wake-up input (default)                                                                      |

**Table 99. DCR5 (0x05) LSB**

| Bit 7              | Bit 6                                   | Bit 5                            | Bit 4            | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|--------------------|-----------------------------------------|----------------------------------|------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 1 (R/W)            | 0 (R/W)                                 | 0 (R/W)                          | 0 (R/W)          | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          |
| WU_ENA             | WU_PU                                   | WU_FILT                          | TIMER_ENA        | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Wake-up enable bit | Wake-up pull-up/-down configuration bit | Wake-up filter configuration bit | Timer enable bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 100. DCR5 (0x05) LSB description**

| Bit | Name      | Description                                                                                                                                                                                                          |
|-----|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | WU_ENA    | WU input enable:<br>1: Device wake-up capability by WU pin enabled (default)<br>0: No wake-up possible by WU pin                                                                                                     |
| 6   | WU_PU     | WU pull-up/-down configuration<br>1: PULL-UP<br>0: PULL-DOWN                                                                                                                                                         |
| 5   | WU_FILT   | WU filter configuration bits<br>1: WU input monitored in cyclic mode with Timer1 (filter time: tWU_cyc, blanking time 80% of timer ON time)<br>0: WU input monitored in static mode (filter time tWU_stat) (default) |
| 4   | TIMER_ENA | Enables timer counting                                                                                                                                                                                               |

| Bit | Name  | Description                             |
|-----|-------|-----------------------------------------|
|     |       | 1: Allow counting<br>0: Counter stopped |
| 3   | CRC 3 |                                         |
| 2   | CRC 2 |                                         |
| 1   | CRC 1 |                                         |
| 0   | CRC 0 |                                         |

**Table 101. DCR6 (0x06) MSB**

| Bit 23   | Bit 22                              | Bit 21                               | Bit 20                      | Bit 19                   | Bit 18                              | Bit 17                               | Bit 16                      |
|----------|-------------------------------------|--------------------------------------|-----------------------------|--------------------------|-------------------------------------|--------------------------------------|-----------------------------|
| -(R0)    | 0 (R/W)                             | 0 (R/W)                              | 0 (R/W)                     | 0 (R/W)                  | 0 (R/W)                             | 0 (R/W)                              | 0 (R/W)                     |
| RES      | MASK_BUCK3_PG_TIMEOUT_IRQ           | MASK_BUCK3_OC_IRQ                    | MASK_BUCK3_PG_IRQ           | MASK_BUCK3_IRQ           | MASK_BUCK2_PG_TIMEOUT_IRQ           | MASK_BUCK2_OC_IRQ                    | MASK_BUCK2_PG_IRQ           |
| Reserved | Mask Buck3 PG timeout interrupt bit | Mask Buck3 overcurrent interrupt bit | Mask Buck3 PG interrupt bit | Mask Buck3 interrupt bit | Mask Buck2 PG timeout interrupt bit | Mask Buck2 overcurrent interrupt bit | Mask Buck2 PG interrupt bit |

**Table 102. DCR6 (0x06) MSB description**

| Bit | Name                      | Description                                                                                                                                                                                              |
|-----|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES                       | Reserved                                                                                                                                                                                                 |
| 22  | MASK_BUCK3_PG_TIMEOUT_IRQ | Mask BUCK3 PG timeout interruption when turned on by SPI command<br>When turned on by a power-up sequence, IRQ is never masked<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default) |
| 21  | MASK_BUCK3_OC_IRQ         | Mask BUCK3 overcurrent interruption<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default)                                                                                            |
| 20  | MASK_BUCK3_PG_IRQ         | Mask BUCK3 power-good interruption when turned ON through SPI<br>1: IRQ signal is not generated<br>0: IRQ signal is generated when the regulator is turned ON through SPI (default)                      |
| 19  | MASK_BUCK3_IRQ            | Mask BUCK3 interruption for overvoltage, undervoltage and for buck internal OV or UV in HIGH- or LOW-POWER<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default)                     |
| 18  | MASK_BUCK2_PG_TIMEOUT_IRQ | Mask BUCK2 PG timeout interruption when turned on by SPI command<br>When turned on by power-up sequence, IRQ is never masked<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default)   |
| 17  | MASK_BUCK2_OC_IRQ         | Mask BUCK2 overcurrent interruption<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default)                                                                                            |
| 16  | MASK_BUCK2_PG_IRQ         | Mask BUCK2 Power Good interruption when turned ON through SPI<br>1: IRQ signal is not generated<br>0: IRQ signal is generated when regulator is turned ON through SPI ( default )                        |

**Table 103. DCR6 (0x06)**

| Bit 15  | Bit 14  | Bit 13  | Bit 12  | Bit 11  | Bit 10  | Bit 9   | Bit 8   |
|---------|---------|---------|---------|---------|---------|---------|---------|
| 0 (R/W) | 0 (R/W) | 0 (R/W) | 0 (R/W) | 0 (R/W) | 0 (R/W) | 0 (R/W) | 0 (R/W) |

| Bit 15                   | Bit 14                              | Bit 13                               | Bit 12                      | Bit 11                   | Bit 10                             | Bit 9                               | Bit 8                                            |
|--------------------------|-------------------------------------|--------------------------------------|-----------------------------|--------------------------|------------------------------------|-------------------------------------|--------------------------------------------------|
| MASK_BUCK2_IRQ           | MASK_BUCK1_PG_TIMEOUT_IRQ           | MASK_BUCK1_OC_IRQ                    | MASK_BUCK1_PG_IRQ           | MASK_BUCK1_IRQ           | MASK_FBB_OV_IRQ                    | MASK_FBB_UV_IRQ                     | MASK_FBB_OV_EW_IRQ                               |
| Mask BUCK2 interrupt bit | Mask BUCK1 PG timeout interrupt bit | Mask BUCK1 overcurrent interrupt bit | Mask BUCK1 PG interrupt bit | Mask BUCK1 interrupt bit | Mask FBB overvoltage interrupt bit | Mask FBB undervoltage interrupt bit | Mask FBB overvoltage early warning interrupt bit |

**Table 104. DCR6 (0x06) description**

| Bit | Name                      | Description                                                                                                                                                                                              |
|-----|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | MASK_BUCK2_IRQ            | Mask BUCK2 interruption for overvoltage, undervoltage and for buck internal OV or UV in HIGH- or LOW-POWER<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default)                     |
| 14  | MASK_BUCK1_PG_TIMEOUT_IRQ | Mask BUCK1 PG timeout interruption when turned on by SPI command<br>When turned on by a power-up sequence, IRQ is never masked<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default) |
| 13  | MASK_BUCK1_OC_IRQ         | Mask BUCK1 overcurrent interruption<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default)                                                                                            |
| 12  | MASK_BUCK1_PG_IRQ         | Mask BUCK1 power-good interruption when turned ON through SPI<br>1: IRQ signal is not generated<br>0: IRQ signal is generated when the regulator is turned ON through SPI (default)                      |
| 11  | MASK_BUCK1_IRQ            | Mask BUCK1 interruption for overvoltage, undervoltage and for BUCK internal OV or UV in HIGH- or LOW-POWER<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default)                     |
| 10  | MASK_FBB_OV_IRQ           | 1: IRQ masked<br>0: IRQ not masked                                                                                                                                                                       |
| 9   | MASK_FBB_UV_IRQ           | 1: IRQ masked<br>0: IRQ not masked                                                                                                                                                                       |
| 8   | MASK_FBB_OV_EW_IRQ        | 1: IRQ masked<br>0: IRQ not masked                                                                                                                                                                       |

**Table 105. DCR6 (0x06) LSB**

| Bit 7                                             | Bit 6                      | Bit 5                              | Bit 4                   | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------------------------------------|----------------------------|------------------------------------|-------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R/W)                                           | 0 (R/W)                    | 0 (R/W)                            | 0 (R/W)                 | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          |
| MASK_FBB_UV_EW_IRQ                                | MASK_LDO2_PG_IRQ           | MASK_LDO2_PG_TIMEOUT_IRQ           | MASK_LDO2_IRQ           | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Mask FBB undervoltage early warning interrupt bit | Mask LDO2 PG interrupt bit | Mask LDO2 PG timeout interrupt bit | Mask LDO2 interrupt bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 106. DCR6 (0x06) LSB description**

| Bit | Name               | Description                                                                                                                |
|-----|--------------------|----------------------------------------------------------------------------------------------------------------------------|
| 7   | MASK_FBB_UV_EW_IRQ | 1: IRQ masked<br>0: IRQ not masked                                                                                         |
| 6   | MASK_LDO2_PG_IRQ   | Mask LDO2 power-good interruption when turned ON through SPI<br>No interrupt generated when turned on by power-up sequence |

| Bit | Name                     | Description                                                                                                                                                                                        |
|-----|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                          | 1: IRQ signal is not generated<br>0: IRQ signal is generated when the regulator is turned ON through SPI (default)                                                                                 |
| 5   | MASK_LDO2_PG_TIMEOUT_IRQ | Mask LDO2 power-good timeout when turned on by SPI request<br>No interrupt generated when turned on by power-up sequence<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default) |
| 4   | MASK_LDO2_IRQ            | Mask LDO2 overvoltage or undervoltage interruption<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default)                                                                       |
| 3   | CRC3                     |                                                                                                                                                                                                    |
| 2   | CRC2                     |                                                                                                                                                                                                    |
| 1   | CRC1                     |                                                                                                                                                                                                    |
| 0   | CRC0                     |                                                                                                                                                                                                    |

**Table 107. DCR7 (0x07) MSB**

| Bit 23   | Bit 22                     | Bit 21                             | Bit 20                  | Bit 19                                     | Bit 18                           | Bit 17                          | Bit 16                |
|----------|----------------------------|------------------------------------|-------------------------|--------------------------------------------|----------------------------------|---------------------------------|-----------------------|
| - (R0)   | 0 (R/W)                    | 0 (R/W)                            | 0 (R/W)                 | 0 (R/W)                                    | 0 (R/W)                          | 0 (R/W)                         | 0 (R/W)               |
| RES      | MASK_LDO1_PG_IRQ           | MASK_LDO1_PG_TIMEOUT_IRQ           | MASK_LDO1_IRQ           | MASK_BOOST_IN_LP_IRQ                       | MASK_BYPASS_VDSMON_IRQ           | MASK_BOOST_VDSMON_IRQ           | IRQ_REQUEST           |
| Reserved | Mask LDO1 PG interrupt bit | Mask LDO1 PG timeout interrupt bit | Mask LDO1 interrupt bit | Mask BOOST in LOW-POWER mode interrupt bit | Mask bypass VDSMON interrupt bit | Mask BOOST VDSMON interrupt bit | Interrupt request bit |

**Table 108. DCR7 (0x07) MSB description**

| Bit | Name                     | Description                                                                                                                                                                                                                                      |
|-----|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES                      | Reserved                                                                                                                                                                                                                                         |
| 22  | MASK_LDO1_PG_IRQ         | Mask LDO1 power-good interruption when turned ON through SPI<br>No interrupt generated when turned on by power-up sequence<br>1: IRQ signal is not generated<br>0: IRQ signal is generated when the regulator is turned ON through SPI (default) |
| 21  | MASK_LDO1_PG_TIMEOUT_IRQ | Mask LDO1 power-good timeout when turned on by SPI request<br>No interrupt generated when turned on by power-up sequence<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default)                                               |
| 20  | MASK_LDO1_IRQ            | Mask LDO1 undervoltage interruption<br>1: IRQ signal is not generated<br>0: IRQ signal is generated (default)                                                                                                                                    |
| 19  | MASK_BOOST_IN_LP_IRQ     | 1: IRQ masked<br>0: IRQ not masked                                                                                                                                                                                                               |
| 18  | MASK_BYPASS_VDSMON_IRQ   | 1: IRQ masked<br>0: IRQ not masked                                                                                                                                                                                                               |
| 17  | MASK_BOOST_VDSMON_IRQ    | 1: IRQ masked<br>0: IRQ not masked                                                                                                                                                                                                               |
| 16  | IRQ_REQUEST              | 1: Send IRQ to MCU<br>This bit is automatically cleared and always read low<br>0: No action                                                                                                                                                      |

**Table 109. DCR7 (0x07)**

| Bit 15                                          | Bit 14                 | Bit 13                                       | Bit 12                                               | Bit 11                                       | Bit 10                                       | Bit 9                                        | Bit 8                            |
|-------------------------------------------------|------------------------|----------------------------------------------|------------------------------------------------------|----------------------------------------------|----------------------------------------------|----------------------------------------------|----------------------------------|
| 0 (R/W)                                         | 0 (R/W)                | 0 (R/W)                                      | 0 (R/W)                                              | 0 (R/W)                                      | 0 (R/W)                                      | 0 (R/W)                                      | 0 (R/W)                          |
| MASK_VS_EW_IRQ                                  | MASK_CAN_IRQ           | MASK_CL4_TW_IRQ                              | MASK_CL3_TW_IRQ                                      | MASK_CL2_TW_IRQ                              | MASK_CL1_TW_IRQ                              | MASK_CL0_TW_IRQ                              | MASK_OUTHS_IRQ                   |
| Mask V <sub>S</sub> early warning interrupt bit | Mask CAN Interrupt Bit | Mask thermal cluster 4 warning interrupt bit | Mask thermal cluster 3 thermal warning interrupt bit | Mask thermal cluster 2 warning interrupt bit | Mask thermal cluster 1 warning interrupt bit | Mask thermal cluster 0 warning interrupt bit | Mask out high side interrupt bit |

**Table 110. DCR7 (0x07) description**

| Bit | Name            | Description                        |
|-----|-----------------|------------------------------------|
| 15  | MASK_VS_EW_IRQ  | 1: IRQ masked<br>0: IRQ not masked |
| 14  | MASK_CAN_IRQ    | 1: IRQ masked<br>0: IRQ not masked |
| 13  | MASK_CL4_TW_IRQ | 1: IRQ masked<br>0: IRQ not masked |
| 12  | MASK_CL3_TW_IRQ | 1: IRQ masked<br>0: IRQ not masked |
| 11  | MASK_CL2_TW_IRQ | 1: IRQ masked<br>0: IRQ not masked |
| 10  | MASK_CL1_TW_IRQ | 1: IRQ masked<br>0: IRQ not masked |
| 9   | MASK_CL0_TW_IRQ | 1: IRQ masked<br>0: IRQ not masked |
| 8   | MASK_OUTHS_IRQ  | 1: IRQ masked<br>0: IRQ not masked |

**Table 111. DCR7 (0x07) LSB**

| Bit 7                        | Bit 6                               | Bit 5                                         | Bit 4                                     | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|------------------------------|-------------------------------------|-----------------------------------------------|-------------------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R/W)                      | 0 (R/W)                             | 0 (R/W)                                       | 0 (R/W)                                   | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          |
| MASK_SPI_ERROR_IRQ           | MASK_NFSO1_ECHO_ERROR_IRQ           | MASK_WD_ENA_ECHO_ERROR_IRQ                    | MASK_FCCU_ENA_ECHO_ERROR_IRQ              | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Mask SPI error interrupt bit | Mask NFSO1 echo error interrupt bit | Mask watchdog enable echo error interrupt bit | Mask FCCU enable echo error interrupt bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 112. DCR7 (0x07) LSB description**

| Bit | Name                         | Description                        |
|-----|------------------------------|------------------------------------|
| 7   | MASK_SPI_ERROR_IRQ           | 1: IRQ masked<br>0: IRQ not masked |
| 6   | MASK_NFSO1_ECHO_ERROR_IRQ    | 1: IRQ masked<br>0: IRQ not masked |
| 5   | MASK_WD_ENA_ECHO_ERROR_IRQ   | 1: IRQ masked<br>0: IRQ not masked |
| 4   | MASK_FCCU_ENA_ECHO_ERROR_IRQ | 1: IRQ masked<br>0: IRQ not masked |
| 3   | CRC3                         |                                    |
| 2   | CRC2                         |                                    |

| Bit | Name | Description |
|-----|------|-------------|
| 1   | CRC1 |             |
| 0   | CRC0 |             |

**Table 113. DCR8 (0x08) MSB**

| Bit 23   | Bit 22                                | Bit 21                                  | Bit 20                 | Bit 19                               | Bit 18                               | Bit 17                               | Bit 16                                |
|----------|---------------------------------------|-----------------------------------------|------------------------|--------------------------------------|--------------------------------------|--------------------------------------|---------------------------------------|
| - (R0)   | 0 (R/W)                               | 0 (R/W)                                 | 0 (R/W)                | 0 (R/W)                              | 0 (R/W)                              | 0 (R/W)                              | 0 (R/W)                               |
| RES      | MASK_SWDBG_VIO_IRQ                    | MASK_LP_READY_IRQ                       | CLR_TSD_CNT_FAIL       | MASK_BUCK3_OC_POWER_OFF              | MASK_BUCK2_OC_POWER_OFF              | MASK_BUCK1_OC_POWER_OFF              | MASK_BUCK3_UV_POWER_OFF               |
| Reserved | Mask software debug VIO interrupt bit | Mask LOW-POWER mode ready interrupt bit | Clear TSD_CNT_FAIL bit | Mask BUCK3 overcurrent power-off bit | Mask BUCK2 overcurrent power-off bit | Mask BUCK1 overcurrent power-off bit | Mask BUCK3 undervoltage power-off bit |

**Table 114. DCR8 (0x08) MSB description**

| Bit | Name                    | Description                                                                                                                                                                                          |
|-----|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES                     | reserved                                                                                                                                                                                             |
| 22  | MASK_SWDBG_VIO_IRQ      | Mask IRQ when SWDBG is still at $V_{IO}$ at the end of timeout detection. In this case, watchdog is restarted with a long open window and SWDBG is ignored.<br>1: IRQ is masked<br>0: IRQ not masked |
| 21  | MASK_LP_READY_IRQ       | Mask IRQ when FSM goes to LOW-POWER state.<br>1: IRQ is masked<br>0: IRQ not masked                                                                                                                  |
| 20  | CLR_TSD_CNT_FAIL        | Clear TSD_CNT_FAIL to 0<br>This bit is always read low                                                                                                                                               |
| 19  | MASK_BUCK3_OC_POWER_OFF | Mask BUCK3 overcurrent as source of its power-off<br>1: Regulator is not turned off after an overcurrent occurs<br>0: Regulator is turned off after an overcurrent occurs                            |
| 18  | MASK_BUCK2_OC_POWER_OFF | Mask BUCK2 overcurrent as source of its power-off<br>1: Regulator is not turned off after an overcurrent occurs<br>0: Regulator is turned off after an overcurrent occurs                            |
| 17  | MASK_BUCK1_OC_POWER_OFF | Mask BUCK1 overcurrent as source of its power-off<br>1: Regulator is not turned off after an overcurrent occurs<br>0: Regulator is turned off after an overcurrent occurs                            |
| 16  | MASK_BUCK3_UV_POWER_OFF | Mask BUCK3 under voltage as source of its power-off<br>1: Regulator is not turned off after an undervoltage occurs<br>0: Regulator is turned off after an undervoltage occurs                        |

**Table 115. DCR8 (0x08)**

| Bit 15                                | Bit 14                                | Bit 13                      | Bit 12                 | Bit 11                            | Bit 10                      | Bit 9                          | Bit 8                                |
|---------------------------------------|---------------------------------------|-----------------------------|------------------------|-----------------------------------|-----------------------------|--------------------------------|--------------------------------------|
| 0 (R/W)                               | 0 (R/W)                               | 0 (R/W)                     | 0 (R/W)                | 0 (R/W)                           | 0 (R/W)                     | 0 (R/W)                        | 0 (R/W)                              |
| MASK_BUCK2_UV_POWER_OFF               | MASK_BUCK1_UV_POWER_OFF               | MASK_TW_GW                  | MASK_OL_GSB            | MASK_FE2_GSB                      | MASK_GW_GSB                 | CAN_ACT                        | CAN_AUTO_BIAS                        |
| Mask BUCK2 undervoltage power-off bit | Mask BUCK1 undervoltage power-off bit | Mask thermal warning GW bit | Mask open load GSB bit | Mask physical layer error GSB bit | Mask global warning GSB bit | CAN transceiver activation bit | CAN automatic biasing activation bit |

**Table 116. DCR8 (0x08) description**

| Bit | Name                    | Description                                        |
|-----|-------------------------|----------------------------------------------------|
| 15  | MASK_BUCK2_UV_POWER_OFF | Mask BUCK2 undervoltage as source of its power-off |

| Bit | Name                    | Description                                                                                                                                                                                                        |
|-----|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                         | 1: Regulator is not turned off after an undervoltage occurs<br>0: Regulator is turned off after an undervoltage occurs                                                                                             |
| 14  | MASK_BUCK1_UV_POWER_OFF | Mask BUCK1 undervoltage as source of its power-off<br>1: Regulator is not turned off after an undervoltage occurs<br>0: Regulator is turned off after an undervoltage occurs                                       |
| 13  | MASK_TW_GW              | Mask thermal Warnings<br>1: Thermal warnings are masked in GW<br>0: Thermal warnings are not masked (default)                                                                                                      |
| 12  | MASK_OL_GSB             | Mask open-load<br>1: Open-load condition at OUTHS is masked<br>It is reported as a functional error 1 (GSB bit 3) but not as a global error (GSB bit 7)<br>0: Open-load condition at OUTHS is not masked (default) |
| 11  | MASK_FE2_GSB            | Mask physical layer error<br>1: Physical layer errors are masked<br>i.e. reported as a physical layer error (GSB bit 4) but not as a global error (GSB bit 7)<br>0: Physical layer errors are not masked (default) |
| 10  | MASK_GW_GSB             | Mask global warning<br>1: Global warning conditions are masked<br>It is reported as a global warning (GSB bit 1) but not as a global error (GSB bit 7)<br>0: Global warning conditions are not masked (default)    |
| 9   | CAN_ACT                 | CAN Transceiver activation<br>1 : CAN Trx normal active mode<br>At Exit from normal active mode, this bit is set to '0' automatically<br>0 : CAN Trx low power mode (default)                                      |
| 8   | CAN_AUTO_BIAS           | CAN automatic biasing activation<br>1 : auto biasing enabled<br>0 : auto biasing disabled ( default )                                                                                                              |

**Table 117. DCR8 (0x08) LSB**

| Bit 7               | Bit 6                     | Bit 5                  | Bit 4        | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------|---------------------------|------------------------|--------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R/W)             | 0 (R/W)                   | 1 (R/W)                | 0 (R/W)      | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          |
| CAN_LOOP_ENA        | CAN_REC_ONLY              | CAN_WU_ENA             | GO_INIT      | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| CAN Loop enable bit | CAN Receive only Mode bit | CAN Wake-up enable bit | NVM INIT bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 118. DCR8 (0x08) LSB description**

| Bit | Name         | Description                                                                                                                             |
|-----|--------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 7   | CAN_LOOP_ENA | CAN Loop enable: TxD_C signal is internal routed to RxD_C pin<br>1: CAN loop enabled<br>0: CAN loop disabled (default)                  |
| 6   | CAN_REC_ONLY | CAN Receive only Mode<br>1 : CAN Receive only mode enabled (CAN Trx must be activated, see CAN_ACT bit)<br>0: TX & RX enabled (default) |

| Bit | Name       | Description                                                                                                                                                                                                       |
|-----|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | CAN_WU_ENA | CAN Wake-up enable: enable wake-up by CAN<br>1 : enabled (default)<br>0: CAN wake-up disabled                                                                                                                     |
| 4   | GO_INIT    | 1: NVM emulation and load phases are completed and INIT state can be executed<br>(valid only in USER_NVM_PROG state)<br>This bit is automatically cleared and always read low and always read low<br>0: (default) |
| 3   | CRC3       |                                                                                                                                                                                                                   |
| 2   | CRC2       |                                                                                                                                                                                                                   |
| 1   | CRC1       |                                                                                                                                                                                                                   |
| 0   | CRC0       |                                                                                                                                                                                                                   |

**Table 119. DCR9 (0x09) MSB**

| Bit 23 (MSB) | Bit 22             | Bit 21   | Bit 20              | Bit 19   | Bit 18                       | Bit 17                              | Bit 16                              |
|--------------|--------------------|----------|---------------------|----------|------------------------------|-------------------------------------|-------------------------------------|
| - (R0)       | 0 (R/W)            | - (R0)   | 0 (R/W)             | - (R0)   | 0 (R/W)                      | 0 (R/W)                             | 0 (R/W)                             |
| RES          | LDT_TIMER_READ_ENA | RES      | BOOST_CNT_END       | RES      | MASK_BOOST_TIMER_CNT_END_IRQ | LDT_CNT_THR_4                       | LDT_CNT_THR_3                       |
| reserved     | Lock LDT counter   | reserved | Reset Boost Counter | reserved | Mask Boost timer end IRQ     | LDT Counter threshold setting bit 4 | LDT Counter threshold setting bit 3 |

**Table 120. DCR9 (0x09) MSB description**

| Bit | Name                         | Description                                                                                                                   |
|-----|------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES                          | reserved                                                                                                                      |
| 22  | LDT_TIMER_READ_ENA           | Lock the LDT counter to allow MCU to read the LDT counter value<br>1 : lock the LDT counter<br>0 : normal LDT counter updates |
| 21  | RES                          | reserved                                                                                                                      |
| 20  | BOOST_CNT_END                | Allow to stop and reset the Boost Counter<br>1 : stop and reset the boost counter<br>0 : re-launch boost timer                |
| 19  | RES                          | reserved                                                                                                                      |
| 18  | MASK_BOOST_TIMER_CNT_END_IRQ | To mask IRQ in case of Boost timer counter end                                                                                |
| 17  | LDT_CNT_THR_4                | Long Duration timer duration ( locked when LDT_CNT_ENA =1)                                                                    |
| 16  | LDT_CNT_THR_3                |                                                                                                                               |

**Table 121. DCR9 (0x09)**

| Bit 15                              | Bit 14                              | Bit 13                              | Bit 12                                               | Bit 11                                               | Bit 10                                               | Bit 9                                                | Bit 8                                                |
|-------------------------------------|-------------------------------------|-------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| 0 (R/W)                             | 0 (R/W)                             | 0 (R/W)                             | 0 (R/W)                                              | 0 (R/W)                                              | 0 (R/W)                                              | 0 (R/W)                                              | 0 (R/W)                                              |
| LDT_CNT_THR_2                       | LDT_CNT_THR_1                       | LDT_CNT_THR_0                       | LDT_CNT_THR_MSB_POS_4                                | LDT_CNT_THR_MSB_POS_3                                | LDT_CNT_THR_MSB_POS_2                                | LDT_CNT_THR_MSB_POS_1                                | LDT_CNT_THR_MSB_POS_0                                |
| LDT Counter threshold setting bit 2 | LDT Counter threshold setting bit 1 | LDT Counter threshold setting bit 0 | LDT Counter threshold setting for MSB position bit 4 | LDT Counter threshold setting for MSB position bit 3 | LDT Counter threshold setting for MSB position bit 2 | LDT Counter threshold setting for MSB position bit 1 | LDT Counter threshold setting for MSB position bit 0 |

**Table 122. DCR9 (0x09) description**

| Bit | Name          | Description |
|-----|---------------|-------------|
| 15  | LDT_CNT_THR_2 |             |

| Bit | Name                  | Description                                                             |
|-----|-----------------------|-------------------------------------------------------------------------|
| 14  | LDT_CNT_THR_1         |                                                                         |
| 13  | LDT_CNT_THR_0         |                                                                         |
| 12  | LDT_CNT_THR_MSB_POS_4 | Long Duration timer duration MSB position ( locked when LDT_CNT_ENA =1) |
| 11  | LDT_CNT_THR_MSB_POS_3 |                                                                         |
| 10  | LDT_CNT_THR_MSB_POS_2 |                                                                         |
| 9   | LDT_CNT_THR_MSB_POS_1 |                                                                         |
| 8   | LDT_CNT_THR_MSB_POS_0 |                                                                         |

**Table 123. DCR9 (0x09) LSB**

| Bit 7                                        | Bit 6       | Bit 5      | Bit 4              | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|----------------------------------------------|-------------|------------|--------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R/W)                                      | 0 (R/W)     | 0 (R/W)    | 0 (R/W)            | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          | 0 (R/W)                          |
| LDT_DEBUG                                    | LDT_MODE    | LDT_ENA    | LDT_CNT_ENA        | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| LDT debug to reduce duration by a factor 100 | LDT wake up | LDT enable | LDT Counter enable | Cyclic Redundancy Checking Bit 3 | Cyclic Redundancy Checking Bit 2 | Cyclic Redundancy Checking Bit 1 | Cyclic Redundancy Checking Bit 0 |

**Table 124. DCR9 (0x09) LSB description**

| Bit | Name        | Description                                                                                                                                                                      |
|-----|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | LDT_DEBUG   | Long duration time mode to reduce LDT duration by a factor 100<br>1: count with 10 ms period<br>0: count with 1s period (locked when LDT_CNT_ENA =1)                             |
| 6   | LDT_MODE    | Long Duration Timer wake-up capability selection<br>1: count up to LDT_THR and take action (wake-up)<br>0: count up to max count and take no action (locked when LDT_CNT_ENA =1) |
| 5   | LDT_ENA     | Long Duration Timer enable<br>1: enable LDT functionality<br>0: Disable and Reset LDT functionality                                                                              |
| 4   | LDT_CNT_ENA | Long Duration Timer counter enable<br>1 : Start LDT CNT<br>0 : Stop LDT CNT (Cnt Value is retained, Cnt value is restarted to 0 at next LDT_CNT set to 1)                        |
| 3   | CRC3        |                                                                                                                                                                                  |
| 2   | CRC2        |                                                                                                                                                                                  |
| 1   | CRC1        |                                                                                                                                                                                  |
| 0   | CRC0        |                                                                                                                                                                                  |

## 9.6 U\_NVM registers

During the emulation mode (described in [Section 3.8.2](#)), the U\_NVM SPI registers from DCR10 to DRC28 can be R/W. After a valid USER-NVM programming procedure, the U\_NVM SPI registers from DCR10 to DRC28 can only be readable as shown below.

**Table 125. DCR10 (0x0A) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19              | Bit 18                            | Bit 17                            | Bit 16                            |
|----------|----------|----------|----------|---------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)               | - (R)                             | - (R)                             | - (R)                             |
| RES      | RES      | RES      | RES      | BUCK1_FREQ          | BUCK1_PU_VALUE_1                  | BUCK1_PU_VALUE_0                  | BUCK1_PU_STEP_ENA_2               |
| Reserved | Reserved | Reserved | Reserved | BUCK1 frequency bit | BUCK1 voltage setting value bit 1 | BUCK1 voltage setting value bit 0 | BUCK1 Power-up step enables bit 2 |

**Table 126. DCR10 (0x0A) MSB description**

| Bit | Name                | Description                                                  |
|-----|---------------------|--------------------------------------------------------------|
| 23  | RES                 | Reserved                                                     |
| 22  | RES                 | Reserved                                                     |
| 21  | RES                 | Reserved                                                     |
| 20  | RES                 | Reserved                                                     |
| 19  | BUCK1_FREQ          | BUCK1 frequency:<br>1: 0.4 MHz<br>0: 2.4 MHz                 |
| 18  | BUCK1_PU_VALUE_1    | BUCK1 voltage setting<br>00: 3.3 V<br>01: 5.0 V<br>1X: 6.5 V |
| 17  | BUCK1_PU_VALUE_0    |                                                              |
| 16  | BUCK1_PU_STEP_ENA_2 |                                                              |

**Table 127. DCR10 (0x0A)**

| Bit 15                            | Bit 14                            | Bit 13                          | Bit 12                          | Bit 11                          | Bit 10                              | Bit 9                               | Bit 8                               |
|-----------------------------------|-----------------------------------|---------------------------------|---------------------------------|---------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|
| - (R)                             | - (R)                             | - (R)                           | - (R)                           | - (R)                           | - (R)                               | - (R)                               | - (R)                               |
| BUCK1_PU_STEP_ENA_1               | BUCK1_PU_STEP_ENA_0               | BUCK1_PD_STEP_OFF_2             | BUCK1_PD_STEP_OFF_1             | BUCK1_PD_STEP_OFF_0             | BUCK1_IPEAK_2                       | BUCK1_IPEAK_1                       | BUCK1_IPEAK_0                       |
| BUCK1 Power-up step enables bit 1 | BUCK1 Power-up step enables bit 0 | BUCK1 power-down step off bit 2 | BUCK1 power-down step off bit 1 | BUCK1 power-down step off bit 0 | BUCK1 peak limitation current bit 2 | BUCK1 peak limitation current bit 1 | BUCK1 peak limitation current bit 0 |

**Table 128. DCR10 (0x0A) description**

| Bit | Name                | Description                                                                                                                                           |
|-----|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | BUCK1_PU_STEP_ENA_1 |                                                                                                                                                       |
| 14  | BUCK1_PU_STEP_ENA_0 | To define BUCK1 turn-on steps<br>000: BUCK is not turned ON<br>001: Step 1<br>010: Step 2<br>011: Step 3<br>100: Step 4<br>101: Step 5<br>110: Step 6 |

| Bit | Name                | Description                                                                                                                             |
|-----|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
|     |                     | 111: Step 7                                                                                                                             |
| 13  | BUCK1_PD_STEP_OFF_2 |                                                                                                                                         |
| 12  | BUCK1_PD_STEP_OFF_1 |                                                                                                                                         |
| 11  | BUCK1_PD_STEP_OFF_0 | To define BUCK1 turn-off steps<br>000: Step 1<br>001: Step 2<br>010: Step 3<br>011: Step 4<br>100: Step 5<br>101: Step 6<br>11X: Step 7 |
| 10  | BUCK1_IPEAK_2       |                                                                                                                                         |
| 9   | BUCK1_IPEAK_1       |                                                                                                                                         |
| 8   | BUCK1_IPEAK_0       | BUCK1 peak limitation current<br>000: 2.0 A<br>001: 2.5 A<br>010: 3.0 A<br>011: 3.5 A<br>100: 4.0 A<br>101: 4.5 A<br>11X: 5.0 A         |

**Table 129. DCR10 (0x0A) LSB**

| Bit 7                                        | Bit 6                        | Bit 5                        | Bit 4                       | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|----------------------------------------------|------------------------------|------------------------------|-----------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)                                        | - (R)                        | - (R)                        | - (R)                       | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| BUCK1_REGFAIL_GO_REC                         | BUCK1_SS_VALUE_1             | BUCK1_SS_VALUE_0             | BUCK1_REFRESH_FREQ          | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| BUCK1 regulator fail power-down to REC-2 bit | BUCK1 soft-start value bit 1 | BUCK1 soft-start value bit 0 | BUCK1 refresh frequency bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 130. DCR10 (0x0A) LSB description**

| Bit | Name                 | Description                                                                                                                                                                                                                                                                                                                                            |
|-----|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | BUCK1_REGFAIL_GO_REC | 1: A fail on BUCK1 regulator initiates a power-down sequence and moves the state machine to REC-2 state<br>0: A fail on BUCK1 regulator sends an IRQ (UV, OV, PG_nok, TW are maskable by SPI, but not TSD), and turns the regulator OFF if the fail is unmasked (UV, PG_nok are maskable by SPI, but not OV and TSD. TW never turns the regulator OFF) |
| 6   | BUCK1_SS_VALUE_1     |                                                                                                                                                                                                                                                                                                                                                        |
| 5   | BUCK1_SS_VALUE_0     | BUCK1 soft-start setting<br>00: 16.5 V/ms<br>01: 8.25 V/ms<br>10: 3.3 V/ms<br>11: 1.65 V/ms                                                                                                                                                                                                                                                            |
| 4   | BUCK1_REFRESH_FREQ   | 1: Refresh frequency 1 kHz<br>0: Refresh frequency 25 kHz                                                                                                                                                                                                                                                                                              |

| Bit | Name | Description |
|-----|------|-------------|
| 3   | CRC3 |             |
| 2   | CRC2 |             |
| 1   | CRC1 |             |
| 0   | CRC0 |             |

**Table 131. DCR11 (0x0B) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19              | Bit 18                            | Bit 17                            | Bit 16                            |
|----------|----------|----------|----------|---------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| -(R0)    | -(R0)    | -(R0)    | -(R0)    | -(R)                | -(R)                              | -(R)                              | -(R)                              |
| RES      | RES      | RES      | RES      | BUCK2_FREQ          | BUCK2_PU_VALUE_1                  | BUCK2_PU_VALUE_0                  | BUCK2_PU_STEP_ENA_2               |
| Reserved | Reserved | Reserved | Reserved | BUCK2 frequency bit | BUCK2 voltage setting value bit 1 | BUCK2 voltage setting value bit 0 | BUCK2 Power-up step enables bit 2 |

**Table 132. DCR11 (0x0B) MSB description**

| Bit | Name                | Description                                                  |
|-----|---------------------|--------------------------------------------------------------|
| 23  | RES                 | Reserved                                                     |
| 22  | RES                 | Reserved                                                     |
| 21  | RES                 | Reserved                                                     |
| 20  | RES                 | Reserved                                                     |
| 19  | BUCK2_FREQ          | BUCK2 frequency<br>1: 0.4 MHz<br>0: 2.4 MHz                  |
| 18  | BUCK2_PU_VALUE_1    | BUCK2 voltage setting<br>00: 3.3 V<br>01: 5.0 V<br>1X: 6.5 V |
| 17  | BUCK2_PU_VALUE_0    |                                                              |
| 16  | BUCK2_PU_STEP_ENA_2 |                                                              |

**Table 133. DCR11 (0x0B)**

| Bit 15                            | Bit 14                            | Bit 13                          | Bit 12                          | Bit 11                          | Bit 10                              | Bit 9                               | Bit 8                               |
|-----------------------------------|-----------------------------------|---------------------------------|---------------------------------|---------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|
| -(R)                              | -(R)                              | -(R)                            | -(R)                            | -(R)                            | -(R)                                | -(R)                                | -(R)                                |
| BUCK2_PU_STEP_ENA_1               | BUCK2_PU_STEP_ENA_0               | BUCK2_PD_STEP_OFF_2             | BUCK2_PD_STEP_OFF_1             | BUCK2_PD_STEP_OFF_0             | BUCK2_IPEAK_2                       | BUCK2_IPEAK_1                       | BUCK2_IPEAK_0                       |
| BUCK2 Power-up step enables bit 1 | BUCK2 Power-up step enables bit 0 | BUCK2 power-down step off bit 2 | BUCK2 power-down step off bit 1 | BUCK2 power-down step off bit 0 | BUCK2 peak limitation current bit 2 | BUCK2 peak limitation current bit 1 | BUCK2 peak limitation current bit 0 |

**Table 134. DCR11 (0x0B) description**

| Bit | Name                | Description                                                                                                                            |
|-----|---------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 15  | BUCK2_PU_STEP_ENA_1 |                                                                                                                                        |
| 14  | BUCK2_PU_STEP_ENA_0 | To define BUCK2 turn-on steps<br>000: BUCK is not turned ON<br>001: Step 1<br>010: Step 2<br>011: Step 3<br>100: Step 4<br>101: Step 5 |

| Bit | Name                | Description                                                                                                                             |
|-----|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
|     |                     | 110: Step 6<br>111: Step 7                                                                                                              |
| 13  | BUCK2_PD_STEP_OFF_2 |                                                                                                                                         |
| 12  | BUCK2_PD_STEP_OFF_1 |                                                                                                                                         |
| 11  | BUCK2_PD_STEP_OFF_0 | To define BUCK2 turn-off steps<br>000: Step 1<br>001: Step 2<br>010: Step 3<br>011: Step 4<br>100: Step 5<br>101: Step 6<br>11X: Step 7 |
| 10  | BUCK2_IPEAK_2       |                                                                                                                                         |
| 9   | BUCK2_IPEAK_1       |                                                                                                                                         |
| 8   | BUCK2_IPEAK_0       | BUCK2 peak limitation current<br>000: 2.0 A<br>001: 2.5 A<br>010: 3.0 A<br>011: 3.5 A<br>100: 4.0 A<br>101: 4.5 A<br>11X: 5.0 A         |

**Table 135. DCR11 (0x0B) LSB**

| Bit 7                                        | Bit 6                        | Bit 5                        | Bit 4                       | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|----------------------------------------------|------------------------------|------------------------------|-----------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)                                        | - (R)                        | - (R)                        | - (R)                       | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| BUCK2_REGFAIL_GO_REC                         | BUCK2_SS_VALUE_1             | BUCK2_SS_VALUE_0             | BUCK2_REFRESH_FREQ          | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| BUCK2 regulator fail power-down to REC-2 bit | BUCK2 soft-start value bit 1 | BUCK2 soft-start value bit 0 | BUCK2 refresh frequency bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 136. DCR11 (0x0B) LSB description**

| Bit | Name                 | Description                                                                                                                                                                                                                                                                                                                                            |
|-----|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | BUCK2_REGFAIL_GO_REC | 1: A fail on BUCK2 regulator initiates a power-down sequence and moves the state machine to REC-2 state<br>0: A fail on BUCK2 regulator sends an IRQ (UV, OV, PG_nok, TW are maskable by SPI, but not TSD), and turns the regulator OFF if the fail is unmasked (UV, PG_nok are maskable by SPI, but not OV and TSD. TW never turns the regulator OFF) |
| 6   | BUCK2_SS_VALUE_1     |                                                                                                                                                                                                                                                                                                                                                        |
| 5   | BUCK2_SS_VALUE_0     | BUCK2 soft-start setting<br>00: 16.5 V/ms<br>01: 8.25 V/ms<br>10: 3.3 V/ms<br>11: 1.65 V/ms                                                                                                                                                                                                                                                            |
| 4   | BUCK2_REFRESH_FREQ   | 1: Refresh frequency 1 kHz                                                                                                                                                                                                                                                                                                                             |

| Bit | Name | Description                 |
|-----|------|-----------------------------|
|     |      | 0: Refresh frequency 25 kHz |
| 3   | CRC3 |                             |
| 2   | CRC2 |                             |
| 1   | CRC1 |                             |
| 0   | CRC0 |                             |

**Table 137. DCR12 (0x0C) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19             | Bit 18   | Bit 17   | Bit 16              |
|----------|----------|----------|----------|--------------------|----------|----------|---------------------|
| -(R0)    | -(R0)    | -(R0)    | -(R0)    | - (R)              | - (R)    | - (R)    | - (R)               |
| RES      | RES      | RES      | RES      | BYPASS_DIS         | RES      | RES      | BUCK3_PU_VALUE      |
| Reserved | Reserved | Reserved | Reserved | Bypass disable bit | Reserved | Reserved | BUCK3 voltage value |

**Table 138. DCR12 (0x0C) MSB description**

| Bit | Name           | Description                                                                           |
|-----|----------------|---------------------------------------------------------------------------------------|
| 23  | RES            | Reserved                                                                              |
| 22  | RES            | Reserved                                                                              |
| 21  | RES            | Reserved                                                                              |
| 20  | RES            | Reserved                                                                              |
| 19  | BYPASS_DIS     | 1 : BYPASS always OFF<br>0 : Bypass ON or OFF based on the sensed value on the VS pin |
| 18  | RES            |                                                                                       |
| 17  | RES            |                                                                                       |
| 16  | BUCK3_PU_VALUE | BUCK3 voltage setting<br>1: 1.02 V<br>0: BUCK3 is OFF                                 |

**Table 139. DCR12 (0x0C)**

| Bit 15                            | Bit 14                            | Bit 13                            | Bit 12                          | Bit 11                          | Bit 10                          | Bit 9                              | Bit 8                              |
|-----------------------------------|-----------------------------------|-----------------------------------|---------------------------------|---------------------------------|---------------------------------|------------------------------------|------------------------------------|
| -(R)                              | -(R)                              | -(R)                              | -(R)                            | -(R)                            | -(R)                            | -(R)                               | -(R)                               |
| BUCK3_PU_STEP_ENA_2               | BUCK3_PU_STEP_ENA_1               | BUCK3_PU_STEP_ENA_0               | BUCK3_PD_STEP_OFF_2             | BUCK3_PD_STEP_OFF_1             | BUCK3_PD_STEP_OFF_0             | BUCK3_IPEAK_1                      | BUCK3_IPEAK_0                      |
| BUCK3 power-up step enables bit 2 | BUCK3 power-up step enables bit 1 | BUCK3 power-up step enables bit 0 | BUCK3 power-down step off bit 2 | BUCK3 power-down step off bit 1 | BUCK3 power-down step off bit 0 | BUCK3 peak switching current bit 1 | BUCK3 peak switching current bit 0 |

**Table 140. DCR12 (0x0C) description**

| Bit | Name                | Description                                                                                                                            |
|-----|---------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 15  | BUCK3_PU_STEP_ENA_2 |                                                                                                                                        |
| 14  | BUCK3_PU_STEP_ENA_1 |                                                                                                                                        |
| 13  | BUCK3_PU_STEP_ENA_0 | To define BUCK3 turn-on steps<br>000: BUCK is not turned ON<br>001: Step 1<br>010: Step 2<br>011: Step 3<br>100: Step 4<br>101: Step 5 |

| Bit | Name                | Description                                                                                                                             |
|-----|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
|     |                     | 110: Step 6<br>111: Step 7                                                                                                              |
| 12  | BUCK3_PD_STEP_OFF_2 | To define BUCK3 turn-off steps<br>000: Step 1<br>001: Step 2<br>010: Step 3<br>011: Step 4<br>100: Step 5<br>101: Step 6<br>11X: Step 7 |
| 11  | BUCK3_PD_STEP_OFF_1 |                                                                                                                                         |
| 10  | BUCK3_PD_STEP_OFF_0 |                                                                                                                                         |
| 9   | BUCK3_IPEAK_1       | BUCK3 peak switching current<br>00: 4.0 A<br>01: 5.0 A<br>10: 6.0 A<br>11: 7.0 A                                                        |
| 8   | BUCK3_IPEAK_0       |                                                                                                                                         |

**Table 141. DCR12 (0x0C) LSB**

| Bit 7                                           | Bit 6                        | Bit 5                        | Bit 4                       | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-------------------------------------------------|------------------------------|------------------------------|-----------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)                                           | - (R)                        | - (R)                        | - (R)                       | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| BUCK3_REGFAIL_GO_REC                            | BUCK3_SS_VALUE_1             | BUCK3_SS_VALUE_0             | BUCK3_REFRESH_FREQ          | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| BUCK3 regulator fail go power-down to REC-2 bit | BUCK3 soft-start value bit 1 | BUCK3 soft-start value bit 0 | BUCK3 refresh frequency bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 142. DCR12 (0x0C) LSB description**

| Bit | Name                 | Description                                                                                                                                                                                                                                                                                                                                            |
|-----|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | BUCK3_REGFAIL_GO_REC | 1: A fail on BUCK3 regulator initiates a power-down sequence and moves the state machine to REC-2 state<br>0: A fail on BUCK3 regulator sends an IRQ (UV, OV, PG_nok, TW are maskable by SPI, but not TSD), and turns the regulator OFF if the fail is unmasked (UV, PG_nok are maskable by SPI, but not OV and TSD. TW never turns the regulator OFF) |
| 6   | BUCK3_SS_VALUE_1     | Buck3 Soft-Start setting :<br>00 : 8.7 V/ms<br>01 : 4.35 V/ms<br>10 : 1.75 V/ms<br>11 : 0.87 V/ms                                                                                                                                                                                                                                                      |
| 5   | BUCK3_SS_VALUE_0     |                                                                                                                                                                                                                                                                                                                                                        |
| 4   | BUCK3_REFRESH_FREQ   | 1: Refresh frequency 1 kHz<br>0: Refresh frequency 25 kHz                                                                                                                                                                                                                                                                                              |
| 3   | CRC 3                |                                                                                                                                                                                                                                                                                                                                                        |
| 2   | CRC 2                |                                                                                                                                                                                                                                                                                                                                                        |
| 1   | CRC 1                |                                                                                                                                                                                                                                                                                                                                                        |

| Bit | Name  | Description |
|-----|-------|-------------|
| 0   | CRC 0 |             |

**Table 143. DCR13 (0x0D) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19                     | Bit 18                     | Bit 17                     | Bit 16                     |
|----------|----------|----------|----------|----------------------------|----------------------------|----------------------------|----------------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)                      | - (R)                      | - (R)                      | - (R)                      |
| RES      | RES      | RES      | RES      | U_NVM_D_15                 | U_NVM_D_14                 | U_NVM_D_13                 | U_NVM_D_12                 |
| Reserved | Reserved | Reserved | Reserved | User NVM D register bit 15 | User NVM D register bit 14 | User NVM D register bit 13 | User NVM D register bit 12 |

**Table 144. DCR13 (0x0D) MSB description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 23  | RES        | Reserved    |
| 22  | RES        | Reserved    |
| 21  | RES        | Reserved    |
| 20  | RES        | Reserved    |
| 19  | U_NVM_D_15 |             |
| 18  | U_NVM_D_14 |             |
| 17  | U_NVM_D_13 |             |
| 16  | U_NVM_D_12 |             |

**Table 145. DCR13 (0x0D)**

| Bit 15                     | Bit 14                     | Bit 13                    | Bit 12                    | Bit 11                    | Bit 10                    | Bit 9                     | Bit 8                     |
|----------------------------|----------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| - (R)                      | - (R)                      | - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                     |
| U_NVM_D_11                 | U_NVM_D_10                 | U_NVM_D_9                 | U_NVM_D_8                 | U_NVM_D_7                 | U_NVM_D_6                 | U_NVM_D_5                 | U_NVM_D_4                 |
| User NVM D register bit 11 | User NVM D register bit 10 | User NVM D register bit 9 | User NVM D register bit 8 | User NVM D register bit 7 | User NVM D register bit 6 | User NVM D register bit 5 | User NVM D register bit 4 |

**Table 146. DCR13 (0x0D) description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 15  | U_NVM_D_11 |             |
| 14  | U_NVM_D_10 |             |
| 13  | U_NVM_D_9  |             |
| 12  | U_NVM_D_8  |             |
| 11  | U_NVM_D_7  |             |
| 10  | U_NVM_D_6  |             |
| 9   | U_NVM_D_5  |             |
| 8   | U_NVM_D_4  |             |

**Table 147. DCR13 (0x0D) LSB**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - (R) | - (R) | - (R) | - (R) | - (R) | - (R) | - (R) | - (R) |

| Bit 7                     | Bit 6                     | Bit 5                     | Bit 4                     | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------------|---------------------------|---------------------------|---------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| U_NVM_D_3                 | U_NVM_D_2                 | U_NVM_D_1                 | U_NVM_D_0                 | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| User NVM D register bit 3 | User NVM D register bit 2 | User NVM D register bit 1 | User NVM D register bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 148. DCR13 (0x0D) LSB description**

| Bit | Name      | Description |
|-----|-----------|-------------|
| 7   | U_NVM_D_3 |             |
| 6   | U_NVM_D_2 |             |
| 5   | U_NVM_D_1 |             |
| 4   | U_NVM_D_0 |             |
| 3   | CRC 3     |             |
| 2   | CRC 2     |             |
| 1   | CRC 1     |             |
| 0   | CRC 0     |             |

**Table 149. DCR14 (0x0E) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19                     | Bit 18                                         | Bit 17             | Bit 16             |
|----------|----------|----------|----------|----------------------------|------------------------------------------------|--------------------|--------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)                      | - (R)                                          | - (R)              | - (R)              |
| RES      | RES      | RES      | RES      | PU_LOOP_FOR_EVER           | LDO2_REGFAIL_GO_REC                            | LDO2_TRK_1         | LDO2_TRK_0         |
| Reserved | Reserved | Reserved | Reserved | Power-up infinite loop bit | LDO2 regulator fail go power-down to REC-2 bit | LDO2 tracker bit 1 | LDO2 tracker bit 0 |

**Table 150. DCR14 (0x0E) MSB description**

| Bit | Name                | Description                                                                                                                                                                                                                                                                                                                                          |
|-----|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES                 | Reserved                                                                                                                                                                                                                                                                                                                                             |
| 22  | RES                 | Reserved                                                                                                                                                                                                                                                                                                                                             |
| 21  | RES                 | Reserved                                                                                                                                                                                                                                                                                                                                             |
| 20  | RES                 | Reserved                                                                                                                                                                                                                                                                                                                                             |
| 19  | PU_LOOP_FOR_EVER    | 1: retry loop activated for ever in case of fault detection<br>0: retry loop of 4 before entering in DEEP-SLEEP in case of fault detection                                                                                                                                                                                                           |
| 18  | LDO2_REGFAIL_GO_REC | 1: A fail on LDO2 regulator initiates a power-down sequence and moves the state machine to REC-2 state<br>0: A fail on LDO2 regulator sends an IRQ (UV, OV, PG_nok, TW are maskable by SPI, but not TSD), and turns the regulator OFF if the fail is unmasked (UV, PG_nok are maskable by SPI, but not OV and TSD. TW never turns the regulator OFF) |
| 17  | LDO2_TRK_1          | 00: BUCK1 (only if BUCK1 output voltage is 3.3 V or 5 V otherwise LDO2 OFF)<br>01: BUCK2 (only if BUCK2 output voltage is 3.3 V or 5 V otherwise LDO2 OFF)<br>1x: BUCK3 (only if BUCK3 output voltage is 3.3 V otherwise LDO2 OFF)                                                                                                                   |
| 16  | LDO2_TRK_0          |                                                                                                                                                                                                                                                                                                                                                      |

**Table 151. DCR14 (0x0E)**

| Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
|--------|--------|--------|--------|--------|--------|-------|-------|
| - (R)  | - (R)  | - (R)  | - (R)  | - (R)  | - (R)  | - (R) | - (R) |

| Bit 15                         | Bit 14                         | Bit 13                         | Bit 12                           | Bit 11                           | Bit 10                           | Bit 9                          | Bit 8                          |
|--------------------------------|--------------------------------|--------------------------------|----------------------------------|----------------------------------|----------------------------------|--------------------------------|--------------------------------|
| LDO2_PD_STEP_OFF_2             | LDO2_PD_STEP_OFF_1             | LDO2_PD_STEP_OFF_0             | LDO2_PU_STEP_ENA_2               | LDO2_PU_STEP_ENA_1               | LDO2_PU_STEP_ENA_0               | LDO1_PD_STEP_OFF_2             | LDO1_PD_STEP_OFF_1             |
| LDO2 Power-Down step off bit 2 | LDO2 Power-Down step off bit 1 | LDO2 Power-Down step off bit 0 | LDO2 Power-Up step enables bit 2 | LDO2 Power-Up step enables bit 1 | LDO2 Power-Up step enables bit 0 | LDO1 Power-Down step off bit 2 | LDO1 Power-Down step off bit 1 |

**Table 152. DCR14 (0x0E) description**

| Bit | Name               | Description                                                                                                                                                         |
|-----|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | LDO2_PD_STEP_OFF_2 | To define LDO2 turn-off steps<br>000: Step 1<br>001: Step 2<br>010: Step 3<br>011: Step 4<br>100: Step 5<br>101: Step 6<br>11X: Step 7                              |
| 14  | LDO2_PD_STEP_OFF_1 |                                                                                                                                                                     |
| 13  | LDO2_PD_STEP_OFF_0 |                                                                                                                                                                     |
| 12  | LDO2_PU_STEP_ENA_2 | To define LDO2 turn-on steps<br>000: LDO2 is not turned ON<br>001: Step 1<br>010: Step 2<br>011: Step 3<br>100: Step 4<br>101: Step 5<br>110: Step 6<br>111: Step 7 |
| 11  | LDO2_PU_STEP_ENA_1 |                                                                                                                                                                     |
| 10  | LDO2_PU_STEP_ENA_0 |                                                                                                                                                                     |
| 9   | LDO1_PD_STEP_OFF_2 | To define LDO1 turn-off steps<br>000: Step 1<br>001: Step 2<br>010: Step 3<br>011: Step 4<br>100: Step 5<br>101: Step 6<br>11X: Step 7                              |
| 8   | LDO1_PD_STEP_OFF_1 |                                                                                                                                                                     |

**Table 153. DCR14 (0x0E) LSB**

| Bit 7                      | Bit 6                    | Bit 5                    | Bit 4                    | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|----------------------------|--------------------------|--------------------------|--------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)                      | - (R)                    | - (R)                    | - (R)                    | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| LDO1_PD_STEP_OFF_0         | LDO1_PU_STEP_ENA_2       | LDO1_PU_STEP_ENA_1       | LDO1_PU_STEP_ENA_0       | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| LDO1 Power-Down step bit 0 | LDO1 Power-Up step bit 2 | LDO1 Power-Up step bit 1 | LDO1 Power-Up step bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 154. DCR14 (0x0E) LSB description**

| Bit | Name               | Description                                                                                                                                                         |
|-----|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | LDO1_PD_STEP_OFF_0 |                                                                                                                                                                     |
| 6   | LDO1_PU_STEP_ENA_2 | To define LDO1 turn-on steps<br>000: LDO1 is not turned ON<br>001: Step 1<br>010: Step 2<br>011: Step 3<br>100: Step 4<br>101: Step 5<br>110: Step 6<br>111: Step 7 |
| 5   | LDO1_PU_STEP_ENA_1 |                                                                                                                                                                     |
| 4   | LDO1_PU_STEP_ENA_0 |                                                                                                                                                                     |
| 3   | CRC 3              |                                                                                                                                                                     |
| 2   | CRC 2              |                                                                                                                                                                     |
| 1   | CRC 1              |                                                                                                                                                                     |
| 0   | CRC 0              |                                                                                                                                                                     |

**Table 155. DCR15 (0x0F) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19                     | Bit 18                     | Bit 17                         | Bit 16                         |
|----------|----------|----------|----------|----------------------------|----------------------------|--------------------------------|--------------------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)                      | - (R)                      | - (R)                          | - (R)                          |
| RES      | RES      | RES      | RES      | U_NVM_F_15                 | U_NVM_F_14                 | PU_WAIT_DEL_ENA_7_1            | PU_WAIT_DEL_ENA_7_0            |
| Reserved | Reserved | Reserved | Reserved | User NVM F register bit 15 | User NVM F register bit 14 | Power-up delay at step 7 bit 1 | Power-up delay at step 7 bit 0 |

**Table 156. DCR15 (0x0F) MSB description**

| Bit | Name                | Description                                                               |
|-----|---------------------|---------------------------------------------------------------------------|
| 23  | RES                 | Reserved                                                                  |
| 22  | RES                 | Reserved                                                                  |
| 21  | RES                 | Reserved                                                                  |
| 20  | RES                 | Reserved                                                                  |
| 19  | U_NVM_F_15          |                                                                           |
| 18  | U_NVM_F_14          |                                                                           |
| 17  | PU_WAIT_DEL_ENA_7_1 | Power-up delay at step 7<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 16  | PU_WAIT_DEL_ENA_7_0 |                                                                           |

**Table 157. DCR15 (0x0F)**

| Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
|--------|--------|--------|--------|--------|--------|-------|-------|
| - (R)  | - (R)  | - (R)  | - (R)  | - (R)  | - (R)  | - (R) | - (R) |

| Bit 15                         | Bit 14                         | Bit 13                         | Bit 12                         | Bit 11                         | Bit 10                         | Bit 9                          | Bit 8                          |
|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| PU_WAIT_DEL_ENA_6_1            | PU_WAIT_DEL_ENA_6_0            | PU_WAIT_DEL_ENA_5_1            | PU_WAIT_DEL_ENA_5_0            | PU_WAIT_DEL_ENA_4_1            | PU_WAIT_DEL_ENA_4_0            | PU_WAIT_DEL_ENA_3_1            | PU_WAIT_DEL_ENA_3_0            |
| Power-up delay at step 6 bit 1 | Power-up delay at step 6 bit 0 | Power-up delay at step 5 bit 1 | Power-up delay at step 5 bit 0 | Power-up delay at step 4 bit 1 | Power-up delay at step 4 bit 0 | Power-up delay at step 3 bit 1 | Power-up delay at step 3 bit 0 |

**Table 158. DCR15 (0x0F) description**

| Bit | Name                | Description                                                               |
|-----|---------------------|---------------------------------------------------------------------------|
| 15  | PU_WAIT_DEL_ENA_6_1 | Power-up delay at step 6<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 14  | PU_WAIT_DEL_ENA_6_0 |                                                                           |
| 13  | PU_WAIT_DEL_ENA_5_1 | Power-up delay at step 5<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 12  | PU_WAIT_DEL_ENA_5_0 |                                                                           |
| 11  | PU_WAIT_DEL_ENA_4_1 | Power-up delay at step 4<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 10  | PU_WAIT_DEL_ENA_4_0 |                                                                           |
| 9   | PU_WAIT_DEL_ENA_3_1 | Power-up delay at step 3<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 8   | PU_WAIT_DEL_ENA_3_0 |                                                                           |

**Table 159. DCR15 (0x0F) LSB**

| Bit 7                          | Bit 6                          | Bit 5                          | Bit 4                          | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|--------------------------------|--------------------------------|--------------------------------|--------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)                          | - (R)                          | - (R)                          | - (R)                          | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| PU_WAIT_DEL_ENA_2_1            | PU_WAIT_DEL_ENA_2_0            | PU_WAIT_DEL_ENA_1_1            | PU_WAIT_DEL_ENA_1_0            | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Power-up delay at step 2 bit 1 | Power-up delay at step 2 bit 0 | Power-up delay at step 1 bit 1 | Power-up delay at step 1 bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 160. DCR15 (0x0F) LSB description**

| Bit | Name                | Description                                                  |
|-----|---------------------|--------------------------------------------------------------|
| 7   | PU_WAIT_DEL_ENA_2_1 | Power-up delay at step 2<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms |

| Bit | Name                | Description                                                               |
|-----|---------------------|---------------------------------------------------------------------------|
|     |                     | 11: 10 ms                                                                 |
| 6   | PU_WAIT_DEL_ENA_2_0 |                                                                           |
| 5   | PU_WAIT_DEL_ENA_1_1 | Power-up delay at step 1<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 4   | PU_WAIT_DEL_ENA_1_0 |                                                                           |
| 3   | CRC 3               |                                                                           |
| 2   | CRC 2               |                                                                           |
| 1   | CRC 1               |                                                                           |
| 0   | CRC 0               |                                                                           |

**Table 161. DCR16 (0x10) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19                     | Bit 18                     | Bit 17                     | Bit 16                      |
|----------|----------|----------|----------|----------------------------|----------------------------|----------------------------|-----------------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)                      | - (R)                      | - (R)                      | - (R)                       |
| RES      | RES      | RES      | RES      | U_NVM_G_15                 | U_NVM_G_14                 | U_NVM_G_13                 | NRESET_PD_STEP_ASSERT_2     |
| Reserved | Reserved | Reserved | Reserved | User NVM G register bit 15 | User NVM G register bit 14 | User NVM G register bit 13 | NRESET assertion step bit 2 |

**Table 162. DCR16 (0x10) MSB description**

| Bit | Name                    | Description                                                                                                                              |
|-----|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES                     | Reserved                                                                                                                                 |
| 22  | RES                     | Reserved                                                                                                                                 |
| 21  | RES                     | Reserved                                                                                                                                 |
| 20  | RES                     | Reserved                                                                                                                                 |
| 19  | U_NVM_G_15              |                                                                                                                                          |
| 18  | U_NVM_G_14              |                                                                                                                                          |
| 17  | U_NVM_G_13              |                                                                                                                                          |
| 16  | NRESET_PD_STEP_ASSERT_2 | To define NRESET assertion step<br>000: Step 1<br>001: Step 2<br>010: Step 3<br>011: Step 4<br>100: Step 5<br>101: Step 6<br>11x: Step 7 |

**Table 163. DCR16 (0x10)**

| Bit 15                      | Bit 14                      | Bit 13                         | Bit 12                         | Bit 11                         | Bit 10                        | Bit 9                         | Bit 8                         |
|-----------------------------|-----------------------------|--------------------------------|--------------------------------|--------------------------------|-------------------------------|-------------------------------|-------------------------------|
| - (R)                       | - (R)                       | - (R)                          | - (R)                          | - (R)                          | - (R)                         | - (R)                         | - (R)                         |
| NRESET_PD_STEP_ASSERT_1     | NRESET_PD_STEP_ASSERT_0     | NRESET_PU_STEP_DEASSERT_2      | NRESET_PU_STEP_DEASSERT_1      | NRESET_PU_STEP_DEASSERT_0      | PU_WAIT_PG_ENA_7              | PU_WAIT_PG_ENA_6              | PU_WAIT_PG_ENA_5              |
| NRESET assertion step bit 1 | NRESET assertion step bit 0 | NRESET de-assertion step bit 2 | NRESET de-assertion step bit 1 | NRESET de-assertion step bit 0 | Wait for power-good in step 7 | Wait for power-good in step 6 | Wait for power-good in step 5 |

**Table 164. DCR16 (0x10) description**

| Bit | Name                      | Description                                                                                                                                                                   |
|-----|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | NRESET_PD_STEP_ASSERT_1   |                                                                                                                                                                               |
| 14  | NRESET_PD_STEP_ASSERT_0   |                                                                                                                                                                               |
| 13  | NRESET_PU_STEP_DEASSERT_2 | To define NRESET deassertion and WD start step<br>000: End of step 7<br>001: Step 1<br>010: Step 2<br>011: Step 3<br>100: Step 4<br>101: Step 5<br>110: Step 6<br>111: Step 7 |
| 12  | NRESET_PU_STEP_DEASSERT_1 |                                                                                                                                                                               |
| 11  | NRESET_PU_STEP_DEASSERT_0 |                                                                                                                                                                               |
| 10  | PU_WAIT_PG_ENA_7          | 1: At power-up step 7, wait for power-good signal<br>0: At power-up step 7, no wait for power-good signal                                                                     |
| 9   | PU_WAIT_PG_ENA_6          | 1: At power-up step 6, wait for power-good signal<br>0: At power-up step 6, no wait for power-good signal                                                                     |
| 8   | PU_WAIT_PG_ENA_5          | 1: At power-up step 5, wait for power-good signal<br>0: At power-up step 5, no wait for power-good signal                                                                     |

**Table 165. DCR16 (0x10) LSB**

| Bit 7                         | Bit 6                         | Bit 5                         | Bit 4                         | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-------------------------------|-------------------------------|-------------------------------|-------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)                         | - (R)                         | - (R)                         | - (R)                         | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| PU_WAIT_PG_ENA_4              | PU_WAIT_PG_ENA_3              | PU_WAIT_PG_ENA_2              | PU_WAIT_PG_ENA_1              | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Wait for power-good in step 4 | Wait for power-good in step 3 | Wait for power-good in step 2 | Wait for power-good in step 1 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 166. DCR16 (0x10) LSB description**

| Bit | Name             | Description                                                                                               |
|-----|------------------|-----------------------------------------------------------------------------------------------------------|
| 7   | PU_WAIT_PG_ENA_4 | 1: At power-up step 4, wait for power-good signal<br>0: At power-up step 4, no wait for power-good signal |
| 6   | PU_WAIT_PG_ENA_3 | 1: At power-up step 3, wait for power-good signal<br>0: At power-up step 3, no wait for power-good signal |
| 5   | PU_WAIT_PG_ENA_2 | 1: At power-up step 2, wait for power-good signal<br>0: At power-up step 2, no wait for power-good signal |
| 4   | PU_WAIT_PG_ENA_1 | 1: At power-up step 1, wait for power-good signal<br>0: At power-up step 1, no wait for power-good signal |
| 3   | CRC 3            |                                                                                                           |
| 2   | CRC 2            |                                                                                                           |
| 1   | CRC 1            |                                                                                                           |

| Bit | Name  | Description |
|-----|-------|-------------|
| 0   | CRC 0 |             |

**Table 167. DCR17 (0x11) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19               | Bit 18               | Bit 17               | Bit 16               |
|----------|----------|----------|----------|----------------------|----------------------|----------------------|----------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)                | - (R)                | - (R)                | - (R)                |
| RES      | RES      | RES      | RES      | U_NVM_CRC0_7         | U_NVM_CRC0_6         | U_NVM_CRC0_5         | U_NVM_CRC0_4         |
| Reserved | Reserved | Reserved | Reserved | User NVM CRC 0 bit 7 | User NVM CRC 0 bit 6 | User NVM CRC 0 bit 5 | User NVM CRC 0 bit 4 |

**Table 168. DCR17 (0x11) MSB description**

| Bit | Name         | Description |
|-----|--------------|-------------|
| 23  | RES          | Reserved    |
| 22  | RES          | Reserved    |
| 21  | RES          | Reserved    |
| 20  | RES          | Reserved    |
| 19  | U_NVM_CRC0_7 |             |
| 18  | U_NVM_CRC0_6 |             |
| 17  | U_NVM_CRC0_5 |             |
| 16  | U_NVM_CRC0_4 |             |

**Table 169. DCR17 (0x11)**

| Bit 15               | Bit 14               | Bit 13               | Bit 12               | Bit 11               | Bit 10               | Bit 9                     | Bit 8                     |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|---------------------------|---------------------------|
| - (R)                | - (R)                | - (R)                | - (R)                | - (R)                | - (R)                | - (R)                     | - (R)                     |
| U_NVM_CRC0_3         | U_NVM_CRC0_2         | U_NVM_CRC0_1         | U_NVM_CRC0_0         | U_PROG0_1            | U_PROG0_0            | U_NVM_H_5                 | U_NVM_H_4                 |
| User NVM CRC 0 bit 3 | User NVM CRC 0 bit 2 | User NVM CRC 0 bit 1 | User NVM CRC 0 bit 0 | User program 0 bit 1 | User program 0 bit 0 | User NVM H register bit 5 | User NVM H register bit 4 |

**Table 170. DCR17 (0x11) description**

| Bit | Name         | Description                                                                     |
|-----|--------------|---------------------------------------------------------------------------------|
| 15  | U_NVM_CRC0_3 |                                                                                 |
| 14  | U_NVM_CRC0_2 |                                                                                 |
| 13  | U_NVM_CRC0_1 |                                                                                 |
| 12  | U_NVM_CRC0_0 |                                                                                 |
| 11  | U_PROG0_1    | Not accessible by user but programmed by NVM controller during user programming |
| 10  | U_PROG0_0    | Not accessible by user but programmed by NVM controller during user programming |
| 9   | U_NVM_H_5    |                                                                                 |
| 8   | U_NVM_H_4    |                                                                                 |

**Table 171. DCR17 (0x11) LSB**

| Bit 7                    | Bit 6     | Bit 5     | Bit 4     | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------------------|-----------|-----------|-----------|-------|-------|-------|-------|
| - (R)                    | - (R)     | - (R)     | - (R)     | - (R) | - (R) | - (R) | - (R) |
| NFSO_STATE_IN_DEEP_SLEEP | U_NVM_H_2 | U_NVM_H_1 | BOOST_DIS | CRC3  | CRC2  | CRC1  | CRC0  |

| Bit 7                                | Bit 6                     | Bit 5                     | Bit 4             | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|--------------------------------------|---------------------------|---------------------------|-------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| NFSO default state in DEEP-SLEEP bit | User NVM H register bit 2 | User NVM H register bit 1 | BOOST disable bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 172. DCR17 (0x11) LSB description**

| Bit | Name                     | Description                                                                                               |
|-----|--------------------------|-----------------------------------------------------------------------------------------------------------|
| 7   | NFSO_STATE_IN_DEEP_SLEEP | 1: NFSO pin is high when FSM is in DEEP-SLEEP state<br>0: NFSO pin is low when FSM is in DEEP-SLEEP state |
| 6   | U_NVM_H_2                |                                                                                                           |
| 5   | U_NVM_H_1                |                                                                                                           |
| 4   | BOOST_DIS                | 1: Disable boost<br>0: Boost is not disabled and depends on BOOST_OFF control bit                         |
| 3   | CRC 3                    |                                                                                                           |
| 2   | CRC 2                    |                                                                                                           |
| 1   | CRC 1                    |                                                                                                           |
| 0   | CRC 0                    |                                                                                                           |

**Table 173. DCR18 (0x12) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19                                     | Bit 18                                     | Bit 17                           | Bit 16                           |
|----------|----------|----------|----------|--------------------------------------------|--------------------------------------------|----------------------------------|----------------------------------|
| -(R0)    | -(R0)    | -(R0)    | -(R0)    | -(R)                                       | -(R)                                       | -(R)                             | -(R)                             |
| RES      | RES      | RES      | RES      | PD_WAIT_VREG_DEL_OFF_1                     | PD_WAIT_VREG_DEL_OFF_0                     | PD_WAIT_DEL_OFF_7_1              | PD_WAIT_DEL_OFF_7_0              |
| Reserved | Reserved | Reserved | Reserved | Power-down delay prior VREG turn-off bit 1 | Power-down delay prior VREG turn-off bit 0 | Power-down delay at step 7 bit 1 | Power-down delay at step 7 bit 0 |

**Table 174. DCR18 (0x12) MSB description**

| Bit | Name                   | Description                                                                 |
|-----|------------------------|-----------------------------------------------------------------------------|
| 23  | RES                    | Reserved                                                                    |
| 22  | RES                    | Reserved                                                                    |
| 21  | RES                    | Reserved                                                                    |
| 20  | RES                    | Reserved                                                                    |
| 19  | PD_WAIT_VREG_DEL_OFF_1 | Power-down delay for VREG<br>00: 2 ms<br>01: 5 ms<br>10: 10 ms<br>11: 20 ms |
| 18  | PD_WAIT_VREG_DEL_OFF_0 |                                                                             |
| 17  | PD_WAIT_DEL_OFF_7_1    | Power-down delay at step 7<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 16  | PD_WAIT_DEL_OFF_7_0    |                                                                             |

**Table 175. DCR18 (0x12)**

| Bit 15                           | Bit 14                           | Bit 13                           | Bit 12                           | Bit 11                           | Bit 10                           | Bit 9                            | Bit 8                            |
|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| -(R)                             | -(R)                             | -(R)                             | -(R)                             | -(R)                             | -(R)                             | -(R)                             | -(R)                             |
| PD_WAIT_DEL_OFF_6_1              | PD_WAIT_DEL_OFF_6_0              | PD_WAIT_DEL_OFF_5_1              | PD_WAIT_DEL_OFF_5_0              | PD_WAIT_DEL_OFF_4_1              | PD_WAIT_DEL_OFF_4_0              | PD_WAIT_DEL_OFF_3_1              | PD_WAIT_DEL_OFF_3_0              |
| Power-down delay at step 6 bit 1 | Power-down delay at step 6 bit 0 | Power-down delay at step 5 bit 1 | Power-down delay at step 5 bit 0 | Power-down delay at step 4 bit 1 | Power-down delay at step 4 bit 0 | Power-down delay at step 3 bit 1 | Power-down delay at step 3 bit 0 |

**Table 176. DCR18 (0x12) description**

| Bit | Name                | Description                                                                 |
|-----|---------------------|-----------------------------------------------------------------------------|
| 15  | PD_WAIT_DEL_OFF_6_1 | Power-down delay at step 6<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 14  | PD_WAIT_DEL_OFF_6_0 |                                                                             |
| 13  | PD_WAIT_DEL_OFF_5_1 | Power-down delay at step 5<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 12  | PD_WAIT_DEL_OFF_5_0 |                                                                             |
| 11  | PD_WAIT_DEL_OFF_4_1 | Power-down delay at step 4<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 10  | PD_WAIT_DEL_OFF_4_0 |                                                                             |
| 9   | PD_WAIT_DEL_OFF_3_1 | Power-down delay at step 3<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 8   | PD_WAIT_DEL_OFF_3_0 |                                                                             |

**Table 177. DCR18 (0x12) LSB**

| Bit 7                            | Bit 6                            | Bit 5                            | Bit 4                            | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| -(R)                             | -(R)                             | -(R)                             | -(R)                             | -(R)                             | -(R)                             | -(R)                             | -(R)                             |
| PD_WAIT_DEL_OFF_2_1              | PD_WAIT_DEL_OFF_2_0              | PD_WAIT_DEL_OFF_1_1              | PD_WAIT_DEL_OFF_1_0              | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Power-down delay at step 2 bit 1 | Power-down delay at step 2 bit 0 | Power-down delay at step 1 bit 1 | Power-down delay at step 1 bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 178. DCR18 (0x12) LSB description**

| Bit | Name                | Description                                                                 |
|-----|---------------------|-----------------------------------------------------------------------------|
| 7   | PD_WAIT_DEL_OFF_2_1 | Power-down delay at step 2<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 6   | PD_WAIT_DEL_OFF_2_0 |                                                                             |
| 5   | PD_WAIT_DEL_OFF_1_1 | Power-down delay at step 1<br>00: 0 ms<br>01: 2 ms<br>10: 5 ms<br>11: 10 ms |
| 4   | PD_WAIT_DEL_OFF_1_0 |                                                                             |
| 3   | CRC 3               |                                                                             |
| 2   | CRC 2               |                                                                             |
| 1   | CRC 1               |                                                                             |
| 0   | CRC 0               |                                                                             |

**Table 179. DCR19 (0x13) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19                  | Bit 18                  | Bit 17                  | Bit 16                  |
|----------|----------|----------|----------|-------------------------|-------------------------|-------------------------|-------------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)                   | - (R)                   | - (R)                   | - (R)                   |
| RES      | RES      | RES      | RES      | U_NVM_RELEASE_15        | U_NVM_RELEASE_14        | U_NVM_RELEASE_13        | U_NVM_RELEASE_12        |
| Reserved | Reserved | Reserved | Reserved | User NVM release bit 15 | User NVM release bit 14 | User NVM release bit 13 | User NVM release bit 12 |

**Table 180. DCR19 (0x13) MSB description**

| Bit | Name             | Description                                           |
|-----|------------------|-------------------------------------------------------|
| 23  | RES              | Reserved                                              |
| 22  | RES              | Reserved                                              |
| 21  | RES              | Reserved                                              |
| 20  | RES              | Reserved                                              |
| 19  | U_NVM_RELEASE_15 | Available for customer to define the user NVM release |
| 18  | U_NVM_RELEASE_14 |                                                       |
| 17  | U_NVM_RELEASE_13 |                                                       |
| 16  | U_NVM_RELEASE_12 |                                                       |

**Table 181. DCR19 (0x13)**

| Bit 15                  | Bit 14                  | Bit 13                 | Bit 12                 | Bit 11                 | Bit 10                 | Bit 9                  | Bit 8                  |
|-------------------------|-------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| - (R)                   | - (R)                   | - (R)                  | - (R)                  | - (R)                  | - (R)                  | - (R)                  | - (R)                  |
| U_NVM_RELEASE_11        | U_NVM_RELEASE_10        | U_NVM_RELEASE_9        | U_NVM_RELEASE_8        | U_NVM_RELEASE_7        | U_NVM_RELEASE_6        | U_NVM_RELEASE_5        | U_NVM_RELEASE_4        |
| User NVM release bit 11 | User NVM release bit 10 | User NVM release bit 9 | User NVM release bit 8 | User NVM release bit 7 | User NVM release bit 6 | User NVM release bit 5 | User NVM release bit 4 |

**Table 182. DCR19 (0x13) description**

| Bit | Name             | Description |
|-----|------------------|-------------|
| 15  | U_NVM_RELEASE_11 |             |
| 14  | U_NVM_RELEASE_10 |             |
| 13  | U_NVM_RELEASE_9  |             |
| 12  | U_NVM_RELEASE_8  |             |
| 11  | U_NVM_RELEASE_7  |             |
| 10  | U_NVM_RELEASE_6  |             |
| 9   | U_NVM_RELEASE_5  |             |
| 8   | U_NVM_RELEASE_4  |             |

**Table 183. DCR19 (0x13) LSB**

| Bit 7                  | Bit 6                  | Bit 5                  | Bit 4                  | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|------------------------|------------------------|------------------------|------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)                  | - (R)                  | - (R)                  | - (R)                  | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| U_NVM_RELEASE_3        | U_NVM_RELEASE_2        | U_NVM_RELEASE_1        | U_NVM_RELEASE_0        | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| User NVM release bit 3 | User NVM release bit 2 | User NVM release bit 1 | User NVM release bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 184. DCR19 (0x13) LSB description**

| Bit | Name            | Description |
|-----|-----------------|-------------|
| 7   | U_NVM_RELEASE_3 |             |
| 6   | U_NVM_RELEASE_2 |             |
| 5   | U_NVM_RELEASE_1 |             |
| 4   | U_NVM_RELEASE_0 |             |
| 3   | CRC 3           |             |
| 2   | CRC 2           |             |
| 1   | CRC 1           |             |
| 0   | CRC 0           |             |

**Table 185. DCR20 (0x14) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19                           | Bit 18                           | Bit 17                                | Bit 16                               |
|----------|----------|----------|----------|----------------------------------|----------------------------------|---------------------------------------|--------------------------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)                            | - (R)                            | - (R)                                 | - (R)                                |
| RES      | RES      | RES      | RES      | FBB_OK_SEL_1                     | FBB_OK_SEL_0                     | BYPASS_OFFSET_SEL                     | FBB_REG_LEVEL_SEL_1                  |
| Reserved | Reserved | Reserved | Reserved | FBB OK threshold selection Bit 1 | FBB OK threshold selection Bit 0 | VTH_BYPASS threshold offset selection | FBB Regulation level selection bit 1 |

**Table 186. DCR20 (0x14) MSB description**

| Bit | Name         | Description                                        |
|-----|--------------|----------------------------------------------------|
| 23  | RES          | Reserved                                           |
| 22  | RES          | Reserved                                           |
| 21  | RES          | Reserved                                           |
| 20  | RES          | Reserved                                           |
| 19  | FBB_OK_SEL_1 | To add flexibility on FBB_OK threshold selection : |

| Bit | Name                | Description                                                                                     |
|-----|---------------------|-------------------------------------------------------------------------------------------------|
|     |                     | 00 : 5.5 V<br>01 : 6.5 V<br>10 : 7.5 V<br>11 : 8.5 V                                            |
| 18  | FBB_OK_SEL_0        |                                                                                                 |
| 17  | BYPASS_OFFSET_SEL   | VTH_BYPASS threshold offset selection<br>1: FBB_REG_LEVEL + 1.0 V<br>0: FBB_REG_LEVEL + 0.5 V   |
| 16  | FBB_REG_LEVEL_SEL_1 | To add flexibility on FBB_REG level selection :<br>00 : 6 V<br>01 : 7 V<br>10 : 8 V<br>11 : 9 V |

**Table 187. DCR20 (0x14)**

| Bit 15                               | Bit 14                                                        | Bit 13                             | Bit 12                             | Bit 11                             | Bit 10                           | Bit 9                              | Bit 8                              |
|--------------------------------------|---------------------------------------------------------------|------------------------------------|------------------------------------|------------------------------------|----------------------------------|------------------------------------|------------------------------------|
| ~ (R)                                | ~ (R)                                                         | ~ (R)                              | ~ (R)                              | ~ (R)                              | ~ (R)                            | ~ (R)                              | ~ (R)                              |
| FBB_REG_LEVEL_SEL_0                  | WAKEUP_GO_TO_DEEP_SLEEP_INH                                   | BOOST_CRK_TO_2                     | BOOST_CRK_TO_1                     | BOOST_CRK_TO_0                     | BOOST_CRK_ONLY                   | VS_SENSE_LEVEL_SEL_1               | VS_SENSE_LEVEL_SEL_0               |
| FBB Regulation level selection bit 0 | Inhibit transition to Deep Sleep if a wake up flag is present | Boost timer duration setting Bit 2 | Boost timer duration setting Bit 1 | Boost timer duration setting Bit 0 | Boost activation during cranking | VS SENSE threshold selection Bit 1 | VS SENSE threshold selection Bit 0 |

**Table 188. DCR20 (0x14) description**

| Bit | Name                        | Description                                                                                                                                                                                              |
|-----|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | FBB_REG_LEVEL_SEL_0         |                                                                                                                                                                                                          |
| 14  | WAKEUP_GO_TO_DEEP_SLEEP_INH |                                                                                                                                                                                                          |
| 13  | BOOST_CRK_TO_2              | To add flexibility on Boost timeout duration selection when $V_S < V_{S\_SENSE}$ :<br>000 : no boost timer<br>001 : 0.5 s<br>010 : 1 s<br>011 : 2 s<br>100 : 4 s<br>101 : 6 s<br>110 : 8 s<br>111 : 10 s |
| 12  | BOOST_CRK_TO_1              |                                                                                                                                                                                                          |
| 11  | BOOST_CRK_TO_0              |                                                                                                                                                                                                          |
| 10  | BOOST_CRK_ONLY              | Selection bit to activate boost only when $V_S < V_{S\_SENSE}$<br>1 : Boost activation in cranking mode enabled<br>0 : Boost activation in cranking mode disabled                                        |
| 9   | VS_SENSE_LEVEL_SEL_1        | To add flexibility on VS_SENSE_LEVEL level selection :<br>00 : 5.4 V<br>01 : 5.55 V<br>10 : 5.7 V<br>11 : 5.85 V                                                                                         |

| Bit | Name                 | Description |
|-----|----------------------|-------------|
| 8   | VS_SENSE_LEVEL_SEL_0 |             |

**Table 189. DCR20 (0x14) LSB**

| Bit 7         | Bit 6         | Bit 5         | Bit 4         | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------|---------------|---------------|---------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)         | - (R)         | - (R)         | - (R)         | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| LOW_SET_3     | LOW_SET_2     | LOW_SET_1     | LOW_SET_0     | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| LOW set bit 3 | LOW set bit 2 | LOW set bit 1 | LOW set bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 190. DCR20 (0x14) LSB description**

| Bit | Name      | Description                                                                                                                                                                                                                                                                                          |
|-----|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | LOW_SET_3 | Long open window setting<br>0000: 319 ms max<br>0001: 479 ms max<br>0010: 638 ms max<br>0011: 1025 ms max<br>0100: 115 ms max<br>0101: 159 ms max<br>0110: 230 ms max<br>0111: 460 ms max<br>1000-1011: 2300 ms max<br>1100: 4600 ms max<br>1101: 6900 ms max<br>1110: 9200 ms max<br>1111: Infinite |
| 6   | LOW_SET_2 |                                                                                                                                                                                                                                                                                                      |
| 5   | LOW_SET_1 |                                                                                                                                                                                                                                                                                                      |
| 4   | LOW_SET_0 |                                                                                                                                                                                                                                                                                                      |
| 3   | CRC 3     |                                                                                                                                                                                                                                                                                                      |
| 2   | CRC 2     |                                                                                                                                                                                                                                                                                                      |
| 1   | CRC 1     |                                                                                                                                                                                                                                                                                                      |
| 0   | CRC 0     |                                                                                                                                                                                                                                                                                                      |

**Table 191. DCR21 (0x15) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19                     | Bit 18                     | Bit 17                     | Bit 16                     |
|----------|----------|----------|----------|----------------------------|----------------------------|----------------------------|----------------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)                      | - (R)                      | - (R)                      | - (R)                      |
| RES      | RES      | RES      | RES      | U_NVM_L_15                 | U_NVM_L_14                 | U_NVM_L_13                 | U_NVM_L_12                 |
| Reserved | Reserved | Reserved | Reserved | User NVM L register bit 15 | User NVM L register bit 14 | User NVM L register bit 13 | User NVM L register bit 12 |

**Table 192. DCR21 (0x15) MSB description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 23  | RES        | Reserved    |
| 22  | RES        | Reserved    |
| 21  | RES        | Reserved    |
| 20  | RES        | Reserved    |
| 19  | U_NVM_L_15 |             |
| 18  | U_NVM_L_14 |             |
| 17  | U_NVM_L_13 |             |
| 16  | U_NVM_L_12 |             |

**Table 193. DCR21 (0x15)**

| Bit 15                     | Bit 14                     | Bit 13                    | Bit 12                    | Bit 11                    | Bit 10                    | Bit 9                     | Bit 8                     |
|----------------------------|----------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| - (R)                      | - (R)                      | - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                     |
| U_NVM_L_11                 | U_NVM_L_10                 | U_NVM_L_9                 | U_NVM_L_8                 | U_NVM_L_7                 | U_NVM_L_6                 | U_NVM_L_5                 | U_NVM_L_4                 |
| User NVM L register bit 11 | User NVM L register bit 10 | User NVM L register bit 9 | User NVM L register bit 8 | User NVM L register bit 7 | User NVM L register bit 6 | User NVM L register bit 5 | User NVM L register bit 4 |

**Table 194. DCR21 (0x15) description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 15  | U_NVM_L_11 |             |
| 14  | U_NVM_L_10 |             |
| 13  | U_NVM_L_9  |             |
| 12  | U_NVM_L_8  |             |
| 11  | U_NVM_L_7  |             |
| 10  | U_NVM_L_6  |             |
| 9   | U_NVM_L_5  |             |
| 8   | U_NVM_L_4  |             |

**Table 195. DCR21 (0x15) LSB**

| Bit 7                     | Bit 6                     | Bit 5                                  | Bit 4                      | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------------|---------------------------|----------------------------------------|----------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R0)                    | - (R0)                    | - (R)                                  | - (R)                      | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| U_NVM_L_3                 | U_NVM_L_2                 | FBB_UV_EW_PD                           | FBB_UV_LEVEL_SEL           | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| User NVM L Register Bit 3 | User NVM L Register Bit 2 | Power-Down execution done by FBB_UV_EW | FBB_UV threshold selection | Cyclic Redundancy Checking Bit 3 | Cyclic Redundancy Checking Bit 2 | Cyclic Redundancy Checking Bit 1 | Cyclic Redundancy Checking Bit 0 |

**Table 196. DCR21 (0x15) LSB description**

| Bit | Name         | Description                                                                                     |
|-----|--------------|-------------------------------------------------------------------------------------------------|
| 7   | U_NVM_L_3    |                                                                                                 |
| 6   | U_NVM_L_2    |                                                                                                 |
| 5   | FBB_UV_EW_PD | Selection bit to execute Power Down when FBB < FBB_UV_EW<br>1 : Power Down when FBB < FBB_UV_EW |

| Bit | Name             | Description                                                               |
|-----|------------------|---------------------------------------------------------------------------|
|     |                  | 0 : Power Down when FBB < FBB_UV_F                                        |
| 4   | FBB_UV_LEVEL_SEL | To add flexibility on FBB_UV level selection :<br>1 : 5.8 V<br>0 : 5.25 V |
| 3   | CRC 3            |                                                                           |
| 2   | CRC 2            |                                                                           |
| 1   | CRC 1            |                                                                           |
| 0   | CRC 0            |                                                                           |

**Table 197. DCR22 (0x16) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19                     | Bit 18                     | Bit 17                     | Bit 16                     |
|----------|----------|----------|----------|----------------------------|----------------------------|----------------------------|----------------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)                      | - (R)                      | - (R)                      | - (R)                      |
| RES      | RES      | RES      | RES      | U_NVM_M_15                 | U_NVM_M_14                 | U_NVM_M_13                 | U_NVM_M_12                 |
| Reserved | Reserved | Reserved | Reserved | User NVM M register bit 15 | User NVM M register bit 14 | User NVM M register bit 13 | User NVM M register bit 12 |

**Table 198. DCR22 (0x16) MSB description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 23  | RES        | Reserved    |
| 22  | RES        | Reserved    |
| 21  | RES        | Reserved    |
| 20  | RES        | Reserved    |
| 19  | U_NVM_M_15 |             |
| 18  | U_NVM_M_14 |             |
| 17  | U_NVM_M_13 |             |
| 16  | U_NVM_M_12 |             |

**Table 199. DCR22 (0x16)**

| Bit 15                     | Bit 14                     | Bit 13                    | Bit 12                    | Bit 11                    | Bit 10                    | Bit 9                     | Bit 8                     |
|----------------------------|----------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| - (R)                      | - (R)                      | - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                     |
| U_NVM_M_11                 | U_NVM_M_10                 | U_NVM_M_9                 | U_NVM_M_8                 | U_NVM_M_7                 | U_NVM_M_6                 | U_NVM_M_5                 | U_NVM_M_4                 |
| User NVM M register bit 11 | User NVM M register bit 10 | User NVM M register bit 9 | User NVM M register bit 8 | User NVM M register bit 7 | User NVM M register bit 6 | User NVM M register bit 5 | User NVM M register bit 4 |

**Table 200. DCR22 (0x16) description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 15  | U_NVM_M_11 |             |
| 14  | U_NVM_M_10 |             |
| 13  | U_NVM_M_9  |             |
| 12  | U_NVM_M_8  |             |
| 11  | U_NVM_M_7  |             |
| 10  | U_NVM_M_6  |             |

| Bit | Name      | Description |
|-----|-----------|-------------|
| 9   | U_NVM_M_5 |             |
| 8   | U_NVM_M_4 |             |

**Table 201. DCR22 (0x16) LSB**

| Bit 7                     | Bit 6                     | Bit 5                     | Bit 4                     | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------------|---------------------------|---------------------------|---------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| U_NVM_M_3                 | U_NVM_M_2                 | U_NVM_M_1                 | U_NVM_M_0                 | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| User NVM M register bit 3 | User NVM M register bit 2 | User NVM M register bit 1 | User NVM M register bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 202. DCR22 (0x16) LSB description**

| Bit | Name      | Description |
|-----|-----------|-------------|
| 7   | U_NVM_M_3 |             |
| 6   | U_NVM_M_2 |             |
| 5   | U_NVM_M_1 |             |
| 4   | U_NVM_M_0 |             |
| 3   | CRC 3     |             |
| 2   | CRC 2     |             |
| 1   | CRC 1     |             |
| 0   | CRC 0     |             |

**Table 203. DCR23 (0x17) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19                     | Bit 18                     | Bit 17                     | Bit 16                     |
|----------|----------|----------|----------|----------------------------|----------------------------|----------------------------|----------------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)                      | - (R)                      | - (R)                      | - (R)                      |
| RES      | RES      | RES      | RES      | U_NVM_N_15                 | U_NVM_N_14                 | U_NVM_N_13                 | U_NVM_N_12                 |
| Reserved | Reserved | Reserved | Reserved | User NVM N register bit 15 | User NVM N register bit 14 | User NVM N register bit 13 | User NVM N register bit 12 |

**Table 204. DCR23 (0x17) MSB description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 23  | RES        | Reserved    |
| 22  | RES        | Reserved    |
| 21  | RES        | Reserved    |
| 20  | RES        | Reserved    |
| 19  | U_NVM_N_15 |             |
| 18  | U_NVM_N_14 |             |
| 17  | U_NVM_N_13 |             |
| 16  | U_NVM_N_12 |             |

**Table 205. DCR23 (0x17)**

| Bit 15                     | Bit 14                     | Bit 13                    | Bit 12                    | Bit 11                    | Bit 10                    | Bit 9                     | Bit 8                     |
|----------------------------|----------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| - (R)                      | - (R)                      | - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                     |
| U_NVM_N_11                 | U_NVM_N_10                 | U_NVM_N_9                 | U_NVM_N_8                 | U_NVM_N_7                 | U_NVM_N_6                 | U_NVM_N_5                 | U_NVM_N_4                 |
| User NVM N register bit 11 | User NVM N register bit 10 | User NVM N register bit 9 | User NVM N register bit 8 | User NVM N register bit 7 | User NVM N register bit 6 | User NVM N register bit 5 | User NVM N register bit 4 |

**Table 206. DCR23 (0x17) description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 15  | U_NVM_N_11 |             |
| 14  | U_NVM_N_10 |             |
| 13  | U_NVM_N_9  |             |
| 12  | U_NVM_N_8  |             |
| 11  | U_NVM_N_7  |             |
| 10  | U_NVM_N_6  |             |
| 9   | U_NVM_N_5  |             |
| 8   | U_NVM_N_4  |             |

**Table 207. DCR23 (0x17) LSB**

| Bit 7                     | Bit 6                     | Bit 5                     | Bit 4                     | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------------|---------------------------|---------------------------|---------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| U_NVM_N_3                 | U_NVM_N_2                 | U_NVM_N_1                 | U_NVM_N_0                 | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| User NVM N register bit 3 | User NVM N register bit 2 | User NVM N register bit 1 | User NVM N register bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 208. DCR23 (0x17) LSB**

| Bit | Name      | Description |
|-----|-----------|-------------|
| 7   | U_NVM_N_3 |             |
| 6   | U_NVM_N_2 |             |
| 5   | U_NVM_N_1 |             |
| 4   | U_NVM_N_0 |             |
| 3   | CRC 3     |             |
| 2   | CRC 2     |             |
| 1   | CRC 1     |             |
| 0   | CRC 0     |             |

**Table 209. DCR24 (0x18) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19                     | Bit 18                     | Bit 17                     | Bit 16                     |
|----------|----------|----------|----------|----------------------------|----------------------------|----------------------------|----------------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)                      | - (R)                      | - (R)                      | - (R)                      |
| RES      | RES      | RES      | RES      | U_NVM_O_15                 | U_NVM_O_14                 | U_NVM_O_13                 | U_NVM_O_12                 |
| Reserved | Reserved | Reserved | Reserved | User NVM O register bit 15 | User NVM O register bit 14 | User NVM O register bit 13 | User NVM O register bit 12 |

**Table 210. DCR24 (0x18) MSB description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 23  | RES        | Reserved    |
| 22  | RES        | Reserved    |
| 21  | RES        | Reserved    |
| 20  | RES        | Reserved    |
| 19  | U_NVM_O_15 |             |
| 18  | U_NVM_O_14 |             |
| 17  | U_NVM_O_13 |             |
| 16  | U_NVM_O_12 |             |

**Table 211. DCR24 (0x18)**

| Bit 15                     | Bit 14                     | Bit 13                    | Bit 12                    | Bit 11                    | Bit 10                    | Bit 9                     | Bit 8                     |
|----------------------------|----------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| - (R)                      | - (R)                      | - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                     |
| U_NVM_O_11                 | U_NVM_O_10                 | U_NVM_O_9                 | U_NVM_O_8                 | U_NVM_O_7                 | U_NVM_O_6                 | U_NVM_O_5                 | U_NVM_O_4                 |
| User NVM O register bit 11 | User NVM O register bit 10 | User NVM O register bit 9 | User NVM O register bit 8 | User NVM O register bit 7 | User NVM O register bit 6 | User NVM O register bit 5 | User NVM O register bit 4 |

**Table 212. DCR24 (0x18) description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 15  | U_NVM_O_11 |             |
| 14  | U_NVM_O_10 |             |
| 13  | U_NVM_O_9  |             |
| 12  | U_NVM_O_8  |             |
| 11  | U_NVM_O_7  |             |
| 10  | U_NVM_O_6  |             |
| 9   | U_NVM_O_5  |             |
| 8   | U_NVM_O_4  |             |

**Table 213. DCR24 (0x18) LSB**

| Bit 7                     | Bit 6                     | Bit 5                     | Bit 4                     | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------------|---------------------------|---------------------------|---------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| U_NVM_O_3                 | U_NVM_O_2                 | U_NVM_O_1                 | U_NVM_O_0                 | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| User NVM O register bit 3 | User NVM O register bit 2 | User NVM O register bit 1 | User NVM O register bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 214. DCR24 (0x18) LSB description**

| Bit | Name      | Description |
|-----|-----------|-------------|
| 7   | U_NVM_O_3 |             |
| 6   | U_NVM_O_2 |             |
| 5   | U_NVM_O_1 |             |
| 4   | U_NVM_O_0 |             |

| Bit | Name  | Description |
|-----|-------|-------------|
| 3   | CRC 3 |             |
| 2   | CRC 2 |             |
| 1   | CRC 1 |             |
| 0   | CRC 0 |             |

**Table 215. DCR25 (0x19) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19              | Bit 18              | Bit 17              | Bit 16              |
|----------|----------|----------|----------|---------------------|---------------------|---------------------|---------------------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R)               | - (R)               | - (R)               | - (R)               |
| RES      | RES      | RES      | RES      | U_NVM_CRC1_7        | U_NVM_CRC1_6        | U_NVM_CRC1_5        | U_NVM_CRC1_4        |
| Reserved | Reserved | Reserved | Reserved | User NVM CRC1 bit 7 | User NVM CRC1 bit 6 | User NVM CRC1 bit 5 | User NVM CRC1 bit 4 |

**Table 216. DCR25 (0x19) MSB description**

| Bit | Name         | Description |
|-----|--------------|-------------|
| 23  | RES          | Reserved    |
| 22  | RES          | Reserved    |
| 21  | RES          | Reserved    |
| 20  | RES          | Reserved    |
| 19  | U_NVM_CRC1_7 |             |
| 18  | U_NVM_CRC1_6 |             |
| 17  | U_NVM_CRC1_5 |             |
| 16  | U_NVM_CRC1_4 |             |

**Table 217. DCR25 (0x19)**

| Bit 15              | Bit 14              | Bit 13              | Bit 12              | Bit 11               | Bit 10               | Bit 9                     | Bit 8                     |
|---------------------|---------------------|---------------------|---------------------|----------------------|----------------------|---------------------------|---------------------------|
| - (R)               | - (R)               | - (R)               | - (R)               | - (R)                | - (R)                | - (R)                     | - (R)                     |
| U_NVM_CRC1_3        | U_NVM_CRC1_2        | U_NVM_CRC1_1        | U_NVM_CRC1_0        | U_PROG1_1            | U_PROG1_0            | U_NVM_P_5                 | U_NVM_P_4                 |
| User NVM CRC1 bit 3 | User NVM CRC1 bit 2 | User NVM CRC1 bit 1 | User NVM CRC1 bit 0 | User program 1 bit 1 | User program 1 bit 0 | User NVM P register bit 5 | User NVM P register bit 4 |

**Table 218. DCR25 (0x19)**

| Bit | Name         | Description                                                                     |
|-----|--------------|---------------------------------------------------------------------------------|
| 15  | U_NVM_CRC1_3 |                                                                                 |
| 14  | U_NVM_CRC1_2 |                                                                                 |
| 13  | U_NVM_CRC1_1 |                                                                                 |
| 12  | U_NVM_CRC1_0 |                                                                                 |
| 11  | U_PROG1_1    | Not accessible by user but programmed by NVM controller during user programming |
| 10  | U_PROG1_0    | Not accessible by user but programmed by NVM controller during user programming |
| 9   | U_NVM_P_5    |                                                                                 |
| 8   | U_NVM_P_4    |                                                                                 |

**Table 219. DCR25 (0x19) LSB**

| Bit 7                     | Bit 6                     | Bit 5                     | Bit 4                     | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------------|---------------------------|---------------------------|---------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R)                     | - (R)                     | - (R)                     | - (R)                     | - (R)                            | - (R)                            | - (R)                            | - (R)                            |
| U_NVM_P_3                 | U_NVM_P_2                 | U_NVM_P_1                 | U_NVM_P_0                 | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| User NVM P register bit 3 | User NVM P register bit 2 | User NVM P register bit 1 | User NVM P register bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 220. DCR25 (0x19) LSB description**

| Bit | Name      | Description |
|-----|-----------|-------------|
| 7   | U_NVM_P_3 |             |
| 6   | U_NVM_P_2 |             |
| 5   | U_NVM_P_1 |             |
| 4   | U_NVM_P_0 |             |
| 3   | CRC 3     |             |
| 2   | CRC 2     |             |
| 1   | CRC 1     |             |
| 0   | CRC 0     |             |

## 9.7 Status registers

The first row of each of the following DSRx tables lists the status register read values, as follows:

- 0 (RC1L): Read and Clear register when the bit is "1".
- 0 (R): Read-only register that cannot be cleared (live bit).
- - (R0): Reserved bits that always read as "0" and shall not be used.

**Table 221. DSR1 (0x21) MSB**

| Bit 23   | Bit 22              | Bit 21                                                 | Bit 20                | Bit 19                | Bit 18                 | Bit 17                       | Bit 16                |
|----------|---------------------|--------------------------------------------------------|-----------------------|-----------------------|------------------------|------------------------------|-----------------------|
| - (R0)   | 0 (RC1L)            | 0 (RC1L)                                               | 0 (RC1L)              | 0 (RC1L)              | 0 (RC1L)               | 0 (RC1L)                     | 0 (RC1L)              |
| RES      | BOOST_TIMER_CNT_END | FORCED_SLEEP_WDFAIL                                    | BUCK3_OC              | BUCK3_OV              | BUCK3_UV               | BUCK3_PG_TIMEOUT             | BUCK2_OC              |
| Reserved | Boost timer end Bit | Device enters in DEEP-SLEEP state after 15 WD fail bit | BUCK3 overcurrent bit | BUCK3 overvoltage bit | BUCK3 undervoltage bit | BUCK3 power-good timeout bit | BUCK2 overcurrent bit |

**Table 222. DSR1 (0x21) MSB description**

| Bit | Name                | Description                                                                                                                        |
|-----|---------------------|------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES                 | Reserved                                                                                                                           |
| 22  | BOOST_TIMER_CNT_END | 1 : Boost timer ended<br>0 : Boost timer not ended                                                                                 |
| 21  | FORCED_SLEEP_WDFAIL | 1: state machine reaches DEEP-SLEEP after 15 watchdog fails<br>0: No transition to DEEP-SLEEP due to 15 consecutive watchdog fails |
| 20  | BUCK3_OC            | 1: BUCK3 overcurrent detected<br>0: No error                                                                                       |
| 19  | BUCK3_OV            | 1: BUCK3 overvoltage detected<br>0: No error                                                                                       |
| 18  | BUCK3_UV            | 1: BUCK3 undervoltage detected<br>0: No error                                                                                      |

| Bit | Name             | Description                                                                                                                                                                   |
|-----|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17  | BUCK3_PG_TIMEOUT | BUCK3 power-good timeout during power-up sequence<br>1: Indicates that the power-good is not reached at the end of timeout<br>Bit is latched until a “Read and clear” command |
| 16  | BUCK2_OC         | 1: BUCK2 overcurrent detected<br>0: No error                                                                                                                                  |

**Table 223. DSR1 (0x21)**

| Bit 15                | Bit 14                 | Bit 13                       | Bit 12                | Bit 11                | Bit 10                 | Bit 9                        | Bit 8                       |
|-----------------------|------------------------|------------------------------|-----------------------|-----------------------|------------------------|------------------------------|-----------------------------|
| 0 (RC1L)              | 0 (RC1L)               | 0 (RC1L)                     | 0 (RC1L)              | 0 (RC1L)              | 0 (RC1L)               | 0 (RC1L)                     | 0 (RC1L)                    |
| BUCK2_OV              | BUCK2_UV               | BUCK2_PG_TIMEOUT             | BUCK1_OC              | BUCK1_OV              | BUCK1_UV               | BUCK1_PG_TIMEOUT             | LDO2_PG_TIMEOUT             |
| BUCK2 overvoltage bit | BUCK2 undervoltage bit | BUCK2 power-good timeout bit | BUCK1 overcurrent bit | BUCK1 overvoltage bit | BUCK1 undervoltage bit | BUCK1 power-good timeout bit | LDO2 power-good timeout bit |

**Table 224. DSR1 (0x21) description**

| Bit | Name             | Description                                                                                                                                                                   |
|-----|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | BUCK2_OV         | 1: BUCK2 overvoltage detected<br>0: No error                                                                                                                                  |
| 14  | BUCK2_UV         | 1: BUCK2 undervoltage detected<br>0: No error                                                                                                                                 |
| 13  | BUCK2_PG_TIMEOUT | BUCK2 power-good timeout during power-up sequence<br>1: Indicates that the power-good is not reached at the end of timeout<br>Bit is latched until a “Read and clear” command |
| 12  | BUCK1_OC         | 1: BUCK1 overcurrent detected<br>0: No error                                                                                                                                  |
| 11  | BUCK1_OV         | 1: BUCK1 overvoltage detected<br>0: No error                                                                                                                                  |
| 10  | BUCK1_UV         | 1: BUCK1 undervoltage detected<br>0: No error                                                                                                                                 |
| 9   | BUCK1_PG_TIMEOUT | BUCK1 power-good timeout during power-up sequence<br>1: Indicates that the power-good is not reached at the end of timeout<br>Bit is latched until a “Read and clear” command |
| 8   | LDO2_PG_TIMEOUT  | LDO2 power-good timeout during power-up sequence<br>1: Indicates that the power-good is not reached at the end of timeout<br>Bit is latched until a “Read and clear” command  |

**Table 225. DSR1 (0x21) LSB**

| Bit 7                 | Bit 6                | Bit 5                       | Bit 4                 | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-----------------------|----------------------|-----------------------------|-----------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (RC1L)              | 0 (RC1L)             | 0 (RC1L)                    | 0 (RC1L)              | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| LDO2_UV               | LDO2_OV              | LDO1_PG_TIMEOUT             | LDO1_UV               | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| LDO2 undervoltage bit | LDO2 overvoltage bit | LDO1 power-good timeout bit | LDO1 undervoltage bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 226. DSR1 (0x21) LSB description**

| Bit | Name            | Description                                                                                                                                                                  |
|-----|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | LDO2_UV         | Indicates undervoltage condition at voltage regulator LDO2 (LDO2 < VRTx)<br>1: Undervoltage<br>Bit is latched until a "Read and clear" command                               |
| 6   | LDO2_OV         | Indicates overvoltage condition at voltage regulator LDO2<br>1: Overvoltage<br>Bit is latched until a "Read and clear" command                                               |
| 5   | LDO1_PG_TIMEOUT | LDO1 power-good timeout during power-up sequence<br>1: Indicates that the power-good is not reached at the end of timeout<br>Bit is latched until a "Read and clear" command |
| 4   | LDO1_UV         | Indicates undervoltage condition at voltage regulator LDO1 (LDO1 < VRTx)<br>1: Undervoltage<br>Bit is latched until a "Read and clear" command                               |
| 3   | CRC 3           |                                                                                                                                                                              |
| 2   | CRC 2           |                                                                                                                                                                              |
| 1   | CRC 1           |                                                                                                                                                                              |
| 0   | CRC 0           |                                                                                                                                                                              |

**Table 227. DSR2 (0x22) MSB**

| Bit 23   | Bit 22              | Bit 21                | Bit 20                      | Bit 19                  | Bit 18                 | Bit 17              | Bit 16               |
|----------|---------------------|-----------------------|-----------------------------|-------------------------|------------------------|---------------------|----------------------|
| -(R0)    | 0 (RC1L)            | 0 (RC1L)              | 0 (RC1L)                    | 0 (RC1L)                | 0 (RC1L)               | 0 (RC1L)            | 0 (RC1L)             |
| RES      | OUTHS_OL            | OUTHS_OC              | BOOST_IN_LP                 | BYPASS_VDSMON_ERROR     | BOOST_VDSMON_ERROR     | FBB_OV              | FBB_UV               |
| Reserved | OUTHS open load bit | OUTHS overcurrent bit | BOOST in LOW-POWER mode bit | Bypass VDSMON error bit | BOOST VDSMON error bit | FBB overvoltage bit | FBB undervoltage bit |

**Table 228. DSR2 (0x22) MSB description**

| Bit | Name                | Description                                                                                                                          |
|-----|---------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES                 | Reserved                                                                                                                             |
| 22  | OUTHS_OL            | Open-load<br>1: Indicates an open-load condition was detected at OUTHS output<br>Bit is latched until a "Read and clear" command     |
| 21  | OUTHS_OC            | Overcurrent<br>1: Indicates an overcurrent condition was detected at OUTHS output<br>Bit is latched until a "Read and clear" command |
| 20  | BOOST_IN_LP         | Boost switched on in LOW-POWER mode<br>1: Occurred                                                                                   |
| 19  | BYPASS_VDSMON_ERROR | BYPASS $V_{ds}$ monitoring error<br>1: Error is detected<br>0: No error reported                                                     |
| 18  | BOOST_VDSMON_ERROR  | BOOST $V_{ds}$ monitoring error<br>1: Error is detected<br>0: No error reported                                                      |
| 17  | FBB_OV              | FBB overvoltage<br>1: Indicates the voltage at FBB increased above the FBB overvoltage threshold                                     |

| Bit | Name   | Description                                                                                                                                                                                                                |
|-----|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |        | In ACTIVE and REC-1 modes, an interrupt pulse is generated at IRQ<br>Bit is latched until a "Read and clear" command                                                                                                       |
| 16  | FBB_UV | FBB undervoltage<br>1: Indicates the voltage at FBB decreased below the FBB undervoltage threshold<br>In ACTIVE and REC-1 modes, an interrupt pulse is generated at IRQ<br>Bit is latched until a "Read and clear" command |

**Table 229. DSR2 (0x22)**

| Bit 15                   | Bit 14                     | Bit 13               | Bit 12                         | Bit 11                | Bit 10               | Bit 9                             | Bit 8                             |
|--------------------------|----------------------------|----------------------|--------------------------------|-----------------------|----------------------|-----------------------------------|-----------------------------------|
| 0 (RC1L)                 | 0 (RC1L)                   | 0 (RC1L)             | 0 (RC1L)                       | 0 (RC1L)              | 0 (RC1L)             | 0 (RC1L)                          | 0 (RC1L)                          |
| IRQ_ECHO_ERROR           | FCCU_ENA_ECHO_ERROR        | NFSO1_ECHO_ERROR     | WD_ENA_ECHO_ERROR              | NRST_ECHO_ERROR       | VIO_UV               | TSD_CL4                           | TSD_CL3                           |
| Interrupt echo error bit | FCCU enable echo error bit | NFSO1 echo error bit | Watchdog enable echo error bit | NRESET echo error bit | VIO undervoltage bit | Thermal shutdown of cluster 4 bit | Thermal shutdown of cluster 3 bit |

**Table 230. DSR2 (0x22) description**

| Bit | Name                | Description                                                                                                                                                                                       |
|-----|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | IRQ_ECHO_ERROR      | IRQ asserted but still high<br>1: Still high when asserted low                                                                                                                                    |
| 14  | FCCU_ENA_ECHO_ERROR | 1: The FCCU_ENA echo monitor reported an error<br>0: No error reported                                                                                                                            |
| 13  | NFSO1_ECHO_ERROR    | 1: The NFSO1 echo monitor reported an error<br>0: No error reported                                                                                                                               |
| 12  | WD_ENA_ECHO_ERROR   | 1: The WD_ENA echo monitor reported an error<br>0: No error reported                                                                                                                              |
| 11  | NRST_ECHO_ERROR     | 1: NRESET input high while NRESET output (expected) low after filter<br>0: No error                                                                                                               |
| 10  | VIO_UV              | V <sub>IO</sub> undervoltage<br>1: Indicates the voltage at VIO has reached the undervoltage threshold<br>Bit is latched until a "Read and clear" command                                         |
| 9   | TSD_CL4             | Thermal shutdown of cluster 4<br>1: Indicates cluster 4 has reached the thermal shutdown threshold (TSD) and the output cluster was shut down<br>Bit is latched until a "Read and clear" command  |
| 8   | TSD_CL3             | Thermal shutdown of Cluster 3<br>'1' indicates Cluster 3 has reached the thermal shutdown threshold (TSD) and the output cluster was shut down<br>Bit is latched until a "Read and clear" command |

**Table 231. DSR2 (0x22) LSB**

| Bit 7                             | Bit 6                             | Bit 5                             | Bit 4                | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-----------------------------------|-----------------------------------|-----------------------------------|----------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (RC1L)                          | 0 (RC1L)                          | 0 (RC1L)                          | 0 (R)                | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| TSD_CL2                           | TSD_CL1                           | TSD_CL0                           | TSD                  | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Thermal shutdown of cluster 2 bit | Thermal shutdown of cluster 1 bit | Thermal shutdown of cluster 0 bit | Thermal shutdown bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 232. DSR2 (0x22) LSB description**

| Bit | Name    | Description                                                                                                                                                                                             |
|-----|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | TSD_CL2 | Thermal shutdown of cluster 2<br>1: Indicates cluster 2 has reached the thermal shutdown threshold (TSD) and the output cluster was shut down<br>Bit is latched until a "Read and clear" command        |
| 6   | TSD_CL1 | Thermal shutdown of cluster 1<br>1: Indicates cluster 1 has reached the thermal shutdown threshold (TSD) and the output cluster was shut down<br>Bit is latched until a "Read and clear" command        |
| 5   | TSD_CL0 | Thermal shutdown of cluster 0<br>1: Indicates cluster 0 has reached the thermal shutdown threshold (TSD) and the output cluster was shut down<br>Bit is latched until a "Read and clear" command        |
| 4   | TSD     | Thermal shutdown was reached (logical or combination of all TSD_CLx, see status register DSR6)<br>This bit cannot be cleared directly. It is reset if the corresponding TSD_CLx bits in SR6 are cleared |
| 3   | CRC 3   |                                                                                                                                                                                                         |
| 2   | CRC 2   |                                                                                                                                                                                                         |
| 1   | CRC 1   |                                                                                                                                                                                                         |
| 0   | CRC 0   |                                                                                                                                                                                                         |

**Table 233. DSR3 (0x23) MSB**

| Bit 23   | Bit 22            | Bit 21                   | Bit 20                   | Bit 19                    | Bit 18                 | Bit 17                 | Bit 16                |
|----------|-------------------|--------------------------|--------------------------|---------------------------|------------------------|------------------------|-----------------------|
| - (R0)   | 0 (RC1L)          | 0 (RC1L)                 | 0 (RC1L)                 | 0 (RC1L)                  | 0 (RC1L)               | 0 (RC1L)               | 0 (RC1L)              |
| RES      | LBIST_STOPPED     | BUCK3_INT_FAIL           | BUCK2_INT_FAIL           | BUCK1_INT_FAIL            | LBIST_ERROR_1          | LBIST_ERROR_0          | ABIST_ERROR           |
| Reserved | LBIST stopped bit | BUCK3 interrupt fail bit | BUCK2 interrupt fail bit | BUCK31 interrupt fail bit | Logic BIST error bit 1 | Logic BIST error bit 0 | Analog BIST error bit |

**Table 234. DSR3 (0x23) MSB description**

| Bit | Name           | Description                                                                                                                                                                      |
|-----|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES            | Reserved                                                                                                                                                                         |
| 22  | LBIST_STOPPED  | 1: Indicates that LBIST has been stopped due to fault events                                                                                                                     |
| 21  | BUCK3_INT_FAIL | BUCK3 internal fail that may be caused by LDO_BUCK3_OV or LDO_Buck3_UV<br>1: Indicates that an internal error occurs on BUCK3<br>Bit is latched until a "Read and clear" command |
| 20  | BUCK2_INT_FAIL | BUCK2 internal fail that may be caused by LDO_BUCK2_OV or LDO_BUCK2_UV<br>1: Indicates that an internal error occurs on BUCK2<br>Bit is latched until a "Read and clear" command |
| 19  | BUCK1_INT_FAIL | BUCK1 internal fail that may be caused by LDO_BUCK1_OV or LDO_BUCK1_UV<br>1: Indicates that an internal error occurs on buck1<br>Bit is latched until a "Read and clear" command |
| 18  | LBIST_ERROR_1  | 1: The logic BIST2 reported an error                                                                                                                                             |
| 17  | LBIST_ERROR_0  | 1: The logic BIST1 reported an error                                                                                                                                             |
| 16  | ABIST_ERROR    | 1: The analog BIST reported an error                                                                                                                                             |

**Table 235. DSR3 (0x23)**

| Bit 15   | Bit 14   | Bit 13   | Bit 12   | Bit 11   | Bit 10   | Bit 9    | Bit 8    |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 0 (RC1L) | 0 (RC1L) | 0 (RC1L) | 0 (RC1L) | 0 (RC1L) | 0 (RC1L) | 0 (RC1L) | 0 (RC1L) |

| Bit 15               | Bit 14                           | Bit 13        | Bit 12            | Bit 11                               | Bit 10                              | Bit 9                 | Bit 8             |
|----------------------|----------------------------------|---------------|-------------------|--------------------------------------|-------------------------------------|-----------------------|-------------------|
| CURRENT_MISMATCH     | FORCED_SLEEP_TSD                 | FCCUFAIL      | WDFAIL            | INT_REG_UV                           | INT_REG_OV                          | NVM_COMP_ERROR        | NVM_CRC_ERROR     |
| Current mismatch bit | Forced sleep after TSD event bit | FCCU fail bit | Watchdog fail bit | Interrupt regulator undervoltage bit | Interrupt regulator overvoltage bit | NVM compare error bit | NVM CRC error bit |

**Table 236. DSR3 (0x23) description**

| Bit | Name             | Description                                                                                                                                                                                                                       |
|-----|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | CURRENT_MISMATCH | 1: A current mismatch occurs between main and monitoring currents                                                                                                                                                                 |
| 14  | FORCED_SLEEP_TSD | 1: State machine reaches DEEP-SLEEP after 3 TSD events                                                                                                                                                                            |
| 13  | FCCUFAIL         | FCCU fault detection<br>1: A fault has been detected by the FCCU monitor bit is latched until a "Read and clear" command                                                                                                          |
| 12  | WDFAIL           | A WD trig fail event occurred<br>Bit is latched until a "Read and clear" command<br>Note that after 15 consecutive WD trig faults, the device reaches DEEP-SLEEP state where WDFAIL_CNT is cleared, while WDFAIL bit is kept at 1 |
| 11  | INT_REG_UV       | Internal regulator undervoltage<br>1: Indicates an internal regulator undervoltage occurs on 3V3<br>This bit is latched until a "Read and clear" command                                                                          |
| 10  | INT_REG_OV       | Internal regulator overvoltage<br>1: Indicates an internal regulator overvoltage occurs on 3V3<br>This bit is latched until a "Read and clear" command                                                                            |
| 9   | NVM_COMP_ERROR   | Indicates an error between NVM and mirror register                                                                                                                                                                                |
| 8   | NVM_CRC_ERROR    | Indicates a NVM CRC error at NVM download                                                                                                                                                                                         |

**Table 237. DSR3 (0x33) LSB**

| Bit 7                     | Bit 6                 | Bit 5                           | Bit 4                                   | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------------|-----------------------|---------------------------------|-----------------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (RC1L)                  | 0 (RC1L)              | 0 (RC1L)                        | 0 (RC1L)                                | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| GNDLOSS                   | OSC_ERROR             | SPI_REG_COMP_ERROR              | FSM_COMP_ERROR                          | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Ground Loss detection bit | Oscillators error bit | SPI registers compare error bit | Finite state machine compares error bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 238. DSR3 (0x33) LSB description**

| Bit | Name               | Description                                                                        |
|-----|--------------------|------------------------------------------------------------------------------------|
| 7   | GNDLOSS            | 1: Digital or analog central ground loss detected<br>0: No error                   |
| 6   | OSC_ERROR          | 1: The oscillator monitor reported an error<br>0: No error reported                |
| 5   | SPI_REG_COMP_ERROR | 1: The SPI safety registers monitor reported an error<br>0: No error reported      |
| 4   | FSM_COMP_ERROR     | 1: The main finite state machine monitor reported an error<br>0: No error reported |
| 3   | CRC 3              |                                                                                    |
| 2   | CRC 2              |                                                                                    |
| 1   | CRC 1              |                                                                                    |
| 0   | CRC 0              |                                                                                    |

**Table 239. DSR4 (0x24) MSB**

| Bit 23   | Bit 22                      | Bit 21                | Bit 20              | Bit 19            | Bit 18                 | Bit 17                | Bit 16                    |
|----------|-----------------------------|-----------------------|---------------------|-------------------|------------------------|-----------------------|---------------------------|
| -(R0)    | 0 (RC1L)                    | 0 (RC1L)              | 0 (RC1L)            | 0 (RC1L)          | 0 (RC1L)               | 0 (RC1L)              | 0 (RC1L)                  |
| RES      | SPI_ALL_WAKEUP_DISABLE      | SPI_CLK_CNT           | SPI_CSN_TIMEOUT     | SPI_CRC_ERR       | SPI_SDI_STUCK_HIGH     | SPI_SDI_STUCK_LOW     | SPI_UNDEF_ADD             |
| Reserved | SPI all wake up disable bit | SPI clock counter bit | SPI CSN timeout bit | SPI CRC error bit | SPI SDI Stuck high bit | SPI SDI Stuck Low bit | SPI undefined address bit |

**Table 240. DSR4 (0x24) MSB description**

| Bit | Name                   | Description                                                                                                                                |
|-----|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES                    | Reserved                                                                                                                                   |
| 22  | SPI_ALL_WAKEUP_DISABLE | SPI attempt occurs to disable all wake-up sources.<br>This attempt for last wake-up disable has not been performed                         |
| 21  | SPI_CLK_CNT            | SPI clock counter<br>1: Indicates an SPI frame with the wrong number of CLK cycles was detected.<br>Bit is latched until a valid SPI frame |
| 20  | SPI_CSN_TIMEOUT        | 1: SPI CSN timeout error detected                                                                                                          |
| 19  | SPI_CRC_ERR            | 1: SPI CRC error detected                                                                                                                  |
| 18  | SPI_SDI_STUCK_HIGH     | 1: SPI SDI stuck at high level                                                                                                             |
| 17  | SPI_SDI_STUCK_LOW      | 1: SPI SDI stuck at low level                                                                                                              |
| 16  | SPI_UNDEF_ADD          | 1: SPI access to undefined address                                                                                                         |

**Table 241. DSR4 (0x24)**

| Bit 15               | Bit 14             | Bit 13                            | Bit 12                             | Bit 11                            | Bit 10             | Bit 9                            | Bit 8                            |
|----------------------|--------------------|-----------------------------------|------------------------------------|-----------------------------------|--------------------|----------------------------------|----------------------------------|
| 0 (RC1L)             | 0 (RC1L)           | 0 (RC1L)                          | 0 (RC1L)                           | 0 (RC1L)                          | 0 (RC1L)           | 0 (RC1L)                         | 0 (RC1L)                         |
| SPI_STATUS_WRT       | SPI_LBISTED        | FBB_OV_EW                         | FBB_UV_EW                          | VS_UV_EW                          | CAN_SUP_LOW        | TW_CL4                           | TW_CL3                           |
| SPI status write bit | SPI LBIST test bit | FBB overvoltage early warning bit | FBB undervoltage early warning bit | VS undervoltage early warning bit | CAN Supply Low Bit | Thermal warning of cluster 4 bit | Thermal warning of cluster 3 bit |

**Table 242. DSR4 (0x24) description**

| Bit | Name           | Description                                                                                                                                                                                                                                                                        |
|-----|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | SPI_STATUS_WRT | 1: SPI writes access to status register                                                                                                                                                                                                                                            |
| 14  | SPI_LBISTED    | 1: SPI access while SPI is under LBIST test                                                                                                                                                                                                                                        |
| 13  | FBB_OV_EW      | FBB overvoltage early warning<br>1: Indicates the voltage at FBB increased above the FBB overvoltage early warning threshold (configured in CR3)<br>In ACTIVE and REC-1 modes, an interrupt pulse is generated at IRQ.<br>Bit is latched until a "Read and clear" command          |
| 12  | FBB_UV_EW      | FBB undervoltage early warning<br>1: Indicates the voltage at FBB decreased below the FBB undervoltage early warning threshold (configured in CR3)<br>In ACTIVE and REC-1 modes, an interrupt pulse is generated at IRQ<br>Bit is latched until a "Read and clear" command         |
| 11  | VS_UV_EW       | V <sub>S</sub> early warning<br>1: Indicates the voltage at V <sub>S</sub> decreased below the V <sub>S</sub> early warning threshold (configured in CR3)<br>In ACTIVE and REC-1 modes, an interrupt pulse is generated at IRQ.<br>Bit is latched until a "Read and clear" command |

| Bit | Name        | Description                                                                                                                                               |
|-----|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | CAN_SUP_LOW | Voltage at CAN supply pin reached the CAN supply low warning threshold $V_{CANSUP} < V_{CANSUP_{low}}$<br>Bit is latched until a "Read and clear" command |
| 9   | TW_CL4      | Thermal warning of cluster 4<br>1: Indicates cluster 4 has reached the thermal warning threshold (TSW)<br>Bit is latched until a "Read and clear" command |
| 8   | TW_CL3      | Thermal warning of cluster 3<br>1: Indicates cluster 3 has reached the thermal warning threshold (TSW)<br>Bit is latched until a "Read and clear" command |

**Table 243. DSR4 (0x24) LSB**

| Bit 7                            | Bit 6                            | Bit 5                       | Bit 4               | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|----------------------------------|----------------------------------|-----------------------------|---------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                    | 0 (R)               | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| TW_CL2                           | TW_CL1                           | TW_CL0                      | TW                  | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Thermal warning of cluster 2 bit | Thermal warning of cluster 1 bit | Central thermal warning bit | Thermal warning bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 244. DSR4 (0x24) LSB description**

| Bit | Name   | Description                                                                                                                                               |
|-----|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | TW_CL2 | Thermal warning of cluster 2<br>1: Indicates cluster 2 has reached the thermal warning threshold (TSW)<br>Bit is latched until a "Read and clear" command |
| 6   | TW_CL1 | Thermal warning of cluster 1<br>1: Indicates cluster 1 has reached the thermal warning threshold (TSW)<br>Bit is latched until a "Read and clear" command |
| 5   | TW_CL0 | Thermal warning of cluster 0<br>1: Indicates cluster 0 has reached the thermal warning threshold (TSW)<br>Bit is latched until a "Read and clear" command |
| 4   | TW     | Thermal warning<br>1: Indicates the temperature has reached the thermal warning threshold (logical OR combination of bits TW_CLx in DSR6)                 |
| 3   | CRC 3  |                                                                                                                                                           |
| 2   | CRC 2  |                                                                                                                                                           |
| 1   | CRC 1  |                                                                                                                                                           |
| 0   | CRC 0  |                                                                                                                                                           |

**Table 245. DSR5 (0x25) MSB**

| Bit 23   | Bit 22               | Bit 21   | Bit 20   | Bit 19            | Bit 18                  | Bit 17                  | Bit 16                  |
|----------|----------------------|----------|----------|-------------------|-------------------------|-------------------------|-------------------------|
| -(R0)    | 0 (RC1L)             | -(R0)    | -(R0)    | 0 (R)             | 0 (RC1L)                | 0 (RC1L)                | 0 (RC1L)                |
| RES      | FP_READY             | RES      | RES      | BYPASS_STATUS     | BUCK3_PG_OK             | BUCK2_PG_OK             | BUCK1_PG_OK             |
| Reserved | FULL-POWER Ready bit | Reserved | Reserved | Bypass status bit | BUCK3 power-good ok bit | BUCK2 power-good ok bit | BUCK1 power-good ok bit |

**Table 246. DSR5 (0x25) MSB description**

| Bit | Name          | Description                                                                                                           |
|-----|---------------|-----------------------------------------------------------------------------------------------------------------------|
| 23  | RES           | Reserved                                                                                                              |
| 22  | FP_READY      | 1: Transition from LOW-POWER to FULL-POWER occurred.<br>IRQ generated when this occurs                                |
| 21  | RES           | Reserved                                                                                                              |
| 20  | RES           | Reserved (some glitches can occur on this Status bit. to not be take into account or masked by software)              |
| 19  | BYPASS_STATUS | 1: Bypass ON<br>0: Bypass OFF<br>Live bit                                                                             |
| 18  | BUCK3_PG_OK   | 1: Power-good reached after the regulator has been turned ON by power-up sequence or through SPI<br>0: PG not reached |
| 17  | BUCK2_PG_OK   | 1: Power-good reached after the regulator has been turned ON by power-up sequence or through SPI<br>0: PG not reached |
| 16  | BUCK1_PG_OK   | 1: Power-good reached after the regulator has been turned ON by power-up sequence or through SPI<br>0: PG not reached |

**Table 247. DSR5 (0x25)**

| Bit 15             | Bit 14             | Bit 13             | Bit 12             | Bit 11             | Bit 10             | Bit 9                            | Bit 8                            |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|----------------------------------|----------------------------------|
| 0 (R)              | 0 (R)              | 0 (R)              | 0 (R)              | 0 (R)              | 0 (R)              | 0 (RC1L)                         | 0 (RC1L)                         |
| DEV_STATE_5        | DEV_STATE_4        | DEV_STATE_3        | DEV_STATE_2        | DEV_STATE_1        | DEV_STATE_0        | DEEP-SLEEP_FROM_DO_POWER_DOWN_1  | DEEP-SLEEP_FROM_DO_POWER_DOWN_0  |
| Device state bit 5 | Device state bit 4 | Device state bit 3 | Device state bit 2 | Device state bit 1 | Device state bit 0 | DEEP-SLEEP from power down bit 1 | DEEP-SLEEP from power down bit 0 |

**Table 248. DSR5 (0x25) description**

| Bit | Name                            | Description                                                                                                                                                |
|-----|---------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | DEV_STATE_5                     |                                                                                                                                                            |
| 14  | DEV_STATE_4                     |                                                                                                                                                            |
| 13  | DEV_STATE_3                     |                                                                                                                                                            |
| 12  | DEV_STATE_2                     |                                                                                                                                                            |
| 11  | DEV_STATE_1                     |                                                                                                                                                            |
| 10  | DEV_STATE_0                     | Current state of state machine<br>00000: START-UP<br>...                                                                                                   |
| 9   | DEEP-SLEEP_FROM_DO_POWER_DOWN_1 | 00: Default<br>01: DEEP-SLEEP entered after a DO_POWER_DOWN command in ACTIVE state<br>1x: DEEP-SLEEP entered after a DO_POWER_DOWN command in REC-1 state |
| 8   | DEEP-SLEEP_FROM_DO_POWER_DOWN_0 |                                                                                                                                                            |

**Table 249. DEV\_STATE binary code for state machine states/modes**

| Digital FSM states | Spec states/modes      | Binary |
|--------------------|------------------------|--------|
| AA_START_UP        | START-UP state         | 000000 |
| ACTIVE_HP          | ACTIVE FULL-POWER mode | 000001 |
| ACTIVE_LP          | ACTIVE LOW-POWER mode  | 000010 |
| ACTIVE_LP2HP1      | LP2FP transition       | 000011 |

| Digital FSM states         | Spec states/modes   | Binary |
|----------------------------|---------------------|--------|
| ACTIVE_LP2HP2              | LP2FP transition    | 000100 |
| ACTIVE_LP2HP3              |                     | 000101 |
| ACTIVE_LP2HP4              |                     | 000110 |
| ANA_TRIM                   | Not usable          | 000111 |
| DEEPSLEEP_INIT1            | DEEP-SLEEP state    | 001000 |
| DEEPSLEEP_INIT2            |                     | 001001 |
| DEEPSLEEP_INIT3            |                     | 001010 |
| DEEPSLEEP_INIT4            |                     | 001011 |
| DEEPSLEEP_TO_START_SM      |                     | 001100 |
| DEEP_SLEEP                 |                     | 001101 |
| INIT1                      | INIT state          | 001110 |
| INIT2                      |                     | 001111 |
| POWER_DOWN_FROM_PG_TIMEOUT | POWER-DOWN sequence | 010001 |
| POWER_DOWN_TO_DEEP_SLEEP   |                     | 010010 |
| POWER_DOWN_TO_REC_2        |                     | 010011 |
| NRESET_PULSE               | POWER-UP sequence   | 010000 |
| POWER_UP_FROM_FAIL         |                     | 010100 |
| POWER_UP_FROM_INIT         |                     | 010101 |
| PROD_TEST_MODE             | Not usable          | 010110 |
| READ_NVM_DL                | U-NVM-DL state      | 010111 |
| REC_1                      | REC-1 state         | 011000 |
| REC_2                      | REC-2 state         | 011001 |
| RESET_SPI_REG              | START-SM state      | 011010 |
| RISE_REF                   |                     | 011011 |
| START_SM                   |                     | 011100 |
| SWDBG                      | SWDBG               | 011101 |
| SWDBG_SET                  |                     | 011110 |
| USER_NVM_PROG_1            | U-NVM-PROG-1        | 011111 |
| USER_NVM_PROG_2            | U-NVM-PROG-2        | 100000 |
| USER_NVM_PROG_2_COMPLETE   |                     | 100001 |
| USER_NVM_PROG_3            |                     | 100010 |
| USER_NVM_PROG_3_COMPLETE   |                     | 100011 |
| USER_NVM_PROG_4            |                     | 100100 |
| USER_NVM_PROG_4_COMPLETE   |                     | 100101 |

**Table 250. DSR5 (0x25) LSB**

| Bit 7                     | Bit 6                            | Bit 5                       | Bit 4                       | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------------|----------------------------------|-----------------------------|-----------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (RC1L)                  | 0 (RC1L)                         | 0 (RC1L)                    | 0 (RC1L)                    | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| FORCED_SLEEP_POWUP        | FSM_TO_REC2                      | REC2_FROM_DO_POWER_CYCLE_1  | REC2_FROM_DO_POWER_CYCLE_0  | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Forced sleep power up bit | Finite state machine to REC2 bit | REC2 from power cycle bit 1 | REC2 from power cycle bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 251. DSR5 (0x25) LSB description**

| Bit | Name                       | Description                                                                                                                                      |
|-----|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | FORCED_SLEEP_POWUP         | 1: State machine reaches DEEP-SLEEP after 4 attempts to power up                                                                                 |
| 6   | FSM_TO_REC2                | Functional state machine state before reaching REC2<br>1: REC1<br>Bit is latched until a "Read and clear" command<br>0: ACTIVE                   |
| 5   | REC2_FROM_DO_POWER_CYCLE_1 | 00: Default<br>01: REC2 entered after a DO_POWER_CYCLE command in ACTIVE state<br>1x: REC2 entered after a DO_POWER_CYCLE command in REC-1 state |
| 4   | REC2_FROM_DO_POWER_CYCLE_0 |                                                                                                                                                  |
| 3   | CRC 3                      |                                                                                                                                                  |
| 2   | CRC 2                      |                                                                                                                                                  |
| 1   | CRC 1                      |                                                                                                                                                  |
| 0   | CRC 0                      |                                                                                                                                                  |

**Table 252. DSR6 (0x26) MSB**

| Bit 23   | Bit 22              | Bit 21                 | Bit 20           | Bit 19          | Bit 18               | Bit 17               | Bit 16                     |
|----------|---------------------|------------------------|------------------|-----------------|----------------------|----------------------|----------------------------|
| - (R0)   | 0 (RC1L)            | 0 (RC1L)               | 0 (R)            | 0 (RC1L)        | 0 (RC1L)             | 0 (RC1L)             | 0 (RC1L)                   |
| RES      | LP_READY            | SWDBG_VIO              | SWDBG_STATE      | CAN_TO          | CAN_RXD_REC          | CAN_PERM_REC         | CAN_PERM_DOM               |
| Reserved | LOW-POWER Ready bit | Software debug VIO bit | SWDBG pin status | CAN Timeout Bit | CAN RXD Receiver Bit | CAN Bus Receiver Bit | CAN Permanent Dominant Bit |

**Table 253. DSR6 (0x26) MSB description**

| Bit | Name         | Description                                                                                                                                                             |
|-----|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES          | Reserved                                                                                                                                                                |
| 22  | LP_READY     | 1: Transition from FULL-POWER to LOW-POWER occurred. IRQ generated and this bit is set when this occurs if not masked by MASK_LP_READY_IRQ                              |
| 21  | SWDBG_VIO    | SWDBG is linked to V <sub>IO</sub> up to the end of the timeout following the power-up sequence.<br>If not masked, IRQ is generated and the watchdog starts with L.O.W. |
| 20  | SWDBG_STATE  | The bit shows the current state of SWDBG pin and cannot be cleared ("live bit")<br>1: Input level is high<br>0: Input level is low                                      |
| 19  | CAN_TO       | CAN communication timeout.<br>Bit is set if there is no communication on the bus for $t > t_{\text{Silence}}$ .<br>Bit is latched until a read and clear access.        |
| 18  | CAN_RXD_REC  | RxD_C has not followed TxD_C for 4 times.<br>The CAN transmitter is disabled until the bit is latched until a "Read and clear" command.                                 |
| 17  | CAN_PERM_REC | CAN bus signal did not follow TxD_C for 4 times.<br>The CAN transmitter is disabled until the bit is cleared Bit is latched until a "Read and clear" command.           |
| 16  | CAN_PERM_DOM | CAN bus signal is dominant for $t > t_{\text{CAN}}$ .<br>Bit is latched until a "Read and clear" command                                                                |

**Table 254. DSR6 (0x26)**

| Bit 15               | Bit 14         | Bit 13        | Bit 12            | Bit 11          | Bit 10      | Bit 9           | Bit 8             |
|----------------------|----------------|---------------|-------------------|-----------------|-------------|-----------------|-------------------|
| 0 (RC1L)             | 0 (R)          | 0 (R)         | 0 (R)             | 0 (RC1L)        | 0 (RC1L)    | 0 (RC1L)        | 0 (RC1L)          |
| CAN_TXD_DOM          | FIN1_STATE     | IGN_STATE     | WU_STATE          | IGN_WAKE        | WU_WAKE     | CAN_WAKE        | TIMER_WAKE        |
| CAN TXD Dominant Bit | FIN1 state bit | IGN state bit | Wake-up state bit | IGN wake up bit | Wake-up bit | CAN Wake-up Bit | Timer wake up bit |

**Table 255. DSR6 (0x26) description**

| Bit | Name        | Description                                                                                                                                                                                                                                                                                                                |
|-----|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | CAN_TXD_DOM | TxD_C pin is dominant for $t > t_{dom}(TXDC)$<br>The CAN transmitter is disabled until the bit is cleared Bit is latched until a "Read and clear" command                                                                                                                                                                  |
| 14  | FIN1_STATE  | State of FIN1 input<br>1: Input level is high<br>The bit shows the current state of FIN1 and cannot be cleared ("live bit")<br>0: Input level is low                                                                                                                                                                       |
| 13  | IGN_STATE   | State of IGN input<br>1: Input level is high<br>The bit shows the momentary status of IGN and cannot be cleared ("live bit")<br>Note that the status is only valid if IGN is configured as wake-up input in configuration register (0x05). Otherwise this bit is read at its previous logic state<br>0: Input level is low |
| 12  | WU_STATE    | State of WU input<br>1: Input level is high<br>The bit shows the momentary status of WU and cannot be cleared ("live bit")<br>Note that the status is only valid if WU is configured as wake-up input in configuration register (0x05). Otherwise this bit is read at its previous logic state<br>0: Input level is low    |
| 11  | IGN_WAKE    | Wake-up by IGN: shows wake up source<br>1: Wake-up<br>Bits are latched until a "Read and clear" command                                                                                                                                                                                                                    |
| 10  | WU_WAKE     | Wake-up by WU: shows wake up source<br>1: Wake-up<br>Bits are latched until a "Read and clear" command                                                                                                                                                                                                                     |
| 9   | CAN_WAKE    | Wake-up by CAN: shows wake up source<br>1: Wake-up<br>Bits are latched until a "Read and clear" command                                                                                                                                                                                                                    |
| 8   | TIMER_WAKE  | Wake-up by timer: shows wake up source<br>1: Wake-up<br>Bits are latched until a "Read and clear" command                                                                                                                                                                                                                  |

**Table 256. DSR6 (0x26) LSB**

| Bit 7    | Bit 6     | Bit 5    | Bit 4      | Bit 3    | Bit 2    | Bit 1    | Bit 0    |
|----------|-----------|----------|------------|----------|----------|----------|----------|
| 0 (R)    | 0 (R)     | 0 (RC1L) | 0 (R)      | 0 (RC1L) | 0 (RC1L) | 0 (RC1L) | 0 (RC1L) |
| IRQ_ECHO | NRST_ECHO | IRQ_SENT | NFSO1_ECHO | CRC3     | CRC2     | CRC1     | CRC0     |

| Bit 7              | Bit 6         | Bit 5              | Bit 4          | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|--------------------|---------------|--------------------|----------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| Interrupt echo bit | NRST echo bit | Interrupt sent bit | NFSO1_echo bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 257. DSR6 (0x26) LSB description**

| Bit | Name       | Description                                                           |
|-----|------------|-----------------------------------------------------------------------|
| 7   | IRQ_ECHO   | Indicates current status of IRQ pin.<br>1: High<br>It is a live bit   |
| 6   | NRST_ECHO  | Indicates current status of NRST pin.<br>1: High<br>It is a live bit  |
| 5   | IRQ_SENT   | IRQ sent from IRQ_REQUEST rising<br>1: IRQ sent                       |
| 4   | NFSO1_ECHO | Indicates current status of NFSO1 pin.<br>1: High<br>It is a live bit |
| 3   | CRC 3      |                                                                       |
| 2   | CRC 2      |                                                                       |
| 1   | CRC 1      |                                                                       |
| 0   | CRC 0      |                                                                       |

**Table 258. DSR7 (0x27) MSB**

| Bit 23   | Bit 22                | Bit 21                 | Bit 20                 | Bit 19                 | Bit 18               | Bit 17                   | Bit 16                     |
|----------|-----------------------|------------------------|------------------------|------------------------|----------------------|--------------------------|----------------------------|
| -(R0)    | 0 (RC1L)              | 0 (RC1L)               | 0 (R)                  | 0 (RC1L)               | 0 (R)                | 0 (R)                    | 0 (R)                      |
| RES      | VPOR                  | LDO1_PG_OK             | LDO2_ENA_STATUS        | LDO2_PG_OK             | FCCU_ENA_ECHO        | WD_ENA_ECHO              | WD_TIMER_STATE_1           |
| Reserved | Vs power on reset bit | LDO1 power-good ok bit | LDO2 enable status bit | LDO2 power-good ok bit | FCCU enable echo bit | Watchdog enable echo bit | Watchdog timer state bit 1 |

**Table 259. DSR7 (0x27) MSB description**

| Bit | Name            | Description                                                                                                                                                   |
|-----|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | RES             | Reserved                                                                                                                                                      |
| 22  | VPOR            | V <sub>S</sub> power-on reset threshold (VPOR) reached.<br>Bit is latched until a "Read and clear" command                                                    |
| 21  | LDO1_PG_OK      | Indicates power-good LDO1.<br>Bit is latched until a "Read and clear" command                                                                                 |
| 20  | LDO2_ENA_STATUS | LDO2 enable status bit. Live bit<br>LDO2 is a tracker and when disabled by SPI or UV or OV, this bit indicates the enable status<br>1: Enabled<br>0: Disabled |
| 19  | LDO2_PG_OK      | 1: Power-good reached after the regulator has been turned ON by power-up sequence or through SPI<br>0: PG not reached                                         |
| 18  | FCCU_ENA_ECHO   | echo of FCCU enable signal at FCCU block input<br>1: Indicates that the FCCU is running<br>Live bit                                                           |

| Bit | Name             | Description                                                                                                                                                                            |
|-----|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                  | 0: Indicates that FCCU block is disabled                                                                                                                                               |
| 17  | WD_ENA_ECHO      | echo of WD enable signal at WD block input<br>1: Indicates that the WD is running<br>Live bit<br>0: Indicates that WD block is disabled<br>It occurs in software debug or in test mode |
| 16  | WD_TIMER_STATE_1 | Watchdog timer status<br>00: WD counter in too early window trig<br>01: WD counter in valid window trig<br>11: WD counter in too late window trig                                      |

**Table 260. DSR7 (0x27)**

| Bit 15                     | Bit 14                    | Bit 13                    | Bit 12                    | Bit 11                    | Bit 10                            | Bit 9                             | Bit 8                      |
|----------------------------|---------------------------|---------------------------|---------------------------|---------------------------|-----------------------------------|-----------------------------------|----------------------------|
| 0 (R)                      | 0 (R)                     | 0 (R)                     | 0 (R)                     | 0 (R)                     | 0 (R)                             | 0 (R)                             | 0 (RC1L)                   |
| WD_TIMER_STATE_0           | WDFAIL_CNT_3              | WDFAIL_CNT_2              | WDFAIL_CNT_1              | WDFAIL_CNT_0              | TSD_CNT_FAIL_1                    | TSD_CNT_FAIL_0                    | POWUP_RETRY_CNT_1          |
| Watchdog timer state bit 0 | Watchdog fail count bit 3 | Watchdog fail count bit 2 | Watchdog fail count bit 1 | Watchdog fail count bit 0 | Thermal shutdown fail count bit 1 | Thermal shutdown fail count bit 0 | Power up retry count bit 1 |

**Table 261. DSR7 (0x27) description**

| Bit | Name              | Description                                                                                                                                                                          |
|-----|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | WD_TIMER_STATE_0  |                                                                                                                                                                                      |
| 14  | WDFAIL_CNT_3      | Indicates number of consecutive watchdog trig faults, from 1 to 15<br>Bits cannot be cleared, will be cleared with a valid watchdog trig during a long open window, or in DEEP-SLEEP |
| 13  | WDFAIL_CNT_2      |                                                                                                                                                                                      |
| 12  | WDFAIL_CNT_1      |                                                                                                                                                                                      |
| 11  | WDFAIL_CNT_0      |                                                                                                                                                                                      |
| 10  | TSD_CNT_FAIL_1    | Thermal shut-down sequence retry counter                                                                                                                                             |
| 9   | TSD_CNT_FAIL_0    |                                                                                                                                                                                      |
| 8   | POWUP_RETRY_CNT_1 | Power-up sequence retry counter<br>MCU must clear this counter in REC-1 or ACTIVE state                                                                                              |

**Table 262. DSR7 (0x27) LSB**

| Bit 7                      | Bit 6    | Bit 5              | Bit 4                | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|----------------------------|----------|--------------------|----------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (RC1L)                   | - (R0)   | 0 (RC1L)           | 0 (RC1L)             | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| POWUP_RETRY_CNT_0          | RES      | NVM_PROG_OK        | NVM_PROG_DONE        | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Power up retry count bit 0 | Reserved | NVM program ok bit | NVM program done bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 263. DSR7 (0x27) LSB description**

| Bit | Name              | Description |
|-----|-------------------|-------------|
| 7   | POWUP_RETRY_CNT_0 |             |
| 6   | RES               |             |

| Bit | Name          | Description                                  |
|-----|---------------|----------------------------------------------|
| 5   | NVM_PROG_OK   | U-NVM programming is completed without error |
| 4   | NVM_PROG_DONE | U-NVM programming is completed               |
| 3   | CRC 3         |                                              |
| 2   | CRC 2         |                                              |
| 1   | CRC 1         |                                              |
| 0   | CRC 0         |                                              |

**Table 264. DSR8 (0x28) MSB**

| Bit 23   | Bit 22                  | Bit 21                  | Bit 20                  | Bit 19                 | Bit 18                 | Bit 17                 | Bit 16                 |
|----------|-------------------------|-------------------------|-------------------------|------------------------|------------------------|------------------------|------------------------|
| -(R0)    | 0 (R)                   | 0 (R)                   | 0 (R)                   | 0 (R)                  | 0 (R)                  | 0 (R)                  | 0 (R)                  |
| RES      | FCCU_LAST_STABLE_12     | FCCU_LAST_STABLE_11     | FCCU_LAST_STABLE_10     | FCCU_LAST_STABLE_9     | FCCU_LAST_STABLE_8     | FCCU_LAST_STABLE_7     | FCCU_LAST_STABLE_6     |
| Reserved | FCCU last stable bit 12 | FCCU last stable bit 11 | FCCU last stable bit 10 | FCCU last stable bit 9 | FCCU last stable bit 8 | FCCU last stable bit 7 | FCCU last stable bit 6 |

**Table 265. DSR8 (0x28) MSB description**

| Bit | Name                | Description |
|-----|---------------------|-------------|
| 23  | RES                 | Reserved    |
| 22  | FCCU_LAST_STABLE_12 |             |
| 21  | FCCU_LAST_STABLE_11 |             |
| 20  | FCCU_LAST_STABLE_10 |             |
| 19  | FCCU_LAST_STABLE_9  |             |
| 18  | FCCU_LAST_STABLE_8  |             |
| 17  | FCCU_LAST_STABLE_7  |             |
| 16  | FCCU_LAST_STABLE_6  |             |

**Table 266. DSR8 (0x28)**

| Bit 15                 | Bit 14                 | Bit 13                 | Bit 12                 | Bit 11                 | Bit 10                 | Bit 9                           | Bit 8                        |
|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|---------------------------------|------------------------------|
| 0 (R)                  | 0 (R)                  | 0 (R)                  | 0 (R)                  | 0 (R)                  | 0 (R)                  | 0 (R)                           | 0 (R)                        |
| FCCU_LAST_STABLE_5     | FCCU_LAST_STABLE_4     | FCCU_LAST_STABLE_3     | FCCU_LAST_STABLE_2     | FCCU_LAST_STABLE_1     | FCCU_LAST_STABLE_0     | FORCED_SLEEP_REGFAIL            | REG_FAIL_CNT_1               |
| FCCU last stable bit 5 | FCCU last stable bit 4 | FCCU last stable bit 3 | FCCU last stable bit 2 | FCCU last stable bit 1 | FCCU last stable bit 0 | Forced sleep regulator fail bit | Regulator fail counter bit 1 |

**Table 267. DSR8 (0x28) description**

| Bit | Name                 | Description                                                                                                                                             |
|-----|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | FCCU_LAST_STABLE_5   |                                                                                                                                                         |
| 14  | FCCU_LAST_STABLE_4   |                                                                                                                                                         |
| 13  | FCCU_LAST_STABLE_3   |                                                                                                                                                         |
| 12  | FCCU_LAST_STABLE_2   |                                                                                                                                                         |
| 11  | FCCU_LAST_STABLE_1   |                                                                                                                                                         |
| 10  | FCCU_LAST_STABLE_0   | FCCU monitor: last stable value duration                                                                                                                |
| 9   | FORCED_SLEEP_REGFAIL | 1: When REG_FAIL_CNT = 3, then FSM transitions from REC_2 to DEEP-SLEEP (similar to TSD_CNT_FAIL)<br>0: No transition to DEEP-SLEEP due to REG_FAIL_CNT |
| 8   | REG_FAIL_CNT_1       |                                                                                                                                                         |

**Table 268. DSR8 (0x28) LSB**

| Bit 7                        | Bit 6                   | Bit 5          | Bit 4          | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|------------------------------|-------------------------|----------------|----------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                        | 0 (R)                   | 0 (RC1L)       | 0 (RC1L)       | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| REG_FAIL_CNT_0               | ABIST_BOOST_IGNORED     | LBIST_COMPLETE | ABIST_COMPLETE | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Regulator fail counter bit 0 | ABIST boost ignored bit |                |                | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 269. DSR8 (0x28) LSB description**

| Bit | Name                | Description                                                                                                                                                                       |
|-----|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | REG_FAIL_CNT_0      | REG_FAIL_CNT is incremented when a reg_fail event occurs on any regulator with REGFAIL_GO_REC = 1 (that is one counter for all regulators with REGFAIL_GO_REC = 1)                |
| 6   | ABIST_BOOST_IGNORED | 1: Boost PWM activity has been detected during the ABIST test. So the BOOST comparator has not been covered by ABIST to not signal a wrong ABIST error<br>0: Boost ABIST well run |
| 5   | LBIST_COMPLETE      | Define logical BIST ending<br>1: LBIST is complete<br>0: LBIST not complete or not running                                                                                        |
| 4   | ABIST_COMPLETE      | Define analog BIST ending<br>1: ABIST is complete<br>0: ABIST not complete or not running                                                                                         |
| 3   | CRC 3               |                                                                                                                                                                                   |
| 2   | CRC 2               |                                                                                                                                                                                   |
| 1   | CRC 1               |                                                                                                                                                                                   |
| 0   | CRC 0               |                                                                                                                                                                                   |

**Table 270. DSR9 (0x29) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19   | Bit 18   | Bit 17   | Bit 16   |
|----------|----------|----------|----------|----------|----------|----------|----------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   |
| RES      | RES      | RES      | RES      | RES      | RES      | RES      | RES      |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

**Table 271. DSR9 (0x29) MSB description**

| Bit | Name | Description |
|-----|------|-------------|
| 23  | RES  | Reserved    |
| 22  | RES  | Reserved    |
| 21  | RES  | Reserved    |
| 20  | RES  | Reserved    |
| 19  | RES  | Reserved    |
| 18  | RES  | Reserved    |
| 17  | RES  | Reserved    |
| 16  | RES  | Reserved    |

**Table 272. DSR9 (0x29)**

| Bit 15   | Bit 14   | Bit 13                            | Bit 12                            | Bit 11                            | Bit 10                            | Bit 9                             | Bit 8                             |
|----------|----------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| - (R0)   | - (R0)   | 0 (R)                             | 0 (R)                             | 0 (R)                             | 0 (R)                             | 0 (R)                             | 0 (R)                             |
| RES      | RES      | TEMP_CL0_9                        | TEMP_CL0_8                        | TEMP_CL0_7                        | TEMP_CL0_6                        | TEMP_CL0_5                        | TEMP_CL0_4                        |
| Reserved | Reserved | Temperature central cluster bit 9 | Temperature central cluster bit 8 | Temperature central cluster bit 7 | Temperature central cluster bit 6 | Temperature central cluster bit 5 | Temperature central cluster bit 4 |

**Table 273. DSR9 (0x29) description**

| Bit | Name       | Description                                                                                                           |
|-----|------------|-----------------------------------------------------------------------------------------------------------------------|
| 15  | RES        | Reserved                                                                                                              |
| 14  | RES        | Reserved                                                                                                              |
| 13  | TEMP_CL0_9 | Temperature cluster 0 (central cluster)<br>Bits cannot be cleared<br>(a clear command generates a SPI_UNDEF_ADD flag) |
| 12  | TEMP_CL0_8 |                                                                                                                       |
| 11  | TEMP_CL0_7 |                                                                                                                       |
| 10  | TEMP_CL0_6 |                                                                                                                       |
| 9   | TEMP_CL0_5 |                                                                                                                       |
| 8   | TEMP_CL0_4 |                                                                                                                       |

**Table 274. DSR9 (0x29) LSB**

| Bit 7                             | Bit 6                             | Bit 5                             | Bit 4                             | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                             | 0 (R)                             | 0 (R)                             | 0 (R)                             | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| TEMP_CL0_3                        | TEMP_CL0_2                        | TEMP_CL0_1                        | TEMP_CL0_0                        | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Temperature central cluster bit 3 | Temperature central cluster bit 2 | Temperature central cluster bit 1 | Temperature central cluster bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 275. DSR9 (0x29) LSB description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 7   | TEMP_CL0_3 |             |
| 6   | TEMP_CL0_2 |             |
| 5   | TEMP_CL0_1 |             |
| 4   | TEMP_CL0_0 |             |
| 3   | CRC 3      |             |
| 2   | CRC 2      |             |
| 1   | CRC 1      |             |
| 0   | CRC 0      |             |

**Table 276. DSR10 (0x2A) MSB**

| Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| - (R0) | - (R0) | - (R0) | - (R0) | - (R0) | - (R0) | - (R0) | - (R0) |

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19   | Bit 18   | Bit 17   | Bit 16   |
|----------|----------|----------|----------|----------|----------|----------|----------|
| RES      | RES      | RES      | RES      | RES      | RES      | RES      | RES      |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

**Table 277. DSR10 (0x2A) MSB description**

| Bit | Name | Description |
|-----|------|-------------|
| 23  | RES  | Reserved    |
| 22  | RES  | Reserved    |
| 21  | RES  | Reserved    |
| 20  | RES  | Reserved    |
| 19  | RES  | Reserved    |
| 18  | RES  | Reserved    |
| 17  | RES  | Reserved    |
| 16  | RES  | Reserved    |

**Table 278. DSR10 (0x2A)**

| Bit 15   | Bit 14   | Bit 13                      | Bit 12                      | Bit 11                      | Bit 10                      | Bit 9                       | Bit 8                       |
|----------|----------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| - (R0)   | - (R0)   | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       |
| RES      | RES      | TEMP_CL1_9                  | TEMP_CL1_8                  | TEMP_CL1_7                  | TEMP_CL1_6                  | TEMP_CL1_5                  | TEMP_CL1_4                  |
| Reserved | Reserved | Temperature cluster 1 bit 9 | Temperature cluster 1 bit 8 | Temperature cluster 1 bit 7 | Temperature cluster 1 bit 6 | Temperature cluster 1 bit 5 | Temperature cluster 1 bit 4 |

**Table 279. DSR10 (0x2A) description**

| Bit | Name       | Description                                                                                         |
|-----|------------|-----------------------------------------------------------------------------------------------------|
| 15  | RES        | Reserved                                                                                            |
| 14  | RES        | Reserved                                                                                            |
| 13  | TEMP_CL1_9 | Temperature cluster 1<br>Bits cannot be cleared<br>(a clear command generates a SPI_UNDEF_ADD flag) |
| 12  | TEMP_CL1_8 |                                                                                                     |
| 11  | TEMP_CL1_7 |                                                                                                     |
| 10  | TEMP_CL1_6 |                                                                                                     |
| 9   | TEMP_CL1_5 |                                                                                                     |
| 8   | TEMP_CL1_4 |                                                                                                     |

**Table 280. DSR10 (0x2A) LSB**

| Bit 7                       | Bit 6                       | Bit 5                       | Bit 4                       | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| TEMP_CL1_3                  | TEMP_CL1_2                  | TEMP_CL1_1                  | TEMP_CL1_0                  | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Temperature cluster 1 bit 3 | Temperature cluster 1 bit 2 | Temperature cluster 1 bit 1 | Temperature cluster 1 bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 281. DSR10 (0x2A) LSB description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 7   | TEMP_CL1_3 |             |
| 6   | TEMP_CL1_2 |             |
| 5   | TEMP_CL1_1 |             |
| 4   | TEMP_CL1_0 |             |
| 3   | CRC 3      |             |
| 2   | CRC 2      |             |
| 1   | CRC 1      |             |
| 0   | CRC 0      |             |

**Table 282. DSR11 (0x2B) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19   | Bit 18   | Bit 17   | Bit 16   |
|----------|----------|----------|----------|----------|----------|----------|----------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   |
| RES      | RES      | RES      | RES      | RES      | RES      | RES      | RES      |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

**Table 283. DSR11 (0x2B) MSB description**

| Bit | Name | Description |
|-----|------|-------------|
| 23  | RES  | Reserved    |
| 22  | RES  | Reserved    |
| 21  | RES  | Reserved    |
| 20  | RES  | Reserved    |
| 19  | RES  | Reserved    |
| 18  | RES  | Reserved    |
| 17  | RES  | Reserved    |
| 16  | RES  | Reserved    |

**Table 284. DSR11 (0x2B)**

| Bit 15   | Bit 14   | Bit 13                      | Bit 12                      | Bit 11                      | Bit 10                      | Bit 9                       | Bit 8                       |
|----------|----------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| - (R0)   | - (R0)   | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       |
| RES      | RES      | TEMP_CL2_9                  | TEMP_CL2_8                  | TEMP_CL2_7                  | TEMP_CL2_6                  | TEMP_CL2_5                  | TEMP_CL2_4                  |
| Reserved | Reserved | Temperature cluster 2 bit 9 | Temperature cluster 2 bit 8 | Temperature cluster 2 bit 7 | Temperature cluster 2 bit 6 | Temperature cluster 2 bit 5 | Temperature cluster 2 bit 4 |

**Table 285. DSR11 (0x2B) description**

| Bit | Name       | Description                                                                                         |
|-----|------------|-----------------------------------------------------------------------------------------------------|
| 15  | RES        | Reserved                                                                                            |
| 14  | RES        | Reserved                                                                                            |
| 13  | TEMP_CL2_9 | Temperature cluster 2<br>Bits cannot be cleared<br>(a clear command generates a SPI_UNDEF_ADD flag) |

| Bit | Name       | Description |
|-----|------------|-------------|
| 12  | TEMP_CL2_8 |             |
| 11  | TEMP_CL2_7 |             |
| 10  | TEMP_CL2_6 |             |
| 9   | TEMP_CL2_5 |             |
| 8   | TEMP_CL2_4 |             |

**Table 286. DSR11 (0x2B) LSB**

| Bit 7                       | Bit 6                       | Bit 5                       | Bit 4                       | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| TEMP_CL2_3                  | TEMP_CL2_2                  | TEMP_CL2_1                  | TEMP_CL2_0                  | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Temperature cluster 2 bit 3 | Temperature cluster 2 bit 2 | Temperature cluster 2 bit 1 | Temperature cluster 2 bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 287. DSR11 (0x2B) LSB description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 7   | TEMP_CL2_3 |             |
| 6   | TEMP_CL2_2 |             |
| 5   | TEMP_CL2_1 |             |
| 4   | TEMP_CL2_0 |             |
| 3   | CRC 3      |             |
| 2   | CRC 2      |             |
| 1   | CRC 1      |             |
| 0   | CRC 0      |             |

**Table 288. DSR12 (0x2C) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19   | Bit 18   | Bit 17   | Bit 16   |
|----------|----------|----------|----------|----------|----------|----------|----------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   |
| RES      | RES      | RES      | RES      | RES      | RES      | RES      | RES      |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

**Table 289. DSR12 (0x2C) MSB description**

| Bit | Name | Description |
|-----|------|-------------|
| 23  | RES  | Reserved    |
| 22  | RES  | Reserved    |
| 21  | RES  | Reserved    |
| 20  | RES  | Reserved    |
| 19  | RES  | Reserved    |
| 18  | RES  | Reserved    |
| 17  | RES  | Reserved    |
| 16  | RES  | Reserved    |

**Table 290. DSR12 (0x2C)**

| Bit 15   | Bit 14   | Bit 13                      | Bit 12                      | Bit 11                      | Bit 10                      | Bit 9                       | Bit 8                       |
|----------|----------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| - (R0)   | - (R0)   | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       |
| RES      | RES      | TEMP_CL3_9                  | TEMP_CL3_8                  | TEMP_CL3_7                  | TEMP_CL3_6                  | TEMP_CL3_5                  | TEMP_CL3_4                  |
| Reserved | Reserved | Temperature cluster 3 bit 9 | Temperature cluster 3 bit 8 | Temperature cluster 3 bit 7 | Temperature cluster 3 bit 6 | Temperature cluster 3 bit 5 | Temperature cluster 3 bit 4 |

**Table 291. DSR12 (0x2C) description**

| Bit | Name       | Description                                                                                         |
|-----|------------|-----------------------------------------------------------------------------------------------------|
| 15  | RES        | Reserved                                                                                            |
| 14  | RES        | Reserved                                                                                            |
| 13  | TEMP_CL3_9 | Temperature cluster 3<br>Bits cannot be cleared<br>(a clear command generates a SPI_UNDEF_ADD flag) |
| 12  | TEMP_CL3_8 |                                                                                                     |
| 11  | TEMP_CL3_7 |                                                                                                     |
| 10  | TEMP_CL3_6 |                                                                                                     |
| 9   | TEMP_CL3_5 |                                                                                                     |
| 8   | TEMP_CL3_4 |                                                                                                     |

**Table 292. DSR12 (0x2C) LSB**

| Bit 7                       | Bit 6                       | Bit 5                       | Bit 4                       | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| TEMP_CL3_3                  | TEMP_CL3_2                  | TEMP_CL3_1                  | TEMP_CL3_0                  | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Temperature cluster 3 bit 3 | Temperature cluster 3 bit 2 | Temperature cluster 3 bit 1 | Temperature cluster 3 bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 293. DSR12 (0x2C) LSB description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 7   | TEMP_CL3_3 |             |
| 6   | TEMP_CL3_2 |             |
| 5   | TEMP_CL3_1 |             |
| 4   | TEMP_CL3_0 |             |
| 3   | CRC 3      |             |
| 2   | CRC 2      |             |
| 1   | CRC 1      |             |
| 0   | CRC 0      |             |

**Table 294. DSR13 (0x2D) MSB**

| Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| - (R0) | - (R0) | - (R0) | - (R0) | - (R0) | - (R0) | - (R0) | - (R0) |
| RES    | RES    | RES    | RES    | RES    | RES    | RES    | RES    |

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19   | Bit 18   | Bit 17   | Bit 16   |
|----------|----------|----------|----------|----------|----------|----------|----------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

**Table 295. DSR13 (0x2D) MSB description**

| Bit | Name | Description |
|-----|------|-------------|
| 23  | RES  | Reserved    |
| 22  | RES  | Reserved    |
| 21  | RES  | Reserved    |
| 20  | RES  | Reserved    |
| 19  | RES  | Reserved    |
| 18  | RES  | Reserved    |
| 17  | RES  | Reserved    |
| 16  | RES  | Reserved    |

**Table 296. DSR13 (0x2D)**

| Bit 15   | Bit 14   | Bit 13                      | Bit 12                      | Bit 11                      | Bit 10                      | Bit 9                       | Bit 8                       |
|----------|----------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| - (R0)   | - (R0)   | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       |
| RES      | RES      | TEMP_CL4_9                  | TEMP_CL4_8                  | TEMP_CL4_7                  | TEMP_CL4_6                  | TEMP_CL4_5                  | TEMP_CL4_4                  |
| Reserved | Reserved | Temperature cluster 4 bit 9 | Temperature cluster 4 bit 8 | Temperature cluster 4 bit 7 | Temperature cluster 4 bit 6 | Temperature cluster 4 bit 5 | Temperature cluster 4 bit 4 |

**Table 297. DSR13 (0x2D) description**

| Bit | Name       | Description                                                                                         |
|-----|------------|-----------------------------------------------------------------------------------------------------|
| 15  | RES        | Reserved                                                                                            |
| 14  | RES        | Reserved                                                                                            |
| 13  | TEMP_CL4_9 | Temperature cluster 4<br>Bits cannot be cleared<br>(a clear command generates a SPI_UNDEF_ADD flag) |
| 12  | TEMP_CL4_8 |                                                                                                     |
| 11  | TEMP_CL4_7 |                                                                                                     |
| 10  | TEMP_CL4_6 |                                                                                                     |
| 9   | TEMP_CL4_5 |                                                                                                     |
| 8   | TEMP_CL4_4 |                                                                                                     |

**Table 298. DSR13 (0x2D) LSB**

| Bit 7                       | Bit 6                       | Bit 5                       | Bit 4                       | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| TEMP_CL4_3                  | TEMP_CL4_2                  | TEMP_CL4_1                  | TEMP_CL4_0                  | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Temperature cluster 4 bit 3 | Temperature cluster 4 bit 2 | Temperature cluster 4 bit 1 | Temperature cluster 4 bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 299. DSR13 (0x2D) LSB description**

| Bit | Name       | Description |
|-----|------------|-------------|
| 7   | TEMP_CL4_3 |             |
| 6   | TEMP_CL4_2 |             |
| 5   | TEMP_CL4_1 |             |
| 4   | TEMP_CL4_0 |             |
| 3   | CRC 3      |             |
| 2   | CRC 2      |             |
| 1   | CRC 1      |             |
| 0   | CRC 0      |             |

**Table 300. DSR14 (0x2E) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19   | Bit 18   | Bit 17   | Bit 16   |
|----------|----------|----------|----------|----------|----------|----------|----------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   |
| RES      | RES      | RES      | RES      | RES      | RES      | RES      | RES      |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

**Table 301. DSR14 (0x2E) MSB description**

| Bit | Name | Description |
|-----|------|-------------|
| 23  | RES  | Reserved    |
| 22  | RES  | Reserved    |
| 21  | RES  | Reserved    |
| 20  | RES  | Reserved    |
| 19  | RES  | Reserved    |
| 18  | RES  | Reserved    |
| 17  | RES  | Reserved    |
| 16  | RES  | Reserved    |

**Table 302. DSR14 (0x2E)**

| Bit 15   | Bit 14   | Bit 13                 | Bit 12                 | Bit 11                 | Bit 10                 | Bit 9                  | Bit 8                  |
|----------|----------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| - (R0)   | - (R0)   | 0 (R)                  | 0 (R)                  | 0 (R)                  | 0 (R)                  | 0 (R)                  | 0 (R)                  |
| RES      | RES      | VS_9                   | VS_8                   | VS_7                   | VS_6                   | VS_5                   | VS_4                   |
| Reserved | Reserved | VS voltage Level bit 9 | VS voltage Level bit 8 | VS voltage Level bit 7 | VS voltage Level bit 6 | VS voltage Level bit 5 | VS voltage Level bit 4 |

**Table 303. DSR14 (0x2E)**

| Bit | Name | Description                                                                                           |
|-----|------|-------------------------------------------------------------------------------------------------------|
| 15  | RES  | Reserved                                                                                              |
| 14  | RES  | Reserved                                                                                              |
| 13  | VS_9 | Voltage level on VS pin<br>Bits cannot be cleared<br>(a clear command generates a SPI_UNDEF_ADD flag) |

| Bit | Name | Description |
|-----|------|-------------|
| 12  | VS_8 |             |
| 11  | VS_7 |             |
| 10  | VS_6 |             |
| 9   | VS_5 |             |
| 8   | VS_4 |             |

**Table 304. DSR14 (0x2E) LSB**

| Bit 7                  | Bit 6                  | Bit 5                  | Bit 4                  | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|------------------------|------------------------|------------------------|------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                  | 0 (R)                  | 0 (R)                  | 0 (R)                  | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| VS_3                   | VS_2                   | VS_1                   | VS_0                   | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| VS voltage Level bit 3 | VS voltage Level bit 2 | VS voltage Level bit 1 | VS voltage Level bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 305. DSR14 (0x2E) LSB description**

| Bit | Name  | Description |
|-----|-------|-------------|
| 7   | VS_3  |             |
| 6   | VS_2  |             |
| 5   | VS_1  |             |
| 4   | VS_0  |             |
| 3   | CRC 3 |             |
| 2   | CRC 2 |             |
| 1   | CRC 1 |             |
| 0   | CRC 0 |             |

**Table 306. DSR15 (0x2F) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19   | Bit 18   | Bit 17   | Bit 16   |
|----------|----------|----------|----------|----------|----------|----------|----------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   |
| RES      | RES      | RES      | RES      | RES      | RES      | RES      | RES      |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

**Table 307. DSR15 (0x2F) MSB**

| Bit | Name | Description |
|-----|------|-------------|
| 23  | RES  | Reserved    |
| 22  | RES  | Reserved    |
| 21  | RES  | Reserved    |
| 20  | RES  | Reserved    |
| 19  | RES  | Reserved    |
| 18  | RES  | Reserved    |
| 17  | RES  | Reserved    |
| 16  | RES  | Reserved    |

**Table 308. DSR15 (0x2F)**

| Bit 15   | Bit 14   | Bit 13                      | Bit 12                      | Bit 11                      | Bit 10                      | Bit 9                       | Bit 8                       |
|----------|----------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| - (R0)   | - (R0)   | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       |
| RES      | RES      | WU_9                        | WU_8                        | WU_7                        | WU_6                        | WU_5                        | WU_4                        |
| Reserved | Reserved | Wake-up voltage level bit 9 | Wake-up voltage level bit 8 | Wake-up voltage level bit 7 | Wake-up voltage level bit 6 | Wake-up voltage level bit 5 | Wake-up voltage level bit 4 |

**Table 309. DSR15 (0x2F) description**

| Bit | Name | Description                                                                                           |
|-----|------|-------------------------------------------------------------------------------------------------------|
| 15  | RES  | Reserved                                                                                              |
| 14  | RES  | Reserved                                                                                              |
| 13  | WU_9 | Voltage level on WU pin<br>Bits cannot be cleared<br>(a clear command generates a SPI_UNDEF_ADD flag) |
| 12  | WU_8 |                                                                                                       |
| 11  | WU_7 |                                                                                                       |
| 10  | WU_6 |                                                                                                       |
| 9   | WU_5 |                                                                                                       |
| 8   | WU_4 |                                                                                                       |

**Table 310. DSR15 (0x2F) LSB**

| Bit 7                       | Bit 6                       | Bit 5                       | Bit 4                       | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (R)                       | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| WU_3                        | WU_2                        | WU_1                        | WU_0                        | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Wake-up voltage level bit 3 | Wake-up voltage level bit 2 | Wake-up voltage level bit 1 | Wake-up voltage level bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 311. DSR15 (0x2F) LSB description**

| Bit | Name  | Description |
|-----|-------|-------------|
| 7   | WU_3  |             |
| 6   | WU_2  |             |
| 5   | WU_1  |             |
| 4   | WU_0  |             |
| 3   | CRC 3 |             |
| 2   | CRC 2 |             |
| 1   | CRC 1 |             |
| 0   | CRC 0 |             |

**Table 312. DSR16 (0x30) MSB**

| Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| - (R0) | - (R0) | - (R0) | - (R0) | - (R0) | - (R0) | - (R0) | - (R0) |
| RES    | RES    | RES    | RES    | RES    | RES    | RES    | RES    |

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19   | Bit 18   | Bit 17   | Bit 16   |
|----------|----------|----------|----------|----------|----------|----------|----------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

**Table 313. DSR16 (0x30) MSB description**

| Bit | Name | Description |
|-----|------|-------------|
| 23  | RES  | Reserved    |
| 22  | RES  | Reserved    |
| 21  | RES  | Reserved    |
| 20  | RES  | Reserved    |
| 19  | RES  | Reserved    |
| 18  | RES  | Reserved    |
| 17  | RES  | Reserved    |
| 16  | RES  | Reserved    |

**Table 314. DSR16 (0x30)**

| Bit 15   | Bit 14   | Bit 13                  | Bit 12                  | Bit 11                  | Bit 10                  | Bit 9                   | Bit 8                   |
|----------|----------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| - (R0)   | - (R0)   | 0 (R)                   | 0 (R)                   | 0 (R)                   | 0 (R)                   | 0 (R)                   | 0 (R)                   |
| RES      | RES      | IGN_9                   | IGN_8                   | IGN_7                   | IGN_6                   | IGN_5                   | IGN_4                   |
| Reserved | Reserved | IGN voltage level bit 9 | IGN voltage level bit 8 | IGN voltage level bit 7 | IGN voltage level bit 6 | IGN voltage level bit 5 | IGN voltage level bit 4 |

**Table 315. DSR16 (0x30) description**

| Bit | Name  | Description                                                                                            |
|-----|-------|--------------------------------------------------------------------------------------------------------|
| 15  | RES   | Reserved                                                                                               |
| 14  | RES   | Reserved                                                                                               |
| 13  | IGN_9 | Voltage level on IGN pin<br>Bits cannot be cleared<br>(a clear command generates a SPI_UNDEF_ADD flag) |
| 12  | IGN_8 |                                                                                                        |
| 11  | IGN_7 |                                                                                                        |
| 10  | IGN_6 |                                                                                                        |
| 9   | IGN_5 |                                                                                                        |
| 8   | IGN_4 |                                                                                                        |

**Table 316. DSR16 (0x30) LSB**

| Bit 7                   | Bit 6                   | Bit 5                   | Bit 4                   | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-------------------------|-------------------------|-------------------------|-------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                   | 0 (R)                   | 0 (R)                   | 0 (R)                   | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| IGN_3                   | IGN_2                   | IGN_1                   | IGN_0                   | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| IGN voltage level bit 3 | IGN voltage level bit 2 | IGN voltage level bit 1 | IGN voltage level bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 317. DSR16 (0x30) LSB description**

| Bit | Name  | Description |
|-----|-------|-------------|
| 7   | IGN_3 |             |
| 6   | IGN_2 |             |
| 5   | IGN_1 |             |
| 4   | IGN_0 |             |
| 3   | CRC 3 |             |
| 2   | CRC 2 |             |
| 1   | CRC 1 |             |
| 0   | CRC 0 |             |

**Table 318. DSR17 (0x31) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20   | Bit 19   | Bit 18   | Bit 17   | Bit 16   |
|----------|----------|----------|----------|----------|----------|----------|----------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   |
| RES      | RES      | RES      | RES      | RES      | RES      | RES      | RES      |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

**Table 319. DSR17 (0x31) MSB description**

| Bit | Name | Description |
|-----|------|-------------|
| 23  | RES  | Reserved    |
| 22  | RES  | Reserved    |
| 21  | RES  | Reserved    |
| 20  | RES  | Reserved    |
| 19  | RES  | Reserved    |
| 18  | RES  | Reserved    |
| 17  | RES  | Reserved    |
| 16  | RES  | Reserved    |

**Table 320. DSR17 (0x31)**

| Bit 15   | Bit 14   | Bit 13                  | Bit 12                  | Bit 11                  | Bit 10                  | Bit 9                   | Bit 8                   |
|----------|----------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| - (R0)   | - (R0)   | 0 (R)                   | 0 (R)                   | 0 (R)                   | 0 (R)                   | 0 (R)                   | 0 (R)                   |
| RES      | RES      | FBB_9                   | FBB_8                   | FBB_7                   | FBB_6                   | FBB_5                   | FBB_4                   |
| Reserved | Reserved | FBB voltage level bit 9 | FBB voltage level bit 8 | FBB voltage level bit 7 | FBB voltage level bit 6 | FBB voltage level bit 5 | FBB voltage level bit 4 |

**Table 321. DSR17 (0x31) description**

| Bit | Name  | Description                                                                                            |
|-----|-------|--------------------------------------------------------------------------------------------------------|
| 15  | RES   | Reserved                                                                                               |
| 14  | RES   | Reserved                                                                                               |
| 13  | FBB_9 | Voltage level on FBB pin<br>Bits cannot be cleared<br>(a clear command generates a SPI_UNDEF_ADD flag) |

| Bit | Name  | Description |
|-----|-------|-------------|
| 12  | FBB_8 |             |
| 11  | FBB_7 |             |
| 10  | FBB_6 |             |
| 9   | FBB_5 |             |
| 8   | FBB_4 |             |

**Table 322. DSR17 (0x31) LSB**

| Bit 7                   | Bit 6                   | Bit 5                   | Bit 4                   | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-------------------------|-------------------------|-------------------------|-------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                   | 0 (R)                   | 0 (R)                   | 0 (R)                   | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| FBB_3                   | FBB_2                   | FBB_1                   | FBB_0                   | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| FBB voltage Level bit 3 | FBB voltage Level bit 2 | FBB voltage Level bit 1 | FBB voltage Level bit 0 | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 323. DSR17 (0x31) LSB description**

| Bit | Name  | Description |
|-----|-------|-------------|
| 7   | FBB_3 |             |
| 6   | FBB_2 |             |
| 5   | FBB_1 |             |
| 4   | FBB_0 |             |
| 3   | CRC 3 |             |
| 2   | CRC 2 |             |
| 1   | CRC 1 |             |
| 0   | CRC 0 |             |

**Table 324. DSR18 (0x32) MSB**

| Bit 23   | Bit 22   | Bit 21   | Bit 20                  | Bit 19                  | Bit 18                        | Bit 17                     | Bit 16                     |
|----------|----------|----------|-------------------------|-------------------------|-------------------------------|----------------------------|----------------------------|
| - (R0)   | - (R0)   | - (R0)   | 0 (RC1L)                | 0 (RC1L)                | 0 (RC1L)                      | 0 (R)                      | 0 (R)                      |
| RES      | RES      | RES      | BUCK2_FBLOSS            | BUCK1_FBLOSS            | NVM_COMPARE_ENA_STATUS        | WD_TIME_STATUS_3           | WD_TIME_STATUS_2           |
| Reserved | Reserved | Reserved | BUCK2 feedback loss bit | BUCK1 feedback loss bit | NVM compare enable status bit | Watchdog time status bit 3 | Watchdog time status bit 2 |

**Table 325. DSR18 (0x32) MSB description**

| Bit | Name                   | Description                              |
|-----|------------------------|------------------------------------------|
| 23  | RES                    | Reserved                                 |
| 22  | RES                    | Reserved                                 |
| 21  | RES                    | Reserved                                 |
| 20  | BUCK2_FBLOSS           | 1: BUCK2 FB pin detection<br>0: No error |
| 19  | BUCK1_FBLOSS           | 1: BUCK1 FB pin detection<br>0: No error |
| 18  | NVM_COMPARE_ENA_STATUS | Live bit                                 |
| 17  | WD_TIME_STATUS_3       | Live bit                                 |
| 16  | WD_TIME_STATUS_2       | Live bit                                 |

**Table 326. DSR18 (0x32)**

| Bit 15                     | Bit 14                     | Bit 13                   | Bit 12                   | Bit 11                   | Bit 10                 | Bit 9                   | Bit 8          |
|----------------------------|----------------------------|--------------------------|--------------------------|--------------------------|------------------------|-------------------------|----------------|
| 0 (R)                      | 0 (R)                      | 0 (R)                    | 0 (R)                    | 0 (R)                    | 0 (R)                  | 0 (R)                   | 0 (R)          |
| WD_TIME_STATUS_1           | WD_TIME_STATUS_0           | VBUCK3_ENA_STATUS        | VBUCK2_ENA_STATUS        | VBUCK1_ENA_STATUS        | LDO1_ENA_STATUS        | OUTHS_ENA_STATUS        | LOW_STATUS     |
| Watchdog time status bit 1 | Watchdog time status bit 0 | VBUCK3 enable status bit | VBUCK2 enable status bit | VBUCK1 enable status bit | LDO1 enable status bit | OUTHS enable status bit | LOW status bit |

**Table 327. DSR18 (0x32) description**

| Bit | Name              | Description                                                                                                                                   |
|-----|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | WD_TIME_STATUS_1  | Live bit                                                                                                                                      |
| 14  | WD_TIME_STATUS_0  | Live bit                                                                                                                                      |
| 13  | VBUCK3_ENA_STATUS | Live bit                                                                                                                                      |
| 12  | VBUCK2_ENA_STATUS | Live bit                                                                                                                                      |
| 11  | VBUCK1_ENA_STATUS | Live bit                                                                                                                                      |
| 10  | LDO1_ENA_STATUS   | Live bit                                                                                                                                      |
| 9   | OUTHS_ENA_STATUS  | Live bit                                                                                                                                      |
| 8   | LOW_STATUS        | Live bit<br>1: Watchdog is counting in LOW. Current window is LOW_SET<br>0: Watchdog is not counting in LOW. Current window is WD_TIME_STATUS |

**Table 328. DSR18 (0x32) LSB**

| Bit 7                   | Bit 6                  | Bit 5                 | Bit 4                    | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|-------------------------|------------------------|-----------------------|--------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                   | 0 (R)                  | 0 (R)                 | 0 (R)                    | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| BOOST_ENA_STATUS        | FCCU_ENA_STATUS        | CAN_ACT_STATUS        | CAN_AUTO_BIAS_STATUS     | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Boost enable status bit | FCCU enable status bit | CAN active status bit | CAN Auto Bias status bit | Cyclic redundancy checking bit 3 | Cyclic redundancy checking bit 2 | Cyclic redundancy checking bit 1 | Cyclic redundancy checking bit 0 |

**Table 329. DSR18 (0x32) LSB description**

| Bit | Name                 | Description |
|-----|----------------------|-------------|
| 7   | BOOST_ENA_STATUS     | Live bit    |
| 6   | FCCU_ENA_STATUS      | Live bit    |
| 5   | CAN_ACT_STATUS       | Live bit    |
| 4   | CAN_AUTO_BIAS_STATUS | Live bit    |
| 3   | CRC 3                |             |
| 2   | CRC 2                |             |
| 1   | CRC 1                |             |
| 0   | CRC 0                |             |

**Table 330. DSR19 (0x33) MSB**

| Bit 23   | Bit 22                           | Bit 21                           | Bit 20                           | Bit 19                           | Bit 18                           | Bit 17                           | Bit 16                           |
|----------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| - (R0)   | - (R0)                           | - (R0)                           | 0 (R)                            | 0 (R)                            | 0 (R)                            | 0 (R)                            | 0 (R)                            |
| RES      | LDT_TIMER_VALUE_23               | LDT_TIMER_VALUE_22               | LDT_TIMER_VALUE_21               | LDT_TIMER_VALUE_20               | LDT_TIMER_VALUE_19               | LDT_TIMER_VALUE_18               | LDT_TIMER_VALUE_17               |
| reserved | Long Duration Timer value Bit 23 | Long Duration Timer value Bit 22 | Long Duration Timer value Bit 21 | Long Duration Timer value Bit 20 | Long Duration Timer value Bit 19 | Long Duration Timer value Bit 18 | Long Duration Timer value Bit 17 |

**Table 331. DSR19 (0x33) MSB description**

| Bit | Name               | Description |
|-----|--------------------|-------------|
| 23  | RES                | reserved    |
| 22  | LDT_TIMER_VALUE_23 | Live bit    |
| 21  | LDT_TIMER_VALUE_22 | Live bit    |
| 20  | LDT_TIMER_VALUE_21 | Live bit    |
| 19  | LDT_TIMER_VALUE_20 | Live bit    |
| 18  | LDT_TIMER_VALUE_19 | Live bit    |
| 17  | LDT_TIMER_VALUE_18 | Live bit    |
| 16  | LDT_TIMER_VALUE_17 | Live bit    |

**Table 332. DSR19 (0x33)**

| Bit 15                           | Bit 14                           | Bit 13                           | Bit 12                           | Bit 11                           | Bit 10                           | Bit 9                            | Bit 8                           |
|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|---------------------------------|
| 0 (R)                            | 0 (R)                            | 0 (R)                            | 0 (R)                            | 0 (R)                            | 0 (R)                            | 0 (R)                            | 0 (R)                           |
| LDT_TIMER_VALUE_16               | LDT_TIMER_VALUE_15               | LDT_TIMER_VALUE_14               | LDT_TIMER_VALUE_13               | LDT_TIMER_VALUE_12               | LDT_TIMER_VALUE_11               | LDT_TIMER_VALUE_10               | LDT_TIMER_VALUE_9               |
| Long Duration Timer value Bit 16 | Long Duration Timer value Bit 15 | Long Duration Timer value Bit 14 | Long Duration Timer value Bit 13 | Long Duration Timer value Bit 12 | Long Duration Timer value Bit 11 | Long Duration Timer value Bit 10 | Long Duration Timer value Bit 9 |

**Table 333. DSR19 (0x33) description**

| Bit | Name               | Description |
|-----|--------------------|-------------|
| 15  | LDT_TIMER_VALUE_16 | Live bit    |
| 14  | LDT_TIMER_VALUE_15 | Live bit    |
| 13  | LDT_TIMER_VALUE_14 | Live bit    |
| 12  | LDT_TIMER_VALUE_13 | Live bit    |
| 11  | LDT_TIMER_VALUE_12 | Live bit    |
| 10  | LDT_TIMER_VALUE_11 | Live bit    |
| 9   | LDT_TIMER_VALUE_10 | Live bit    |
| 8   | LDT_TIMER_VALUE_9  | Live bit    |

**Table 334. DSR19 (0x33) LSB**

| Bit 7                           | Bit 6                           | Bit 5                           | Bit 4                           | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|---------------------------------|---------------------------------|---------------------------------|---------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 0 (R)                           | 0 (R)                           | 0 (R)                           | 0 (R)                           | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| LDT_TIMER_VALUE_8               | LDT_TIMER_VALUE_7               | LDT_TIMER_VALUE_6               | LDT_TIMER_VALUE_5               | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| Long Duration Timer value Bit 8 | Long Duration Timer value Bit 7 | Long Duration Timer value Bit 6 | Long Duration Timer value Bit 5 | Cyclic Redundancy Checking Bit 3 | Cyclic Redundancy Checking Bit 2 | Cyclic Redundancy Checking Bit 1 | Cyclic Redundancy Checking Bit 0 |

**Table 335. DSR19 (0x33) LSB description**

| Bit | Name              | Description |
|-----|-------------------|-------------|
| 7   | LDT_TIMER_VALUE_8 | Live Bit    |
| 6   | LDT_TIMER_VALUE_7 | Live Bit    |
| 5   | LDT_TIMER_VALUE_6 | Live Bit    |
| 4   | LDT_TIMER_VALUE_5 | Live Bit    |
| 3   | CRC 3             |             |
| 2   | CRC 2             |             |

| Bit | Name  | Description |
|-----|-------|-------------|
| 1   | CRC 1 |             |
| 0   | CRC 0 |             |

**Table 336. DSR20 (0x34) MSB**

| Bit 23   | Bit 22                          | Bit 21                          | Bit 20                          | Bit 19                          | Bit 18                          | Bit 17                    | Bit 16                     |
|----------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------|----------------------------|
| - (R0)   | - (R0)                          | - (R0)                          | 0 (R)                           | 0 (R)                           | 0 (R)                           | 0 (RC1L)                  | 0 (R)                      |
| RES      | LDT_TIMER_VALUE_4               | LDT_TIMER_VALUE_3               | LDT_TIMER_VALUE_2               | LDT_TIMER_VALUE_1               | LDT_TIMER_VALUE_0               | LDT_WAKE                  | LDT_RUNNING                |
| reserved | Long Duration Timer value Bit 4 | Long Duration Timer value Bit 3 | Long Duration Timer value Bit 2 | Long Duration Timer value Bit 1 | Long Duration Timer value Bit 0 | Long Duration Wake up Bit | Long Duration Trunning Bit |

**Table 337. DSR20 (0x34) MSB description**

| Bit | Name              | Description                          |
|-----|-------------------|--------------------------------------|
| 23  | RES               | reserved                             |
| 22  | LDT_TIMER_VALUE_4 | Live bit                             |
| 21  | LDT_TIMER_VALUE_3 | Live bit                             |
| 20  | LDT_TIMER_VALUE_2 | Live bit                             |
| 19  | LDT_TIMER_VALUE_1 | Live bit                             |
| 18  | LDT_TIMER_VALUE_0 | Live bit                             |
| 17  | LDT_WAKE          | Long Duration wake up bit            |
| 16  | LDT_RUNNING       | Long Duration status bit<br>Live bit |

**Table 338. DSR20 (0x34)**

| Bit 15   | Bit 14   | Bit 13   | Bit 12   | Bit 11   | Bit 10   | Bit 9    | Bit 8    |
|----------|----------|----------|----------|----------|----------|----------|----------|
| - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   | - (R0)   |
| RES      | RES      | RES      | RES      | RES      | RES      | RES      | RES      |
| reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |

**Table 339. DSR20 (0x34) description**

| Bit | Name | Description |
|-----|------|-------------|
| 15  | RES  | reserved    |
| 14  | RES  | reserved    |
| 13  | RES  | reserved    |
| 12  | RES  | reserved    |
| 11  | RES  | reserved    |
| 10  | RES  | reserved    |
| 9   | RES  | reserved    |
| 8   | RES  | reserved    |

**Table 340. DSR20 (0x34) LSB**

| Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3                            | Bit 2                            | Bit 1                            | Bit 0                            |
|----------|----------|----------|----------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| -(R0)    | -(R0)    | -(R0)    | -(R0)    | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         | 0 (RC1L)                         |
| RES      | RES      | RES      | RES      | CRC3                             | CRC2                             | CRC1                             | CRC0                             |
| reserved | reserved | reserved | reserved | Cyclic Redundancy Checking Bit 3 | Cyclic Redundancy Checking Bit 2 | Cyclic Redundancy Checking Bit 1 | Cyclic Redundancy Checking Bit 0 |

**Table 341. DSR20 (0x34) LSB description**

| Bit | Name  | Description |
|-----|-------|-------------|
| 7   | RES   | reserved    |
| 6   | RES   | reserved    |
| 5   | RES   | reserved    |
| 4   | RES   | reserved    |
| 3   | CRC 3 |             |
| 2   | CRC 2 |             |
| 1   | CRC 1 |             |
| 0   | CRC 0 |             |

## 9.8 Status register that must be cleared to enter ACTIVE - FP mode

**Table 342. Status register list to be cleared for ACTIVE - FP mode**

| Register            |
|---------------------|
| abist_boost_ignored |
| abist_complete      |
| boost_in_lp         |
| boost_vdsmon_error  |
| buck1_int_fail      |
| buck1_oc            |
| buck1_ov            |
| buck1_pg_ok         |
| buck1_pg_timeout    |
| buck1_uv            |
| buck2_int_fail      |
| buck2_oc            |
| buck2_ov            |
| buck2_pg_ok         |
| buck2_pg_timeout    |
| buck2_uv            |
| buck3_int_fail      |
| buck3_oc            |
| buck3_ov            |
| buck3_pg_ok         |
| buck3_pg_timeout    |

| Register               |
|------------------------|
| buck3_uv               |
| bypass_vdsmon_error    |
| current_mismatch       |
| fbb_ov                 |
| fbb_uv                 |
| fccu_ena_echo_error    |
| fccufail               |
| forced_sleep_powup     |
| fp_ready               |
| fsm_comp_error         |
| fsm_to_rec2            |
| gndloss                |
| ign_wake               |
| int_reg_ov             |
| int_reg_uv             |
| irq_echo_error         |
| irq_sent               |
| lbist_complete         |
| lbist_stopped          |
| ldo1_pg_ok             |
| ldo1_pg_timeout        |
| ldo1_uv                |
| ldo2_ov                |
| ldo2_pg_ok             |
| ldo2_pg_timeout        |
| ldo2_uv                |
| lp_ready               |
| nvm_comp_error         |
| nvm_crc_error          |
| osc_error              |
| ouths_oc               |
| ouths_ol               |
| nrst_echo_error        |
| spi_all_wakeup_disable |
| spi_clk_cnt            |
| spi_crc_error          |
| spi_csn_timeout        |
| spi_reg_comp_error     |
| spi_sdi_stuck_high     |
| spi_sdi_stuck_low      |
| spi_lbisted            |



| Register             |
|----------------------|
| spi_status_wrt       |
| spi_undef_add        |
| timer_wake           |
| tsd_cl0              |
| tsd_cl1              |
| tsd_cl2              |
| tsd_cl3              |
| tsd_cl4              |
| vio_uv               |
| vpor                 |
| wdfail               |
| wu_wake              |
| forced_sleep_regfail |

## 10 PCB layout recommendation

In designing devices with high-frequency switching converters, PCB layout is crucial because it affects noise pickup and can cause even a well-designed system to perform below expectations.

As a general rule, the connections for the power components should be on the top layer with wide, copper-filled areas or shapes. Moreover, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

Output capacitors, inductors and the SPSB100GS itself should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them and avoid inserting any other additional components necessary to put in place a suitable filtering action.

Place the input capacitors directly at the VIN12 and VIN3 pins of the SPSB100GS. The feedback paths should be kept away from the inductors and other noise sources.

The critical bypass components such as capacitors for VINx and VREG should be close to their respective pins. It is important to place the feedback components including feedback resistors close to the FBx pins.

In a multilayer PCB, use at least one layer as a power ground plane, as it is not always necessary to have a dedicated signal ground plane. In any case, it is good practice to reference sensitive analog signals to a low-noise ground point to avoid interference from high-current loops. The QFN is a thermally enhanced package. To effectively remove heat from the device, the exposed pad should be connected to the ground plane using via holes. Figures below illustrate the implementation of the layout guidelines outlined above, on the 6-layer demo board.

As shown in the PCB layout:

- Allow enough copper for VIN, GND and PHx
- All bypass capacitors are placed as close as possible to their connecting pins
- SGND as well as CANGND are connected to the inner PGND plane through via holes
- PHx nodes copper should only be routed on the top layer to minimize switching noises
- FBx trace routing is kept away from the SW node
- Thermal via holes are placed on the exposed pad to improve thermal dissipation

Figure 73. SPSB100GS 6-Layer Demo Board – Top Layer

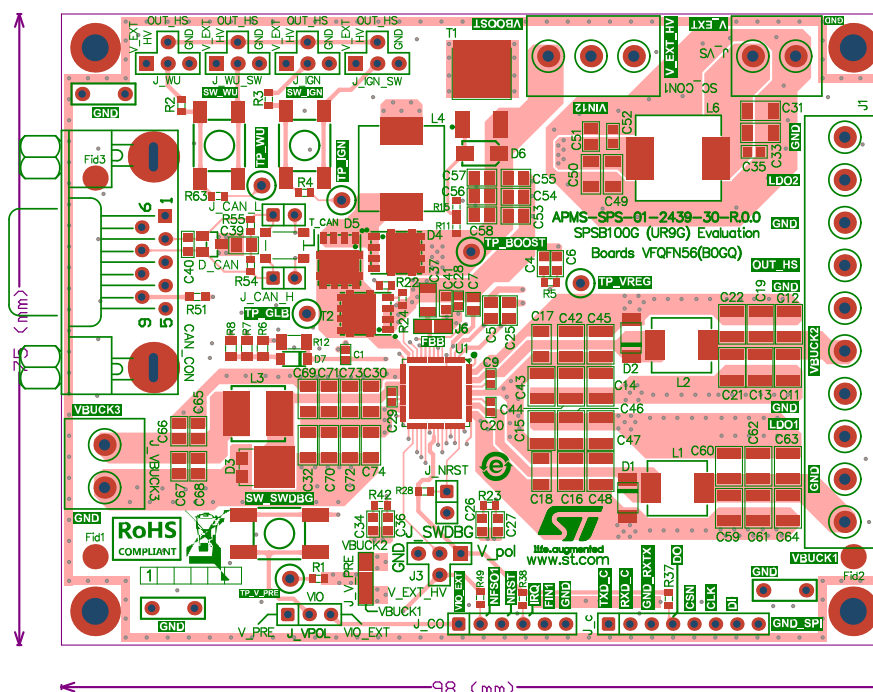


Figure 74. SPSB100GS 6-Layer Demo Board – Layer 2

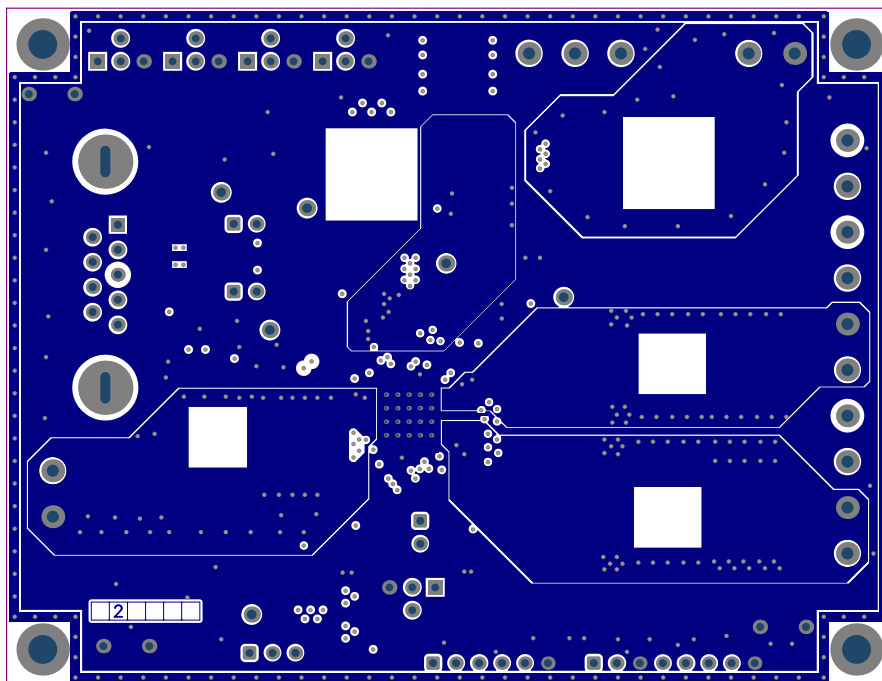


Figure 75. SPSB100GS 6-Layer Demo Board – Layer 3

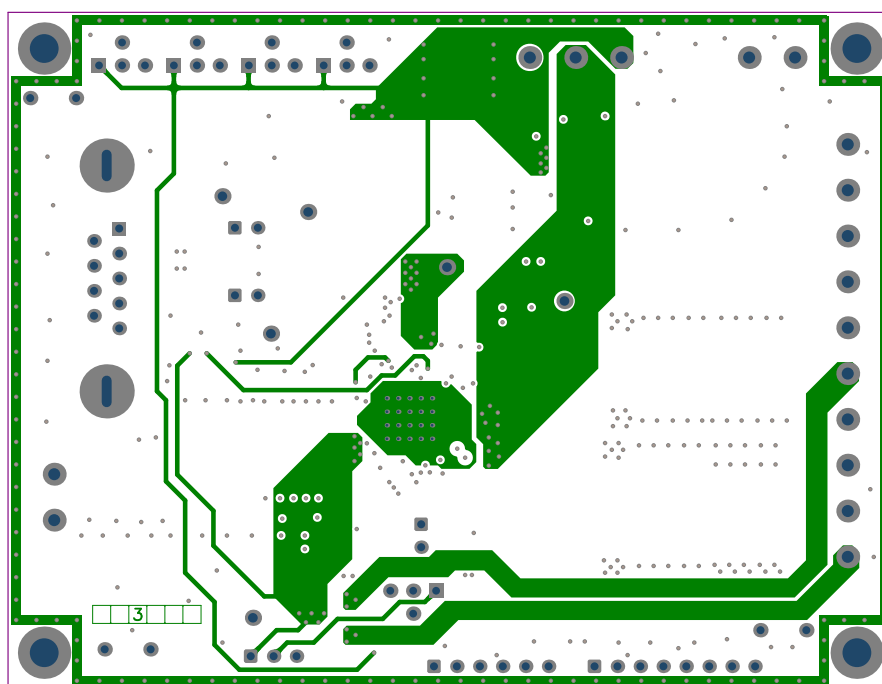


Figure 76. SPSB100GS 6-Layer Demo Board – Layer 4

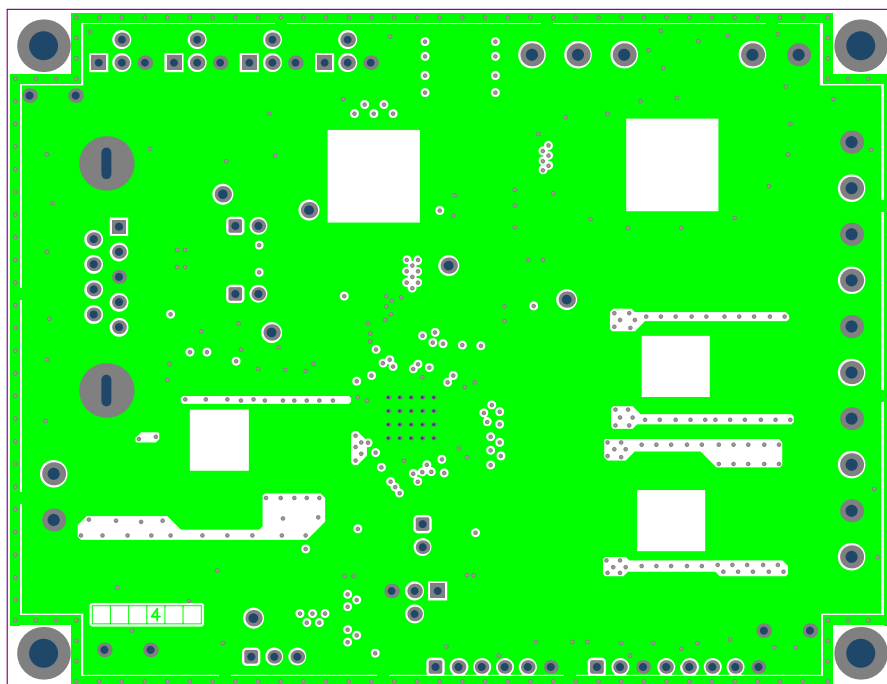


Figure 77. SPSB100GS 6-Layer Demo Board – Layer 5

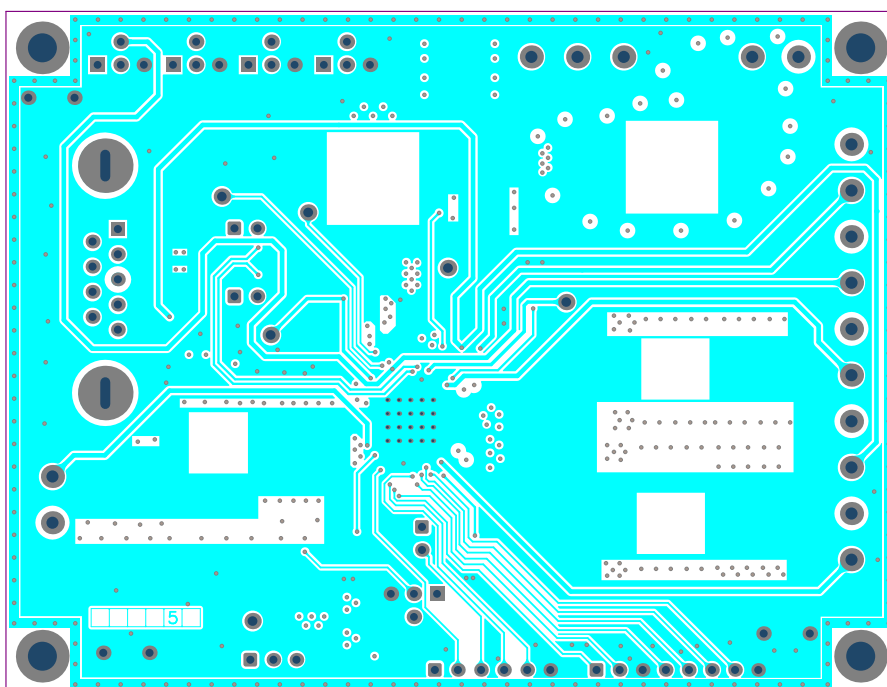
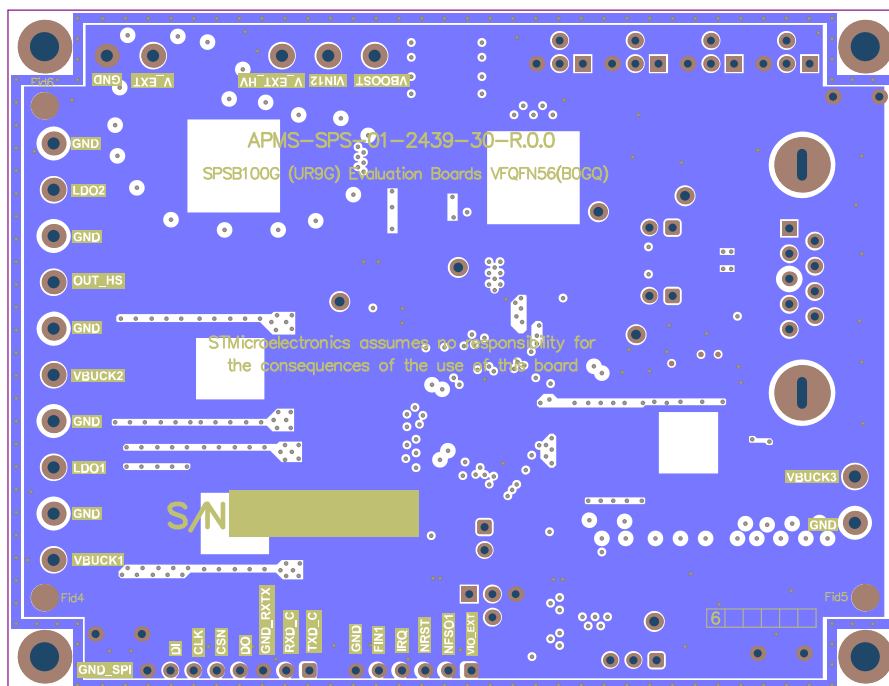


Figure 78. SPSB100GS 6-Layer Demo Board – Bottom Layer



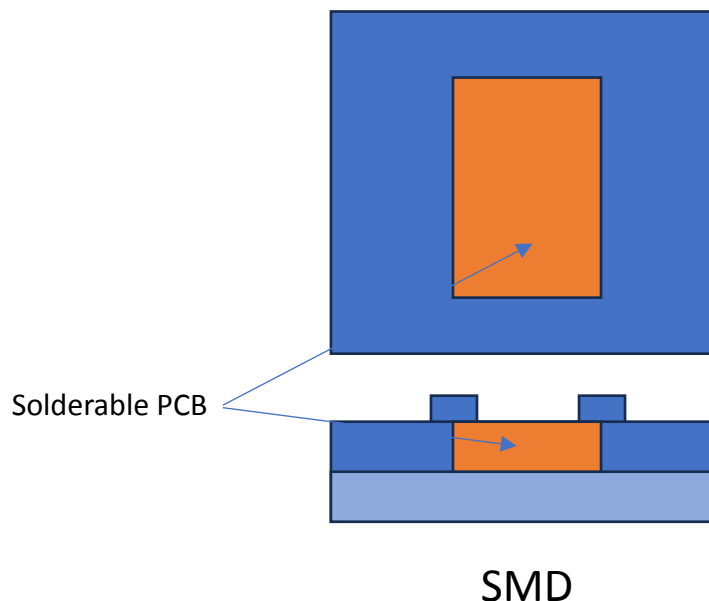
## 10.1 PCB metal and component placement

Evaluation has shown that the best overall performance is achieved using the recommended substrate/PCB layout. QFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

## 10.2 Solder mask

We recommend that larger power or land area pads are Solder Mask Defined (SMD). This allows the underlying copper traces to be as large as possible, which helps in terms of current-carrying capability and device-cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the openings in the solder mask. This allows for layers to be misaligned by up to 0.1 mm on both axes. Ensure that the solder resist in-between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.

Figure 79. Solder mask defined (SMD)



### 10.3

#### Stencil design

Stencils for QFN packages can be used with a thicknesses of 0.100 - 0.250 mm (0.004-0.010"). Stencils thinner than 0.100 mm are unsuitable, as they deposit insufficient solder paste to make good solder joints with the ground pad. High reductions sometimes create similar problems. Stencils in the range of 0.125 mm - 0.200 mm (0.005 - 0.008"), with suitable reductions, yield the best results.

## 11 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 11.1 QFN56L + 4 (8 x 8 mm) with wettable flank (half cut leads) package information

Figure 80. QFN56L (8 x 8 mm) package outline

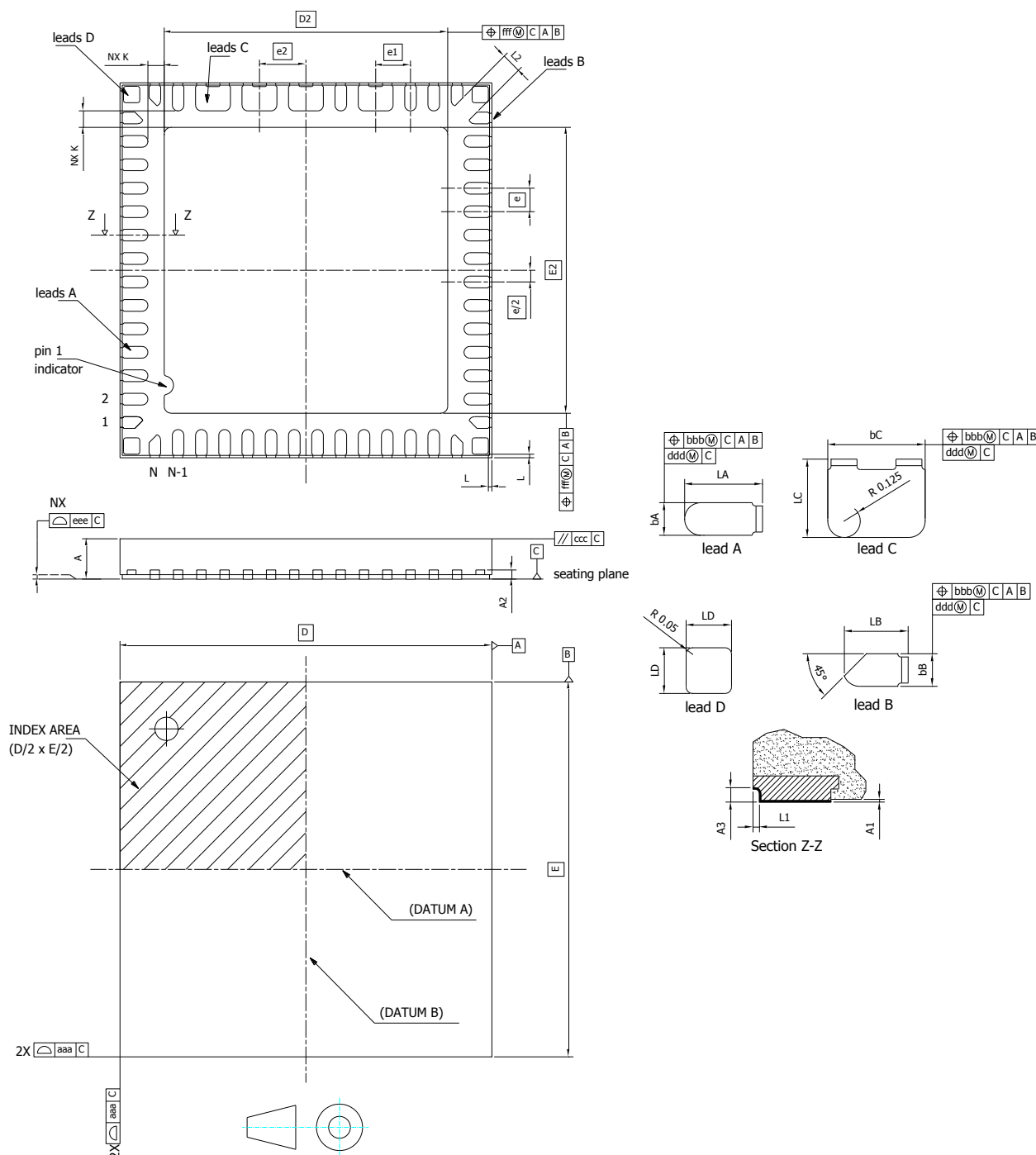


**Table 343. QFN56L (8 x 8 mm) mechanical data**

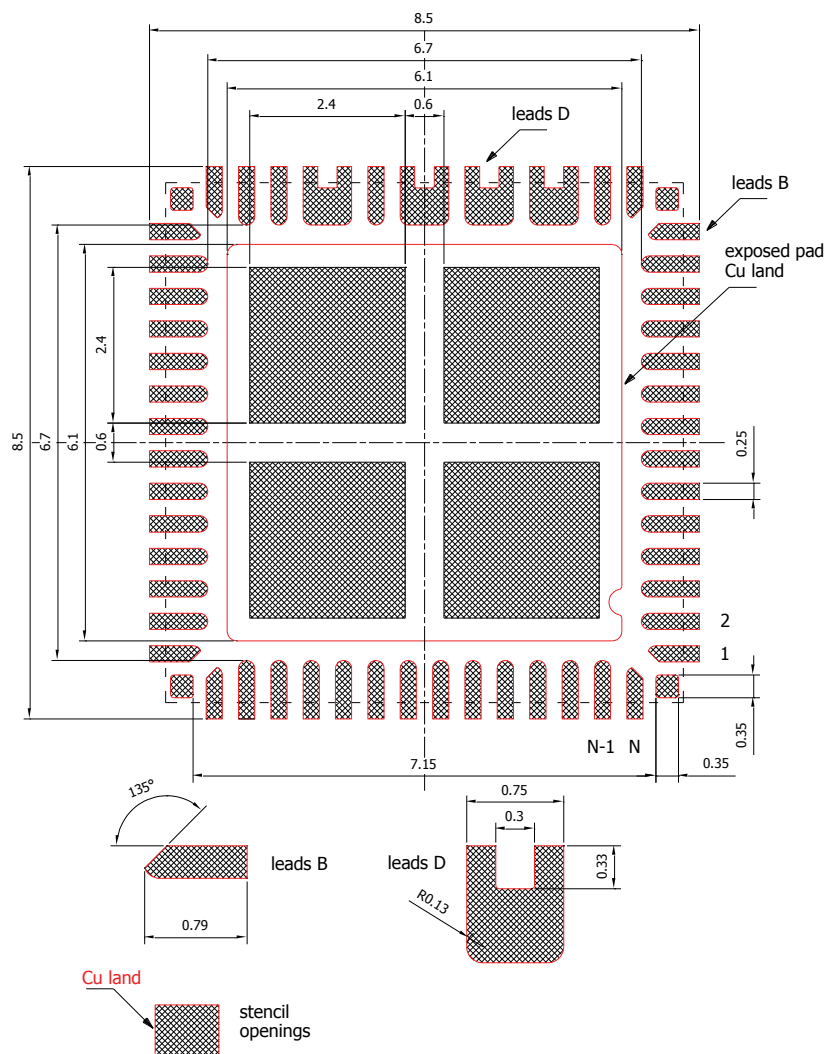
| Dim.                           | mm        |       |      |
|--------------------------------|-----------|-------|------|
|                                | Min.      | Typ.  | Max. |
| A                              | 0.80      | 0.90  | 1.00 |
| A1                             | 0.00      | -     | 0.05 |
| A2                             | 0.2 REF   |       |      |
| A3                             | 0.10      |       |      |
| D                              | 8.00 BSC  |       |      |
| E                              | 8.00 BSC  |       |      |
| D1                             | VARIATION |       |      |
| E1                             | VARIATION |       |      |
| e                              | 0.50 BSC  |       |      |
| e1                             | 0.75 BSC  |       |      |
| e2                             | 1.00 BSC  |       |      |
| L1                             | 0.05 REF  |       |      |
| L2                             | 0.38      | 0.43  | 0.48 |
| LA                             | 0.55      | 0.60  | 0.65 |
| bA                             | 0.20      | 0.25  | 0.30 |
| LB                             | 0.44      | 0.49  | 0.54 |
| L1B                            | 0.27      | 0.32  | 0.37 |
| L2B                            | 0.33      | 0.38  | 0.43 |
| bB                             | 0.20      | 0.25  | 0.30 |
| LC                             | 0.55      | 0.60  | 0.65 |
| bC                             | 0.70      | 0.75  | 0.80 |
| LD                             | 0.30      | 0.36  | 0.40 |
| bD                             | 0.30      | 0.36  | 0.40 |
| Φ                              |           | 45°   |      |
| R1                             |           | 0.125 |      |
| k                              | 0.20      |       |      |
| N                              | 56+4      |       |      |
| TOLERANCE OF FORM AND POSITION |           |       |      |
| aaa                            | 0.15      |       |      |
| bbb                            | 0.10      |       |      |
| ccc                            | 0.10      |       |      |
| ddd                            | 0.05      |       |      |
| eee                            | 0.08      |       |      |
| fff                            | 0.10      |       |      |
| NOTE                           | 1,12      |       |      |
| REF                            |           |       |      |

EXPOSED PAD VARIATION

|  |    |    |  |
|--|----|----|--|
|  | D1 | E1 |  |
|--|----|----|--|

| EXPOSED PAD VARIATION |      |      |      |      |      |      |        |
|-----------------------|------|------|------|------|------|------|--------|
| VARIATION             |      |      |      |      |      |      |        |
| A                     | 6.00 | 6.10 | 6.20 | 6.00 | 6.10 | 6.20 | 10, 12 |
| B                     |      |      |      |      |      |      |        |
| C                     |      |      |      |      |      |      |        |

**Figure 81. QFN56L (8 x 8 mm) recommended footprint - dimensions are in mm**





## 12 Ordering information

**Table 344. Order code**

| Order code   | Phy    | Package              | Packing       | NVM configuration             |
|--------------|--------|----------------------|---------------|-------------------------------|
| SPSB100GSTR  | CAN-FD | QFN 8 x 8 56L + 4 WF | Tape and reel | System supply configuration 1 |
| SPSB100GBSTR | N/A    |                      |               |                               |

Prerelease product(s)



## Revision history

**Table 345. Document revision history**

| Date        | Version | Changes          |
|-------------|---------|------------------|
| 17-Jul-2026 | 1       | Initial release. |

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