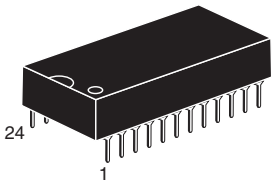
M48Z02, M48Z12

5 V, 16 kbit (2 Kb x 8) ZEROPOWER® SRAM

Datasheet - production data



PDIP 24.7

Battery CAPHAT™

Features

- Integrated, ultra low power SRAM and power-fail control circuit
- Unlimited WRITE cycles
- READ cycle time equals WRITE cycle time
- Automatic power-fail chip deselect and WRITE protection
- WRITE protect voltages
  - (V_{PFD} = power-fail deselect voltage):
  - M48Z02: V_{CC} = 4.75 to 5.5 V;
    4.5 V ≤ V_{PFD} ≤ 4.75 V
  - M48Z12: V_{CC} = 4.5 to 5.5 V;
    4.2 V ≤ V_{PFD} ≤ 4.5 V
- Self-contained battery in the CAPHAT™ DIP package
- Pin and function compatible with JEDEC standard 2 K x 8 SRAMs
- RoHS compliant
  - Lead-free second level interconnect

Description

The M48Z02/12 ZEROPOWER® RAM is a 2 K x 8 non-volatile static RAM which is pin and function compatible with the DS1220.

A special 24-pin, 600 mil DIP CAPHAT™ package houses the M48Z02/12 silicon with a long-life lithium button cell to form a highly integrated battery-backed memory solution.

The M48Z02/12 button cell has sufficient capacity and storage life to maintain data functionality for an accumulated time period of at least 10 years in the absence of power over commercial operating temperature range.

The M48Z02/12 is a non-volatile pin and function equivalent to any JEDEC standard 2 K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

This is information on a product in full production. www.st.com

Contents

1 Diagram 3

2 Pin setting 4

3 Operation modes 5

3.1 READ mode 5

3.2 WRITE mode 6

3.3 Data retention mode 8

3.4 V_{CC} noise and negative going transients 10

4 Maximum ratings 11

5 DC and AC parameters 12

6 Package mechanical data 15

7 Part numbering 17

8 Environmental information 18

9 Revision history 19

1 Diagram

Figure 1. Logic diagram

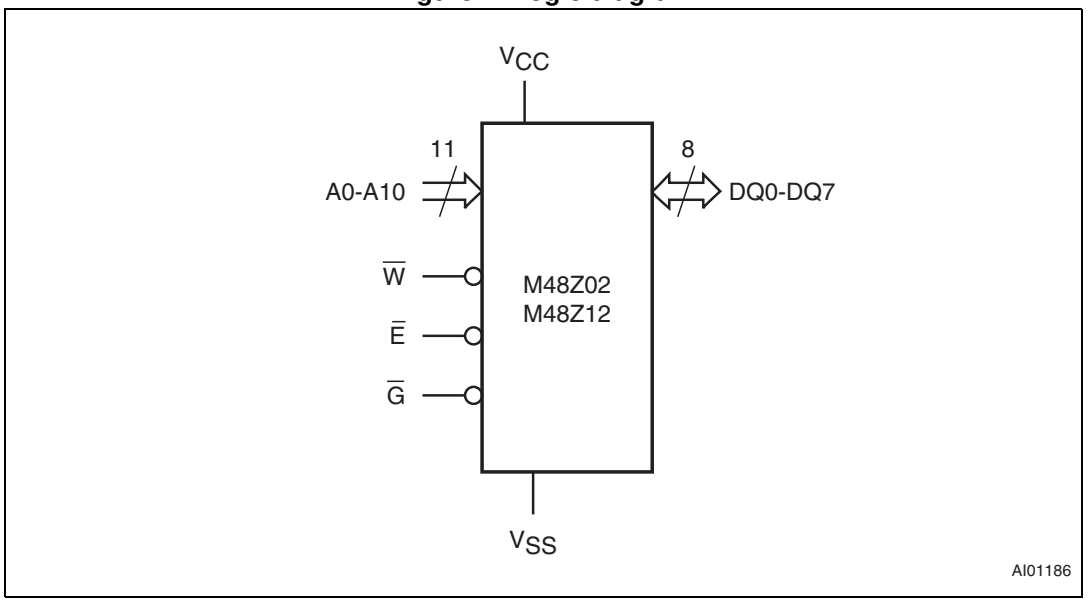


Table 1. Signal names

A0-A10	Address inputs
DQ0-DQ7	Data inputs / outputs
$\overline{E}$	Chip enable
$\overline{G}$	Output enable
$\overline{W}$	WRITE enable
V_{CC}	Supply voltage
V_{SS}	Ground

2 Pin setting

Figure 2. DIP connections

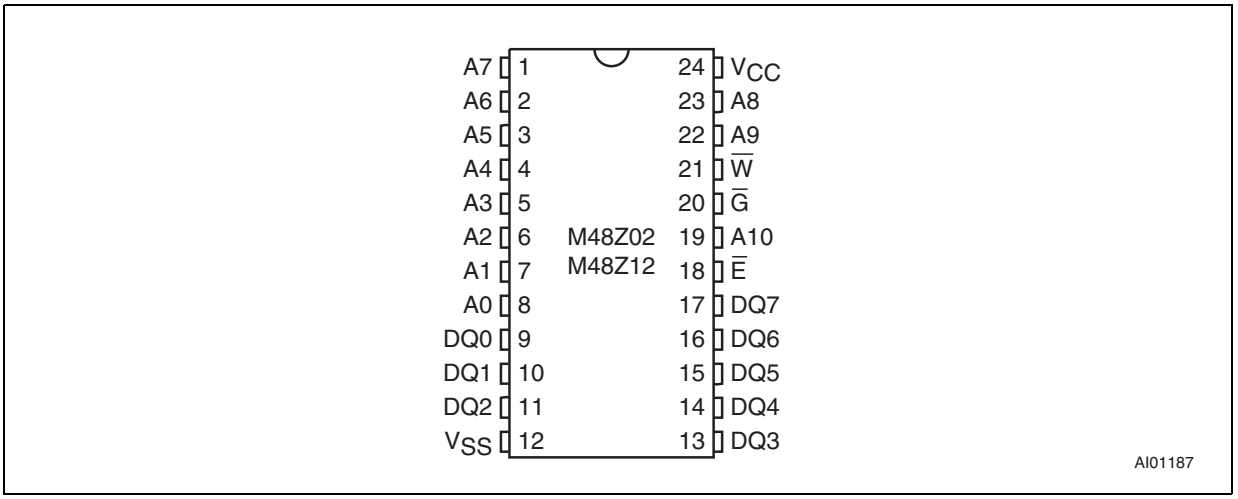
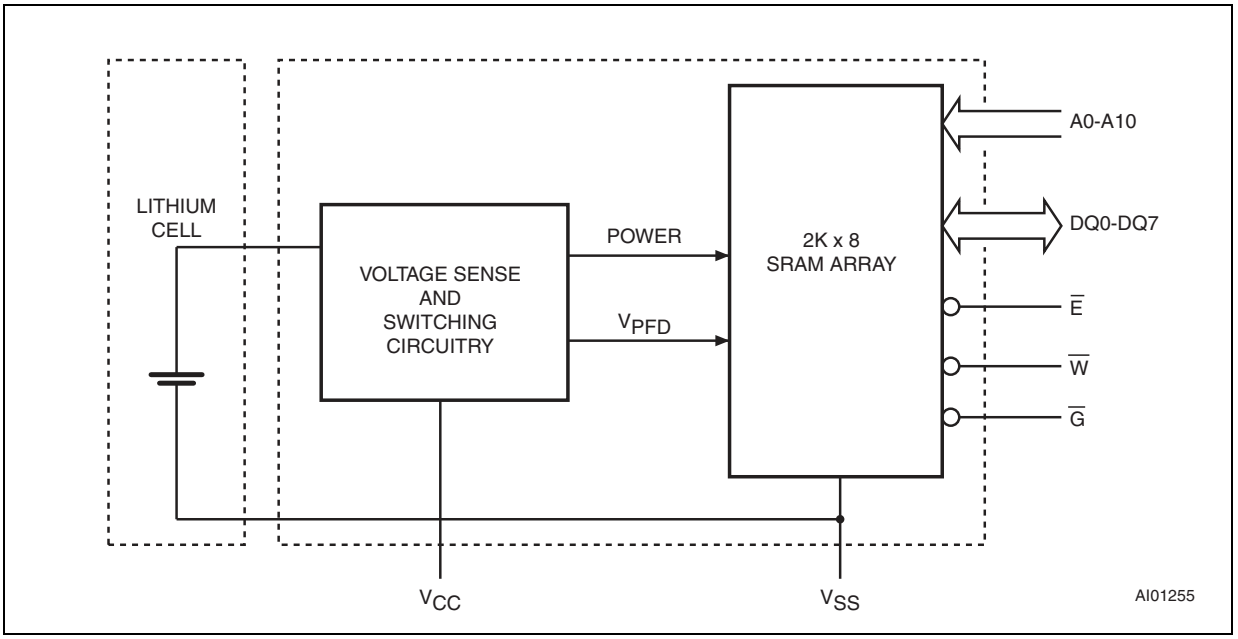


Figure 3. Block diagram



3 Operation modes

The M48Z02/12 also has its own power-fail detect circuit. The control circuitry constantly monitors the single 5 V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3 V, the control circuitry connects the battery which maintains data operation until valid power returns.

Table 2. Operating modes

Mode	V_{CC}	E	G	W	DQ0-DQ7	Power
Deselect	4.75 to 5.5 V or 4.5 to 5.5 V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD}(min)(1)	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	High Z	Battery backup mode

1. See *Table 10* for details.

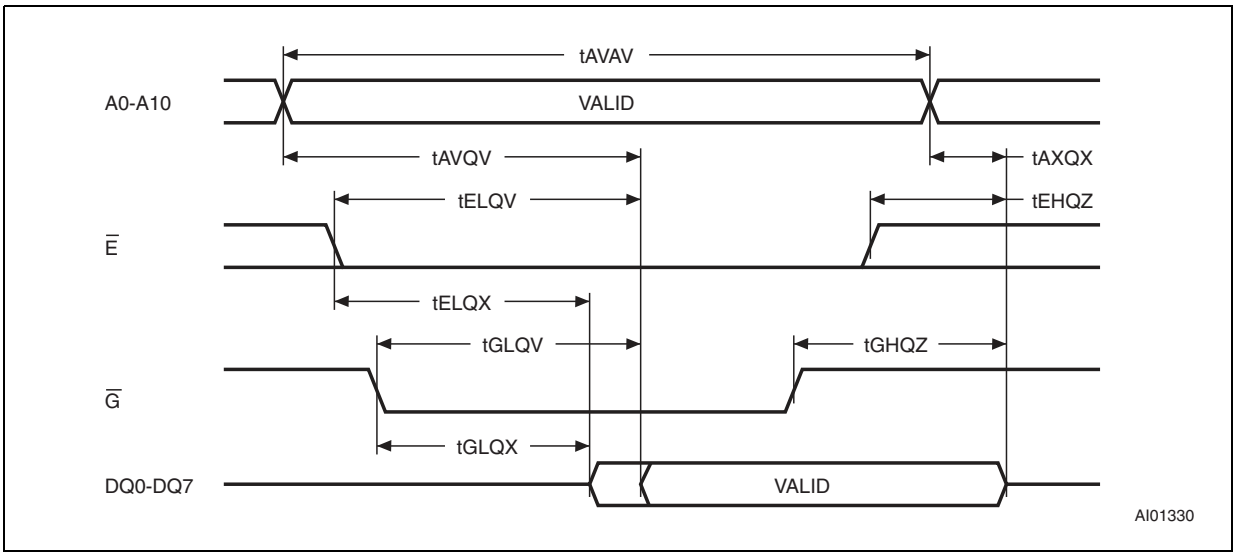
Note: X = V_{IH} or V_{IL}; V_{SO} = battery backup switchover voltage.

3.1 READ mode

The M48Z02/12 is in the READ mode whenever $\overline{W}$ (WRITE enable) is high and $\overline{E}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs defines which one of the 2,048 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the chip enable access time (t_{ELQV}) or output enable access time (t_{GLQV}).

The state of the eight three-state data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the address inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for output data hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 4. READ mode AC waveforms



Note: WRITE enable ($\overline{W}$) = high.

Table 3. READ mode AC characteristics

Symbol	Parameter[1]	M48Z02/M48Z12						Unit
		–70		–150		–200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	READ cycle time	70		150		200		ns
t_{AVQV}	Address valid to output valid		70		150		200	ns
t_{ELQV}	Chip enable low to output valid		70		150		200	ns
t_{GLQV}	Output enable low to output valid		35		75		80	ns
t_{ELQX}	Chip enable low to output transition	5		10		10		ns
t_{GLQX}	Output enable low to output transition	5		5		5		ns
t_{EHQZ}	Chip enable high to output Hi-Z		25		35		40	ns
t_{GHQZ}	Output enable high to output Hi-Z		25		35		40	ns
t_{AXQX}	Address transition to output transition	10		5		5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

3.2 WRITE mode

The M48Z02/12 is in the WRITE mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from chip enable or t_{WHAX} from WRITE enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 5. WRITE enable controlled, WRITE AC waveform

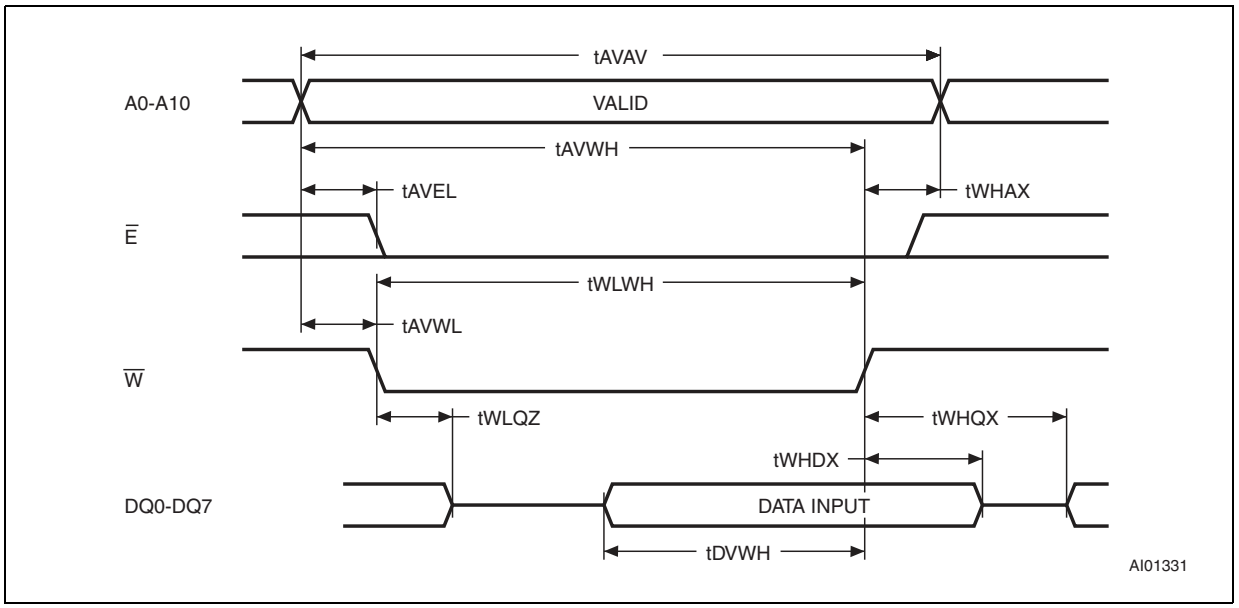


Figure 6. Chip enable controlled, WRITE AC waveforms

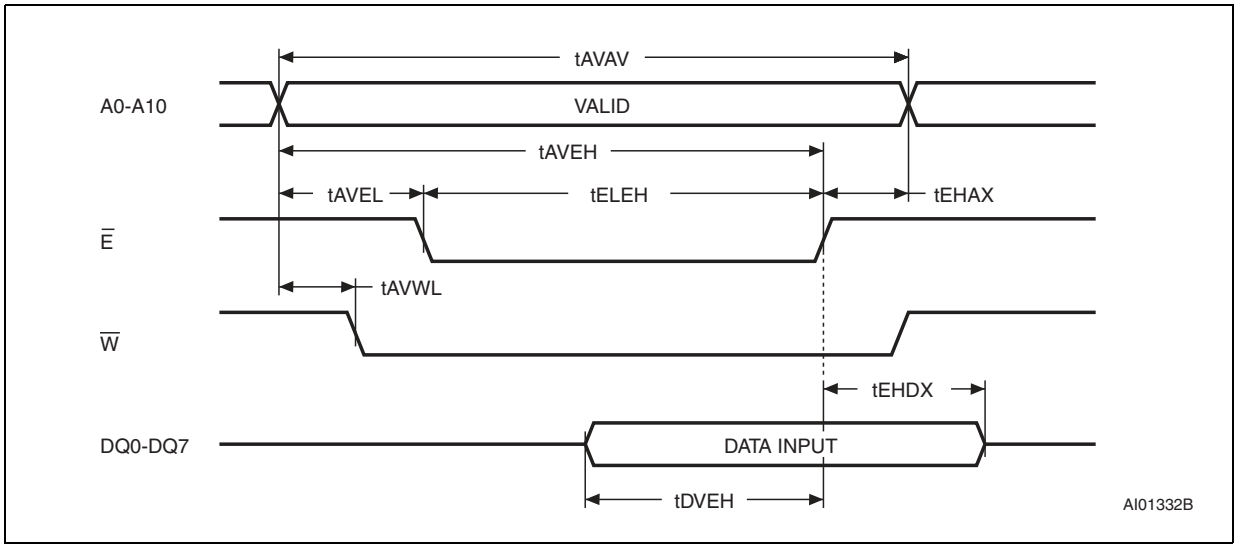


Table 4. WRITE mode AC characteristics

Symbol	Parameter[1]	M48Z02/M48Z12						Unit
		–70		–150		–200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	WRITE cycle time	70		150		200		ns
t_{AVWL}	Address valid to WRITE enable low	0		0		0		ns
t_{AVEL}	Address valid to chip enable 1 low	0		0		0		ns
t_{WLWH}	WRITE enable pulse width	50		90		120		ns
t_{ELEH}	Chip enable low to chip enable 1 high	55		90		120		ns
t_{WHAX}	WRITE enable high to address transition	0		10		10		ns
t_{EHAX}	Chip enable high to address transition	0		10		10		ns
t_{DVWH}	Input valid to WRITE enable high	30		40		60		ns
t_{DVEH}	Input valid to chip enable high	30		40		60		ns
t_{WHDX}	WRITE enable high to input transition	5		5		5		ns
t_{EHDX}	Chip enable high to input transition	5		5		5		ns
t_{WLQZ}	WRITE enable low to output Hi-Z		25		50		60	ns
t_{AVWH}	Address valid to WRITE enable high	60		120		140		ns
t_{AVEH}	Address valid to chip enable high	60		120		140		ns
t_{WHQX}	WRITE enable high to output transition	5		10		10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

3.3 Data retention mode

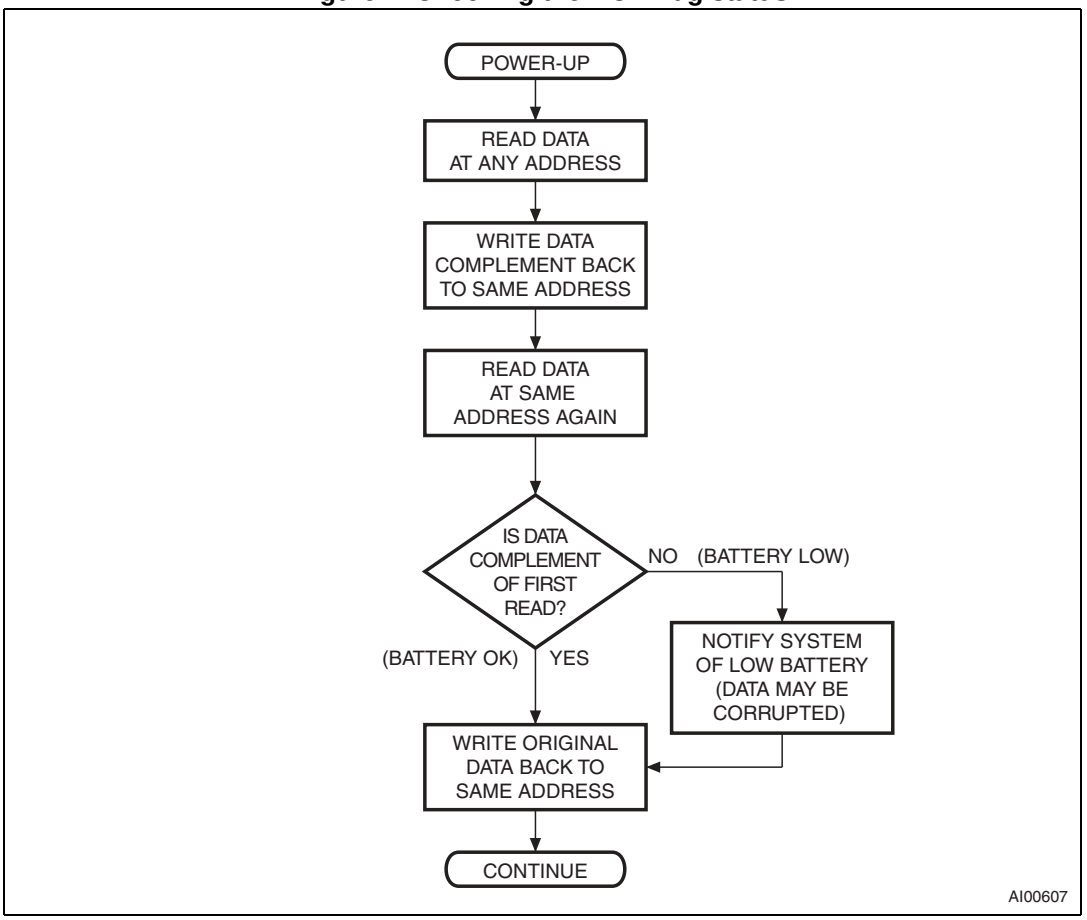
With valid V_{CC} applied, the M48Z02/12 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as “don't care.”

Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z02/12 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises, the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first WRITE attempted will be blocked. The flag is automatically cleared after the first WRITE, and normal RAM operation resumes. *Figure 7* illustrates how a $\overline{BOK}$ check routine could be structured.

For more information on a battery storage life refer to the application note AN1012.

Figure 7. Checking the $\overline{\text{BOK}}$ flag status

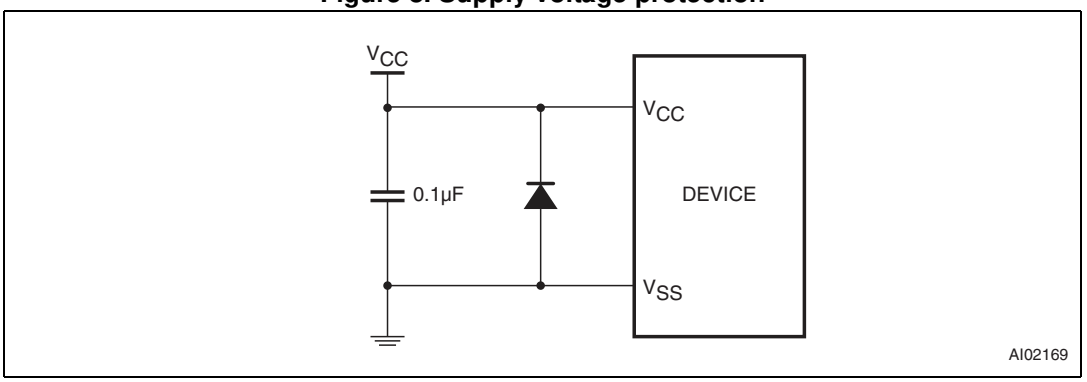


3.4 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 µF (as shown in *Figure 8*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a Schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 8. Supply voltage protection



4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_A	Ambient operating temperature	Grade 1	0 to 70	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)		–40 to 85	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages		–0.3 to 7	V
V_{CC}	Supply voltage		–0.3 to 7	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. Soldering temperature of the IC leads is to not exceed 260 °C for 10 seconds. Furthermore, the devices shall not be exposed to IR reflow nor preheat cycles (as performed as part of wave soldering). ST recommends the devices be hand-soldered or placed in sockets to avoid heat damage to the batteries.

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in *Table 6*. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 6. Operating and AC measurement conditions

Parameter		M48Z02	M48Z12	Unit
Supply voltage (V_{CC})		4.75 to 5.5	4.5 to 5.5	V
Ambient operating temperature (T_A)	Grade 1	0 to 70	0 to 70	°C
Load capacitance (C_L)		100	100	pF
Input rise and fall times		≤ 5	≤ 5	ns
Input pulse voltages		0 to 3	0 to 3	V
Input and output timing ref. voltages		1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 9. AC testing load circuit

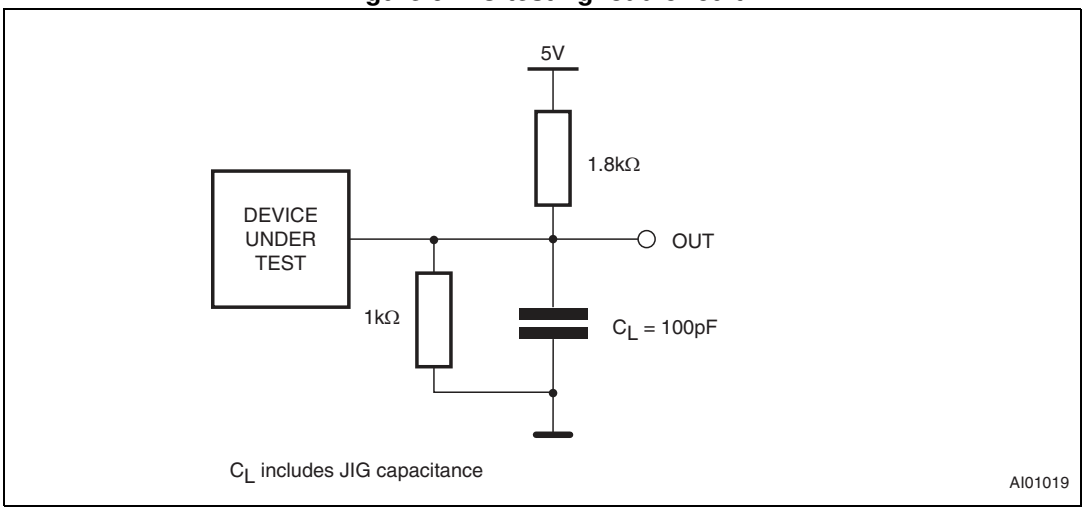


Table 7. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance	-	10	pF
C_{IO}[3]	Input / output capacitance	-	10	pF

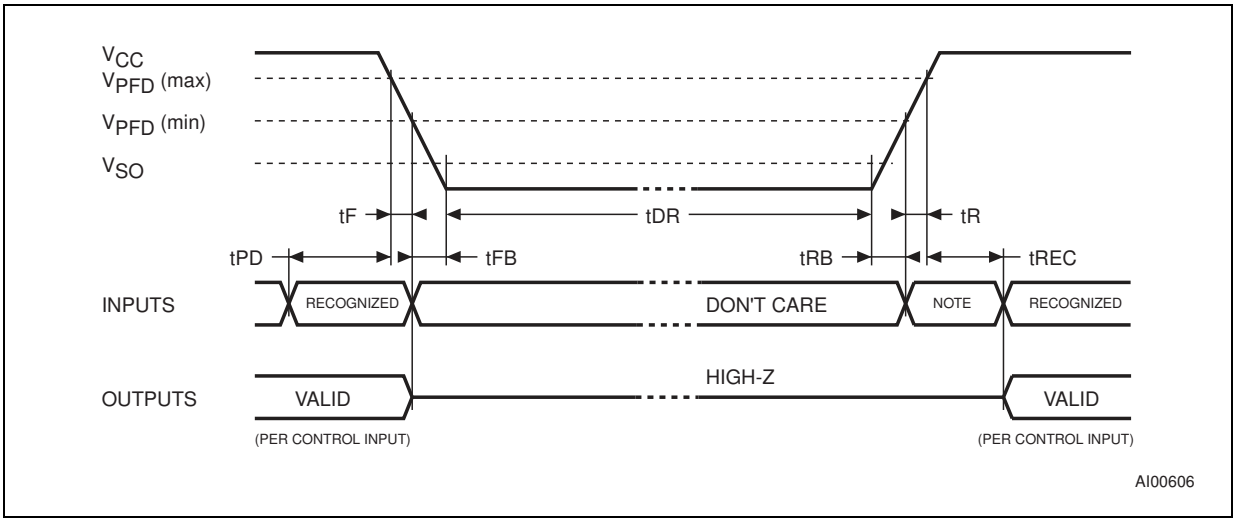
1. Effective capacitance measured with power supply at 5 V. Sampled only, not 100% tested.
2. At 25°C, f = 1 MHz.
3. Outputs deselected.

Table 8. DC characteristics

Symbol	Parameter	Test condition(1)	Min	Max	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}(2)	Output leakage current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply current	Outputs open		80	mA
I_{CC1}	Supply current (standby) TTL	$\overline{E} = V_{IH}$		3	mA
I_{CC2}	Supply current (standby) CMOS	$\overline{E} = V_{CC} - 0.2$ V		3	mA
V_{IL}	Input low voltage		–0.3	0.8	V
V_{IH}	Input high voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = –1 mA	2.4		V

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. Outputs deselected.

Figure 10. Power down/up mode AC waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertent WRITE cycles after V_{CC} rises above V_{PFD} (min) but before normal system operations begin. Even though a power on reset is being applied to the processor, a reset condition may not occur until after the system is running.

Table 9. Power down/up AC characteristics

Symbol	Parameter[1]	Min.	Max.	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before power down	0	-	µs
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time	300	-	µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} fall time	10	-	µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time	0	-	µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time	1	-	µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after power up	2	-	ms

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 10. Power down/up trip points DC characteristics

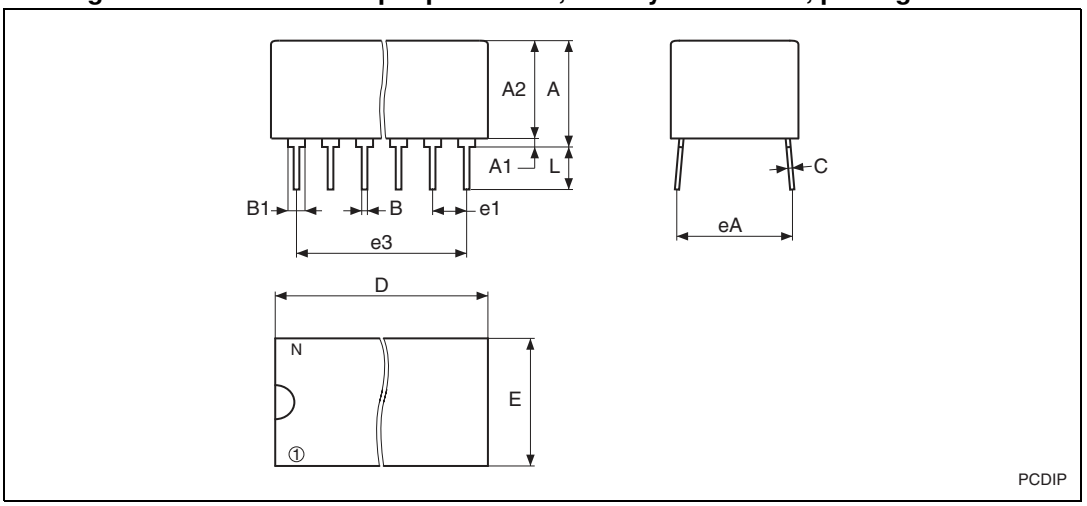
Symbol	Parameter[1][2]		Min.	Typ.	Max.	Unit
V_{PFD}	Power-fail deselect voltage	M48Z02	4.5	4.6	4.75	V
		M48Z12	4.2	4.3	4.5	V
V_{SO}	Battery backup switchover voltage			3.0		V
t_{DR}[3]	Expected data retention time		10			YEARS

1. All voltages referenced to V_{SS}.
2. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
3. At 25 °C, V_{CC} = 0 V.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 11. PDIP24.7 – 24-pin plastic DIP, battery CAPHAT™, package outline

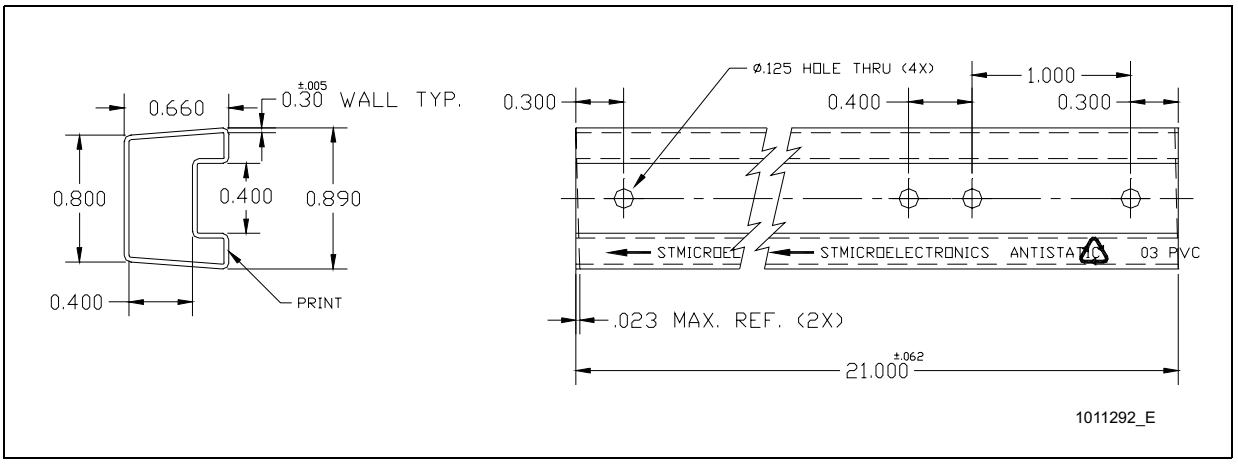


Note: Drawing is not to scale.

Table 11. PDIP 24.7 – 24-pin plastic DIP, battery CAPHAT™, package mechanical data

Symb	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		34.29	34.80		1.350	1.370
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3	27.94			1.1		
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	24			24		

Figure 12. Shipping tube dimensions for PDIP 24.7 package



Note: All dimensions are in inches.

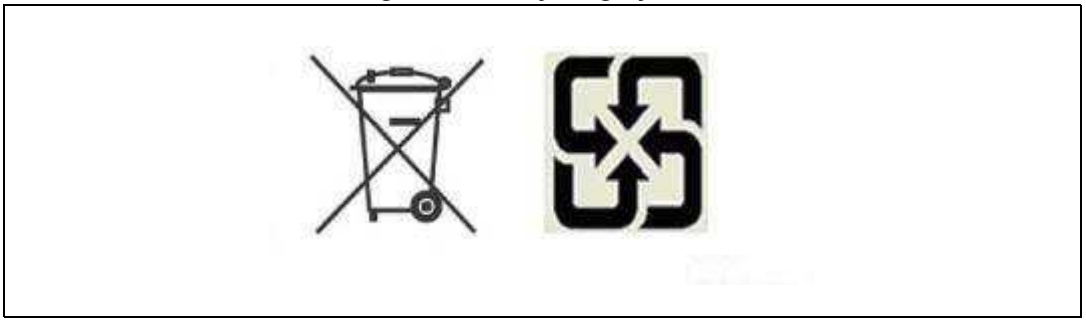
7 Part numbering

Table 12. Ordering information

Order code	Package	Temperature range	Speed	Supply voltage
M48Z02-150PC1	PDIP 24.7	0 to 70 °C	-150	V_{CC} = 4.75 to 5.5 V; V_{PFD} = 4.5 to 4.75 V
M48Z02-70PC1			-70	
M48Z12-150PC1			-150	V_{CC} = 4.5 to 5.5 V; V_{PFD} = 4.2 to 4.5 V
M48Z12-70PC1			-70	

8 Environmental information

Figure 13. Recycling symbols



This product contains a non-rechargeable lithium (lithium carbon monofluoride chemistry) button cell battery fully encapsulated in the final product.

Recycle or dispose of batteries in accordance with the battery manufacturer's instructions and local/national disposal and recycling regulations.

9 Revision history

Table 13. Document revision history

Date	Revision	Changes
May-1999	1	First issue
09-Jul-2001	2	Reformatted; temperature information added to tables (Table 5, 6, 7, 8, 3, 4, 9, 10); Figure updated (Figure 10)
17-Dec-2001	2.1	Remove references to “clock” in document.
20-May-2002	2.2	Updated V_{CC} noise and negative going transients text
01-Apr-2003	3	v2.2 template applied; test condition updated (Table 10)
22-Apr-2003	3.1	Fix error in ordering information (Table 12)
12-Dec-2005	4	Update template, Lead-free text, and remove references to ‘crystal’ and footnote (Table 8, 12)
02-Nov-2007	5	Reformatted document; added lead-free second level interconnect information to cover page and Section 5: Package mechanical data; updated Table 5, 6, 8, 9, 10, 12.
03-Dec-2008	6	Added Section 7: Environmental information; minor formatting changes
27-May-2010	7	Updated Section 3, Table 11, text in Section 5; reformatted document.
21-Jan-2011	8	Updated Table 12: Ordering information scheme for 200 ns version of devices; updated Section 7; added Figure 12; minor textual updates
07-Jun-2011	9	Updated footnote of Table 5: Absolute maximum ratings.
14-Sep-2020	10	Added *Table 12: Ordering information*. Updated package name.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to *www.st.com/trademarks*. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved