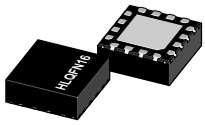
# NXLS9xxxxAES

Datasheet

## Dual channel inertial sensor



## Features

- Independent X-axis, Y-axis, or Z-axis ranges for each channel
  - Z-Axis, Low g ranges from ± 1.50 g to ± 20 g nominal full-scale range
  - Medium g ranges from ± 15.5 g to ± 150 g nominal full-scale range
  - High g ranges from ± 50 g to ± 500 g nominal full-scale range
- –40 °C to 125 °C operating temperature range
- DSI3 compatible
  - Discovery mode for physical location identification
  - High side bus switch output driver
  - Command and response mode support for device configuration
  - Periodic data collection mode support for sensor data transfers.
  - Background diagnostic mode support during periodic data collection mode
- PSI5 Version 2.1 compatible
  - Compatible modes:
    - P10P-500/3L
    - P10P-500/4H
    - A10P-228/1L
    - P10CRC-xxx/xx
    - P16CRC-xxx/xx
    - and many others
  - Programmable time slots with 1 µs resolution
  - Selectable baud rate: 125 kBd or 189 kBd
  - 10- and 16-bit data options
  - Selectable error detection: even parity, or 3-bit CRC
  - Optional daisy chain with external low side switch
  - Two-wire programming mode
- 32-bit SPI compatible serial interface
  - 3.3 V or 5 V single supply operation
  - Register read and write commands
  - Sensor data transmission commands
    - 12-bit data, left justified in a 16-bit data field
    - Command echo with 3-bit source identification
    - 2-bit basic status and 2-bit detailed status fields
    - 8-bit CRC
- I²C compatible serial interface (UM10204 [1] )
  - Slave mode operation
  - Standard mode, fast mode, and fast mode plus support
- Independent programmable arming functions for each channel

- DSP
  - Dual, independent signal chains from ADC to Communications Interface
  - Up to a fourth order low-pass filter with rolloff frequency options from 12.5 Hz to 1500 Hz
  - Optional single pole high pass filter with fast startup and output rate limiting
  - Optional moving average
  - Optional 16 to 1 output interpolation
- Pb-free 16-Pin QFN 4 mm x 4 mm x 1.45 mm package

## Applications

**Automotive**

- Airbag, collision/crash detection
- Active suspension vibration monitoring

**Industrial**

- Machine condition monitoring

## Description

The NXLS9xxxx is a dual channel DSI3, PSI5, SPI, and I²C compatible lateral (X-axis or Y-axis) or vertical (Z-axis) inertial sensor.

# 1 Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| NXLS9xxxxAESR2 | HLQFN16 | Plastic, thermal enhanced low profile quad flat non-leaded package; 16 terminals; 0.8 mm pitch; 4 mm x 4 mm x 1.45 mm body | Package outline - LQFN16 (step-cut wettable flank) |
| | | Plastic, thermal enhanced low profile quad flat non-leaded package, dimple deburr wettable flank; 16 terminals; 0.8 mm pitch; 4 mm x 4 mm x 1.45 mm body | Package outline - LQFN16 (dimple deburr wettable flank) |

## 1.1 Ordering options

**Table 2. Ordering options**

| Device | Channel 0 | | Channel 1 | | Protocol |
|---|---|---|---|---|---|
| | Axis | Range | Axis | Range | |
| NXLS95322 | X | M | Y | M | SPI/DSI3 |
| NXLS95422 | X | M | Z | M | SPI/DSI3 |
| NXLS95722 | Y | M | Z | M | SPI/DSI3 |
| NXLS95421 | X | M | Z | L | SPI/DSI3 |
| NXLS95333 | X | H | Y | H | SPI/DSI3 |
| NXLS95433 | X | H | Z | H | SPI/DSI3 |
| NXLS95733 | Y | H | Z | H | SPI/DSI3 |
| NXLS96322 | X | M | Y | M | PSI5 |
| NXLS96422 | X | M | Z | M | PSI5 |
| NXLS96722 | Y | M | Z | M | PSI5 |
| NXLS96421 | X | M | Z | L | PSI5 |
| NXLS96333 | X | H | Y | H | PSI5 |
| NXLS96433 | X | H | Z | H | PSI5 |
| NXLS96733 | Y | H | Z | H | PSI5 |

# 2 Marking

**Figure 1. Part marking**




Data Code Legend:

F: ASECL assembly site
WL: 2 alpha character representation of the wafer lot
YW: 2 alpha character representation of the year and work week
Z: Assembly Split




Data Code Legend:

N: ATBK assembly site
WL: 2 alpha character representation of the wafer lot
YW: 2 alpha character representation of the year and work week
Z: Assembly Split

*aaa-030573*

# 3 Application diagrams

## 3.1 DSI3 application diagrams

### 3.1.1 DSI3 discovery mode application diagram

**Figure 2. DSI3 discovery mode application diagram**

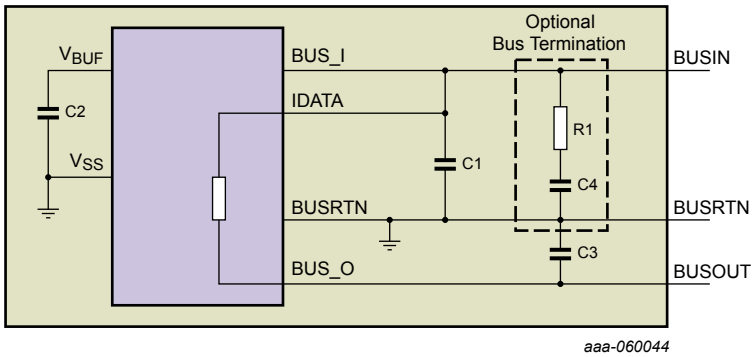



**Table 3. DSI3 discovery mode external component recommendations(1) (2)**

| Ref Des | Type | Typical value description | Component value selection and range | Comment |
|---|---|---|---|---|
| R1 | General purpose | 330 Ω, 5 %, 200 PPM | The system level communication, EMC, and ESD testing determine the optimal value of this component. | Optional bus termination for high inductance bus wire connections. For optimal EMC performance, this component along with C4 are to be placed as close to the BUS_I and BUSRTN connector pins as possible. |
| C1 | Ceramic | 220 pF, 10 %, 50 V minimum, X7R | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. | For optimal EMC performance, this component along with R1 are to be placed as close to the BUS_I and BUSRTN connector pins as possible. |
| C2 | Ceramic | 0.47 µF, 10 %, 10 V minimum, X7R | The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22 µF. The maximum specified value including all tolerances is 2 µF. | For optimal EMC performance, this component is to be placed as close to the VBUF and BUSRTN pins as possible. |
| C3 | Ceramic | 100 pF, 10 %, 50 V minimum, X7R | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. | For optimal EMC performance, this component is to be placed as close to the BUS_O and BUSRTN connector pins as possible. |
| C4 | Ceramic | 2.2 nF, 10 %, 50 V minimum, X7R | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. | Optional bus termination for high inductance bus wire connections. For optimal EMC performance, this component along with R1 are to be placed as close to the BUS_I and BUSRTN connector pins as possible. |

1. *The total bus capacitance must not exceed the values specified in the DSI3 standard.*
2. *The external components are dependent on the bus master and bus impedance and may vary from application to application.*

## 3.2 PSI5 application diagrams

### 3.2.1 PSI5 parallel or universal mode application diagram

**Figure 3. PSI5 parallel or universal mode application diagram**

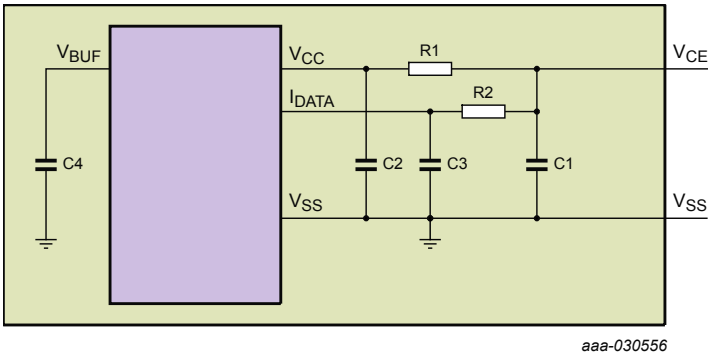



**Table 4. PSI5 parallel or universal mode external component recommendations(1)**

| Ref Des | Type | Description | Component value selection and range | Purpose |
|---|---|---|---|---|
| R1 | General purpose | 82 Ω, 5 %, 200 PPM | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing.<br>For proper device function, the minimum value can be 0 Ω. The maximum value is determined by the minimum bus voltage provided at the module pin and the minimum operating voltage of the device. To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 89.0 Ω.(2) | $V_{CC}$ filtering and signal damping |
| R2 | General purpose | 27 Ω, 5 %, 200 PPM | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing.<br>For proper device function, the minimum value can be 0 Ω. The maximum value is determined by the minimum bus voltage provided at the module pin. To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 66.6 Ω. If the low response current is used, the maximum resistance including all tolerances is 133 Ω. | $I_{DATA}$ filtering and signal damping |
| C1 | Ceramic | 2.2 nF, 10 %, 50 V minimum, X7R | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing | $V_{CC}$ power supply decoupling and signal damping. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN connector pins as possible. |
| C2 | Ceramic | 15 nF, 10 %, 50 V minimum, X7R | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing(3) | $V_{CC}$ power supply decoupling. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN pins as possible. |
| C3 | Ceramic | 470 pF, 10 %, 50 V minimum, X7R | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing | $I_{DATA}$ Filtering and Signal Damping |
| C4 | Ceramic | 0.47 µF, 10 %, 10 V minimum, X7R | The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22 µF. The maximum specified value including all tolerances is 2 µF. | For optimal EMC performance, this component is to be placed as close to the VBUF and BUSRTN pins as possible. |

1. *The total bus capacitance must not exceed the values specified in the PSI5 standard.*
2. *R1 must be sized to handle both the programming current at the maximum rated temperature for programming and the operating current at the maximum rated temperature for operation.*
3. *If the high baud rate is used, ST recommends reducing the value of C2. The actual value depends on the bus configuration and number of slaves.*

### 3.2.2 PSI5 daisy chain mode application diagram

**Figure 4. PSI5 daisy chain mode application diagram**

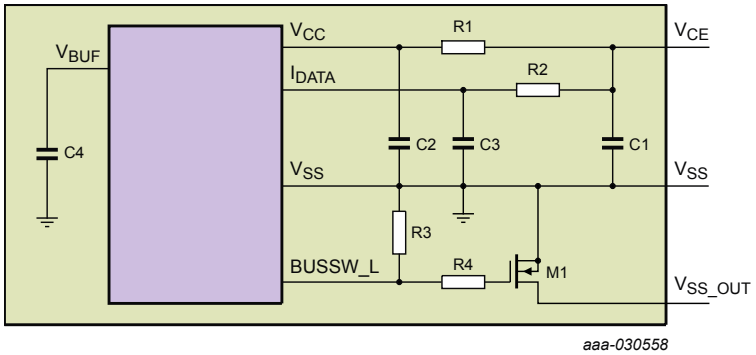



**Table 5. PSI5 daisy chain mode external component recommendations(1) (2) (3)**

| Ref Des | Type | Description | Component value selection and range | Purpose |
|---|---|---|---|---|
| R1 | General purpose | 82 Ω, 5 %, 200 PPM | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing.<br>For proper device function, the minimum value can be 0 Ohms. The maximum value is determined by the minimum bus voltage provided at the module pin and the minimum operating voltage of the device. To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 89.0 Ohms. | $V_{CC}$ filtering and signal damping |
| R2 | General purpose | 27 Ω, 5 %, 200 PPM | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing.<br>For proper device function, the minimum value can be 0 Ohms. The maximum value is determined by the minimum bus voltage provided at the module pin. To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 66.6 Ohms. If the low response current is used, the maximum resistance including all tolerances is 133 Ohms. | $I_{DATA}$ filtering and signal damping |
| R3 | General purpose | 20 kΩ, 5 %, 200 PPM | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. | Gate resistor for external low side daisy chain FET |
| C1 | Ceramic | 2.2 nF, 10 %, 50 V minimum, X7R | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. | $V_{CC}$ power supply decoupling and signal damping. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN connector pins as possible. |
| C2 | Ceramic | 15 nF, 10 %, 50 V minimum, X7R | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. | $V_{CC}$ power supply decoupling. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN pins as possible. |
| C3 | Ceramic | 470 pF, 10 %, 50 V minimum, X7R | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. | $I_{DATA}$ Filtering and Signal Damping |
| C4 | Ceramic | 0.47 µF, 10 %, 10 V minimum, X7R | The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22 µF. The maximum specified value including all tolerances is 2 µF. | For optimal EMC performance, this component is to be placed as close to the VBUF and BUSRTN pins as possible. |
| R4 | General purpose | 100 kΩ, 5 %, 200 PPM | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. | Gate pulldown resistor for external low side daisy chain FET |
| M1 | N-Channel MOSFET | NTR4501NT1G, or similar | The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. | Low side daisy chain transistor |

1. *The total bus capacitance must not exceed the values specified in the PSI5 standard.*
2. *R1 must be sized to handle both the programming current at the maximum rated temperature for programming and the operating current at the maximum rated temperature for operation.*
3. *If the high baud rate is used, ST recommends reducing the value of C2. The actual value depends on the bus configuration and number of slaves.*

## 3.3 SPI application diagram

Figure 5. SPI application diagram

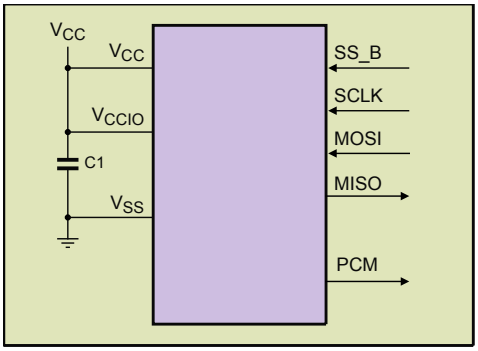



Table 6. SPI external component recommendations

| Ref Des | Type | Typical value description | Comment |
|---|---|---|---|
| C1 | Ceramic | 0.1 µF, 10 %, 10 V Minimum, X7R | $V_{CC}$ power supply decoupling. For optimal EMC performance, this component is to be placed as close to the $V_{CC}$ and $V_{SS}$ pins as possible. |

## 3.4 I²C application diagram

Figure 6. I²C application diagram

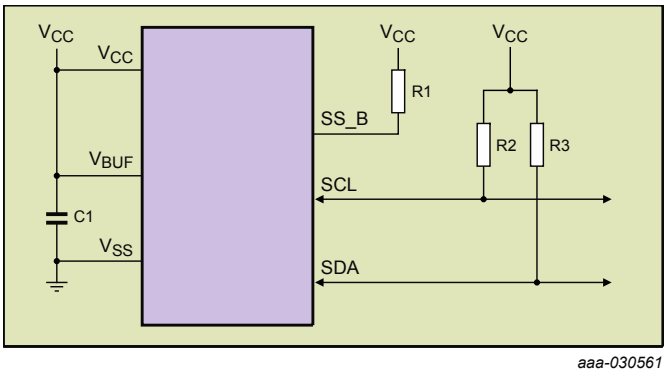
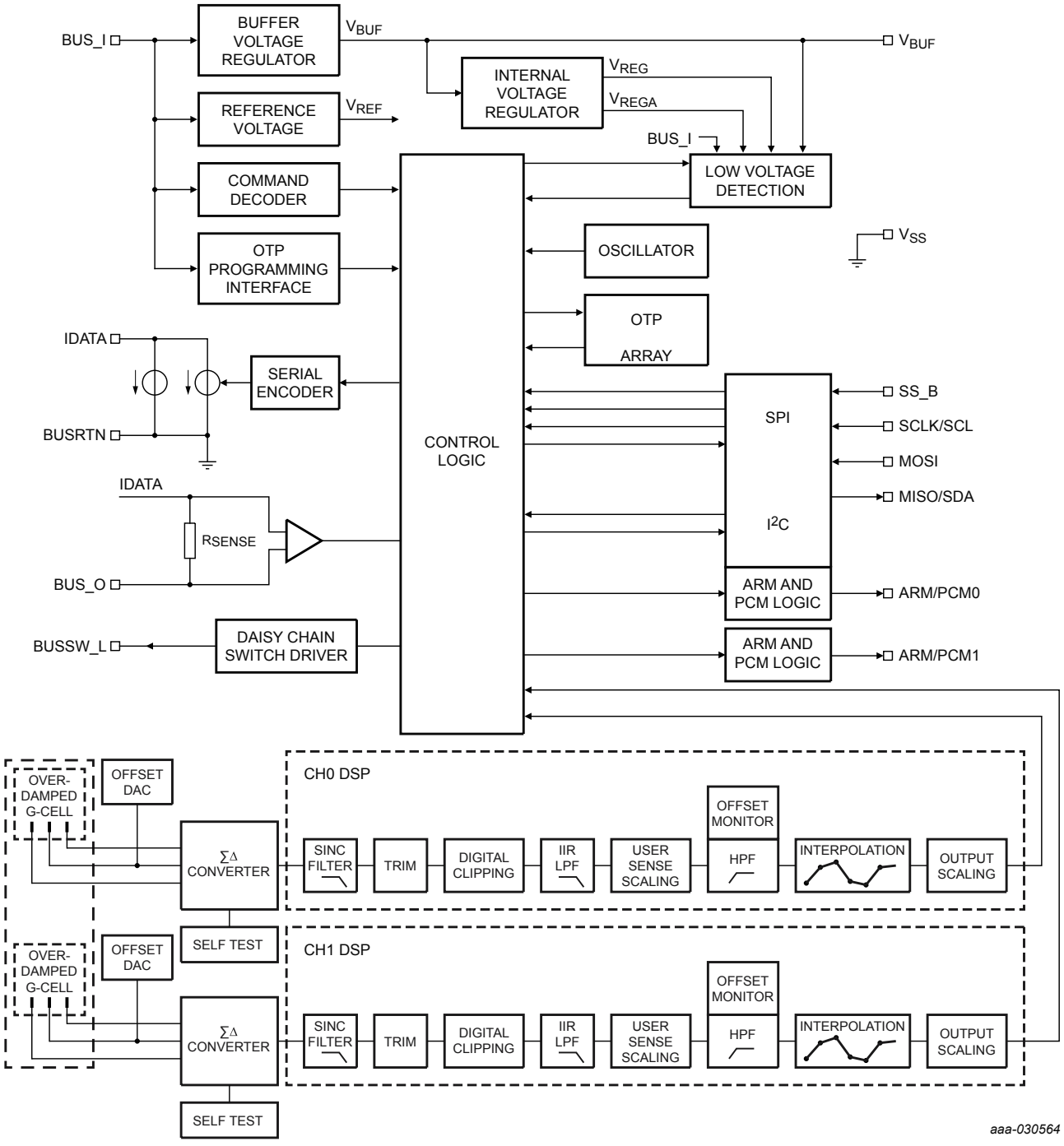



Table 7. I²C external component recommendations

| Ref Des | Type | Description | Purpose |
|---|---|---|---|
| R1 | General purpose | 1000 Ω, 5 %, 200 PPM | I²C selection pin pull-up resistor |
| R2 | General purpose | 1000 Ω, 5 %, 200 PPM | Serial clock pull-up resistor |
| R3 | General purpose | 1000 Ω, 5 %, 200 PPM | Serial data pull-up resistor |
| C1 | Ceramic | 0.1 µF, 10 %, 10 V Minimum, X7R | $V_{CC}$ power supply decoupling |

# 4 Block diagram

Figure 7. **Dual channel internal block diagram**



# 5 Device orientation diagrams

Figure 8. **Orientation diagram**

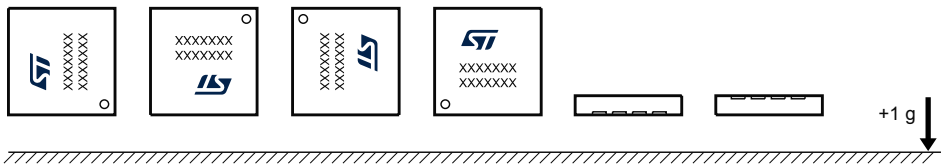


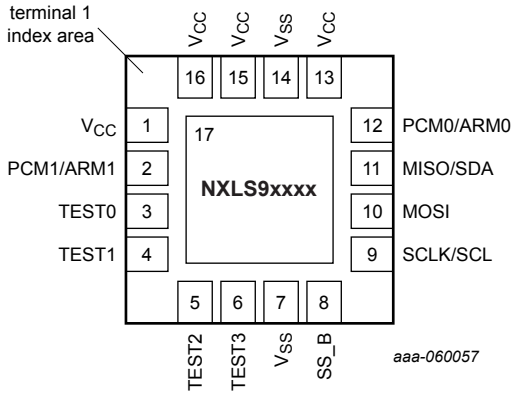

Table 8. **Dual axis device orientation**

| |  |  |  |  |  |  |
|---|---|---|---|---|---|---|
| **XY** | Ch0: 0 g | Ch0: +1 g | Ch0: 0 g | Ch0: –1 g | Ch0: 0 g | Ch0: 0 g |
| | Ch1: –1 g | Ch1: 0 g | Ch1: +1 g | Ch1: 0 g | Ch1: 0 g | Ch1: 0 g |
| **XZ** | Ch0: 0 g | Ch0: +1 g | Ch0: 0 g | Ch0: –1 g | Ch0: 0 g | Ch0: 0 g |
| | Ch1: 0 g | Ch1: 0 g | Ch1: 0 g | Ch1: 0 g | Ch1: +1 g | Ch1: –1 g |
| **YZ** | Ch0: –1 g | Ch0: 0 g | Ch0: +1 g | Ch0: 0 g | Ch0: 0 g | Ch0: 0 g |
| | Ch1: 0 g | Ch1: 0 g | Ch1: 0 g | Ch1: 0 g | Ch1: +1 g | Ch1: –1 g |

# 6 Pinning information

## 6.1 Pinning: SPI or I²C mode

**Figure 9. Device pinout: SPI or I²C mode**




Transparent topview

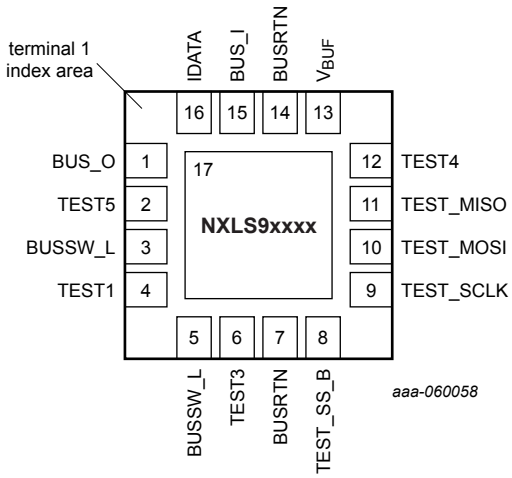
## 6.2 Pin description: SPI or I²C mode

**Table 9. Device pinout: SPI or I²C mode**

| Pin | Pin Name | Definition | Description |
|---|---|---|---|
| 1 | $V_{CC}$ | Supply | ST recommends that this pin be connected to $V_{CC}$. Optionally, this pin can be unterminated. |
| 2 | PCM1 / ARM1 | Channel 1 PCM<br>Channel 1 Arm | This pin has multiplexed functions:<br>• When the channel 1 arming output is selected, the pin can be configured as an open-drain, active low output with a pull-up current; or an open-drain, active high output with a pull-down current.<br>• When PCM mode is selected, this pin can be configured as a digital output with PCM signal proportional to the channel 1 sensor data.<br>If unused, or in I²C mode, ST recommends that this pin be unterminated. |
| 3, 4, 5, 6 | TEST | Test Pin | ST recommends that these pins be unterminated. Optionally, this pin can be tied to $V_{SS}$. |
| 7, 14 | $V_{SS}$ | Supply Return | This pin is the supply return node. |
| 8 | SS_B | Slave select | In SPI mode, this input pin provides the slave select for the SPI port. An internal pull-up device is connected to this pin.<br>In I²C mode, this pin must be connected to $V_{BUF}$ with an external pull-up resistor as shown in Figure 6. I²C application diagram. |
| 9 | SCLK/SCL | SPI Clock | In SPI mode, this input pin provides the serial clock. An internal pull-down device is connected to this pin.<br>In I²C mode, this input pin provides the serial clock. This pin must be connected to $V_{BUF}$ with an external pull-up resistor as shown in Figure 6. I²C application diagram. |
| 10 | MOSI | SPI Data In | In SPI mode, this pin functions as the serial data input to the SPI port. An internal pull-down device is connected to this pin.<br>In I²C mode, ST recommends that this pin be unterminated. Optionally, this pin can be connected to $V_{SS}$. |
| 11 | MISO/SDA | SPI Data Out | In SPI mode, this pin functions as the serial data output.<br>In I²C mode, this pin functions as the serial data input/output. This pin must be connected to $V_{BUF}$ with an external pull-up resistor as shown in Figure 6. I²C application diagram. |
| 12 | PCM0 / ARM0 | Channel 0 PCM<br>Channel 0 Arm | This pin has multiplexed functions:<br>• When the channel 0 arming output is selected, the pin can be configured as an open-drain, active low output with a pull-up current; or an open-drain, active high output with a pull-down current.<br>• When PCM mode is selected, this pin can be configured as a digital output with PCM signal proportional to the channel 0 sensor data.<br>If unused, or in I²C mode, ST recommends that this pin be unterminated. |
| 13, 15, 16 | $V_{CC}$ | Supply | This pin is connected to the supply for the device. An external capacitor must be connected between this pin and $V_{SS}$ as shown in Figure 5. SPI application diagram and Figure 6. I²C application diagram. |
| 17 | PAD | Die Attach Pad | This pin is the die attach flag, and must be connected to $V_{SS}$. See Section 13: Package outlines for die attach pad connection details. |

## 6.3 Pinning: DSI3 or PSI5 mode

**Figure 10. Device pinout: DSI3 or PSI5 mode pinout**




Transparent topview

## 6.4 Pin description: DSI3 or PSI5 mode

**Table 10. Device pinout: DSI3 or PSI5 mode pinout**

| Pin | Pin Name | Definition | Description |
|---|---|---|---|
| 1 | BUS_O | Supply Out | This pin is connected to the IDATA pin through an internal sense resistor and provides the supply connection to the next slave in a daisy chain configuration.<br>In DSI3 mode, an external capacitor must be connected between this pin and $V_{SS}$ as shown in Figure 2. DSI3 discovery mode application diagram.<br>In PSI5 mode, ST recommends that this pin be unterminated. Optionally, this pin can be connected to IDATA. |
| 2, 4, 6, 12 | TEST | Test Pin | ST recommends that these pins be unterminated. Optionally, this pin can be tied to $V_{SS}$. |
| 3, 5 | BUSSW_L | Low Side Bus Switch Driver | In PSI5 daisy chain mode, these pins are connected to the gate of an N-channel FET which connects BUSRTN to the next slave in the daisy chain. An external pulldown resistor is required on the gate of the N-channel FET as shown in Figure 4. PSI5 daisy chain mode application diagram. Note: both pins provide the identical function. It is necessary to connect only one pin is to the bus switch gate.<br>If unused, or in DSI3 mode, ST recommends that this pin be unterminated. Optionally, this pin can be tied to $V_{SS}$. |
| 7, 14 | BUSRTN/$V_{SS}$ | Supply Return | This pin is the supply return node. |
| 8 | TEST_SS_B | Slave select | ST recommends that this pin be unterminated. Optionally, this pin can be connected to $V_{BUF}$. |
| 9 | TEST_SCLK | SPI Clock | ST recommends that this pin be unterminated. Optionally, this pin can be connected to $V_{SS}$. |
| 10 | TEST_MOSI | SPI Data In | ST recommends that this pin be unterminated. Optionally, this pin can be connected to $V_{SS}$. |
| 11 | TEST_MISO | SPI Data Out | This pin must be left unconnected. |
| 13 | $V_{BUF}$ | Power Supply | This pin is connected to a buffer regulator for the internal circuitry. The buffer regulator supplies the internal regulators to provide immunity from EMC and supply dropouts. An external capacitor must be connected between this pin and $V_{SS}$ as shown in Figure 2. DSI3 discovery mode application diagram, Figure 3. PSI5 parallel or universal mode application diagram, and Figure 4. PSI5 daisy chain mode application diagram. |
| 15 | BUS_I | Supply and Communication Receiver | This pin is connected to the supply line and supplies power to the device. An external filter must be connected between this pin and BUSRTN as shown in Figure 2. DSI3 discovery mode application diagram, Figure 3. PSI5 parallel or universal mode application diagram, and Figure 4. PSI5 daisy chain mode application diagram. |
| 16 | IDATA | Communication Transmitter | This pin modulates the response current for DSI3 and PSI5 communication. An external filter must be connected between this pin and BUSRTN as shown in Figure 2. DSI3 discovery mode application diagram, Figure 3. PSI5 parallel or universal mode application diagram, and Figure 4. PSI5 daisy chain mode application diagram. |
| 17 | PAD | Die Attach Pad | This pin is the die attach flag, and must be connected to $V_{SS}$. See Section 13: Package outlines for die attach pad connection details. |

# 7 Electrical characteristics

Section 7.1: Maximum ratings through Section 7.21: Dynamic electrical characteristics - supply and support circuitry contain tables with "Test notes". The note identifiers cross reference to the identifiers and descriptions found in Table 11. Test notes legend.

**Table 11. Test notes legend**

| Identifier | Description |
|---|---|
| * | Indicates critical characteristic. |
| 1 | Parameter tested 100 % at final test. Temperature = –40 °C, 25 °C, and 105 °C, $V_{BUS\_I}$ = 7 V, Unless otherwise stated |
| 2 | Parameter tested 100 % at final test during safe launch |
| 3 | Parameter verified by pass/fail testing at final test |
| 4 | Parameter verified by pass/fail testing at final test during safe launch |
| 5 | Parameter verified by qualification testing |
| 6 | Parameter verified by characterization |
| 7 | Functionality verified by modeling, simulation and/or design verification. |
| 8 | Circuit integrity assured through IDDQ and scan testing. Timing is determined by internal system clock frequency. |
| 9 | Parameter verified by functional evaluation |
| 10 | Thermal resistance provided with device mounted to a 2 layer, 1.6 mm FR4 PCB as documented in AN1902 with 1 signal layer and 1 ground layer. |
| 11 | Digital low-pass filter characteristics are specified independently and do not include g-cell characteristics. Higher frequency filters will have lower system cut-off frequencies due to the g-cell damping. |

## 7.1 Maximum ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it.

**Table 12. Maximum ratings**

| # | Rating | Symbol | Value | Unit | Test notes |
|---|---|---|---|---|---|
| **Supply Voltage (BUS_I/$V_{CC}$, IDATA, BUS_O)** | | | | | |
| 3381 | Reverse Current externally limited to ≤ 160 mA, t ≤ 100 ms | BUS_$I_{REV}$ | –0.7 | V | 6 |
| 3383 | Continuous | BUS_$I_{MAX}$ | +20.0 | V | 6 |
| 3384 | $V_{BUF}$ | VBUFMAX | –0.3 to +7.0 | V | 6 |
| 3385 | SCLK, SS_B, MOSI, MISO (High Z), PCM0/ARM0, PCM1/ARM1 | VIOMAX | –0.3 to $V_{BUF}$ +0.3 | V | 6 |
| 3386 | BUS_I/$V_{CC}$, IDATA, and BUS_O Continuous Current | $I_{SUPMAX}$ | 200 | mA | 6 |
| 3387 | Powered Shock (six sides, 0.5 ms duration) | $g_{pms}$ | ±2000 | g | 5 |
| 3390 | Unpowered Shock (six sides, 0.5 ms duration) | $g_{shock}$ | ±2000 | g | 5 |
| 3389 | Powered Shock (six sides, 0.5 ms duration) | $g_{pms}$ | ±4000 | g | 9 |
| 3388 | Unpowered Shock (six sides, 0.5 ms duration) | $g_{shock}$ | ±4000 | g | 9 |
| 3391 | Drop Shock (to concrete, tile or steel surface, 10 drops, any orientation) | $h_{DROP}$ | 1.5 | m | 5 |
| **Electrostatic Discharge (per AEC-Q100 [4] ), External Pins** | | | | | |
| 3392 | BUS_I/$V_{CC}$, IDATA, BUS_O, BUSRTN, HBM (100 pF, 1.5 kΩ) | $V_{ESD}$ | ±4000 | V | 5 |
| **Electrostatic Discharge (per AEC-Q100 [4] )** | | | | | |
| 3393 | HBM (100 pF, 1.5 kΩ) | $V_{ESD}$ | ±2000 | V | 5 |
| 3395 | CDM (R = 0 Ω) | $V_{ESD}$ | ±750 | V | 5 |
| **Temperature Range** | | | | | |
| 3396 | Storage | $T_{stg}$ | –55 to +150 | °C | 5 |
| 3397 | Junction | $T_J$ | –55 to +150 | °C | 7 |
| 3400 | Thermal Resistance | $\theta_{JA}$ | 47 | °C/W | 7 , 10 |

## 7.2 Operating range - DSI / PSI5

**Table 13. Operating range - DSI / PSI5**

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| 3398 | DSI3 Supply Voltage ($V_{HIGH}$), Measured at BUS_I * | $V_{HIGH}$ | — | | 20.0 | V | 5 , 6 , 7 |
| 10468 | DSI3 Supply Voltage ($V_{LOW}$) Measured at BUS_I * | $V_{LOW}$ | 4.0 | — | — | V | 1 |
| 10467 | PSI5 Supply Voltage (Excluding Sync Pulse) * | $V_{PSI5}$ | 4.0 | — | 16.5 | V | 1 |
| 10466 | Supply Voltage (Undervoltage) | $V_{BUS\_I\_UV}$ | $V_{BUS\_I\_UV\_F}$ | — | $V_{LOW\_min}$ | V | 3 , 6 |
| 10472 | Supply Power On Ramp Rate | $V_{CC\_RAMP\_SAT}$ | 0.00001 | — | 10 | V / µs | 6 |
| **Programming Voltage ($I_{PP}$ ≤ 5 mA, 10 °C ≤ $T_A$ ≤ 40 °C)** | | | | | | | |
| 10469 | Applied to BUS_I | $V_{PP}$ | 9.0 | 10.0 | 11.0 | V | 3 , 6 |
| **ESD Operating Voltage (No Device Reset, $C_{BUS\_IN}$ = 220 pF)** | | | | | | | |
| 10470 | Maximum ±15 kV Air Discharge, 330 pF, 2.0 kΩ | $V_{BUS\_I\_ESD}$ | $V_{BUS\_I\_LOW\_min}$ | — | 10.0 | V | 7 , 9 |
| **Operating Temperature Range** | | | $T_L$ | | $T_H$ | | |
| 10471 | Production Tested Operating Temperature Range | $T_A$ | –40 | — | +105 | °C | 1 |
| 10490 | Guaranteed Operating Temperature Range | $T_A$ | –40 | — | +125 | °C | 5 , 6 , 7 |

## 7.3 Operating range - SPI / I²C

**Table 14. Operating range - SPI / I²C**

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| 10501 | Supply Voltage ($V_{CC}$ = $V_{BUF}$) Measured at $V_{BUF}$ | $V_{CC\_BUF}$ | — | — | 5.25 | V | 5, 6, 7 |
| 10502 | Supply Voltage ($V_{CC}$ = $V_{BUF}$) Measured at $V_{BUF}$ * | $V_{CC\_BUF}$ | 3.135 | — | — | V | 1 |
| 10504 | Supply Voltage (Undervoltage) | $V_{BUF\_UV\_OP}$ | $V_{BUF\_UV\_F}$ | — | $V_{CC\_BUF\_min}$ | V | 3, 6 |
| 10509 | Supply Power On Ramp Rate | $V_{CC\_RAMP\_SPI}$ | 0.00001 | — | 10 | V/µs | 6 |
| **Operating Temperature Range** | | | $T_L$ | | $T_H$ | | |
| 10507 | Production Tested Operating Temperature Range | $T_A$ | –40 | — | +105 | °C | 1 |
| 10508 | Guaranteed Operating Temperature Range | $T_A$ | –40 | — | +125 | °C | 5, 6, 7 |

## 7.4 Electrical characteristics - supply and I/O

**Table 15. Electrical characteristics - supply and I/O**

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

| # | Characteristic | | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|---|
| **Quiescent Supply Current** | | | | | | | | |
| 39203 | $V_{BUS\_I}$ = 4 V, DSI, PSI5 | * | $I_{q\_4\_2}$ | 4.0 | 9.2 | 10.0 | mA | 1 |
| 39204 | $V_{BUS\_I}$ = 20 V, DSI / PSI5 | * | $I_{q\_20\_2}$ | 4.0 | 9.2 | 10.0 | mA | 1 |
| 39205 | $V_{BUS\_I}$ = 3.135 V, SPI, I²C | * | $I_{q\_31\_2}$ | — | — | 10.0 | mA | 3, 6 |
| **Response Current** | | | | | | | | |
| 10515 | DSI Low | * | $I_{R\_DSI\_1}$ | $I_q$ + 10.5 | $I_q$ + 12.0 | $I_q$ + 13.5 | mA | 1 |
| 10519 | DSI High | * | $I_{R\_DSI\_2}$ | $I_{R\_DSI\_1}$ + 10.5 | $I_{R\_DSI\_1}$ + 12.0 | $I_{R\_DSI\_1}$ + 13.5 | mA | 1 |
| 10518 | PSI5 Normal | * | $I_{R\_PSI5}$ | $I_q$ + 22.0 | $I_q$ + 26.0 | $I_q$ + 30.0 | mA | 1 |
| 10517 | PSI5 Low | * | $I_{R\_PSI5\_Low}$ | $I_q$ + 11.0 | $I_q$ + 13.0 | $I_q$ + 15.0 | mA | 6 |
| | In-Rush Current (No external Components) | | $t_{INRUSH}$ | — | — | 40 | mA | 6 |
| **Internally Regulated Voltage** | | | | | | | | |
| 10522 | ($V_{BUF}$, $V_{BUS\_I}$ = 4 V, $V_{BUS\_I}$ = 20 V) | | $V_{BUF}$ | 2.85 | 3.00 | 3.15 | V | 1 |
| **Low Voltage Detection Threshold** | | | | | | | | |
| 10523 | BUS_I Falling, COMMTYPE = 2, 3, 4, 5, 6, 7 | * | $V_{BUS\_I\_UV\_F}$ | 3.85 | 3.95 | 4.00 | V | 3, 6 |
| | BUS_I Falling, COMMTYPE = 0, 1 | | $V_{BUS\_I\_UV\_01}$ | 3.31 | 3.50 | 3.67 | V | 6 |
| 10542 | $V_{BUF}$ Falling | * | $V_{BUF\_UV\_F}$ | 2.64 | 2.74 | 2.84 | V | 3, 6 |
| **$V_{BUF}$ External Capacitor** | | | | | | | | |
| 10525 | Capacitance | | CVBUF | 100 | 1000 | 2000 | nF | 7, 9 |
| 10543 | ESR (including interconnect resistance) | | ESR | 0 | — | 200 | mΩ | 7, 9 |
| **DSI3 $V_{LOW}$ Detection Threshold (Section 9.1.1: Command receiver)** | | | | | | | | |
| **$V_{LOW\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{HIGH\_max}$** | | | | | | | | |
| 10526 | $V_{LOW}$ Detection Threshold | * | $V_{DELTA\_THRESH}$ | $V_{HIGH}$ – 1.25 | $V_{HIGH}$ – 1.0 | $V_{HIGH}$–0.75 | V | 3, 6 |
| **DSI3 Discovery Mode Current Sense (Section 9.2.3: DSI3 discovery mode: Address assignment method for resistor connected daisy chain devices)** | | | | | | | | |
| 10527 | Sense Resistor | | $R_{SENSE}$ | 1.0 | 1.3 | 3.0 | Ω | 6 |
| 10545 | $I_{RESP}$ Detection Threshold ($I_{BUS\_O\_q} \le 24$ mA) | | $I_{RESP\_Offset}$ | 6 | 12 | 18 | mA | 3, 6 |
| **PSI5 Synchronization Pulse** | | | | | | | | |
| **$V_{PSI5\_min} \le (V_{BUS\_I} - V_{SS}) \le BUS\_I_{MAX}$** | | | | | | | | |
| 10528 | DC Sync Pulse Detection Threshold | | $\Delta V_{SYNC}$ | $V_{PSI5}$+1.0 | $V_{PSI5}$+1.5 | $V_{PSI5}$+2.0 | V | 3, 6 |
| 10529 | PSI5 Sync Pulse Pulldown Current | | $I_{SYNC\_PD}$ | — | $I_{R\_PSI5}$ | — | mA | 7 |
| **Bus Switch Output** | | | | | | | | |
| 10530 | High Voltage (BUSSW_L, $I_{Load}$ = –100 µA) | | $V_{BUSSW\_L\_OH}$ | $V_{BUF}$ – 0.35 | — | $V_{BUF}$ | V | 3, 6 |
| 10546 | Low Voltage (BUSSW_L, $I_{Load}$ = 100 µA) | | $V_{BUSSW\_L\_OL}$ | — | — | 0.1 | V | 3, 6 |
| **Open-Drain Output (ARM0, ARM1)** | | | | | | | | |
| 10549 | Pulldown Current ($V_{ARM}$ = 1.5 V) | | $I_{ODPD}$ | 10 | 20 | 100 | µA | 3, 6 |
| 10536 | Pullup Current ($V_{ARM}$ = 1.5 V) | | $I_{ODPU}$ | –100 | –20 | –10 | µA | 3, 6 |
| **Output Voltage** | | | | | | | | |
| 21205 | $V_{BUF}$ = VCC, $I_{Load}$ = –1 mA | | $V_{OH}$ | $V_{BUF}$ – 0.2 | — | $V_{BUF}$ | V | 3, 6 |
| | $V_{BUF}$ internally regulated, $I_{Load}$ = –1 mA | | $V_{OH\_SAT}$ | $V_{BUF}$ – 0.2 | — | $V_{BUF}$ | V | 3, 6 |
| 10547 | Output Low Voltage (MISO/SDA, PCM0/ARM0, PCM1/ARM1), $I_{Load}$ = 2 mA | | $V_{OL}$ | — | — | 0.4 | V | 3, 6 |
| **Input Voltage** | | | | | | | | |
| 10537 | Input High Voltage SS_B, SCLK/SCL, MOSI | | $V_{IH}$ | 2.0 | — | — | V | 3, 7 |
| 10560 | Input Low Voltage SS_B, SCLK/SCL, MOSI | | $V_{IL}$ | — | — | 1.0 | V | 3, 7 |

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| 10561 | Input Voltage Hysteresis SS_B, SCLK, MOSI | $V_{I\_HYST}$ | — | 0.250 | — | V | 7 |
| 10562 | Input Current High (at $V_{IH}$) (SCLK/SCL, MOSI) | $I_{IH}$ | 10 | 20 | 70 | µA | 6 |
| 10565 | Input Current Low (at $V_{IL}$) (SS_B) | $I_{IL}$ | –70 | –20 | –10 | µA | 6 |
| 10563 | MISO Output Leakage | $I_{MISO\_Lkg}$ | –10 | — | 10 | µA | 6 |

## 7.5 Electrical characteristics - temperature sensor signal chain

**Table 16. Electrical characteristics - temperature sensor signal chain**

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| 10520 | Temperature Measurement Range | $T_{RANGE}$ | –50 | — | +160 | °C | 7, 9 |
| 10559 | Temperature Output at 25 °C | $T_{25}$ | 83 | 93 | 103 | LSB | 6, 7 |
| **Range of Output (8 bit)** | | | | | | | |
| 10558 | Unsigned Temperature | $T_{RANGE}$ | 0 | — | 255 | LSB | 7, 8, 9 |
| 10557 | Temperature Output Sensitivity (8 bit) | $T_{SENSE}$ | | 1.10 | | LSB/°C | 6, 7 |
| 10556 | Temperature Output Accuracy (8 bit) | $T_{ACC}$ | –20 | | +20 | °C | 6, 7 |
| **Temperature Output Noise RMS (8 bit)** | | | | | | | |
| 10555 | Standard Deviation of 50 readings, $f_{Samp}$ = 8 kHz | $T_{RMS}$ | — | — | +2 | LSB | 6, 7 |

## 7.6 Electrical characteristics - inertial sensor signal chain: High g

**Table 17. Electrical characteristics - inertial sensor signal chain: High g**

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Sensitivity** | | | | | | | |
| **Total Sensitivity Error Including Linearity (From Trim Target, Output @ 0 Hz)** | | | | | | | |
| 10584 | High g, lateral, or Z-Axis, verified with a 50 g Range * | $SENS_{ERRH}$ | –5 | — | +5 | % | 1 |
| **High g Standard Trim Range 12-bit Sensitivity Target, Lateral, or Z-Axis** | | | | | | | |
| 10612 | ± 50 g Range (± 2047 LSB, U_SNS_SHIFT = 0x3, U_SNS_MULT = 0xDF) * | $SENS_{50H}$ | 38.9157 | 40.9639 | 43.0121 | LSB/g | 1 |
| **Offset** | | | | | | | |
| 10626 | Digital Offset Before Offset Cancellation, 12 bit, Lateral or Z-Axis High g (100 g Range, scales with user sensitivity scaling) * | $OFF_{High\_1}$ | –100 | — | +100 | LSB | 1 |
| 10583 | Digital Offset After Offset Cancellation, Lateral, or Z-Axis, All Ranges, 12 bit | $OFFCANC_{12Bit}$ | –1 | 0 | +1 | LSB | 6, 8, 9 |
| | Digital Offset After Offset Cancellation with rate limiter, Lateral, or Z-Axis, All Ranges, 12 bit | $OFFCANCRL_{12Bit}$ | –2 | 0 | +2 | LSB | 7, 8, 9 |
| **Continuous Offset Monitor Limit (U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00)** | | | | | | | |
| 10619 | 12 bit: Scales with user gain, High g = ~15 g | $OFF_{MON}$ | –164 | — | +164 | LSB | 7, 8, 9 |
| **Sensor** | | | | | | | |
| **Range of Signed Output (SPI, DSI3, Lateral, or Z-Axis, All Ranges)** | | | | | | | |
| 10635 | Signed Sensor Data, 10 bit | $RANGE_{Signed\_10}$ | –511 | — | +511 | LSB | 7, 8, 9 |
| 10628 | Signed Sensor Data, 12 bit | $RANGE_{Signed\_12}$ | –2047 | — | +2047 | LSB | 7, 8, 9 |
| 10636 | Signed Error Code, 10 bit | $ERR_{Signed\_10}$ | — | –512 | — | LSB | 7, 8, 9 |
| 10637 | Signed Error Code, 12 bit | $ERR_{Signed\_12}$ | — | –2048 | — | LSB | 7, 8, 9 |
| **Range of Unsigned Output (SPI, DSI3, Lateral, or Z-Axis, All Ranges)** | | | | | | | |
| 10638 | Unsigned Sensor Data, 10 bit | $RANGE_{Unsigned\_10}$ | 1 | — | 1023 | LSB | 7, 8, 9 |
| 10639 | Unsigned Sensor Data, 12 bit | $RANGE_{Unsigned\_12}$ | 1 | — | 4095 | LSB | 7, 8, 9 |
| 10640 | Unsigned Error Code, 10 bit, 12 bit | $ERR_{Unsigned}$ | — | 0 | — | LSB | 7, 8, 9 |
| **Range of Signed Output (PSI5, Lateral, or Z-Axis, All Ranges)** | | | | | | | |
| 10634 | Signed Sensor Data, 10 bit | $RANGE_{Signed\_10}$ | –480 | — | +480 | LSB | 7, 8, 9 |
| **Cross-Axis Sensitivity, Lateral, or Z-Axis, All Ranges** | | | | | | | |
| 10645 | Z-axis to X-Axis, Y-axis to X-Axis, Z-axis to Y-Axis, X-axis to Y-Axis | $V_{ZX}$, $V_{YX}$ | –5 | — | +5 | % | 6 |
| 10647 | X-axis to Z-Axis, Y-axis to Z-Axis | $V_{XZ}$, $V_{YZ}$ | –5 | — | +5 | % | 6 |
| **Non-Linearity (12 bit, Lateral, or Z-Axis, All Ranges)** | | | | | | | |
| 10669 | Differential Non-Linearity (No Missing Codes) * | DNL | — | — | +1.0 | LSB | 7 |
| 10670 | End Point Non-Linearity (Least Squares BFSL) * | INL | — | — | +20.0 | LSB | 6 |
| **Supply Coupling ($C_{BUF}$ = 1 µf, 12 bit, DSI3, PSI5, Lateral, or Z-Axis, All Ranges)** | | | | | | | |
| 10663 | 1 kHz ≤ $f_n$ ≤ 10 kHz, BUS_I = 8.0 V ± 2.0 V (Represents PSI5 Sync Pulse) | $PSC_{PSI5}$ | — | — | 1 | LSB | 6 |
| 10682 | 10 kHz ≤ $f_n$ ≤ 100 kHz, BUS_I = 6.0 V ± 1.0 V (Represents DSI3 BRC) | $PSC_{DSI3C}$ | — | — | 1 | LSB | 6 |
| 10681 | 100 kHz ≤ $f_n$ ≤ 1 MHz, BUS_I = 6.0 V ± 0.5 V (Represents DSI3/PSI5 Response) | $PSC_{DSI3R}$ | — | — | 1 | LSB | 6 |
| 10680 | 1 MHz ≤ $f_n$ ≤ 20 MHz, BUS_I = 6.0 V ± 0.1 V (Represents Response Harmonics) | $PSC_{SATH}$ | — | — | 1 | LSB | 6 |
| **Supply Coupling ($C_{BUF}$ = 0.1 µf, 12 bit, SPI, Lateral, or Z-Axis, All Ranges)** | | | | | | | |
| 10675 | 1 kHz ≤ $f_n$ ≤ 20 MHz, $V_{BUF}$ = 5.0 V ± 0.1 V | $PSC_{SPI5}$ | — | — | 2 | LSB | 6 |
| 10683 | 1 kHz ≤ $f_n$ ≤ 20 MHz, $V_{BUF}$ = 3.3 V ± 0.1 V | $PSC_{SPI3}$ | — | — | 2 | LSB | 6 |
| **Noise: Lateral Sensor** | | | | | | | |
| **System Output Noise Peak (12 bit), High g Range = 125 g, Lateral** | | | | | | | |
| 10653 | Max. Deviation from Mean, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{PeakX\_400C}$ | –14 | — | +14 | LSB | 6 |
| 10655 | Max. Deviation from Mean, Min. 50 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{PeakX\_400T}$ | –14 | — | +14 | LSB | 1 |
| **System Output Noise Average (12 bit), High g Range = 125 g, Lateral** | | | | | | | |
| 10654 | Standard Deviation, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{RMSX\_400C}$ | — | — | +3.5 | LSB | 6 |

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| 10656 | Standard Deviation, Min. 50 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{RMSX\_400T}$ | — | — | +3.5 | LSB | 1 |
| **Noise: Z-Axis Sensor** | | | | | | | |
| **System Output Noise Peak (12 bit), High g Range = 125 g, Z-Axis** | | | | | | | |
| 10659 | Max. Deviation from Mean, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{PeakZ\_400C}$ | –14 | — | +14 | LSB | 6 |
| 10661 | Max. Deviation from Mean, Min. 50 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{PeakZ\_400T}$ | –14 | — | +14 | LSB | 1 |
| **System Output Noise Average (12 bit), High g Range = 125 g, Z-Axis** | | | | | | | |
| 10660 | Standard Deviation, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{RMSZ\_400C}$ | — | — | +3.5 | LSB | 6 |
| 10662 | Standard Deviation, Min. 50 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{RMSZ\_400T}$ | — | — | +3.5 | LSB | 1 |

The offset before offset cancellation scales with the user gain. The higher the gain (lower range), the higher the offset. Table 18. High g adjusted offset specification limits lists the adjusted offset specification limits for some SPI and DSI3 12-bit user gain settings.

**Table 18. High g adjusted offset specification limits**

| User range (g) | Offset (LSB, 12 bit) |
|---|---|
| 50 | ± 200 |
| 60 | ± 167 |
| 62 | ± 162 |
| 62.5 | ± 160 |
| 100 | ± 100 |
| 105 | ± 96 |
| 112.5 | ± 89 |
| 125 | ± 80 |
| 128 | ± 79 |
| 150 | ± 67 |
| 187 | ± 54 |
| 250 | ± 40 |
| 312.5 | ± 32 |
| 375 | ± 27 |
| 500 | ± 20 |

Table 19. PSI5, High g offset cancellation limits lists the offset before offset cancellation limits for some PSI5 10-bit user gain settings.

**Table 19. PSI5, High g offset cancellation limits**

| User range (g) | Offset (LSB, 10 bit) |
|---|---|
| 60 | ± 40 |
| 120 | ± 20 |
| 240 | ± 10 |
| 480 | ± 5 |

The signal noise scales with the user gain and with signal bandwidth. The higher the gain (lower range), the higher the noise, the wider the bandwidth, the higher the noise. Table 20. Lateral, High g, SPI/DSI3 12-bit noise specification and Table 21. Z-Axis, High g, SPI/DSI3 12-bit noise specification lists the adjusted specification limits for some user gain settings and low-pass filter selections on the Lateral, and Z-axis.

*Note: Peak values indicate the maximum deviation from the mean.*

**Table 20. Lateral, High g, SPI/DSI3 12-bit noise specification**

| User range (g) | LPF 400 Hz, 4p | | LPF 400 Hz, 3p | | LPF 180 Hz, 2p | | LPF 325 Hz, 3p | | LPF 1500 Hz, 4p | | LPF 800 Hz, 4p | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit |
| 50 | 35 | 9 | 37 | 10 | 25 | 7 | 33 | 9 | 68 | 17 | 50 | 13 |
| 62.5 | 28 | 7 | 29 | 8 | 20 | 5 | 26 | 7 | 55 | 14 | 40 | 10 |
| 100 | 18 | 5 | 19 | 5 | 13 | 4 | 17 | 5 | 34 | 9 | 25 | 7 |
| 125 | 14 | 4 | 15 | 4 | 10 | 3 | 13 | 4 | 28 | 7 | 20 | 5 |
| 187 | 10 | 3 | 10 | 3 | 7 | 2 | 9 | 3 | 19 | 5 | 14 | 4 |
| 250 | 7 | 2 | 8 | 2 | 5 | 2 | 7 | 2 | 14 | 4 | 10 | 3 |
| 312.5 | 6 | 2 | 6 | 2 | 4 | 1 | 6 | 2 | 11 | 3 | 8 | 2 |
| 375 | 5 | 2 | 5 | 2 | 4 | 1 | 5 | 2 | 10 | 3 | 7 | 2 |
| 500 | 4 | 1 | 4 | 1 | 3 | 1 | 4 | 1 | 7 | 2 | 5 | 2 |

**Table 21. Z-Axis, High g, SPI/DSI3 12-bit noise specification**

| User range (g) | LPF 400 Hz, 4p | | LPF 400 Hz, 3p | | LPF 180 Hz, 2p | | LPF 325 Hz, 3p | | LPF 1500 Hz, 4p | | LPF 800 Hz, 4p | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit |
| 50 | 35 | 9 | 37 | 10 | 25 | 7 | 33 | 9 | 68 | 17 | 50 | 13 |
| 62.5 | 28 | 7 | 29 | 8 | 20 | 5 | 26 | 7 | 55 | 14 | 40 | 10 |
| 100 | 18 | 5 | 19 | 5 | 13 | 4 | 17 | 5 | 34 | 9 | 25 | 7 |
| 125 | 14 | 4 | 15 | 4 | 10 | 3 | 13 | 4 | 28 | 7 | 20 | 5 |
| 187 | 10 | 3 | 10 | 3 | 7 | 2 | 9 | 3 | 19 | 5 | 14 | 4 |
| 250 | 7 | 2 | 8 | 2 | 5 | 2 | 7 | 2 | 14 | 4 | 10 | 3 |
| 312.5 | 6 | 2 | 6 | 2 | 4 | 1 | 6 | 2 | 11 | 3 | 8 | 2 |
| 375 | 5 | 2 | 5 | 2 | 4 | 1 | 5 | 2 | 10 | 3 | 7 | 2 |
| 500 | 4 | 1 | 4 | 1 | 3 | 1 | 4 | 1 | 7 | 2 | 5 | 2 |

Table 22. Lateral, High g, PSI5 10-bit noise specification and Table 23. Z-Axis, High g, PSI5 10-bit noise specification list the adjusted specification limits for some PSI5 10-bit user gain settings and low-pass filter selections on the Lateral, and Z-axis.

**Table 22. Lateral, High g, PSI5 10-bit noise specification**

| User range (g) | LPF 400 Hz, 4p | | LPF 400 Hz, 3p | | LPF 800 Hz, 4p | |
|---|---|---|---|---|---|---|
| | Peak LSB 10 bit | RMS LSB 10 bit | Peak LSB 10 bit | RMS LSB 10 bit | Peak LSB 10 bit | RMS LSB 10 bit |
| 60, PSI5 | 9 | 2.1 | 9 | 2.2 | 12 | 3 |
| 120, PSI5 | 5 | 1.1 | 5 | 1.1 | 6 | 1.5 |
| 240 PSI5 | 3 | 0.6 | 3 | 0.6 | 3 | 0.8 |
| 480 PSI5 | 2 | 0.5 | 2 | 0.5 | 2 | 0.5 |

Table 23. **Z-Axis, High g, PSI5 10-bit noise specification**

| User range (g) | LPF 400 Hz, 4p | | LPF 400 Hz, 3p | | LPF 800 Hz, 4p | |
|---|---|---|---|---|---|---|
| | Peak LSB 10 bit | RMS LSB 10 bit | Peak LSB 10 bit | RMS LSB 10 bit | Peak LSB 10 bit | RMS LSB 10 bit |
| 60, PSI5 | 9 | 2.1 | 9 | 2.2 | 12 | 3 |
| 120, PSI5 | 5 | 1.1 | 5 | 1.1 | 6 | 1.5 |
| 240 PSI5 | 3 | 0.6 | 3 | 0.6 | 3 | 0.8 |
| 480 PSI5 | 2 | 0.5 | 2 | 0.5 | 2 | 0.5 |

## 7.7 Electrical characteristics - inertial sensor signal chain: Medium g

**Table 24. Electrical characteristics - inertial sensor signal chain: Medium g**

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Sensitivity** | | | | | | | |
| **Total Sensitivity Error Including Linearity (From Trim Target, Output @ 0 Hz)** | | | | | | | |
| 10585 | Medium g, Lateral or Z-Axis, Verified with a 15 g Range * | $SENS_{ERRM}$ | –5 | — | +5 | % | 1 |
| **Medium g Standard Trim Range 12-bit Sensitivity Target, Lateral or Z-Axis** | | | | | | | |
| 10602 | ± 16 g Range (±2047 LSB, U_SNS_SHIFT = 0x3, U_SNS_MULT = 0xF0) * | $SENS_{016M}$ | 121.5406 | 127.9375 | 134.3344 | LSB/g | 1 |
| **Offset** | | | | | | | |
| 10627 | Digital Offset Before Offset Cancellation, 12 Bit, Lateral or Z-Axis Medium g (25 g Range, scales with user sensitivity scaling) * | $OFF_{Med\_1}$ | –100 | — | +100 | LSB | 1 |
| 10583 | Digital Offset After Offset Cancellation, Lateral or Z-Axis, All Ranges, 12 bit | $OFFCANC_{12Bit}$ | –1 | 0 | +1 | LSB | 6, 8, 9 |
| | Digital Offset After Offset Cancellation with rate limiter, Lateral or Z-Axis, All Ranges, 12 bit | $OFFCANCRL_{12Bit}$ | –2 | 0 | +2 | LSB | 7, 8, 9 |
| **Continuous Offset Monitor Limit (U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00)** | | | | | | | |
| 10619 | 12 bit: Scales with user gain, Medium g = ~5 g | $OFF_{MON}$ | –164 | — | +164 | LSB | 7, 8, 9 |
| **Sensor** | | | | | | | |
| **Range of Signed Output (SPI, DSI3, Lateral or Z-Axis, All Ranges)** | | | | | | | |
| 10635 | Signed Sensor Data, 10 bit | $RANGE_{Signed\_10}$ | –511 | — | +511 | LSB | 7, 8, 9 |
| 10628 | Signed Sensor Data, 12 bit | $RANGE_{Signed\_12}$ | –2047 | — | +2047 | LSB | 7, 8, 9 |
| 10636 | Signed Error Code, 10 bit | $ERR_{Signed\_10}$ | — | –512 | — | LSB | 7, 8, 9 |
| 10637 | Signed Error Code, 12 bit | $ERR_{Signed\_12}$ | — | –2048 | — | LSB | 7, 8, 9 |
| **Range of Unsigned Output (SPI, DSI3, Lateral or Z-Axis, All Ranges)** | | | | | | | |
| 10638 | Unsigned Sensor Data, 10 bit | $RANGE_{Unsigned\_10}$ | 1 | — | 1023 | LSB | 7, 8, 9 |
| 10639 | Unsigned Sensor Data, 12 bit | $RANGE_{Unsigned\_12}$ | 1 | — | 4095 | LSB | 7, 8, 9 |
| 10640 | Unsigned Error Code, 10 bit, 12 bit | $ERR_{Unsigned}$ | — | 0 | — | LSB | 7, 8, 9 |
| **Range of Signed Output (PSI5, Lateral or Z-Axis, All Ranges)** | | | | | | | |
| 10634 | Signed Sensor Data, 10 bit | $RANGE_{Signed\_10}$ | –480 | — | +480 | LSB | 7, 8, 9 |
| **Cross-Axis Sensitivity, Lateral or Z-Axis, All Ranges** | | | | | | | |
| 10645 | Z-axis to X-Axis, Y-axis to X-Axis, Z-axis to Y-Axis, X-axis to Y-Axis | $V_{ZX}$, $V_{YX}$ | –5 | — | +5 | % | 6 |
| 10647 | X-axis to Z-Axis, Y-axis to Z-Axis | $V_{XZ}$, $V_{YZ}$ | –5 | — | +5 | % | 6 |
| **Non-Linearity (12 bit, Lateral or Z-Axis, All Ranges)** | | | | | | | |
| 10669 | Differential Non-Linearity (No Missing Codes) * | DNL | — | — | +1.0 | LSB | 7 |
| 10670 | End Point Non-Linearity (Least Squares BFSL) * | INL | — | — | +20.0 | LSB | 6 |
| **Supply Coupling ($C_{BUF}$ = 1 µf, 12 bit, DSI3, PSI5, Lateral or Z-Axis, All Ranges)** | | | | | | | |
| 10663 | 1 kHz ≤ $f_n$ ≤ 10 kHz, BUS_I = 8.0 V ± 2.0 V (Represents PSI5 Sync Pulse) | $PSC_{PSI5}$ | — | — | 1 | LSB | 6 |
| 10682 | 10 kHz ≤ $f_n$ ≤ 100 kHz, BUS_I = 6.0 V ± 1.0 V (Represents DSI3 BRC) | $PSC_{DSI3C}$ | — | — | 1 | LSB | 6 |
| 10681 | 100 kHz ≤ $f_n$ ≤ 1 MHz, BUS_I = 6.0 V ± 0.5 V (Represents DSI3/PSI5 Response) | $PSC_{DSI3R}$ | — | — | 1 | LSB | 6 |
| 10680 | 1 MHz ≤ $f_n$ ≤ 20 MHz, BUS_I = 6.0 V ± 0.1 V(Represents Response Harmonics) | $PSC_{SATH}$ | — | — | 1 | LSB | 6 |
| **Supply Coupling ($C_{BUF}$ = 0.1 µf, 12 bit, SPI, Lateral or Z-Axis, All Ranges)** | | | | | | | |
| 10675 | 1 kHz ≤ $f_n$ ≤ 20 MHz, $V_{BUF}$ = 5.0 V ± 0.1 V | $PSC_{SPI5}$ | — | — | 2 | LSB | 6 |
| 10683 | 1 kHz ≤ $f_n$ ≤ 20 MHz, $V_{BUF}$ = 3.3 V ± 0.1 V | $PSC_{SPI3}$ | — | — | 2 | LSB | 6 |
| **Noise: Lateral Sensor** | | | | | | | |
| **System Output Noise Peak (12 bit), Medium g Range = 50 g, Lateral** | | | | | | | |
| 10653 | Max. Deviation from Mean, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{PeakX\_400C}$ | –12 | — | +12 | LSB | 6 |
| 10655 | Max. Deviation from Mean, Min. 50 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{PeakX\_400T}$ | –12 | — | +12 | LSB | 1 |
| **System Output Noise Average (12 bit), Medium g Range = 50 g, Lateral** | | | | | | | |
| 10654 | Standard Deviation, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{RMSX\_400C}$ | — | — | +3 | LSB | 6 |

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| 10656 | Standard Deviation, Min. 50 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{RMSX\_400T}$ | — | — | +3 | LSB | 1 |
| **Noise: Z-Axis Sensor** | | | | | | | |
| **System Output Noise Peak (12 bit), Medium g Range = 50 g, Z-Axis** | | | | | | | |
| 10659 | Max. Deviation from Mean, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{PeakZ\_400C}$ | –12 | — | +12 | LSB | 6 |
| 10661 | Max. Deviation from Mean, Min. 50 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{PeakZ\_400T}$ | –12 | — | +12 | LSB | 1 |
| **System Output Noise Average (12 bit), Medium g Range = 50 g, Z-Axis** | | | | | | | |
| 10660 | Standard Deviation, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{RMSZ\_400C}$ | — | — | +3 | LSB | 6 |
| 10662 | Standard Deviation, Min. 50 values, Min. $f_{Samp}$ = 2 kHz, LPF = 400 Hz, 4-Pole * | $n_{RMSZ\_400T}$ | — | — | +3 | LSB | 1 |

The offset before offset cancellation scales with the user gain. The higher the gain (lower range), the higher the offset. Table 25. Medium g, SPI/DSI3 12-bit offset specification lists the adjusted offset specification limits for some SPI and DSI3 12-bit user gain settings.

**Table 25. Medium g, SPI/DSI3 12-bit offset specification**

| User range (g) | Offset (LSB, 12 bit) |
|---|---|
| 15.5 | ± 162 |
| 16 | ± 157 |
| 20 | ± 126 |
| 25 | ± 100 |
| 35 | ± 72 |
| 50 | ± 50 |
| 60 | ± 42 |
| 62 | ± 41 |
| 62.5 | ± 41 |
| 75 | ± 34 |
| 85.3 | ± 30 |
| 100 | ± 25 |
| 105 | ± 24 |
| 112.5 | ± 23 |
| 125 | ± 21 |
| 128 | ± 20 |
| 150 | ± 17 |

Table 26. Medium g, PSI5 10-bit offset specification lists the offset before offset cancellation limits for some PSI5 10-bit user gain settings.

**Table 26. Medium g, PSI5 10-bit offset specification**

| User range (g) | Offset (LSB, 10 bit) |
|---|---|
| 15 | ± 40 |
| 20 | ± 30 |
| 30 | ± 20 |
| 60 | ± 10 |
| 120 | ± 5 |

The signal noise scales with the user gain and with signal bandwidth. The higher the gain (lower range), the higher the noise, the wider the bandwidth, the higher the noise. Table 27. Lateral Medium g, SPI/DSI3 12-bit noise specification lists the adjusted specification limits for some user gain settings and low-pass filter selections.

*Note: Peak values indicate the maximum deviation from the mean.*

**Table 27. Lateral Medium g, SPI/DSI3 12-bit noise specification**

| User range (g) | LPF 400 Hz, 4p | | LPF 400 Hz, 3p | | LPF 180 Hz, 2p | | LPF 325 Hz, 3p | | LPF 1500 Hz, 4p | | LPF 800 Hz, 4p | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit |
| 15.5 | 39 | 10 | 40 | 10 | 28 | 7 | 36 | 9 | 75 | 19 | 55 | 14 |
| 25 | 24 | 6 | 25 | 7 | 18 | 5 | 23 | 6 | 47 | 12 | 34 | 9 |
| 50 | 12 | 3 | 13 | 4 | 9 | 3 | 12 | 3 | 24 | 6 | 17 | 5 |
| 62.5 | 10 | 3 | 10 | 3 | 7 | 2 | 9 | 3 | 19 | 5 | 14 | 4 |
| 100 | 6 | 2 | 7 | 2 | 5 | 2 | 6 | 2 | 12 | 3 | 9 | 3 |
| 125 | 5 | 2 | 5 | 2 | 4 | 1 | 5 | 2 | 10 | 3 | 7 | 2 |
| 150 | 4 | 1 | 5 | 2 | 3 | 1 | 4 | 1 | 8 | 2 | 6 | 2 |

**Table 28. Z-axis, Medium g, SPI/DSI3 12-bit noise specification**

| User range (g) | LPF 400 Hz, 4p | | LPF 400 Hz, 3p | | LPF 180 Hz, 2p | | LPF 325 Hz, 3p | | LPF 1500 Hz, 4p | | LPF 800 Hz, 4p | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit | Peak LSB 12 bit | RMS LSB 12 bit |
| 15.5 | 39 | 10 | 40 | 10 | 28 | 7 | 36 | 9 | 75 | 19 | 55 | 14 |
| 25 | 24 | 6 | 25 | 7 | 18 | 5 | 23 | 6 | 47 | 12 | 34 | 9 |
| 50 | 12 | 3 | 13 | 4 | 9 | 3 | 12 | 3 | 24 | 6 | 17 | 5 |
| 62.5 | 10 | 3 | 10 | 3 | 7 | 2 | 9 | 3 | 19 | 5 | 14 | 4 |
| 100 | 6 | 2 | 7 | 2 | 5 | 2 | 6 | 2 | 12 | 3 | 9 | 3 |
| 125 | 5 | 2 | 5 | 2 | 4 | 1 | 5 | 2 | 10 | 3 | 7 | 2 |
| 150 | 4 | 1 | 5 | 2 | 3 | 1 | 4 | 1 | 8 | 2 | 6 | 2 |

Table 29. Lateral Medium g, PSI5 10-bit noise specifications and Table 30. Z-axis, Medium g, PSI5 10-bit noise specification list the adjusted specification limits for some PSI5 10-bit user gain settings and low-pass filter selections.

**Table 29. Lateral Medium g, PSI5 10-bit noise specifications**

| User range (g) | LPF 400 Hz, 4p | | LPF 400 Hz, 3p | | LPF 800 Hz, 4p | |
|---|---|---|---|---|---|---|
| | Peak LSB 10 bit | RMS LSB 10 bit | Peak LSB 10 bit | RMS LSB 10 bit | Peak LSB 10 bit | RMS LSB 10 bit |
| 30, PSI5 | 7 | 1.7 | 7 | 1.8 | 10 | 2.4 |
| 60, PSI5 | 4 | 0.9 | 4 | 0.9 | 5 | 1.2 |
| 120, PSI5 | 2 | 0.5 | 2 | 0.5 | 3 | 0.6 |

**Table 30. Z-axis, Medium g, PSI5 10-bit noise specification**

| User range (g) | LPF 400 Hz, 4p | | LPF 400 Hz, 3p | | LPF 800 Hz, 4p | |
|---|---|---|---|---|---|---|
| | Peak LSB 10 bit | RMS LSB 10 bit | Peak LSB 10 bit | RMS LSB 10 bit | Peak LSB 10 bit | RMS LSB 10 bit |
| 30, PSI5 | 7 | 1.7 | 7 | 1.8 | 10 | 2.4 |
| 60, PSI5 | 4 | 0.9 | 4 | 0.9 | 5 | 1.2 |
| 120, PSI5 | 2 | 0.5 | 2 | 0.5 | 3 | 0.6 |

## 7.8 Electrical characteristics - inertial sensor signal chain: Low g

**Table 31. Electrical characteristics - inertial sensor signal chain: Low g**

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Sensitivity** | | | | | | | |
| **Total Sensitivity Error Including Linearity (From Trim Target, Output @ 0 Hz)** | | | | | | | |
| 10568 | Low g, Verified with a 20 g Range * | $SENS_{ERRL}$ | –5 | — | +5 | % | 1 |
| **Low g Standard Trim Range 12-bit Sensitivity Target** | | | | | | | |
| 44622 | ±20 g Range (± 2047 LSB, U_SNS_SHIFT = 0x0, U_SNS_MULT = 0x33) * | $SENS_{020L}$ | 97.3593 | 102.4835 | 107.6076 | LSB/g | 1 |
| **Offset** | | | | | | | |
| | 12 g Range, scales with user sensitivity scaling (400 mg) * | $OFF_{Low\_1}$ | –68 | — | +68 | LSB | 1 |
| 10583 | Digital Offset After Offset Cancellation, Lateral or Z-Axis, All Ranges, 12-Bit | $OFFCANC_{12Bit}$ | –1 | 0 | +1 | LSB | 6, 8, 9 |
| | Digital Offset After Offset Cancellation with rate limiter, Lateral or Z-Axis, All Ranges, 12-Bit | $OFFCANCRL_{12Bit}$ | –2 | 0 | +2 | LSB | 7, 8, 9 |
| **Digital Offset Error Due to Temperature (12-bit Z-Axis, 8 g, Scales with Range)** | | | | | | | |
| | Maximum Offset Variation over any 60 C Range (200 mg) | $OFF_{TCO}$ | — | — | 34 | LSB | 6 |
| **Continuous Offset Monitor Limit (U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00)** | | | | | | | |
| 10619 | 12 bit: Scales with user gain (~1.45 g) | $OFF_{MON}$ | –496 | — | +496 | LSB | 7, 8, 9 |
| **Sensor** | | | | | | | |
| **Range of Output (SPI, DSI3, All Ranges)** | | | | | | | |
| 10635 | Signed Sensor Data, 10-bit | $RANGE_{Signed\_10}$ | –511 | — | +511 | LSB | 7, 8, 9 |
| 10628 | Signed Sensor Data, 12-bit | $RANGE_{Signed\_12}$ | –2047 | — | +2047 | LSB | 7, 8, 9 |
| 10636 | Signed Error Code, 10-bit | $ERR_{Signed\_10}$ | — | –512 | — | LSB | 7, 8, 9 |
| 10637 | Signed Error Code, 12-bit | $ERR_{Signed\_12}$ | — | –2048 | — | LSB | 7, 8, 9 |
| **Range of Output (SPI, DSI3, All Ranges)** | | | | | | | |
| 10638 | Unsigned Sensor Data, 10-bit | $RANGE_{Unsigned\_10}$ | 1 | — | 1023 | LSB | 7, 8, 9 |
| 10639 | Unsigned Sensor Data, 12-bit | $RANGE_{Unsigned\_12}$ | 1 | — | 4095 | LSB | 7, 8, 9 |
| 10640 | Unsigned Error Code, 10-bit, 12-bit | $ERR_{Unsigned}$ | — | 0 | — | LSB | 7, 8, 9 |
| **Range of Output (PSI5, All Ranges)** | | | | | | | |
| 10634 | Signed Sensor Data, 10-bit | $RANGE_{Signed\_10}$ | –480 | — | +480 | LSB | 7, 8, 9 |
| **Cross-Axis Sensitivity, All Ranges** | | | | | | | |
| 10643 | X-axis to Z-Axis, Y-axis to Z-Axis | $V_{XZ}$, $V_{YZ}$ | –5 | — | +5 | % | 6 |
| **Non-Linearity (12-bit, All Ranges)** | | | | | | | |
| 10669 | Differential Non-Linearity (No Missing Codes) * | DNL | — | — | +1.0 | LSB | 7 |
| 10670 | End Point Non-Linearity (Least Squares BFSL) * | INL | — | — | +20.0 | LSB | 6 |
| **Supply Coupling ($C_{BUF}$ = 1 µf, 12-bit, DSI3, PSI5, All Ranges)** | | | | | | | |
| 10663 | 1 kHz ≤ $f_n$ ≤ 10 kHz, BUS_I = 8.0 V ± 2.0 V (Represents PSI5 Sync Pulse) | $PSC_{PSI5}$ | — | — | 1 | LSB | 6 |
| 10682 | 10 kHz ≤ $f_n$ ≤ 100 kHz, BUS_I = 6.0 V ± 1.0 V (Represents DSI3 BRC) | $PSC_{DSI3C}$ | — | — | 1 | LSB | 6 |
| 10681 | 100 kHz ≤ $f_n$ ≤ 1 MHz, BUS_I = 6.0 V ± 0.5 V (Represents DSI3/PSI5 Response) | $PSC_{DSI3R}$ | — | — | 1 | LSB | 6 |
| 10680 | 1 MHz ≤ $f_n$ ≤ 20 MHz, BUS_I = 6.0 V ± 0.1 V (Represents Response Harmonics) | $PSC_{SATH}$ | — | — | 1 | LSB | 6 |
| **Supply Coupling ($C_{BUF}$ = 0.1 µf, 12-bit, SPI, All Ranges)** | | | | | | | |
| 10675 | 1 kHz ≤ $f_n$ ≤ 20 MHz, $V_{BUF}$ =5.0 V ± 0.1 V | $PSC_{SPI5}$ | — | — | 2 | LSB | 6 |
| 10683 | 1 kHz ≤ $f_n$ ≤ 20 MHz, $V_{BUF}$ =3.3 V ± 0.1 V | $PSC_{SPI3}$ | — | — | 2 | LSB | 6 |
| **Noise** | | | | | | | |
| **System Output Noise Peak (12-bit, Low g Range = 8 g, Z-Axis)** | | | | | | | |
| 36803 | Max. Deviation from Mean, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 250 Hz, 3-Pole * | $n_{PeakZ\_250C}$ | –12 | — | +12 | LSB | 6 |
| | Max. Deviation from Mean, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 250 Hz, 3-Pole * | $n_{PeakZ\_250T}$ | –12 | — | +12 | LSB | 1 |
| **System Output Noise Average (12-bit, Low g Range = 8 g, Z-Axis)** | | | | | | | |

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| 36804 | Standard Deviation, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 250 Hz, 3-Pole * | $n_{RMSZ\_250C}$ | — | — | +4.0 | LSB | 6 |
| | Standard Deviation, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 250 Hz, 3-Pole * | $n_{RMSZ\_250T}$ | — | — | +4.0 | LSB | 1 |
| **System Output Noise Peak (12 bit, Low g Range = 3.5 g, Z-Axis)** | | | | | | | |
| 10657 | Max .Deviation from Mean, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 50 Hz, 2-Pole * | $n_{PeakZ\_50C}$ | –9 | — | +9 | LSB | 6 |
| | Max.Deviation from Mean, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 50 Hz, 2-Pole * | $n_{PeakZ\_50T}$ | –9 | — | +9 | LSB | 1 |
| **System Output Noise Average (12 bit, Low g Range = 3.5 g, Z-Axis)** | | | | | | | |
| 10658 | Standard Deviation, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF = 50 Hz, 2-Pole * | $n_{RMSZ\_50C}$ | — | — | +3.0 | LSB | 6 |
| | Standard Deviation, Min. 2000 values, Min. $f_{Samp}$ = 2 kHz, LPF= 50 Hz, 2-Pole * | $n_{RMSZ\_50T}$ | — | — | +3.0 | LSB | 1 |

## 7.9 Electrical characteristics - inertial sensor self-test

**Table 32. Electrical characteristics - inertial sensor self-test**

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Med g Lateral Self-test, 62 g, U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00** | | | $\Delta ST_{MIN}$ | $\Delta ST_{NOM}$ | $\Delta ST_{MAX}$ | | |
| | Low self-test, 14.80 g, 10-bit Signed Delta from Offset | $ST_{ML\_62X\_10}$ | 54 | 121 | 188 | LSB | 7 |
| | High self-test, 44.50 g, 10-bit Signed Delta from Offset | $ST_{MH\_62X\_10}$ | 220 | 367 | 511 | LSB | 7 |
| | Low self-test, 14.80 g, 12-bit Signed Delta from Offset | $ST_{ML\_62X\_12}$ | 218 | 485 | 752 | LSB | 7 |
| | High self-test, 44.50 g, 12-bit Signed Delta from Offset | $ST_{MH\_62X\_12}$ | 881 | 1470 | 2047 | LSB | 7 |
| | Low self-test, 14.80 g, 16-bit SPI/PSI5 Extended Signed Delta from Offset | $ST_{ML\_62X\_16}$ | 3456 | 7744 | 12032 | LSB | 7 |
| | High self-test, 44.50 g, 16-bit SPI/PSI5 Extended Signed Delta from Offset | $ST_{MH\_62X\_16}$ | 14080 | 23488 | 32767 | LSB | 7 |
| 10687 | Low self-test, 14.80 g, 16-bit Signed SNSDATAx Register Delta from Offset * | $ST_{ML\_62X\_13}$ | 436 | 970 | 1504 | LSB | 1 |
| 10688 | High self-test, 44.50 g, 16-bit Signed SNSDATAx Register Delta from Offset * | $ST_{MH\_62X\_13}$ | 1763 | 2939 | 4115 | LSB | 1 |
| **Med g Z-Axis Self-test, 62 g, U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00** | | | $\Delta ST_{MIN}$ | $\Delta ST_{NOM}$ | $\Delta ST_{MAX}$ | | |
| | Low self-test, 10.28 g, 10-bit Signed Delta from Offset | $ST_{ML\_62Z\_10}$ | 34 | 85 | 135 | LSB | 7 |
| | High self-test, 27.47 g, 10-bit Signed Delta from Offset | $ST_{MH\_62Z\_10}$ | 136 | 227 | 318 | LSB | 7 |
| | Low self-test, 10.28 g, 12-bit Signed Delta from Offset | $ST_{ML\_62Z\_12}$ | 139 | 340 | 540 | LSB | 7 |
| | High self-test, 27.47 g, 12-bit Signed Delta from Offset | $ST_{MH\_62Z\_12}$ | 544 | 907 | 1270 | LSB | 7 |
| | Low self-test, 10.28 g, 16-bit SPI/PSI5 Extended Signed Delta from Offset | $ST_{ML\_62Z\_16}$ | 2176 | 5432 | 8640 | LSB | 7 |
| | High self-test, 27.47 g, 16-bit SPI/PSI5 Extended Signed Delta from Offset | $ST_{MH\_62Z\_16}$ | 8708 | 14514 | 20320 | LSB | 7 |
| 30134 | Low self-test, 10.28 g, 16-bit Signed SNSDATAx Register Delta from Offset * | $ST_{ML\_62Z\_13}$ | 278 | 679 | 1080 | LSB | 1 |
| 30135 | High self-test, 27.47 g, 16-bit Signed SNSDATAx Register Delta from Offset * | $ST_{MH\_62Z\_13}$ | 1088 | 1814 | 2540 | LSB | 1 |
| **High g Lateral Self-test, 187 g, U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00** | | | $\Delta ST_{MIN}$ | $\Delta ST_{NOM}$ | $\Delta ST_{MAX}$ | | |
| | Low self-test, 18.33 g, 10-bit Signed Delta from Offset | $ST_{HL\_187X\_10}$ | 24 | 55 | 86 | LSB | 7 |
| | High self-test, 55.00 g, 10-bit Signed Delta from Offset | $ST_{HH\_187X\_10}$ | 90 | 150 | 212 | LSB | 7 |
| | Low self-test, 18.33 g, 12-bit Signed Delta from Offset | $ST_{HL\_187X\_12}$ | 99 | 220 | 341 | LSB | 7 |
| | High self-test, 55.00 g, 12-bit Signed Delta from Offset | $ST_{HH\_187X\_12}$ | 361 | 603 | 845 | LSB | 7 |
| | Low self-test, 18.33 g, 16-bit SPI/PSI5 Extended Signed Delta from Offset | $ST_{HL\_187X\_16}$ | 1536 | 3520 | 5504 | LSB | 7 |
| | High self-test, 55.00 g, 16-bit SPI/PSI5 Extended Signed Delta from Offset | $ST_{HH\_187X\_16}$ | 5760 | 9600 | 13568 | LSB | 7 |
| 10685 | Low self-test, 18.33 g, 16-bit Signed SNSDATAx Register Delta from Offset * | $ST_{HL\_187X\_13}$ | 198 | 440 | 682 | LSB | 1 |
| 10686 | High self-test, 55.00 g, 16-bit Signed SNSDATAx Register Delta from Offset * | $ST_{HH\_187X\_13}$ | 723 | 1206 | 1689 | LSB | 1 |
| **High g Z-Axis Self-test, 187 g, U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00** | | | $\Delta ST_{MIN}$ | $\Delta ST_{NOM}$ | $\Delta ST_{MAX}$ | | |
| | Low self-test, 27.63 g, 10-bit Signed Delta from Offset | $ST_{HL\_187Z\_10}$ | 31 | 76 | 120 | LSB | 7 |
| | High self-test, 75.04 g, 10-bit Signed Delta from Offset | $ST_{HH\_187Z\_10}$ | 123 | 205 | 288 | LSB | 7 |
| | Low self-test, 27.63 g, 12-bit Signed Delta from Offset | $ST_{HL\_187Z\_12}$ | 125 | 303 | 480 | LSB | 7 |
| | High self-test, 75.04 g, 12-bit Signed Delta from Offset | $ST_{HH\_187Z\_12}$ | 492 | 821 | 1150 | LSB | 7 |
| | Low self-test, 27.63 g, 16-bit SPI/PSI5 Extended Signed Delta from Offset | $ST_{HL\_187Z\_16}$ | 1984 | 4840 | 7680 | LSB | 7 |
| | High self-test, 75.04 g, 16-bit SPI/PSI5 Extended Signed Delta from Offset | $ST_{HH\_187Z\_16}$ | 7885 | 13143 | 18400 | LSB | 7 |
| 30136 | Low self-test, 27.63 g, 16-bit Signed SNSDATAx Register Delta from Offset * | $ST_{HL\_187Z\_13}$ | 250 | 605 | 960 | LSB | 1 |
| 30137 | High self-test, 75.04 g, 16-bit Signed SNSDATAx Register Delta from Offset * | $ST_{HH\_187Z\_13}$ | 985 | 1643 | 2300 | LSB | 1 |
| **Low g Z-Axis Self-Test, 12 g, U_SNS_SHIFT = 0x0, U_SNS_MULT = 0xFF** | | | | | | | |
| | Low self-test, 2.820 g, 10-bit Signed Delta from Positive to Negative self-test | $ST_{LL\_12Z\_10}$ | 144 | 240 | 338 | LSB | 7 |
| | High self-test, 7.830 g, 10-bit Signed Delta from Offset | $ST_{LH\_12Z\_10}$ | 200 | 334 | 468 | LSB | 7 |
| | Low self-test, 2.820 g, 12-bit Signed Delta from Positive to Negative self-test | $ST_{LL\_12Z\_12}$ | 578 | 964 | 1350 | LSB | 7 |
| | High self-test, 7.830 g, 12-bit Signed Delta from Offset | $ST_{LH\_12Z\_12}$ | 801 | 1336 | 1871 | LSB | 7 |
| | Low self-test, 2.820 g, 16-bit SPI/PSI5 Extended Signed Delta from Positive to Negative self-test | $ST_{LL\_12Z\_16}$ | 9248 | 15414 | 21580 | LSB | 7 |

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| | High self-test, 7.830 g, 16-bit SPI/PSI5 Extended Signed Delta from Offset | $ST_{LH\_12Z\_16}$ | 12824 | 21375 | 29925 | LSB | 7 |
| 30312 | Low self-test, 2.820 g, 16-bit Signed SNSDATAx Register Delta from Positive to Negative self-test * | $ST_{LL\_12Z\_13}$ | 1156 | 1926 | 2698 | LSB | 1 |
| 30133 | High self-test, 7.830 g, 16-bit Signed SNSDATAx Register Delta from Offset * | $ST_{LH\_12Z\_13}$ | 1603 | 2672 | 3741 | LSB | 1 |
| **High self-test Accuracy: Δ from Stored Value, including Sensitivity Error** | | | | | | | |
| **(12-bit, High/Medium g Lateral or Z-axis, All Ranges)** | | | | | | | |
| 10678 | 25 °C, Post Pre-conditioning * | ΔSTHACC_25P | –2 | — | +2 | % | 6 |
| 10690 | –40 °C ≤ $T_A$ ≤ 125 °C * | ΔSTHACC_T | –10 | — | +10 | % | 1 |
| **High self-test Accuracy: Δ from Stored Value, including Sensitivity Error** | | | | | | | |
| **(12-bit, Low g Z-axis, All Ranges)** | | | | | | | |
| | 25 °C, Post Pre-conditioning, +1 g field Z-Axis direction * | ΔSTHACCL_25P | –2 | — | +2 | % | 6 |
| | –40 °C ≤ $T_A$ ≤ 125 °C * | ΔSTHACCL_T | –10 | — | +10 | % | 1 |
| **Self-test Delta Offset: Δ Offset from Pre-Self-test to Post Self-test** | | | | | | | |
| **(12-bit, Lateral or Z-Axis, All Ranges)** | | | | | | | |
| 10692 | 25 °C | ΔSTOFF_25 | –2 | — | +2 | LSB | 1 |
| 10692 | –40 °C ≤ $T_A$ ≤ 125 °C | ΔSTOFF_T | –4 | — | +4 | LSB | 1 |
| **Digital Self-test Before Offset Cancellation** | | | | | | | |
| 44629 | Digital Self-test 0xC, 16-bit Signed SNSDATAx Register Value | $DST_{C0}$ | E77F | E780 | E781 | HEX | 7 |
| 44630 | Digital Self-test 0xD, 16-bit Signed SNSDATAx Register Value | $DST_{D0}$ | 0FA3 | 0FA4 | 0FA5 | HEX | 7 |
| 44631 | Digital Self-test 0xE, 16-bit Signed SNSDATAx Register Value | $DST_{E0}$ | EFA2 | EFA3 | EFA4 | HEX | 7 |
| 44632 | Digital Self-test 0xF, 16-bit Signed SNSDATAx Register Value | $DST_{F0}$ | 07B7 | 07B8 | 07B9 | HEX | 7 |

## 7.10 Electrical characteristics - lateral inertial sensor overload

**Table 33. Electrical characteristics - lateral inertial sensor overload**

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Acceleration Range, Lateral Transducer** | | | | | | | |
| 10694 | Medium g | $g_{g\text{-}cell\_ClipMedX}$ | ± 500 | — | — | g | 7 |
| 10693 | High g | $g_{g\text{-}cell\_ClipHiX}$ | ± 2000 | — | — | g | 7 |
| 21074 | Digital Clipping Limit (Medium g Lateral, must clip before transducer and ADC) | $g_{Dig\_ClipMedXHi}$ | ± 400 | — | — | g | 7 |
| 21082 | Digital Clipping Limit (High g Lateral, must clip before transducer and ADC) | $g_{Dig\_ClipHiXHi}$ | ± 1500 | — | — | g | 7 |

## 7.11 Electrical characteristics - Z-axis inertial sensor overload

**Table 34. Electrical characteristics - Z-axis inertial sensor overload**

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Acceleration Range, Z-Axis Transducer** | | | | | | | |
| 10697 | Low g | $g_{g\text{-}cell\_ClipLowZ}$ | ± 80 | — | — | g | 7 |
| 10698 | Medium g | $g_{g\text{-}cell\_ClipMedZ}$ | ± 500 | — | — | g | 7 |
| 10699 | High g | $g_{g\text{-}cell\_ClipHiZ}$ | ± 2000 | — | — | g | 7 |
| 10700 | Digital Clipping Limit (Z-Axis) | $g_{Dig\_ClipLoZ}$ | ± 45 | — | — | g | 7 |
| 21105 | Digital Clipping Limit (Medium g Z-Axis, must clip before transducer and ADC) | $g_{Dig\_ClipMedZHi}$ | ± 400 | — | — | g | 7 |
| 21113 | Digital Clipping Limit (High g Z-Axis, must clip before transducer and ADC) | $g_{Dig\_ClipHiZHi}$ | ± 1500 | — | — | g | 7 |

## 7.12 Dynamic electrical characteristics - DSI3

**Table 35. Dynamic electrical characteristics - DSI3**

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Command Reception (General)** | | | | | | | |
| 10709 | $V_{HIGH}$ low-pass filter time constant (Section 9.1.1: Command receiver) | $t_{VHIGH\_RC}$ | 60 | 120 | 180 | µs | 7, 9 |
| 10722 | $V_{HIGH}$ Detection Analog Delay (Section 9.1.1: Command receiver) | $t_{VHIGH\_Delay}$ | — | — | 600 | ns | 7, 9 |
| 10721 | Command Valid time (Section 9.1.1: Command receiver) | $t_{Cmd\_Valid}$ | — | 2 | — | µs | 7, 9 |
| **Response Transmission (General, Slew Control Enabled, Section 9.3.3: DSI3 command and response mode timing)** | | | | | | | |
| 10710 | Response Slew Time: 2.0 mA to 10.0 mA, 10.0 mA to 2.0 mA | $t_{SLEW1\_RESP}$ | 350 | 400 | 500 | ns | 1, 7, 9 |
| 10726 | Response Slew Time: 4.0 mA to 20.0 mA, 20.0 mA to 4.0 mA | $t_{SLEW2\_RESP}$ | 350 | 400 | 500 | ns | 1, 7, 9 |
| 10725 | $t_{SLEW1\_RESP} - t_{SLEW2\_RESP}$ | $\Delta t_{SLEW}$ | –100 | — | 100 | ns | 7, 9 |
| 10724 | $t_{SLEW1\_RESP\_Rise} - t_{SLEW2\_RESP\_Fall}$ | $\Delta t_{SLEW\_rf}$ | –250 | — | 250 | ns | 7, 9 |
| 10723 | Response Current Activation Time: Current Activated to 50 % | $t_{ACT\_RESP}$ | 200 | — | 400 | ns | 3, 7, 9 |
| **Response Transmission (General, Slew Control Disabled, Section 9.3.3: DSI3 command and response mode timing)** | | | | | | | |
| 10727 | Response Slew Time: 2.0 mA to 10.0 mA, 10.0 mA to 2.0 mA | $t_{nSLEW1\_RESP}$ | — | — | 300 | ns | 7, 9 |
| 10728 | Response Slew Time: 4.0 mA to 20.0 mA, 20.0 mA to 4.0 mA | $t_{nSLEW2\_RESP}$ | — | — | 300 | ns | 7, 9 |
| 10729 | $t_{SLEW1\_RESP} - t_{SLEW2\_RESP}$ | $\Delta t_{nSLEW}$ | –300 | — | 300 | ns | 7, 9 |
| 10730 | $t_{SLEW1\_RESP\_Rise} - t_{SLEW2\_RESP\_Fall}$ | $\Delta t_{nSLEW\_rf}$ | –300 | — | 300 | ns | 7, 9 |
| 10731 | Response Current Activation Time: Current Activated to 50 % | $t_{nACT\_RESP}$ | — | — | 300 | ns | 7, 9 |
| **Command Reception (Discovery Mode)** | | | | | | | |
| 10719 | Command Start Time (Section 9.2: Address assignment ) | $t_{START\_DISC}$ | $t_{POR\_DSI}$ | — | 13.5 | ms | 7, 8, 9 |
| 10734 | Command Bit Time (Section 9.2: Address assignment ) | $t_{DISC\_BitTime}$ | 14 | 16 | 18 | µs | 7, 8, 9 |
| 10733 | Command Transmission Period (Section 9.2: Address assignment ) | $t_{PER\_DISC}$ | 125 | — | — | µs | 7, 8, 9 |
| 10732 | Command Blocking Time, Discovery Mode (Section 9.1.1: Command receiver) | $t_{CmdBlock\_DISC}$ | — | 80 | — | µs | 7, 8, 9 |
| **Response Transmission (Discovery Mode)** | | | | | | | |
| 30078 | Idle Current Sample Delay (Section 9.2: Address assignment ) | $t_{DISC\_DLY}$ | — | 48 | — | µs | 7, 8, 9 |
| 30079 | Idle Current Sample Time (Section 9.2: Address assignment ) | $t_{DISC\_ICCQ\_SAMP}$ | — | 15 | — | µs | 7, 8, 9 |
| 10718 | Response Start Delay (Section 9.2: Address assignment ) | $t_{START\_DISC\_RSP}$ | — | 64 | — | µs | 7, 8, 9 |
| 10738 | Response Ramp Time (Section 9.2: Address assignment ) | $t_{DISC\_Ramp\_RSP}$ | — | 16 | — | µs | 7, 8, 9 |
| 10737 | Response Ramp Rate (Section 9.2: Address assignment ) | $I_{DISC\_Ramp}$ | — | 1.5 | — | mA/µs | 7, 8, 9 |
| 10736 | Response Idle Time (Section 9.2: Address assignment ) | $t_{DISC\_Idle\_RSP}$ | — | 16 | — | µs | 7, 8, 9 |
| 10735 | Response Peak Current (Section 9.2: Address assignment ) | $I_{DISC\_Peak}$ | — | $2*I_{RESP}$ | — | mA | 7, 8, 9 |
| 30081 | Response Current Sample Delay (Section 9.2: Address assignment ) | $t_{IDISC\_Samp\_Dly}$ | — | 65 | — | µs | 7, 8, 9 |
| 30080 | Response Current Sample Time (Section 9.2: Address assignment ) | $t_{IDISC\_Samp}$ | — | 31 | — | µs | 7, 8, 9 |
| **Command Reception (Command and Response Mode)** | | | | | | | |
| 10717 | Command Bit Time (Section 9.3: DSI3 command and response mode) | $t_{Cmd\_BitTime}$ | — | 8 | — | µs | 7, 8, 9 |
| 10741 | Command Transmission Period (Section 9.3: DSI3 command and response mode) | $t_{PER\_CRM}$ | 475 | — | — | µs | 7, 8, 9 |
| 10740 | Command Blocking Time, CRM (Section 9.1.1: Command receiver) | $t_{CmdBlock\_CRM}$ | — | 455 | — | µs | 7, 8, 9 |
| 10739 | Command Blocking Start Time, CRM (Section 9.1.1: Command receiver) | $t_{CmdBlock\_ST\_CRM}$ | — | 290 | — | µs | 7, 8, 9 |
| **Response Transmission (Command and Response Mode)** | | | | | | | |
| 10716 | Response Chip Time | $t_{CHIP\_CRM}$ | — | 5 | — | µs | 7, 8, 9 |
| 10742 | Response Start Time (Section 9.3: DSI3 command and response mode) | $t_{START\_CRM}$ | — | 295 | — | µs | 7, 8, 9 |
| **Command Reception (Periodic Data Collection Mode)** | | | | | | | |
| 10715 | Command Bit Time (Section 9.4: DSI3 periodic data collection mode and background diagnostic mode) | $t_{Cmd\_BitTime}$ | — | 8 | — | µs | 7, 8, 9 |
| 10743 | Command Transmission Period (Section 9.4: DSI3 periodic data collection mode and background diagnostic mode) | $t_{PER\_PDCM}$ | 50 | — | — | µs | 7, 8, 9 |

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Response Transmission (Periodic Data Collection Mode)** | | | | | | | |
| 10714 | Response Chip Time Typical (Section 8.2.15.4: Chip time (CHIPTIME)) | $t_{CHIP\_PDCM}$ | 1.0 | — | 5.0 | µs | 7, 8, 9 |
| 10746 | Min Programmed Start Time: PDCM_RSPSTx < 0x0015 | $t_{START\_PDCM\_Min}$ | — | 20 | — | µs | 7, 8, 9 |
| 10745 | Min Programmed Start Time: BDM Enabled | $t_{START\_PDCMBDMMin}$ | — | 51 | — | µs | 7, 8, 9 |
| 10744 | Max Programmed Start Time: PDCM_RSPSTx = 0x1FFF | $t_{START\_PDCM\_Max}$ | — | 8191 | — | µs | 7, 8, 9 |
| **Response Transmission (Background Diagnostic Mode)** | | | | | | | |
| 49314 | Response Chip Time | $t_{CHIP\_BDM}$ | — | $t_{CHIP\_PDCM}$ | — | µs | 7, 8, 9 |
| 10747 | Response Start Time (Section 9.4: DSI3 periodic data collection mode and background diagnostic mode) | $t_{START\_BDM}$ | — | 20 | — | µs | 7, 8, 9 |
| **Data Latency** | | | | | | | |
| 10712 | DSI Data Latency | $t_{LAT\_DSI}$ | 0 | — | 2.00 | µs | 7, 8 |
| **OTP Program Timing** | | | | | | | |
| 10711 | Time to program an OTP User Region | $t_{OTP\_WRITE\_MAX}$ | — | — | 10 | ms | 7, 8, 9 |

## 7.13 Dynamic electrical characteristics - PSI5

**Table 36. Dynamic electrical characteristics - PSI5**

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Initialization Timing** | | | | | | | |
| 10748 | Phase 1 | $t_{PSI5\_INIT1}$ | — | 133 | — | ms | 7, 8, 9 |
| 10758 | Phase 2 (Synchronous Mode, k = 4, $t_{S-S}$ = 500 µs) | $t_{PSI5\_INIT2\_10s}$ | — | 256 * $t_{S-S}$ | — | s | 7, 8, 9 |
| 10757 | Phase 2 (Asynchronous Mode, k = 8) | $t_{PSI5\_INIT2\_10a}$ | — | 512 * $t_{ASYNC}$ | — | s | 7, 8, 9 |
| 10756 | Phase 3 (Synchronous Mode, $t_{S-S}$ = 500 µs) | $t_{PSI5\_INIT3\_10s}$ | — | 2 * $t_{S-S}$ | — | s | 7, 8, 9 |
| 10755 | Phase 3 (Asynchronous Mode) | $t_{PSI5\_INIT3\_10a}$ | — | 2 * $t_{ASYNC}$ | — | s | 7, 8, 9 |
| 10754 | PSI5 Self-test Start Time | $t_{PSI5ST\_START}$ | — | 30 | — | ms | 7, 8 |
| 10753 | PSI5 Self-test Time, including Post OC Startup Offset | $t_{ST}$ | — | 223 | — | ms | 7, 8 |
| 41756 | Programming Mode Entry Window | $t_{PME}$ | — | 127 | — | ms | 7, 8, 9 |
| **Synchronization Pulse** | | | | | | | |
| 10759 | Reset to first sync pulse (Program Mode Entry) | $t_{RS\_PM}$ | 6 | — | — | ms | 7, 8, 9 |
| 10779 | Reset to first sync pulse (Normal Mode) | $t_{RS}$ | $t_{PSI5\_INIT1}$ | — | — | s | 7, 8, 9 |
| 10778 | Sync Pulse Period | $t_{S-S}$ | 175 | — | — | µs | 7, 8, 9 |
| 10777 | Sync Pulse Width | $t_{SYNC}$ | 9 | — | — | µs | 7, 8, 9 |
| 10776 | Sync Pulse Reference LPF time constant | $t_{SYNC\_LPF}$ | 120 | 280 | — | µs | 7, 9 |
| 10775 | Sync Pulse Reference Discharge Start Time | $t_{SYNC\_LPF\_RST\_ST}$ | — | 9.0 | — | µs | 7, 9 |
| 10774 | Sync Pulse Reference Discharge Activation Time | $t_{SYNC\_LPF\_RST}$ | — | 154 | — | µs | 7, 9 |
| 10773 | Sync Pulse Detection Disable Time (PDCM_CMD_B = 0) | $t_{SYNC\_OFF\_500}$ | — | 450 | — | µs | 7, 8, 9 |
| 10772 | Analog Delay of Sync Pulse Detection | $t_{A\_SYNC\_DLY}$ | 50 | — | 600 | ns | 7, 9 |
| 10771 | Sync Pulse Pulldown Function Delay Time | $t_{PD\_DLY}$ | — | 9.0 | — | µs | 7, 9 |
| 10770 | Sync Pulse Pulldown Function Activate Time | $t_{PD\_ON}$ | — | 16 | — | µs | 7, 8 |
| 10769 | Sync Pulse Detection Jitter | $t_{SYNC\_JIT}$ | 0 | — | 0.5 | µs | 7, 8 |
| **Data Transmission Bit Time** | | | | | | | |
| 10768 | PSI5 Standard Bit Rate | $t_{BIT\_Standard}$ | — | 8.00 | — | µs | 7, 8, 9 |
| 10767 | PSI5 High Bit Rate | $t_{BIT\_HI}$ | — | 5.30 | — | µs | 7, 8, 9 |
| **Response Current Transmission (No external Components)** | | | | | | | |
| 10766 | Response Slew Time: 20 % to 80 % of $I_{R\_PSI5}$ | $t_{SLEW1\_RESP}$ | 350 | 400 | 500 | ns | 1, 7, 9 |
| 10765 | Position of bit transition (All except 5.3 µs) | $t_{Bittrans\_LowBaud}$ | 49 | 50 | 51 | % | 8, 9 |
| 10780 | Position of bit transition (5.3 us) | $t_{Bittrans\_HighBaud}$ | 49 | □ | 51 | % | 8, 9 |
| **Time Slots** | | | | | | | |
| 10764 | Asynchronous Response Time | $t_{ASYNC}$ | — | 228 | — | µs | 7, 8, 9 |
| 10763 | Min Programmed Time Slot: PDCM_RSPSTx < 0x0014 | $t_{TIMESLOTx\_MIN}$ | — | 20 | — | µs | 7, 8, 9 |
| 10790 | Max Programmed Time Slot: PDCM_RSPSTx = 0x1FFF | $t_{TIMESLOTx\_MAX}$ | — | 8191 | — | µs | 7, 8, 9 |
| 10789 | Default Time Slot (PDCM_RSPSTx = 0x0000) | $t_{TIMESLOT\_DFLT}$ | — | 20 | — | µs | 7, 8, 9 |
| 10788 | Time Slot Resolution | $t_{TIMESLOTx\_RES}$ | — | 1.0 | — | µs/LSB | 7, 8, 9 |
| 10787 | Sync pulse to Daisy Chain Default Time Slot 0 | $t_{TIMESLOT\_DC0}$ | — | 46.5 | — | µs | 7, 8, 9 |
| 10786 | Sync pulse to Daisy Chain Default Time Slot 1 (Low) | $t_{TIMESLOT\_DC1\_L}$ | — | 192 | — | µs | 7, 8, 9 |
| 10785 | Sync pulse to Daisy Chain Default Time Slot 2 (Low) | $t_{TIMESLOT\_DC2\_L}$ | — | 350 | — | µs | 7, 8, 9 |
| 10784 | Sync pulse to Daisy Chain Default Time Slot 1 (High) | $t_{TIMESLOT\_DC1\_H}$ | — | 150 | — | µs | 7, 8, 9 |
| 10783 | Sync pulse to Daisy Chain Default Time Slot 2 (High) | $t_{TIMESLOT\_DC2\_H}$ | — | 260 | — | µs | 7, 8, 9 |
| 10782 | Sync pulse to Daisy Chain Default Time Slot 3 (High) | $t_{TIMESLOT\_DC3\_H}$ | — | 380 | — | µs | 7, 8, 9 |
| 10781 | Sync pulse to Daisy Chain Programming Time Slot | $t_{TIMESLOT\_DCP}$ | — | 46.5 | — | µs | 7, 8, 9 |
| **Data Latency** | | | | | | | |

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| 10762 | PSI5 Data Latency | $t_{LAT\_PSI5}$ | 0 | — | 1.00 | µs | 7, 8 |
| **Bus Switch Output Activation Time (C = 50 pF)** | | | | | | | |
| 10761 | From last bit of "SetAdr" Response to 80 % of $V_{BUS\_SW\_OH}$ | $t_{BUS\_SW}$ | □ | □ | 300 | µs | 7 |
| **PSI5 Programming Mode** | | | | | | | |
| 10760 | PSI5 Programming Mode Sync Pulse Period<br>The user must provide a sync pulse period within this range to guarantee Programming Mode communications | $t_{S\text{-}S\_PM}$ | 245 | 250 | 255 | µs | 7, 8, 9 |
| | PSI5 Programming Mode Command Blanking Time | $t_{SYNC\_OFF\_250}$ | — | 200 | — | µs | 7, 8, 9 |
| **Daisy Chain Mode** | | | | | | | |
| 39810 | Daisy Chain Mode Sync Pulse Period<br>The user must provide a sync pulse period within this range to guarantee communications | $t_{S\text{-}S\_DC}$ | 490 | 500 | 510 | µs | 7, 8, 9 |
| **OTP Program Timing** | | | | | | | |
| 10793 | Time to program one OTP User Region | $t_{OTP\_WRITE\_MAX}$ | — | — | 10 | ms | 7, 8, 9 |

## 7.14 Dynamic electrical characteristics - SPI

**Table 37. Dynamic electrical characteristics - SPI**

$V_{CC\_BUF\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{CC\_BUF\_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Serial Interface Timing (See Figure 97. SPI timing diagram, $C_{MISO} \leq 80$ pF, $R_{MISO} \geq 10$ kΩ)** | | | | | | | |
| 10794 | Clock (SCLK) period (10 % of $V_{CC}$ to 10 % of $V_{CC}$) | $t_{SCLK}$ | 88 | — | — | ns | 6 |
| 10801 | Clock (SCLK) high time (90 % of $V_{CC}$ to 90 % of $V_{CC}$) | $t_{SCLKH}$ | 30 | — | — | ns | 6 |
| 10802 | Clock (SCLK) low time (10 % of $V_{CC}$ to 10 % of $V_{CC}$) | $t_{SCLKL}$ | 30 | — | — | ns | 6 |
| 10800 | Clock (SCLK) risetime (10 % of $V_{CC}$ to 90 % of $V_{CC}$) | $t_{SCLKR}$ | — | 10 | 25 | ns | 7 |
| 10803 | Clock (SCLK) fall time (90 % of $V_{CC}$ to 10 % of $V_{CC}$) | $t_{SCLKF}$ | — | 10 | 25 | ns | 7 |
| 10799 | SS_B asserted to SCLK high (SS_B = 10 % of $V_{CC}$ to SCLK = 10 % of $V_{CC}$) | $t_{LEAD}$ | 50 | — | — | ns | 6 |
| 10798 | SS_B asserted to MISO valid (SS_B = 10 % of $V_{CC}$ to MISO = 10/90 % of $V_{CC}$) | $t_{ACCESS}$ | — | — | 50 | ns | 6 |
| 10797 | Data setup time (MOSI = 10/90 % of $V_{CC}$ to SCLK = 10 % of $V_{CC}$) | $t_{SETUP}$ | 20 | — | — | ns | 6 |
| 10796 | MOSI Data hold time (SCLK = 90 % of $V_{CC}$ to MOSI = 10/90 % of $V_{CC}$) | $t_{HOLD\_IN}$ | 10 | — | — | ns | 6 |
| 10804 | MISO Data hold time (SCLK = 90 % of $V_{CC}$ to MISO = 10/90 % of $V_{CC}$) | $t_{HOLD\_OUT}$ | 0 | — | — | ns | 6 |
| 10795 | SCLK low to data valid (SCLK = 10 % of $V_{CC}$ to MISO = 10/90 % of $V_{CC}$) | $t_{VALID}$ | — | — | 30 | ns | 6 |
| 10807 | SCLK low to SS_B high (SCLK = 10 % of $V_{CC}$ to SS_B = 90 % of $V_{CC}$) | $t_{LAG}$ | 60 | — | — | ns | 6 |
| 10806 | SS_B high to MISO disable (SS_B = 90 % of $V_{CC}$ to MISO = High Z) | $t_{DISABLE}$ | — | — | 60 | ns | 6 |
| 10808 | SCLK low to SS_B low (SCLK = 10 % of $V_{CC}$ to SS_B = 90 % of $V_{CC}$) | $t_{CLKSS}$ | 50 | — | — | ns | 6 |
| 10815 | SS_B high to SCLK high (SS_B = 90 % of $V_{CC}$ to SCLK = 90 % of $V_{CC}$) | $t_{SSCLK}$ | 50 | — | — | ns | 7 |
| 10818 | SPI Data Latency | $t_{LAT\_SPI}$ | — | — | 1 | µs | 7, 8 |
| **SS_B high to SS_B low (SS_B = 90 % of $V_{CC}$ to SS_B = 90 % of $V_{CC}$)** | | | | | | | |
| 10805 | Following Sensor Data Request Commands | $t_{SSN\_SENSE}$ | 500 | — | — | ns | 6 |
| 10813 | Following Register Reads/Writes Registers | $t_{SSN\_R}$ | 500 | — | — | ns | 6 |
| 10812 | Following Register Write to the UF_REGION_W Register | $t_{SSN\_UF01}$ | 50 | — | — | µs | 6 |
| **Time Between Sensor Data Requests** | | | | | | | |
| 10810 | Time Between Sensor Data Requests (Same Channel, SPI Only, Arm Enabled) | $t_{ACC\_REQ\_x}$ | 15 | — | — | µs | 6 |
| **Arming Output Activation Time (ARM0, ARM1, $I_{ARM} = 200$ µA)** | | | | | | | |
| 10809 | Moving Average and Count Arming Modes | $t_{ARM}$ | 0 | — | 1.50 | µs | 6 |
| 10817 | Unfiltered Mode Activation Delay | $t_{ARM\_UF\_DLY}$ | 0 | — | 1.50 | µs | 6 |
| 10816 | Unfiltered Mode Arm Assertion Time | $t_{ARM\_UF\_ASSERT}$ | 5.00 | — | 6.00 | µs | 6 |
| **Pin Capacitance** | | | | | | | |
| | Pin Capacitance (MISO, MOSI, SCLK, SS_B to VSS) | $C_{SPI\_PIN}$ | — | — | 10 | pF | 7 |

## 7.15 Dynamic electrical characteristics - I²C

**Table 38. Dynamic electrical characteristics - I²C**

$V_{CC\_BUF\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{CC\_BUF\_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Clock (SCL) Period (30 % of $V_{CC}$ to 30 % of $V_{CC}$)** | | | | | | | |
| 10819 | 100 kHz Mode | $t_{SCLK\_100}$ | 9.50 | — | — | µs | 6 |
| 10820 | 400 kHz Mode | $t_{SCLK\_400}$ | 2.37 | — | — | µs | 6 |
| 10821 | 1000 kHz Mode | $t_{SCLK\_1000}$ | 1.00 | — | — | µs | 6 |
| **Clock (SCL) High Time (70 % of $V_{CC}$ to 70 % of $V_{CC}$)** | | | | | | | |
| 10823 | 100 kHz Mode | $t_{SCLH\_100}$ | 4.00 | — | — | µs | 6 |
| 10837 | 400 kHz Mode | $t_{SCLH\_400}$ | 0.60 | — | — | µs | 6 |
| 10836 | 1000 kHz Mode (note: not compliant with UM10204 [1] | $t_{SCLH\_1000}$ | 0.50 | — | — | µs | 6 |
| **Clock (SCL) Low Time (30 % of $V_{CC}$ to 30 % of $V_{CC}$)** | | | | | | | |
| 10835 | 100 kHz Mode | $t_{SCLL\_100}$ | 4.70 | — | — | µs | 6 |
| 10839 | 400 kHz Mode | $t_{SCLL\_400}$ | 1.30 | — | — | µs | 6 |
| 10838 | 1000 kHz Mode | $t_{SCLL\_1000}$ | 0.50 | — | — | µs | 6 |
| **Clock (SCL) and Data (SDA) Rise Time (30 % of $V_{CC}$ to 70 % of $V_{CC}$)** | | | | | | | |
| 10834 | 100 kHz Mode | $t_{SRISE\_100}$ | — | — | 1000 | ns | 6 |
| 10841 | 400 kHz Mode | $t_{SRISE\_400}$ | — | — | 300 | ns | 6 |
| 10840 | 1000 kHz Mode | $t_{SRISE\_1000}$ | — | — | 120 | ns | 6 |
| **Clock (SCL) and Data (SDA) Fall Time (70 % of $V_{CC}$ to 30 % of $V_{CC}$)** | | | | | | | |
| 10833 | 100 kHz Mode | $t_{SFALL\_100}$ | — | — | 300 | ns | 6 |
| 10844 | 400 kHz Mode | $t_{SFALL\_400}$ | — | — | 300 | ns | 6 |
| 10843 | 1000 kHz Mode | $t_{SFALL\_1000}$ | — | — | 120 | ns | 6 |
| **Data Input Setup Time (SDA = 30/70 % of $V_{CC}$ to SCL = 30 % of $V_{CC}$)** | | | | | | | |
| 10832 | 100 kHz Mode | $t_{SETUP\_100}$ | 250 | — | — | ns | 6 |
| 10846 | 400 kHz Mode | $t_{SETUP\_400}$ | 100 | — | — | ns | 6 |
| 10845 | 1000 kHz Mode | $t_{SETUP\_1000}$ | 50 | — | — | ns | 6 |
| **Data Input Hold Time (SCL = 70 % of $V_{CC}$ to SDA = 30/70 % of $V_{CC}$)** | | | | | | | |
| 10831 | 100 kHz Mode | $t_{HOLD\_100}$ | 0 | — | 900 | ns | 6 |
| 10848 | 400 kHz Mode | $t_{HOLD\_400}$ | 0 | — | 900 | ns | 6 |
| 10847 | 1000 kHz Mode | $t_{HOLD\_1000}$ | 0 | — | 300 | ns | 6 |
| **Start Condition Setup Time (SDA = 30/70 % of $V_{CC}$ to SCL = 30 % of $V_{CC}$)** | | | | | | | |
| 10830 | 100 kHz Mode | $t_{STARTSETUP\_100}$ | 4.70 | — | — | µs | 6 |
| 10851 | 400 kHz Mode | $t_{STARTSETUP\_400}$ | 0.60 | — | — | µs | 6 |
| 10850 | 1000 kHz Mode | $t_{STARTSETUP\_1000}$ | 0.26 | — | — | µs | 6 |
| **Start Condition Hold Time (SCL = 70 % of $V_{CC}$ to SDA = 30/70 % of $V_{CC}$)** | | | | | | | |
| 10829 | 100 kHz Mode | $t_{STARTHOLD\_100}$ | 4.00 | — | — | µs | 6 |
| 10853 | 400 kHz Mode | $t_{STARTHOLD\_400}$ | 0.60 | — | — | µs | 6 |
| 10852 | 1000 kHz Mode | $t_{STARTHOLD\_1000}$ | 0.26 | — | — | µs | 6 |
| **Stop Condition Setup Time (SDA = 30/70 % of $V_{CC}$ to SCL = 30 % of $V_{CC}$)** | | | | | | | |
| 10828 | 100 kHz Mode | $t_{STOPSETUP\_100}$ | 4.00 | — | — | µs | 6 |
| 10855 | 400 kHz Mode | $t_{STOPSETUP\_400}$ | 0.60 | — | — | µs | 6 |
| 10854 | 1000 kHz Mode | $t_{STOPSETUP\_1000}$ | 0.26 | — | — | µs | 6 |
| **SCLK low to data valid (SCL = 30 % of $V_{CC}$ to SDA = 30/70 % of $V_{CC}$)** | | | | | | | |
| 10827 | 100 kHz Mode | $t_{VALID\_100}$ | — | — | 3.45 | µs | 6 |

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| 10857 | 400 kHz Mode | $t_{VALID\_400}$ | — | — | 0.90 | µs | 6 |
| 10856 | 1000 kHz Mode | $t_{VALID\_1000}$ | — | — | 0.45 | µs | 6 |
| **Bus Free Time (SDA = 70 % of $V_{CC}$ to SDA = 70 % of $V_{CC}$)** | | | | | | | |
| 10826 | 100 kHz Mode | $t_{FREE\_100}$ | 4.00 | — | — | µs | 6 |
| 10859 | 400 kHz Mode | $t_{FREE\_400}$ | 1.30 | — | — | µs | 6 |
| 10859 | 1000 kHz Mode | $t_{FREE\_1000}$ | 0.50 | — | — | µs | 6 |
| **Bus Capacitive Load** | | | | | | | |
| 10825 | Bus Capacitive Load | $C_{BUS}$ | — | — | 400 | pF | 7, 9 |

## 7.16 Dynamic electrical characteristics - signal chain, low-pass filter

**Table 39. Dynamic electrical characteristics - signal chain, low-pass filter**

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_min}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

| # | Characteristic | | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|---|
| **DSP Low-Pass Filters Sample Times** | | | | | | | | |
| 10872 | SAMPLERATE = 00, 01 | * | $t_{SigChain00}$, $t_{SigChain01}$ | — | 16 | — | µs | 7,8,9 |
| 10872 | SAMPLERATE = 10 | * | $t_{SigChain10}$ | — | 32 | — | µs | 7,8,9 |
| 10871 | SAMPLERATE = 11 | * | $t_{SigChain11}$ | — | 64 | — | µs | 7,8,9 |
| **DSP Low-Pass Filters (Signal Chain Sample Time = 16 µs)** | | | | | | | | |
| 21379 | Cutoff Frequency, Filter Option #0, and #2, 4-Pole | * | $f_{c0\_16}$, $f_{c2\_16}$ | — | 400 | — | Hz | 7,8,9,11 |
| 21380 | Cutoff Frequency, Filter Option #1, and #3, 3-Pole | * | $f_{c1\_16}$, $f_{c3\_16}$ | — | 400 | — | Hz | 7,8,9,11 |
| 21381 | Cutoff Frequency, Filter Option #4, 3-Pole | * | $f_{c4\_16}$ | — | 325 | — | Hz | 7,8,9,11 |
| 21382 | Cutoff Frequency, Filter Option #5, 2-Pole | * | $f_{c5\_16}$ | — | 370 | — | Hz | 7,8,9,11 |
| 21383 | Cutoff Frequency, Filter Option #6, 2-Pole | * | $f_{c6\_16}$ | — | 180 | — | Hz | 7,8,9,11 |
| 21384 | Cutoff Frequency, Filter Option #7, 2-Pole | * | $f_{c7\_16}$ | — | 100 | — | Hz | 7,8,9,11 |
| 21385 | Cutoff Frequency, Filter Option #8, 4-Pole | * | $f_{c8\_16}$ | — | 1500 | — | Hz | 7,8,9,11 |
| 26413 | Cutoff Frequency, Filter Option #9, 4-Pole | * | $f_{c9\_16}$ | — | 500 | — | Hz | 7,8,9,11 |
| 10860 | Cutoff Frequency, Filter Option #10, 4-Pole | * | $f_{c10\_16}$ | — | 800 | — | Hz | 7,8,9,11 |
| 10870 | Cutoff Frequency, Filter Option #11, 3-Pole | * | $f_{c11\_16}$ | — | 1200 | — | Hz | 7,8,9,11 |
| 10869 | Cutoff Frequency, Filter Option #12, 3-Pole | * | $f_{c12\_16}$ | — | 120 | — | Hz | 7,8,9,11 |
| | Cutoff Frequency, Filter Option #13, 3-Pole | * | $f_{c13\_16}$ | — | 20,000 | — | Hz | 7,8,9,11 |
| 10868 | Cutoff Frequency, Filter Option #14, 2-Pole | * | $f_{c14\_16}$ | — | 120 | — | Hz | 7,8,9,11 |
| 38364 | Cutoff Frequency, Filter Option #15, 2-Pole | * | $f_{c15\_16}$ | — | 50 | — | Hz | 7,8,9,11 |
| **DSP Low-Pass Filters (Signal Chain Sample Time = 32 µs)** | | | | | | | | |
| 38378 | Cutoff Frequency, Filter Option #0, and #2, 4-Pole | * | $f_{c0\_32}$, $f_{c2\_32}$ | — | 200 | — | Hz | 7,8,9,11 |
| 38379 | Cutoff Frequency, Filter Option #1, and #3, 3-Pole | * | $f_{c1\_32}$, $f_{c3\_32}$ | — | 200 | — | Hz | 7,8,9,11 |
| 38380 | Cutoff Frequency, Filter Option #4, 3-Pole | * | $f_{c4\_32}$ | — | 162.5 | — | Hz | 7,8,9,11 |
| 38381 | Cutoff Frequency, Filter Option #5, 2-Pole | * | $f_{c5\_32}$ | — | 185 | — | Hz | 7,8,9,11 |
| 38382 | Cutoff Frequency, Filter Option #6, 2-Pole | * | $f_{c6\_32}$ | — | 90 | — | Hz | 7,8,9,11 |
| 38383 | Cutoff Frequency, Filter Option #7, 2-Pole | * | $f_{c7\_32}$ | — | 50 | — | Hz | 7,8,9,11 |
| 38384 | Cutoff Frequency, Filter Option #8, 4-Pole | * | $f_{c8\_32}$ | — | 750 | — | Hz | 7,8,9,11 |
| 38385 | Cutoff Frequency, Filter Option #9, 3-Pole | * | $f_{c9\_32}$ | — | 250 | — | Hz | 7,8,9,11 |
| 38386 | Cutoff Frequency, Filter Option #10, 4-Pole | * | $f_{c10\_32}$ | — | 400 | — | Hz | 7,8,9,11 |
| 38387 | Cutoff Frequency, Filter Option #11, 4-Pole | * | $f_{c11\_32}$ | — | 600 | — | Hz | 7,8,9,11 |
| 38388 | Cutoff Frequency, Filter Option #12, 3-Pole | * | $f_{c12\_32}$ | — | 60 | — | Hz | 7,8,9,11 |
| | Cutoff Frequency, Filter Option #13, 2-Pole | | $f_{c13\_32}$ | — | 10,000 | — | Hz | 7,8,9,11 |
| 38389 | Cutoff Frequency, Filter Option #14, 2-Pole | * | $f_{c14\_32}$ | — | 60 | — | Hz | 7,8,9,11 |
| 38390 | Cutoff Frequency, Filter Option #15, 4-Pole | * | $f_{c15\_32}$ | — | 25 | — | Hz | 7,8,9,11 |
| **DSP Low-Pass Filters (Signal Chain Sample Time = 64 µs)** | | | | | | | | |
| 38365 | Cutoff Frequency, Filter Option #0, and #2, 4-Pole | * | $f_{c0\_64}$, $f_{c2\_64}$ | — | 100 | — | Hz | 7,8,9,11 |
| 38366 | Cutoff Frequency, Filter Option #1, and #3, 3-Pole | * | $f_{c1\_64}$, $f_{c3\_64}$ | — | 100 | — | Hz | 7,8,9,11 |
| 38367 | Cutoff Frequency, Filter Option #4, 3-Pole | * | $f_{c4\_64}$ | — | 81.25 | — | Hz | 7,8,9,11 |
| 38368 | Cutoff Frequency, Filter Option #5, 2-Pole | * | $f_{c5\_64}$ | — | 92.75 | — | Hz | 7,8,9,11 |
| 38369 | Cutoff Frequency, Filter Option #6, 2-Pole | * | $f_{c6\_64}$ | — | 45 | — | Hz | 7,8,9,11 |
| 38370 | Cutoff Frequency, Filter Option #7, 2-Pole | * | $f_{c7\_64}$ | — | 25 | — | Hz | 7,8,9,11 |
| 38371 | Cutoff Frequency, Filter Option #8, 4-Pole | * | $f_{c8\_64}$ | — | 375 | — | Hz | 7,8,9,11 |
| 38372 | Cutoff Frequency, Filter Option #9, 3-Pole | * | $f_{c9\_64}$ | — | 125 | — | Hz | 7,8,9,11 |

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| 38373 | Cutoff Frequency, Filter Option #10, 4-Pole * | $f_{c10\_64}$ | — | 200 | — | Hz | 7, 8, 9, 11 |
| 38374 | Cutoff Frequency, Filter Option #11, 4-Pole * | $f_{c11\_64}$ | — | 300 | — | Hz | 7, 8, 9, 11 |
| 38375 | Cutoff Frequency, Filter Option #12, 3-Pole * | $f_{c12\_64}$ | — | 30 | — | Hz | 7, 8, 9, 11 |
| | Cutoff Frequency, Filter Option #13, 2-Pole * | $f_{c13\_64}$ | — | 5,000 | — | Hz | 7, 8, 9, 11 |
| 38376 | Cutoff Frequency, Filter Option #14, 2-Pole * | $f_{c14\_64}$ | — | 30 | — | Hz | 7, 8, 9, 11 |
| 38377 | Cutoff Frequency, Filter Option #15, 4-Pole * | $f_{c15\_64}$ | — | 12.5 | — | Hz | 7, 8, 9, 11 |

## 7.17 Dynamic electrical characteristics - signal chain

**Table 40. Dynamic electrical characteristics - signal chain**

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_min}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Offset Cancellation Low-Pass Filter** | | | | | | | |
| 10863 | Sample Time, Phase 0 | $t_{OCSAMP0}$ | — | 256 | — | µs | 7, 8 |
| 10874 | Cutoff Frequency, Phase 0, 1-Pole | $f_{OC0}$ | — | 163.8 | — | Hz | 7, 8 |
| 10875 | Time in Phase 0 | $t_{OC0}$ | — | 4.096 | — | ms | 7, 8 |
| 10888 | Sample Time, Phase 1 | $t_{OCSAMP1}$ | — | 256 | — | µs | 7, 8 |
| 10889 | Cutoff Frequency, Phase 1, 1-Pole | $f_{OC1}$ | — | 40.96 | — | Hz | 7, 8 |
| 10890 | Time in Phase 1 | $t_{OC1}$ | — | 4.096 | — | ms | 7, 8 |
| 10885 | Sample Time, Phase 2 | $t_{OCSAMP2}$ | — | 256 | — | µs | 7, 8 |
| 10886 | Cutoff Frequency, Phase 2, 1-Pole | $f_{OC2}$ | — | 10.24 | — | Hz | 7, 8 |
| 10887 | Time in Phase 2 | $t_{OC2}$ | — | 16.388 | — | ms | 7, 8 |
| 10900 | Sample Time, Phase 3 | $t_{OCSAMP3}$ | — | 256 | — | µs | 7, 8 |
| 10901 | Cutoff Frequency, Phase 3, 1-Pole | $f_{OC3}$ | — | 2.560 | — | Hz | 7, 8 |
| 10902 | Time in Phase 3 | $t_{OC3}$ | — | 65.53 | — | ms | 7, 8 |
| 10897 | Sample Time, Phase 4 | $t_{OCSAMP4}$ | — | 256 | — | µs | 7, 8 |
| 10898 | Cutoff Frequency, Phase 4, 1-Pole | $f_{OC4}$ | — | 0.6400 | — | Hz | 7, 8 |
| 10899 | Time in Phase 4 | $t_{OC4}$ | — | 262.19 | — | ms | 7, 8 |
| 10894 | Sample Time, Phase 5 | $t_{OCSAMP5}$ | — | 256 | — | µs | 7, 8 |
| 10895 | Cutoff Frequency, Phase 5, 1-Pole | $f_{OC5}$ | — | 0.1600 | — | Hz | 7, 8 |
| 10896 | Time in Phase 5 | $t_{OC5}$ | — | 1049 | — | ms | 7, 8 |
| 39811 | Sample Time, Phase 6a | $t_{OCSAMP6a}$ | — | 256 | — | µs | 7, 8 |
| 39812 | Cutoff Frequency, Phase 6a, 1-Pole * | $f_{OC6a}$ | — | 0.0400 | — | Hz | 7, 8 |
| 39813 | Sample Time, Phase 6b | $t_{OCSAMP6b}$ | — | 1024 | — | µs | 7, 8 |
| 39814 | Cutoff Frequency, Phase 6b, 1-Pole * | $f_{OC6b}$ | — | 0.005 | — | Hz | 7, 8 |
| **Offset Cancellation Output Rate Limiting (0.04 Hz Offset LPF only)** | | | | | | | |
| 10882 | Rate Limiting Output Update Time | $t_{RL\_Rate}$ | — | 2 | — | s | 7, 8, 9 |
| 10903 | Rate Limiting Output Step Size (10 bit) | $OFF_{Step10}$ | — | 0.5 | — | LSB | 7, 8, 9 |
| | Rate Limiting Output Step Size (16 bit, PSI5, SPI) | $OFF_{Step16}$ | — | 32 | — | LSB | 7, 8 |
| **Offset Monitor** | | | | | | | |
| 10883 | Update Rate | $OFFMON_{OSC}$ | — | 0.5 | — | ms | 7, 8 |
| 10905 | Count Limit | $OFFMON_{CNTLIMIT}$ | — | 4096 | — | 1 | 7, 8 |
| 10904 | Counter Size | $OFFMON_{CNTSIZE}$ | — | 8192 | — | 1 | 7, 8 |
| **Signal delay** | | | | | | | |
| 10881 | Signal Delay (Sinc Filter to Output Delay, excluding LPF) | $t_{SigDelay}$ | — | — | 128 | µs | 7, 8 |
| **Interpolation** | | | | | | | |
| 20923 | $t_{SigChain} = t_{SigChain00}$, $t_{SigChain01}$ | $t_{INTERP\_00, 01}$ | — | 1 | — | µs | 7, 8 |
| 20922 | $t_{SigChain} = t_{SigChain02}$ | $t_{INTERP\_02}$ | — | 2 | — | µs | 7, 8 |
| 20921 | $t_{SigChain} = t_{SigChain03}$ | $t_{INTERP\_03}$ | — | 4 | — | µs | 7, 8 |
| 10877 | Interpolation Latency | $t_{LAT\_INTERP}$ | — | $t_{SigChainxx}$ | — | s | 7, 8 |

## 7.18 Dynamic electrical characteristics - analog self-test response time

**Table 41. Dynamic electrical characteristics - analog self-test response time**

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_min}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Medium g, Lateral** | | | | | | | |
| **Self-test Response Time: Self-test Activation/Deactivation to 99 %/1 % $g_{ST}$** | | | | | | | |
| 10878 | Medium g Lateral, LPF = 800 Hz, 4-Pole | $t_{ST\_Resp\_MedX\_800\_4}$ | 750 | 795 | 1020 | µs | 7, 8 |
| 44634 | Medium g Lateral, LPF = 1500 Hz, 4-Pole | $t_{ST\_Resp\_MedX\_1500\_4}$ | 395 | 415 | 725 | µs | 7, 8 |
| 38147 | Medium g Lateral, LPF = 400 Hz, 4-Pole | $t_{ST\_Resp\_MedX\_400\_4}$ | 1510 | 1590 | 1810 | µs | 7, 8 |
| 38151 | Medium g Lateral, LPF = 400 Hz, 3-Pole | $t_{ST\_Resp\_MedX\_400\_3}$ | 1420 | 1490 | 1710 | µs | 7, 8 |
| 38150 | Medium g Lateral, LPF = 180 Hz, 2-Pole | $t_{ST\_Resp\_MedX\_180\_2}$ | 3030 | 3190 | 3470 | µs | 7, 8 |
| 38149 | Medium g Lateral, LPF = 300 Hz, 4-Pole | $t_{ST\_Resp\_MedX\_300\_4}$ | 2010 | 2120 | 2360 | µs | 7, 8 |
| 38148 | Medium g Lateral, LPF = 188 Hz, 4-Pole | $t_{ST\_Resp\_MedX\_188\_4}$ | 3210 | 3380 | 3680 | µs | 7, 8 |
| **High g, Lateral** | | | | | | | |
| **Self-test Response Time: Self-test Activation/Deactivation to 99 % / 1 % $g_{ST}$** | | | | | | | |
| 38152 | High g Lateral, LPF = 800 Hz, 4-Pole | $t_{ST\_Resp\_HiX\_800\_4}$ | 750 | 795 | 892 | µs | 7, 8 |
| 44636 | High g Lateral, LPF = 1500 Hz, 4-Pole | $t_{ST\_Resp\_HiX\_1500\_4}$ | 395 | 415 | 490 | µs | 7, 8 |
| 38153 | High g Lateral, LPF = 400 Hz, 4-Pole | $t_{ST\_Resp\_HiX\_400\_4}$ | 1510 | 1590 | 1720 | µs | 7, 8 |
| 38154 | High g Lateral, LPF = 400 Hz, 3-Pole | $t_{ST\_Resp\_HiX\_400\_3}$ | 1420 | 1490 | 1620 | µs | 7, 8 |
| 38155 | High g Lateral, LPF = 180 Hz, 2-Pole | $t_{ST\_Resp\_HiX\_180\_2}$ | 3030 | 3190 | 3400 | µs | 7, 8 |
| 38156 | High g Lateral, LPF = 300 Hz, 4-Pole | $t_{ST\_Resp\_HiX\_300\_4}$ | 2010 | 2120 | 2280 | µs | 7, 8 |
| 38157 | High g Lateral, LPF = 188 Hz, 4-Pole | $t_{ST\_Resp\_HiX\_188\_4}$ | 3210 | 3380 | 3600 | µs | 7, 8 |
| **Low g, Z-Axis** | | | | | | | |
| **Self-test Response Time: Self-test Activation/Deactivation to 99 % / 1 % $g_{ST}$** | | | | | | | |
| | Low g Z-Axis, LPF = 250 Hz, 3-Pole | $t_{ST\_Resp\_LowZ\_250\_3}$ | 2400 | 2600 | 3100 | µs | 7, 8 |
| | Low g Z-Axis, LPF = 50 Hz, 2-Pole | $t_{ST\_Resp\_LowZ\_50\_2}$ | 11000 | 11700 | 12500 | µs | 7, 8 |
| **Medium g, Z-Axis** | | | | | | | |
| **Self-test Response Time: Self-test Activation/Deactivation to 99 % / 1 % $g_{ST}$** | | | | | | | |
| 38158 | Medium g Z-Axis, LPF = 800 Hz, 4-Pole | $t_{ST\_Resp\_MedZ\_800\_4}$ | 750 | 795 | 1010 | µs | 7, 8 |
| 44637 | Medium g Z-Axis, LPF = 1500 Hz, 4-Pole | $t_{ST\_Resp\_MedZ\_1500\_4}$ | 395 | 415 | 710 | µs | 7, 8 |
| 38159 | Medium g Z-Axis, LPF = 400 Hz, 4-Pole | $t_{ST\_Resp\_MedZ\_400\_4}$ | 1510 | 1590 | 1810 | µs | 7, 8 |
| 38160 | Medium g Z-Axis, LPF = 400 Hz, 3-Pole | $t_{ST\_Resp\_MedZ\_400\_3}$ | 1420 | 1490 | 1700 | µs | 7, 8 |
| 38161 | Medium g Z-Axis, LPF = 180 Hz, 2-Pole | $t_{ST\_Resp\_MedZ\_180\_2}$ | 3030 | 3190 | 3470 | µs | 7, 8 |
| 38162 | Medium g Z-Axis, LPF = 300 Hz, 4-Pole | $t_{ST\_Resp\_MedZ\_300\_4}$ | 2010 | 2120 | 2360 | µs | 7, 8 |
| 38163 | Medium g Z-Axis, LPF = 188 Hz, 4-Pole | $t_{ST\_Resp\_MedZ\_188\_4}$ | 3210 | 3380 | 3680 | µs | 7, 8 |
| **High g, Z-Axis** | | | | | | | |
| **Self-test Response Time: Self-test Activation/Deactivation to 99 % / 1 % $g_{ST}$** | | | | | | | |
| 38164 | High g Z-Axis, LPF = 800 Hz, 4-Pole | $t_{ST\_Resp\_HiZ\_800\_4}$ | 750 | 795 | 994 | µs | 7, 8 |
| 44638 | High g Z-Axis, LPF = 1500 Hz, 4-Pole | $t_{ST\_Resp\_HiZ\_1500\_4}$ | 395 | 415 | 675 | µs | 7, 8 |
| 38165 | High g Z-Axis, LPF = 400 Hz, 4-Pole | $t_{ST\_Resp\_HiZ\_400\_4}$ | 1510 | 1590 | 1800 | µs | 7, 8 |
| 38166 | High g Z-Axis, LPF = 400 Hz, 3-Pole | $t_{ST\_Resp\_HiZ\_400\_3}$ | 1420 | 1490 | 1690 | µs | 7, 8 |
| 38167 | High g Z-Axis, LPF = 180 Hz, 2-Pole | $t_{ST\_Resp\_HiZ\_180\_2}$ | 3030 | 3190 | 3470 | µs | 7, 8 |
| 38168 | High g Z-Axis, LPF = 300 Hz, 4-Pole | $t_{ST\_Resp\_HiZ\_300\_4}$ | 2010 | 2120 | 2360 | µs | 7, 8 |
| 38169 | High g Z-Axis, LPF = 188 Hz, 4-Pole | $t_{ST\_Resp\_HiZ\_188\_4}$ | 3210 | 3380 | 3680 | µs | 7, 8 |

## 7.19 Dynamic electrical characteristics - digital self-test response time

**Table 42. Dynamic electrical characteristics - digital self-test response time**

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_min}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Self-test Response Time: Self-test Activation/Deactivation to Final Value** | | | | | | | |
| 44639 | LPF ≤ 60 Hz | $t_{DST\_Resp\_50}$ | — | — | 50 | ms | 7, 8 |
| 44641 | 60 Hz ≤ LPF ≤ 200 Hz | $t_{DST\_Resp\_100}$ | — | — | 25 | ms | 7, 8 |
| 44640 | 300 Hz ≤ LPF ≤ 1500 Hz | $t_{DST\_Resp\_400}$ | — | — | 12 | ms | 7, 8 |
| 38176 | Fixed Pattern Response Time: Self-test Activation/Deactivation | $t_{ST\_FP\_Resp}$ | — | — | 100 | µs | 7, 8 |

## 7.20 Dynamic electrical characteristics - transducer

**Table 43. Dynamic electrical characteristics - transducer**

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_min}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Lateral Transducer Rolloff Frequency (–3 db)** | | | | | | | |
| 10917 | Medium g | $f_{gcell\_3dB\_mid}$ | 1500 | 2500 | 4500 | Hz | 7 |
| 10915 | High g | $f_{gcell\_3dB\_hi}$ | 4000 | 7000 | 13000 | Hz | 7 |
| **Lateral Transducer Delay (@100 Hz)** | | | | | | | |
| 10921 | Medium g | $f_{gcell\_delay100\_mid}$ | — | — | 250 | µs | 7 |
| 10919 | High g | $f_{gcell\_delay100\_hi}$ | — | — | 250 | µs | 7 |
| **Z-Axis Transducer Rolloff Frequency (–3 db)** | | | | | | | |
| | Low g | $f_{gcell\_3dB\_low}$ | 360 | 580 | 900 | Hz | 7 |
| 10923 | Medium g | $f_{gcell\_3dB\_mid}$ | 1500 | 2500 | 4500 | Hz | 7 |
| 10925 | High g | $f_{gcell\_3dB\_hi}$ | 1500 | 2500 | 7500 | Hz | 7 |
| **Z-Axis Transducer Delay (@100 Hz)** | | | | | | | |
| 10927 | Medium g | $f_{gcell\_delay100\_mid}$ | — | — | 250 | µs | 7 |
| 10929 | High g | $f_{gcell\_delay100\_hi}$ | — | — | 250 | µs | 7 |
| **Z-axis Transducer Delay (@10 Hz)** | | | | | | | |
| | Low g | $f_{gcell\_delay10\_low}$ | — | — | 350 | µs | 7 |
| **Package Resonance Frequency** | | | | | | | |
| 10912 | Package Resonance Frequency | $f_{Package}$ | 100 | — | — | kHz | 7 |

## 7.21 Dynamic electrical characteristics - supply and support circuitry

**Table 44. Dynamic electrical characteristics - supply and support circuitry**

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_min}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | Test notes |
|---|---|---|---|---|---|---|---|
| **Reset Recovery (All Modes, excluding $V_{BUS\_I}$ voltage ramp time)** | | | | | | | |
| 10930 | VCC = VCCMIN to POR Release | $t_{VCC\_POR}$ | — | — | 1 | ms | 7,8,9 |
| 10939 | POR to first DSI Command (Section 9.1: DSI3 physical layer) | $t_{POR\_DSI}$ | — | — | 6 | ms | 7,8,9 |
| 10938 | POR to PSI5 Initialization Phase 1 Start (Section 10.4: Initialization) | $t_{POR\_PSI5}$ | — | — | 6 | ms | 7,8 |
| 10937 | POR to first SPI Command | $t_{POR\_SPI}$ | 0.400 | — | 0.700 | ms | 7,8,9 |
| 10936 | POR to Sensor Data Valid | $t_{POR\_DataValid}$ | — | — | 30 | ms | 7,8,9 |
| 10935 | DSP Setting Change to Sensor Data Valid: DS3, SPI, I²C | $t_{RANGE\_DataValid}$ | — | — | 6 | ms | 7,8,9 |
| **Soft Reset Activation Time** | | | | | | | |
| 10934 | SPI: SS_B high to Reset | $t_{SOFT\_RESET\_SPI}$ | — | — | 700 | ns | 7,8 |
| 30152 | I²C: Command Complete to Reset (No ACK follows) | $t_{SOFT\_RESET\_I2C}$ | — | — | 700 | ns | 7,8 |
| 30151 | DSI3: Command/Response Complete to Reset | $t_{SOFT\_RESET\_DSI}$ | — | — | 11 | µs | 7,8 |
| 41495 | PSI5: Command/Response Complete to Reset | $t_{SOFT\_RESET\_PSI}$ | — | — | 120 | µs | 7,8 |
| **Internal Oscillator Period** | | | | | | | |
| 10933 | Untrained * | $f_{OSC}$ | 9.560 | 10.000 | 10.440 | MHz | 1,7,8,9 |
| 10940 | With Oscillator Training | $f_{OSC\_TRAIN}$ | 9.900 | 10.000 | 10.100 | MHz | 7,8,9 |
| **Oscillator Training (Section 8.5.1: Oscillator training)** | | | | | | | |
| 10932 | Oscillator Training Time | $t_{OscTrain}$ | — | 4 | — | ms | 7,8 |
| 10942 | Oscillator Cycles in Training Time | $n_{OSC\_4ms\_TYP}$ | — | 40000 | — | $1/f_{OSC}$ | 7,8 |
| 10944 | Oscillator Training Window | $OscTrain_{WIN}$ | 38000 | — | 42000 | $1/f_{OSC}$ | 7,8 |
| 10943 | Oscillator Training Adjustment Threshold | $OscTrain_{ADJ}$ | –400 | — | 400 | $1/f_{OSC}$ | 7,8 |
| 10941 | Oscillator Training Step Size | $OscTrain_{RES}$ | | 250 | | $1/f_{OSC}$ | 7,8 |
| **Quiescent Current Settling** | | | | | | | |
| 10946 | Quiescent Current Settling Time (Power Applied to Iq = $I_{IDLE}$ ± 2 mA) | $t_{SET}$ | — | — | 4 | ms | 7,9 |
| **BUS_I Micro-cut** | | | | | | | |
| 10931 | Survival Time (BUS_I disconnect without Reset, $C_{BUF}$=1 µF, Bus with 1 slave) | $t_{BUS\_I\_MICROCUT}$ | 30 | — | — | µs | 7,9 |
| 10952 | Reset Time (BUS_I disconnect time to Reset, $C_{BUF}$=1 µF, Bus with 1 slave) | $t_{BUS\_I\_RESET}$ | — | — | 1000 | µs | 7,9 |
| 10953 | Survival Time (BUS_I disconnect without Reset, $C_{BUF}$=470 nF, Bus with 1 slave) | $t_{BUS\_I\_MICROCUT}$ | 15 | — | — | µs | 7,9 |
| 10954 | Reset Time (BUS_I disconnect time to Reset, $C_{BUF}$=470 nF, Bus with 1 slave) | $t_{BUS\_I\_RESET}$ | — | — | 1000 | µs | 7,9 |
| **BUS_I Undervoltage Detection Delay** | | | | | | | |
| 10947 | BUS_I < $V_{BUS\_I\_UV\_F}$ to $I_{RESP}$ Deactivation | $t_{BUS\_I\_POR}$ | — | — | 5 | µs | 7 |
| **$V_{BUF}$ Undervoltage Detection Delay** | | | | | | | |
| 10958 | $V_{BUF}$ < $V_{BUF\_UV\_F}$ to $I_{RESP}$ Deactivation | $t_{VBUF\_POR}$ | — | — | 5 | µs | 7 |
| **Undervoltage/Overvoltage Recovery Delay** | | | | | | | |
| 10957 | Undervoltage/Overvoltage Recovery Delay | $t_{UVOV\_RCV}$ | — | 100 | — | µs | 7 |
| **$V_{BUF}$ Capacitor Monitor** | | | | | | | |
| 36817 | DSI Command Start to Capacitor Test | $t_{D\_CAPTEST}$ | — | 3.0 | — | µs | 7 |
| 36821 | PSI5 Synchronous Command Start to Capacitor Test | $t_{P\_CAPTEST}$ | — | 9.2 | — | µs | 7 |
| 36823 | PSI5 Asynchronous Response Start to Capacitor Test | $t_{A\_CAPTEST}$ | — | 179.2 | — | µs | 7 |
| 36822 | Capacitor Test Disconnect Time | $t_{CAPTST\_TIME}$ | — | 1 | — | µs | 7 |

# 8 Functional description

## 8.1 User accessible data array

A user accessible data array allows for each device to be customized. The array consists of an OTP factory programmable block, an OTP user programmable block, and read-only registers for data and device status. The OTP blocks incorporate independent data verification.

### 8.1.1 User accessible data - general device information

**Table 45. User accessible data - general device information**

| | | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Type | Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | $00 | COUNT | COUNT[7:0] | | | | | | | |
| R | $01 | DEVSTAT | CH0_ERR | CH1_ERR | COMM_ERR | MEMTEMP_ERR | SUPPLY_ERR | TESTMODE | DEVRES | DEVINIT |
| R | $02 | DEVSTAT1 | VBUFUV_ERR | BUSINUV_ERR | VBUFOV_ERR | RESERVED | INTREGA_ERR | INTREG_ERR | INTREGF_ERR | CONT_ERR |
| R | $03 | DEVSTAT2 | F_OTP_ERR | U_OTP_ERR | U_RW_ERR | U_W_ACTIVE | TEMP1_ERR | TEMP0_ERR | RESERVED | RESERVED |
| R | $04 | DEVSTAT3 | MISO_ERR | OSCTRAIN_ERR | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| R | $05 | COMMREV | 0 | 0 | 0 | 0 | COMMREV[3:0] | | | |
| R | $06 | MREAD_STAT | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | MARGIN_RD_ACT | MARGIN_RD_ERR |
| R | $07 - $0D | RESERVED | RESERVED | | | | | | | |
| R | $0E | TEMPERATURE | TEMP[7:0] | | | | | | | |
| R | $0F | RESERVED | RESERVED | | | | | | | |

### 8.1.2 User accessible data - communication information

**Table 46. User accessible data - communication information**

| | | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Type[1] | Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W | $10 | DEVLOCK_WR | ENDINIT | RESERVED | RESERVED | RESERVED | SUP_ERR_DIS | RESERVED | RESET[1:0] | |
| R/W | $11 | WRITE_OTP_EN | UOTP_WR_INIT | MARGIN_RD_EN | RESERVED | RESERVED | EX_COMMTYPE | EX_PADDR | UOTP_REGION[1:0] | |
| R/W | $12 | BUSSW_CTRL | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | BUSSW_CTRL[1:0] | |
| R/W | $13 | PSI5_TEST | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | PSI5_TEST |
| R/W | $14 | UF_REGION_W | REGION_LOAD[3:0] | | | | 0 | 0 | 0 | 0 |
| R | $15 | UF_REGION_R | REGION_ACTIVE[3:0] | | | | 0 | 0 | 0 | 0 |
| UF2 | $16 | COMMTYPE | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | COMMTYPE[2:0] | | |
| UF2 | $17 | RESERVED | RESERVED | | | | | | | |
| UF2 | $18 | PHYSADDR | 0 | 0 | 0 | 0 | PADDR[3:0] | | | |
| UF2 | $19 | RESERVED | RESERVED | | | | | | | |
| UF2 | $1A | SOURCEID_0 | SID0_EN | PDCMFORMAT[2:0] | | | SOURCEID_0[3:0] | | | |
| UF2 | $1B | SOURCEID_1 | SID1_EN | RESERVED | RESERVED | RESERVED | SOURCEID_1[3:0] | | | |
| UF2 | $1C | SOURCEID_2 | SID2_EN | RESERVED | RESERVED | RESERVED | SOURCEID_2[3:0] | | | |
| UF2 | $1D | SOURCEID_3 | SID3_EN | RESERVED | RESERVED | RESERVED | SOURCEID_3[3:0] | | | |
| UF2 | $1E - $21 | RESERVED | RESERVED | | | | | | | |
| UF2 | $22 | TIMING_CFG | PDCM_PER[2:0] | | | OSCTRAIN_SEL | CK_CAL_RST | CRM_PER[1:0] | | CK_CAL_EN |
| UF2 | $23 | CHIPTIME | ST_RPT[1:0] | | PSI5_ERRLATCH | SS_EN | CHIPTIME[3:0] | | | |
| UF2 | $24 | TIMING_CFG2 | PSI5_INIT2_D19 | OSCTRAIN_ERRCNT[2:0] | | | CAPTEST_OFF | RESERVED | BDM_FRAGSIZE | BDM_EN |
| UF2 | $25 | PSI5_CFG | SYNC_PD | DAISY_CHAIN | PSI5_ILOW | DUALTRANS | EMSG_EXT | P_CRC | INIT2_EXT | ASYNC |
| UF2 | $26 | PDCM_RSPST0_L | PDCM_RSPST0[7:0] | | | | | | | |
| UF2 | $27 | PDCM_RSPST0_H | BRC_RSP0[1:0] | | RESERVED | PDCM_RSPST0[12:8] | | | | |
| UF2 | $28 | PDCM_RSPST1_L | PDCM_RSPST1[7:0] | | | | | | | |
| UF2 | $29 | PDCM_RSPST1_H | BRC_RSP1[1:0] | | RESERVED | PDCM_RSPST1[12:8] | | | | |
| UF2 | $2A | PDCM_RSPST2_L | PDCM_RSPST2[7:0] | | | | | | | |
| UF2 | $2B | PDCM_RSPST2_H | BRC_RSP2[1:0] | | RESERVED | PDCM_RSPST2[12:8] | | | | |
| UF2 | $2C | PDCM_RSPST3_L | PDCM_RSPST3[7:0] | | | | | | | |
| UF2 | $2D | PDCM_RSPST3_H | BRC_RSP3[1:0] | | RESERVED | PDCM_RSPST3[12:8] | | | | |
| UF2 | $2E - $37 | RESERVED | RESERVED | | | | | | | |
| UF2 | $38 | PDCM_CMD_B_L | PDCM_CMD_B[7:0] | | | | | | | |
| UF2 | $39 | PDCM_CMD_B_H | RESERVED | RESERVED | RESERVED | PDCM_CMD_B[12:8] | | | | |
| UF2 | $3A - $3C | RESERVED | RESERVED | | | | | | | |
| UF2 | $3D | SPI_CFG | SPI_STATUS | DATASIZE | SPI_CRC_LEN[1:0] | | SPICRCSEED[3:0] | | | |
| UF2 | $3E | WHO_AM_I | WHO_AM_I[7:0] | | | | | | | |
| UF2 | $3F | I2C_ADDRESS | I2C_ADDRESS[7:0] | | | | | | | |

1. *Memory Type Codes*
   *R - Readable Register with No OTP*
   *F – User Readable Register with OTP*
   *UF0 – One Time User Programmable OTP Location Region 0*
   *UF1 – One Time User Programmable OTP Location Region 1*
   *UF2 – One Time User Programmable OTP Location Region 2*
   *R/W – User Writable Register*

### 8.1.3 User accessible data - sensor specific information

**Table 47. User accessible data - sensor specific information**

| | | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Type[1] | Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UF2 | $40 | CH0_CFG_U1 | LPF[3:0] | | | | SAMPLERATE[1:0] | | USER_SNS_SHIFT[1:0] | |
| UF2 | $41 | CH0_CFG_U2 | U_SNS_MULT[7:0] | | | | | | | |
| UF2 | $42 | CH0_CFG_U3 | UNSIGNEDDATA | DATATYPE0[1:0] | | DATATYPE1[2:0] | | | MOVEAVG[1:0] | |
| UF2 | $43 | CH0_CFG_U4 | RESET_OC | INVERT | OC_FILT[1:0] | | PCM | ARM_CFG[2:0] | | |
| UF2 | $44 | CH0_CFG_U5 | ST_CTRL[3:0] | | | | OC_LIMIT[2:0] | | | DSP_DIS |
| UF2 | $45 | CH0_ARM_CFG | ARM_DS[1:0] | | ARM_PS[1:0] | | ARM_WS_N[1:0] | | ARM_WS_P[1:0] | |
| UF2 | $46 | CH0_ARM_T_P | ARM_T_P[7:0] | | | | | | | |
| UF2 | $47 | CH0_ARM_T_N | ARM_T_N[7:0] | | | | | | | |
| UF2 | $48 | CH1_CFG_U1 | LPF[3:0] | | | | SAMPLERATE[1:0] | | USER_SNS_SHIFT[1:0] | |
| UF2 | $49 | CH1_CFG_U2 | U_SNS_MULT[7:0] | | | | | | | |
| UF2 | $4A | CH1_CFG_U3 | UNSIGNEDDATA | DATATYPE0[1:0] | | DATATYPE1[2:0] | | | MOVEAVG[1:0] | |
| UF2 | $4B | CH1_CFG_U4 | RESET_OC | INVERT | OC_FILT[1:0] | | PCM | ARM_CFG[2:0] | | |
| UF2 | $4C | CH1_CFG_U5 | ST_CTRL[3:0] | | | | OC_LIMIT[2:0] | | | DSP_DIS |
| UF2 | $4D | CH1_ARM_CFG | ARM_DS[1:0] | | ARM_PS[1:0] | | ARM_WS_N[1:0] | | ARM_WS_P[1:0] | |
| UF2 | $4E | CH1_ARM_T_P | ARM_T_P[7:0] | | | | | | | |
| UF2 | $4F | CH1_ARM_T_N | ARM_T_N[7:0] | | | | | | | |
| UF2 | $50 | OC_PHASE_CFG | CH0_OCFINAL | CH1_OCFINAL | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| UF2 | $51-$54 | RESERVED | RESERVED | | | | | | | |
| UF2 | $55 | CH0_U_OFFSET_L | CH0_U_OFFSET[7:0] | | | | | | | |
| UF2 | $56 | CH0_U_OFFSET_H | CH0_U_OFFSET[15:8] | | | | | | | |
| UF2 | $57-$5C | RESERVED | RESERVED | | | | | | | |
| UF2 | $5D | CH1_U_OFFSET_L | CH1_U_OFFSET[7:0] | | | | | | | |
| UF2 | $5E | CH1_U_OFFSET_H | CH1_U_OFFSET[15:8] | | | | | | | |
| F | $5F | CRC_UF2 | LOCK_UF2 | 0 | 0 | 0 | CRC_UF2[3:0] | | | |
| R | $60 | CH0_STAT | SIGNALCLIP | OCPHASE[2:0] | | | ST_INCMPLT | ST_ACTIVE | OFFSET_ERR | ST_ERROR |
| R | $61 | DEVSTAT_COPY | CH0_ERR | CH1_ERR | COMM_ERR | MEMTEMP_ERR | SUPPLY_ERR | TESTMODE | DEVRES | DEVINIT |
| R | $62 | CH0_SNSDATA0_L | CH0_SNSDATA0[7:0] | | | | | | | |
| R | $63 | CH0_SNSDATA0_H | CH0_SNSDATA0[15:8] | | | | | | | |
| R | $64 | CH0_SNSDATA1_L | CH0_SNSDATA1[7:0] | | | | | | | |
| R | $65 | CH0_SNSDATA1_H | CH0_SNSDATA1[15:8] | | | | | | | |
| R | $66-$6F | RESERVED | RESERVED | | | | | | | |
| R | $70 | CH1_STAT | SIGNALCLIP | OCPHASE[2:0] | | | ST_INCMPLT | ST_ACTIVE | OFFSET_ERR | ST_ERROR |
| R | $71 | RESERVED | RESERVED | | | | | | | |
| R | $72 | CH1_SNSDATA0_L | CH1_SNSDATA0[7:0] | | | | | | | |
| R | $73 | CH1_SNSDATA0_H | CH1_SNSDATA0[15:8] | | | | | | | |
| R | $74 | CH1_SNSDATA1_L | CH1_SNSDATA1[7:0] | | | | | | | |
| R | $75 | CH1_SNSDATA1_H | CH1_SNSDATA1[15:8] | | | | | | | |
| R | $76-$9F | RESERVED | RESERVED | | | | | | | |

1. *Memory Type Codes*
   - *R - Readable Register with No OTP*
   - *F – User Readable Register with OTP*
   - *UF0 – One Time User Programmable OTP Location Region 0*
   - *UF1 – One Time User Programmable OTP Location Region 1*
   - *UF2 – One Time User Programmable OTP Location Region 2*
   - *R/W – User Writable Register*

### 8.1.4 User accessible data - sensor specific information

**Table 48. User accessible data - sensor specific information**

| | | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Type[1] | Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| F | $A0 | CH0_CFG_F | DEV_RANGE[3:0] | | | | RESERVED | RESERVED | AXIS[1:0] | |
| F | $A1 | RESERVED | RESERVED | | | | | | | |
| F | $A2 | CH0_STL_P_L | CH0_STL_P[7:0] | | | | | | | |
| F | $A3 | CH0_STL_P_H | CH0_STL_P[15:8] | | | | | | | |
| F | $A4 | CH0_STH_P_L | CH0_STH_P[7:0] | | | | | | | |
| F | $A5 | CH0_STH_P_H | CH0_STH_P[15:8] | | | | | | | |
| F | $A6 | CH0_STL_N_L | CH0_STL_N[7:0] | | | | | | | |
| F | $A7 | CH0_STL_N_H | CH0_STL_N[15:8] | | | | | | | |
| F | $A8 | CH0_STH_N_L | CH0_STH_N[7:0] | | | | | | | |
| F | $A9 | CH0_STH_N_H | CH0_STH_N[15:8] | | | | | | | |
| F | $AA-$AE | RESERVED | RESERVED | | | | | | | |
| F | $AF | CRC_F_A | LOCK_F_A | REGA_BLOCKID[2:0] | | | CRC_F_A[3:0] | | | |
| F | $B0 | CH1_CFG_F | DEV_RANGE[3:0] | | | | RESERVED | RESERVED | AXIS[1:0] | |
| F | $B1 | RESERVED | RESERVED | | | | | | | |
| F | $B2 | CH1_STL_P_L | CH1_STL_P[7:0] | | | | | | | |
| F | $B3 | CH1_STL_P_H | CH1_STL_P[15:8] | | | | | | | |
| F | $B4 | CH1_STH_P_L | CH1_STH_P[7:0] | | | | | | | |
| F | $B5 | CH1_STH_P_H | CH1_STH_P[15:8] | | | | | | | |
| F | $B6 | CH1_STL_N_L | CH1_STL_N[7:0] | | | | | | | |
| F | $B7 | CH1_STL_N_H | CH1_STL_N[15:8] | | | | | | | |
| F | $B8 | CH1_STH_N_L | CH1_STH_N[7:0] | | | | | | | |
| F | $B9 | CH1_STH_N_H | CH1_STH_N[15:8] | | | | | | | |
| F | $BA-$BE | RESERVED | RESERVED | | | | | | | |
| F | $BF | CRC_F_B | LOCK_F_B | REGB_BLOCKID[2:0] | | | CRC_F_B[3:0] | | | |

1. *Memory Type Codes*
   *R - Readable Register with No OTP*
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   *UF1 – One Time User Programmable OTP Location Region 1*
   *UF2 – One Time User Programmable OTP Location Region 2*
   *R/W – User Writable Register*

### 8.1.5 User accessible data - traceability information

**Table 49. User accessible data - traceability information**

| | | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Type[1] | Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| F | $C0 | ICTYPEID | ICTYPEID[7:0] | | | | | | | |
| F | $C1 | ICREVID | ICREVID[7:0] | | | | | | | |
| F | $C2 | ICMFGID | ICMFGID[7:0] | | | | | | | |
| F | $C3 | RESERVED | RESERVED | | | | | | | |
| F | $C4 | PN0 | PN0[7:0] | | | | | | | |
| F | $C5 | PN1 | PN1[7:0] | | | | | | | |
| F | $C6 | SN0 | SN[7:0] | | | | | | | |
| F | $C7 | SN1 | SN[15:8] | | | | | | | |
| F | $C8 | SN2 | SN[23:16] | | | | | | | |
| F | $C9 | SN3 | SN[31:24] | | | | | | | |
| F | $CA | SN4 | SN[39:36] = DEVICE_REV[3:0] | | | | SN[35:32] | | | |
| F | $CB | ASICWFR# | ASICWFR#[7:0] | | | | | | | |
| F | $CC | ASICWFR_X | ASICWFR_X[7:0] | | | | | | | |
| F | $CD | ASICWFR_Y | ASICWFR_Y[7:0] | | | | | | | |
| F | $CE | DVCREVID | RESERVED | | | | DVCREVID[3:0] | | | |
| F | $CF | CRC_F_C | LOCK_F_C | REGC_BLOCKID[2:0] | | | CRC_F_C[3:0] | | | |
| F | $D0 | ASICWLOT_L | ASICWLOT_L[7:0] | | | | | | | |
| F | $D1 | ASICWLOT_H | ASICWLOT_H[7:0] | | | | | | | |
| F | $D2 | TRNS1WFR_X | TRNS1WFR_X[7:0] | | | | | | | |
| F | $D3 | TRNS1WFR_Y | TRNS1WFR_Y[7:0] | | | | | | | |
| F | $D4 | TRNS1LOT_L | TRNS1LOT_L[7:0] | | | | | | | |
| F | $D5 | TRNS1LOT_H | TRNS1LOT_H[7:0] | | | | | | | |
| F | $D6-$D9 | RESERVED | RESERVED | | | | | | | |
| F | $DA | TRNS1WFR# | TRNS_ASSY_REV[2:0] | | | TRNS1WFR#[4:0] | | | | |
| F | $DB-$DE | RESERVED | RESERVED | | | | | | | |
| F | $DF | CRC_F_D | LOCK_F_D | REGD_BLOCKID[2:0] | | | CRC_F_D[3:0] | | | |
| UF0 | $E0 | USERDATA_0 | USERDATA_0[7:0] | | | | | | | |
| UF0 | $E1 | USERDATA_1 | USERDATA_1[7:0] | | | | | | | |
| UF0 | $E2 | USERDATA_2 | USERDATA_2[7:0] | | | | | | | |
| UF0 | $E3 | USERDATA_3 | USERDATA_3[7:0] | | | | | | | |
| UF0 | $E4 | USERDATA_4 | USERDATA_4[7:0] | | | | | | | |
| UF0 | $E5 | USERDATA_5 | USERDATA_5[7:0] | | | | | | | |
| UF0 | $E6 | USERDATA_6 | USERDATA_6[7:0] | | | | | | | |
| UF0 | $E7 | USERDATA_7 | USERDATA_7[7:0] | | | | | | | |
| UF0 | $E8 | USERDATA_8 | USERDATA_8[7:0] | | | | | | | |
| UF0 | $E9 | USERDATA_9 | USERDATA_9[7:0] | | | | | | | |
| UF0 | $EA | USERDATA_A | USERDATA_A[7:0] | | | | | | | |
| UF0 | $EB | USERDATA_B | USERDATA_B[7:0] | | | | | | | |
| UF0 | $EC | USERDATA_C | USERDATA_C[7:0] | | | | | | | |
| UF0 | $ED | USERDATA_D | USERDATA_D[7:0] | | | | | | | |
| UF0 | $EE | USERDATA_E | USERDATA_E[7:0] | | | | | | | |
| F | $EF | CRC_UF0 | LOCK_UF0 | REGE_BLOCKID[2:0] | | | CRC_UF0[3:0] | | | |
| UF1 | $F0 | USERDATA_10 | USERDATA_10[7:0] | | | | | | | |
| UF1 | $F1 | USERDATA_11 | USERDATA_11[7:0] | | | | | | | |
| UF1 | $F2 | USERDATA_12 | USERDATA_12[7:0] | | | | | | | |
| UF1 | $F3 | USERDATA_13 | USERDATA_13[7:0] | | | | | | | |
| UF1 | $F4 | USERDATA_14 | USERDATA_14[7:0] | | | | | | | |
| UF1 | $F5 | USERDATA_15 | USERDATA_15[7:0] | | | | | | | |
| UF1 | $F6 | USERDATA_16 | USERDATA_16[7:0] | | | | | | | |
| UF1 | $F7 | USERDATA_17 | USERDATA_17[7:0] | | | | | | | |

| | | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Type[1] | Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UF1 | $F8 | USERDATA_18 | USERDATA_18[7:0] | | | | | | | |
| UF1 | $F9 | USERDATA_19 | USERDATA_19[7:0] | | | | | | | |
| UF1 | $FA | USERDATA_1A | USERDATA_1A[7:0] | | | | | | | |
| UF1 | $FB | USERDATA_1B | USERDATA_1B[7:0] | | | | | | | |
| UF1 | $FC | USERDATA_1C | USERDATA_1C[7:0] | | | | | | | |
| UF1 | $FD | USERDATA_1D | USERDATA_1D[7:0] | | | | | | | |
| UF1 | $FE | USERDATA_1E | USERDATA_1E[7:0] | | | | | | | |
| F | $FF | CRC_UF1 | LOCK_UF1 | REGF_BLOCKID[2:0] | | | CRC_UF1[3:0] | | | |

1. *Memory Type Codes*
   *R - Readable Register with No OTP*
   *F – User Readable Register with OTP*
   *UF0 – One Time User Programmable OTP Location Region 0*
   *UF1 – One Time User Programmable OTP Location Region 1*
   *UF2 – One Time User Programmable OTP Location Region 2*
   *R/W – User Writable Register*

## 8.2 Register definitions

### 8.2.1 Rolling counter register (COUNT)

The count register is a read-only register which provides the current value of a free-running 8-bit counter derived from the primary oscillator. A 10-bit prescaler divides the primary oscillator frequency by 1000. Thus, the value in the register increases by one count every 100 µs and the counter rolls over every 25.6 ms.

This register is readable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 50. Rolling counter register (COUNT)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $00 | COUNT | COUNT[7:0] | | | | | | | |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.2.2 Device status registers (DEVSTATx)

The device status registers are read-only registers which contain device status information.

These registers are readable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 51. Device status registers (DEVSTATx)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $01 | DEVSTAT | CH0_ERR | CH1_ERR | COMM_ERR | MEMTEMP_ERR | SUPPLY_ERR | TESTMODE | DEVRES | DEVINIT |
| Reset Value | | 1 | 1 | 0 | 0 | x | 0 | 1 | 1 |
| $02 | DEVSTAT1 | VBUFUV_ERR | BUSINUV_ERR | VBUFOV_ERR | RESERVED | INTREGA_ERR | INTREG_ERR | INTREGF_ERR | CONT_ERR |
| Reset Value | | x | x | x | x | x | x | x | 0 |
| $03 | DEVSTAT2 | F_OTP_ERR | U_OTP_ERR | U_RW_ERR | U_W_ACTIVE | TEMP1_ERR | TEMP0_ERR | RESERVED | RESERVED |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | x | x |
| $04 | DEVSTAT3 | MISO_ERR | OSCTRAIN_ERR | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset Value | | 0 | 0 | x | x | x | x | x | x |

#### *8.2.2.1 Channel 0 error flag (CH0_ERR)*

The channel 0 error flag is set if a channel 0 specific error is present in the channel 0 DSP:

*CH0_ERR = CH0_STAT[SIGNALCLIP] | CH0_STAT[ST_INCMPLT] | CH0_STAT[OFFSET_ERR] | CH0_STAT[ST_ERROR]*

#### 8.2.2.2 *Channel 1 error flag (CH1_ERR)*

The channel 1 error flag is set if a channel 1 specific error is present in the channel 1 DSP:

*CH1_ERR = CH1_STAT[SIGNALCLIP] | CH1_STAT[ST_INCMPLT] |CH1_STAT[OFFSET_ERR] | CH1_STAT[ST_ERROR]*

#### 8.2.2.3 *Communication error flag (COMM_ERR)*

The communication error flag is set if any bit in DEVSTAT3 is set:

*COMM_ERR = MISO_ERR | OSCTRAIN_ERR*

#### 8.2.2.4 *Memory or temperature error flag (MEMTEMP_ERR)*

The memory error flag is set if any bit in DEVSTAT2 is set:

*MEMTEMP_ERR = F_OTP_ERR | U_OTP_ERR | U_RW_ERR | U_W_ACTIVE | TEMP1_ERR | TEMP0_ERR*

#### 8.2.2.5 *Supply error flag (SUPPLY_ERR)*

The supply error flag is set if any bit in DEVSTAT1 is set:

*SUPPLY_ERR = VBUFUV_ERR | BUSINUV_ERR | VBUFOV_ERR | INTREG_ERR | INTREGA_ERR | INTREGF_ERR | CONT_ERR*

A common timer is used for all error bits in the DEVSTAT1 register. If any bit in DEVSTAT1 is set, the timer is reset to $t_{UVOV\_RCV}$. When no supply errors are present, the timer is decremented until it reaches zero. This error is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Table 52. Supply error flag (SUPPLY_ERR).

**Table 52. Supply error flag (SUPPLY_ERR)**

| SUP_ERR_DIS | DSI3 and SPI operating modes (COMMTYPE =0, 2, 3 and 4) | PSI5 operating modes (COMMTYPE =1 and 5) | I²C operating modes (COMMTYPE =6, 7) |
|---|---|---|---|
| 0 | No Response until the supply monitor timer expires. The Sensor Data Field Error Code is transmitted for one response after the supply monitor timer expires.<br>A read of the DEVSTAT1 register clears all supply errors, using any communication interface or on a data transmission that includes the error in the status field, if and only if the timer has reached zero. | No transmissions occur if the timer is non-zero. The error is cleared when the timer reaches zero and normal transmissions resume. | No response until the supply monitor timer expires.<br>A read of the DEVSTAT1 register clears all supply errors. |
| 1 | No transmissions occur if the timer is non-zero. The error is cleared when the timer reaches zero and normal transmissions resume. | | |

#### 8.2.2.6 *Test mode (TESTMODE)*

The test mode bit is set if the device is in test mode. The TESTMODE bit can be cleared by a test mode operation or by a power cycle.

**Table 53. Test mode (TESTMODE)**

| TESTMODE | Operating mode |
|---|---|
| 0 | Test mode is not active |
| 1 | Test mode is active |

#### 8.2.2.7 *Device reset (DEVRES)*

The device reset bit is set following a device reset. This error is cleared by a read of the DEVSTAT register through any communication interface or on a data transmission that includes the error in the status field.

Table 54. **Device reset (DEVRES)**

| DEVRES | Error condition |
|---|---|
| 0 | Normal operation |
| 1 | Device reset occurred |

#### 8.2.2.8 *Device initialization (DEVINIT)*

The device initialization bit is set following either a device reset or a change to any of the following bits: CHx_CFG_U1[7:2] or CHx_CFG_U3[1:0]. The bit is cleared once sensor data is valid for read through one of the device communication inter-faces ($t_{POR\_DataValid}$).

*Note: Some LPF selections have a step response time longer than the $t_{POR\_DataValid}$ delay. If any of these filters are used, the filter may not have achieved the final value once DEVINIT is cleared.*

Table 55. **Device initialization (DEVINIT)**

| DEVINIT | Condition |
|---|---|
| 0 | Normal operation |
| 1 | Device Initialization in Process |

#### 8.2.2.9 *$V_{BUF}$ under-voltage error (VBUFUV_ERR)*

The $V_{BUF}$ under-voltage error bit is set if the VBUF voltage falls below the voltage specified in Section 7.4: Electrical characteristics - supply and I/O. See Section 8.4: Voltage regulators for details on the $V_{BUF}$ under-voltage monitor. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to $t_{UVOV\_RCV}$. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).

Table 56. **$V_{BUF}$ under-voltage error (VBUFUV_ERR)**

| VBUFUV_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | VBUF Voltage Low |

#### 8.2.2.10 *BUS IN under-voltage error (BUSINUV_ERR)*

The BUS IN under-voltage error bit is set if the BUS_IN voltage falls below the voltage specified in Section 7.4: Electrical characteristics - supply and I/O. See Section 8.4: Voltage regulators for details on the BUS IN under-voltage monitor. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to $t_{UVOV\_RCV}$. This bit is cleared based on the state of the SUP_ER-R_DIS bit in the DEVLOCK_WR register as shown in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).

Table 57. **BUS IN under-voltage error (BUSINUV_ERR)**

| BUSINUV_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | BUS_IN Voltage Low |

#### 8.2.2.11 *$V_{BUF}$ over-voltage error (VBUFOV_ERR)*

The $V_{BUF}$ over-voltage error bit is set if the VBUF voltage rises above the voltage specified in Section 7.4: Electrical characteristics - supply and I/O. See Section 8.4: Voltage regulators for details on the $V_{BUF}$ over-voltage monitor. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to $t_{UVOV\_RCV}$. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).

Table 58. $V_{BUF}$ over-voltage error (VBUFOV_ERR)

| VBUFUV_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | VBUF Voltage High |

#### 8.2.2.12 *Internal analog regulator voltage out of range error (INTREGA_ERR)*

The internal analog regulator voltage out of range error bit is set if the internal analog regulator voltage falls outside expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to $t_{UVOV\_RCV}$. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).

Table 59. Internal analog regulator voltage out of range error (INTREGA_ERR)

| INTREGA_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | Internal Analog Regulator Voltage Out of Range |

#### 8.2.2.13 *Internal digital regulator voltage out of range error (INTREG_ERR)*

The internal digital regulator voltage out of range error bit is set if the internal digital regulator voltage falls outside expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to $t_{UVOV\_RCV}$. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).

Table 60. Internal digital regulator voltage out of range error (INTREG_ERR)

| INTREG_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | Internal Digital Regulator Voltage Out of Range |

#### 8.2.2.14 *Internal OTP regulator voltage out of range error (INTREGF_ERR)*

The internal OTP regulator voltage out of range error bit is set if the internal OTP regulator voltage falls outside expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to $t_{UVOV\_RCV}$. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).

Table 61. Internal OTP regulator voltage out of range error (INTREGF_ERR)

| INTREGF_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | Internal OTP Regulator Voltage Out of Range |

#### 8.2.2.15 *Continuity monitor error (CONT_ERR)*

The continuity monitor passes a low current through a connection around the perimeter of the device and monitors the continuity of the connection. The error bit is set if a discontinuity is detected in the connection. A common timer is used for all error bits in the DEVSTAT1 register. If the CONT_ERR bit is set, the timer is reset to $t_{UVOV\_RCV}$. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).

Table 62. **Continuity monitor error (CONT_ERR)**

| CONT_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | Error detected in the continuity of the monitor circuit |

#### 8.2.2.16 *ST OTP array error (F_OTP_ERR)*

The factory OTP array error bit is set if a fault is detected in the factory OTP array. This error is cleared by a device reset. See Section 8.2.15.2: PSI5 error latching enable bit (PSI5_ERRLATCH) for details on a method to disable the automatic clearing of this error in PSI5 mode.

Table 63. **ST OTP array error (F_OTP_ERR)**

| F_OTP_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | Error Detected in the Factory OTP Array |

#### 8.2.2.17 *User OTP array error (U_OTP_ERR)*

The user OTP array error bit is set if a fault is detected in the user OTP array. This error is cleared by a device reset. See Section 8.2.15.2: PSI5 error latching enable bit (PSI5_ERRLATCH) for details on a method to disable the automatic clearing of this error in PSI5 mode.

Table 64. **User OTP array error (U_OTP_ERR)**

| U_OTP_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | Error Detected in the User OTP Array |

#### 8.2.2.18 *User read/write array error (U_RW_ERR)*

When ENDINIT is set, an error detection is enabled for all user writable registers. The error detection code is continuously calculated on the user writable registers and verified against a previously calculated error detection code. If a mismatch is detected in the error detection, the U_RW_ERR bit is set. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field. See Section 8.2.15.2: PSI5 error latching enable bit (PSI5_ERRLATCH) for details on a method to disable the automatic clearing of this error in PSI5 mode.

Table 65. **User read/write array error (U_RW_ERR)**

| U_RW_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | Error Detected in the User Read/Write Array |

#### 8.2.2.19 *User OTP write in process status bit (U_W_ACTIVE)*

The user OTP write in process status bit is set if a user initiated write to OTP is currently in process. The U_W_ACTIVE bit is automatically cleared once the write to OTP is complete.

Table 66. **User OTP write in process status bit (U_W_ACTIVE)**

| U_W_ACTIVE | Status condition |
|---|---|
| 0 | No OTP Write in Process |
| 1 | OTP Write in Process |

#### 8.2.2.20 *Channel 1 temperature sensor error (TEMP1_ERR)*

The channel 1 temperature error bit is set if an over or under temperature condition exists on channel 1. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field. See Section 8.2.15.2: PSI5 error latching enable bit (PSI5_ERRLATCH) for details on a method to disable the automatic clearing of this error in PSI5 mode.

**Table 67. Channel 1 temperature sensor error (TEMP1_ERR)**

| TEMP1_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | Over- or Under-Temperature error condition detected |

#### 8.2.2.21 *Channel 0 temperature sensor error (TEMP0_ERR)*

The channel 0 temperature error bit is set if an over or under temperature condition exists on channel 0. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field. See Section 8.2.15.2: PSI5 error latching enable bit (PSI5_ERRLATCH) for details on a method to disable the automatic clearing of this error in PSI5 mode.

**Table 68. Channel 0 temperature sensor error (TEMP0_ERR)**

| TEMP0_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | Over- or Under-Temperature error condition detected |

#### 8.2.2.22 *SPI MISO data mismatch error flag (MISO_ERROR)*

In SPI mode, the MISO data mismatch flag is set when a MISO Data mismatch fault occurs as specified in Section 11.5.7: SPI data output verification error. The MISO_ERROR bit is cleared by a read of the DEVSTAT3 register through any communication interface, or by a status transmission including the error status through the SPI.

**Table 69. SPI MISO data mismatch error flag (MISO_ERROR)**

| MISO_ERROR | Error condition |
|---|---|
| 0 | Normal operation |
| 1 | MISO Data Mismatch |

#### 8.2.2.23 *Oscillator training error (OSCTRAIN_ERR)*

The oscillator training error bit is set if an error detected in either the oscillator training settings, or the master communication timing. See Section 8.5.2: Oscillator training error handling. Once the error condition is corrected, the OSCTRAIN_ERR bit is cleared after a read of the OSCTRAIN_ERR bit through any communication interface, or by a status transmission including the error status through any communication interface.

**Table 70. Oscillator training error (OSCTRAIN_ERR)**

| OSCTRAIN_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | Oscillator Training Error. See Section 8.5.2: Oscillator training error handling |

### 8.2.3 Communication protocol revision register (COMMREV)

The communication protocol revision register is a read-only register which contains the revision for the communication protocol used.

This register is readable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 71. Communication protocol revision register (COMMREV)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $05 | COMMREV | 0 | 0 | 0 | 0 | COMMREV[3:0] | | | |
| Reset Value for DSI3 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Reset Value for PSI5 | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| Reset Value for SPI | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset Value for I²C | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

*Note: The response to a register write of the COMMREV register is a valid response with the register contents equal to 0x00.*

### 8.2.4 Margin read status register (MREAD_STAT)

The Margin Read Status register is a read-only register which contains the status for the user enabled OTP margin read test.

This register is readable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 72. Margin read status register (MREAD_STAT)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $06 | MREAD_STAT | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | MARGIN_RD_ACT | MARGIN_RD_ERR |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

*Note: The user enabled OTP margin read test is not intended for use in normal operation. It is intended for use only after user OTP programming during manufacturing.*

#### *8.2.4.1 Margin read active status (MARGIN_RD_ACT)*

The margin read active status bit is set if a user enabled OTP margin read test is in process. The status bit is automatically cleared when the OTP margin read test is complete. See Section 8.2.7.1: Margin read enable bit (MARGIN_RD_EN) for details regarding the user enabled OTP margin read test.

**Table 73. Margin read active status (MARGIN_RD_ACT)**

| MARGIN_RD_ACT | Condition |
|---|---|
| 0 | No Margin Read Test is in Process |
| 1 | Margin Read Test is in Process |

#### *8.2.4.2 Margin read error status (MARGIN_RD_ERR)*

The margin read error status bit is set if a user enabled OTP margin read test has failed. The margin read error status bit is cleared on a read of the MREAD_STAT register. The margin read error status bit has no impact on device operation or performance. See Section 8.2.7.1: Margin read enable bit (MARGIN_RD_EN) for details regarding the user enabled OTP margin read test.

**Table 74. Margin read error status (MARGIN_RD_ERR)**

| MARGIN_RD_ERR | Condition |
|---|---|
| 0 | No Margin Read Test Failure |
| 1 | Margin Read Test Failure |

### 8.2.5 Temperature register (TEMPERATURE)

The temperature register is a read-only register which provides a temperature value from the channel 0 temperature sensor. The temperature value is specified in Section 7.5: Electrical characteristics - temperature sensor signal chain.

Note, the device is only guaranteed to operate within the temperature limits specified in Section 7: Electrical characteristics. This includes the performance of the temperature register values.

This register is readable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 75. Temperature register (TEMPERATURE)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $0E | TEMPERATURE | TEMP[7:0] | | | | | | | |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.2.6 Device lock register (DEVLOCK_WR)

The device lock register is a user programmed read/write register which contains the ENDINIT bit and reset control bits.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 76. Device lock register (DEVLOCK_WR)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $10 | DEVLOCK_WR | ENDINIT | RESERVED | RESERVED | RESERVED | SUP_ERR_DIS | RESERVED | RESET[1:0] | |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### *8.2.6.1 End initialization bit (ENDINIT)*

The ENDINIT bit is a control bit used to indicate that the user has completed all device and system level initialization tests. Once the ENDINIT bit is set, writes to all writable register bits are inhibited except for the DEVLOCK_WR register. Once set, the ENDINIT bit can only be cleared by a device reset.

When ENDINIT is set, the following occurs:

- An error detection is enabled for all user writable registers. The error detection code is continuously calculated on the user writable registers and verified against a previously calculated error detection code.
- The offset cancellation filter is forced to its final stage.
- Self-test is disabled and inhibited.
- Register Writes are inhibited with the exception of the RESET[1:0] bits in the DEVLOCK_WR register.

In DSI3 mode, when the ENDINIT bit is set, the device is forced to PDCM according to the device settings and no longer responds to CRM commands.

In PSI5 mode, the ENDINIT bit is automatically set when the device exits Initialization Phase 3.

#### *8.2.6.2 Supply error reporting disable bit (SUP_ERR_DIS)*

The supply error disable bit allows the user to disable reporting of the supply errors in the DSI3 PDCM and SPI status fields. See Section 8.2.2.5: Supply error flag (SUPPLY_ERR).

#### *8.2.6.3 Reset control bits (RESET[1:0])*

In DSI3 mode, SPI mode, I²C mode or PSI5 mode, a series of three consecutive register write operations to the reset control bits results in a device reset. To reset the device, the following register write operations must be performed in consecutive commands and in the order shown in Table 77. Reset control bits (RESET[1:0]) or the device will reset.

**Table 77. Reset control bits (RESET[1:0])**

| Register write to DEVLOCK_WR | RES_1 | RES_0 | Effect |
|---|---|---|---|
| Register Write 1 | 0 | 0 | No Effect |
| Register Write 2 | 1 | 1 | No Effect |
| Register Write 3 | 0 | 1 | Device RESET |

The response to a register write returns the new register value, including the values written to the RESET[1:0] bits. After the third Register Write command, the device initiates a reset and therefore does not transmit a response to this command or an Acknowledge in I²C mode. The response to a register read returns '00' for RESET[1:0] and terminates the reset sequence. The reset control bits are not included in the read/write array error detection.

### 8.2.7 Write OTP enable register

The write OTP enable register is a user programmed read/write register that allows the user to write the contents of the user programmed OTP array mirror registers to the OTP registers. This register is included in the user read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 78. Write OTP enable register**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $11 | WRITE_OTP_EN | UOTP_WR_INIT | MARGIN_RD_EN | RESERVED | RESERVED | EX_COMMTYPE | EX_PADDR | UOTP_REGION[1:0] | |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.7.1 *Margin read enable bit (MARGIN_RD_EN)*

The margin read enable bit initiates an OTP margin read test for all user programmable OTP regions: UF2, UF0, and UF1. The user enabled OTP margin read test is not intended for use in normal operation. It is intended for use only after user OTP programming during manufacturing.

The procedure for completing an OTP margin read test is shown in step 1. through step 7.:

1. Read the MREAD_STAT register to confirm that the MARGIN_RD_ACT and MARGIN_RD_ERR bits are both cleared.
2. Write 0x40 to the WRITE_OTP_EN register to set the MARGIN_RD_EN bit. This initiates the OTP margin read test which completes the sequence listed in steps a. through i..
   a. The UF2 block is read. The ECC is checked for double bit errors and the CRC is verified. If an ECC error or CRC error exists or if UF2 block is unlocked, the MARGIN_RD_ERR bit is set and the test is terminated.
   b. A margin read low test is run with the read threshold reduced by 25 %. The data is checked against the expected values in the mirror registers. If a double bit ECC error or data comparison mismatch occurs, the MARGIN_RD_ERR bit is set and the test is terminated.
   c. A margin read high test is run with the read threshold increased by 25 %. The data is checked against the expected values in the mirror registers. If a double bit error or data comparison mismatch occurs, the MARGIN_RD_ERR bit is set and the test is terminated.
   d. The UF0 block is read. The ECC is checked for double bit errors and the CRC is verified. If an ECC error or CRC error exists or if UF0 block is unlocked, the MARGIN_RD_ERR bit is set and the test is terminated.
   e. A margin read low test is run with the read threshold reduced by 25 %. The data is checked against the expected values in the mirror registers. If a double bit ECC error or data comparison mismatch occurs, the MARGIN_RD_ERR bit is set and the test is terminated.
   f. A margin read high test is run with the read threshold increased by 25 %. The data is checked against the expected values in the mirror registers. If a double bit error or data comparison mismatch occurs, the MARGIN_RD_ERR bit is set and the test is terminated.
   g. The UF1 block is read. The ECC is checked for double bit errors and the CRC is verified. If an ECC error or CRC error exists or if UF1 block is unlocked, the MARGIN_RD_ERR bit is set and the test is terminated.
   h. A margin read low test is run with the read threshold reduced by 25 %. The data is checked against the expected values in the mirror registers. If a double bit ECC error or data comparison mismatch occurs, the MARGIN_RD_ERR bit is set and the test is terminated.
   i. A margin read high test is run with the read threshold increased by 25 %. The data is checked against the expected values in the mirror registers. If a double bit error or data comparison mismatch occurs, the MARGIN_RD_ERR bit is set and the test is terminated.
3. Read the MREAD_STAT register to confirm that the MARGIN_RD_ACT bit is set and the MARGIN_RD_ERR bit is cleared.
4. Delay 1.5 ms minimum.
5. Read the MREAD_STAT register to confirm that the MARGIN_RD_ACT bit is cleared. Check the state of the MARGIN_RD_ERR bit.
   – If the MARGIN_RD_ERR bit is cleared, the margin read test passed.
   – If the MARGIN_RD_ERR bit is set, the margin read test failed.
6. When the test is complete, the MARGIN_RD_EN bit is cleared.
7. When the test is complete and the MREAD_STAT register has been read, the MARGIN_RD_ACT and the MARGIN_RD_ERR bit are cleared.

The user enabled OTP margin read test can only be enabled when the ENDINIT bit is not set.

#### 8.2.7.2 *Write OTP enable and programming bits*

Register writes executed by the user to the user programmed OTP array only update the mirror register contents for the OTP array, not the actual OTP registers. To copy the values to the actual OTP registers, a write must be executed to the WRITE_OTP_EN register with the UOTP_WR_INIT bit set. The state of the UOTP_REGION[1:0], the EX_COMMTYPE, and the EX_PADDR bits in the command determine which region of OTP are written as shown in Table 79. Write OTP enable and programming bits.

**Table 79. Write OTP enable and programming bits**

| EX_COMMTYPE | EX_PADDR | UOTP_REGION[1] | UOTP_REGION[0] | OTP write operation | Special conditions |
|---|---|---|---|---|---|
| x | x | 0 | 0 | Write the current contents of the UF0 registers to OTP | |
| x | x | 0 | 1 | Write the current contents of the UF1 registers to OTP | |
| 0 | 0 | 1 | 0 | Write the current contents of the UF2 registers to OTP, including the COMMTYPE register and the PHYSADDR register | |
| 0 | 1 | 1 | 0 | Write the current contents of the UF2 registers to OTP, including COMMTYPE and excluding PHYSADDR. | PHYSADDR = 0x00 after OTP Write |
| 1 | 0 | 1 | 0 | Write the current contents of the UF2 registers to OTP, excluding COMMTYPE and including PHYSADDR. | User must not overwrite COMMTYPE |
| 1 | 1 | 1 | 0 | Write the current contents of the UF2 registers to OTP, excluding COMMTYPE and excluding PHYSADDR. | User must not overwrite COMMTYPE<br>PHYSADDR = 0x00 after OTP Write |
| x | x | 1 | 1 | Reserved for Future Use | |

The UF0 and UF1 user OTP regions as well as the ST programmed F OTP regions share common mirror registers. For this reason, writes to the OTP for each region must be completed independently according to the procedure below.

Depending upon the operating mode used, the user needs to write the UF2 values to OTP either with or without the PHYSADDR register and the COMMTYPE register being written. If Discovery Mode or switch connected daisy chain mode is used, the PHYSADDR register must remain un-programmed (0x0000). If a pre-programmed bus mode is used, the PHYSADDR register must be programmed to a non-zero value. To support these two user modes, the EX_PADDR bit is used as described in Table 79. Write OTP enable and programming bits.

Once a region is written using the OTP Write sequence, the LOCK_Uxx bit in the appropriate CRC_xxx register is automatically set, locking the array from future writes. Once a region is locked, an error detection is activated to detect changes to the register values. Register values in the UF2 region can be over-written using register write commands, but no new values can be written to the OTP.

The procedure for writing to the user OTP array UF0 and UF1 regions is:

1. Read the appropriate CRC_UFx register and confirm the LOCK_Uxx bit is not set.
2. Write the desired values to the user array registers for only the region to be written using the procedures in Section 8.2.10: UF region selection registers (UF_REGION_x).
   – The user must take care to ensure that the proper data is written to each region. If a register write is executed to a new region, the base address changes to the new region. The previous data written to the register block remains in the shared registers and is written to OTP if the Write OTP sequence is completed.
3. Execute a write to the WRITE_OTP_EN register with the appropriate bits set for the desired region to program.
   – Once the WRITE_OTP_EN register write is completed, a CRC is calculated for the data to be written to the region, the register values are written to OTP and the region is locked from future writes. The UOTP_WR_INIT bit remains set.
4. Delay $t_{OTP\_WRITE\_MAX}$ to allow the device to complete the writes to OTP.
5. Verify that the OTP write successfully completed by reading back all of the OTP registers using Register Read commands as defined in Section 8.2.10: UF region selection registers (UF_REGION_x).
6. Repeat steps 1 through 4 for all regions to be programmed.

The procedure for writing to the user OTP array UF2 region is:

1. Read the CRC_UF2 register and confirm the LOCK_UF2 bit is not set.
2. Write the desired values to the user array registers.
3. Execute a write to the WRITE_OTP_EN register with region 2 selected and the EX_COMMTYPE and EX_PADDR bit set as desired.
   – Once the WRITE_OTP_EN register write is completed, a CRC is calculated for the data to be written to the region, the register values are written to OTP and the region is locked from future writes. The UOTP_WR_INIT bit remains set.
4. Delay $t_{OTP\_WRITE\_MAX}$ to allow the device to complete the writes to OTP and an automatic read of the UF2 registers from OTP.

5. Verify that the OTP write successfully completed by reading back all of the OTP registers using Register Read commands.

### 8.2.8 Bus switch control register (BUSSW_CTRL)

The bus switch control register is a user programmed read/write register which controls the state of the bus switch output driver. This register is included in the user read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 80. Bus switch control register (BUSSW_CTRL)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $12 | BUSSW_CTRL | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | BUSSW_CTRL[1:0] | |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The BUSSW_CTRL bit controls the state of the BUSSW_L pin.

**Table 81. BUSSW_L pin state**

| BUSSW_CTRL[1] | BUSSW_CTRL[0] | BUSSW_L Pin State |
|---|---|---|
| 0 | 0 | High Impedance. An external pullup or pulldown resistor is required if an external switch is connected |
| 0 | 1 | High Impedance. An external pullup or pulldown resistor is required if an external switch is connected |
| 1 | 0 | Active Low. |
| 1 | 1 | Active High. |

Note: In DSI3 and PSI5 DPM modes, the bus switch is activated upon receipt of the register write command. The bus switch activation may impact the current on the bus and cause corruption of the register write response.

### 8.2.9 PSI5 test register (PSI5_TEST)

The PSI5 test register is a user read/write register that contains the PSI5 test control. This register is included in the user read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 82. PSI5 test register (PSI5_TEST)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $13 | PSI5_TEST | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | PSI5_TEST |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### *8.2.9.1 PSI5 test bit (PSI5_TEST)*

If PSI5 mode is not enabled in the COMMTYPE, the PSI5 test bit enables a single PSI5 command receive and response transmission to allow for the PSI5 transceiver to be tested in other modes.

When the PSI5_TEST bit is set, the device and system proceed through following process.

1. The device switches the BUS_I transceiver to PSI5 mode.
2. The system holds the BUS_I node constant for 2 ms minimum to allow the BUS_I command receiver to capture the average voltage.
3. The system must transmit a sync pulse meeting the specifications in Section 7: Electrical characteristics.

4. The device transmits a response to the sync pulse with the following configuration:
   a. The sync pulse is pulled down as configured by the SYNC_PD bit in the PSI5_CFG register.
   b. The response starts in the time slot selected in the PDCM_RSPST0 register.
   c. The response bit time is configured in the CHIPTIME register.
   d. The response current is configured by the PSI5_ILOW bit in the PSI5_CFG register.
   e. Two start bits are transmitted as specified in Section 10.3.2: PSI5 data transmission.
   f. 10-bits of data equal to 0x2AA are transmitted.
   g. Error checking bits are transmitted as configured by the P_CRC bit in the PSI5_CFG register.
5. Once the transmission is complete, the PSI5_TEST bit is cleared and the device returns to the communication mode as defined in the COMMTYPE register.

If the bit is set from DSI3 mode, this process occurs once the device has replied to the write message, regardless of whether or not the reply attempted was successful.

If the bit is set from SPI mode, the process occurs once the PSI5_TEST bit is set with no SPI reply necessary.

If the bit is set from I²C mode, the process occurs once the PSI5_TEST bit is set with no I²C reply necessary.

If PSI5 mode is enabled in the COMMTYPE register, this bit has no impact on device operation or performance.

### 8.2.10 UF region selection registers (UF_REGION_x)

The UF region load register is a user read/write register that contains the control bits for the UF0 and UF1 regions to be accessed. This register is included in the user read/write array error detection. The UF region active register is a read-only register that contains the status bits for the UF0 and UF1 regions to be accessed.

The UF_REGION_W register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode. The UF_REGION_R register is readable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming mode.

**Table 83. UF region selection registers (UF_REGION_x)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $14 | UF_REGION_W | REGION_LOAD[3:0] | | | | 0 | 0 | 0 | 0 |
| $15 | UF_REGION_R | REGION_ACTIVE[3:0] | | | | 0 | 0 | 0 | 0 |
| Reset Value | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

The user OTP regions UF0, UF1, and F share a block of 16 registers. Prior to reading the registers via any communication interface, the user must ensure that the desired OTP registers are loaded into the readable registers. To ensure proper reading of the UF0, UF1 and F registers, follow this procedure:

1. Write the desired address range to be read to the REGION_LOAD[3:0] bits in the UF_REGION_W register using one of the communication interfaces available via the COMMTYPE register.

**Table 84. Region load bits**

| REGION_LOAD[3:0] | | | | OTP register addresses loaded into the readable registers |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Not Applicable |
| 0 | 0 | 0 | 1 | Not Applicable |
| 0010 through 1001 | | | | RESERVED |
| 1 | 0 | 1 | 0 | Address Range $A0 through $AF |
| 1 | 0 | 1 | 1 | Address Range $B0 through $BF |
| 1 | 1 | 0 | 0 | Address Range $C0 through $CF |
| 1 | 1 | 0 | 1 | Address Range $D0 through $DF |
| 1 | 1 | 1 | 0 | Address Range $E0 through $EF |
| 1 | 1 | 1 | 1 | Address Range $F0 through $FF |

2. Delay a minimum of $t_{SSN\_UF01}$.

3. Optional: Execute a register read of the UF_REGION_R register and confirm the REGION_ACTIVE[3:0] bits match the values written to the REGION_LOAD[3:0] bits in the UF_REGION_W register.

**Table 85. Region active bits**

| REGION_ACTIVE[3:0] | | | | OTP register addresses loaded into the readable registers |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Load of OTP registers is in process |
| 0 | 0 | 0 | 1 | The contents of the shared registers has been over-written by the user |
| 0010 through 1001 | | | | Not Applicable |
| 1 | 0 | 1 | 0 | Address Range $A0 through $AF |
| 1 | 0 | 1 | 1 | Address Range $B0 through $BF |
| 1 | 1 | 0 | 0 | Address Range $C0 through $CF |
| 1 | 1 | 0 | 1 | Address Range $D0 through $DF |
| 1 | 1 | 1 | 0 | Address Range $E0 through $EF |
| 1 | 1 | 1 | 1 | Address Range $F0 through $FF |

4. Execute a Register Read of the desired registers from the UF0, UF1, or F register section. Complete all desired Register Reads of the selected UF Region.
5. Repeat steps 1. through 4. for the next desired UF region to read.

Notes:

- The user must take care to ensure that the desired registers are addressed. For example, if the REGION_LOAD bits are set to 0xA and the user executes a read of address $C2, the contents of registers $A2 are transmitted. No error detection is included other than a read of the REGION_ACTIVE bits.
- For COMMTYPE options with multiple protocol options (COMMTYPE = '000' or '001'), no error detection is included other than a read of the REGION_ACTIVE bits. The user must take care to ensure that the REGION_LOAD, bits are not inadvertently changed by an alternative protocol while executing register reads.
- In DSI3, BDM, writes to registers are inhibited. For this reason, reads of the UF0, UF1, and F registers will only be possible for the region selected by the REGION_ACTIVE bits at the time ENDINIT is set.
- In SPI and I²C mode, once the ENDINIT bit is set, writes to registers other than the RESET[1:0] bits are inhibited. For this reason, reads of the UF0, UF1, and F registers will only be possible for the region selected by the REGION_ACTIVE bits at the time ENDINIT is set.

## 8.2.11 Communication type register (COMMTYPE)

The communication type register is a user programmed read/write register which contains user-specific configuration information for communication type. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, and I²C mode. In PSI5 Programming Mode, the value of this register must not be changed or a U_OTP Memory occurs.

**Table 86. Communication type register (COMMTYPE)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $16 | COMMTYPE | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | COMMTYPE[2:0] | | |
| Unprogrammed OTP Value: NXLS95xxx | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Programmed OTP Value: NXLS96xxx | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

### *8.2.11.1 Communication type (COMMTYPE[2:0])*

The communication type bits select the available protocols for the device as shown in Table 87. Communication type (COMMTYPE[2:0]).

**Table 87. Communication type (COMMTYPE[2:0])**

| COMMTYPE [2:0] | | | Available communication protocols | | | | Arming function availability | BUS_I undervoltage detection |
|---|---|---|---|---|---|---|---|---|
| | | | DSI3[1] | PSI5[2] | 32-bit SPI[3] | I²C[4] | | |
| 0 | 0 | 0 | X | | X | | Enabled based on ARM_CFG[2:0] | Disabled |
| 0 | 0 | 1 | | X | X | | Enabled based on ARM_CFG[2:0] | Disabled |
| 0 | 1 | 0 | | | X | | Enabled based on ARM_CFG[2:0] | Disabled |
| 0 | 1 | 1 | X | | | | Disabled | Enabled |
| 1 | 0 | 0 | | | X | | Enabled based on ARM_CFG[2:0] | Disabled |
| 1 | 0 | 1 | | X | | | Disabled | Enabled |
| 1 | 1 | 0 | | | | X | Disabled | Disabled |
| 1 | 1 | 1 | | | | X | Disabled | Disabled |

1. *See Section 9*
2. *See Section 10*
3. *See Section 11*
4. *See Section 12*

When writing to this register, care must be taken to prevent from inadvertently disabling the desired communication mode. Communication mode register value changes which disable a protocol, including writes to OTP, will not take effect until a device reset to prevent from disabling a necessary communication method. Table 88. COMMTYPEs and effect on device describes how communication mode register changes are handled.

**Table 88. COMMTYPEs and effect on device**

| Original COMMTYPE | New COMMTYPE | Device effect |
|---|---|---|
| 0 (DSI3 / SPI) | 1 (PSI5 / SPI) | A protocol change does not occur until a device reset (assuming the OTP is programmed). |
| 0 (DSI3 / SPI) | 2, 3, 4, 5 (SPI, DSI3 or PSI5) | A protocol change does not occur until a device reset (assuming the OTP is programmed). |
| 0 (DSI3 / SPI) | 6, 7 (I²C) | A protocol change does not occur until a device reset (assuming the OTP is programmed). |
| 1 (PSI5 / SPI) | 5 (PSI5) | A protocol change does not occur until a device reset (assuming the OTP is programmed). |
| 2, 3, 4, 5 (SPI) | Any | No protocol change occurs. |
| 6, 7 (I²C) | Any | No protocol change occurs. |

Notes:

- In PSI5 / SPI mode (COMMTYPE = 1), SPI transactions are ignored by the device until PSI5 initialization 3 is complete. SPI Test Mode Entry is not restricted.
- In PSI5 / SPI mode (COMMTYPE = 1), only SPI read register transactions are available.
- In DSI3 / SPI mode (COMMTYPE = 0) and PSI5 / SPI mode (COMMTYPE = 1), registers accesses by protocol are completed in the order received. Care must be taken to prevent from incorrect addressing of the F, UF0, and UF1 registers.
- In SPI only mode and in I²C only mode, the BUS_I undervoltage detection is disabled to allow for 3.3 V system operation. the $V_{BUF}$ undervoltage detection replaces the BUS_I undervoltage detection.
- If the COMMTYPE register is pre-programmed in OTP to a specific communication type, the user must prevent writes to this register when writing the UF2 register to OTP. If a pre-programmed COMMTYPE register is over-written and then written to OTP, the UF2 CRC verification will fail.

### 8.2.12 Physical address register (PHYSADDR)

The physical address register is a user programmed OTP register which contains the physical address of the slave for use in DSI3. This register is included in the read/write array error detection. If the physical address stored in the OTP array is zero, the address is assigned either during Discovery Mode or during Command and Response Mode.

If the physical address stored in the OTP array is non-zero, the device ignores Discovery Mode and uses the programmed physical address for Command and Response Mode. The physical address register value can be changed by a Command and Response Mode register write command. However, if the UF2 region is locked, the value will always be reset to the OTP array value after a reset.

In SPI mode, I²C mode and PSI5 mode, the PHYSADDR register is readable and writable, but has no impact on device operation or performance.

**Table 89. Physical address register (PHYSADDR)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $18 | PHYSADDR | 0 | 0 | 0 | 0 | PADDR[3:0] | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.2.13 Source identification registers (SOURCEID_x)

The source identification registers are user programmed read/write registers which contain the source identification information used for DSI3 PDCM, PSI5 mode, and SPI Mode. These registers are included in the read/write array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 90. Source identification registers (SOURCEID_x)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $1A | SOURCEID_0 | SID0_EN | PDCMFORMAT[2:0] | | | SOURCEID_0[3:0] | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx Unprogrammed Default PSI5 Mode | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| $1B | SOURCEID_1 | SID1_EN | RESERVED | RESERVED | RESERVED | SOURCEID_1[3:0] | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $1C | SOURCEID_2 | SID2_EN | RESERVED | RESERVED | RESERVED | SOURCEID_2[3:0] | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx Unprogrammed Default PSI5 Mode | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $1D | SOURCEID_3 | SID3_EN | RESERVED | RESERVED | RESERVED | SOURCEID_3[3:0] | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.13.1 *Data source enable bits (SIDx_EN)*

The SIDx_EN bits enable the data source for the associated source identification as described in Section 8.2.13.3: Source identification (SOURCEID_x).

#### 8.2.13.2 *PDCM format control bits (PDCMFORMAT[2:0])*

In DSI3 mode, the PDCM format control bits set the PDCM field sizes as shown in Table 91. PDCM format control bits (PDCMFORMAT[2:0]). See Section 9.4.2: DSI3 periodic data collection mode response transmission for PDCM response format details.

**Table 91. PDCM format control bits (PDCMFORMAT[2:0])**

| PDCMFORMAT[2:0] | | | Source ID field size (Bits) | Keep alive counter field size (Bits) | Status field size (Bits) | Data field size (Bits) | Total including CRC (Bits) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 2 | 4 | 10 | 24 |
| 0 | 0 | 1 | 4 | 2 | 4 | 10 | 28 |
| 0 | 1 | 0 | 0 | 0 | 4 | 12 | 24 |
| 0 | 1 | 1 | 4 | 0 | 4 | 12 | 28 |
| 1 | 0 | 0 | 0 | 2 | 0 | 10 | 20 |
| 1 | 0 | 1 | 0 | 0 | 0 | 16 | 24 |
| 1 | 1 | 0 | 0 | 0 | 4 | 16 | 28 |
| 1 | 1 | 1 | 4 | 0 | 4 | 16 | 32 |

In PSI5 mode, the PDCM format control bits set the PSI5 response format as shown in Table 92. PDCM format control bits. See Section 10.3.2: PSI5 data transmission for PSI5 response format details. Note: the data field size applies to all modes except Programming Mode which has a fixed size of 10 bits. The user must take care to prevent from combining incompatible data field sizes and transmission times.

**Table 92. PDCM format control bits**

| PDCMFORMAT[2:0] | | | Data field size (Bits) |
|---|---|---|---|
| 0 | x | x | 10 |
| 1 | x | x | 16 |

In SPI and I²C mode, the PDCMFORMAT bits are readable and writable, but have no impact on device operation or performance.

#### 8.2.13.3 *Source identification (SOURCEID_x)*

In SPI mode, the SOURCEID field in the SPI command is compared against the values in the SOURCEID_x registers. If the SOURCEID field matches one of the values in the SOURCEID_x registers and the SIDx_EN bit is set for that register, the sensor data for that SOURCEID is transmitted as shown in Table 93. SPI source identification (SOURCEID_x). If more than one enabled SOURCEID_x register value matches the SOURCEID field in the SPI command a SPI sensor data request error response is transmitted. If no enabled SOURCEID_X register value matches the SOURCEID field in the SPI command a SPI sensor data request error response is transmitted.

**Table 93. SPI source identification (SOURCEID_x)**

| Source ID | Source ID enable (SIDx_EN) | Transmitted data |
|---|---|---|
| SOURCEID_0 | 0 | SPI Error Response |
| | 1 | CH0_SNSDATA0 |
| SOURCEID_1 | 0 | SPI Error Response |
| | 1 | CH0_SNSDATA1 |
| SOURCEID_2 | 0 | SPI Error Response |
| | 1 | CH1_SNSDATA0 |
| SOURCEID_3 | 0 | SPI Error Response |
| | 1 | CH1_SNSDATA1 |

In DSI3 mode, if the SIDx_EN bit in the SOURCEID_x register is set, the associated SOURCEID value is transmitted in the SOURCEID field of PDCM mode using the associated transmission time shown in Table 94. DSI3 source identification (SOURCEID_x).

**Table 94. DSI3 source identification (SOURCEID_x)**

| Source ID | Source ID enable (SIDx_EN) | Transmission time[1] | Transmitted data[2] |
|---|---|---|---|
| SOURCEID_0 | 0 | NA | NA |
| | 1 | PDCM_RSPST0 | CH0_SNSDATA0 |
| SOURCEID_1 | 0 | NA | NA |
| | 1 | PDCM_RSPST1 | CH0_SNSDATA1 |
| SOURCEID_2 | 0 | NA | NA |
| | 1 | PDCM_RSPST2 | CH1_SNSDATA0 |
| SOURCEID_3 | 0 | NA | NA |
| | 1 | PDCM_RSPST3 | CH1_SNSDATA1 |

1. *See Section 8.2.18.1*
2. *See Section 8.2.25.2 and See Section 8.2.25.3*

In PSI5 mode, the SOURCEID_x register SIDx_EN bit values control data transmissions as shown in Table 95. PSI5 source identification (SOURCEID_x). The SOURCEID_x bits have no effect in PSI5 mode.

**Table 95. PSI5 source identification (SOURCEID_x)**

| Source ID | Source ID enable (SIDx_EN) | Asynchronous mode | | Synchronous mode | | Daisy chain mode | |
|---|---|---|---|---|---|---|---|
| | | Transmission time | Transmission data | Transmission time[1] | Transmitted data[2] | Transmission time | Transmitted data |
| SOURCEID_0 | 0 | $t_{ASYNC}$ | CH0_SNSDATA0 | NA | NA | See Section 10.8: Daisy chain mode | CH0_SNSDATA0 |
| | 1 | | | PDCM_RSPST0 | CH0_SNSDATA0 | | |
| SOURCEID_1 | 0 | NA | NA | NA | NA | NA | NA |
| | 1 | | | PDCM_RSPST1 | CH0_SNSDATA1 | | |

| Source ID | Source ID enable (SIDx_EN) | Asynchronous mode | | Synchronous mode | | Daisy chain mode | | Dual transmission mode | |
|---|---|---|---|---|---|---|---|---|---|
| | | Transmission time | Transmission data | Transmission time[3] | Transmitted data[4] | Transmission time | Transmitted data | Transmission time | Transmitted data |
| SOURCEID_0 | 0 | $t_{ASYNC}$ | CH0_SNSDATA0 | NA | NA | See Section 10.8: Daisy chain mode | CH0_SNSDATA0 | PDCM_RSPST0 | CH1_SNSDATA0, CH0_SNSDATA0 See Section 10.7: Dual transmission mode |
| | 1 | | | PDCM_RSPST0 | CH0_SNSDATA0 | | | | |
| SOURCEID_1 | 0 | NA | NA | NA | NA | NA | NA | NA | NA |
| | 1 | | | PDCM_RSPST1 | CH0_SNSDATA1 | | | | |
| SOURCEID_2 | 0 | NA | NA | NA | NA | See Section 10.8: Daisy chain mode | CH1_SNSDATA0 | NA | NA |
| | 1 | | | PDCM_RSPST2 | CH1_SNSDATA0 | | | | |
| SOURCEID_3 | 0 | NA | NA | NA | NA | NA | NA | NA | NA |
| | 1 | | | PDCM_RSPST3 | CH1_SNSDATA1 | | | | |

1. *See Section 8.2.18.1*
2. *See Section 8.2.25.2 and Section 8.2.25.3*
3. *See Section 8.2.18.1*
4. *See Section 8.2.25.2 and Section 8.2.25.3*

In I²C mode, the SOURCEID_x registers are readable and writable. See Section 12.6.3: Sensor data register read wraparound options, for details regarding the effect of the SIDx_EN bits.

### 8.2.14 Communication timing register (TIMING_CFG)

The communication timing configuration register is a user programmed read/write register which contains user-specific con-figuration information for protocol timing. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 96. Communication timing register (TIMING_CFG)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $22 | TIMING_CFG | PDCM_PER[2:0] | | | OSCTRAIN_SEL | CK_CAL_RST | CRM_PER[1:0] | | CK_CAL_EN |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### *8.2.14.1 Periodic data collection mode period (PDCM_PER[3:0])*

The periodic data collection mode period selection bits set the data collection mode period to be used by the DSI3, SPI, PSI5, or I²C master as shown in Table 97. Periodic data collection mode period (PDCM_PER[3:0]). This value is only necessary for oscillator training and is only used if the CK_CAL_EN bit is set in the TIMING_CFG register.

**Table 97. Periodic data collection mode period (PDCM_PER[3:0])**

| PDCM_PER[2] | PDCM_PER[1] | PDCM_PER[0] | Periodic data collection mode period |
|---|---|---|---|
| 0 | 0 | 0 | 100 µs |
| 0 | 0 | 1 | 125 µs |
| 0 | 1 | 0 | 250 µs |
| 0 | 1 | 1 | 333 µs |
| 1 | 0 | 0 | 500 µs |
| 1 | 0 | 1 | 800 µs |
| 1 | 1 | 0 | 1000 µs |
| 1 | 1 | 1 | 2000 µs |

In DSI3 mode, PDCM, and BDM commands are decoded and responded to regardless of the value of this register as long as the general PDCM timing parameters specified in Section 7.12: Dynamic electrical characteristics - DSI3 are met. See Section 8.5.1: Oscillator training for details regarding oscillator training.

In PSI5 synchronous mode, sync pulses are decoded and responded to regardless of the value of this register as long as the general timing parameters specified in Section 7.13: Dynamic electrical characteristics - PSI5 are met. See Section 8.5.1: Oscillator training for details regarding oscillator training.

In PSI5 asynchronous mode, oscillator training is not applicable.

In PSI5 Programming Mode, oscillator training is not applicable.

In PSI5 Daisy Chain command phase, oscillator training is not applicable.

In SPI mode, sensor data requests are decoded and responded to regardless of the value of this register as long as the general timing parameters specified in Section 7.14: Dynamic electrical characteristics - SPI are met. See Section 8.5.1: Oscillator training for details regarding oscillator training.

In I²C mode, sensor data register reads are decoded and responded to regardless of the value of this register as long as the general timing parameters specified in Section 7.15: Dynamic electrical characteristics - I²C are met. See Section 8.5.1: Oscillator training for details regarding oscillator training.

#### 8.2.14.2 *Oscillator training protocol selection bit (OSCTRAIN_SEL)*

The oscillator training selection bit selects the protocol to use for oscillator training for the COMMTYPE values that enable multiple protocols as shown in Table 98. Oscillator training protocol selection bit (OSCTRAIN_SEL).

**Table 98. Oscillator training protocol selection bit (OSCTRAIN_SEL)**

| COMMTYPE | OSCTRAIN_SEL | Protocol to use for oscillator training |
|---|---|---|
| 0 | 0 | DSI3 |
| | 1 | SPI |
| 1 | 0 | PSI5 |
| | 1 | SPI |
| 2 | x | SPI |
| 3 | x | DSI3 |
| 4 | x | SPI |
| 5 | x | PSI5 |
| 6 | x | I²C |
| 7 | x | I²C |

#### 8.2.14.3 *Clock calibration value reset (CK_CAL_RST)*

The clock calibration reset bit controls the state of the oscillator training when the CK_CAL_EN bit is cleared as described in the table in Section 8.2.14.5: Clock calibration enable (CK_CAL_EN). See Section 8.5.1: Oscillator training for details regarding oscillator training.

#### 8.2.14.4 *Command and response mode period (CRM_PER[1:0])*

In DSI3 mode, the command and response mode period bits set the period for command and response mode commands in increments of the periodic data collection mode period (PDCM_PER). This value is only necessary for DSI3 oscillator training and is only used if the CK_CAL_EN bit is set in the TIMING_CFG register. command and response mode commands will be decoded and responded to regardless of the value of this register as long as the general command and response mode timing parameters specified in Section 7.12: Dynamic electrical characteristics - DSI3 are met. See Section 8.5.1: Oscillator training for details regarding oscillator training.

In SPI and I²C mode, the CRM_PER[1:0] bits are readable and writable, but have no impact on device operation or performance.

In PSI5 mode, the CRM_PER[1:0] bits are readable and writable, but have no impact on device operation or performance.

**Table 99. Command and response mode period (CRM_PER[1:0])**

| CRM_PER[1] | CRM_PER[0] | Command and response mode period (Multiples of the periodic data collection mode period) |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 8 |

#### 8.2.14.5 *Clock calibration enable (CK_CAL_EN)*

The clock calibration enable bit enables oscillator training over the DSI3, PSI5, SPI, or I²C communication interface. See Section 8.5.1: Oscillator training for details regarding oscillator training.

**Table 100. Clock calibration enable (CK_CAL_EN)**

| CK_CAL_EN | CK_CAL_RST | Oscillator training |
|---|---|---|
| 0 | 0 | The oscillator value is maintained at the last trained value prior to clearing the CK_CAL_RST bit. |
| 0 | 1 | The oscillator value is reset to the untrained value with a tolerance specified in Section 7.21: Dynamic electrical characteristics - supply and support circuitry. |
| 1 | x | Oscillator is trained as specified in Section 8.5.1: Oscillator training |

### 8.2.15 Chip time and bit time register (CHIPTIME)

The chip time and bit time register is a user programmed read/write register which contains user-specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 101. Chip time and bit time register (CHIPTIME)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $23 | CHIPTIME | ST_RPT[1:0] | | PSI5_ERRLATCH | SS_EN | CHIPTIME[3:0] | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx Unprogrammed Default PSI5 Mode | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

#### 8.2.15.1 *PSI5 self-test repetition bits (ST_RPT[1:0])*

In PSI5 mode, the PSI5 self-test repetition bits set the maximum number of PSI5 self-test repetitions that the device will run before setting the ST_ERROR bit. See Section 6.6.2.5 for details regarding the PSI5 startup self-test.

**Table 102. PSI5 self-test repetition bits (ST_RPT[1:0])**

| ST_RPT[1] | ST_RPT[0] | Maximum PSI5 self-test repetitions |
|---|---|---|
| 0 | 0 | 8 |
| 0 | 1 | 1 |
| 1 | 0 | 4 |
| 1 | 1 | 2 |

#### 8.2.15.2 *PSI5 error latching enable bit (PSI5_ERRLATCH)*

In PSI5 mode, the PSI5 error latching enable bit allows for users to disable the automatic error clearing mechanism for internal faults. When this bit is set, internal errors are latched until reset. See Section 10.9.4: Normal mode error handling with internal error automatic clearing and Section 10.9.5: Normal mode error handling with internal error latching for details regarding internal error handling.

**Table 103. PSI5 error latching enable bit (PSI5_ERRLATCH)**

| PSI5_ERRLATCH | PSI5 error handling |
|---|---|
| 0 | Error handling is as specified in Section 8.2.2: Device status registers (DEVSTATx) and Section 10.9.4: Normal mode error handling with internal error automatic clearing |
| 1 | Automatic error clearing is disabled and internal errors are latched until reset as specified in Section 10.9.5: Normal mode error handling with internal error latching |

#### 8.2.15.3 *Simultaneous sampling enable (SS_EN)*

In DSI3 mode, the simultaneous sampling enable bit selects between one of two data latency methods. See Section 9.4.7: DSI3 PDCM data transmission modes for details regarding sample timing.

**Table 104. DSI3 simultaneous sampling enable (SS_EN)**

| SS_EN | Data latency |
|---|---|
| 0 | Synchronous Sampling Mode: Latency relative to transmission start time (PDCM_RSPST) |
| 1 | Simultaneous Sampling Mode: Latency relative to the start of the Periodic Data Collection Mode command (falling edge) |

In PSI5 mode, the simultaneous sampling enable bit selects between one of two data latency methods to accommodate synchronized sampling or simultaneous sampling.

**Table 105. PSI5 simultaneous sampling enable (SS_EN)**

| SS_EN | Data latency |
|---|---|
| 0 | Synchronous Sampling Mode (Latency relative to Time Slot) |
| 1 | Simultaneous Sampling Mode (Latency relative to sync pulse) |

In SPI mode, the simultaneous sampling enable bit selects between one of two data latency methods.

**Table 106. SPI simultaneous sampling enable (SS_EN)**

| SS_EN | Data latency |
|---|---|
| 0 | Synchronous sampling mode: The data for all sources is latent relative to the falling edge of slave select for the response to the Sensor Data Request for the corresponding SOURCEID. |
| 1 | Simultaneous sampling mode: The data for all sources is latent relative to the falling edge of slave select for the response to the Sensor Data Request for SOURCEID_0.<br>If SOURCEID_0 is disabled, then the data for all SOURCEIDs is latent relative to the falling edge of slave select for the response to the Sensor Data Request for lowest enabled SOURCEID register address.<br>*Note: If multiple SOURCEIDs are enabled, sensor data for the higher SOURCEID register addresses only changes on a sensor data request for the lowest enabled SOURCEID register address. If continuous sensor data requests occur without sensor data requests for the lowest SOURCEID register address, sensor data will not be updated. Care must be taken by the user to ensure proper data transmissions.* |

In I²C mode, the simultaneous sampling enable bit is readable and writable but has no impact on device operation or performance.

#### 8.2.15.4 *Chip time (CHIPTIME)*

In DSI3 mode, the CHIPTIME bits set the chip time for Periodic Data Collection Mode as described in Table 107. Chip time (CHIPTIME). The chip time for Command and Response Mode is always set to 5 µs with slew control enabled.

In PSI5 mode, the CHIPTIME bits set the bit time for the PSI5 response data as described in Table 107. Chip time (CHIPTIME).

**Table 107. Chip time (CHIPTIME)**

| CHIPTIME[3] | CHIPTIME[2] | CHIPTIME[1] | CHIPTIME[0] | PSI5 | | | DSI3 | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Period time | Baud rate | Slew control | Chip time | Chip rate | Slew control |
| 0 | 0 | 0 | 0 | 5.3 µs | 189 kHz | Enabled | 1.0 µs | 1000 kHz | Disabled |
| 0 | 0 | 0 | 1 | 5.3 µs | 189 kHz | Enabled | 2.0 µs | 500.0 kHz | Disabled |
| 0 | 0 | 1 | 0 | 5.3 µs | 189 kHz | Enabled | 2.5 µs | 400.0 kHz | Enabled |
| 0 | 0 | 1 | 1 | 5.3 µs | 189 kHz | Enabled | 2.6 µs | 384.6 kHz | Enabled |
| 0 | 1 | 0 | 0 | 5.3 µs | 189 kHz | Enabled | 2.6 µs | 384.6 kHz | Enabled |
| 0 | 1 | 0 | 1 | 5.3 µs | 189 kHz | Enabled | 2.7 µs | 370.3 kHz | Enabled |
| 0 | 1 | 1 | 0 | 5.3 µs | 189 kHz | Enabled | 2.8 µs | 357.1 kHz | Enabled |
| 0 | 1 | 1 | 1 | 5.3 µs | 189 kHz | Enabled | 2.9 µs | 344.8 kHz | Enabled |
| 1 | 0 | 0 | 0 | 8.0 µs | 125 kHz | Enabled | 3.0 µs | 333.3 kHz | Enabled |
| 1 | 0 | 0 | 1 | 8.0 µs | 125 kHz | Enabled | 3.1 µs | 322.6 kHz | Enabled |
| 1 | 0 | 1 | 0 | 8.0 µs | 125 kHz | Enabled | 3.2 µs | 312.5 kHz | Enabled |
| 1 | 0 | 1 | 1 | 8.0 µs | 125 kHz | Enabled | 3.3 µs | 303.0 kHz | Enabled |
| 1 | 1 | 0 | 0 | 8.0 µs | 125 kHz | Enabled | 3.5 µs | 294.1 kHz | Enabled |
| 1 | 1 | 0 | 1 | 8.0 µs | 125 kHz | Enabled | 4.0 µs | 250.0 kHz | Enabled |
| 1 | 1 | 1 | 0 | 8.0 µs | 125 kHz | Enabled | 4.5 µs | 222.2 kHz | Enabled |
| 1 | 1 | 1 | 1 | 8.0 µs | 125 kHz | Enabled | 5.0 µs | 200.0 kHz | Enabled |

In SPI and I²C mode, the CHIPTIME bits are readable and writable but have no impact on device operation or performance.

### 8.2.16 Timing configuration #2 register (TIMING_CFG2)

The timing configuration #2 register is a user programmed read/write register which contains user-specific timing configuration information. This register is included in the read/write array error detection. See Section 9.4: DSI3 periodic data collection mode and background diagnostic mode for details regarding Background Diagnostic Mode.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 108. Timing configuration #2 register (TIMING_CFG2)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $24 | TIMING_CFG2 | PSI5_INIT2_D19 | OSCTRAIN_ERRCNT[2:0] | | | CAPTEST_OFF | RESERVED | BDM_FRAGSIZE | BDM_EN |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### *8.2.16.1 PSI5 initialization phase 2 D19 and D20 change bit (PSI5_INIT2_D19)*

The PSI5 initialization phase 2 D19 and D20 change bit provides the option to change the data transmitted in PSI5 Initialization Phase 2 nibbles D19 and D20 as shown in Table 109. PSI5 initialization phase 2 D19 and D20 change bit (PSI5_INIT2_D19).

**Table 109. PSI5 initialization phase 2 D19 and D20 change bit (PSI5_INIT2_D19)**

| PSI5_INIT2_D19 | Initialization phase 2 data | | Reference |
|---|---|---|---|
| | D19 | D20 | |
| 0 | SN4[7:4] | SN4[3:0] | Section 8.2.42: Device serial number registers, Section 10.4.2.1: PSI5 initialization phase 2 data transmissions |
| 1 | USERDATA_6[7:4] | USERDATA_E[7:4] | Section 8.2.46.1: PSI5 initialization phase 2 data transmissions of user data, Section 10.4.2.1: PSI5 initialization phase 2 data transmissions |

In DSI3 mode, SPI mode, and I²C mode, the PSI5_INIT2_D19 bit is readable and writable, but has no impact on device operation or performance.

#### 8.2.16.2 *Oscillator training error counter (OSCTRAIN_ERRCNT[2:0])*

The oscillator training error counter bits use the number of 4 ms periods used to determine the error detection time for oscillator training as shown in Table 110. Oscillator training error counter (OSCTRAIN_ERRCNT[2:0]). See Section 8.5.2: Oscillator training error handling for details regarding oscillator training error detection.

**Table 110. Oscillator training error counter (OSCTRAIN_ERRCNT[2:0])**

| OSCTRAIN_ERRCNT[2:0] | | | 4 ms periods counted before the OSCTRAIN error flag is set | Minimum time for error detection (ms) |
|---|---|---|---|---|
| 0 | 0 | 0 | 64 | 256 |
| 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 0 | 2 | 8 |
| 0 | 1 | 1 | 4 | 16 |
| 1 | 0 | 0 | 8 | 32 |
| 1 | 0 | 1 | 16 | 64 |
| 1 | 1 | 0 | 32 | 128 |
| 1 | 1 | 1 | 64 | 256 |

#### 8.2.16.3 *Capacitor test disable bit (CAPTEST_OFF)*

The capacitor test disable bit provides the option to disable the VBUF capacitor test in DSI3 mode as shown in Table 111. Capacitor test disable bit (CAPTEST_OFF).

**Table 111. Capacitor test disable bit (CAPTEST_OFF)**

| CAPTEST_OFF | Capacitor test status |
|---|---|
| 0 | Capacitor test is operational as specified in Section 8.4.1: $V_{BUF}$ regulator capacitor and capacitor monitor |
| 1 | Capacitor test will not run |

If a capacitor error is present, the VBUFUV_ERR bit is set in the DEVSTAT1 register as specified in Section 8.4.1: $V_{BUF}$ regulator capacitor and capacitor monitor. The presence of the VBUFUV_ERR will prevent the user from writing to the TIMING_CFG2 register to disable the capacitor test unless and until the capacitor error recovers.

In SPI and I²C mode, the CAPTEST_OFF bit is readable and writable, but has no impact on device operation or performance.

In PSI5 mode, the CAPTEST_OFF bit is readable and writable, but has no impact on device operation or performance.

#### 8.2.16.4 *Background diagnostic mode fragment size (BDM_FRAGSIZE)*

The background diagnostic mode fragment size bit sets the number of background diagnostic command bits and response chips to be sent per Periodic Data Collection Mode sampling period.

**Table 112. Background diagnostic mode fragment size (BDM_FRAGSIZE)**

| BDM_FRAGSIZE | BDM command fragment size (Bits) | BDM response fragment size (Chips) |
|---|---|---|
| 0 | 2 | 3 |
| 1 | 4 | 6 |

In SPI and I²C mode, the BDM_FRAGSIZE bit is readable and writable, but has no impact on device operation or performance.

In PSI5 mode, the BDM_FRAGSIZE bit is readable and writable, but has no impact on device operation or performance.

#### 8.2.16.5 *Background diagnostic mode enable (BDM_EN)*

The background diagnostic mode enable bit enables background diagnostic mode as described in Table 113. Background diagnostic mode enable (BDM_EN). See Section 9.4: DSI3 periodic data collection mode and background diagnostic mode for details regarding background diagnostic mode.

**Table 113. Background diagnostic mode enable (BDM_EN)**

| BDM_EN | Background diagnostic mode |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

In SPI and I²C mode, the BDM_EN bit is readable and writable, but has no impact on device operation or performance.

In PSI5 mode, the BDM_EN bit is readable and writable, but has no impact on device operation or performance.

### 8.2.17 PSI5 configuration register (PSI5_CFG)

The PSI5 configuration register is a user programmable OTP register that contains PSI5 specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode.

**Table 114. PSI5 configuration register (PSI5_CFG)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $25 | PSI5_CFG | SYNC_PD | DAISY_CHAIN | PSI5_ILOW | RESERVED<br>DUALTRANS | EMSG_EXT | P_CRC | INIT2_EXT | ASYNC |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx<br>Unprogrammed Default PSI5 Mode | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

#### 8.2.17.1 *Sync pulse pull-down enable bit (SYNC_PD)*

In PSI5 mode, the sync pulse pull-down enable bit selects if the Sync pulse pull-down is enabled once a sync pulse is detected. See Section 8.2.18.1: Periodic data collection mode response start time (PDCM_RSPSTx[12:0]) for more information regarding the sync pulse pulldown.

**Table 115. Sync pulse pull-down enable bit (SYNC_PD)**

| SYNC_PD | Sync pulse pull-down |
|---|---|
| 0 | Disabled |
| 1 | Enabled for all PSI5 operating modes |

In DSI3 mode, the SYNC_PD bit is readable and writable, but has no impact on device operation or performance.

In SPI and I²C mode, the SYNC_PD bit is readable and writable, but has no impact on device operation or performance.

#### 8.2.17.2 *PSI5 daisy chain selection bit (DAISY_CHAIN)*

In PSI5 mode, the transmission mode selection bits select the PSI5 transmission mode as shown in Table 116. PSI5 daisy chain selection bit (DAISY_CHAIN).

**Table 116. PSI5 daisy chain selection bit (DAISY_CHAIN)**

| DAISY_CHAIN | Operating mode | Response (PDCM_RSTST0) | Reference |
|---|---|---|---|
| 0 | Normal Mode (Asynchronous or Parallel, Synchronous) | SNSDATA0 | Section 10.5: Normal mode |
| 1 | Daisy Chain Mode | SNSDATA0 | Section 10.8: Daisy chain mode |

In DSI3 mode, the DAISY_CHAIN bit is readable and writable, but has no impact on device operation or performance.

In SPI and I²C mode, the DAISY_CHAIN bit is readable and writable, but has no impact on device operation or performance.

#### 8.2.17.3 *PSI5 low response current selection bit (PSI5_ILOW)*

In PSI5 mode, the PSI5 low response current selection bit selects the low PSI5 response current specified in Section 7.4: Electrical characteristics - supply and I/O as shown in Table 117. PSI5 low response current selection bit (PSI5_ILOW).

**Table 117. PSI5 low response current selection bit (PSI5_ILOW)**

| PSI5_ILOW | PSI5 response current |
|---|---|
| 0 | Normal Response Current |
| 1 | Low Response Current |

In DSI3 mode, the PSI5_ILOW bit is readable and writable, but has no impact on device operation or performance.

In SPI and I²C mode, the PSI5_ILOW bit is readable and writable, but has no impact on device operation or performance.

#### 8.2.17.4 *Dual transmission mode (DUALTRANS)*

In PSI5 mode, the dual transmission mode bit enables dual data transmission as described in Section 10.7: Dual transmission mode only if the DAISY_CHAIN bit is not set and the ASYNC bit is not set.

**Table 118. Dual transmission mode (DUALTRANS)**

| DUALTRANS | SID3_EN | SID2_EN | SID1_EN | SID0_EN | Operating mode | Response PDCM_RSPST0 | Response PDCM_RSPST1 | Response PDCM_RSPST2 | Response PDCM_RSPST3 | Reference |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | As specified in Section 8.2.13.3: Source identification (SOURCEID_x) | | | | Normal Mode Asynchronous or Synchronous, Parallel, Daisy Chain | CH0_SNSDATA0 | CH0_SNSDATA1 | CH1_SNSDATA0 | CH1_SNSDATA1 | Section 10.5: Normal mode, Section 10.8: Daisy chain mode |
| 1 | x | x | 0 | 0 | No Transmission | None | None | None | None | Section 10.7: Dual transmission mode |
| | x | x | 0 | 1 | Dual Data Transmission Mode, Single Transmission | CONCATENATE (CH1_SNSDA-TA0, CH0_SNS-DATA0) | None | None | None | |
| | x | x | 1 | 0 | Dual Data Transmission Mode, Single Transmission | None | CONCATENATE (CH1_SNSDA-TA1, CH0_SNS-DATA1) | None | None | |
| | x | x | 1 | 1 | Dual Data Transmission Mode, Double Transmission | CONCATENATE (CH1_SNSDA-TA0, CH0_SNS-DATA0) | CONCATENATE (CH1_SNSDA-TA1, CH0_SNS-DATA1) | None | None | |

In DSI3 mode, the DUALTRANS mode is readable and writable, but has no impact on device operation or performance.

In SPI and I²C mode, the DUALTRANS bits are readable and writable, but has no impact on device operation or performance.

#### 8.2.17.5 *Error message information extension bit (EMSG_EXT)*

In PSI5 mode, the error message information extension bit enables or disables additional PSI5 error message information as shown in Table 119. Error message information extension bit (EMSG_EXT).

**Table 119. Error message information extension bit (EMSG_EXT)**

| EMSG_EXT | Description |
|---|---|
| 0 | All internal Errors map to 0x1F4 (See Section 10.3.4: PSI5 data field and data range values) |
| 1 | Additional PSI5 reserved codes are used for internal error distinction (See Section 10.3.4: PSI5 data field and data range values) |

In DSI3 mode, the EMSG_EXT bit is readable and writable, but has no impact on device operation or performance.

In SPI and I²C mode, the EMSG_EXT bit is readable and writable, but has no impact on device operation or performance.

#### 8.2.17.6 *PSI5 response message error detection selection bit (P_CRC)*

In PSI5 mode, the response message error detection selection bit selects either even parity, or a 3-bit CRC for error detection of the PSI5 response message. See Section 8.2.18.1: Periodic data collection mode response start time (PDCM_RSPSTx[12:0]) for details regarding response message error detection.

**Table 120. PSI5 response message error detection selection bit (P_CRC)**

| P_CRC | Parity or CRC |
|---|---|
| 0 | Parity |
| 1 | CRC |

In DSI3 mode, the P_CRC bit is readable and writable, but has no impact on device operation or performance.

In SPI and I²C mode, the P_CRC bit is readable and writable, but has no impact on device operation or performance.

#### 8.2.17.7 *Initialization phase 2 data extension bit (INIT2_EXT)*

In PSI5 mode, the initialization phase 2 data extension bit enables or disables data transmission in data fields D33 through D48 of PSI5 initialization phase 2 as shown in Table 121. Initialization phase 2 data extension bit (INIT2_EXT).

**Table 121. Initialization phase 2 data extension bit (INIT2_EXT)**

| INIT2_EXT | Description |
|---|---|
| 0 | D33 through D48 are not transmitted |
| 1 | D33 through D48 are transmitted as defined in Section 10.4.2.1: PSI5 initialization phase 2 data transmissions |

In DSI3 mode, the INIT2_EXT bit is readable and writable, but has no impact on device operation or performance.

In SPI and I²C mode, the INIT2_EXT bit is readable and writable, but has no impact on device operation or performance.

#### 8.2.17.8 *Asynchronous mode bit (ASYNC)*

In PSI5 mode, the asynchronous mode bit enables asynchronous data transmission as described in Section 8.2.18.1: Periodic data collection mode response start time (PDCM_RSPSTx[12:0]) only if the DAISY_CHAIN bit is not set.

In DSI3 mode, the ASYNC bit is readable and writable, but has no impact on device operation or performance.

In SPI and I²C mode, the ASYNC bit is readable and writable, but has no impact on device operation or performance.

### 8.2.18 DSI3 and PSI5 start time registers (PDCM_RSPSTx_x)

The DSI3 and PSI5 start time registers are user programmed read/write registers which contain user-specific configuration information for DSI3 periodic data collection mode and PSI5 synchronous mode. These registers are included in the read/write array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 122. DSI3 and PSI5 start time registers (PDCM_RSPSTx_x)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $26 | PDCM_RSPST0_L | PDCM_RSPST0[7:0] | | | | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx Unprogrammed Default PSI5 Mode | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| $27 | PDCM_RSPST0_H | BRC_RSP0[1:0] | | RESERVED | PDCM_RSPST0[12:8] | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx Unprogrammed Default PSI5 Mode | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $28 | PDCM_RSPST1_L | PDCM_RSPST1[7:0] | | | | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx Unprogrammed Default PSI5 Mode | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $29 | PDCM_RSPST1_H | BRC_RSP1[1:0] | | RESERVED | PDCM_RSPST1[12:8] | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx Unprogrammed Default PSI5 Mode | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $2A | PDCM_RSPST2_L | PDCM_RSPST2[7:0] | | | | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx Unprogrammed Default PSI5 Mode | | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| $2B | PDCM_RSPST2_H | BRC_RSP2[1:0] | | RESERVED | PDCM_RSPST2[12:8] | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx Unprogrammed Default PSI5 Mode | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $2C | PDCM_RSPST3_L | PDCM_RSPST3[7:0] | | | | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx Unprogrammed Default PSI5 Mode | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $2D | PDCM_RSPST3_H | BRC_RSP3[1:0] | | RESERVED | PDCM_RSPST3[12:8] | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NXLS96xxx Unprogrammed Default PSI5 Mode | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.18.1 *Periodic data collection mode response start time (PDCM_RSPSTx[12:0])*

The periodic data collection mode response start time registers set the DSI3 periodic data collection mode or PSI5 synchronous mode response start time for the associated data and SOURCEID. The value is stored in 1.0 µs increments.

**Table 123. Periodic data collection mode response start time (PDCM_RSPSTx[12:0])**

| PDCM_RSPSTx[12:0] | Periodic data collection mode response start time |
|---|---|
| 0 | See Table 124. Synchronous mode: Source ID response start time |
| 0 < PDCM_RSPSTx[12:0] < 20 | 20.0 µs |

| PDCM_RSPSTx[12:0] | Periodic data collection mode response start time |
|---|---|
| 20 < PDCM_RSPSTx[12:0] | PDCM response start = PDCM_RSPST x 1.0 µs |

Table 124. Synchronous mode: Source ID response start time shows the relationship of the SOURCEID, the transmitted data, the response start times, and the default states for each set of registers in DSI3 periodic data collection mode. Care must be taken to prevent from programming response start times which cause data contention in the system.

**Table 124. Synchronous mode: Source ID response start time**

| SOURCEID register | Transmitted data | Start time registers | Default start (PDCM_RSPSTx[12:0] = 0x00) |
|---|---|---|---|
| SOURCEID_0 | CH0_SNSDATA0 | PDCM_RSPST0[12:0] | Transmit Data with a start time of 20 µs |
| SOURCEID_1 | CH0_SNSDATA1 | PDCM_RSPST1[12:0] | Transmit Data with a start time of 20 µs |
| SOURCEID_2 | CH1_SNSDATA0 | PDCM_RSPST2[12:0] | Transmit Data with a start time of 20 µs |
| SOURCEID_3 | CH1_SNSDATA1 | PDCM_RSPST3[12:0] | Transmit Data with a start time of 20 µs |

Table 125. Asynchronous mode: Source ID response start time shows the PSI5 data transmission start times based on the values in the PDCM_RSPSTx registers and the value of the ASYNC bit. Care must be taken to prevent from programming time slots which violate the PSI5 Version 1.3 specification, or time slots which will cause data contention.

**Table 125. Asynchronous mode: Source ID response start time**

| ASYNC bit | SOURCEID register | Transmitted data | Time slot start time | Default start (PDCM_RSPSTx[12:0] = 0x00) |
|---|---|---|---|---|
| 1 | SOURCEID_0 | CH0_SNSDATA0 | Asynchronous Mode | $t_{ASYNC}$ |
| 0 | SOURCEID_0 | CH0_SNSDATA0 | PDCM_RSPST0[12:0] | Transmit Data with a start time of 20 µs |
| | SOURCEID_1 | CH0_SNSDATA1 | PDCM_RSPST1[12:0] | Transmit Data with a start time of 20 µs |
| **ASYNC bit** | **SOURCEID register** | **Transmitted data** | **Time slot start time** | **Default start (PDCM_RSPSTx[12:0] = 0x00)** |
| 1 | SOURCEID_0 | CH0_SNSDATA0 | Asynchronous Mode | $t_{ASYNC}$ |
| 0 | SOURCEID_0 | CH0_SNSDATA0 | PDCM_RSPST0[12:0] | Transmit Data with a start time of 20 µs |
| | SOURCEID_1 | CH0_SNSDATA1 | PDCM_RSPST1[12:0] | Transmit Data with a start time of 20 µs |
| | SOURCEID_2 | CH1_SNSDATA0 | PDCM_RSPST2[12:0] | Transmit Data with a start time of 20 µs |
| | SOURCEID_3 | CH1_SNSDATA1 | PDCM_RSPST3[12:0] | Transmit Data with a start time of 20 µs |

In SPI and I²C mode, the PDCM_RSPSTx registers are readable and writable, but have no impact on device operation or performance.

#### 8.2.18.2 *Broadcast read command type selection bits (BRC_RSP[1:0])*

The broadcast read command type selection bits select the broadcast read command types that the device responds to for each Source ID as shown in Table 126. Broadcast read command type selection bits (BRC_RSP[1:0]):

**Table 126. Broadcast read command type selection bits (BRC_RSP[1:0])**

| BRC_RSP[1] | BRC_RSP[0] | Response |
|---|---|---|
| 0 | 0 | Respond to all Broadcast Read Commands |

| BRC_RSP[1] | BRC_RSP[0] | Response |
|---|---|---|
| 0 | 1 | Respond to Broadcast Read Command 0 only |
| 1 | 0 | Respond to Broadcast Read Command 1 only |
| 1 | 1 | Respond to all Broadcast Read Commands |

If a device is programmed to respond only to BRC0 or BRC1 commands, it will synchronize to alternate responses when BDM commands are received.

- If the last command prior to a BDM command is a BRC0, a device programmed to respond only to BRC0 commands will not respond to the first BDM command and will then respond to every other BDM command until the next BRC command is received.
- If the last command prior to a BDM command is a BRC0, a device programmed to respond only to BRC1 commands will respond to the first BDM command, and will then response to every other BDM command until the next BRC command is received.
- If the last command prior to a BDM command is a BRC1, a device programmed to respond only to BRC0 commands will respond to the first BDM command, and will then response to every other BDM command until the next BRC command is received.
- If the last command prior to a BDM command is a BRC1, a device programmed to respond only to BRC1 commands will not respond to the first BDM command and will then respond to every other BDM command until the next BRC command is received.

In PSI5 mode, the BRC_RSP[1:0] bits are readable and writable, but have no impact on device operation or performance.

In SPI and I²C mode, the BRC_RSP[1:0] bits are readable and writable, but have no impact on device operation or performance.

### 8.2.19 DSI3 and PSI5 command blocking time registers (PDCM_CMD_B_x)

The DSI3 and PSI5 command blocking registers are user programmed read/write registers which contain user-specific con-figuration information for DSI3 mode and PSI5 mode. These registers are included in the read/write array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode.

**Table 127. DSI3 and PSI5 command blocking time registers (PDCM_CMD_B_x)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $38 | PDCM_CMD_B_L | PDCM_CMD_B[7:0] | | | | | | | |
| $39 | PDCM_CMD_B_H | RESERVED | RESERVED | RESERVED | PDCM_CMD_B[12:8] | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

In DSI3 mode, the DSI3 periodic data collection mode command blocking time bits set the periodic data collection mode command blocking time in 1.0 µs increments, with zero as the default value of 450 µs. For proper communication, the command blocking time must exceed the completion of the last source response transmission. See Section 9.1.1: Command receiver for details regarding the command receiver and command blocking.

Care must be taken to prevent from programming command blocking times which prevent proper command decoding in the system and to ensure proper sampling of the VHIGH voltage. As shown in Section 9.1.1: Command receiver, Figure 63. DSI3 command receiver timing diagram: valid command, the VHIGH voltage is initially captured at the end of the command blocking time and then filtered. The user must ensure that the command blocking end time is set for a time when no command or response transmissions are occurring to provide the most stable BUS_I voltage.

**Table 128. DSI3 mode: Command blocking time bits**

| PDCM_CMD_B[12:0] | Sync pulse blocking time |
|---|---|
| 0 | 450 µs |

| PDCM_CMD_B[12:0] | Sync pulse blocking time |
|---|---|
| Non-Zero | Sync Pulse Blocking Time = PDCM_CMD_B x 1 µs |

In PSI5 mode, the command blocking time bits set the PSI5 sync pulse blocking time in 1.0 µs increments, with zero as the default value of 450 µs. See Section 10.2.1: Synchronization pulse for details regarding the PSI5 sync pulse receiver and command blocking.

Care must be taken to prevent from programming command blocking times which prevent proper sync pulse decoding in the system and to ensure proper sampling of the PSI5 voltage.

**Table 129. PSI5 mode: Command blocking time bits**

| PDCM_CMD_B[12:0] | Sync pulse blocking time |
|---|---|
| 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 | 450 µs |
| 10 - 8191 | Sync Pulse Blocking Time = PDCM_CMD_B x 1 µs |

In SPI and I²C mode, the PDCM_CMD_B bits are readable and writable, but have no impact on device operation or performance.

### 8.2.20 SPI configuration control register

In SPI mode, the SPI configuration control register is a user programmed read/write register which contains the SPI protocol configuration information. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode.

**Table 130. SPI configuration control register**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $3D | SPI_CFG | SPI_STATUS | DATASIZE | SPI_CRC_LEN[1:0] | | SPICRCSEED[3:0] | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.20.1 *SPI status reporting selection bit (SPI_STATUS)*

The SPI status reporting bit controls the reporting of the SPI basic status as shown in Table 131. SPI status reporting selection bit (SPI_STATUS). See Section 11.5: Exception handling.

**Table 131. SPI status reporting selection bit (SPI_STATUS)**

| SPI_STATUS | SPI basic status reporting |
|---|---|
| 0 | As documented in Section 11.5.1: Standard basic status reporting field |
| 1 | As documented in Section 11.5.2: Alternative basic status reporting field |

In DSI3 mode, the SPI_STATUS bit is readable and writable, but has no impact on device operation or performance.

In PSI5 mode, the SPI_STATUS bit is readable and writable, but has no impact on device operation or performance.

In I²C mode, the SPI_STATUS bit is readable and writable, but has no impact on device operation or performance.

#### 8.2.20.2 *SPI data field size bit (DATASIZE)*

The SPI data field size bit controls the size of the SPI data field as shown in Table 132. SPI data field size bit (DATASIZE). See Section 8.6.4.9: Output scaling.

Table 132. **SPI data field size bit (DATASIZE)**

| DATASIZE | SPI data field size |
|---|---|
| 0 | 12-bits |
| 1 | 16-bits |

In DSI3 mode, the DATASIZE bit is readable and writable, but has no impact on device operation or performance.

In PSI5 mode, the DATASIZE bit is readable and writable, but has no impact on device operation or performance.

In I²C mode, the DATASIZE bit is readable and writable, but has no impact on device operation or performance.

#### 8.2.20.3 *SPI CRC length and seed bits (SPI_CRC_LEN[1:0], SPICRCSEED[3:0])*

The SPI_CRC_LEN[1:0] bits select the CRC length for SPI mode as shown in Table 133. SPI CRC length and seed bits (SPI_CRC_LEN[1:0], SPICRCSEED[3:0]). The SPI CRC seed bits contain the seed used for the SPI Mode. The default SPI CRC is an 8-bit. When the SPI_CRC_LEN[1:0] bits are set to a non-zero value using a register write command, the SPI CRC changes as defined in the table. The new polynomial value is enabled for both MISO and MOSI on the next SPI mode command.

The default seed (SPICRCSEED[3:0] = 0x0) is 0xFF for an 8-bit CRC. When the value is changed to a non-zero value using a register write command, the SPI CRC seed changes to the value programmed as shown in the table. The new seed value is enabled for both MISO and MOSI on the next SPI mode command.

Table 133. **SPI CRC length and seed bits (SPI_CRC_LEN[1:0], SPICRCSEED[3:0])**

| SPI_CRC_LEN[1:0] | | SPICRCSEED | CRC polynomial | CRC seed |
|---|---|---|---|---|
| 0 | 0 | 0 | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111, 1111 |
| | | Non-Zero | | 1111, SPICRCSEED[3:0] |
| 0 | 1 | 0 | $x^4 + 1$ | 1010 |
| | | Non-Zero | | SPICRCSEED[3:0] |
| 1 | 0 | 0 | $x^3 + x + 1$ | 111 |
| | | Non-Zero | | SPICRCSEED[2:0] |
| 1 | 1 | 0 | $x^3 + x + 1$ | 111 |
| | | Non-Zero | | SPICRCSEED[2:0] |

In PSI5 mode, the SPI CRC bits are readable and writable, but have no impact on device operation or performance.

In DSI3 mode, the SPI CRC bits are readable and writable, but have no impact on device operation or performance.

In I²C mode, the SPI CRC bits are readable and writable, but have no impact on device operation or performance.

### 8.2.21 Who Am I register

The Who Am I register is a user programmed read/write register which contains the unique product identifier for I²C mode. The register is readable in all modes. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

Table 134. **Who Am I register**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $3E | WHO_AM_I | WHO_AM_I[7:0] | | | | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Unprogrammed Read Value | | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

The default register value is 0x00. If the register value is 0x00, a value of 0xC4 is transmitted in response to a read command. For all other register values, the actual register value is transmitted in response to a read command.

**Table 135. WHO_AM_I bits**

| WHO_AM_I Register Value (HEX) | Response to a register read command |
|---|---|
| 0X00 | 0xC4 |
| 0X01 Through 0xFF | Actual register value |

### 8.2.22 I²C slave address register

The I²C slave address register is a user programmed read/write register which contains the unique I²C slave address. The register is readable in all modes. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 136. I²C slave address register**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $3F | I2C_ADDRESS | I2C_ADDRESS[7:0] | | | | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Unprogrammed Read Value | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

The default register value is 0x00. If the register value is 0x00, the I²C slave address is 0x60 and a value of 0x60 is transmitted in response to a read command. For all other register values, the I²C slave address is the lower 7 bits of the actual register value and the actual register value is transmitted in response to a read command.

**Table 137. I2C_ADDRESS bits**

| I2C_ADDRESS register value (HEX) | Response to a register read command | I²C slave address |
|---|---|---|
| 0x00, 0x80 | 0x60 | 0x60 |
| 0x01 Through 0x7F, 0x81 Through 0xFF | Actual Register Value | I2C_ADDRESS[6:0] |

### 8.2.23 Channel 0 and Channel 1 user configuration #1 registers (CH0_CFG_U1, CH1_CFG_U1)

The Channel 0 and Channel 1 user configuration #1 register is a s are user programmable read/write registers which contains channel-specific configuration information. This register is These registers are included in the read/write array error detection.

This register is These registers are readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode.

**Table 138. Channel 0 and Channel 1 user configuration #1 registers (CH0_CFG_U1, CH1_CFG_U1)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $40 | CH0_CFG_U1 | LPF[3:0] | | | | SAMPLERATE[1:0] | | USER_SNS_SHIFT[1:0] | |
| $48 | CH1_CFG_U1 | LPF[3:0] | | | | SAMPLERATE[1:0] | | USER_SNS_SHIFT[1:0] | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.23.1 *Low-pass filter and sample rate selection bits (LPF[3:0], SAMPLERATE[1:0])*

The low-pass filter selection bits and sample rate bits select the low-pass filter for the associated channel. See Section 8.6.4.4: Low-pass filter for details regarding the low-pass filter.

**Table 139. Low-pass filter and sample rate selection bits (LPF[3:0], SAMPLERATE[1:0])**

| LPF[3] | LPF[2] | LPF[1] | LPF[0] | Low-pass filter type | | |
|---|---|---|---|---|---|---|
| | | | | SAMPLERATE = 00, 01 | SAMPLERATE = 10 | SAMPLERATE = 11 |
| | | | | 16 µs | 32 µs | 64 µs |
| 0 | 0 | 0 | 0 | 400 Hz, 4-Pole | 200 Hz, 4-Pole | 100 Hz, 4-Pole |
| 0 | 0 | 0 | 1 | 400 Hz, 3-Pole | 200 Hz, 3-Pole | 100 Hz, 3-Pole |
| 0 | 0 | 1 | 0 | 400 Hz, 4-Pole | 200 Hz, 4-Pole | 100 Hz, 4-Pole |
| 0 | 0 | 1 | 1 | 400 Hz, 3-Pole | 200 Hz, 3-Pole | 100 Hz, 3-Pole |
| 0 | 1 | 0 | 0 | 325 Hz, 3-Pole | 162.5 Hz, 3-Pole | 81.25 Hz, 3-Pole |
| 0 | 1 | 0 | 1 | 370 Hz, 2-Pole | 185 Hz, 2-Pole | 92.5 Hz, 2-Pole |
| 0 | 1 | 1 | 0 | 180 Hz, 2-Pole | 90 Hz, 2-Pole | 45 Hz, 2-Pole |
| 0 | 1 | 1 | 1 | 100 Hz, 2-Pole | 50 Hz, 2-Pole | 25 Hz, 2-Pole |
| 1 | 0 | 0 | 0 | 1500 Hz, 4-Pole | 750 Hz, 4-Pole | 375 Hz, 4-Pole |
| 1 | 0 | 0 | 1 | 500 Hz, 3-Pole | 250 Hz, 3-Pole | 125 Hz, 3-Pole |
| 1 | 0 | 1 | 0 | 800 Hz, 4-Pole | 400 Hz, 4-Pole | 200 Hz, 4-Pole |
| 1 | 0 | 1 | 1 | 1200 Hz, 4-Pole | 600 Hz, 4-Pole | 300 Hz, 4-Pole |
| 1 | 1 | 0 | 0 | 120 Hz, 3-Pole | 60 Hz, 3-Pole | 30 Hz, 3-Pole |
| 1 | 1 | 0 | 1 | 20 kHz, 2-Pole | 10 kHz, 2-Pole | 5 kHz, 2-Pole |
| 1 | 1 | 1 | 0 | 120 Hz, 2-Pole | 60 Hz, 2-Pole | 30 Hz, 2-Pole |
| 1 | 1 | 1 | 1 | 50 Hz, 4-Pole | 25 Hz, 4-Pole | 12.5 Hz, 4-Pole |

Changes to these register bits reset the DSP data path. The contents of the SNSDATA_x registers are not guaranteed until the DSP has completed initialization as specified in Section 7.21: Dynamic electrical characteristics - supply and support circuitry. Reads of the SNSDATA_x registers and Sensor Data requests should be prevented during this time.

#### 8.2.23.2 *User sensitivity shift selection bits (U_SNS_SHIFT[1:0])*

The user sensitivity selection bits are used along with the user sensitivity multiplier bits to scale the output sensitivity of the device. See Section 8.2.24.1: User sensitivity multiplier bits (U_SNS_MULT[7:0]) for details.

### 8.2.24 Channel 0 and Channel 1 user configuration #2 registers (CH0_CFG_U2, CH1_CFG_U2)

The Channel 0 and Channel 1 user configuration #2 register is a s are user programmable read/write registers which contains channel-specific configuration information. This register is The registers are included in the read/write array error detection.

This register is These registers are readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode.

**Table 140. Channel 0 and Channel 1 user configuration #2 registers (CH0_CFG_U2, CH1_CFG_U2)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $41 | CH0_CFG_U2 | U_SNS_MULT[7] | U_SNS_MULT[6] | U_SNS_MULT[5] | U_SNS_MULT[4] | U_SNS_MULT[3] | U_SNS_MULT[2] | U_SNS_MULT[1] | U_SNS_MULT[0] |
| $49 | CH1_CFG_U2 | U_SNS_MULT[7] | U_SNS_MULT[6] | U_SNS_MULT[5] | U_SNS_MULT[4] | U_SNS_MULT[3] | U_SNS_MULT[2] | U_SNS_MULT[1] | U_SNS_MULT[0] |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.24.1 *User sensitivity multiplier bits (U_SNS_MULT[7:0])*

The user sensitivity multiplier bits are used along with the user sensitivity shift bits to scale the output sensitivity of the device. Eq. (1) describes the scaling:

$$OutputSensitivity = TrimSensitivity \times SensitivityShiftFactor \times \frac{256 + SensitivityMultiplier}{256} \quad (1)$$

Where:

TrimSensitivity = The default trimmed sensitivity of the device, as specified in Section 7.6: Electrical characteristics - inertial sensor signal chain: High g

SensitivityMultiplier = The unsigned multiplier value contained in the U_SNS_MULT[7:0] bits

SensitivityShiftFactor = The Shift Factor selected by the U_SNS_SHIFT[1:0] bits as described in Table 141. Sensitivity shift factors

**Table 141. Sensitivity shift factors**

| Device Type | U_SNS_SHIFT[1] | U_SNS_SHIFT[0] | Sensitivity shift factor |
|---|---|---|---|
| Normal Range | 0 | 0 | 0.25 |
| Normal Range | 0 | 1 | 0.50 |
| Normal Range | 1 | 0 | 1 |
| Normal Range | 1 | 1 | 2 |

Table 142. Example user shift and multiplier configuration for typical scale range shows some example user shift and multiplier values for typical full scale ranges (± 2047, 12 bit):

**Table 142. Example user shift and multiplier configuration for typical scale range(1)**

| Device type | Desired range (g) | Desired sensitivity (12 bit, LSB/g) | ST trim (12 bit, LSB/g) | User sensitivity shift factor | | User multiplier value | | Actual sensitivity 16 bit register Chx_SNS-DATAx LSB/g) | Actual sensitivity 10 bit Sensor data request, LSB/g | Actual sensitivity 12 bit Sensor data request, LSB/g | Actual sensitivity 16 bit Sensor data request, LSB/g |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | U_SNS_SHIFT (HEX) | Shift Factor | U_SNS_-MULT (HEX) | Multiplier value (Dec) | | | | |
| Low g | 1.50 | 1364.6667 | 341.8343 | 0x3 | 2 | 0xFF | 255 | 2729.333 | 341.1667 | 1364.6667 | 21834.67 |
| | 1.75 | 1169.7143 | 341.8343 | 0x3 | 2 | 0xB6 | 182 | 2339.429 | 292.4286 | 1169.7143 | 18715.43 |
| | 2.00 | 1023.5000 | 341.8343 | 0x3 | 2 | 0x7F | 127 | 2045.665 | 255.7081 | 1022.8324 | 16365.32 |
| | 3.00 | 682.3333 | 341.8343 | 0x2 | 1 | 0xFF | 255 | 1364.667 | 170.5833 | 682.3333 | 10917.33 |
| | 3.50 | 584.8571 | 341.8343 | 0x2 | 1 | 0xB6 | 182 | 1169.714 | 146.2143 | 584.8571 | 9357.714 |
| | 3.75 | 545.8667 | 341.8343 | 0x2 | 1 | 0x99 | 153 | 1092.267 | 136.5334 | 546.1337 | 8738.139 |
| | 4.00 | 511.7500 | 341.8343 | 0x2 | 1 | 0x7F | 127 | 1022.832 | 127.8541 | 511.4162 | 8182.659 |
| | 5.00 | 409.4000 | 341.8343 | 0x2 | 1 | 0x33 | 51 | 819.8682 | 102.4835 | 409.9341 | 6558.946 |
| | 5.98 | 341.8343 | 341.8343 | 0x2 | 1 | 0x00 | 0 | 683.6686 | 85.4586 | 341.8343 | 5469.349 |
| | 6.00 | 341.1667 | 341.8343 | 0x1 | 0.5 | 0xFF | 255 | 682.3334 | 85.2917 | 341.1667 | 5458.667 |
| | 7.50 | 272.9333 | 341.8343 | 0x1 | 0.5 | 0x99 | 153 | 546.1338 | 68.2667 | 273.0669 | 4369.070 |
| | 8.00 | 255.8750 | 341.8343 | 0x1 | 0.5 | 0x7F | 127 | 511.4162 | 63.9270 | 255.7081 | 4091.330 |
| | 10.00 | 204.7000 | 341.8343 | 0x1 | 0.5 | 0x33 | 51 | 409.9342 | 51.2418 | 204.9671 | 3279.474 |
| | 12.00 | 170.5833 | 341.8343 | 0x0 | 0.25 | 0xFF | 255 | 341.1666 | 42.6458 | 170.5833 | 2729.333 |
| | 15.00 | 136.4667 | 341.8343 | 0x0 | 0.25 | 0x99 | 153 | 273.0668 | 34.1333 | 136.5334 | 2184.534 |
| | 20.00 | 102.3500 | 341.8343 | 0x0 | 0.25 | 0x33 | 51 | 204.9670 | 25.6209 | 102.4835 | 1639.736 |
| | 23.95 | 85.4586 | 341.8343 | 0x0 | 0.25 | 0x00 | 0 | 170.9170 | 21.3646 | 85.4586 | 1367.338 |
| Medium g | 15.5 | 131.7246 | 33.0161 | 0x3 | 2 | 0xFF | 255 | 263.6130 | 32.9516 | 131.8065 | 2108.904 |
| | 16 | 127.9375 | 33.0161 | 0x3 | 2 | 0xF0 | 240 | 255.8748 | 31.9844 | 127.9374 | 2046.998 |
| | 20 | 102.3500 | 33.0161 | 0x3 | 2 | 0x8D | 141 | 204.8030 | 25.6004 | 102.4015 | 1638.424 |
| | 25 | 81.8800 | 33.0161 | 0x3 | 2 | 0x3D | 61 | 163.5328 | 20.4416 | 81.7664 | 1308.262 |
| | 35 | 58.4857 | 33.0161 | 0x2 | 1 | 0xC5 | 197 | 116.8460 | 14.6058 | 58.4230 | 934.7680 |
| | 50 | 40.9400 | 33.0161 | 0x2 | 1 | 0x3D | 61 | 81.7664 | 10.2208 | 40.8832 | 654.1312 |

| Device type | Desired range (g) | Desired sensitivity (12 bit, LSB/g) | ST trim (12 bit, LSB/g) | User sensitivity shift factor | | User multiplier value | | Actual sensitivity 16 bit register Chx_SNS-DATAx LSB/g) | Actual sensitivity 10 bit Sensor data request, LSB/g | Actual sensitivity 12 bit Sensor data request, LSB/g | Actual sensitivity 16 bit Sensor data request, LSB/g |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | U_SNS_SHIFT (HEX) | Shift Factor | U_SNS_-MULT (HEX) | Multiplier value (Dec) | | | | |
| Medium g | 60 | 34.1167 | 33.0161 | 0x2 | 1 | 0x09 | 9 | 68.3536 | 8.5442 | 34.1768 | 546.8288 |
| | 62 | 33.0161 | 33.0161 | 0x2 | 1 | 0x00 | 0 | 66.0322 | 8.2540 | 33.0161 | 528.2576 |
| | 62.5 | 32.7520 | 33.0161 | 0x1 | 0.5 | 0xFC | 252 | 65.5164 | 8.1896 | 32.7582 | 524.1312 |
| | 75 | 27.2933 | 33.0161 | 0x1 | 0.5 | 0xA7 | 167 | 54.5540 | 6.8193 | 27.2770 | 436.4320 |
| | 85.3 | 24.0000 | 33.0161 | 0x1 | 0.5 | 0x74 | 116 | 47.9766 | 5.9971 | 23.9883 | 383.8128 |
| | 100 | 20.4700 | 33.0161 | 0x1 | 0.5 | 0x3D | 61 | 40.8832 | 5.1104 | 20.4416 | 327.0656 |
| | 105 | 19.5000 | 33.0161 | 0x1 | 0.5 | 0x2E | 46 | 38.9486 | 4.8686 | 19.4743 | 311.5888 |
| | 112.5 | 18.2000 | 33.0161 | 0x1 | 0.5 | 0x1A | 26 | 36.3692 | 4.5462 | 18.1846 | 290.9536 |
| | 125 | 16.3760 | 33.0161 | 0x0 | 0.25 | 0xFC | 252 | 32.7582 | 4.0948 | 16.3791 | 262.0656 |
| | 128 | 16.0000 | 33.0161 | 0x0 | 0.25 | 0xF0 | 240 | 31.9844 | 3.998 | 15.9922 | 255.8752 |
| | 150 | 13.6467 | 33.0161 | 0x0 | 0.25 | 0xA7 | 167 | 27.2770 | 3.4096 | 13.6385 | 218.2160 |
| High g | 50 | 40.9400 | 10.9465 | 0x3 | 2 | 0xDF | 223 | 81.9278 | 10.2410 | 40.9639 | 655.4224 |
| | 60 | 34.1167 | 10.9465 | 0x3 | 2 | 0x8F | 143 | 68.2446 | 8.5306 | 34.1223 | 545.9568 |
| | 62 | 33.0161 | 10.9465 | 0x3 | 2 | 0x82 | 130 | 66.0210 | 8.2526 | 33.0105 | 528.1680 |
| | 62.5 | 32.7520 | 10.9465 | 0x3 | 2 | 0x7F | 127 | 65.5080 | 8.1885 | 32.7540 | 524.0640 |
| | 100 | 20.4700 | 10.9465 | 0x2 | 1 | 0xDF | 223 | 40.9638 | 5.1205 | 20.4819 | 327.7104 |
| | 105 | 19.5000 | 10.9465 | 0x2 | 1 | 0xC8 | 200 | 38.9970 | 4.8746 | 19.4985 | 311.9760 |
| | 112.5 | 18.2000 | 10.9465 | 0x2 | 1 | 0xAA | 170 | 36.4314 | 4.5539 | 18.2157 | 291.4512 |
| | 125 | 16.3760 | 10.9465 | 0x2 | 1 | 0x7F | 127 | 32.7540 | 4.0943 | 16.3770 | 262.0320 |
| | 128 | 16.0000 | 10.9465 | 0x2 | 1 | 0x76 | 118 | 31.9844 | 3.9981 | 15.9922 | 255.8752 |
| | 150 | 13.6467 | 10.9465 | 0x2 | 1 | 0x3F | 63 | 27.2808 | 3.4101 | 13.6404 | 218.2464 |
| | 187 | 10.9465 | 10.9465 | 0x2 | 1 | 0x00 | 0 | 21.8930 | 2.7366 | 10.9465 | 175.1440 |
| | 250 | 8.1880 | 10.9465 | 0x1 | 0.5 | 0x7F | 127 | 16.3770 | 2.0471 | 8.1885 | 131.0160 |
| | 312.5 | 6.5504 | 10.9465 | 0x1 | 0.5 | 0x32 | 50 | 13.0844 | 1.6356 | 6.5422 | 104.6752 |
| | 375 | 5.4587 | 10.9465 | 0x0 | 0.25 | 0xFF | 255 | 10.9252 | 1.3657 | 5.4626 | 87.4016 |
| | 500 | 4.0940 | 10.9465 | 0x0 | 0.25 | 0x7F | 127 | 8.1884 | 1.0236 | 4.0942 | 65.5072 |

1. *Table 142. Example user shift and multiplier configuration for typical scale range includes some typical device ranges. Other ranges are possible with the user-selected shift and multiplier values.*

Table 143. Example user shift and multiplier configuration for typical psi5 scale range shows some example user shift and multiplier values for typical PSI5 full scale ranges (± 480, 10 bit):

**Table 143. Example user shift and multiplier configuration for typical psi5 scale range(1)**

| Device type | Desired range (g) | Desired sensitivity (10 bit, LSB/g) | ST trim (10 bit, LSB/g) | ST trim (16 bit, LSB/g) | User sensitivity shift factor | | User multiplier value | | Actual sensitivity (PSI5 10 bit, LSB/g) | Actual sensitivity (PSI5 16 bit, LSB/g) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | U_SNS_SHIFT (HEX) | Shift Factor | U_SNS_MULT (HEX) | Multiplier value (Dec) | | |
| Medium g | 15 | 32.0000 | 8.2540 | 528.256 | 0x3 | 2 | 0xF0 | 240 | 31.9844 | 2047.00 |
| | 20 | 24.0000 | 8.2540 | 528.256 | 0x3 | 2 | 0x74 | 116 | 23.9883 | 1535.25 |
| | 30 | 16.0000 | 8.2540 | 528.256 | 0x2 | 1 | 0xF0 | 240 | 15.9922 | 1023.50 |
| | 60 | 8.0000 | 8.2540 | 528.256 | 0x1 | 0.5 | 0xF0 | 240 | 7.9961 | 511.500 |
| | 120 | 4.0000 | 8.2540 | 528.256 | 0x0 | 0.25 | 0xF0 | 240 | 3.9980 | 255.875 |
| High g | 60 | 8.0000 | 2.7366 | 175.142 | 0x3 | 2 | 0x76 | 118 | 7.9961 | 511.749 |
| | 120 | 4.0000 | 2.7366 | 175.142 | 0x2 | 1 | 0x76 | 118 | 3.9980 | 255.874 |
| | 240 | 2.0000 | 2.7366 | 175.142 | 0x1 | 0.5 | 0x76 | 118 | 1.9990 | 127.937 |
| | 480 | 1.0000 | 2.7366 | 175.142 | 0x0 | 0.25 | 0x76 | 118 | 0.9995 | 63.9686 |

1. *Table 143. Example user shift and multiplier configuration for typical psi5 scale range includes some typical device ranges. Other ranges are possible with the user-selected shift and multiplier values.*

### 8.2.25 Channel 0 and Channel 1 user configuration #3 registers (CH0_CFG_U3, CH1_CFG_U3)

The Channel 0 and Channel 1 user configuration #3 register is a s are user programmable read/write registers which contains channel-specific configuration information. This register is The registers are included in the read/write array error detection.

This register is These registers are readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 144. Channel 0 and Channel 1 user configuration #3 registers (CH0_CFG_U3, CH1_CFG_U3)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $42 | CH0_CFG_U3 | UNSIGNEDDATA | DATATYPE0[1:0] | | DATATYPE1[2:0] | | | MOVEAVG[1:0] | |
| $4A | CH1_CFG_U3 | UNSIGNEDDATA | DATATYPE0[1:0] | | DATATYPE1[2:0] | | | MOVEAVG[1:0] | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.25.1 *Unsigned data select bit (UNSIGNEDDATA)*

The unsigned data selection bit selects signed or unsigned data for the register and sensor data transmissions as shown in Table 145. Unsigned data select bit (UNSIGNEDDATA).

**Table 145. Unsigned data select bit (UNSIGNEDDATA)**

| UNSIGNEDDATA | Register values | | DATATYPE transmissions | |
|---|---|---|---|---|
| | CHx_SNSDATA0 | CHx_SNSDATA1 | Sensor data (DSI, SPI) | Sensor data (PSI5) |
| Channel Sensor Data | | | | |
| 0 | Signed Data | Signed Data | Signed Data | Signed Data |
| 1 | Unsigned Data | Unsigned Data | Unsigned Data | |
| Temperature Sensor Data | | | | |
| 0 | As specified in Section 8.7.2: Temperature sensor output scaling equations | | | |
| 1 | | | | |

#### 8.2.25.2 *Channel 0 data type 0 selection bits (CHxDATATYPE0)*

The Channel Data Type 0 selection bits select the type of data to be included in the SNSDATA0_L and SNSDATA0_H registers for each channel.

**Table 146. Channel 0 data type 0 selection bits (CHxDATATYPE0)**

| CHxDATATYPE0[1] | CHxDATATYPE0[0] | Data transmitted | | | |
|---|---|---|---|---|---|
| | | Data transmitted | Offset canceled? | Moving average? | Interpolation? |
| 0 | 0 | CHx Sensor Data | Selected by OC_-FILT[1:0] | Selected by MOVEAVG[1:0] | Selected by MOVEAVG[1:0] |
| 0 | 1 | CHx Sensor Data | No | | |
| 1 | 0 | Temperature Sensor Data (As specified in Section 8.7.2: Temperature sensor output scaling equations) | | | |
| 1 | 1 | | | | |

#### 8.2.25.3 *Channel 0 data type 1 selection bits (CHxDATATYPE1)*

The Channel data type 1 selection bits select the type of data to be included in the SNSDATA1_L and SNSDATA1_H registers for each channel.

**Table 147. Channel 0 data type 1 selection bits (CHxDATATYPE1)**

| CHxDATATYPE 1[2] | CHxDATATYPE 1[1] | CHxDATATYPE 1[0] | Data transmitted | | | |
|---|---|---|---|---|---|---|
| | | | Data transmitted | Offset canceled? | Moving average? | Interpolation? |
| 0 | 0 | 0 | CHx Sensor Data | Selected by OC_-FILT[1:0] | Selected by MOVEAVG[1:0] | No |
| 0 | 0 | 1 | CHx Sensor Data | No | Selected by MOVEAVG[1:0] | No |
| 0 | 1 | 0 | Temperature Sensor Data (As specified in Section 8.7.2: Temperature sensor output scaling equations) | | | |
| 0 | 1 | 1 | | | | |
| 1 | 0 | 0 | CHx Sensor Data | Selected by OC_-FILT[1:0] | No | No |
| 1 | 0 | 1 | CHx Sensor Data | No | Selected by MOVEAVG[1:0] | No |
| 1 | 1 | 0 | Temperature Sensor Data (As specified in Section 8.7.2: Temperature sensor output scaling equations) | | | |
| 1 | 1 | 1 | | | | |

#### 8.2.25.4 *Signal chain moving average selection bits (MOVEAVG[1:0])*

The signal chain moving average selection bits determine the input sample period to be used for the signal chain moving average filter.

**Table 148. Signal chain moving average selection bits (MOVEAVG[1:0])**

| MOVEAVG[1] | MOVEAVG[0] | Typical signal sampling period (Dependent on oscillator) (µs) | Signal chain moving average | Interpolation |
|---|---|---|---|---|
| 0 | 0 | Determined by LPF | Bypassed | Enabled |
| 0 | 1 | 32 | 8 Sample Moving Average | Disabled |
| 1 | 0 | 64 | 8 Sample Moving Average | Disabled |
| 1 | 1 | 128 | 8 Sample Moving Average | Disabled |

Changes to these register bits reset the DSP data path. The contents of the SNSDATA_x registers are not guaranteed until the DSP has completed initialization as specified in Section 7.21: Dynamic electrical characteristics - supply and support circuitry. Reads of the SNSDATA_x registers and Sensor Data requests should be prevented during this time.

### 8.2.26 Channel 0 and Channel 1 user configuration #4 registers (CH0_CFG_U4, CH1_CFG_U4)

The Channel 0 and Channel 1 user configuration #4 register is a registers are user programmable read/write registers which contains channel-specific configuration information. This register is These registers are included in the read/write array error detection.

This register is These registers are readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 149. Channel 0 and Channel 1 user configuration #4 registers (CH0_CFG_U4, CH1_CFG_U4)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $43 | CH0_CFG_U4 | RESET_OC | INVERT | OC_FILT[1:0] | | PCM | ARM_CFG[2:0] | | |
| $4B | CH1_CFG_U4 | RESET_OC | INVERT | OC_FILT[1:0] | | PCM | ARM_CFG[2:0] | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.26.1 *Reset offset cancellation startup bit (RESET_OC)*

When the reset offset cancellation startup bit is written to logic 1, the offset cancellation startup is forced to phase 0 and follows the phase advancement as documented in Section 8.6.4.6: Offset cancellation. The RESET_OC bit is cleared when the offset cancellation phase reaches phase 1.

#### 8.2.26.2 *Signal inversion bit (INVERT)*

The signal inversion bit provides the option to invert the polarity of the sensor signals as shown in Table 150. Signal inversion bit (INVERT).

**Table 150. Signal inversion bit (INVERT)**

| INVERT | Acceleration sensor data | Fixed pattern self-test | Digital self-test | Analog self-test | | Temperature |
|---|---|---|---|---|---|---|
| 0 | As shown in Section 5: Device orientation diagrams. | As specified in Section 8.2.27.1: Self-test control bits (ST_CTRL[3:0]) | Digital Self-Test Activation results in the values specified in Section 7.9: Electrical characteristics - inertial sensor self-test. | Positive Self-Test: | Delta from Offset as specified in Section 7: Electrical characteristics | As specified in Section 8.7.2: Temperature sensor output scaling equations |
| | | | | Negative Self-Test: | Delta from Offset inverted from the specified values in Section 7.9: Electrical characteristics - inertial sensor self-test (Negative Values) | |
| 1 | Inverted polarity from that shown in Section 5: Device orientation diagrams | | Digital Self-Test Activation results in the two's complement of the values specified in Section 7.9: Electrical characteristics - inertial sensor self-test. | Positive Self-Test: | Delta from Offset inverted from the specified values in Section 7.9: Electrical characteristics - inertial sensor self-test (Negative Values) | |
| | | | | Negative Self-Test: | Delta from Offset as specified in Section 7: Electrical characteristics | |

#### 8.2.26.3 *Offset cancellation filter selection bits (OC_FILT[1:0])*

The offset cancellation filter selection bits provide the option to bypass the offset cancellation filter and the rate limiting for the associated channel. See Section 8.6.4.6: Offset cancellation for details regarding offset cancellation.

**Table 151. Offset cancellation filter selection bits (OC_FILT[1:0])**

| OC_FILT[1] | OC_FILT[0] | Offset cancellation IIR filter | Offset cancellation rate limiting |
|---|---|---|---|
| 0 | 0 | 0.04 Hz | Enabled |
| 0 | 1 | 0.04 Hz | Bypassed |
| 1 | 0 | 0.005 Hz | Bypassed |
| 1 | 1 | Bypassed | Bypassed |

#### 8.2.26.4 *Arming pin configuration bits (ARM_CFG[2:0]) and PCM range selection bit (PCM)*

The ARM configuration bits (ARM_CFG[2:0]) select the mode of operation for the arming pins.

**Table 152. Arming pin configuration bits (ARM_CFG[2:0]) and PCM range selection bit (PCM)**

| ARM_CFG[2] | ARM_CFG[1] | ARM_CFG[0] | PCM | Operating mode | Output type | Reference |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | x | Arm/PCM Output Disabled | High Impedance | |
| 0 | 0 | 1 | 0 | Arm/PCM Output Disabled | Driven Low | |
| 0 | 0 | 1 | 1 | PCM Output | Digital Output | Section 8.8: PCM output function |

| ARM_CFG[2] | ARM_CFG[1] | ARM_CFG[0] | PCM | Operating mode | Output type | Reference |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | x | Moving Average Mode | Open-Drain, Active High with Pull-down Current | Section 8.9.1: Arming function: moving average mode |
| 0 | 1 | 1 | x | Moving Average Mode | Open-Drain, Active Low with Pull-up Current | Section 8.9.1: Arming function: moving average mode |
| 1 | 0 | 0 | x | Count Mode | Open-Drain, Active High with Pull-down Current | Section 8.9.2: Arming function: count mode |
| 1 | 0 | 1 | x | Count Mode | Open-Drain, Active Low with Pull-up Current | Section 8.9.2: Arming function: count mode |
| 1 | 1 | 0 | x | Unfiltered Mode | Open-Drain, Active High with Pull-down Current | Section 8.9.3: Arming function: unfiltered mode |
| 1 | 1 | 1 | x | Unfiltered Mode | Open-Drain, Active Low with Pull-up Current | Section 8.9.3: Arming function: unfiltered mode |

*Note: The arming function is reset on a change to the ARM_CFG bits. This includes the downsampling state and all history registers.*

When the PCM output is enabled, a Pulse Code Modulated signal proportional to the data selected by the DATATYPE0 selection bits is output on the ARM/PCM pin. See Section 8.8: PCM output function for more information regarding the PCM output.

### 8.2.27 Channel 0 and Channel 1 user configuration #5 register (CH0_CFG_U5, CH1_CFG_U5)

The Channel 0 and Channel 1 user configuration #5 register is a registers are user programmable read/write registers which contains channel-specific configuration information. This register is These registers are included in the read/write array error detection.

This register is These registers are readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 153. Channel 0 and Channel 1 user configuration #5 register (CH0_CFG_U5, CH1_CFG_U5)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $44 | CH0_CFG_U5 | ST_CTRL[3:0] | | | | OC_LIMIT[2:0] | | | DSP_DIS |
| $4C | CH1_CFG_U5 | ST_CTRL[3:0] | | | | OC_LIMIT[2:0] | | | DSP_DIS |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.27.1 *Self-test control bits (ST_CTRL[3:0])*

The self-test control bits select one of the various analog and digital self-test features of the device as shown in Table 154. Self-test control bits (ST_CTRL[3:0]).

The self-test control bits are writable in DSI3 command and response mode.

The self-test control bits are writable in SPI Mode.

The self-test control bits are writable in I²C Mode.

The self-test control bits are writable in PSI5 programming mode.

**Table 154. Self-test control bits (ST_CTRL[3:0])**

| ST_CTRL[3] | ST_CTRL[2] | ST_CTRL[1] | ST_CTRL[0] | Function | 16-bit SNSDATAx Register value signed | Effect on ST_INCMPLT bit in Chx_STAT | Effect on ST_ACTIVE bit in Chx_STAT |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DSP writes to the SNS_DATAx_X registers as configured in the ChxDATATYPEx registers. | Sensor Data | No Effect | Clear when Active |
| 0 | 0 | 0 | 1 | | | Clear on Activation | Set When Active |
| 0 | 0 | 1 | 0 | | | Clear on Activation | Set When Active |
| 0 | 0 | 1 | 1 | | | Clear on Activation | Set When Active |
| 0 | 1 | 0 | 0 | DSP write to registers inhibited. | 0x0000 | Clear on Activation | Set When Active |
| 0 | 1 | 0 | 1 | | 0xAAAA | Clear on Activation | Set When Active |
| 0 | 1 | 1 | 0 | | 0x5555 | Clear on Activation | Set When Active |
| 0 | 1 | 1 | 1 | | 0xFFFF | Clear on Activation | Set When Active |
| 1 | 0 | 0 | 0 | Positive Analog Self-test - Low | Sensor Data | Clear on Activation | Set When Active |
| 1 | 0 | 0 | 1 | Negative Analog Self-test - Low | | Clear on Activation | Set When Active |
| 1 | 0 | 1 | 0 | Positive Analog Self-test - High | | Clear on Activation | Set When Active |
| 1 | 0 | 1 | 1 | Negative Analog Self-test - High | | Clear on Activation | Set When Active |
| 1 | 1 | 0 | 0 | Digital Self-test | Reference Section 7.9: Electrical characteristics - inertial sensor self-test | Clear on Activation | Set When Active |
| 1 | 1 | 0 | 1 | | | Clear on Activation | Set When Active |
| 1 | 1 | 1 | 0 | | | Clear on Activation | Set When Active |
| 1 | 1 | 1 | 1 | | | Clear on Activation | Set When Active |

#### 8.2.27.2 *Offset cancellation test limit bits (OC_LIMIT[2:0])*

The offset cancellation test limit bits set the offset limits for the offset test at the end of the PSI5 self-test documented in Section 8.6.2.5: PSI5 automatic startup self-test procedure . The test limits are set as shown in Table 155. Offset cancellation test limit bits (OC_LIMIT[2:0]).

**Table 155. Offset cancellation test limit bits (OC_LIMIT[2:0])**

| OC_LIMIT[2:0] | Post PSI5 self-test offset limits |
|---|---|
| 0x0 | The post PSI5 self-test offset test is disabled. |
| 0x1 | ± 2 LSB, 10-bit |
| 0x2 | ± 4 LSB, 10-bit |
| 0x3 | ± 6 LSB, 10-bit |
| 0x4 | ± 8 LSB, 10-bit |
| 0x5 | ± 10 LSB, 10-bit |
| 0x6 | ± 12 LSB, 10-bit |
| 0x7 | ± 14 LSB, 10-bit |

#### 8.2.27.3 *DSP disable bit (DSP_DIS)*

The DSP disable bit provides the option for the user to disable the clocking to the DSP if sensor data from the associated channel is not used.

**Table 156. DSP disable bit (DSP_DIS)**

| DSP_DIS | DSP status |
|---|---|
| 0 | DSP operational as specified |
| 1 | DSP clocking disabled. Sensor data is readable but will not be updated by the DSP even when self-test is enabled |

Care must be taken to ensure the DSP is not disabled for sources that are enabled.

### 8.2.28 Channel 0 and Channel 1 arming configuration registers (CH0_ARM_CFG, CH1_ARM_CFG)

The arming configuration registers contains configuration information for the arming function. The values in this these registers are only relevant if the arming function is operating in moving average mode, or count mode.

*Note: The arming function is reset on a change to the CHx_ARM_CFG bits. This includes the downsampling state and all history registers.*

This register These registers can be written during initialization but is are locked once the ENDINIT bit is set. Refer to Section 8.2.6: Device lock register (DEVLOCK_WR). The register is registers are included in the read/write array error detection.

**Table 157. Channel 0 and Channel 1 arming configuration registers (CH0_ARM_CFG, CH1_ARM_CFG)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $45 | CH0_ARM_CFG | ARM_DS[1:0] | | ARM_PS[1:0] | | ARM_WS_N[1:0] | | ARM_WS_P[1:0] | |
| $4D | CH1_ARM_CFG | ARM_DS[1:0] | | ARM_PS[1:0] | | ARM_WS_N[1:0] | | ARM_WS_P[1:0] | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.28.1 *Arming function downsampling selection bits (ARM_DS[1:0])*

The arming function down sampling selection bits select the down sample rate for the arming function. See Section 8.9.4: Arming function downsampling.

**Table 158. Arming function downsampling selection bits (ARM_DS[1:0])**

| ARM_DS[1] | ARM_DS[0] | Downsampling |
|---|---|---|
| 0 | 0 | Provide every Sensor Data Request sample to the arming function for the relevant channel. |
| 0 | 1 | Provide every other Sensor Data Request sample to the arming function for the relevant channel. |
| 1 | 0 | Provide every fourth Sensor Data Request sample to the arming function for the relevant channel. |
| 1 | 1 | Provide every eighth Sensor Data Request sample to the arming function for the relevant channel. |

#### 8.2.28.2 *Arming pulse stretch (ARM_PS[1:0])*

The ARM_PS[1:0] bits set the programmable pulse stretch time for the arming outputs. See Section 8.9: Arming function for more details regarding the arming function. Pulse stretch times are derived from the internal oscillator, so the tolerance on this oscillator applies.

**Table 159. Arming pulse stretch (ARM_PS[1:0])**

| ARM_PS[1] | ARM_PS[0] | Pulse stretch time (typical oscillator) |
|---|---|---|
| 0 | 0 | 0 ms |
| 0 | 1 | 128.000 ms - 130.048 ms |
| 1 | 0 | 512.000 ms - 514.048 ms |
| 1 | 1 | 2048.000 ms - 2050.048 ms |

#### 8.2.28.3 *Arming window size (ARM_WS_N[1:0], A_WS_P[1:0])*

The ARM_WS_N[1:0] and ARM_WS_P[1:0] bits have a different function depending on the state of the ARM_CFG bits in the CHx_CFG_U3 CHx_CFG_U4 registers. See Section 8.9: Arming function for more details regarding the arming function. If the arming function is set to moving average mode, the ARM_WS bits set the number of sensor samples used for the arming function moving aver-age. The number of samples is set independently for each channel and polarity. If the arming function is set to count mode, the ARM_WS bits set the sample count limit for the arming function. The sample count limit is set independently for each channel.

**Table 160. Positive arming window size definitions (moving average mode)**

| ARM_WS_P[1] | ARM_WS_P[0] | Positive window size |
|---|---|---|
| 0 | 0 | 2 |
| 0 | 1 | 4 |
| 1 | 0 | 8 |
| 1 | 1 | 16 |

**Table 161. Negative arming window size definitions (moving average mode)**

| ARM_WS_N[1] | ARM_WS_N[0] | Negative window size |
|---|---|---|
| 0 | 0 | 2 |
| 0 | 1 | 4 |
| 1 | 0 | 8 |
| 1 | 1 | 16 |

**Table 162. Arming count limit definitions (count mode)**

| ARM_WS_N[1] | ARM_WS_N[0] | ARM_WS_P[1] | ARM_WS_P[0] | Sample count limit |
|---|---|---|---|---|
| Don't Care | Don't Care | 0 | 0 | 1 |
| Don't Care | Don't Care | 0 | 1 | 3 |
| Don't Care | Don't Care | 1 | 0 | 7 |
| Don't Care | Don't Care | 1 | 1 | 15 |

### 8.2.29 Arming threshold registers (CH0_ARM_T_P CHx_ARM_T_P, CH0_ARM_T_N CHx_ARM_T_N)

The arming threshold registers contain the positive and negative thresholds to be used by the arming function for each channel. Refer to Section 8.9: Arming function for more details regarding the arming function.

These registers can be written during initialization but are locked once the ENDINIT bit is set. Refer to Section 8.2.6: Device lock register (DEVLOCK_WR). The registers are included in the read/write array error detection.

**Table 163. Arming threshold registers (CH0_ARM_T_P CHx_ARM_T_P, CH0_ARM_T_N CHx_ARM_T_N)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $46 | CH0_ARM_T_P | ARM_T_P[7:0] | | | | | | | |
| $47 | CH0_ARM_T_N | ARM_T_N[7:0] | | | | | | | |
| $4E | CH1_ARM_T_P | ARM_T_P[7:0] | | | | | | | |
| $4F | CH1_ARM_T_N | ARM_T_N[7:0] | | | | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The values programmed into the threshold registers are the threshold values used for the arming function as described in Section 8.9: Arming function. The threshold registers hold independent unsigned 8-bit values for each channel and polarity. Each threshold increment is equivalent to 1 output LSB, 10-bit. Table 164. Example threshold register values and corresponding threshold shows examples of some threshold register values and the corresponding threshold.

**Table 164. Example threshold register values and corresponding threshold**

| Device Range (g) | Sensitivity (12 bit, LSB/g) | Arming thresh-old resolution (10 bit, LSB/g) | Range of arm threshold (g) | Programmed thresholds | | | |
|---|---|---|---|---|---|---|---|
| | | | | Positive (Decimal) | Negative (Decimal) | Positive threshold (g) | Negative threshold (g) |
| 125 | 16.3760 | 4.0940 | 62.2863 | 40 | 12 | 10 | –3 |
| 62 | 33.0161 | 8.2540 | 30.8940 | 123 | 24 | 15 | –3 |
| 50 | 40.9400 | 10.2350 | 24.9145 | 245 | 61 | 24 | –6 |
| 25 | 81.8800 | 20.4700 | 12.4573 | 245 | 61 | 12 | –3 |
| 16 | 127.9375 | 31.9844 | 7.9726 | 223 | 95 | 7 | –3 |

If either the positive or negative threshold for one channel is programmed to 0x00, comparisons are disabled for only that polarity. The arming function still operates for the opposite polarity. If both the positive and negative arming thresholds for one channel are programmed to 0x00, the arming function for the associated channel is disabled and the output pin is set to high impedance, regardless of the value of the ARM_CFG bits in the CH0_CFG_U4 CHx_CFG_U4 register.

### 8.2.30 Offset cancellation user configuration register (OC_PHASE_CFG)

The offset cancellation user configuration register is a user programmable read/write register which contains offset cancellation configuration information. The register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode.

**Table 165. Offset cancellation user configuration register (OC_PHASE_CFG)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $50 | OC_PHASE_CFG | CH0_OCFINAL | RESERVED CH1_OCFINAL | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.30.1 *Channel 0 and Channel 1 offset cancellation final phase control bit (CH0_OCFINAL, CH1_OCFINAL)*

The channel 0 offset cancellation final phase control bit provides the option for the user to control the final offset cancellation phase for normal mode as shown in Table 166. Channel 0 offset cancellation final phase control bit (CH0_OCFINAL, CH1_OCFINAL).

**Table 166. Channel 0 offset cancellation final phase control bit (CH0_OCFINAL, CH1_OCFINAL)**

| CH0_OCFINAL | Channel 0 offset cancellation final phase for normal mode |
|---|---|
| 0 | Phase 6 (a or b) as specified in the table in Section 8.6.4.6: Offset cancellation |
| 1 | Phase 5 as specified in the table in Section 8.6.4.6: Offset cancellation<br>(Rate Limiting is always bypassed) |

The channel 1 offset cancellation final phase control bit provides the option for the user to control the final offset cancellation phase for normal mode as shown in Table 167. Channel 1 offset cancellation final phase control bit (CH0_OCFINAL, CH1_OCFINAL).

**Table 167. Channel 1 offset cancellation final phase control bit (CH0_OCFINAL, CH1_OCFINAL)**

| CH1_OCFINAL | Channel 1 offset cancellation final phase for normal mode |
|---|---|
| 0 | Phase 6 (a or b) as specified in the table in Section 8.6.4.6: Offset cancellation |
| 1 | Phase 5 as specified in the table in Section 8.6.4.6: Offset cancellation |

| CH1_OCFINAL | Channel 1 offset cancellation final phase for normal mode |
|---|---|
| | (Rate Limiting is always bypassed) |

### 8.2.31 User offset calibration registers (Chx_U_OFFSET_L, Chx_U_OFFSET_H)

The user offset calibration registers contain a user programmable 16-bit signed offset correction value for the sensor data.

These registers can be written during initialization but are locked once the ENDINIT bit is set. Refer to Section 8.2.6: Device lock register (DEVLOCK_WR). The registers are included in the read/write array error detection.

**Table 168. User offset calibration registers (Chx_U_OFFSET_L, Chx_U_OFFSET_H)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $55 | CH0_U_OFFSET_L | CH0_U_OFFSET[7:0] | | | | | | | |
| $56 | CH0_U_OFFSET_H | CH0_U_OFFSET[15:8] | | | | | | | |
| $5D | CH1_U_OFFSET_L | CH1_U_OFFSET[7:0] | | | | | | | |
| $5E | CH1_U_OFFSET_H | CH1_U_OFFSET[15:8] | | | | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The value programmed into the user offset calibration register is directly added to the sensor data after the user sensitivity scaling but before the offset cancellation. See Section 8.6.4.9: Output scaling for scaling of the CHx_U_OFFSET value. The CHx-_U_OFFSET register has the same resolution as the sensor value in the SNSDATAx registers. A 1 LSB change in the CHx-_U_OFFSET register will result in a 1 LSB change to the value in the SNSDATAx registers.

*Note: The user offset calibration register range is larger than the full scale range of the output. The user must take care to ensure that the value stored in this register does not result in a compressed output range or a railed output.*

### 8.2.32 Channel-specific status register (CH0_STAT, CH1_STAT)

The channel-specific status register is a registers are read-only registers which contains sensor data-specific status information.

This register is These registers are readable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode.

**Table 169. Channel-specific status register (CH0_STAT, CH1_STAT)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $60 | CH0_STAT | SIGNALCLIP | OCPHASE[2:0] | | | ST_INCMPLT | ST_ACTIVE | OFFSET_ERR | ST_ERROR |
| $70 | CH1_STAT | SIGNALCLIP | OCPHASE[2:0] | | | ST_INCMPLT | ST_ACTIVE | OFFSET_ERR | ST_ERROR |
| Reset Value | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

#### *8.2.32.1 Signal clipped status bit (SIGNALCLIP)*

In DSI3 mode, SPI mode, and I²C mode, the signal clipped status bit is set if the output of the sinc filter reaches either the maximum or minimum value. The SIGNALCLIP bit is cleared on a read of the CHx_STAT register through any communication interface or on a data transmission that includes the error in the status field.

In PSI5 mode, the SIGNALCLIP bit has no impact on device operation or performance.

#### *8.2.32.2 Offset cancellation phase status (OCPHASE[2:0])*

The offset cancellation phase status bits indicate the current phase of the offset cancellation filter as described in Section 8.6.4.6: Offset cancellation.

**Table 170. Offset cancellation phase status (OCPHASE[2:0])**

| OCPHASE[2:0] | Offset cancellation startup phase | Offset low-pass filter frequency (Hz) |
|---|---|---|
| 000 | Phase 0 | 163.8 |
| 001 | Phase 1 | 40.96 |
| 010 | Phase 2 | 10.24 |
| 011 | Phase 3 | 2.560 |
| 100 | Phase 4 | 0.640 |
| 101 | Phase 5 | 0.160 |
| 110 | Phase 6 / Normal Mode | 0.04 |
| 111 | Not Applicable | |

#### 8.2.32.3 *Self-test incomplete (ST_INCMPLT)*

The self-test incomplete bit is set after a device reset and is cleared when one of the analog or digital self-tests modes are enabled in the ST_CTRL register (ST_CTRL[3] = logic 1 | ST_CTRL[2] = logic 1 | | ST_CTRL[1] = logic 1 | | ST_CTRL[0] = logic 1) or the PSI5 internal self-test procedure has started.

**Table 171. Self-test incomplete (ST_INCMPLT)**

| ST_INCMPLT | Condition |
|---|---|
| 0 | An Analog or Digital Self-test has been activated since the last reset |
| 1 | No Analog or Digital Self-test has not been activated since the last reset AND the PSI5 internal self-test procedure has not completed |

#### 8.2.32.4 *Self-test active flag (ST_ACTIVE)*

The self-test active bit is set if any self-test mode is currently active, including the PSI5 internal self-test or a self-test voltage is applied to the transducer. The self-test active bit is cleared when no self-test mode is active and no self-test voltage is applied to the transducer.

*ST_ACTIVE = ST_CTRL[3] | ST_CTRL[2] |ST_CTRL[1] | ST_CTRL[0] | (self-test voltage applied to transducer)*

#### 8.2.32.5 *Offset error flag (OFFSET_ERR)*

The offset error flag is set if the sensor signal reaches the offset limit specified in Section 7.6: Electrical characteristics - inertial sensor signal chain: High g. The OFFSET_ERR bit is cleared on a read of the CHx_STAT register through any communication interface or on a data transmission that includes the error in the status field. See Section 8.2.15.2: PSI5 error latching enable bit (PSI5_ERRLATCH) for details on a method to disable the automatic clearing of this error in PSI5 mode.

**Table 172. Offset error flag (OFFSET_ERR)**

| OFFSET_ERR | Error condition |
|---|---|
| 0 | No error detected |
| 1 | Offset error detected |

#### 8.2.32.6 *Self-test error flag (ST_ERROR)*

The self-test error flag is set if the PSI5 startup self-test fails as described in Section 6.6.2.5. This bit can only be cleared by a device reset.

### 8.2.33 Device status copy register (DEVSTAT_COPY)

The device status copy register is a read-only register which contains a copy of the device status information contained in the DEVSTAT register. See Section 8.2.2: Device status registers (DEVSTATx) for details regarding the DEVSTAT register contents.

This register is readable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode. A read of the DEVSTAT_COPY register has the same effect as a read of the DEVSTAT register.

**Table 173. Device status copy register (DEVSTAT_COPY)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $61 | DEVSTAT_COPY | CH0_ERR | RESERVED<br>CH1_ERR | COMM_ERR | MEMTEMP_ERR | SUPPLY_ERR | TESTMODE | DEVRES | DEVINIT |

### 8.2.34 Sensor data #0 registers (CHx_SNSDATA0_L, CHx_SNSDATA0_H)

The sensor data #0 registers are read-only registers which contain the 16-bit sensor data. The data type for the sensor data #0 registers is selected by the DATATYPE0 bits in the CHx_CFG_U3 register. See Section 8.2.25.2: Channel 0 data type 0 selection bits (CHxDATATYPE0). See Section 8.6.4.9: Output scaling for details regarding the 16-bit sensor data.

These registers are readable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode. In I²C mode, the SNSDA-TA0_H register value is latched on a read of the SNSDATA0_L register value until the SNSDATA0_H register is read. To avoid data mismatch, it is required that the user always read the registers in sequence, SNSDATA0_L register first, followed by the SNSDATA0_H register.

**Table 174. Sensor data #0 registers (CHx_SNSDATA0_L, CHx_SNSDATA0_H)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $62 | CH0_SNSDATA0_L | CH0_SNSDATA0[7:0] | | | | | | | |
| $63 | CH0_SNSDATA0_H | CH0_SNSDATA0[15:8] | | | | | | | |
| $72 | CH1_SNSDATA0_L | CH1_SNSDATA0[7:0] | | | | | | | |
| $73 | CH1_SNSDATA0_H | CH1_SNSDATA0[15:8] | | | | | | | |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.2.35 Sensor data #1 registers (CHx_SNSDATA1_L, CHx_SNSDATA1_H)

The sensor data #1 registers are read-only registers which contain the 16-bit sensor data. The data type for the sensor data #1 registers is selected by the DATATYPE1 bits in the CHx_CFG_U3 register. See Section 8.2.25.3: Channel 0 data type 1 selection bits (CHxDATATYPE1). See Section 8.6.4.9: Output scaling for details regarding the 16-bit sensor data.

These registers are readable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode. In I²C mode, the SNSDA-TA1_H register value is latched on a read of the SNSDATA1_L register value until the SNSDATA1_H register is read. To avoid data mismatch, it is required that the user always read the registers in sequence, SNSDATA1_L register first, followed by the SNSDATA1_H register.

**Table 175. Sensor data #1 registers (CHx_SNSDATA1_L, CHx_SNSDATA1_H)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $64 | CH0_SNSDATA1_L | CH0_SNSDATA1[7:0] | | | | | | | |
| $65 | CH0_SNSDATA1_H | CH0_SNSDATA1[15:8] | | | | | | | |
| $74 | CH1_SNSDATA1_L | CH1_SNSDATA1[7:0] | | | | | | | |
| $75 | CH1_SNSDATA1_H | CH1_SNSDATA1[15:8] | | | | | | | |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.2.36 Channel-specific factory configuration register (CHx_CFG_F)

The channel-specific configuration register is registers are factory programmable OTP registers which contains channel specific configuration information. This register is These registers are included in the factory programmed OTP array error detection.

This register is These registers are readable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode when ENDINIT is not set. See Section 8.2.10: UF region selection registers (UF_REGION_x) for details on the register read process for this register.

Table 176. **Channel-specific factory configuration register (CHx_CFG_F)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $A0 | CH0_CFG_F | DEV_RANGE[3:0] | | | | RESERVED | RESERVED | AXIS[1:0] | |
| $B0 | CH1_CFG_F | DEV_RANGE[3:0] | | | | RESERVED | RESERVED | AXIS[1:0] | |

#### 8.2.36.1 *Range indication bits (RANGE[3:0])*

The range indication bits indicate the full scale range of the channel as shown in Table 177. Range indication bits (RANGE[3:0]).

Table 177. **Range indication bits (RANGE[3:0])**

| RANGE[3] | RANGE[2] | RANGE[1] | RANGE[0] | Acceleration range |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Low |
| 0 | 0 | 0 | 1 | RESERVED |
| 0 | 0 | 1 | 0 | Medium |
| 0 | 0 | 1 | 1 | RESERVED |
| 0 | 1 | 0 | 0 | High |
| 0 | 1 | 0 | 1 | RESERVED |
| 0 | 1 | 1 | 0 | RESERVED |
| 0 | 1 | 1 | 1 | RESERVED |
| 1 | 0 | 0 | 0 | RESERVED |
| 1 | 0 | 0 | 1 | RESERVED |
| 1 | 0 | 1 | 0 | RESERVED |
| 1 | 0 | 1 | 1 | RESERVED |
| 1 | 1 | 0 | 0 | RESERVED |
| 1 | 1 | 0 | 1 | RESERVED |
| 1 | 1 | 1 | 0 | RESERVED |
| 1 | 1 | 1 | 1 | RESERVED |

#### 8.2.36.2 *Axis indication bits (AXIS[1:0])*

The axis indication bits indicate the axes of sensitivity for the channel as shown in Table 178. Axis indication bits (AXIS[1:0]).

Table 178. **Axis indication bits (AXIS[1:0])**

| AXIS[1] | AXIS[0] | Axis of sensitivity |
|---|---|---|
| 0 | 0 | X |
| 0 | 1 | Y |
| 1 | 0 | Z |
| 1 | 1 | RESERVED |

### 8.2.37 Self-test deflection storage registers

The self-test deflection registers are factory programmable OTP registers which contain the nominal self-test values for the various self-tests at 25 °C. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode when ENDINIT is not set. See Section 8.2.10: UF region selection registers (UF_REGION_x) for details on the register read process for these registers.

**Table 179. Self-test deflection storage registers**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $A2 | CH0_STL_P_L | CH0_STL_P[7:0] | | | | | | | |
| $A3 | CH0_STL_P_H | CH0_STL_P[15:8] | | | | | | | |
| $A4 | CH0_STH_P_L | CH0_STH_P[7:0] | | | | | | | |
| $A5 | CH0_STH_P_H | CH0_STH_P[15:8] | | | | | | | |
| $A6 | CH0_STL_N_L | CH0_STL_N[7:0] | | | | | | | |
| $A7 | CH0_STL_N_H | CH0_STL_N[15:8] | | | | | | | |
| $A8 | CH0_STH_N_L | CH0_STH_N[7:0] | | | | | | | |
| $A9 | CH0_STH_N_H | CH0_STH_N[15:8] | | | | | | | |
| $B2 | CH1_STL_P_L | CH1_STL_P[7:0] | | | | | | | |
| $B3 | CH1_STL_P_H | CH1_STL_P[15:8] | | | | | | | |
| $B4 | CH1_STH_P_L | CH1_STH_P[7:0] | | | | | | | |
| $B5 | CH1_STH_P_H | CH1_STH_P[15:8] | | | | | | | |
| $B6 | CH1_STL_N_L | CH1_STL_N[7:0] | | | | | | | |
| $B7 | CH1_STL_N_H | CH1_STL_N[15:8] | | | | | | | |
| $B8 | CH1_STH_N_L | CH1_STH_N[7:0] | | | | | | | |
| $B9 | CH1_STH_N_H | CH1_STH_N[15:8] | | | | | | | |

The self-test values are positive and negative deflection values, measured at the factory, and factory programmed for each device. The stored value is equal to one half of the absolute value of the difference be tween the factory measured Chx-_SNSDATA0 register value with the analog self-test active and the factory measured CHx_SNSDATA0 register value for offset at nominal temperature (Data is aligned to the 12-bit sensor data).

For medium and high g variants, both the self-test and offset values are measured with the user scaling set to 1: U_SNS_SHIFT[1:0] = 0x2 and U_SNS_MULT[7:0] = 0x00.

For low g variant both the self test and offset values are measured with the user scaling set to 0.5: U_SNS_SHIFT[1:0] = 0x0 and U_SNS_MULT[7:0] = 0xFF.

$CH0\_STL\_P = 0.5 * [CH0\_SNSDATA0_{ST\_CTRL=0x8} - CH0\_SNSDATA0_{ST\_CTRL=0x0}]$

$CH0\_STL\_N = 0.5 * [CH0\_SNSDATA0_{ST\_CTRL=0x0} - CH0\_SNSDATA0_{ST\_CTRL=0x9}]$

$CH0\_STH\_P = 0.5 * [CH0\_SNSDATA0_{ST\_CTRL=0xA} - CH0\_SNSDATA0_{ST\_CTRL=0x0}]$

$CH0\_STH\_N = 0.5 * [CH0\_SNSDATA0_{ST\_CTRL=0x0} - CH0\_SNSDATA0_{ST\_CTRL=0xB}]$

$CH1\_STL\_P = 0.5 * [CH1\_SNSDATA0_{ST\_CTRL=0x8} - CH1\_SNSDATA0_{ST\_CTRL=0x0}]$

$CH1\_STL\_N = 0.5 * [CH1\_SNSDATA0_{ST\_CTRL=0x0} - CH1\_SNSDATA0_{ST\_CTRL=0x9}]$

$CH1\_STH\_P = 0.5 * [CH1\_SNSDATA0_{ST\_CTRL=0xA} - CH1\_SNSDATA0_{ST\_CTRL=0x0}]$

$CH1\_STH\_N = 0.5 * [CH1\_SNSDATA0_{ST\_CTRL=0x0} - CH1\_SNSDATA0_{ST\_CTRL=0xB}]$

Two self-test values are stored and available for comparison: a high self-test value and a low self-test value. The self-test value is controlled by the user via the ST_CTRL[3:0] bits in the CHx_CFG_U5 registers as described in Section 8.2.27.1: Self-test control bits (ST_CTRL[3:0]).

When self-test is activated, the sensor data can be compared to the values in the appropriate registers. The difference from the measured deflection value, and the nominal deflection value stored in the register shall not fall outside the self-test accuracy limits specified in Section 7.7: Electrical characteristics - inertial sensor signal chain: Medium g ($\Delta ST_{ACC}$). See Section 8.6.2: Inertial sensor self-test interface for more details on calculating the self-test limits.

### 8.2.38 IC type register

The IC type register is a factory programmable OTP register which contains the IC type as defined in Table 180. IC type register. This register is included in the factory programmed OTP array error detection.

**Table 180. IC type register**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $C0 | ICTYPEID | 0 | 0 | 0 | 0 | 0 | 0 | 0<br>1 | 1 |

### 8.2.39 IC revision register

The IC revision register is a factory programmable OTP register which contains the IC revision. The upper nibble contains the main IC revision. The lower nibble contains the sub IC revision. This register is included in the factory programmed OTP array error detection.

This register is readable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode when ENDINIT is not set. See Section 8.2.10: UF region selection registers (UF_REGION_x) for details on the register read process for this register.

**Table 181. IC revision register**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $C1 | ICREVID | ICREVID[7:0] | | | | | | | |

### 8.2.40 IC manufacturer identification register

The IC manufacturer identification register is a factory programmable OTP register which identifies ST as the IC manufacturer. This register is included in the factory programmed OTP array error detection.

This register is readable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode when ENDINIT is not set. See Section 8.2.10: UF region selection registers (UF_REGION_x) for details on the register read process for this register.

**Table 182. IC manufacturer identification register**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $C2 | ICMFGID | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

### 8.2.41 Part number register

The part number registers are factory programmed OTP registers which include the numeric portion of the device part number. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode when ENDINIT is not set. See Section 8.2.10: UF region selection registers (UF_REGION_x) for details on the register read process for these registers.

**Table 183. Part number register**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $C4 | PN0 | PN0[7:0] | | | | | | | |
| $C5 | PN1 | PN1[7:0] | | | | | | | |

**Table 184. Part number: Protocol type**

| PN1[7:4] | Protocol type |
|---|---|
| 0 | User Selectable |
| 1 | SPI32 |
| 2 | DSI3 |
| 3 | PSI5 |

| PN1[7:4] | Protocol type |
|---|---|
| 4 | I²C |
| 5 - 15 | RESERVED |

**Table 185. Part number: Unused**

| PN0[3:0] | N/A |
|---|---|
| 0 | 0 |

**Table 186. Part number: Axis**

| PN1[3:0] | Channel 0 axis | Channel 1 axis |
|---|---|---|
| 0 | RESERVED | |
| 1 | RESERVED | |
| 2 | RESERVED | |
| 3 | X | Y |
| 4 | X | Z |
| 5 | RESERVED | |
| 6 | RESERVED | |
| 7 | Y | Z |
| 8 - 15 | RESERVED | |

**Table 187. Part number: Channel 0 range**

| PN0[7:4] | Channel 0 range |
|---|---|
| 0 | RESERVED |
| 1 | RESERVED |
| 2 | Medium g |
| 3 | High g |
| 4 - 15 | RESERVED |

**Table 188. Part number: Channel 1 range**

| PN0[3:0] | Channel 1 range |
|---|---|
| 0 | RESERVED |
| 1 | Low g |
| 2 | Medium g |
| 3 | High g |
| 4 - 15 | RESERVED |

### 8.2.42 Device serial number registers

The serial number registers are factory programmed OTP registers which include the unique serial number of the device. Serial numbers begin at 1 for all produced devices in each lot and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 16-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode when ENDINIT is not set. See Section 8.2.10: UF region selection registers (UF_REGION_x) for details on the register read process for these registers.

**Table 189. Device serial number registers**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $C6 | SN0 | SN[7:0] | | | | | | | |
| $C7 | SN1 | SN[15:8] | | | | | | | |
| $C8 | SN2 | SN[23:16] | | | | | | | |
| $C9 | SN3 | SN[31:24] | | | | | | | |
| $CA | SN4 | SN[39:32] | | | | | | | |

Table 190. Example serial number decoding shows an example serial number decoding:

**Table 190. Example serial number decoding**

| Serial number | Full serial number | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Stored Data Format | SN4 | | | | SN3 | | | | SN2 | | | | SN1 | | | | SN0 | | | |
| Serial Number Mapping | Test ID | | Lot Number | | | | | | | | | | Serial Number within a lot | | | | | | | |
| Example SN (Hex) | 1 | | 0 | | 0 | | 0 | | 5 | | 2 | | 0 | | 0 | | 5 | | 0 | |
| Example SN (Binary) | 00 | 01 | 00 | 00 | 00 | 00 | 00 | 00 | 01 | 01 | 00 | 10 | 00 | 00 | 00 | 00 | 01 | 01 | 00 | 00 |
| Example Lot Number | 0b 00 00 00 00 0101 0010 = 0x0052 = 82d | | | | | | | | | | | | | | | | | | | |
| Example Serial Number | 16'b 00 00 00 00 01 01 00 00 = 0x0050 = 80d | | | | | | | | | | | | | | | | | | | |

### 8.2.43 ASIC wafer ID registers

The ASIC wafer ID registers are factory programmed OTP registers which include the wafer number, wafer X, and Y coordinates and the wafer lot number for the device ASIC. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode when ENDINIT is not set. See Section 8.2.10: UF region selection registers (UF_REGION_x) for details on the register read process for these registers.

**Table 191. ASIC wafer ID registers**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $CB | ASICWFR# | ASICWFR#[7:0] | | | | | | | |
| $CC | ASICWFR_X | ASICWFR_X[7:0] | | | | | | | |
| $CD | ASICWFR_Y | ASICWFR_Y[7:0] | | | | | | | |
| $D0 | ASICWLOT_L | ASICWLOT_L[7:0] | | | | | | | |
| $D1 | ASICWLOT_H | ASICWLOT_H[7:0] | | | | | | | |

### 8.2.44 Transducer wafer ID registers

The transducer wafer ID registers are factory programmed OTP registers which include the wafer number, wafer X, and Y coordinates and the wafer lot number for the device transducers. The upper 3 bits of the TRNSWFR# register include a transducer and assembly revision counter. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode when ENDINIT is not set. See Section 8.2.10: UF region selection registers (UF_REGION_x) for details on the register read process for these registers.

**Table 192. Transducer wafer ID registers**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $D2 | TRNS1WFR_X | TRNS1WFR_X[7:0] | | | | | | | |
| $D3 | TRNS1WFR_Y | TRNS1WFR_Y[7:0] | | | | | | | |
| $D4 | TRNS1LOT_L | TRNS1LOT_L[7:0] | | | | | | | |
| $D5 | TRNS1LOT_H | TRNS1LOT_H[7:0] | | | | | | | |
| $DA | TRNS1WFR# | TRNS_ASSY_REV[2:0] | | | TRNS1WFR#[4:0] | | | | |

## 8.2.45 Device revision ID register

The Device revision ID register is a factory-programmed OTP register that includes the device revision information. This register is included in the factory-programmed OTP array error detection.

This register is readable in DSI3 mode, SPI mode, I²C mode, or PSI5 Programming mode when the ENDINIT is not set. See Section 8.2.10: UF region selection registers (UF_REGION_x) for details on the register read process for this register.

**Table 193. Device revision ID register**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $CE | DVCREVID | Reserved | Reserved | Reserved | Reserved | DVCREVID[3:0] | | | |

| DVCREVID[3:0] | Sample revision |
|---|---|
| 0-14 | Engineering device |
| 15 | Qualifiable and production device |

## 8.2.46 User data registers (USERDATA_0 - USERDATA_E)

User data registers are user programmable OTP registers which contain user-specific information. These registers are included in the user programmed OTP array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 Programming Mode when ENDINIT is not set. See Section 8.2.10: UF region selection registers (UF_REGION_x) for details on the register read process for these registers.

**Table 194. User data registers (USERDATA_0 - USERDATA_E)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $E0 | USERDATA_0 | USERDATA_0[7:0] | | | | | | | |
| $E1 | USERDATA_1 | USERDATA_1[7:0] | | | | | | | |
| $E2 | USERDATA_2 | USERDATA_2[7:0] | | | | | | | |
| $E3 | USERDATA_3 | USERDATA_3[7:0] | | | | | | | |
| $E4 | USERDATA_4 | USERDATA_4[7:0] | | | | | | | |
| $E5 | USERDATA_5 | USERDATA_5[7:0] | | | | | | | |
| $E6 | USERDATA_6 | USERDATA_6[7:0] | | | | | | | |
| $E7 | USERDATA_7 | USERDATA_7[7:0] | | | | | | | |
| $E8 | USERDATA_8 | USERDATA_8[7:0] | | | | | | | |
| $E9 | USERDATA_9 | USERDATA_9[7:0] | | | | | | | |
| $EA | USERDATA_A | USERDATA_A[7:0] | | | | | | | |
| $EB | USERDATA_B | USERDATA_B[7:0] | | | | | | | |
| $EC | USERDATA_C | USERDATA_C[7:0] | | | | | | | |
| $ED | USERDATA_D | USERDATA_D[7:0] | | | | | | | |
| $EE | USERDATA_E | USERDATA_E[7:0] | | | | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.2.46.1 *PSI5 initialization phase 2 data transmissions of user data*

In PSI5 Mode, the values of the user data registers are transmitted in Initialization phase 2 as shown in Table 195. PSI5 initialization phase 2 data transmissions of user data. See Section 10.4.2.1: PSI5 initialization phase 2 data transmissions for details on the PSI5 Initialization Phase 2 Transmissions.

**Table 195. PSI5 initialization phase 2 data transmissions of user data**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $E0 | USERDATA_0 | RESERVED<br>Channel 1 F1: D1 | | | | Channel 0 F1: D1 | | | |
| $E1 | USERDATA_1 | Channel 0 F3: D5 | | | | Channel 0 F3: D4 | | | |
| $E2 | USERDATA_2 | Channel 0 F4: D7 | | | | Channel 0 F4: D6 | | | |
| $E3 | USERDATA_3 | Channel 0 F5: D9 | | | | Channel 0 F5: D8 | | | |
| $E4 | USERDATA_4 | Channel 0 F6: D11 | | | | Channel 0 F6: D10 | | | |
| $E5 | USERDATA_5 | Channel 0 F7: D13 | | | | Channel 0 F7: D12 | | | |
| $E6 | USERDATA_6 | PSI5_INIT2_D19 = 0, Channel 0 F9: D32<br>PSI5_INIT2_D19 = 1, Ch 0 F9: D32 = Ch 0 F9: D19 = Ch 1 F9: D19 | | | | Channel 0 F7: D14 | | | |
| $E7 | USERDATA_7 | Channel 0 F8: D16<br>Channel 0 F8: D16 = Channel 1 F8: D16 | | | | Channel 0 F8: D15<br>Channel 0 F8: D15 = Channel 1 F8: D15 | | | |
| $E8 | USERDATA_8 | Channel 0 F8: D18<br>Channel 0 F8: D18 = Channel 1 F8: D18 | | | | Channel 0 F8: D17<br>Channel 0 F8: D17 = Channel 1 F8: D17 | | | |
| $E9 | USERDATA_9 | RESERVED<br>Channel 1 F3: D5 | | | | RESERVED<br>Channel 1 F3: D4 | | | |
| $EA | USERDATA_A | RESERVED<br>Channel 1 F4: D7 | | | | RESERVED<br>Channel 1 F4: D6 | | | |
| $EB | USERDATA_B | RESERVED<br>Channel 1 F5: D9 | | | | RESERVED<br>Channel 1 F5: D8 | | | |
| $EC | USERDATA_C | RESERVED<br>Channel 1 F6: D11 | | | | RESERVED<br>Channel 1 F6: D10 | | | |
| $ED | USERDATA_D | RESERVED<br>Channel 1 F7: D13 | | | | RESERVED<br>Channel 1 F7: D12 | | | |
| $EE | USERDATA_E | RESERVED<br>PSI5_INIT2_D19 = 0, Channel 1 F9: D32<br>PSI5_INIT2_D19 = 1, Ch 1 F9: D32 = Ch 0 F9: D20 = Ch 1 F9: D20 | | | | RESERVED<br>Channel 1 F7: D14 | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.2.47 User data registers (USERDATA_10 - USERDATA_1E)

User data registers are user programmable OTP registers which contain user-specific information. These registers are included in the user programmed OTP array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I²C mode or PSI5 programming mode when ENDINIT is not set. See Section 8.2.10: UF region selection registers (UF_REGION_x) for details on the register read process for these registers.

**Table 196. User data registers (USERDATA_10 - USERDATA_1E)**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $F0 | USERDATA_10 | USERDATA_10[7:0] | | | | | | | |
| $F1 | USERDATA_11 | USERDATA_11[7:0] | | | | | | | |
| $F2 | USERDATA_12 | USERDATA_12[7:0] | | | | | | | |
| $F3 | USERDATA_13 | USERDATA_13[7:0] | | | | | | | |
| $F4 | USERDATA_14 | USERDATA_14[7:0] | | | | | | | |
| $F5 | USERDATA_15 | USERDATA_15[7:0] | | | | | | | |
| $F6 | USERDATA_16 | USERDATA_16[7:0] | | | | | | | |
| $F7 | USERDATA_17 | USERDATA_17[7:0] | | | | | | | |
| $F8 | USERDATA_18 | USERDATA_18[7:0] | | | | | | | |

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $F9 | USERDATA_19 | USERDATA_19[7:0] | | | | | | | |
| $FA | USERDATA_1A | USERDATA_1A[7:0] | | | | | | | |
| $FB | USERDATA_1B | USERDATA_1B[7:0] | | | | | | | |
| $FC | USERDATA_1C | USERDATA_1C[7:0] | | | | | | | |
| $FD | USERDATA_1D | USERDATA_1D[7:0] | | | | | | | |
| $FE | USERDATA_1E | USERDATA_1E[7:0] | | | | | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 8.2.48 Lock and CRC registers

The lock and CRC registers are automatically programmed OTP registers which include the lock bit, the block identifier, and the block OTP array CRC use for error detection.

These registers are automatically programmed when the corresponding data array is programmed to OTP using the Write OTP Enable register as documented in Section 8.2.7: Write OTP enable register.

**Table 197. Lock and CRC registers**

| Location | | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $5F | CRC_UF2 | LOCK_UF2 | 0 | 0 | 0 | CRC_UF2[3:0] | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $AF | CRC_F_A | LOCK_F_A | REGA_BLOCKID[2:0] | | | CRC_F_A[3:0] | | | |
| Reset Value | | 1 | 0 | 0 | 1 | Varies | | | |
| $BF | CRC_F_B | LOCK_F_B | REGB_BLOCKID[2:0] | | | CRC_F_B[3:0] | | | |
| Reset Value | | 1 | 0 | 1 | 0 | Varies | | | |
| $CF | CRC_F_C | LOCK_F_C | REGC_BLOCKID[2:0] | | | CRC_F_C[3:0] | | | |
| Reset Value | | 1 | 0 | 1 | 1 | Varies | | | |
| $DF | CRC_F_D | LOCK_F_D | REGD_BLOCKID[2:0] | | | CRC_F_D[3:0] | | | |
| Reset Value | | 1 | 1 | 0 | 0 | Varies | | | |
| $EF | CRC_F_E | LOCK_F_E | REGE_BLOCKID[2:0] | | | CRC_F_E[3:0] | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $FF | CRC_F_F | LOCK_F_F | REGF_BLOCKID[2:0] | | | CRC_F_F[3:0] | | | |
| Unprogrammed OTP Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 198. Lock bit, block identifier, and CRC states shows the state of the lock bits, the block identifiers, and the CRC for each register block before and after programming.

**Table 198. Lock bit, block identifier, and CRC states**

| Register block address | Lock bit bit[7] | | Block identifier bits[6:4] | | CRC bits[3:0] | |
|---|---|---|---|---|---|---|
| | Before programming | After programming | Before programming | After programming | Before programming | After programming |
| UF2 | 0 | 1 | 000 | 000 | 0000 | Varies |
| $Ax | 0 | 1 | N/A | 001 | N/A | Varies |
| $Bx | 0 | 1 | N/A | 010 | N/A | Varies |
| $Cx | 0 | 1 | N/A | 011 | N/A | Varies |
| $Dx | 0 | 1 | N/A | 100 | N/A | Varies |
| $Ex | 0 | 1 | 000 | 101 | 0000 | Varies |
| $Fx | 0 | 1 | 000 | 110 | 0000 | Varies |

## 8.2.49 Reserved registers

A register read command to a reserved register or a register with reserved bits will result in a valid response. The data for reserved bits may be logic 0 or logic 1.

A register write command to a reserved register or a register with reserved bits will execute and result in a valid response. The data for the reserved bits may be logic 0 or logic 1. A write to the reserved bits must always be '0' for normal device operation and performance.

### 8.2.50 Invalid register addresses

A register read command to a register address outside the addresses listed in Section 8.1: User accessible data array will result in a valid response. The data for the registers will be '0x00'.

A register write command to a register address outside the addresses listed in Section 8.1: User accessible data array will not execute, but will result in a valid response. The data for the registers will be '0x00'.

A register write command to a read-only register will not execute, but will result in a valid response. The data for the registers will be the current contents of the register.

## 8.3 OTP and read/write register array CRC verification

### 8.3.1 ST OTP registers

The following registers are internal OTP registers. These registers are verified by the OTP ECC as well as an independent 4-bit CRC for each 16 byte block.

**Table 199. Memory type code: ST OTP register**

| Memory type codes | |
|---|---|
| F | User readable register with OTP |

### 8.3.2 User OTP only registers

The following registers are user OTP registers. These registers are verified by the OTP ECC as well as an independent 4-bit CRC for each 16 byte block. The CRC verification uses a generator polynomial of $g(x) = X^4 + X^3 + 1$, with a seed value = '0000'. The bits are fed into the CRC calculation from right to left (MSB first) and from top to bottom (lowest address first) in the register map.

**Table 200. Memory type code: User OTP register**

| Memory type codes | |
|---|---|
| UF0 | One time user programmable OTP region 0 |
| UF1 | One time user programmable OTP region 1 |

### 8.3.3 OTP modifiable registers

The following registers are user read/write registers as well as OTP registers with writable mirror registers. The OTP registers are verified by the OTP ECC as well as an independent 4-bit CRC stored in the CRC_UF2 register.

The values read from OTP can be over-written while ENDINIT is not set. Once ENDINIT is set, the writable registers (all registers in the R/W and UF2 regions with the exception of the DEVLOCK_WR register) are verified by an additional continuous 4-bit CRC that is calculated on the entire array. The CRC verification uses a generator polynomial of $g(x) = X^4+X^3+1$, with a seed value = '0000'. The bits are fed into the CRC calculation from right to left (MSB first) and from top to bottom (lowest address first) in the register map.

Registers verified by the OTP CRC:

**Table 201. Memory type code: CRC verified OTP registers**

| Memory type codes | |
|---|---|
| UF2 | One time user programmable OTP region 3 with modifiable mirror registers |

Registers verified by the ENDINIT calculated CRC:

**Table 202. Memory type code: ENDINIT CRC verified OTP registers**

| Memory type codes | |
|---|---|
| UF2 | One time user programmable OTP region 3 with modifiable mirror registers |
| R/W | User writable register, with the exception of the DEVLOCK_WR register |

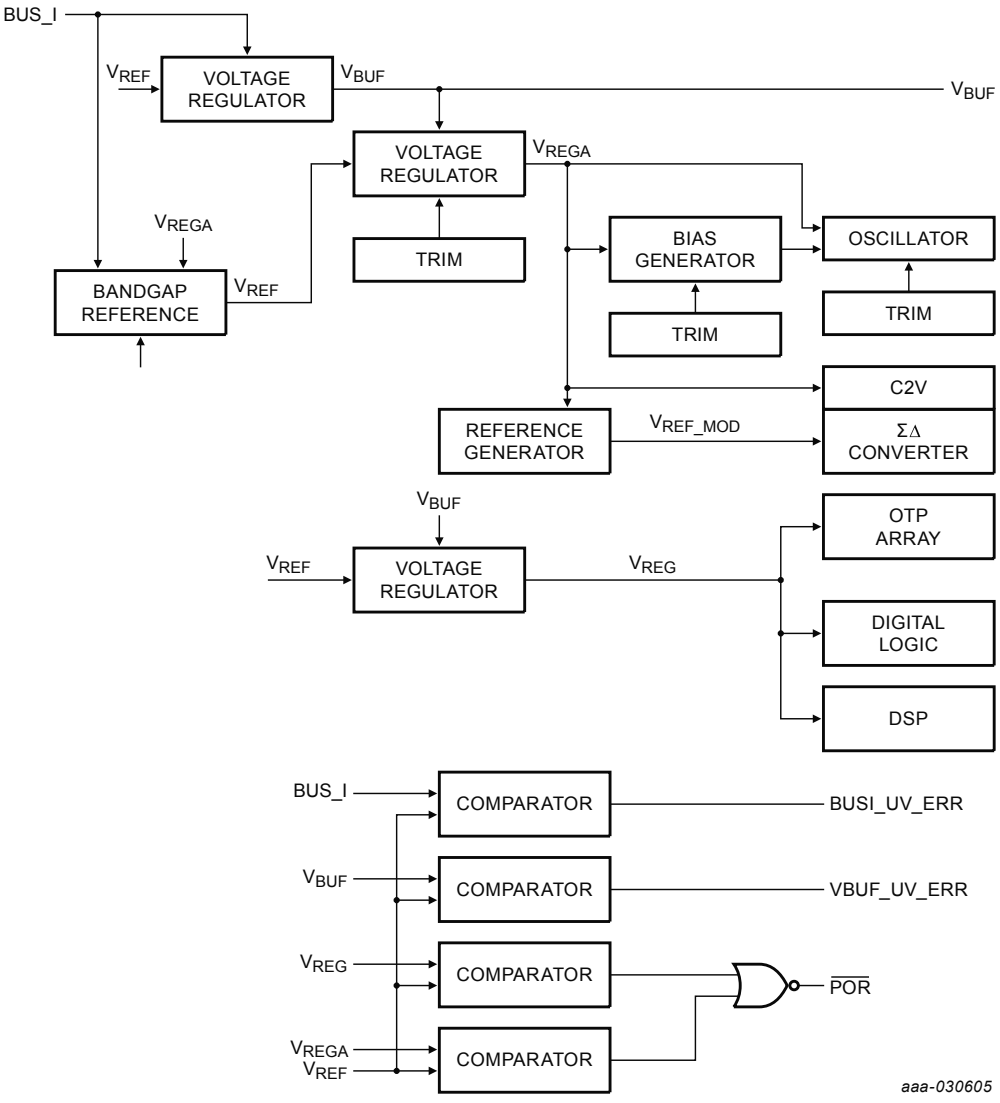
## 8.4 Voltage regulators

The device derives its internal supply voltage from the $V_{CC}$/BUS_I and $V_{SS}$ pins. The internal regulators are supplied by a buffer regulator ($V_{BUF}$) to provide immunity from EMC and supply dropouts on BUS_I. An external filter capacitor is required for $V_{BUF}$, as shown in Section 3: Application diagrams.

The voltage regulator module includes voltage monitoring circuitry which holds the device in reset following power-on until the internal voltages have increased above the under-voltage detection thresholds. The voltage monitor asserts undervoltage error flag as specified in Section 8.4.2: BUS_I, $V_{BUF}$, $V_{REG}$, $V_{REGA}$, undervoltage monitor when the external supply or internally regulated voltages fall below the undervoltage detection thresholds.

A reference generator provides a reference voltage for the ΣΔ converter.

**Figure 11. Voltage regulation and monitoring**



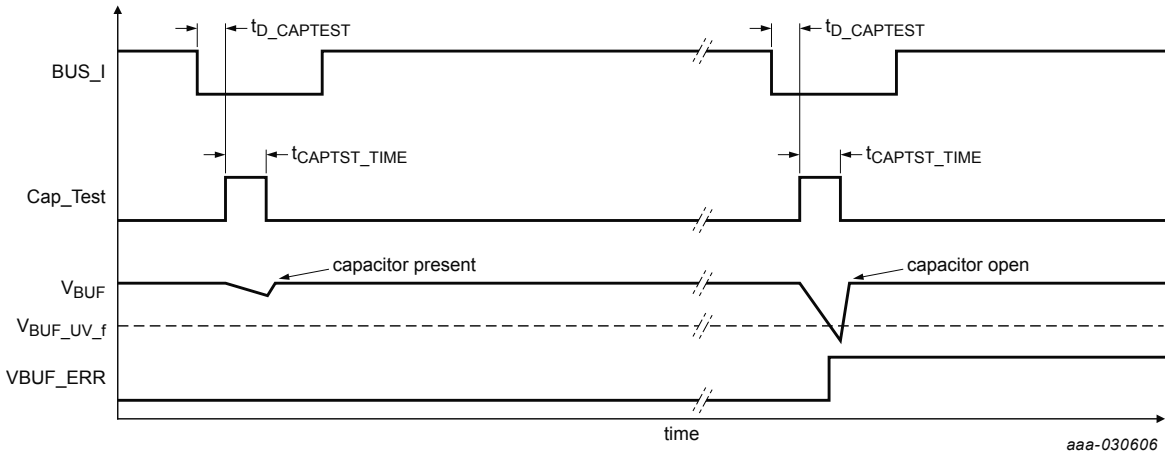
### 8.4.1 $V_{BUF}$ regulator capacitor and capacitor monitor

In DSI3 and PSI5 modes, the buffer regulator requires an external capacitor between the $V_{BUF}$ pin and the $V_{SS}$ pin. Section 3: Application diagrams shows the recommended types and values for each of these capacitors. A monitor circuit is incorporated to ensure predict-able operation if the connection to the external $V_{BUF}$ capacitor becomes open. If the external capacitor is not present, the regulator voltage will fall below the threshold specified in Section 7.4: Electrical characteristics - supply and I/O causing the VBUF_ERR bit to be set in the DEVSTAT1 register.

The $V_{BUF}$ capacitor is tested synchronous to the protocol transmissions as shown in the diagrams in Figure 12. $V_{BUF}$ capacitor monitor timing, DSI3, Figure 13. $V_{BUF}$ capacitor monitor timing, PSI5 synchronous mode, and Figure 14. $V_{BUF}$ capacitor monitor timing, psi5 asynchronous mode.

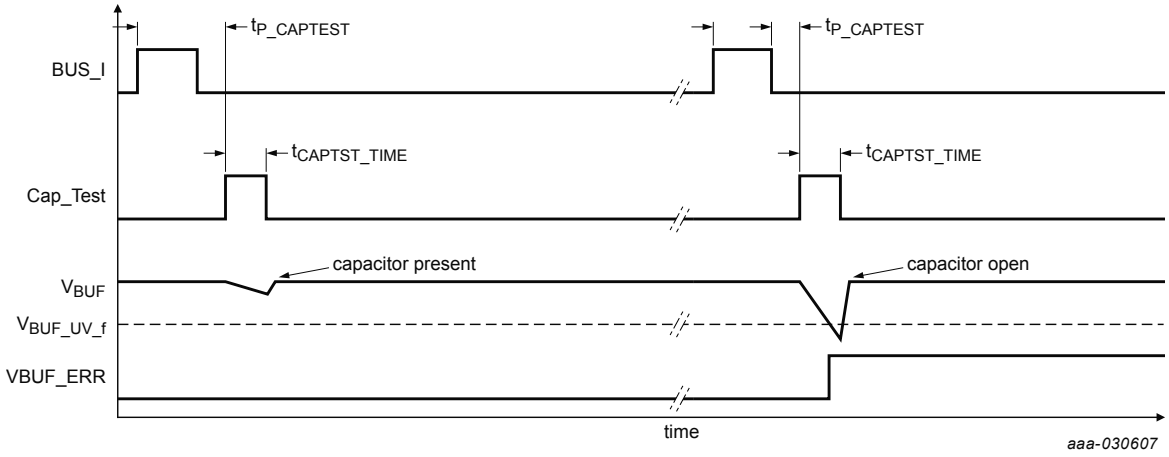
#### 8.4.1.1 *$V_{BUF}$ capacitance monitor timing, DSI3*

**Figure 12. $V_{BUF}$ capacitor monitor timing, DSI3**



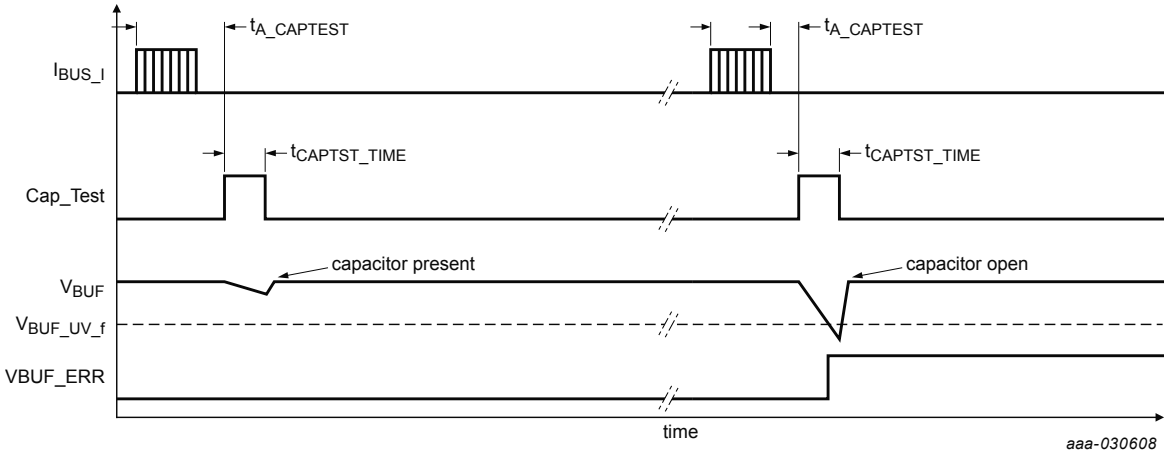

#### 8.4.1.2 *$V_{BUF}$ capacitance monitor timing, PSI5*

**Figure 13. $V_{BUF}$ capacitor monitor timing, PSI5 synchronous mode**



#### 8.4.1.3 *$V_{BUF}$ capacitance monitor timing, PSI5 asynchronous mode*

Figure 14. **$V_{BUF}$ capacitor monitor timing, psi5 asynchronous mode**



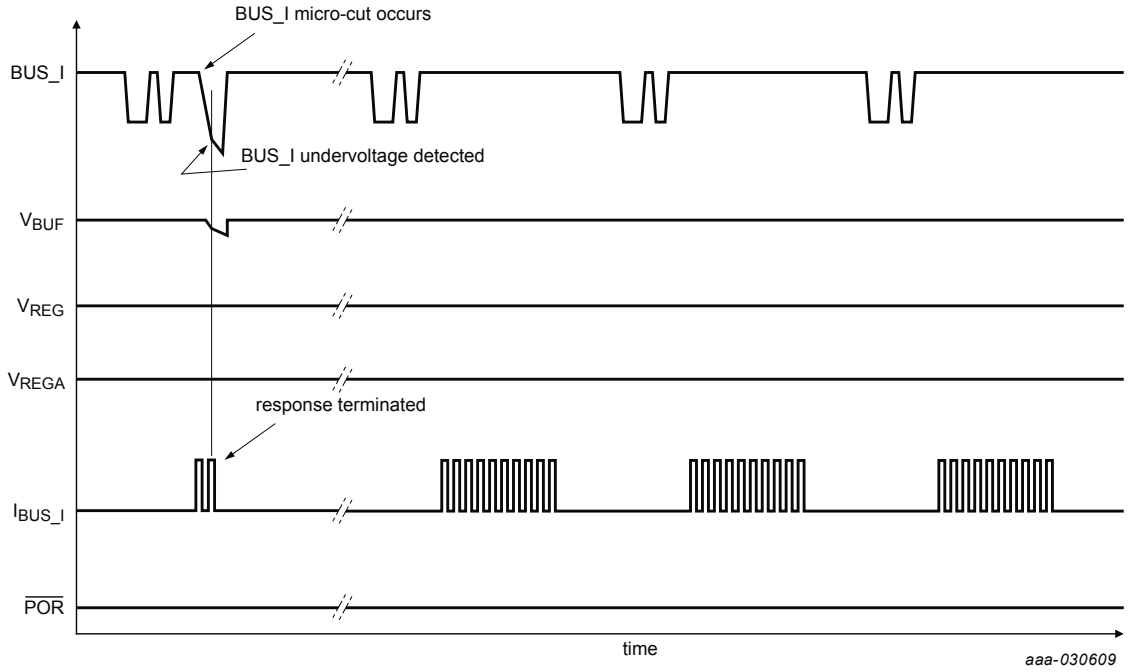

### 8.4.2 BUS_I, $V_{BUF}$, $V_{REG}$, $V_{REGA}$, undervoltage monitor

A circuit is incorporated to monitor the BUS_I supply voltage and the internally regulated voltages, $V_{BUF}$, $V_{REG}$, and $V_{REGA}$. If any of the voltages fall below the specified under-voltage thresholds in Section 7.4: Electrical characteristics - supply and I/O, the device reacts as described:

- DSI3
  - If any supply falls below the specified threshold during a command transmission in Command and Response Mode, the command is ignored, and no DSI3 response transmission occurs. Once the supply returns above the threshold, the device will resume decoding commands as specified in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).
  - If any supply falls below the specified threshold during a response transmission in Command and Response Mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume decoding commands as specified in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).
  - If any supply falls below the specified threshold during a command transmission in Periodic Data Collection Mode, the command is ignored and no periodic response occurs during that period. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands as specified in Section 8.2.2.5: Supply error flag (SUPPLY_ERR). Any partially received Background Diagnostic Mode command is flushed and the device will begin decoding a new Background Diagnostic Mode command.
  - If any supply falls below the specified threshold during a periodic response transmission in Periodic Data Collection Mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands as specified in Section 8.2.2.5: Supply error flag (SUPPLY_ERR). Any partially received Background Diagnostic Mode command is flushed and the device will begin decoding a new Background Diagnostic Mode command.
  - If any supply falls below the specified threshold during a Background Diagnostic Mode response transmission in Periodic Data Collection Mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands as specified in Section 8.2.2.5: Supply error flag (SUPPLY_ERR). Any partially received Background Diagnostic Mode command is flushed and the device will begin decoding a new Background Diagnostic Mode command.
- PSI5
  - If any supply falls below the specified threshold, all PSI5 transmissions are terminated for the present sync pulse or asynchronous transmission cycle. Once the supply returns above the threshold, the device will resume responses as specified in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).
- SPI
  - If any supply falls below the specified threshold, SPI responses are terminated. Once the supply returns above the threshold, the device will resume command decode and response transmissions as specified in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).
- I²C
  - If any supply falls below the specified threshold, I²C transactions are terminated. Once the supply returns above the threshold, the device will resume responses as specified in Section 8.2.2.5: Supply error flag (SUPPLY_ERR).

See Figure 15. BUS_I micro-cut response (DSI3 or PSI5) for an example of a supply line interruption during a DSI3 or PSI5 response.

Figure 15. **BUS_I micro-cut response (DSI3 or PSI5)**




## 8.5 Internal oscillator

The device includes a factory trimmed oscillator as specified in Section 7.21: Dynamic electrical characteristics - supply and support circuitry.

### 8.5.1 Oscillator training

The device includes a feature to train the oscillator to a tighter accuracy than the factory trimmed capability assuming the system master has a tighter oscillator accuracy than the slave factory trimmed capability. This feature can be enabled for all modes: DSI3, PSI5, SPI, and I²C.

*Note: Do not use oscillator training in systems that employ spread spectrum communication methods to reduce emissions.*

#### *8.5.1.1 DSI3 oscillator training*

Oscillator training is enabled if the CK_CAL_EN bit is set in the TIMING_CFG register and is accomplished by verifying the timing of periodic transmissions from the master against the values stored in the CRM_PER[1:0] and PDCM_PER[2:0] bits of the user read/write register array. The master programs the intended Periodic Data Collection Mode command period into the PDCM_PER[2:0] bits and the intended Command and Response Mode command period into the CRM_PER[1:0] bits. The device then calculates the number of transmission periods for every 4 ms ($n_{CRM\_PER\_4ms\_TYP}$ and $n_{PDCM\_PER\_4ms\_TYP}$).

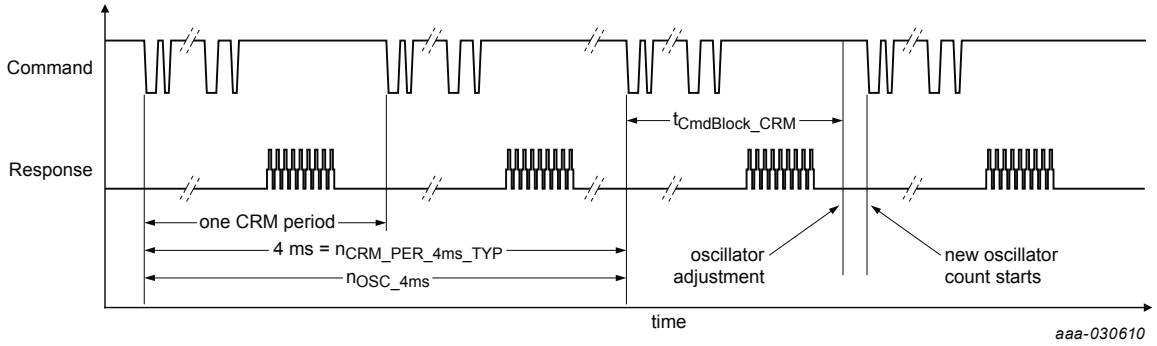
In Command and Response Mode, oscillator training is completed over 4 ms periods if and only if the CK_CAL_EN bit is set and the Command and Response Mode period is between 500 µs and 4 ms, inclusive. The following procedure is used to train the oscillator (See Figure 16. Command and response mode oscillator training timing diagram):

1. The device counts the number of oscillator cycles in $n_{CRM\_PER\_4ms\_TYP}$ periods ($n_{OSC\_4ms}$).

2. $n_{OSC\_4ms}$ is compared to $n_{OSC\_4ms\_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 7.21: Dynamic electrical characteristics - supply and support circuitry, an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If $n_{OSC\_4ms}$ is greater than $n_{OSC\_4ms\_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
   b. If $n_{OSC\_4ms}$ is less than $n_{OSC\_4ms\_TYP}$ - $OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed at the end of the command blocking time for the command ending the $n_{CRM\_PER\_OSC}$ calculation.

If the CK_CAL_EN bit is cleared after oscillator training has already been initiated, the state of the oscillator is determined by the state of the CK_CAL_RST bit in the TIMING_CFG register. If the CK_CAL_RST bit is cleared, the last adjustment value for the oscillator is maintained. If the CK_CAL_RST bit is set, the oscillator is reset to its untrained value with the untrained tolerance specified in Section 7.21: Dynamic electrical characteristics - supply and support circuitry.

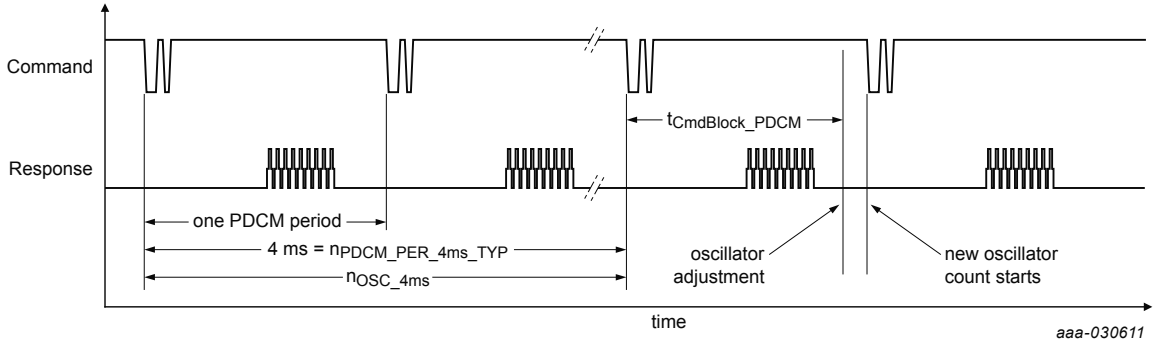
**Figure 16. Command and response mode oscillator training timing diagram**




In Periodic Data Collection Mode, oscillator training is completed over 4 ms periods if the CK_CAL_EN bit is set. The following procedure is used to train the oscillator (See Figure 17. Periodic data collection mode oscillator training timing diagram):

1. The device counts the number of oscillator cycles in $n_{PDCM\_PER\_4ms\_TYP}$ periods ($n_{OSC\_4ms}$).
2. $n_{OSC\_4ms}$ is compared to $n_{OSC\_4ms\_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 7.21: Dynamic electrical characteristics - supply and support circuitry, an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If $n_{OSC\_4ms}$ is greater than $n_{OSC\_4ms\_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
   b. If $n_{OSC\_4ms}$ is less than $n_{OSC\_4ms\_TYP}$ - $OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed at the end of the command blocking time for the command ending the $n_{PDCM\_PER\_OSC}$ calculation.

**Figure 17. Periodic data collection mode oscillator training timing diagram**



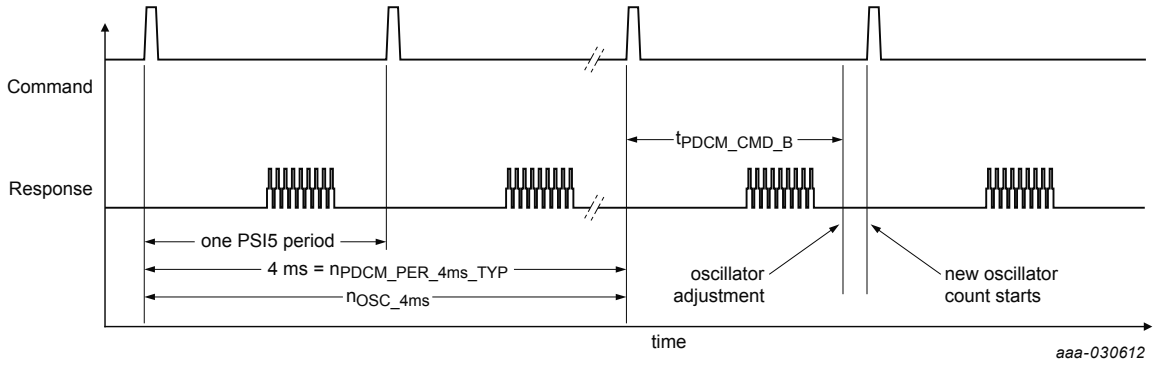
#### 8.5.1.2 PSI5 oscillator training

Oscillator training is enabled if the CK_CAL_EN bit is set in the TIMING_CFG register and is accomplished by verifying the timing of periodic transmissions from the master against the values stored in the PDCM_PER[2:0] bits of the user read/write register array. The sync pulse period is pre-programmed into the PDCM_PER[2:0] bits. The device then calculates the number of transmission periods for every 4 ms ($n_{PSI5\_PER\_4ms\_TYP}$).

Oscillator training is completed over 4 ms periods if the CK_CAL_EN bit is set. The following procedure is used to train the oscillator (see Figure 18. PSI5 oscillator training timing diagram):

1. The device counts the number of oscillator cycles in $n_{PSI5\_PER\_4ms\_TYP}$ periods ($n_{OSC\_4ms}$).
2. $n_{OSC\_4ms}$ is compared to $n_{OSC\_4ms\_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 7.21: Dynamic electrical characteristics - supply and support circuitry, an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If $n_{OSC\_4ms}$ is greater than $n_{OSC\_4ms\_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
   b. If $n_{OSC\_4ms}$ is less than $n_{OSC\_4ms\_TYP}$ - $OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed at the end of the command blocking time for the command ending the $n_{PDCM\_PER\_OSC}$ calculation.

**Figure 18. PSI5 oscillator training timing diagram**




Notes:

- In order to benefit from the PSI5 oscillator training accuracy improvements, the oscillator must be trained prior to data transmissions in Initialization phase 2. For this reason, if oscillator training is enabled in PSI5 mode, the device will not respond to sync pulses during initialization phase 1, but oscillator training will be enabled $t_{RS\_PM}$ after reset.

#### 8.5.1.3 SPI oscillator training

Oscillator training is enabled if the CK_CAL_EN bit is set in the TIMING_CFG register and is accomplished by verifying the timing of periodic SOURCEID_0 sensor data request SPI commands from the master against the value stored in the PDC-M_PER[2:0] bits of the user read/write register array. The master programs the intended command period into the PDC-M_PER[2:0] bits. The device then calculates the number of transmission periods for every 4 ms ($n_{SPI\_PER\_4ms\_TYP}$).

In SPI Mode, oscillator training is completed over 4 ms periods if the CK_CAL_EN bit is set. The following procedure is used to train the oscillator:

1. The device counts the number of oscillator cycles in $n_{SPI\_PER\_4ms\_TYP}$ periods ($n_{OSC\_4ms}$).
2. $n_{OSC\_4ms}$ is compared to $n_{OSC\_4ms\_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 7.21: Dynamic electrical characteristics - supply and support circuitry, an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If $n_{OSC\_4ms}$ is greater than $n_{OSC\_4ms\_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
   b. If $n_{OSC\_4ms}$ is less than $n_{OSC\_4ms\_TYP}$ - $OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed.

#### 8.5.1.4 *I²C oscillator training*

Oscillator training is enabled if the CK_CAL_EN bit is set in the TIMING_CFG register and is accomplished by verifying the timing of periodic I²C reads of the SNSDATA0_L register from the master against the value stored in the PDCM_PER[2:0] bits of the user read/write register array. The master programs the intended command period into the PDCM_PER[2:0] bits. The device then calculates the number of transmission periods for every 4 ms ($n_{SPI\_PER\_4ms\_TYP}$).

In I²C mode, oscillator training is completed over 4 ms periods if the CK_CAL_EN bit is set. The following procedure is used to train the oscillator:

1. The device counts the number of oscillator cycles in $n_{I2C\_PER\_4ms\_TYP}$ periods ($n_{OSC\_4ms}$).
2. $n_{OSC\_4ms}$ is compared to $n_{OSC\_4ms\_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 7.21: Dynamic electrical characteristics - supply and support circuitry, an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If $n_{OSC\_4ms}$ is greater than $n_{OSC\_4ms\_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
   b. If $n_{OSC\_4ms}$ is less than $n_{OSC\_4ms\_TYP}$ - $OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed.

### 8.5.2 Oscillator training error handling

If oscillator training is enabled by the user, but the conditions are not correct to complete oscillator training, the OSC-TRAIN_ERR bit is set in the DEVSTAT register. The following conditions will result in the OSCTRAIN_ERR bit being set.

- The CLK_CAL_EN bit in the TIMING_CFG register is set and the measured period ($n_{OSC\_4ms}$) for any mode is outside the Oscillator Training Window ($OscTrain_{WIN}$).
- The result of the comparison is filtered with an up and down counter.
- If $n_{OSC\_4ms}$ is outside the oscillator training window, the counter is incremented.
- If $n_{OSC\_4ms}$ is inside the oscillator training window, the counter is decremented.
- If the counter reaches the OSCTRAIN_ERRCNT setting in the TIMING_CFG2 register, the OSCTRAIN_ERR bit is set.
- The up and down counter has a maximum value of 127 and a minimum value of 0.
- The Command and Response Mode period established by the PDCM_PER and CRM_PER settings does not fall within the 500 µs to 4 ms window.
- The Command and Response Mode period established by the PDCM_PER and CRM_PER settings is not a whole number divisor of 4 ms.

## 8.6 Inertial sensor signal path

### 8.6.1 Inertial sensor transducer

The device transducer is an overdamped mass-spring-damper system defined by the following transfer function:

$$H(s) = \frac{\omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2} \quad (2)$$

Where:

$\zeta$ = Damping Ratio

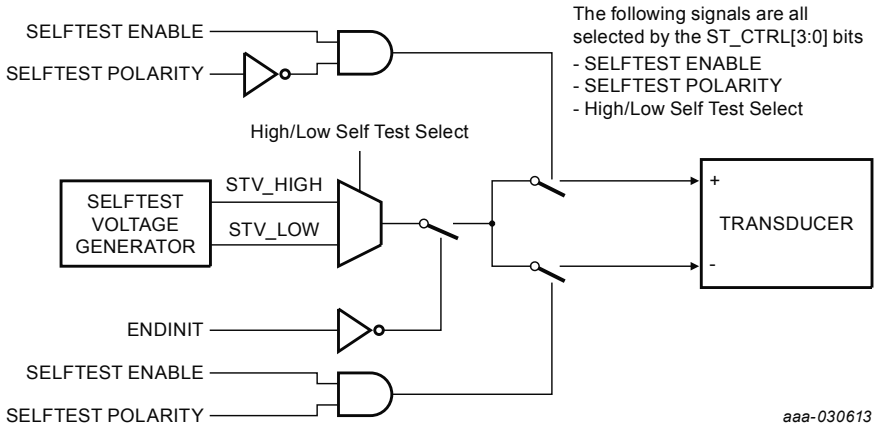
$\omega_n$ = Natural Frequency = $2 * \Pi * f_n$

See Section 7.20: Dynamic electrical characteristics - transducer for transducer parameters.

### 8.6.2 Inertial sensor self-test interface

The analog self-test interface applies a voltage to the g-cell, causing deflection of the proof mass. The resulting sensor data can be compared against the values stored in the Self-test Deflection Registers (See Section 8.2.37: Self-test deflection storage registers). The self-test interface is controlled through register write operations to the ST_CTRL[3:0] bits in the CHx_CFG_U5 register described in Section 8.2.27: Channel 0 and Channel 1 user configuration #5 register (CH0_CFG_U5, CH1_CFG_U5). A diagram of the self-test interface is shown in Figure 19. Self-test interface.

**Figure 19. Self-test interface**




Two self-test voltages are available for each device range. The self-test voltage is selected via the ST_CTRL[3:0] bits.

Self-test can be verified via the following methods:

#### *8.6.2.1 Raw self-test deflection verification*

In DSI3 mode, SPI mode or I²C mode, the raw self-test deflection can be verified against raw self-test limits in Section 7.7: Electrical characteristics - inertial sensor signal chain: Medium g.

#### *8.6.2.2 Delta self-test deflection verification*

In DSI3 mode, SPI mode or I²C mode, the raw self-test deflection can be verified against the nominal temperature self-test deflection value recorded at the time the device was produced. The production self-test deflection is stored in the CHx-_STy_z register as defined in Section 8.2.37: Self-test deflection storage registers. The Delta Self-test Deflection limits can then be determined by Eq. (3) and Eq. (4):

$$\Delta ST_{ACCMINLIMIT} = STDATA \times (1 - \Delta ST_{ACC}) \quad (3)$$

*Note: This value is truncated.*

$$\Delta ST_{ACCMAXLIMIT} = STDATA \times (1 + \Delta ST_{ACC}) \quad (4)$$

*Note: This value is rounded up.*

Where:

$\Delta ST_{ACC}$ = The accuracy of the self-test deflection relative to the stored deflection as specified in Section 7.9: Electrical characteristics - inertial sensor self-test.

STDATA = The value stored in the appropriate CHx_STy_z register as defined in Section 8.2.37: Self-test deflection storage registers.

#### 8.6.2.3 *Startup digital self-test*

In DSI3 mode, SPI mode or I²C mode, during device initialization (ENDINIT not set), the user can activate a digital self-test by writing to the ST_CTRL[3:0] bits in the CHx_CFG_U5 register. The digital self-test inputs a known signal stream into the front end of the DSP. After a delay defined by the low-pass filter selected, the output sensor data reaches a fixed value which can be verified by the user. The digital self-test values are listed in Section 8.2.27.1: Self-test control bits (ST_CTRL[3:0]).

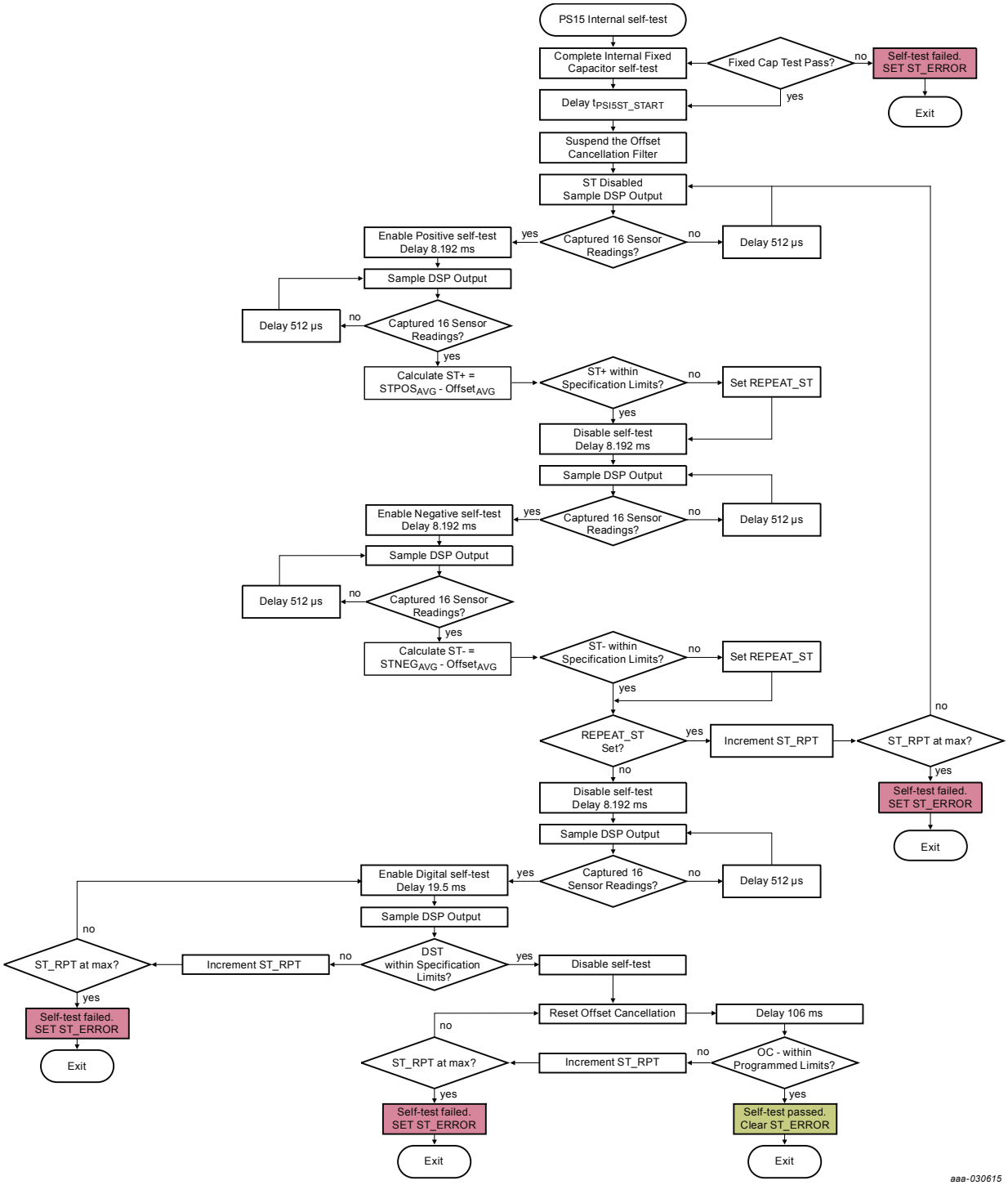
#### 8.6.2.4 *Fixed pattern self-test*

In DSI3 mode, SPI mode or I²C mode, during device initialization (ENDINIT not set), the user can activate a fixed pattern self-test by writing to the ST_CTRL[3:0] bits in the CHx_CFG_U5 register. Fixed pattern self-tests force the DSP output to a set of known values, enabling the user to verify each bit of the sensor data. The fixed pattern self-test values are listed in Section 8.2.27.1: Self-test control bits (ST_CTRL[3:0]).

#### 8.6.2.5 *PSI5 automatic startup self-test procedure*

Figure 20. PSI5 self-test procedure shows the PSI5 self-test procedure which is run automatically at startup on each channel if the device is a PSI5 device. The minimum gain settings are used for this procedure: U_SNS_SHIFT = '00', U_SNS_MULT = 0x00.

Figure 20. **PSI5 self-test procedure**

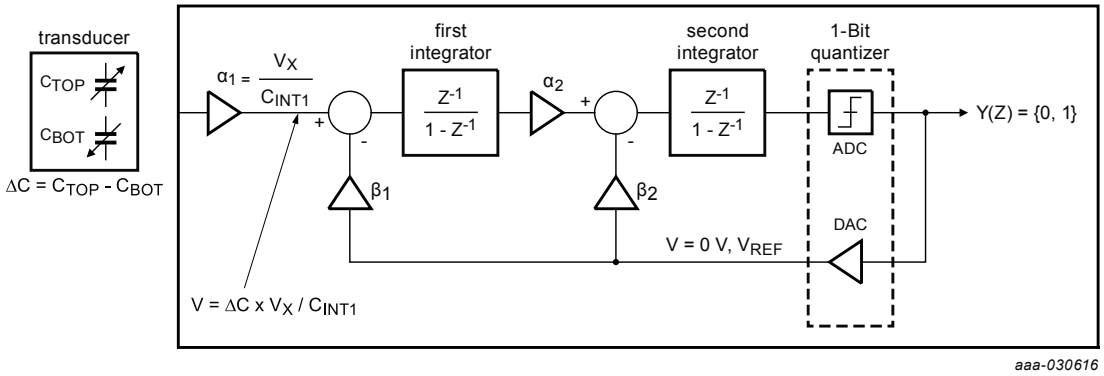



If the ST_ERROR flag in the CHx_STAT register is set once this test is complete, the device will exit PSI5 initialization phase 2 with a self-test error and the self-test error message are transmitted instead of sensor data. In this case, the ST_ER-ROR bit can only be cleared by a device reset.

### 8.6.3 Inertial sensor ΣΔ converter

A second order sigma delta modulator converts the differential capacitance of the transducer to a data stream that is input to the DSP. The sigma delta modulator operates at a frequency of 1 MHz. A simplified block diagram is shown in Figure 6. I²C application diagram.

Figure 21. **ΣΔ converter block diagram**




## 8.6.4 Inertial sensor digital signal processor

A digital signal processor (DSP) is used to perform signal filtering and compensation. A diagram illustrating the signal processing flow within the DSP is shown in Figure 22. Signal chain diagram.

Figure 22. **Signal chain diagram**

| selectable output types | data type 0 | data type 1 |
|---|---|---|
| - F with interpolation | yes (01) | no |
| - F without interpolation | no | yes (100) |
| - M with interpolation | no | no |
| - M without interpolation | yes (01) | yes (001) |
| - F - K with interpolation | yes (00) | no |
| - F - K without interpolation | no | yes (000) |
| - M - K with interpolation | no | no |
| - M - K without interpolation | yes (01) | yes (000) |
| - F - L with interpolation | yes (01) | no |
| - F - L without interpolation | no | yes (100) |
| - M - L with interpolation | no | no |
| - M - L without interpolation | yes (01) | yes (000) |

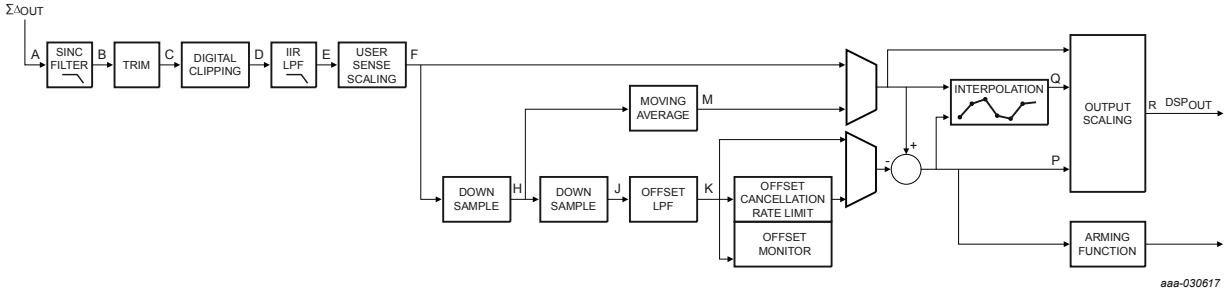



Table 203. **Signal chain diagram legend**

| | Description | Sample Time (µs) | Data width (Bits) | Sign (Bits) | Over range (Bits) | Signal width (Bits) | Signal margin (Bits) | Typical block latency | Reference |
|---|---|---|---|---|---|---|---|---|---|
| A | ΣΔ | 1 | 1 | 1 | NA | 1 | NA | 2.5 µs | Section 8.6.3: Inertial sensor ΣΔ converter |
| B | SINC Filter | 16, 32, 64 | 23 | 1 | NA | 21 | NA | 22.5 µs | Section 8.6.4.1: Decimation sinc filter |
| C | Trim | 16, 32, 64 | 32 | 1 | 2 | 18 | 11 | N/A | Section 8.6.4.2: Signal trim and compensation |
| D | Digital Clipping | 16, 32, 64 | 32 | 1 | 2 | 18 | 11 | N/A | Section 8.6.4.3: Digital clipping |
| E | Low-pass filter | 16, 32, 64 | 32 | 1 | 2 | 18 | 11 | Filter Dependent | Section 8.6.4.4: Low-pass filter |

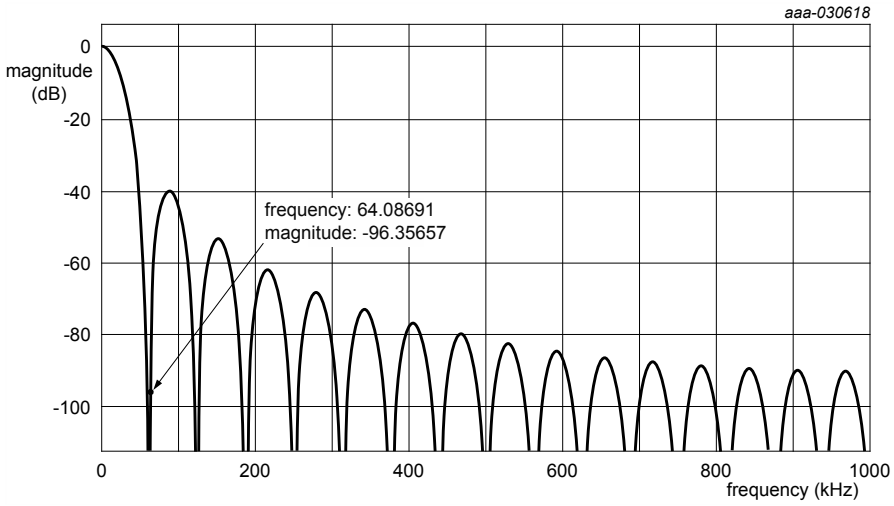
| | Description | Sample Time (µs) | Data width (Bits) | Sign (Bits) | Over range (Bits) | Signal width (Bits) | Signal margin (Bits) | Typical block latency | Reference |
|---|---|---|---|---|---|---|---|---|---|
| F | User Scaling | 16, 32, 64 | 32 | 1 | 2 | 18 | 11 | N/A | Section 8.6.4.5: User sensitivity scaling |
| H | Down Sample | 32, 64, 128 | 32 | 1 | NA | 31 | NA | N/A | Section 8.6.4.7: Moving average |
| J | Secondary Down Sample | 256 | 32 | 1 | NA | 31 | NA | N/A | Section 8.6.4.6: Offset cancellation |
| K | Offset low-pass filter | 256 | 32 | 1 | 2 | 18 | 11 | N/A | Section 8.6.4.6: Offset cancellation |
| L | Offset Rate Limiting | 256 | 16 | 1 | 2 | 11 | 2 | N/A | Section 8.6.4.6: Offset cancellation |
| M | Moving Average Filter | 32, 64, 128 | 24 | 1 | 2 | 18 | 3 | Filter Dependent | Section 8.6.4.7: Moving average |
| P | Offset Subtraction | 32, 64, 128 | 24 | 1 | 2 | 18 | 3 | N/A | Section 8.6.4.6: Offset cancellation |
| Q | Interpolation | 1, 2, 4 | 24 | 1 | 2 | 18 | 3 | $t_{SigChainXX}$ | Section 8.6.4.8: Data interpolation |
| R | Output Range Selection | 1, 2, 4 | 18 | User Selectable | | | | N/A | Section 8.6.4.9: Output scaling |

### 8.6.4.1 *Decimation sinc filter*

The output of the ΣΔ modulator is decimated and converted to a parallel value by a third order Sinc Filter with a decimation ratio of 16.

$$H(Z) = \left(\frac{1}{16^3}\right) \times \left(\frac{1 - Z^{-16}}{1 - Z^{-1}}\right)^3 \quad (5)$$

**Figure 23. Sinc filter response 3rd order sinc filter magnitude response**




### 8.6.4.2 *Signal trim and compensation*

The device includes digital trim to compensate for sensor offset, sensitivity, and non-linearity over temperature. Eq. (6), Eq. (7), Eq. (8), and Eq. (9) are used for the trim compensation.

$$Offset_{Trim} = A_0 + B_2 \times (T - T_{25}) + C_{22} \times (T - T_{25})^2 \quad (6)$$

$$Sensitivity_{Trim} = B_1 + (T - T_{25}) \times C_{12} \quad (7)$$

$$Linearity_{Trim} = C_{11} \quad (8)$$

$$Trim_{OUT} = Trim_{In} \times [Sensitivity_{Trim} + Trim_{In} \times Linearity_{Trim}] + Offset_{Trim} \quad (9)$$

**Table 204. Signal trim and compensation variable descriptions**

| Variable name | Description | Range (Real) | Variable size (Bits) | Resolution (Real) |
|---|---|---|---|---|
| $A_0$ | Offset Compensation | –1.0 to +1.0 | 12 | 4.8852e–04 |
| $B_2$ | Offset Compensation with First Order Temperature Compensation | –1.0 to +1.0 | 12 | 4.8852e–04 |
| $C_{22}$ | Offset Compensation with Second Order Temperature Compensation | –1.0 to +1.0 | 12 | 4.8852e–04 |
| $B_1$ | Sensitivity Compensation | –1.0 to +1.0 | 12 | 4.8852e–04 |
| $C_{12}$ | Sensitivity Compensation with First Order Temperature Compensation | –1.0 to +1.0 | 12 | 4.8852e–04 |
| $C_{11}$ | Linearity Compensation | –1.0 to +1.0 | 12 | 4.8852e–04 |
| $T$ | Temperature Sensor Digital Output Value | –1.0 to +1.0 | 12 | 4.8852e–04 |
| $T_{25}$ | Temperature Sensor Output Value stored at the Ambient Test Insertion | –1.0 to +1.0 | 12 | 4.8852e–04 |
| $Trim_{In}$ | Output of the Sinc Filter | | | |
| $Trim_{Out}$ | Output of the Trim Block | | | |

#### 8.6.4.3 *Digital clipping*

The device includes a digital clipping block to maximize the symmetry between the positive and negative electrical dynamic range of the device. Digital clipping values are specified in Section 7.10: Electrical characteristics - lateral inertial sensor overload and Section 7.11: Electrical characteristics - Z-axis inertial sensor overload.

#### 8.6.4.4 *Low-pass filter*

Data from the Sinc filter is processed by an infinite impulse response (IIR) low-pass filter.

$$H(z) = a_0 \cdot \frac{\left(n_{11} \cdot z^0\right) + \left(n_{12} \cdot z^{-1}\right) + \left(n_{13} \cdot z^{-2}\right)}{\left(d_{11} \cdot z^0\right) + \left(d_{12} \cdot z^{-1}\right) + \left(d_{13} \cdot z^{-2}\right)} \cdot \frac{\left(n_{21} \cdot z^0\right) + \left(n_{22} \cdot z^{-1}\right) + \left(n_{23} \cdot z^{-2}\right)}{\left(d_{21} \cdot z^0\right) + \left(d_{22} \cdot z^{-1}\right) + \left(d_{23} \cdot z^{-2}\right)} \quad (10)$$

The device provides the option for one of several low-pass filters. The filter coefficients are selected with the LPF[3:0] bits in the CHx_CFG_U1 registers.

The filter selection options are listed in Section 8.2.23.1: Low-pass filter and sample rate selection bits (LPF[3:0], SAMPLERATE[1:0]). Response parameters for the low-pass filter are specified in Section 7.19: Dynamic electrical characteristics - digital self-test response time. Filter characteristics for the highest sample rate are illustrated in Figure 24. 400 Hz, 4-pole low-pass filter response magnitude through Figure 49. 50 Hz, 4-pole low-pass filter response signal delay.

### Table 205. LPF #0 and LPF #2

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0, 2 | 0000 or 0010 | 00 or 01 | 400 | 16 | 4 | 839 | –19.5 | 1.59 | $a_0$ | 0.003143225986084408 | | |
| | | | | | | | | | $n_{11}$ | 0.0009951105668343345 | $d_{11}$ | 1 |
| | | 10 | 200 | 32 | | 1678 | –42.3 | 3.18 | $n_{12}$ | 0.00200348780064749 | $d_{12}$ | –1.892328151433503 |
| | | | | | | | | | $n_{13}$ | 0.001008466113720278 | $d_{13}$ | 0.8954713774195870 |
| | | | | | | | | | $n_{21}$ | 0.2516720624825626 | $d_{21}$ | 1 |
| | | 11 | 100 | 64 | | 3356 | –66.0 | 6.36 | $n_{22}$ | 0.4999888752940916 | $d_{22}$ | –1.918978239761011 |
| | | | | | | | | | $n_{23}$ | 0.2483390622233452 | $d_{23}$ | 0.9229853042218408 |

### Table 206. LPF #1 and LPF #3

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1, 3 | 0001 or 0011 | 00 or 01 | 400 | 16 | 3 | 697 | –16.6 | 1.49 | $a_0$ | 0.05189235225042199 | | |
| | | | | | | | | | $n_{11}$ | 0.001629077582099646 | $d_{11}$ | 1 |
| | | 10 | 200 | 32 | | 1394 | –33.5 | 2.98 | $n_{12}$ | 0.001630351547919014 | $d_{12}$ | –0.9481076477495780 |
| | | | | | | | | | $n_{13}$ | 0 | $d_{13}$ | 0 |
| | | | | | | | | | $n_{21}$ | 0.2500977520825902 | $d_{21}$ | 1 |
| | | 11 | 100 | 64 | | 2788 | –51.5 | 5.96 | $n_{22}$ | 0.4999999235890745 | $d_{22}$ | –1.915847097557409 |
| | | | | | | | | | $n_{23}$ | 0.2499023243303036 | $d_{23}$ | 0.9191065266874253 |

### Table 207. LPF #4

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 | 0100 | 00 or 01 | 325 | 16 | 4 | 856 | –21.4 | 1.84 | $a_0$ | 0.0424754749983549118 | | |
| | | | | | | | | | $n_{11}$ | 0.0010903775691986084 | $d_{11}$ | 1 |
| | | 10 | 162.5 | 32 | | 1712 | –38.7 | 3.68 | $n_{12}$ | 0.00108939409255981445 | $d_{12}$ | –0.9575245380401613281 |
| | | | | | | | | | $n_{13}$ | 0 | $d_{13}$ | 0 |
| | | | | | | | | | $n_{21}$ | 0.24988752603530883789 | $d_{21}$ | 1 |
| | | 11 | 81.25 5 | 64 | | 3424 | –56.8 | 7.36 | $n_{22}$ | 0.49999895691871643 07 | $d_{22}$ | –1.9314087629318237 3047 |
| | | | | | | | | | $n_{23}$ | 0.2501125633716583252 | $d_{23}$ | 0.9335850479125976562 |

### Table 208. LPF #5

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5 | 0101 | 00 or 01 | 370 | 16 | 2 | 586 | –14.1 | 1.55 | $a_0$ | 0.0022098285844549536 7 | | |
| | | | | | | | | | $n_{11}$ | 0.25 | $d_{11}$ | 1 |
| | | 10 | 185 | 32 | | 1172 | –25.2 | 3.10 | $n_{12}$ | 0.49999985098838806 15 | $d_{12}$ | –1.9180315136909484 8633 |
| | | | | | | | | | $n_{13}$ | 0.25 | $d_{13}$ | 0.9202413558959960 9375 |
| | | | | | | | | | $n_{21}$ | 1 | $d_{21}$ | 1 |
| | | 11 | 92.5 | 64 | | 2344 | –37.2 | 6.20 | $n_{22}$ | 0 | $d_{22}$ | 0 |
| | | | | | | | | | $n_{23}$ | 0 | $d_{23}$ | 0 |

### Table 209. LPF #6

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6 | 0110 | 00 or 01 | 180 | 16 | 2 | 1187 | –25.6 | 3.19 | $a_0$ | 0.0005340692005120 2178 | | |
| | | | | | | | | | $n_{11}$ | 0.25 | $d_{11}$ | 1 |
| | | 10 | 90 | 32 | | 2374 | –37.5 | 6.38 | $n_{12}$ | 0.50 | $d_{12}$ | –1.95983958244323730469 |
| | | | | | | | | | $n_{13}$ | 0.25 | $d_{13}$ | 0.96037364006042480469 |
| | | | | | | | | | $n_{21}$ | 1 | $d_{21}$ | 1 |
| | | 11 | 45 | 64 | | 4748 | –49.7 | 12.8 | $n_{22}$ | 0 | $d_{22}$ | 0 |
| | | | | | | | | | $n_{23}$ | 0 | $d_{23}$ | 0 |

### Table 210. LPF #7

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 0111 | 00 or 01 | 100 | 16 | 2 | 2167 | –35.7 | 4<br>5.75 | $a_0$ | 0.0001663098373683 1695 | | |
| | | | | | | | | | $n_{11}$ | 0.25 | $d_{11}$ | 1 |
| | | 10 | 50 | 32 | | 4334 | –47.7 | 11.5 | $n_{12}$ | 0.5 | $d_{12}$ | –1.97762179374694824219 |
| | | | | | | | | | $n_{13}$ | 0.25 | $d_{13}$ | 0.97778090705871582 03 |
| | | | | | | | | | $n_{21}$ | 1 | $d_{21}$ | 1 |
| | | 11 | 25 | 64 | | 8668 | –60.0<br>5 | 23.0 | $n_{22}$ | 0 | $d_{22}$ | 0 |
| | | | | | | | | | $n_{23}$ | 0 | $d_{23}$ | 0 |

### Table 211. LPF #8

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 8 | 1000 | 00 or 01 | 1500 | 16 | 4 | 223 | –1.26 | 0.420 | $a_0$ | 0.0383433729561284 4088 | | |
| | | | | | | | | | $n_{11}$ | 0.012602858551678 35381 | $d_{11}$ | 1 |
| | | 10 | 750 | 32 | | 446 | –5.70 | 0.840 | $n_{12}$ | 0.025205812956353 51826 | $d_{12}$ | –1.62182206187479138748 |
| | | | | | | | | | $n_{13}$ | 0.012602841714538 99225 | $d_{13}$ | 0.66016543483091971734 |
| | | | | | | | | | $n_{21}$ | 0.250003918548375 7809 | $d_{21}$ | 1 |
| | | 11 | 375 | 64 | | 892 | –21.7 | 1.68 | $n_{22}$ | 0.499998882296568 74739 | $d_{22}$ | –1.69136566438039781524 |
| | | | | | | | | | $n_{23}$ | 0.250000725848651 73919 | $d_{23}$ | 0.74177717760299266558 |

### Table 212. LPF #9

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (HZ) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 9 | 1001 | 00 or 01 | 500 | 16 | 3 | 558 | –12.0 | 1.18 | $a_0$ | 0.0646157039288756 1187 | | |
| | | | | | | | | | $n_{11}$ | 0.0025322835860241 2005 | $d_{11}$ | 1 |
| | | 10 | 250 | 32 | | 1116 | –27.9 | 2.36 | $n_{12}$ | 0.0025338245574624 9506 | $d_{12}$ | –0.93538429607112438813 |
| | | | | | | | | | $n_{13}$ | 0.0 | $d_{13}$ | 0.0 |
| | | | | | | | | | $n_{21}$ | 0.250076066293792 14302 | $d_{21}$ | 1 |
| | | 11 | 125 | 64 | | 2232 | –45.8 | 4.72 | $n_{22}$ | 0.499999537256002 9905 | $d_{22}$ | –1.89461887839771225828 |
| | | | | | | | | | $n_{23}$ | 0.249923979977556 22097 | $d_{23}$ | 0.89968498654120099278 |

### Table 213. LPF #A

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | 1010 | 00 or 01 | 800 | 16 | 4 | 419 | –4.92 | 0.795 | $a_0$ | 0.0119041098420571422 9 | | |
| | | | | | | | | | $n_{11}$ | 0.0038415818652894405 2 | $d_{11}$ | 1 |
| | | 10 | 400 | 32 | | 838 | –19.5 | 1.59 | $n_{12}$ | 0.0076832541450712367 5 | $d_{12}$ | –1.7900046271928506946 8 |
| | | | | | | | | | $n_{13}$ | 0.0038415549853448461 4 | $d_{13}$ | 0.8019087370349079479 9 |
| | | | | | | | | | $n_{21}$ | 0.2500010336651343756 4 | $d_{21}$ | 1 |
| | | 11 | 200 | 64 | | 1676 | –42.3 | 3.18 | $n_{22}$ | 0.4999961833987475179 3 | $d_{22}$ | –1.8368494349175779056 8 |
| | | | | | | | | | $n_{23}$ | 0.2500027829312634342 1 | $d_{23}$ | 0.8522158259133094659 9 |

### Table 214. LPF #B

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B | 1011 | 00 or 01 | 1200 | 16 | 4 | 279 | –2.00 | 0.530 | $a_0$ | 0.0254619582709132465 1 | | |
| | | | | | | | | | $n_{11}$ | 0.0083076945867290117 5 | $d_{11}$ | 1 |
| | | 10 | 600 | 32 | | 558 | –9.30 | 1.06 | $n_{12}$ | 0.0166154934194557776 8 | $d_{12}$ | –1.6922607339438120455 1 |
| | | | | | | | | | $n_{13}$ | 0.0083076737378434614 7 | $d_{13}$ | 0.7177226922147252885 5 |
| | | | | | | | | | $n_{21}$ | 0.2500006274083957369 4 | $d_{21}$ | 1 |
| | | 11 | 300 | 64 | | 1116 | –28.8 | 2.12 | $n_{22}$ | 0.4999811778583796995 | $d_{22}$ | –1.7538506263979973809 3 |
| | | | | | | | | | $n_{23}$ | 0.2500012548031438353 0 | $d_{23}$ | 0.7870814881420525877 0 |

### Table 215. LPF #C

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C | 1100 or 1101 | 00 or 01 | 120 | 16 | 3 | 2325 | –46.5 | 5.00 | $a_0$ | 0.0158950014594796407 2 | | |
| | | | | | | | | | $n_{11}$ | 0.0001516198854450196 0 | $d_{11}$ | 1 |
| | | 10 | 60 | 32 | | 4650 | –64.5 | 10.0 | $n_{12}$ | 0.0001520095484536158 4 | $d_{12}$ | –0.98410499854052035928 |
| | | | | | | | | | $n_{13}$ | 0.0 | $d_{13}$ | 0.0 |
| | | | | | | | | | $n_{21}$ | 0.2503212499430660376 0 | $d_{21}$ | 1 |
| | | 11 | 30 | 64 | | 9300 | –82.8 | 20.0 | $n_{22}$ | 0.4999991755395360448 8 | $d_{22}$ | –1.9746404539263164856 8 |
| | | | | | | | | | $n_{23}$ | 0.2496795747014305955 1 | $d_{23}$ | 0.9749440833602062150 8 |

### Table 216. LPF #D

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (kHz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D | 1100 or 1101 | 00 or 01 | 20 | 16 | 2 | < 50 | 0 | < 0.100 | $a_0$ | 0.46228490769863128662 | | |
| | | | | | | | | | $n_{11}$ | 1.03297972679138183594 | $d_{11}$ | 1 |
| | | 10 | 10 | 32 | | < 100 | –0.01 | < 0.200 | $n_{12}$ | 2.06595945358276367188 | $d_{12}$ | 0.72391998767852783203 |
| | | | | | | | | | $n_{13}$ | 1.03297972679138183594 | $d_{13}$ | 0.18620371818542480469 |
| | | | | | | | | | $n_{21}$ | 1 | $d_{21}$ | 1 |
| | | 11 | 5 | 64 | | < 200 | –0.04 | < 0.400 | $n_{22}$ | 0 | $d_{22}$ | 0 |
| | | | | | | | | | $n_{23}$ | 0 | $d_{23}$ | 0 |

**Table 217. LPF #E**

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E | 1110 | 00 or 01 | 120 | 16 | 2 | 1804 | –32.8 | 4.85 | $a_0$ | 0.0002389528021065068 2 | | |
| | | | | | | | | | $n_{11}$ | 0.25 | $d_{11}$ | 1 |
| | | 10 | 60 | 32 | | 3608 | –44.7 | 9.70 | $n_{12}$ | 0.50 | $d_{12}$ | –1.9731662501396218 8007 |
| | | | | | | | | | $n_{13}$ | 0.25 | $d_{13}$ | 0.9734052029417282 7587 |
| | | | | | | | | | $n_{21}$ | 1 | $d_{21}$ | 1 |
| | | 11 | 30 | 64 | | 7216 | –57.0 | 19.4 | $n_{22}$ | 0 | $d_{22}$ | 0 |
| | | | | | | | | | $n_{23}$ | 0 | $d_{23}$ | 0 |

**Table 218. LPF #F**

| Filter # | LPF[3:0] | SAMPLERATE[1:0] | Typical –3 dB Frequency (Hz) | Sample time (µs) | Filter order | Group delay (µs) | 1000 Hz Attenuation (dB) | Step response Activation to 99 % (ms) | Filter coefficients | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F | 1111 | 00 or 01 | 50 | 16 | 4 | 6726 | –89.7 | 12.8 | $a_0$ | 0.0000513732266482 7693 | | |
| | | | | | | | | | $n_{11}$ | 0.0000150412414317 7110 | $d_{11}$ | 1 |
| | | 10 | 25 | 32 | | 13,452 | –114 | 25.6 | $n_{12}$ | 0.0000322611116208 7577 | $d_{12}$ | –1.9862631920569757 6820 |
| | | | | | | | | | $n_{13}$ | 0.0000173872064838 6979 | $d_{13}$ | 0.9863145652836241 5614 |
| | | | | | | | | | $n_{21}$ | 0.2688006391147707 5633 | $d_{21}$ | 1 |
| | | 11 | 12.5 | 64 | | 26,904 | –138 | 51.2 | $n_{22}$ | 0.4986318155607519 680 | $d_{22}$ | –1.9899756803576962 3052 |
| | | | | | | | | | $n_{23}$ | 0.2325358786649665 2770 | $d_{23}$ | 0.9900403698824448 1510 |

**Figure 24. 400 Hz, 4-pole low-pass filter response magnitude**

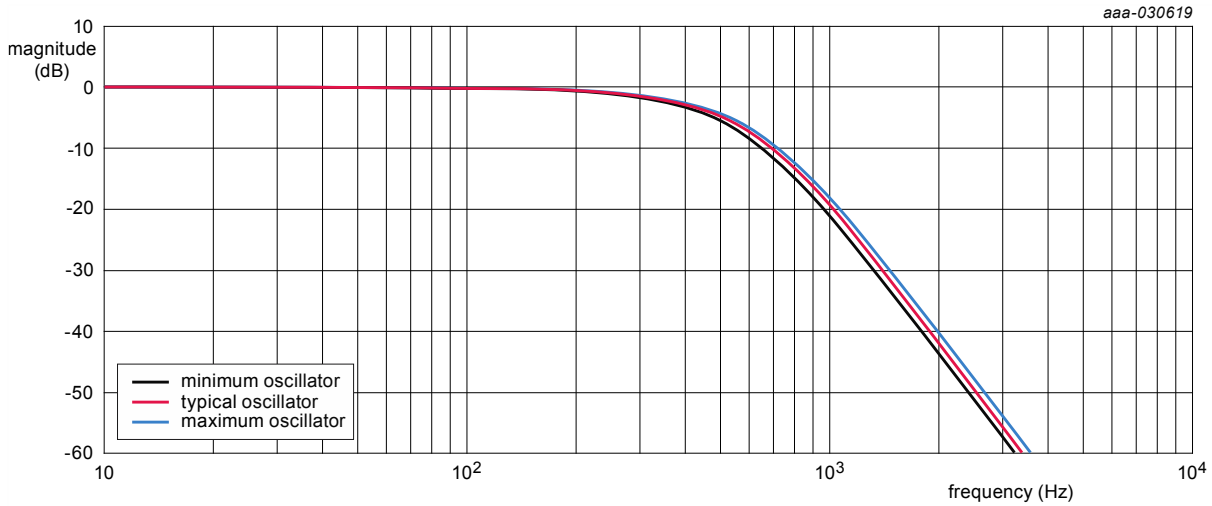


Figure 25. **400 Hz, 4-pole low-pass filter response signal delay**

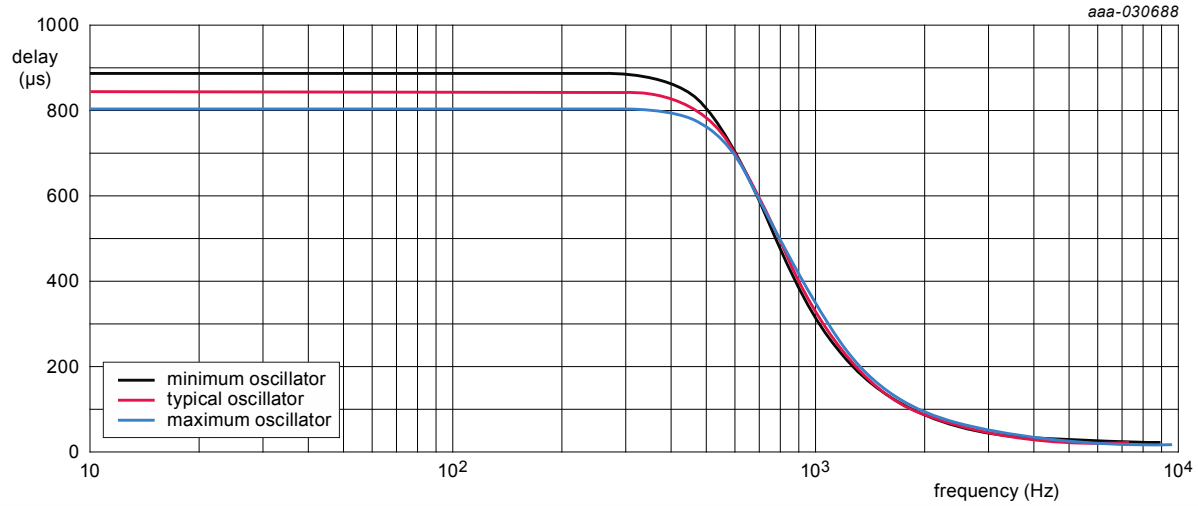



Figure 26. **400 Hz, 3-pole low-pass filter response magnitude**

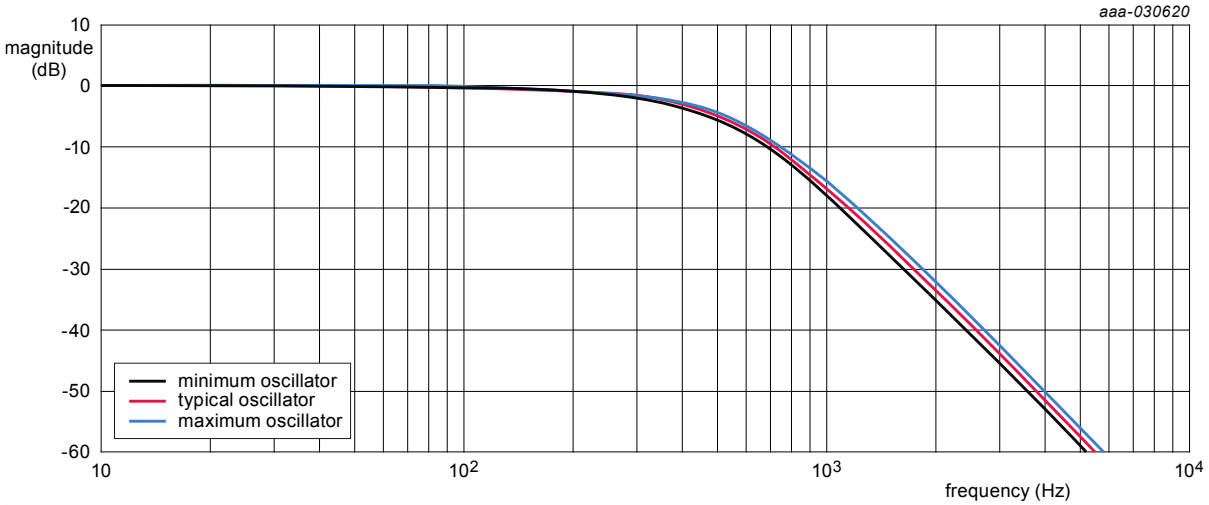



Figure 27. **400 Hz, 3-pole low-pass filter response signal delay**

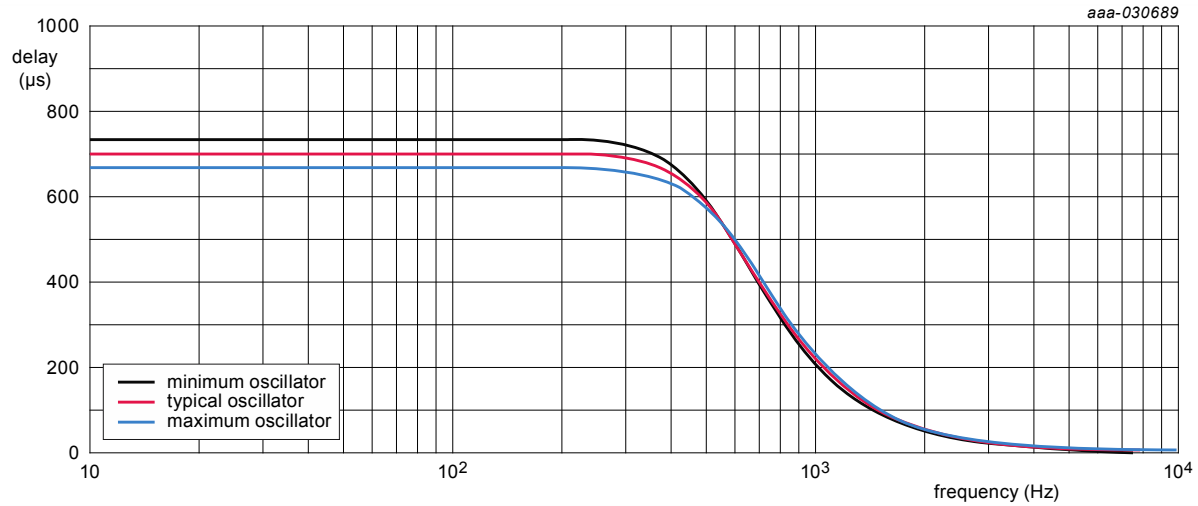


Figure 28. **325 Hz, 3-pole low-pass filter response magnitude**

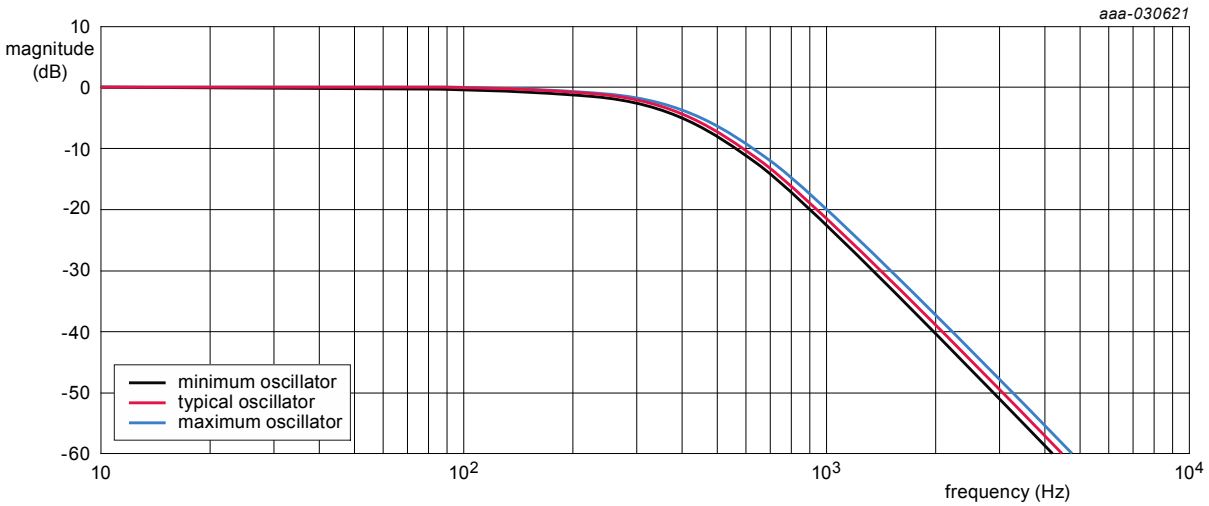



Figure 29. **325 Hz, 3-pole low-pass filter response signal delay**

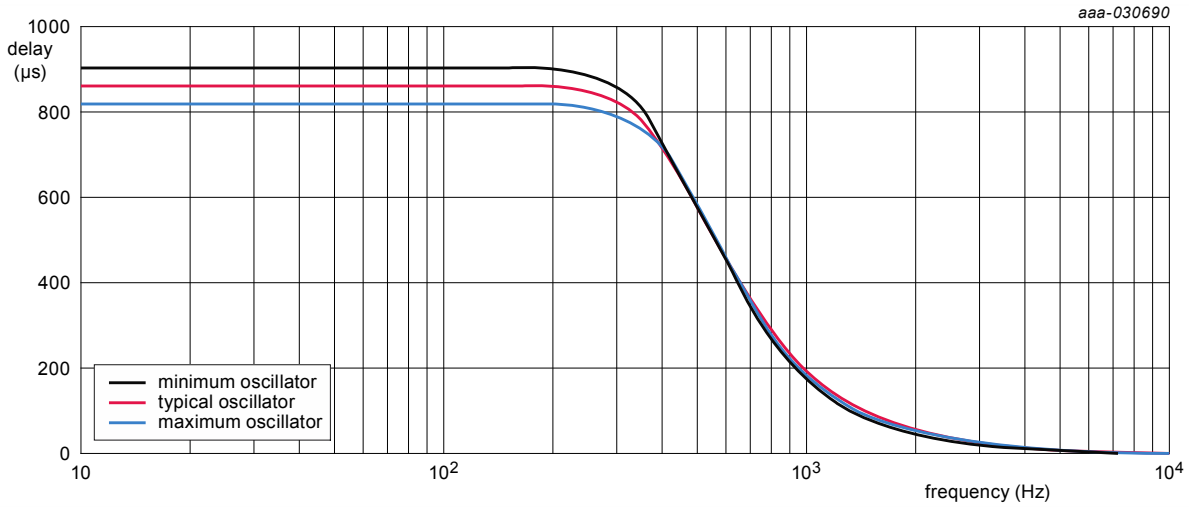


Figure 30. 370 Hz, 2-pole low-pass filter response magnitude

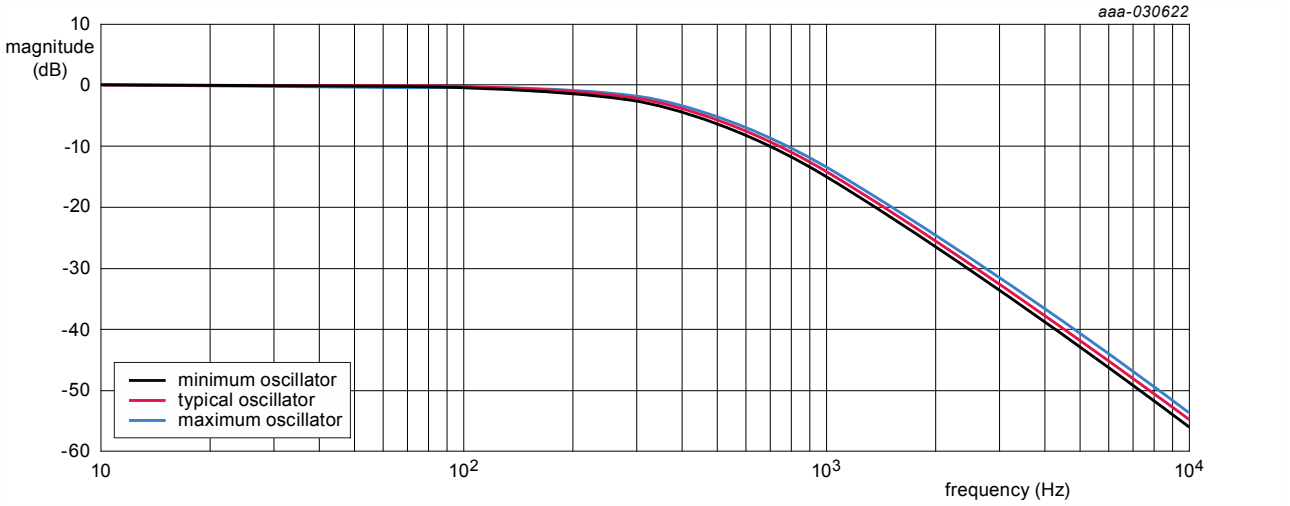



Figure 31. 370 Hz, 2-pole low-pass filter response signal delay

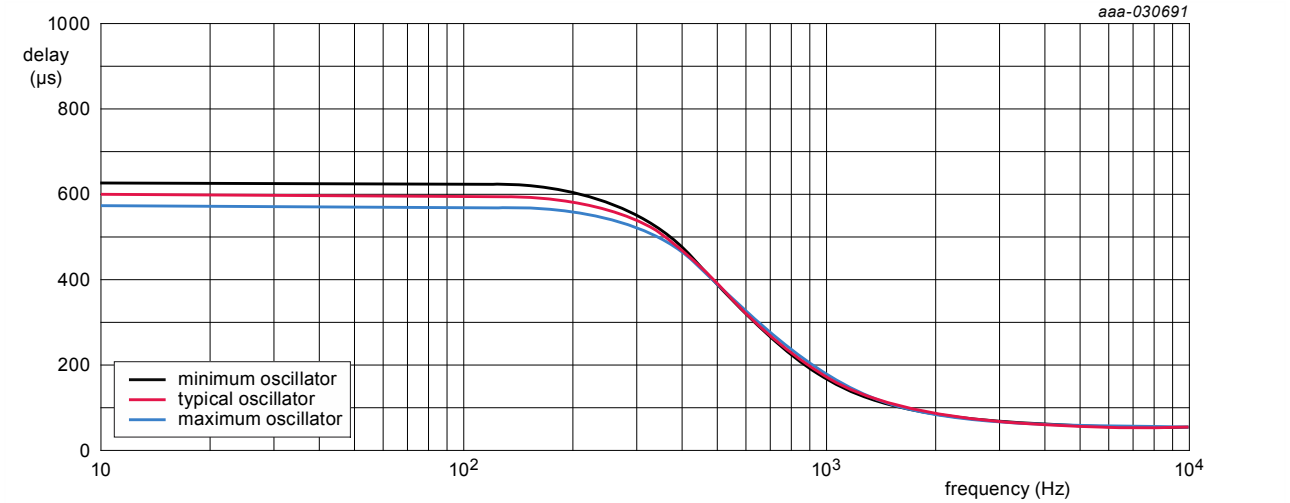


Figure 32. 180 Hz, 2-pole low-pass filter response magnitude

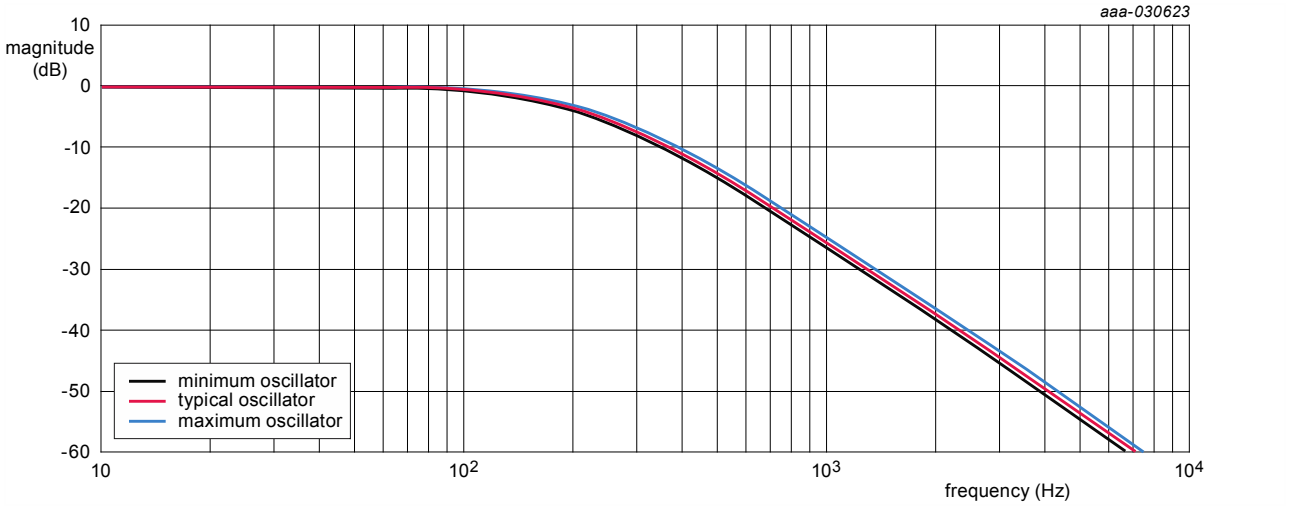



Figure 33. 180 Hz, 2-pole low-pass filter response signal delay

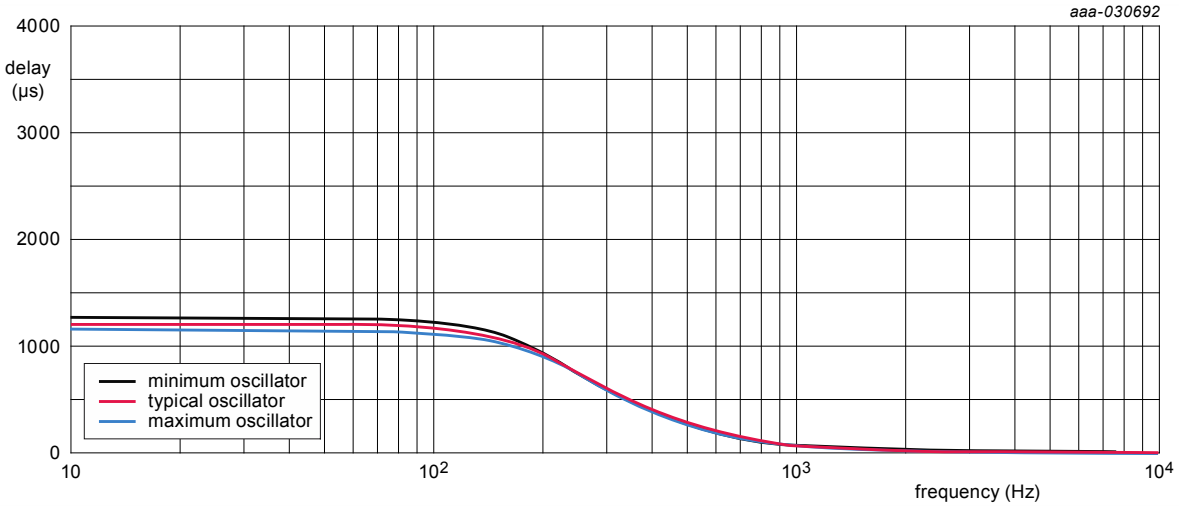


Figure 34. **100 Hz, 2-pole low-pass filter response magnitude**

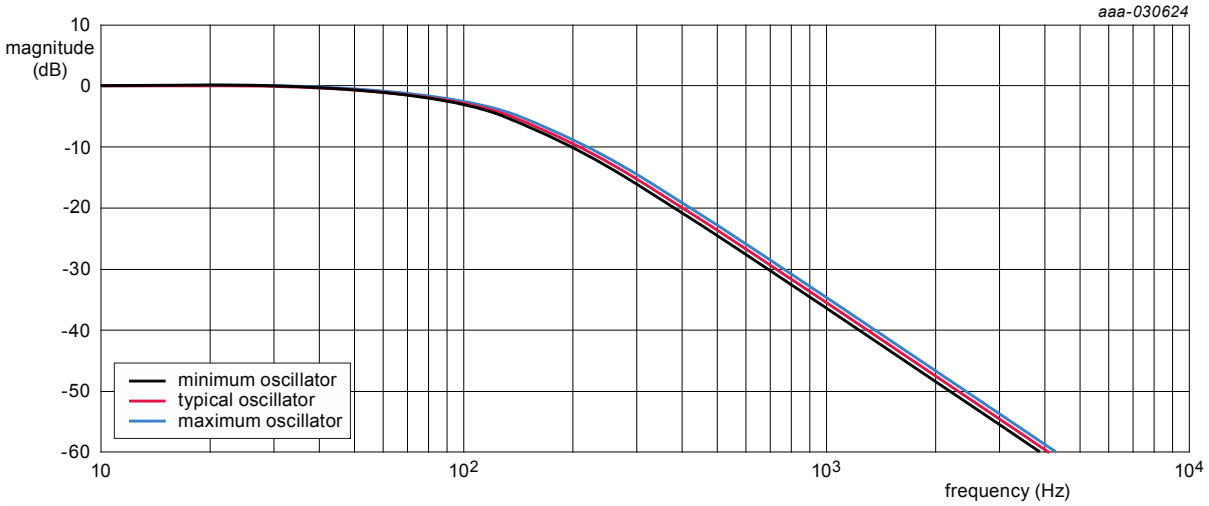



Figure 35. **100 Hz, 2-pole low-pass filter response signal delay**

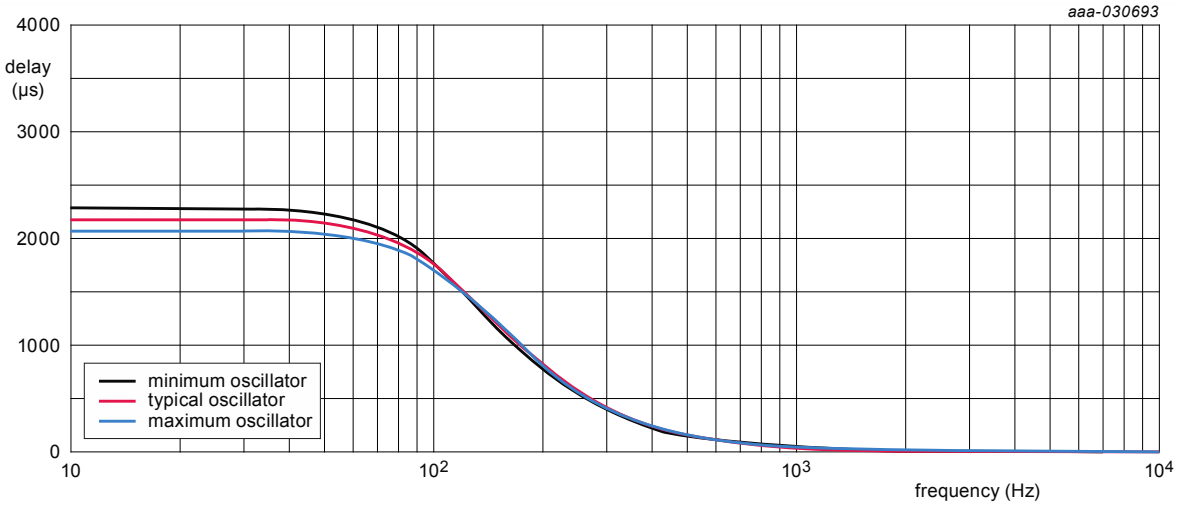


Figure 36. **1500 Hz, 4-pole low-pass filter response magnitude**

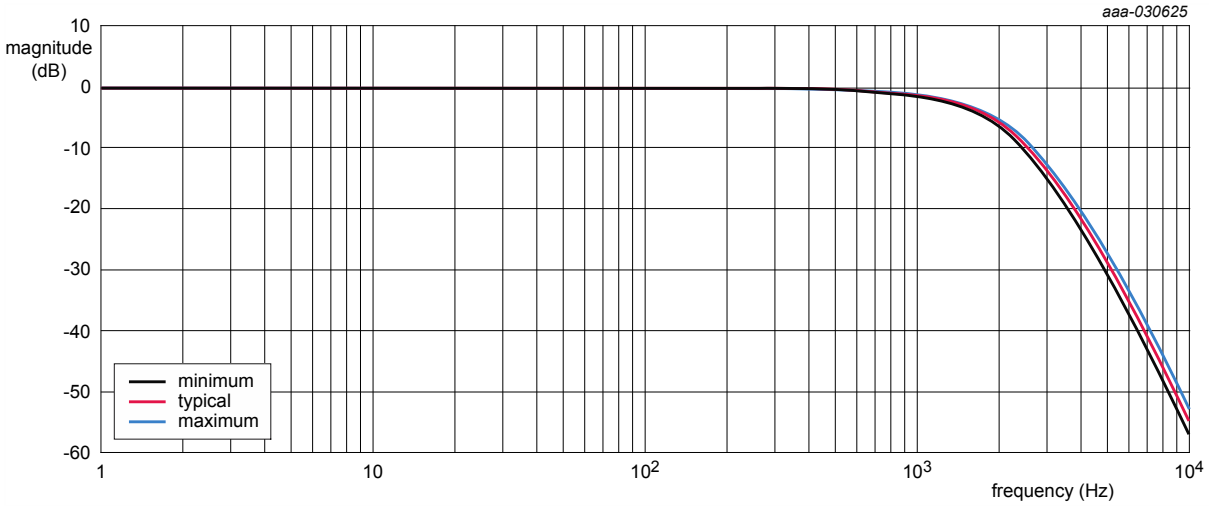



Figure 37. **1500 Hz, 4-pole low-pass filter response signal delay**

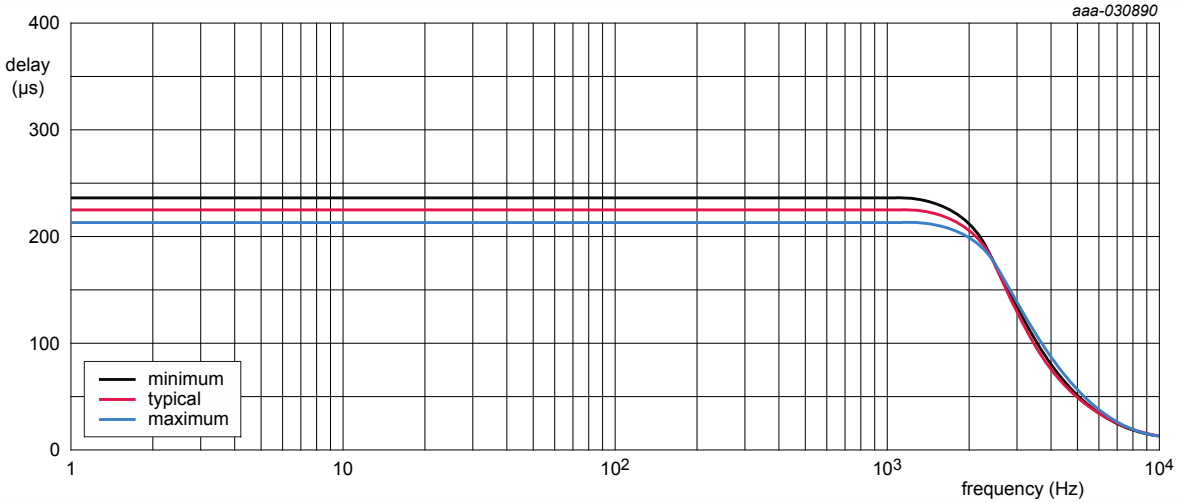


Figure 38. **500 Hz, 3-pole low-pass filter response magnitude**

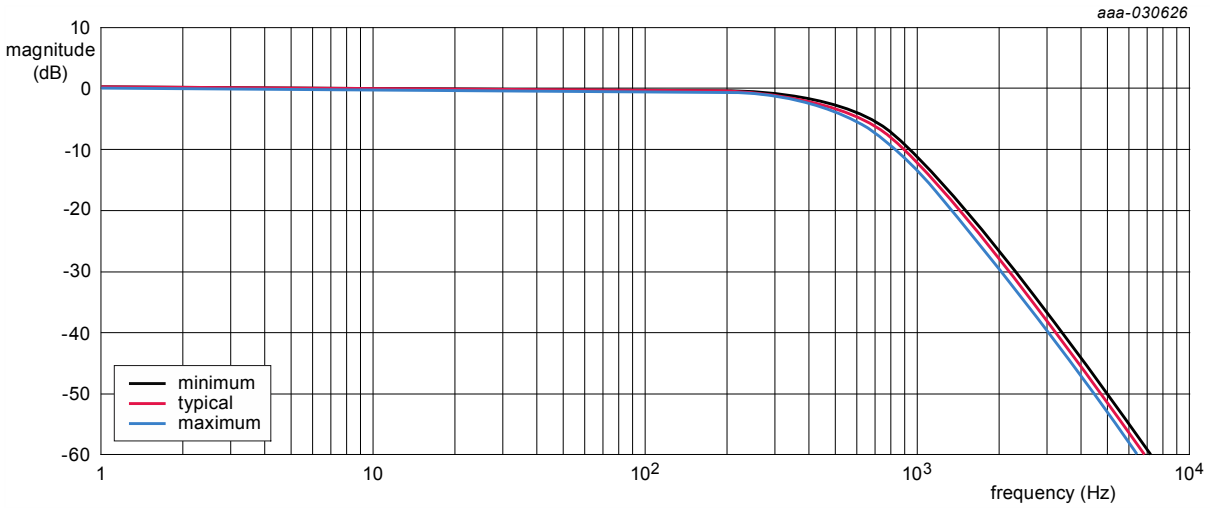



Figure 39. **500 Hz, 3-pole low-pass filter response signal delay**

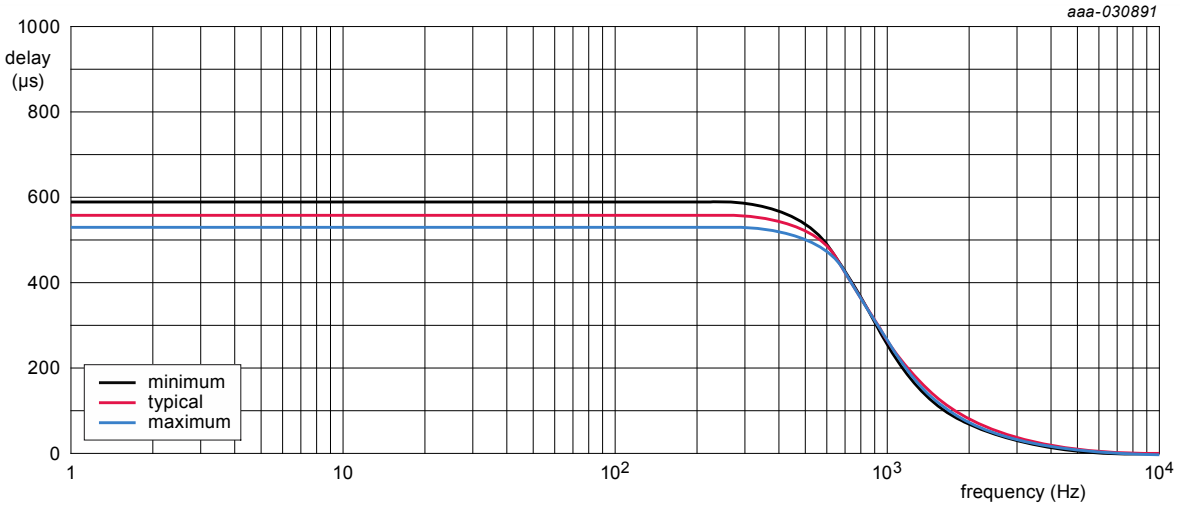


Figure 40. **800 Hz, 4-pole low-pass filter response magnitude**

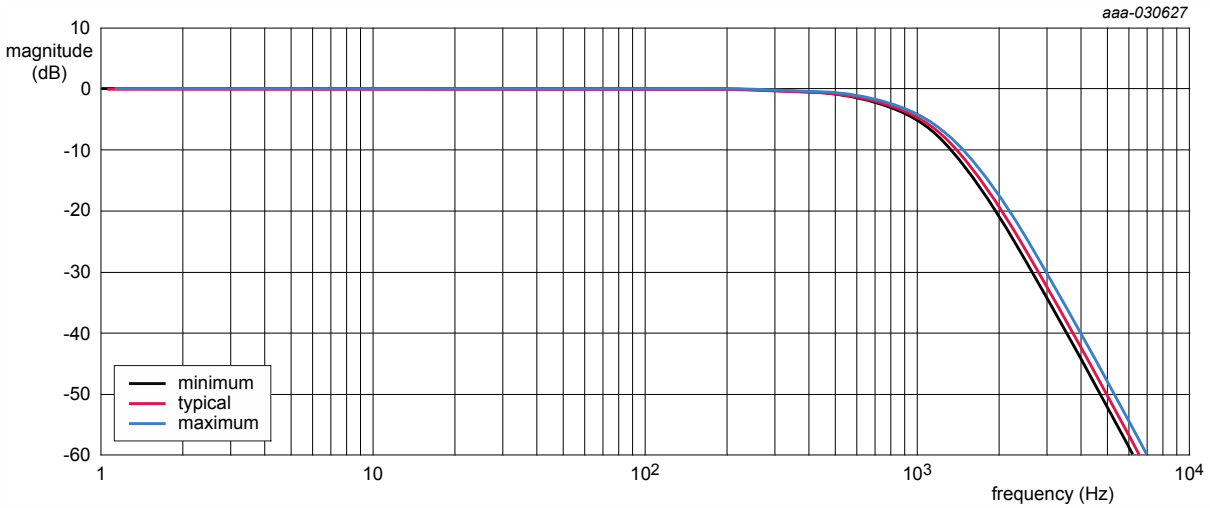



Figure 41. **800 Hz, 4-pole low-pass filter response signal delay**

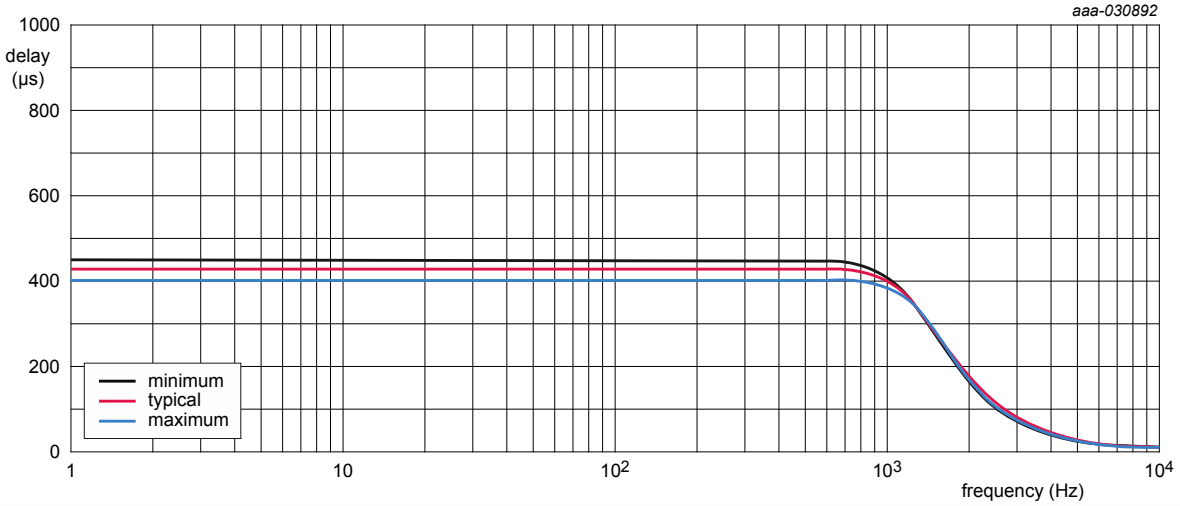


Figure 42. **1200 Hz, 4-pole low-pass filter response magnitude**

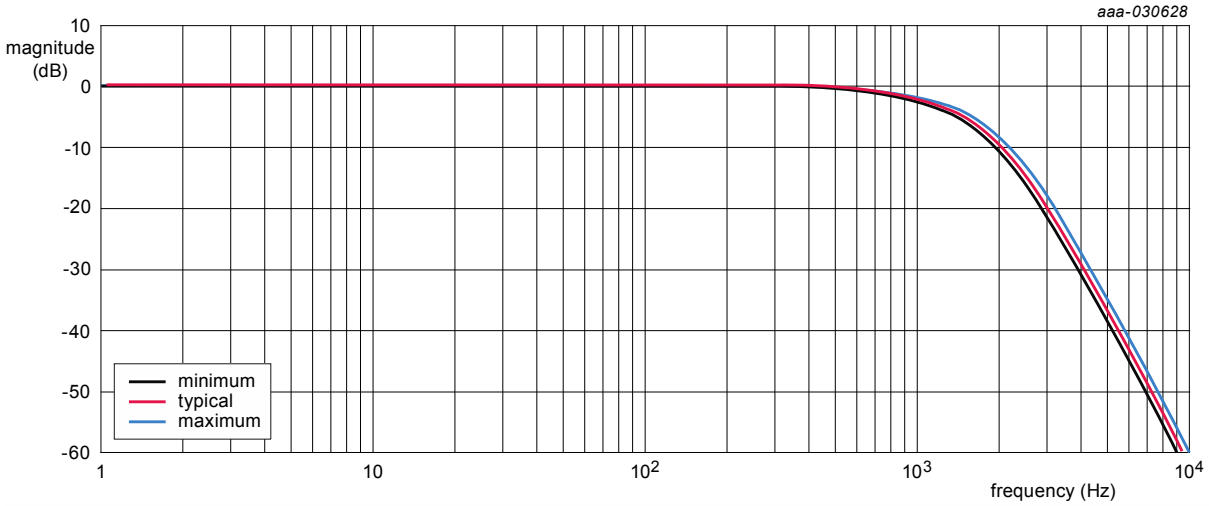



Figure 43. **1200 Hz, 4-pole low-pass filter response signal delay**

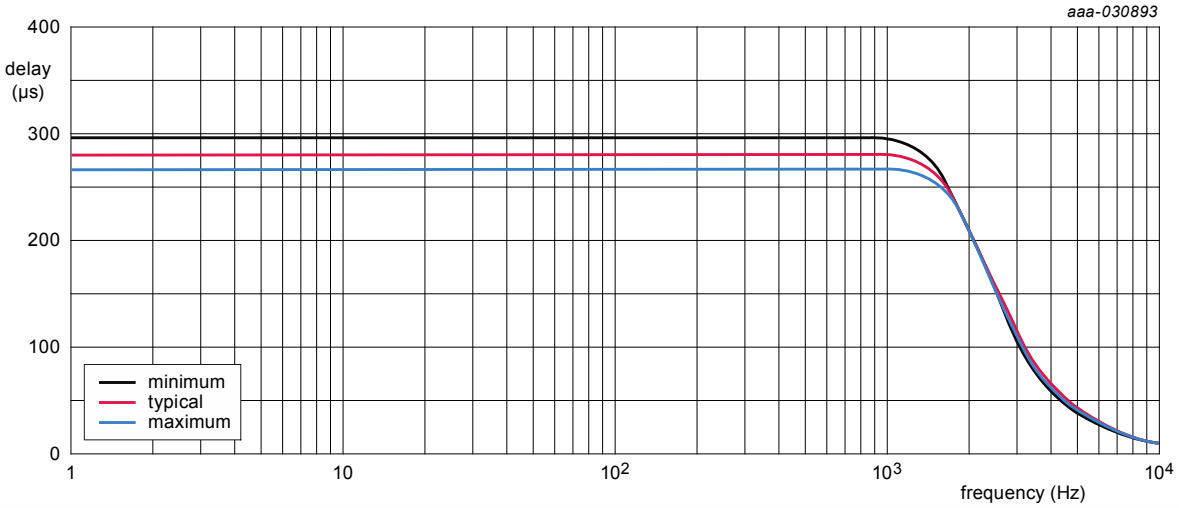


Figure 44. **120 Hz, 3-pole low-pass filter response magnitude**

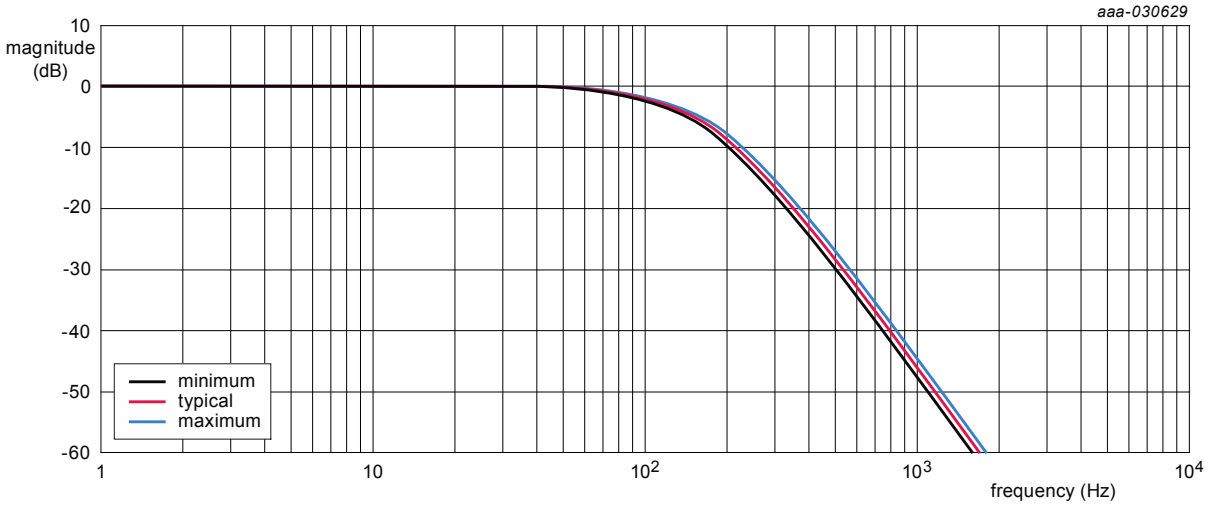



Figure 45. **120 Hz, 3-pole low-pass filter response signal delay**

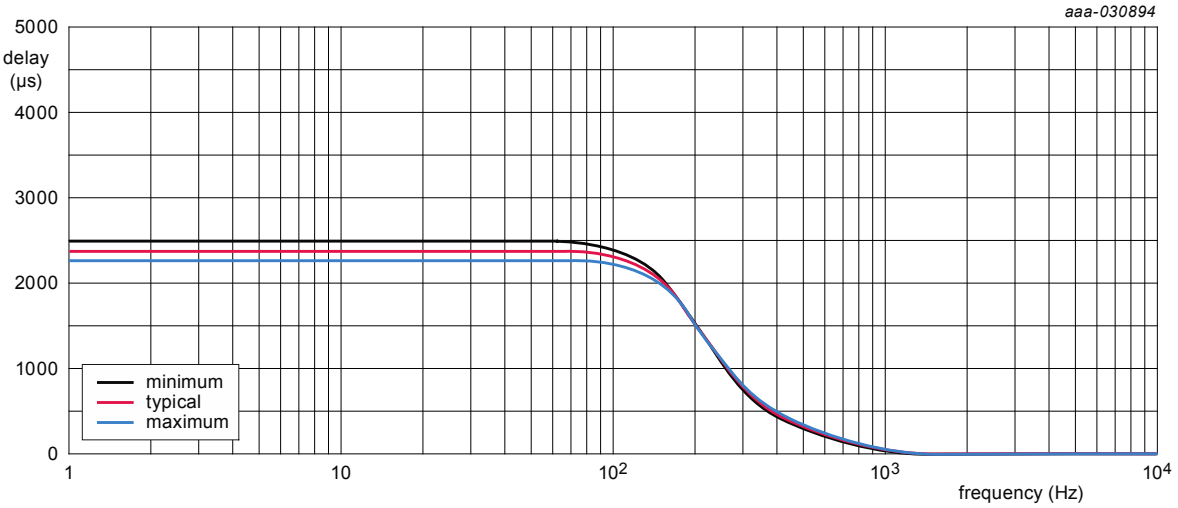


Figure 46. **120 Hz, 2-pole low-pass filter output magnitude response**

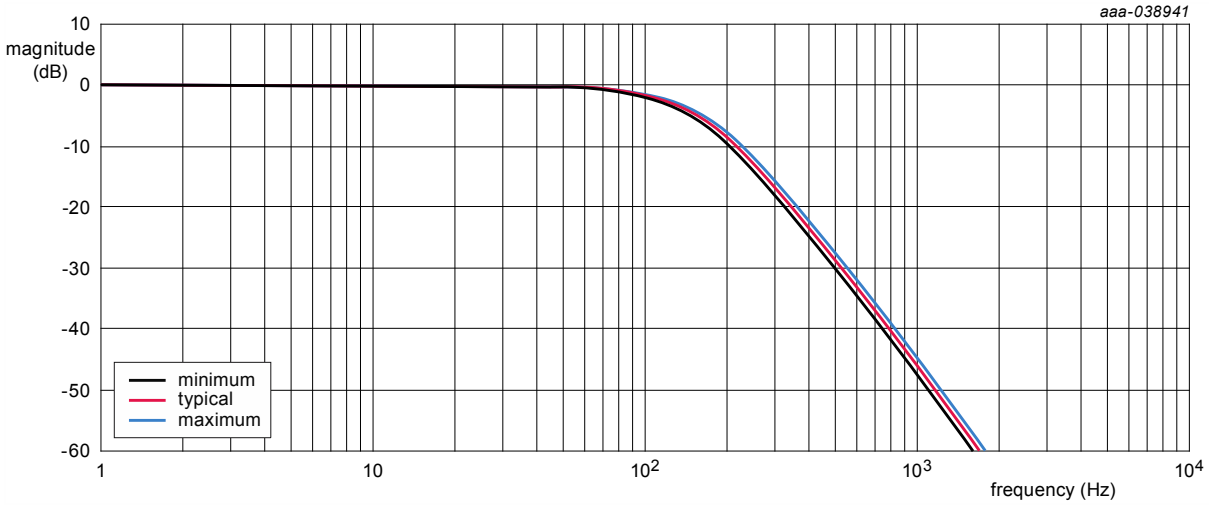



Figure 47. **120 Hz, 2-pole low-pass filter output magnitude response**

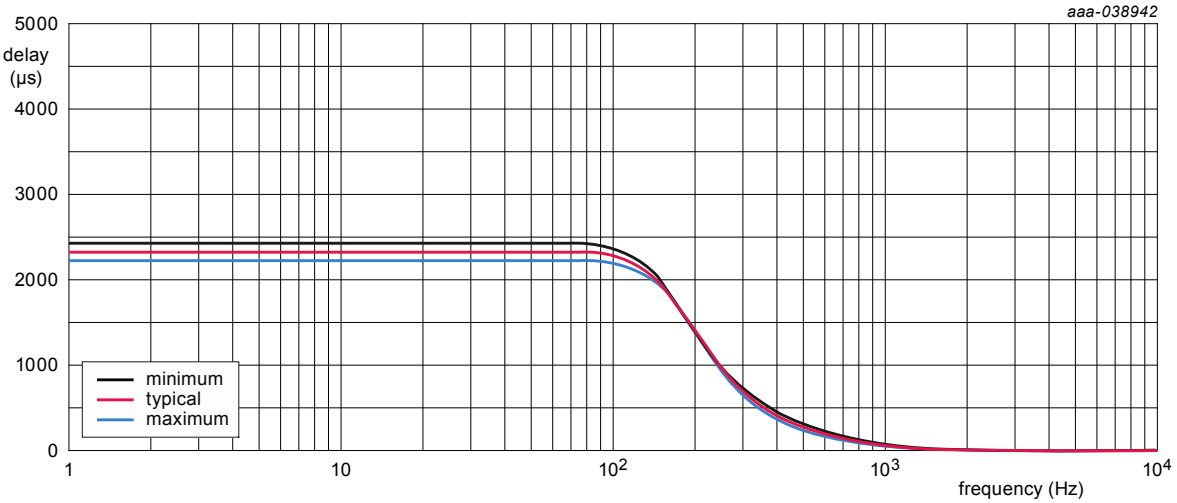



Figure 48. **50 Hz, 4-pole low-pass filter response magnitude**

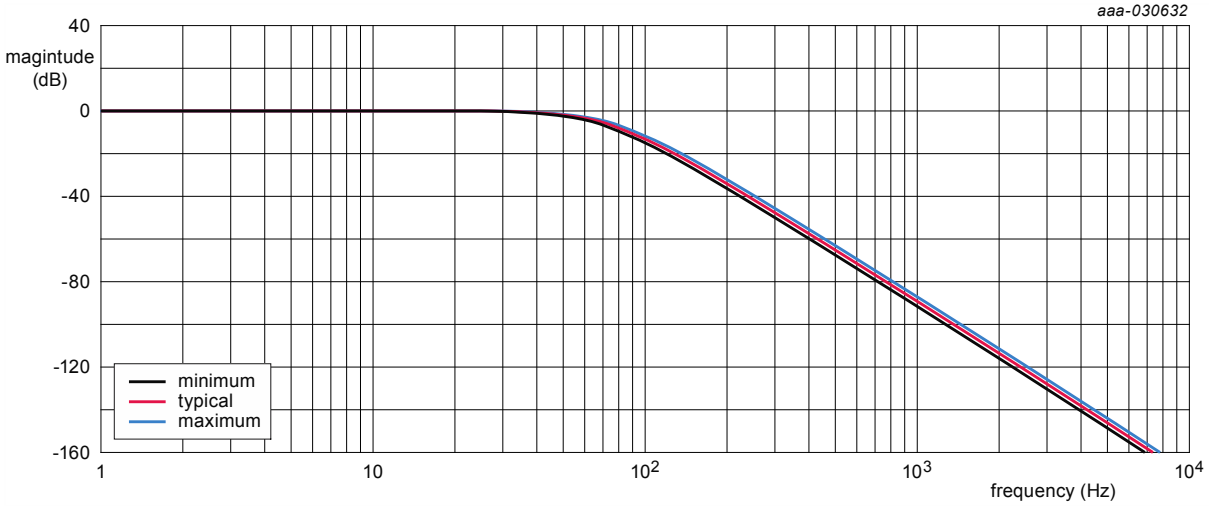
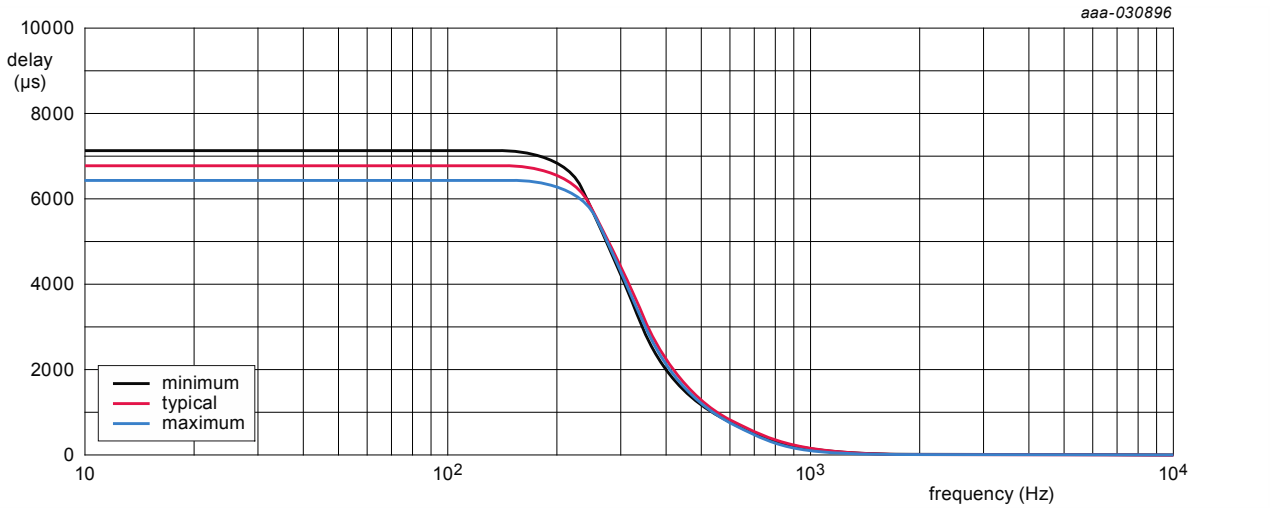


Figure 49. **50 Hz, 4-pole low-pass filter response signal delay**



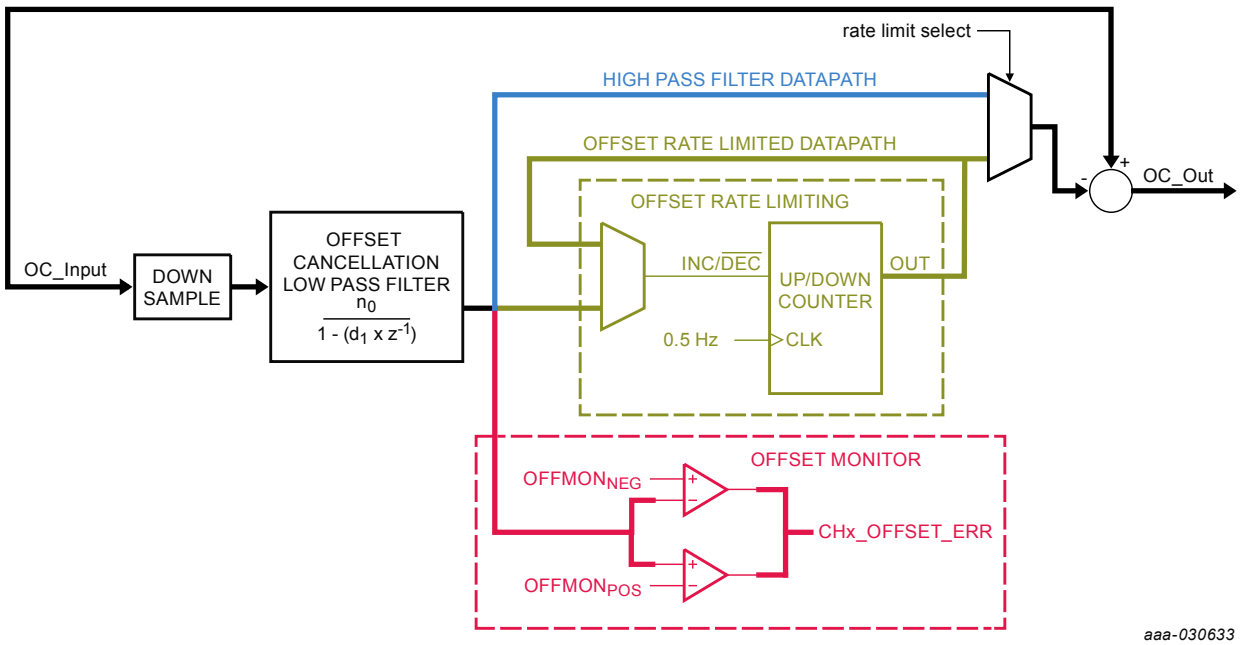

### 8.6.4.5 *User sensitivity scaling*

The device includes a user controlled sensitivity scaling as described in Section 8.2.24.1: User sensitivity multiplier bits (U_SNS_MULT[7:0]).

### 8.6.4.6 *Offset cancellation*

The device provides an optional offset cancellation circuit to remove internal offset error. A simplified block diagram of the offset cancellation is shown in Figure 50. Offset cancellation block diagram.

Figure 50. **Offset cancellation block diagram**




The transfer function for the offset low-pass filter is:

$$H(z) = a_0 \times \frac{n_0(n_1 \cdot z^{-1})}{d_0(d_1 \cdot z^{-1})} \quad (11)$$

Response parameters are specified in Section 7: Electrical characteristics and the offset low-pass filter coefficients are specified in Table 219. Offset cancellation phases and times: DSI3, SPI, and I²C modes.

During startup, multiple phases of the offset low-pass filter are used to allow for fast convergence of the internal offset error during initialization. The offset rate limiting is also bypassed regardless of the state of the OC_FILT bits in the CHx_CFG_U4 register. The low-pass filter details and timing for the startup phases is shown in Table 219. Offset cancellation phases and times: DSI3, SPI, and I²C modes.

In normal mode, the offset low-pass filter frequency can be selected and output rate limiting can be applied to the output of the offset low-pass filter via the OC_FILT bits in the CHx_CFG_U4 register. Rate limiting can only be enabled if the 0.04 Hz offset LPF is selected. If rate limiting is enabled, the offset cancellation output is updated by $OFF_{Step}$ LSB every $t_{RL\_Rate}$ seconds.

The offset cancellation circuit output value is frozen when analog or digital self-test is active (ST_CTRL = 0x8 - 0xF) regard-less of the offset cancellation phase. When analog or digital self-test is deactivated, the offset cancellation output value freeze is extended for 15 ms before continuing updates.

**Table 219. Offset cancellation phases and times: DSI3, SPI, and I²C modes**

| Offset LPF startup phase | Time from reset to start of phase (ms) | Sample Time (us) | Coefficients (24 bit) | | | | LPF corner frequency (-3 dB) (Hz) | Time constant (τ) (ms) | Rate limiting |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 256 | a0 | 0.234051465988159 | | | 163.8 | 0.9714 | Bypassed |
| | | | n0 | 0.49999988079071 | n1 | 0.49999988079071 | | | |
| | | | d0 | 1.0 | d1 | –0.765948414802551 | | | |
| 1 | 4.096 | 256 | a0 | 0.063805103302002 | | | 40.96 | 3.886 | Bypassed |
| | | | n0 | 0.49999988079071 | n1 | 0.49999988079071 | | | |
| | | | d0 | 1.0 | d1 | –0.936194777488708 | | | |
| 2 | 8.192 | 256 | a0 | 0.0163367986679077 | | | 10.24 | 15.54 | Bypassed |
| | | | n0 | 0.49999988079071 | n1 | 0.49999988079071 | | | |
| | | | d0 | 1.0 | d1 | –0.983663082122802 | | | |
| 3 | 24.58 | 256 | a0 | 0.00410926342010498 | | | 2.560 | 62.17 | Bypassed |
| | | | n0 | 0.49999988079071 | n1 | 0.49999988079071 | | | |
| | | | d0 | 1.0 | d1 | –0.995890617370605 | | | |
| 4 | 90.11 | 256 | a0 | 0.00102889537811279 | | | 0.6400 | 248.7 | Bypassed |
| | | | n0 | 0.49999988079071 | n1 | 0.49999988079071 | | | |
| | | | d0 | 1.0 | d1 | –0.998970985412597 | | | |
| 5 | 352.3 | 256 | a0 | 0.000257253646850586 | | | 0.1600 | 994.7 | Bypassed |
| | | | n0 | 0.49999988079071 | n1 | 0.49999988079071 | | | |
| | | | d0 | 1.0 | d1 | –0.999742627143859 | | | |
| 6a | 1401 | 256 | a0 | 0.0000643377478321934 | | | 0.0400 | 3979 | Controlled by OC_FILT[1:0] |
| | | | n0 | 0.49999988079071 | n1 | 0.49999988079071 | | | |
| | | | d0 | 1.0 | d1 | –0.9999356623 | | | |
| 6b | 1401 | 1024 | a1 | 0.00003216939131789331 | | | 0.005 | 32000 | Bypassed |
| | | | n10 | 0.5 | n11 | 0.5 | | | |
| | | | d10 | 1 | d11 | –0.99996783025562763214 | | | |
| Self-test Active | Output Frozen | | | | | | | | |

**Table 220. Offset cancellation phases and times: PSI5 modes**

| Offset LPF startup phase | Time from reset to start of phase (ms) | LPF corner frequency (–3 dB) (Hz) | Time constant (τ) (ms) | Rate limiting |
|---|---|---|---|---|
| 0 | 0 | 163.8 | 0.9714 | Bypassed |
| 1 | 4.096 | 40.96 | 3.886 | Bypassed |
| 2 | 8.192 | 10.24 | 15.54 | Bypassed |
| 3 | 24.58 | 2.560 | 62.17 | Bypassed |
| 4 | 90.11 | 0.6400 | 248.7 | Bypassed |

| Offset LPF startup phase | Time from reset to start of phase (ms) | LPF corner frequency (–3 dB) (Hz) | Time constant (τ) (ms) | Rate limiting |
|---|---|---|---|---|
| 6a | End of Initialization Phase 3 | 0.0400 | 3979 | Controlled by OC_FILT[1:0] |
| 6b | End of Initialization Phase 3 | 0.005 | 32000 | Bypassed |

**Figure 51. 0.04 Hz offset cancellation low–pass filter characteristics**

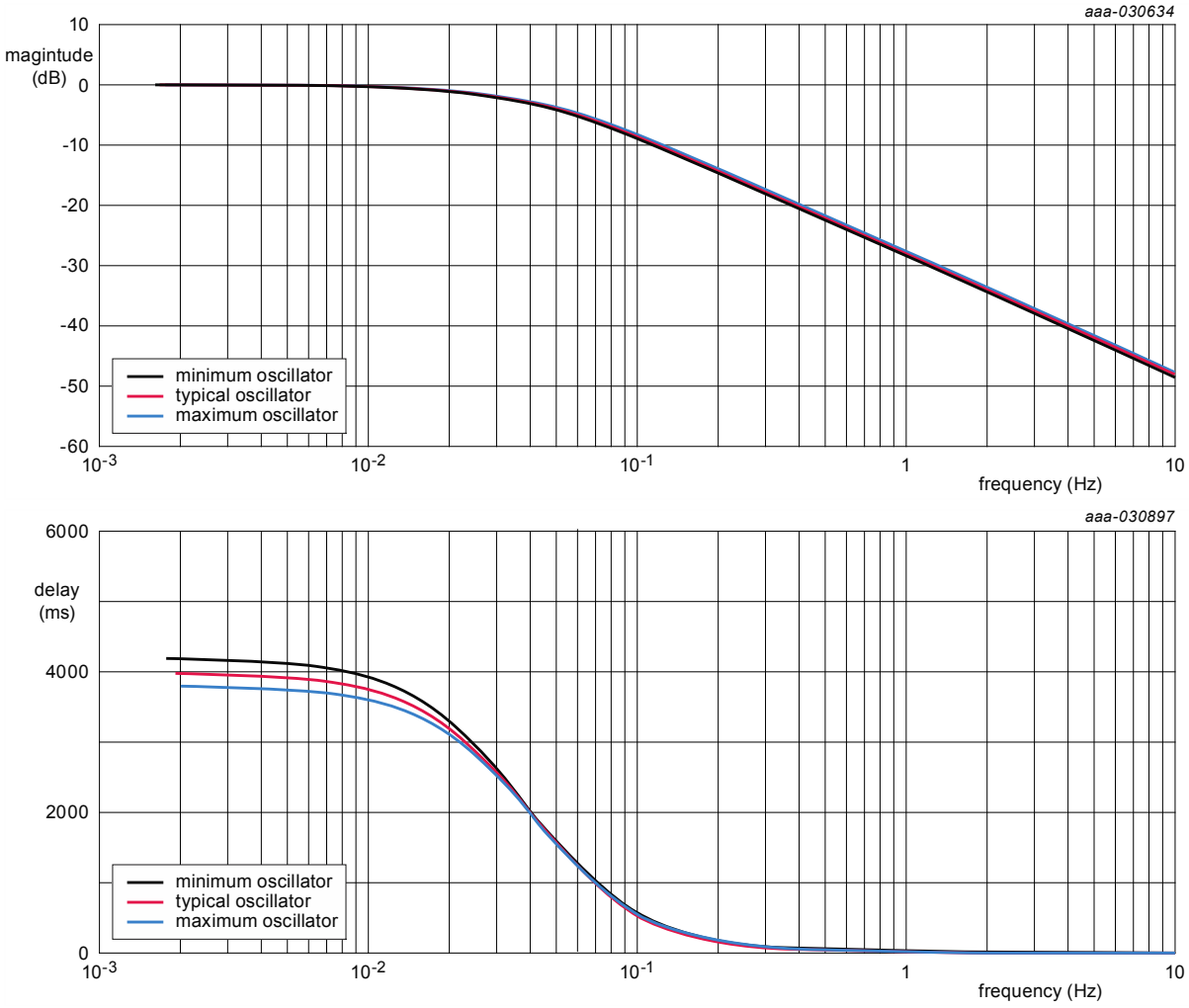
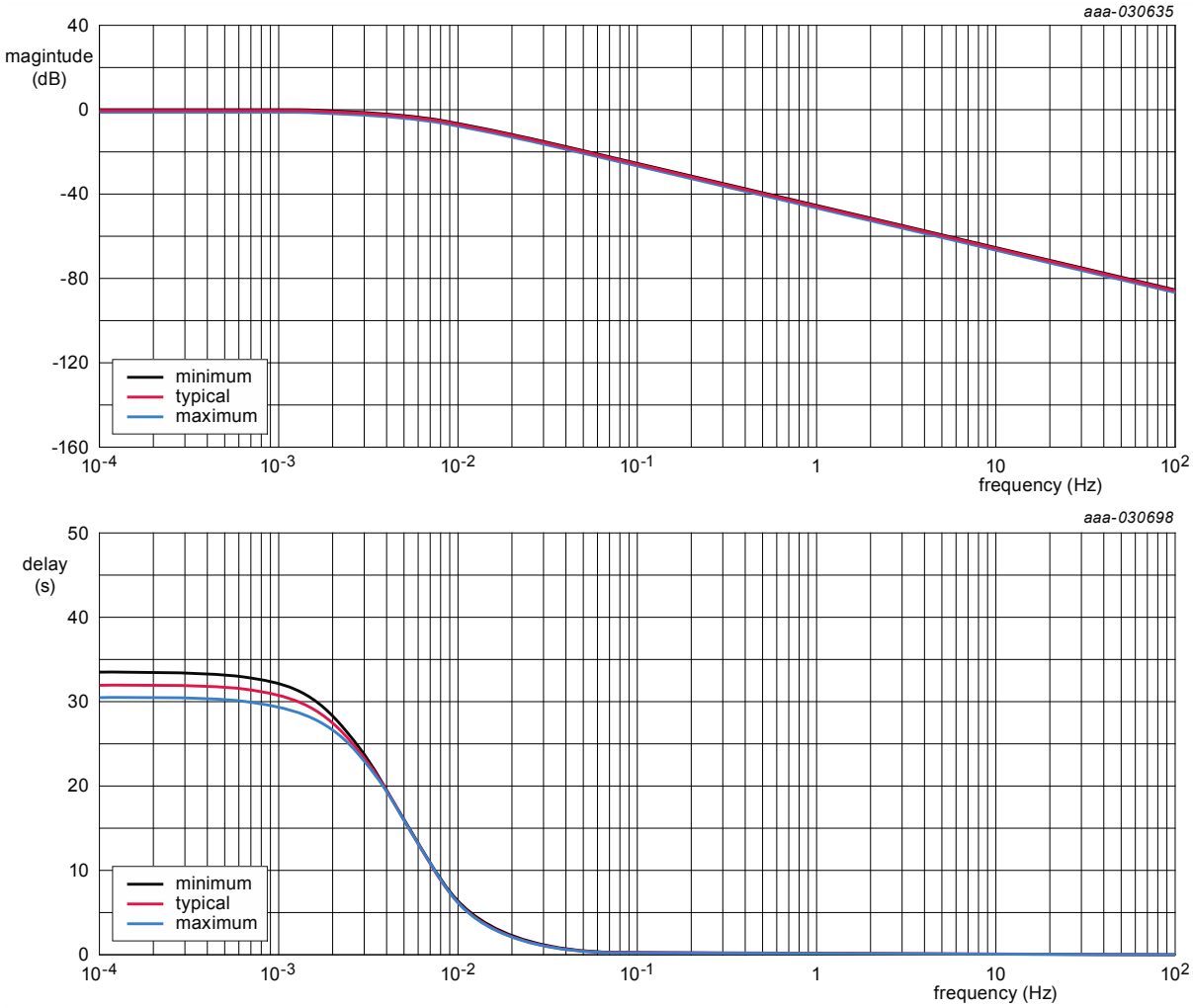


Figure 52. **0.005 Hz offset cancellation low-pass filter characteristics**




### 8.6.4.7 *Moving average*

The device includes an optional moving average function. See Section 8.2.25.4: Signal chain moving average selection bits (MOVEAVG[1:0]) for details regarding the moving aver-age function. If the moving average function is enabled, interpolation is disabled.

### 8.6.4.8 *Data interpolation*

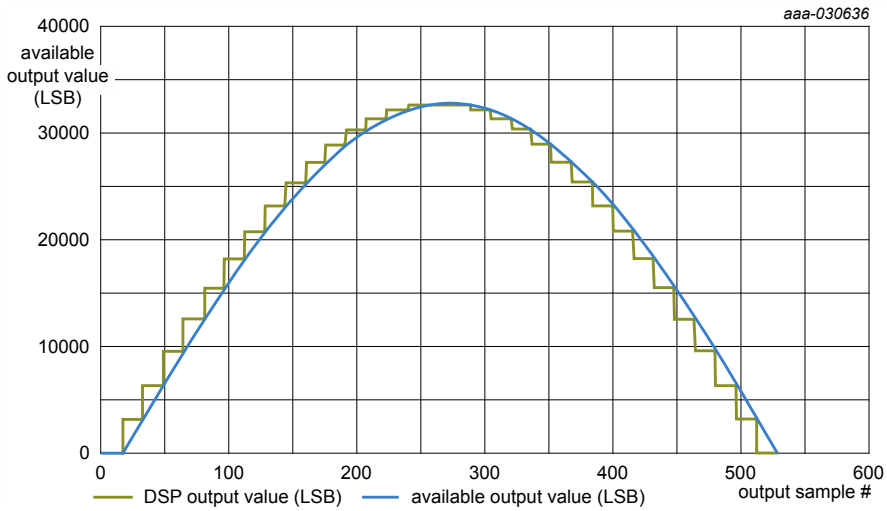
The device includes 16 to 1 linear data interpolation to minimize the system sample jitter. Each result produced by the digital signal processing chain is delayed one sample time. Transmitted data is interpolated from the 2 previous samples, resulting in a latency of one sample time, and a maximum signal jitter of 1/16 of the sample time. The device uses the following functions for calculating the interpolation:

$$DataInterpOut_i = DataInterpOut_{i-1} + \frac{DSPOut_{Current} - DataInterpOut_{i-1}}{16 - (i-1)} \quad (12)$$

$$DataInterpOut_0 = DSPOut_{Previous} \quad (13)$$

An example of the output interpolation is shown in Figure 53. Output interpolation example: Linear interpolation (16 to 1).

Figure 53. **Output interpolation example: Linear interpolation (16 to 1)**




### 8.6.4.9 *Output scaling*

Table 221. Output scaling shows the output scaling for each output data type and protocol.

Table 221. **Output scaling**

| Data Type | PCM | SPI | DSI | PSI5 | I²C | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 16-bit Register Read | | x | x | x | x | | | | | | | | | | | | | | | | | | | | | | | | |
| 16-bit | | | x | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 16-bit | | x | | x | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12-bit | | x | x | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10-bit | x | | x | x | | | | | | | | | | | | | | | | | | | | | | | | | |
| CHx_U_OFFSET | x | x | x | x | x | | | | | | | | | | | | | | | | | | | | | | | | |
| | Readable Data | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Noise Bits | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Clipped Bits | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Eq. (14) is used to convert sensor data readings to acceleration using the variables specified in Table 222. Sensor data variables.

*Note: The values listed apply for a user gain of 1x (U_SNS_SHIFT = '10' and U_SNS_MULT = 0x00).*

$$Acceleration_g = \frac{SensorData_{LSB} - SensorDataOFF_{LSB}}{SENSE_{ACCEL}} \quad (14)$$

Where:

*Acceleration* $_g$ = The acceleration output in g

*SensorData* $_{LSB}$ = The acceleration output in LSB

*SensorDataOFF* $_{LSB}$ = The acceleration output value at 0 g in LSB

*SENSE* $_{ACCEL}$ = The expected sensitivity in LSB/g

Table 222. **Sensor data variables**

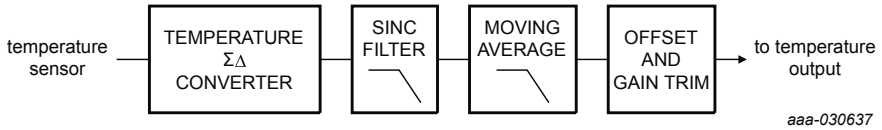
| g Range type | Data reading | Typical *SensorDataOFF* LSB (LSB) | *SENSE* ACCEL (LSB/g) | Minimum sensor data value (Signed LSB) | Maximum sensor data value (Signed LSB) |
|---|---|---|---|---|---|
| Low g | 16-bit Register Read | 0 | 683.6686 | 0x8000 (–32768) | 0x7FFF (+32767) |
| | 16-bit DSI3 PDCM Sensor Data | 0 | 683.6686 | 0x8001 (–32767) | 0x7FFF (+32767) |
| | 16-bit SPI Sensor Data | 0 | 5469.349 | 0x8010 (–32752) | 0x7FFF (+32767) |
| | 16-bit PSI5 Sensor Data | 0 | 5469.349 | 0x8800 (–30720) | 0x7800 (+30720) |
| | 12-bit DSI3 PDCM Sensor Data | 0 | 341.8343 | 0x801 (–2047) | 0x7FF (+2047) |
| | 12-bit SPI Sensor Data | 0 | 341.8343 | 0x801 (–2047) | 0x7FF (+2047) |
| | 10-bit DSI3 PDCM Sensor Data | 0 | 85.45858 | 0x201 (–511) | 0x1FF (+511) |
| | 10-bit PSI5 Sensor Data | 0 | 85.45858 | 0x220 (–480) | 0x1E0 (+480) |
| Medium g | 16-bit Register Read | 0 | 66.0322 | 0x8000 (–32768) | 0x7FFF (+32767) |
| | 16-bit DSI3 PDCM Sensor Data | 0 | 66.0322 | 0x8001 (–32767) | 0x7FFF (+32767) |
| | 16-bit SPI Sensor Data | 0 | 528.258 | 0x8010 (–32752) | 0x7FFF (+32767) |
| | 16-bit PSI5 Sensor Data | 0 | 528.258 | 0x8800 (–30720) | 0x7800 (+30720) |
| | 12-bit DSI3 PDCM Sensor Data | 0 | 33.0161 | 0x801 (–2047) | 0x7FF (+2047) |
| | 12-bit SPI Sensor Data | 0 | 33.0161 | 0x801 (–2047) | 0x7FF (+2047) |
| | 10-bit DSI3 PDCM Sensor Data | 0 | 8.25403 | 0x201 (–511) | 0x1FF (+511) |
| | 10-bit PSI5 Sensor Data | 0 | 8.25403 | 0x220 (–480) | 0x1E0 (+480) |
| High g | 16-bit Register Read | 0 | 21.8930 | 0x8000 (–32768) | 0x7FFF (+32767) |
| | 16-bit DSI3 PDCM Sensor Data | 0 | 21.8930 | 0x8001 (–32767) | 0x7FFF (+32767) |
| | 16-bit SPI Sensor Data | 0 | 175.144 | 0x8010 (–32752) | 0x7FFF (+32767) |
| | 16-bit PSI5 Sensor Data | 0 | 175.144 | 0x8800 (–30720) | 0x7800 (+30720) |
| | 12-bit DSI3 PDCM Sensor Data | 0 | 10.9465 | 0x801 (–2047) | 0x7FF (+2047) |
| | 12-bit SPI Sensor Data | 0 | 10.9465 | 0x801 (–2047) | 0x7FF (+2047) |
| | 10-bit DSI3 PDCM Sensor Data | 0 | 2.73663 | 0x201 (–511) | 0x1FF (+511) |
| | 10-bit PSI5 Sensor Data | 0 | 2.73663 | 0x220 (–480) | 0x1E0 (+480) |

## 8.7 Temperature sensor

### 8.7.1 Temperature sensor signal chain

The device includes an independent temperature sensor for each channel for signal compensation. The output of the channel 0 temperature sensor is provided for user readability. A simplified block diagram is shown in Figure 54. Temperature sensor signal chain block diagram. Temperature sensor parameters are specified in Section 7.5: Electrical characteristics - temperature sensor signal chain and Section 7.19: Dynamic electrical characteristics - digital self-test response time.

Figure 54. **Temperature sensor signal chain block diagram**



### 8.7.2 Temperature sensor output scaling equations

Eq. (15) is used to convert temperature readings with the variables as specified.

$$T_{DEGC} = \frac{T_{LSB} - T0_{LSB}}{T_{SENSE}} \quad (15)$$

Where:

$T_{DEGC}$ = The temperature output in degrees C

$T_{LSB}$ = The temperature output in LSB

$T0_{LSB}$ = The expected temperature output in LSB at 0 C

$T_{SENSE}$ = The expected temperature sensitivity in LSB/C

**Table 223. Temperature sensor output scaling equation variables**

| Data reading | $T0_{LSB}$ (LSB) | $T_{SENSE}$ (LSB/C) |
|---|---|---|
| 8-bit Register Read | 68 | $T_{SENSE}$ |
| 16-bit Register Read | 17408 | $T_{SENSE} * 256$ |
| 16-bit DSI3 PDCM Sensor Data | 17408 | $T_{SENSE} * 256$ |
| 16-bit SPI Sensor Data | 17408 | $T_{SENSE} * 256$ |
| 16-bit PSI5 Sensor Data | –1728 | $T_{SENSE} * 64$ |
| 12-bit DSI3 PDCM Sensor Data | 1100 | $T_{SENSE} * 16$ |
| 12-bit SPI Sensor Data | 1100 | $T_{SENSE} * 16$ |
| 10-bit DSI3 PDCM Sensor Data | 276 | $T_{SENSE} * 4$ |
| 10-bit PSI5 Sensor Data | –27 | $T_{SENSE}$ |

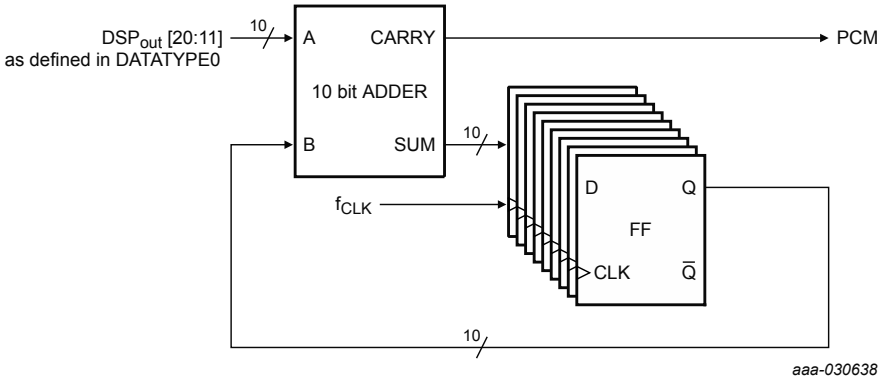
## 8.8 PCM output function

The device provides the option for a PCM output function. The PCM output is enabled if the ARM_CFG bits in the CHx_CF-G_U4 registers are configured for PCM output. Selecting the PCM output enables the following functions:

- The non-interpolated sensor data output as defined in the DATATYPE0 bits in the Chx_CFG_U3 register is saturated to 10-bits as shown in Section 8.6.4.9: Output scaling and converted to an unsigned value.
- The 10-bit sensor value is input into a summer clocked at 10 MHz.
- The carry from the summer circuit is output to the PCM pin.

A block diagram of the PCM output is shown in Figure 55. PCM output function block diagram.

Figure 55. **PCM output function block diagram**




## 8.9 Arming function

When SPI mode is enabled via the COMMTYPE register, the device provides the option for an arming function with 3 modes of operation. The operation of the arming function is selected by the state of the ARM_CFG bits in the CHx_CFG_U4 registers.

See Section 11.5: Exception handling for the operation of the Arming function with exception conditions. Error conditions do not impact prior arming function responses. If an error occurs after an arming activation, the corresponding pulse stretch for the existing arming condition will continue. However, new sensor reads will not update the arming function regardless of the sensor value.

### 8.9.1 Arming function: moving average mode

In moving average mode, the arming function runs a moving average on the offset canceled output of the associated sensor channel DATATYPE0. The number of samples used for the moving average (k) is programmable via the ARM_WS[1:0] bits in the CHx_ARM_CFG registers. See Section 8.2.28.3: Arming window size (ARM_WS_N[1:0], A_WS_P[1:0]) for register details.

$$ARM\_MA_n = \frac{(OC_n + OC_{n-1} + \ldots + OC_{n+1-k})}{k} \quad (16)$$

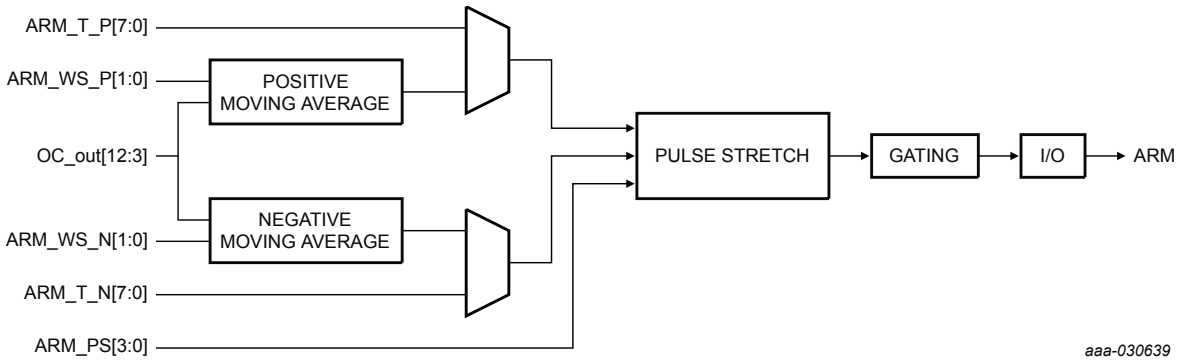
Where n is the current sample.

The sample rate for each channel is determined by the rate of the SPI sensor data requests. At the falling edge of SS_B for a sensor data SPI response for SOURCEID_0 SOURCEID_0 (channel 0) or SOURCEID_2 (channel 1), the moving average for the associated channel is updated with a new sample. See Figure 56. Arming function block diagram - moving average mode. The arming function input data rate can be down sampled as described in Section 8.9.4: Arming function downsampling. The SPI sensor data sample rate must meet the minimum time between requests ($t_{ACC\_REQ\_x}$) specified in Section 7.14: Dynamic electrical characteristics - SPI.

The moving average output is compared against positive and negative thresholds that are individually programmed for each channel via the CHx_ARMT_x registers. See Section 8.2.29: Arming threshold registers (CH0_ARM_T_P CHx_ARM_T_P, CH0_ARM_T_N CHx_ARM_T_N) for register details. If the moving average equals or exceeds either threshold, an arming condition is indicated, the arming pin output is asserted for the associated channel, and the pulse stretch counter is set as described in Section 8.9.5: Arming pulse stretch function.

The arming pin output is deasserted only when the pulse stretch counter expires. Figure 56. Arming function block diagram - moving average mode shows the arming output operation for different SPI conditions.

Figure 56. **Arming function block diagram - moving average mode**




### 8.9.2 Arming function: count mode

In count mode, the arming function compares each offset canceled sample against positive and negative thresholds that are individually programmed for each channel via the CHx_ARMT_x_x and CHx_ARMT_x_x registers. See Section 8.2.29: Arming threshold registers (CH0_ARM_T_P CHx_ARM_T_P, CH0_ARM_T_N CHx_ARM_T_N) for register details. If the sample equals or exceeds either threshold, a sample counter is incremented. If the sample does not exceed either threshold, the sample counter is reset to zero.

The sample rate for each channel is determined by the SPI sensor data sample rate. At the falling edge of SS_B for a sensor data SPI response for SOURCEID_0 SOURCEID_0 (channel 0) or SOURCEID_2 (channel 1), a new sample for the associated channel is compared against the thresholds. See Figure 57. Arming function block diagram - count mode. The arming function input data rate can be down sampled as described in Section 8.9.4: Arming function downsampling. The SPI sensor data sample rate must meet the minimum time between requests ($t_{ACC\_REQ\_x}$) specified in Section 7.14: Dynamic electrical characteristics - SPI.

A sample count limit is programmable via the ARM_WS[1:0] bits in the CHx_ARM_CFG registers. If the sample count reaches the programmable sample count limit, an arming condition is indicated, the associated arm pin output is asserted, and the pulse stretch counter is set as described in Section 8.9.5: Arming pulse stretch function.

The associated arm pin output is deasserted only when the pulse stretch counter expires. Figure 58. Arming condition, moving average and count mode shows the arming output operation for different SPI conditions.

Figure 57. **Arming function block diagram - count mode**

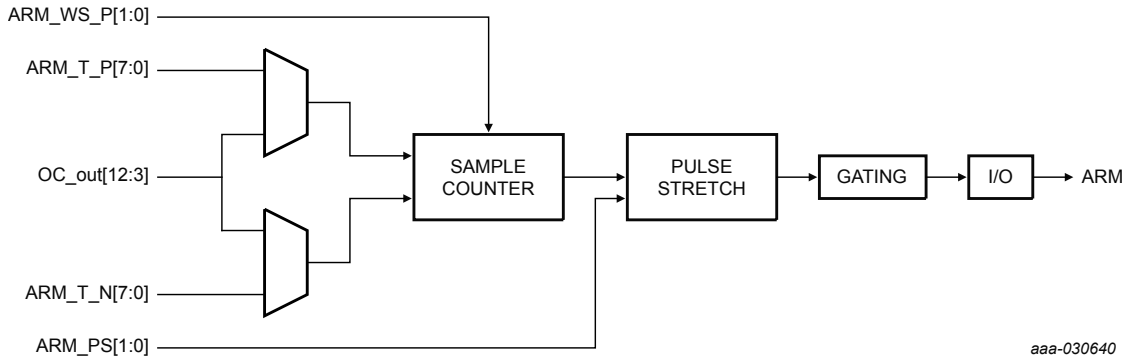
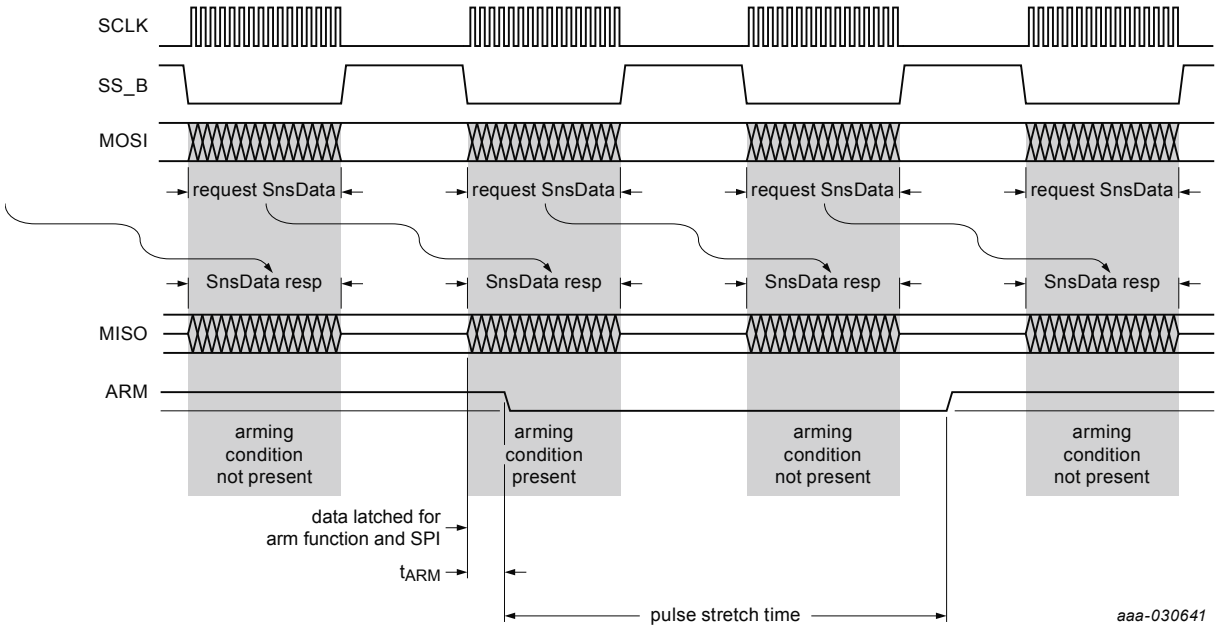


Figure 58. **Arming condition, moving average and count mode**




### 8.9.3 Arming function: unfiltered mode

At the falling edge of SS_B for a sensor data SPI response for SOURCEID_0 SOURCEID_0 (channel 0) or SOURCEID_2 (channel 1), the most recent available offset canceled sample for the requested channel is compared against positive and negative thresholds that are individually programmed for each channel via the CHx_ARM_T_x and CHx_ARM_T_x registers. See Section 8.2.29: Arming threshold registers (CH0_ARM_T_P CHx_ARM_T_P, CH0_ARM_T_N CHx_ARM_T_N) for register details. If the sample equals or exceeds either threshold, an arming condition is indicated.

Once an arming condition is indicated for the associated channel, the arm pin output for that channel is asserted when SS_B is asserted and the MISO data includes a sensor data response for that channel. The pulse stretch function is not applied in Unfiltered mode.

Figure 59. Arming function block diagram - unfiltered mode contains a block diagram of the Arming Function operation in Unfiltered Mode. Figure 60. Arming condition, unfiltered mode shows the Arming output operation under the different SPI request conditions.

Figure 59. **Arming function block diagram - unfiltered mode**

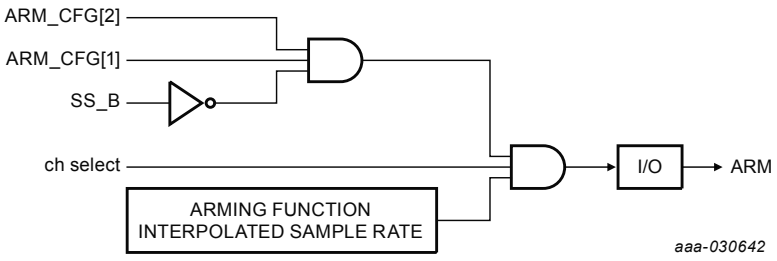
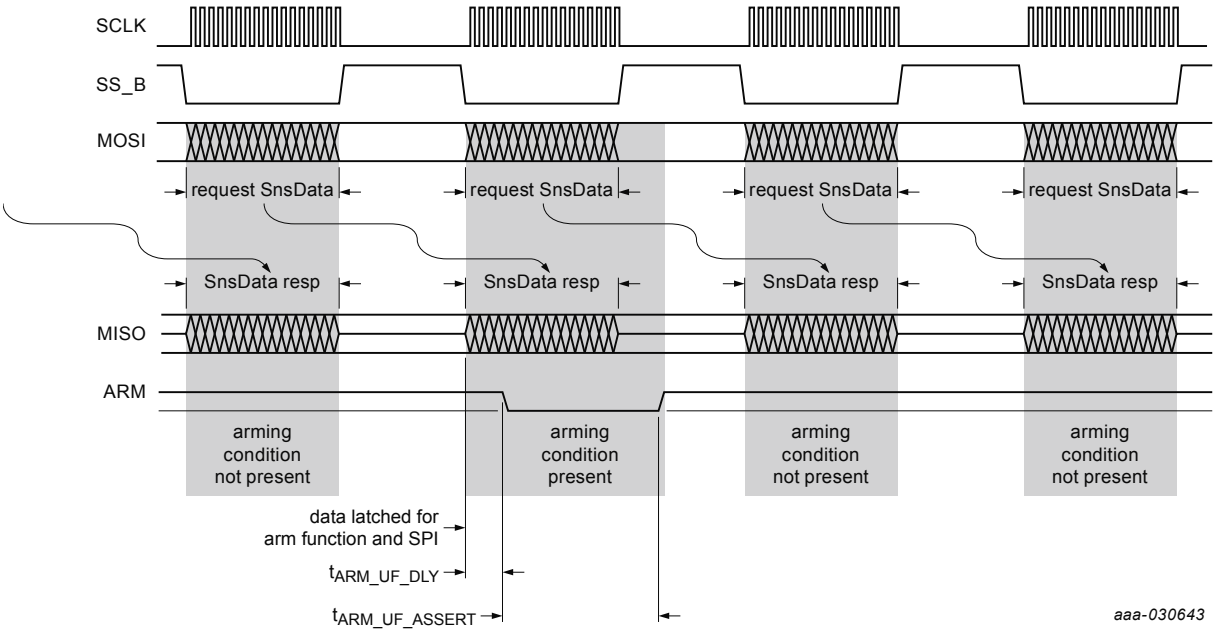


Figure 60. **Arming condition, unfiltered mode**




### 8.9.4 Arming function downsampling

The data provided to the arming function can be downsampled using the ARM_DS[1:0] bits in the CHx_ARM_CFG registers.

The initial value of the counter is zero. At the falling edge of SS_B for a sensor data SPI response, if the counter value is equal to '00', the arming function is updated with the new sample as described in Section 8.9.1: Arming function: moving average mode or Section 8.9.2: Arming function: count mode. The counter is then incremented by one. The counter rolls over to '00' after the maximum value specified in the ARM_DS[1:0] bits is reached.

### 8.9.5 Arming pulse stretch function

A pulse stretch function can be applied to the arming outputs in moving average mode, or count mode.

If the pulse stretch function is not used (ARM_PS[1:0] = '00'), the arming output is asserted if and only if an arming condition exists for the associated channel after the most recent evaluated sample. The arming output is deasserted if and only if an arming condition does not exist for the associated channel after the most recent evaluated sample.

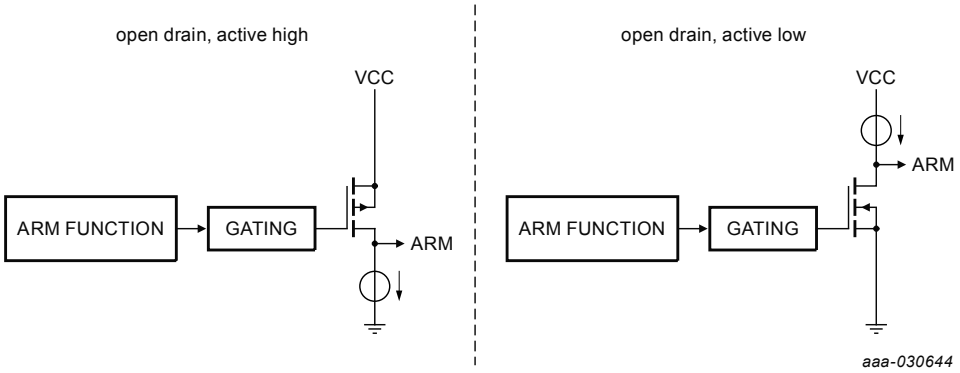
If the pulse stretch function is used (ARM_PS[1:0] not equal '00'), the arming output is controlled only by the value of the pulse stretch timer value. If the pulse stretch timer value is non-zero, the arming output is asserted. If the pulse stretch timer is zero, the arming output is deasserted. The pulse stretch counter continuously decrements until it reaches zero. The pulse stretch counter is reset to the programmed pulse stretch value if and only if an arming condition exists for the associated channel after the most recent evaluated sample. See Figure 58. Arming condition, moving average and count mode.

Exception conditions listed in Section 11.5: Exception handling do not impact prior arming function responses. If an exception occurs after an arming activation, the corresponding pulse stretch for the existing arming condition will continue. However, new sensor reads will not reset the pulse stretch counter regardless of the sensor value.

### 8.9.6 Arming pin output structure

The arming output pin structure can be set to active high, or active low with the ARM_CFG bits in the CHx_CFG_U4 registers as described in Section 8.2.26.4: Arming pin configuration bits (ARM_CFG[2:0]) and PCM range selection bit (PCM). The active high and active low pin output structures are shown in Figure 61. Arming function - pin output structure.

**Figure 61. Arming function - pin output structure**



# 9 DSI3 protocol

The DSI3 [2] standard describes two function classes: Signal Function Class and Power Function Class. The device is a slave conforming to the Signal Function Class requirements. The device does not support Power Function Class. The following sections describe the DSI3 Signal Function Class features supported by the device.

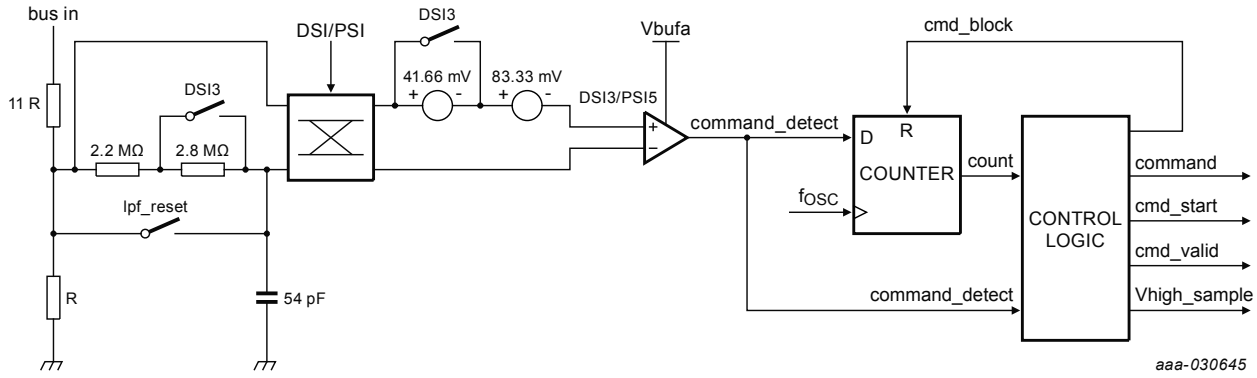
## 9.1 DSI3 physical layer

### 9.1.1 Command receiver

The command receive block converts voltage transitions on the BUS_I pin to a digital pulse train for decoding by the DSI data link layer.

The supply voltage can vary throughout the specified range, so the communication high voltage ($V_{HIGH}$) must be sampled and averaged with a low-pass filter. The communication low voltage is then determined by comparing the supply voltage to the sampled and averaged $V_{HIGH}$ voltage. Figure 62. Command receiver physical layer shows a block diagram of the command receiver physical layer.

**Figure 62. Command receiver physical layer**




The start of a command is detected when the comparator output (Command_Detect) is low. The comparator output is input to a counter that is updated at the internal oscillator frequency. Control logic monitors the counter output and generates the necessary internal signals for the logic.

Figure 63. DSI3 command receiver timing diagram: valid command shows a timing diagram of the command receiver when a valid command is received, and Figure 64. DSI3 command receiver timing diagram: micro-cut shows a timing diagram of the command receiver when a micro-cut is received during the command window. Voltage values and timing parameters are specified in Section 7.4: Electrical characteristics - supply and I/O and Section 7.21: Dynamic electrical characteristics - supply and support circuitry.

Figure 63. **DSI3 command receiver timing diagram: valid command**

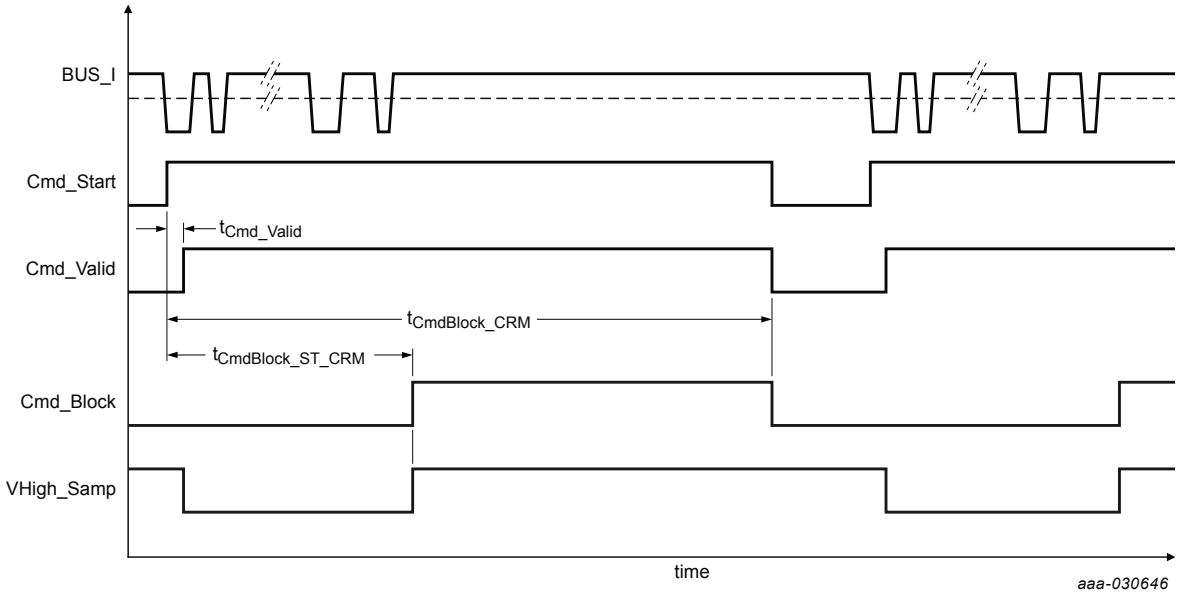
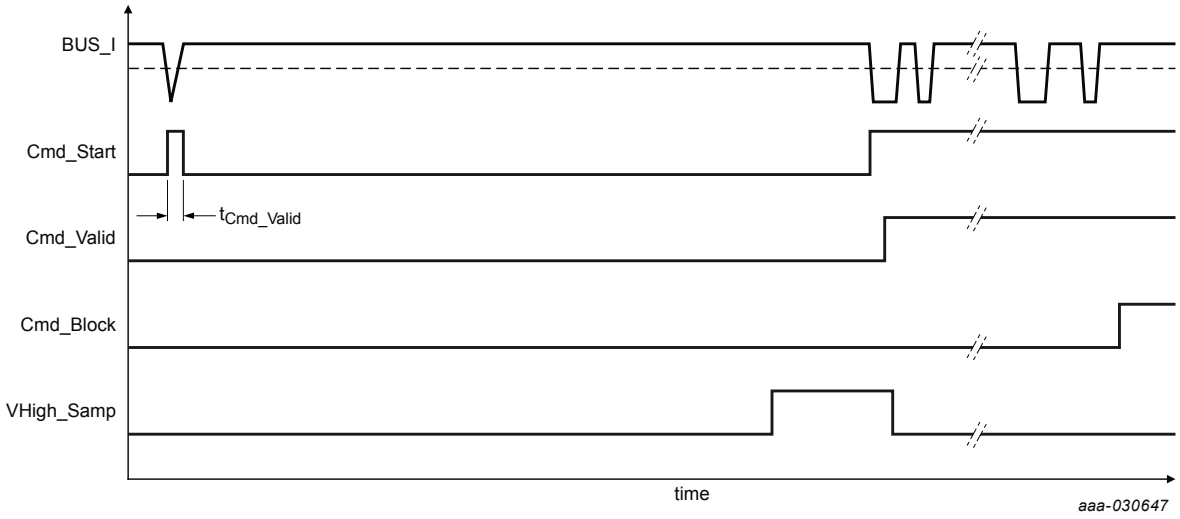


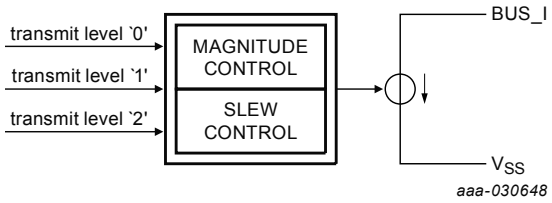

Figure 64. **DSI3 command receiver timing diagram: micro-cut**




### 9.1.2 Response transmitter

The response transmitter block converts two digital signals into two supply modulation current. The response currents are generated such that the rise and fall times are the same whether the $I_{RESP}$ current is being transmitted or the 2 x $I_{RESP}$ cur-rent is being transmitted. A diagram of the response transmitter is shown in Figure 63. DSI3 command receiver timing diagram: valid command. Current values and timing parameters are specified in Section 7.4: Electrical characteristics - supply and I/O and Section 7.12: Dynamic electrical characteristics - DSI3.

Figure 65. **DSI3 transmitter block diagram**




### 9.1.3 Discovery mode current sense

The current sense circuit is used during discovery mode to determine if any additional slaves are connected to the BUS_O pin of the device. A diagram of the current sense circuit is shown in Figure 66. Discovery mode current sense circuit block diagram. Current values and timing parameters are specified in Section 7.4: Electrical characteristics - supply and I/O and Section 7.12: Dynamic electrical characteristics - DSI3. Details regarding discovery mode are included in Section 9.2.3: DSI3 discovery mode: Address assignment method for resistor connected daisy chain devices.

Figure 66. **Discovery mode current sense circuit block diagram**

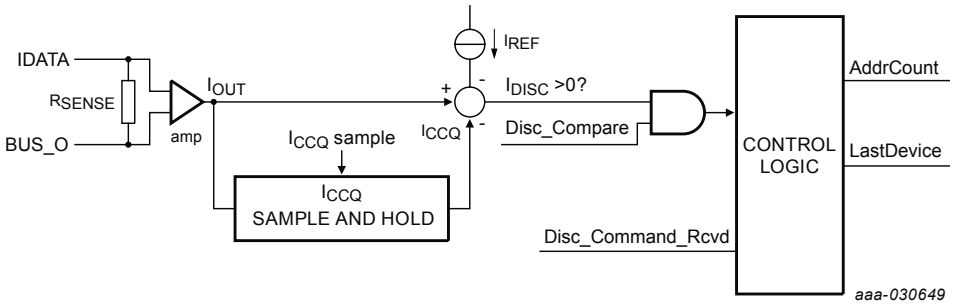
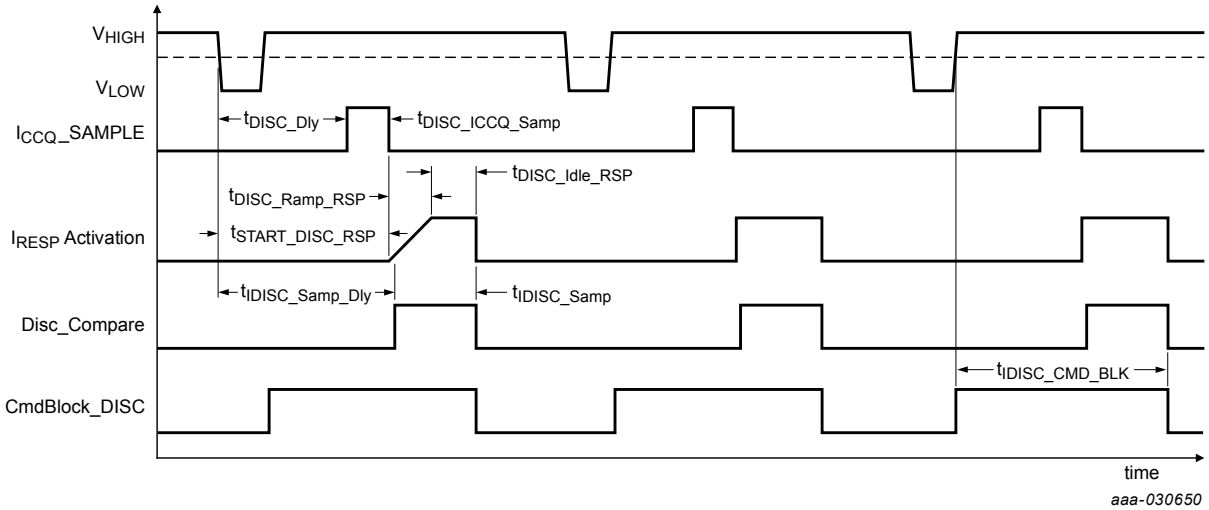



Figure 67. **DSI3 discovery mode sensing timing diagram**




## 9.2 Address assignment

The device supports all three address assignment methods described in the DSI3 [2] standard as described in Section 9.2.1: Address assignment method for parallel connected slaves, Section 9.2.2: Address assignment method for bus switch connected daisy chain devices, and Section 9.2.3: DSI3 discovery mode: Address assignment method for resistor connected daisy chain devices.

### 9.2.1 Address assignment method for parallel connected slaves

Devices connected in parallel must have pre-programmed addresses by storing a non-zero value into the PADDR[3:0] bits of the PHYSADDR OTP register. If a non-zero value is stored in this OTP register, The device does not participate in any other address assignment method and waits for Command and Response Mode for further configuration. See Section 9.3: DSI3 command and response mode for details regarding Command and Response Mode.

### 9.2.2 Address assignment method for bus switch connected daisy chain devices

A device connected in daisy chain by a bus switch may have either a pre-programmed address as described in Section 9.2.1: Address assignment method for parallel connected slaves, or an un-programmed address.

If the address is pre-programmed, the device does not participate in any other address assignment method and waits for Command and Response Mode for further configuration information, including activating the bus switch to connect the next device on the bus. See Section 9.3: DSI3 command and response mode for details regarding Command and Response Mode.

If the address is un-programmed, once power is applied, the device is the only device on the segment which requires an address assignment. The device will accept a Command and Response Mode register write command addressed to Address $0 (global command), which writes the PADDR[3:0] bits to a non-zero value. Once a physical address is assigned to the device, Command and Response Mode is used with the assigned physical address for further configuration.

On power up, the device bus switch output defaults to deactivated.

### 9.2.3 DSI3 discovery mode: Address assignment method for resistor connected daisy chain devices

A device connected in daisy chain via a resistor has an un-programmed address and uses Discovery Mode to obtain its physical address (PADDR[3:0]).

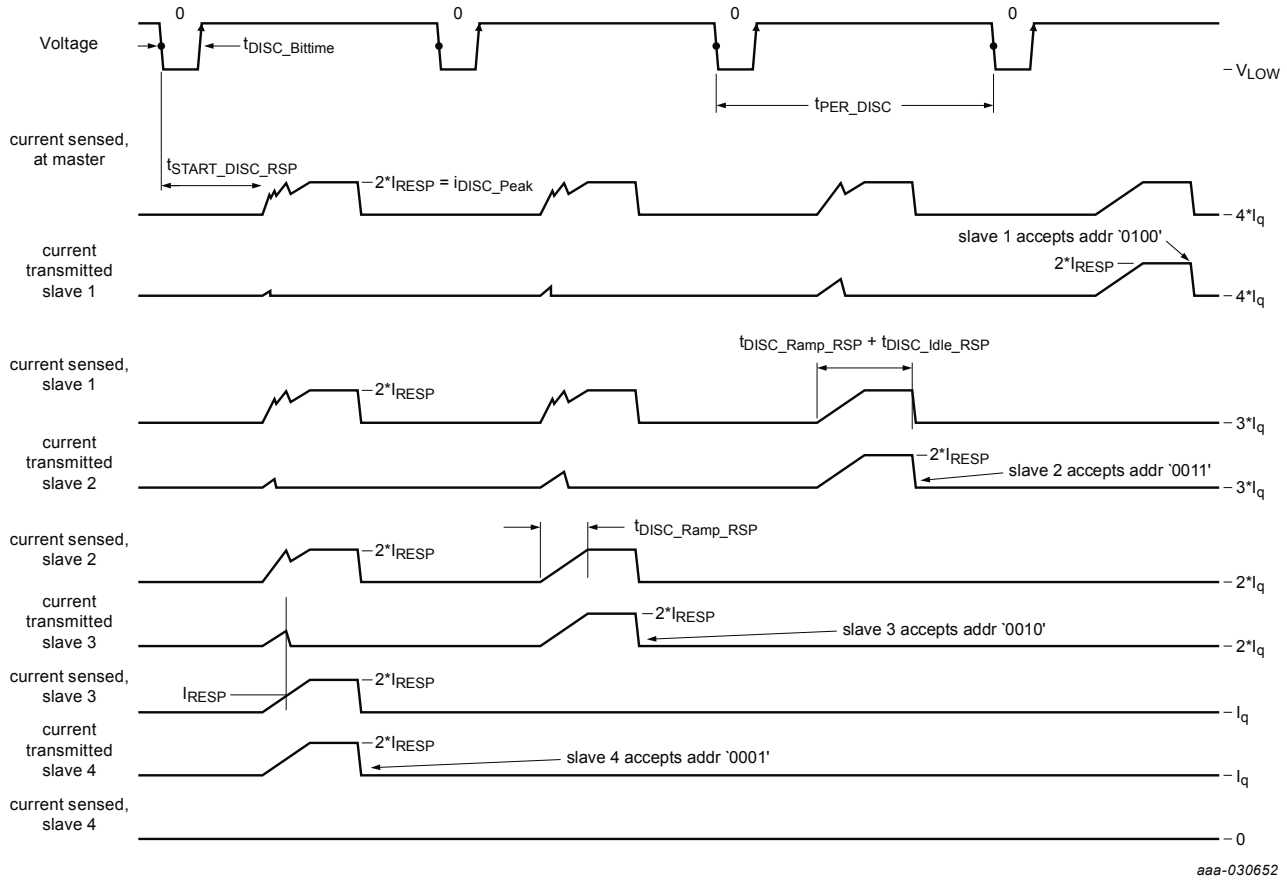
The master device must initiate Discovery Mode automatically after power is applied to the bus segment by sending a sequence of Discovery Commands. Discovery mode timing is defined in Section 7.12: Dynamic electrical characteristics - DSI3. If the ENDINIT bit is not set and the PADDR[3:0] field is set to '0000', the device will detect a Discovery Command $t_{START\_DISC}$ after a power-on reset and for intervals of $t_{PER\_Disc}$ until Discovery Mode has ended (the maximum value of $t_{START\_DISC}$).

Discovery Mode follows the sequence listed here. Figure 68. DSI3 discovery mode timing diagram shows a timing diagram of the Discover Protocol for a 4 device segment.

1. The master powers up the bus segment to a known state.
2. The master transmits the Discovery Command.
3. After a predetermined delay ($t_{START\_DISC\_RSP}$), all devices without a physical address activate a current ramp to the 2x response current at a ramp rate of $i_{DISC\_RAMP}$.
4. Each device monitors the current through its sense resistor ($\Delta i_{SENSE}$).
   a. If the current is above $i_{RESP}$, the device disables its response current, increments its physical address counter, and waits for the next Discovery Command.
   b. If the current is low ($\Delta i_{SENSE}$ less than $i_{RESP}$), the device continues to ramp its response current to 2* $i_{RESP}$ in time $t_{DISC\_RAMP\_RSP}$ and maintains the current at 2* $i_{RESP}$ for time $t_{DISC\_IDLE\_RSP}$.
   c. After time $t_{DISC\_IDLE\_RSP}$, if a device has not detected a current through its current sense resistor of iRESP, the device accepts physical address '1' and disables its response current.
5. After a pre-defined period ($t_{PER\_DISC}$), the master transmits another Discovery Command.
6. Steps 3. and 4. are repeated, with the device accepting the address in its address assignment counter if the sense current is low.
7. The master repeats step 5 until it has transmitted Discovery Commands for all the devices it expects on the bus.
8. Device initialization can now begin using Command and Response Mode.

Once the Discovery Mode is complete, a physical address is assigned to the device, and Command and Response Mode is used with the assigned physical address for further configuration.

**Figure 68. DSI3 discovery mode timing diagram**




## 9.3 DSI3 command and response mode

DSI3 command and response mode is the main communication method used for initialization of the device.

### 9.3.1 DSI3 command and response mode command reception

Command and response mode data packets are exchanged between a single master and a single slave. The primary purpose of command and response transactions are to read from and write to registers within the device memory structure.

An example command and response mode command is shown in Figure 69. Command and response mode example command. The command consists of 32 bits of data broken up into multiple fields as described in Section 9.3.1.2: Command message format.

**Figure 69. Command and response mode example command**

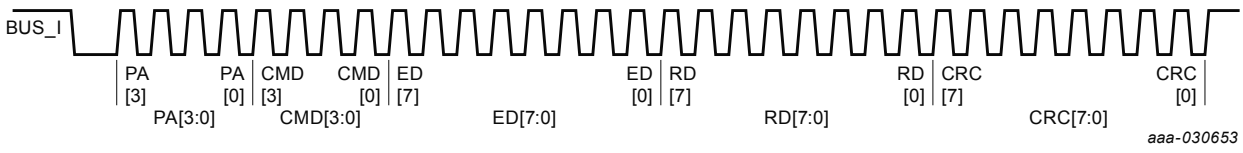


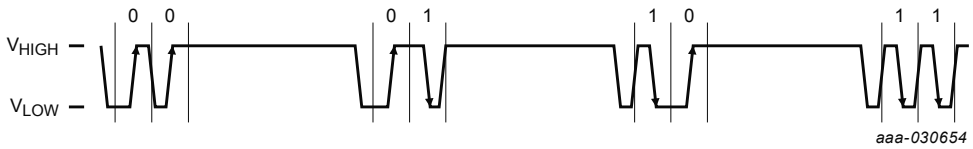

**Table 224. Command and response mode example command descriptions**

| Physical address | | | | Command | | | | Extended data | | | | | | | | Register data | | | | | | | | Error checking | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |

#### 9.3.1.1 Bit encoding

Figure 70. Command and response mode command bit encoding shows the bit encoding used for Command and Response Mode Commands from the Master device.

**Figure 70. Command and response mode command bit encoding**




#### 9.3.1.2 Command message format

The command and response mode command format is shown in Table 225. Command and response mode - command format.

**Table 225. Command and response mode - command format**

| Physical address | Command | Extended data | Register data | CRC |
|---|---|---|---|---|
| PA[3:0] | CMD[3:0] | ED[7:0] | RD[7:0] | CRC[7:0] |

**Table 226. Command and response mode - field definitions**

| Field | Length (Bits) | Definition |
|---|---|---|
| PA[3:0] | 4 | Physical Address. The physical address must match the value in the PADDR[3:0] of the PHYSADDR register |
| CMD[3:0] | 4 | Command (see Section 9.3.4: DSI3 command and response mode command summary) |
| ED[7:0] | 8 | Extended Data (see Section 9.3.4: DSI3 command and response mode command summary) |
| RD[7:0] | 8 | Register Data (see Section 9.3.4: DSI3 command and response mode command summary) |
| CRC[7:0] | 8 | Error Checking (see Section 9.3.1.3: Error checking) |

#### 9.3.1.3 Error checking

The device calculates an 8-bit CRC on the entire 32-bits of each command. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message. If the calculated CRC does not match the transmitted CRC, the command is ignored and the device does not respond.

The CRC decoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
4. If the shift register contains all zeros, the CRC is correct.
5. If the shift register contains a value other than zero, the CRC is incorrect.

The CRC polynomial and seed for Command and Response Mode are shown in Table 227. Command and response mode command CRC .

**Table 227. Command and response mode command CRC**

| Mode | Default polynomial | Non-direct seed |
|---|---|---|
| Command and Response Mode | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 |

Some example CRC calculations are shown in Table 228. Command and response mode - CRC calculation examples .

**Table 228. Command and response mode - CRC calculation examples**

| Physical address | Command | Extended data | Register data | Non-direct seed | 8-bit CRC |
|---|---|---|---|---|---|
| 0x01 | 0x08 | 0x11 | 0x86 | 0xFF | 0xB0 |
| 0x02 | 0x01 | 0x25 | 0xFF | 0xFF | 0x38 |
| 0x03 | 0x0F | 0x1A | 0x41 | 0xFF | 0x2C |
| 0x04 | 0x01 | 0x01 | 0x01 | 0xFF | 0xD4 |

### 9.3.2 DSI3 command and response mode response transmission

An example command and response mode response is shown in Figure 71. Command and response mode response example. The response consists of 32 bits of data broken up into multiple fields as described in Section 9.3.2.2: Response message format.

**Figure 71. Command and response mode response example**

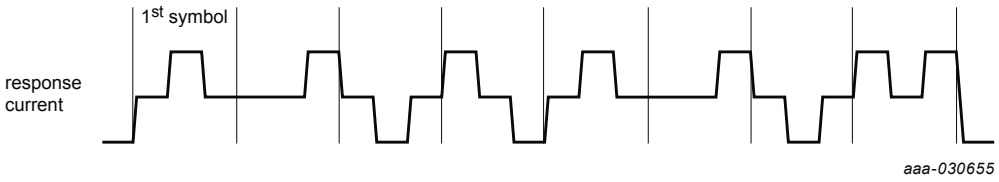


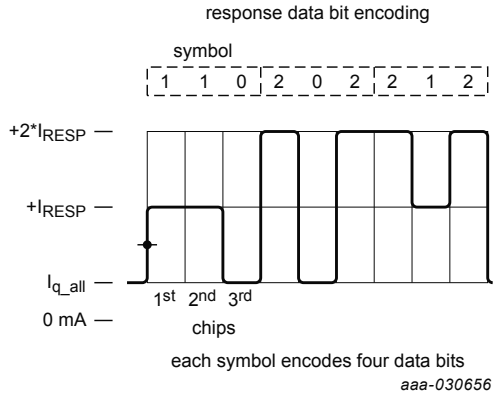

**Table 229. Command and response mode response example**

| Physical address | | | | Command | | | | Extended data | | | | | | | | Register data | | | | | | | | Error checking | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |

#### 9.3.2.1 *Symbol encoding*

The device response to a Command and Response Mode Command uses multi-level source coding where data nibbles are first encoded into symbols and then the symbols are encoded into current levels. The symbols are assembled from three consecutive three-level current pulses called chips. Within a symbol there are 3 consecutive chips that can assume one of three discrete current levels as described in Section 7.5: Electrical characteristics - temperature sensor signal chain: $i_q$, $i_q$ + $i_{RESP}$, and $i_q$ + 2 x $i_{RESP}$. Figure 72. Response symbol encoding shows the chip trans-missions and an example of a 3 symbol (9 chip), 12-bit data packet.

**Figure 72. Response symbol encoding**



Of the 27 possible combinations for three consecutive tri-level chips, the combinations that begin with the null current level ($i_q$) are discarded. Of the remaining 18 symbols, the two symbols that contain the same value for all three chips are also dis-carded. The remaining 16 symbols all begin with a non-null current level and have at least one transition. These characteristics guarantee that any response packet has a transition at the beginning of a packet and at least one transition in every symbol. Each 3-chip symbol encodes the information of 4-bits. Table 230. Symbol mapping shows the symbol encoding used by the device.

**Table 230. Symbol mapping**

| Encoded data (4 Bits) | | Symbol transmitted | | |
|---|---|---|---|---|
| Binary | HEX | 1st Chip | 2nd Chip | 3rd Chip |
| 0000 | 0 | 1 | 1 | 0 |
| 0001 | 1 | 2 | 1 | 1 |
| 0010 | 2 | 1 | 0 | 2 |
| 0011 | 3 | 2 | 0 | 2 |
| 0100 | 4 | 1 | 0 | 0 |
| 0101 | 5 | 2 | 1 | 2 |
| 0110 | 6 | 1 | 1 | 2 |
| 0111 | 7 | 2 | 0 | 1 |
| 1000 | 8 | 2 | 2 | 0 |
| 1001 | 9 | 2 | 1 | 0 |
| 1010 | A | 1 | 2 | 2 |
| 1011 | B | 2 | 2 | 1 |
| 1100 | C | 1 | 2 | 0 |
| 1101 | D | 2 | 0 | 0 |
| 1110 | E | 1 | 0 | 1 |
| 1111 | F | 1 | 2 | 1 |

Where:
0 = iq
1 = $i_{RESP}$
2 = 2 x $i_{RESP}$

### 9.3.2.2 *Response message format*

The command and response mode response format is shown in Table 231. Command and response mode - response format.

**Table 231. Command and response mode - response format**

| Physical address | Command | Register + 1 data | Register data | CRC |
|---|---|---|---|---|
| PA[3:0] | CMD[3:0] | RD1[7:0] | RD[7:0] | CRC[7:0] |

**Table 232. Command and response mode - field definitions**

| Field | Length (Bits) | Definition |
|---|---|---|
| PA[3:0] | 4 | Physical Address<br>Matches the value in the PADDR[3:0] of the PHYSADDR register |
| CMD[3:0] | 4 | An echo of the received command |
| ED[7:0] | 8 | The data contained in the register addressed by RA[7:1] + 1 (High Byte, see Section 9.3.4: DSI3 command and response mode command summary) |

| Field | Length (Bits) | Definition |
|---|---|---|
| RD[7:0] | 8 | The data contained in the register addressed by RA[7:1] + 0 (Low Byte, see Section 9.3.4: DSI3 command and response mode command summary) |
| CRC[7:0] | 8 | Error Checking (see Section 9.3.2.3: Error checking) |

#### 9.3.2.3 *Error checking*

The device calculates a CRC on the entire 32-bits of each response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC Encoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds eight zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and seed for Command and Response Mode are shown in Table 233. Command and response mode response CRC.

**Table 233. Command and response mode response CRC**

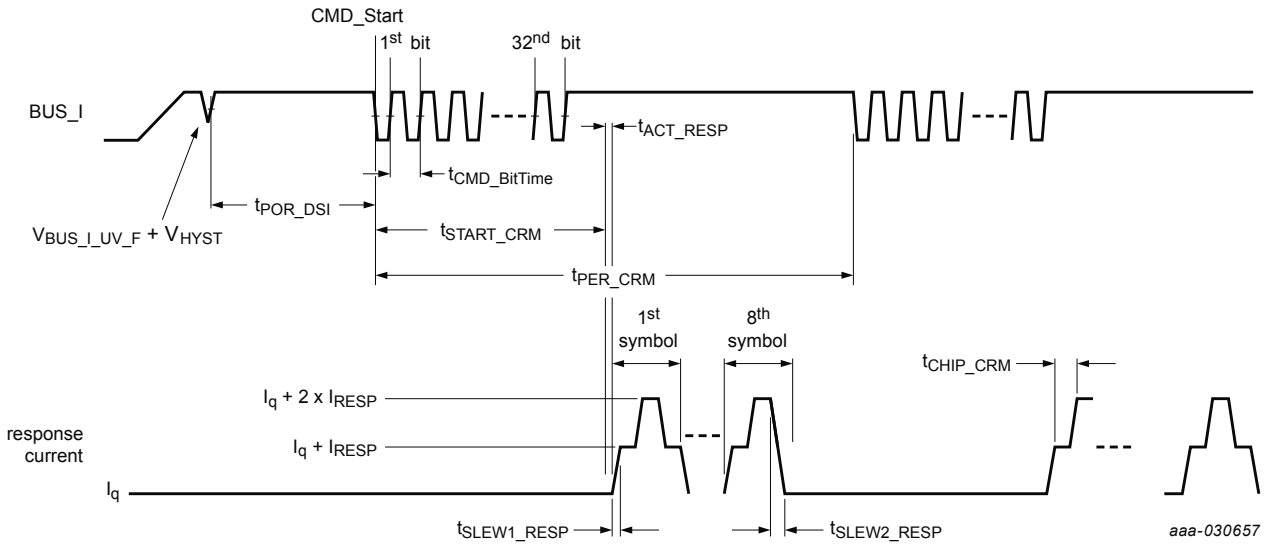
| Mode | Default polynomial | Non-direct seed |
|---|---|---|
| Command and Response Mode | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 |

Some example CRC calculations are shown in Table 228. Command and response mode - CRC calculation examples.

### 9.3.3 DSI3 command and response mode timing

A timing diagram for command and response mode is shown in Figure 73. Command and response mode timing diagram. Timing parameters are specified in Section 7.12: Dynamic electrical characteristics - DSI3.

**Figure 73. Command and response mode timing diagram**



### 9.3.4 DSI3 command and response mode command summary

**Table 234. DSI3 command and response mode command summary**

| Command | | | | | | Data | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C3 | C2 | C1 | C0 | Hex | Description | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | $0 | Register Read | RA[7] | RA[6] | RA[5] | RA[4] | RA[3] | RA[2] | RA[1] | x | x | x | x | x | x | x | x | x |
| 0 | 0 | 0 | 1 | $1 | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 0 | 0 | 1 | 0 | $2 | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 0 | 0 | 1 | 1 | $3 | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 0 | 1 | 0 | 0 | $4 | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 0 | 1 | 0 | 1 | $5 | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 0 | 1 | 1 | 0 | $6 | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 0 | 1 | 1 | 1 | $7 | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1 | 0 | 0 | 0 | $8 | Register Write | RA[7] | RA[6] | RA[5] | RA[4] | RA[3] | RA[2] | RA[1] | RA[0] | RD[7] | RD[6] | RD[5] | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] |
| 1 | 0 | 0 | 1 | $9 | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1 | 0 | 1 | 0 | $A | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1 | 0 | 1 | 1 | $B | Enter PDCM | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1 | 1 | 0 | 0 | $C | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1 | 1 | 0 | 1 | $D | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1 | 1 | 1 | 0 | $E | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1 | 1 | 1 | 1 | $F | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |

#### 9.3.4.1 *Register read command*

The device supports the Register Read command as a device address specific command only. If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register and a valid CRC is calculated, the device responds to the command.

The device ignores the Register Read command if the command is sent to any other physical address, including the DSI Global Device Address of '0000'.

The Register Read command uses the byte address definitions shown in Section 8.1: User accessible data array. The Register Read response includes the register contents at the time the Register Read command decode is complete. Readable registers along with their byte addresses are shown in Section 8.1: User accessible data array. If an attempt is made to read a register that is not readable, the device will respond with all zero data.

**Table 235. Register read command format**

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 0 | 0 | 0 | RA[7] | RA[6] | RA[5] | RA[4] | RA[3] | RA[2] | RA[1] | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 bits |

**Table 236. Register read command format description**

| Bit field | Definition |
|---|---|
| PA[3:0] | DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register. Otherwise, the command is ignored. |
| C[3:0] | Register Read Command = '0000' |
| RA[7:1] | RA[7:1] contains the upper 7 bits of the byte address for the register to be read. |

**Table 237. Register read command: response format**

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 0 | 0 | 0 | RD[15] | RD[14] | RD[13] | RD[12] | RD[11] | RD[10] | RD[9] | RD[8] | RD[7] | RD[6] | RD[5] | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] | 8 bits |

**Table 238. Register read command: response format description**

| Bit field | Definition |
|---|---|
| PA[3:0] | DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register. |
| C[3:0] | Register Read Command = '0000' |
| RD[15:8] | The data contained in the register addressed by RA[7:1] + 1 (High Byte) |
| RD[7:0] | The data contained in the register addressed by RA[7:1] + 0 (Low Byte) |

A register read command to a register address outside the addresses listed in Section 8.1: User accessible data array will result in a valid response. The data for the registers will be '0x0000'.

#### 9.3.4.2 *Register write command*

The device supports the Register Write command as a device address specific command. If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register, the device will execute the register write and respond to the command.

The device ignores the Register Write command if the command is sent to any other physical address, including the DSI Global Device Address of '0000', with one exception as explained in Section 9.3.4.3: Global register write command to the PHYSADDR register.

The Register Write command uses the byte address definitions shown in Section 8.1: User accessible data array. Writable registers along with their Byte addresses are shown in Section 8.1: User accessible data array.

**Table 239. Register write command format**

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 0 | 0 | RA[7] | RA[6] | RA[5] | RA[4] | RA[3] | RA[2] | RA[1] | RA[0] | RD[7] | RD[6] | RD[5] | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] | 8 bits |

**Table 240. Register write command format description**

| Bit field | Definition |
|---|---|
| PA[3:0] | DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register. Otherwise, the command is ignored. |
| C[3:0] | Register Write Command = 1000' |
| RA[7:0] | RA[7:0] contains the byte address of the register to be read. |
| RD[7:0] | RD[7:0] contains the data to be written to the register addressed by RA[7:0]. |

**Table 241. Register write command: response format**

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 0 | 0 | RD[15] | RD[14] | RD[13] | RD[12] | RD[11] | RD[10] | RD[9] | RD[8] | RD[7] | RD[6] | RD[5] | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] | 8 bits |

**Table 242. Register write command: response format description**

| Bit field | Definition |
|---|---|
| PA[3:0] | DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register. |
| C[3:0] | Register Write Command = '1000' |
| RD[15:8] | The data contained in the register addressed by RA[7:1] + 1 (High Byte) (after the register write is executed) |
| RD[7:0] | The data contained in the register addressed by RA[7:1] + 0 (Low Byte) (after the register write is executed) |

A register write command to a register address outside the addresses listed in Section 8.1: User accessible data array will not execute, but will result in a valid response. The data for the registers will be '0x0000'.

A register write command to a read-only register will not execute, but will result in a valid response. The data for the registers will be the current contents of the register.

### 9.3.4.3 *Global register write command to the PHYSADDR register*

The device supports the Register Write command as a global address under the following conditions:

1. The Register Write command is written to the PHYSADDR register.
2. The PADDR[3:0] bits of the PHYSADDR register are equal to '0000' prior to the register write being executed.

If these conditions are met, the device will execute the register write and respond to the command.

**Table 243. Global register write command format**

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | RD[3] | RD[2] | RD[1] | RD[0] | 8 bits |

**Table 244. Global register write command format description**

| Bit field | Definition |
|---|---|
| PA[3:0] | The DSI Global address of '0000'. |
| C[3:0] | Register Write Command = '1000' |
| RA[7:0] | RA[7:0] must be set to the PHYSADDR register address. |
| RD[3:0] | RD[3:0] contains the new physical address for the device. |

**Table 245. Global register write command: response format**

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 0 | 0 | RD[15] | RD[14] | RD[13] | RD[12] | RD[11] | RD[10] | RD[9] | RD[8] | RD[7] | RD[6] | RD[5] | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] | 8 bits |

**Table 246. Global register write command: response format description**

| Bit field | Definition |
|---|---|
| PA[3:0] | The new DSI physical address programmed to the PADDR[3:0] bits in the PHYSADDR register. |
| C[3:0] | Register Write Command = '1000' |
| RD[15:8] | The data contained in register after PHYSADDR |
| RD[7:0] | The data contained in the PHYSADDR register after the register write is executed. |

### 9.3.4.4 *Enter periodic data collection mode command*

The device supports an Enter PDCM command as a device address specific command and as a Global Command.

If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register, the device will set the ENDINIT bit in the DEVLOCK_WR register, enter Periodic Data Collection Mode, and respond to the command as shown in Table 250. Enter periodic data collection mode command: response format. If the PA[3:0] field in the command matches the Global address of '0000', the device will set the ENDINIT bit in the DEVLOCK_RW register and enter Periodic Data Collection Mode regardless of the value of the PADDR[3:0] bits in the PHYSADDR register (this includes PADDR = 0x0). No response is transmitted for a global command. The device ignores the Enter PDCM command if the command is sent to any other physical address.

The various DSI3 communication modes are controlled by the PDCM enable command and the BDM_EN bit in the TIMING_CFG2 register as shown in Table 247. PDCM enable command and BDM_EN bit status.

**Table 247. PDCM enable command and BDM_EN bit status**

| PDCM Enabled? | BDM_EN | Command and Response Mode | Periodic Data Collection Mode | Background Diagnostic Mode |
|---|---|---|---|---|
| No | 0 | Enabled | Disabled | Disabled |
| No | 1 | Enabled | Disabled | Disabled |
| Yes | 0 | Disabled | Enabled | Disabled |
| Yes | 1 | Disabled | Enabled | Enabled |

Once the ENDINIT bit is set, the registers listed in Section 8.3.3: OTP modifiable registers are locked and the user array read/write register array verification is enabled. The ENDINIT bit can only be cleared by a device reset.

**Table 248. Enter periodic data collection mode command format**

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 bits |

**Table 249. Enter periodic data collection mode command format description**

| Bit field | Definition |
|---|---|
| PA[3:0] | DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register or the Global Address of '0000'. Otherwise, the command is ignored. |
| C[3:0] | Enter PDCM Command = '1011' |

**Table 250. Enter periodic data collection mode command: response format**

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Ch[3] | Ch[2] | Ch[1] | Ch[0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 bits |

**Table 251. Enter periodic data collection mode command: response format description**

| Bit field | Definition |
|---|---|
| PA[3:0] | DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register. |
| Ch[3:0] | CHIPTIME[3:0] in the CHIPTIME register |
| C[3:0] | Enter Periodic Data Collection Mode Command = '1011' |

### 9.3.4.5 *Reserved commands*

If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register and a valid CRC is calculated, the device will respond to reserved commands. The physical address and command will be echoed and the correct CRC are transmitted. The data included in the response is undefined.

**Table 252. Reserved commands**

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 0 | 1 | 1 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 1 | 0 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 1 | 0 | 1 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 1 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 1 | 1 | 1 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 1 | 0 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 1 | 0 | 1 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 1 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 1 | 1 | 1 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |

**Table 253. Reserved commands description**

| Bit field | Definition |
|---|---|
| PA[3:0] | DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register. Otherwise, the command is ignored. |
| C[3:0] | Invalid Commands |
| x | Don't Care |

**Table 254. Reserved command response format**

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | C[3] | C[2] | C[1] | C[0] | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8 bits |

**Table 255. Reserved command response format description**

| Bit field | Definition |
|---|---|
| PA[3:0] | DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register. |
| C[3:0] | Reserved Command Echo |

## 9.4 DSI3 periodic data collection mode and background diagnostic mode

When the ENDINIT bit in the DEVLOCK_WR register is set, periodic data collection mode is enabled and the optional background diagnostic mode is enabled.

### 9.4.1 DSI3 periodic data collection mode and background diagnostic mode command reception

When periodic data collection mode is enabled, the device will decode the DSI3 broadcast read command as well as background diagnostic mode command fragments as described below.

#### *9.4.1.1 Bit encoding*

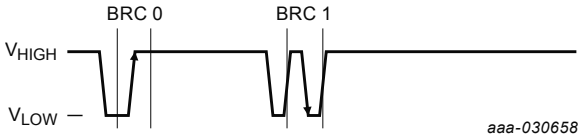
The Command Bit encoding for Periodic Data Collection Mode and Background Diagnostic Mode is the same as the bit encoding for Command and Response Mode, as described in Section 9.3.1.1: Bit encoding.

#### *9.4.1.2 Command message format*

The command message format for Periodic Data Collection Mode and Background Diagnostic Mode is the same as the command message format for Command and Response Mode, as described in Section 9.3.1.2: Command message format.

If Background Diagnostic Mode is disabled, then the device responds with the Periodic Data Collection Mode response only if the command is the single bit Broadcast Read Command. A Broadcast Read Command may be either a '1' or a '0'. Figure 74. Background diagnostic mode command bit encoding shows the Broadcast Read Commands supported by the device.

**Figure 74. Background diagnostic mode command bit encoding**




If Background Diagnostic Mode is enabled:

- Background Diagnostic Mode commands are transmitted and decoded in 2- or 4-bit fragments depending on the state of the BDM_FRAGSIZE bit in the TIMING_CFG2 register.
- The device responds with the Periodic Data Collection Mode response if and only if the command is a Broadcast Read Command or a command fragment.
- A Broadcast Read Command or any command length other than 2 or 4 bits resets the Background Diagnostic Mode command decode.
- The device responds with a Background Diagnostic Mode response only when a full 32-bit command is received and the decoded command is a valid Command and Response Mode command.

See Section 9.4.4: Background diagnostic mode response transmission for additional details on Background Diagnostic Mode timing.

#### 9.4.1.3 *Error checking*

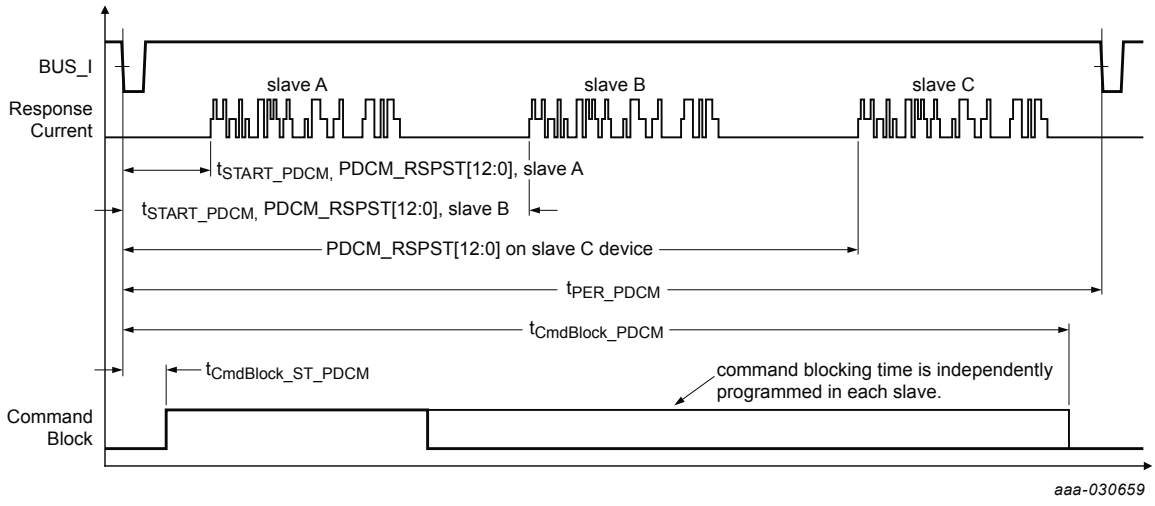
The error checking for Background Diagnostic Mode commands is the same as the error checking for Command and Response Mode, and described in Section 9.3.1.3: Error checking.

No error checking is employed for the Broadcast Read Commands.

### 9.4.2 DSI3 periodic data collection mode response transmission

When periodic data collection mode is enabled and the device receives either a broadcast read or background diagnostic command, the device will respond with periodic data as shown in Figure 75. Periodic data mode response transmission and described in the following sections.

**Figure 75. Periodic data mode response transmission**




#### 9.4.2.1 *Symbol encoding*

The symbol encoding used for Periodic Data Collection Mode Responses is the same as for Command and Response Mode responses, and described in Section 9.3.2.1: Symbol encoding.

#### 9.4.2.2 *Response message format*

The Periodic Data Collection Mode response format is shown in Table 256. Periodic data collection mode response format and Table 257. Periodic data collection mode status field definition. Field sizes are defined by the PDCMFORMAT[2:0] bits in the SOURCEID_x register in Section 8.2.13: Source identification registers (SOURCEID_x).

**Table 256. Periodic data collection mode response format**

| Source ID | Keep alive counter | Status | Sensor data | CRC |
|---|---|---|---|---|
| SOURCEID | KAC | S | D | CRC[7:0] |

- If enabled in the PDCMFORMAT[2:0] bits, the SOURCEID field includes the value stored in the SOURCEID_x[3:0] bits of the SOURCEID_x register.
- If enabled in the PDCMFORMAT[2:0] bits, the Keep Alive Counter field is a 2-bit rolling message counter that is independently incremented for each SOURCEID. The initial value of the counter is '00'.
- If enabled, the status field is transmitted as listed in Table 257. Periodic data collection mode status field definition. See Section 9.7: DSI3 exception handling for details on exception handling.
- The Sensor Data field includes the sensor data as selected by the DATATYPEx bits for the SOURCEID.
- The CRC field includes an 8-bit CRC as defined in Section 9.4.2.3: Error checking.

**Table 257. Periodic data collection mode status field definition**

| s[3:0] | | | | Description | DEVSTAT state | SUP_ER-R_DIS state | Error priority | Sensor data field value | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | STATUS field size = 4 | STATUS field size = 0 |
| 0 | 0 | 0 | 0 | Normal Mode | N/A | N/A | 16 | Sensor Data | |
| 0 | 0 | 0 | 1 | Normal Mode, User Array Not Locked<br>(UF2 region has not been locked) | N/A | N/A | 15 | Sensor Data | The Sensor Data Field Error Code is transmitted for a minimum of one transmission |
| 0 | 0 | 1 | 0 | Self-test Incomplete or Self-test Active or Self-test Error Present | Bit set in CHx_STAT:<br>ST_INCMPLT or ST_ACTIVE or ST_ERROR | N/A | 14 | Sensor Data | The Sensor Data Field Error Code is transmitted for a minimum of one transmission |
| 0 | 0 | 1 | 1 | Oscillator Training Error | Bit set in DEVSTAT3 | N/A | 13 | Sensor Data | The Sensor Data Field Error Code is transmitted for a minimum of one transmission |
| 0 | 1 | 0 | 0 | Offset Error | Bit set in CHx_STAT:<br>SIGNALCLIP or OFFSET_ERR | N/A | 12 | Sensor Data | The Sensor Data Field Error Code is transmitted for a minimum of one transmission |
| 0 | 1 | 0 | 1 | Temperature Error | Bit set in DEVSTAT2 | N/A | 11 | Sensor Data | The Sensor Data Field Error Code is transmitted for a minimum of one transmission |
| 0110 to 0111 | | | | RESERVED | N/A | N/A | 9.10 | Sensor Data | The Sensor Data Field Error Code is transmitted for a minimum of one transmission |
| 1 | 0 | 0 | 0 | User OTP Memory Error (UF2) | U_OTP_ERR set in DEVSTAT2 | N/A | 8 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | |
| 1 | 0 | 0 | 1 | User R/W Memory Error (UF2) | U_RW_ERR set in DEVSTAT2 | N/A | 7 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | |
| 1 | 0 | 1 | 0 | ST OTP Memory Error | F_OTP_ERR set in DEVSTAT2 | N/A | 6 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | |
| 1 | 0 | 1 | 1 | Test Mode Active | TESTMODE bit set in DEVSTAT | N/A | 5 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | |
| 1 | 1 | 0 | 0 | Supply Error | Bit set in DEVSTAT1 | 0 | 4 | No Response until the supply monitor timer expires<br>The Sensor Data Field Error Code is transmitted for a minimum of one transmission<br>(See Section 8.2.2.5: Supply error flag (SUPPLY_ERR)) | |
| | | | | | | 1 | | No Response until the supply monitor timer expires<br>(See Section 8.2.2.5: Supply error flag (SUPPLY_ERR)) | |
| 1 | 1 | 0 | 1 | Reset Error | DEVRES Set | N/A | 3 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | |
| 1110 to 1111 | | | | RESERVED | N/A | N/A | 1, 2 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | |

#### 9.4.2.3 *Error checking*

The device calculates a CRC on the entire response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC Encoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds eight zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and seed for periodic data collection mode are shown in Table 258. Periodic data collection mode response CRC.

**Table 258. Periodic data collection mode response CRC**

| Mode | Default polynomial | Non-direct seed |
|---|---|---|
| Periodic Data Collection Mode | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 0000, SOURCEID_x[3:0] |

Some example CRC calculations are shown in Table 259. Periodic data collection mode - CRC calculation examples.

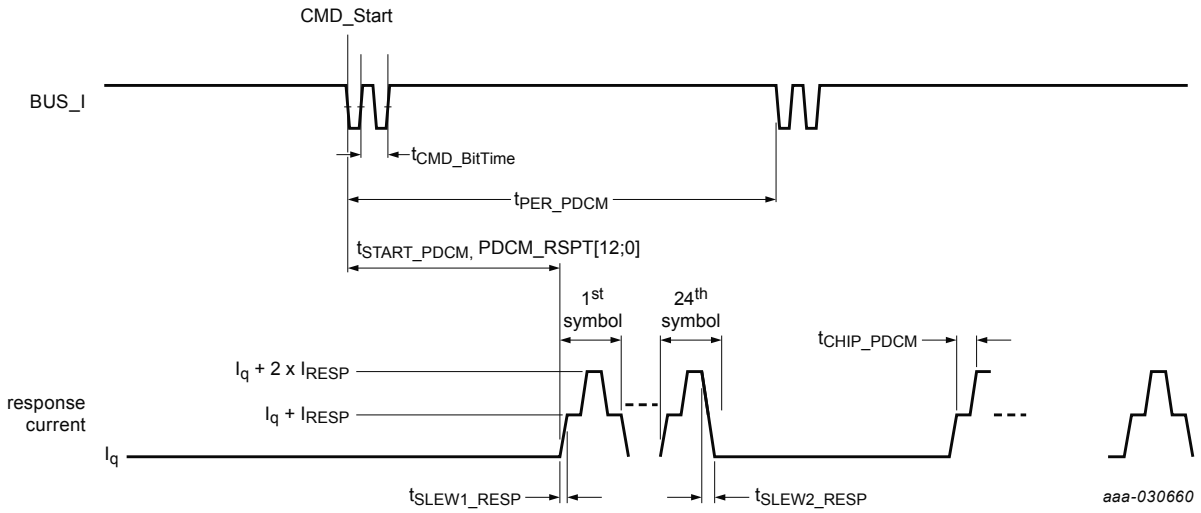
**Table 259. Periodic data collection mode - CRC calculation examples**

| Source identification (4 Bits) | Keep alive counter (2 Bits) | Status (4 Bits) | Sensor data (10 Bits) | Non-direct seed | 8-bit CRC |
|---|---|---|---|---|---|
| 0x1 | 0x3 | 0x0 | 0x1FF | 0x01 | 0xD6 |
| 0x2 | 0x2 | 0x0 | 0x1FE | 0x02 | 0x70 |
| 0x3 | 0x1 | 0x0 | 0x20D | 0x03 | 0xB0 |
| 0x4 | 0x0 | 0x0 | 0x1EA | 0x04 | 0x5F |

### 9.4.3 DSI3 periodic data collection mode timing

A timing diagram for periodic data collection mode is shown in Figure 76. Periodic data collection mode timing diagram. Timing parameters are specified in Section 7.12: Dynamic electrical characteristics - DSI3.

**Figure 76. Periodic data collection mode timing diagram**



### 9.4.4 Background diagnostic mode response transmission

#### *9.4.4.1 Symbol encoding*

The Background Diagnostic Mode response symbol encoding is the same as the symbol encoding used for Command and Response Mode responses and is described in Section 9.3.2.1: Symbol encoding.

#### *9.4.4.2 Response message format*

The Background Diagnostic Mode response message format is the same as the format used for Command and Response Mode responses and is described in Section 9.3.2.2: Response message format.

- If a complete 32-bit command is received and decoded to a valid Command and Response Mode command, the device provides a Background Diagnostic Mode response.
- Responses are initiated by the master transmitting 1-bit Broadcast Read Commands following a completed Background Diagnostic Mode command transmission.
- Responses are transmitted in one or two symbol fragments (depending on the state of the BDM_FRAGSIZE bit) following the 1-bit Broadcast Read Command, using the same timing window within the frame that the Background Diagnostic Mode Command used.
- Responses are transmitted if and only if Broadcast Read Commands are received.
- Four or eight consecutive Broadcast Read Commands are required following a valid Background Diagnostic Mode command to complete a response transmission (depending on the state of the BDM_FRAGSIZE bit).
- If any command other than the Broadcast Read Command is received, no response is transmitted and the remainder of the Broadcast Read Command response is terminated.
- The data to be transmitted in the response is latched just before the first symbol of the background diagnostic mode response.

See Figure 77. Background diagnostic mode timing diagram for Background Diagnostic Mode timing.

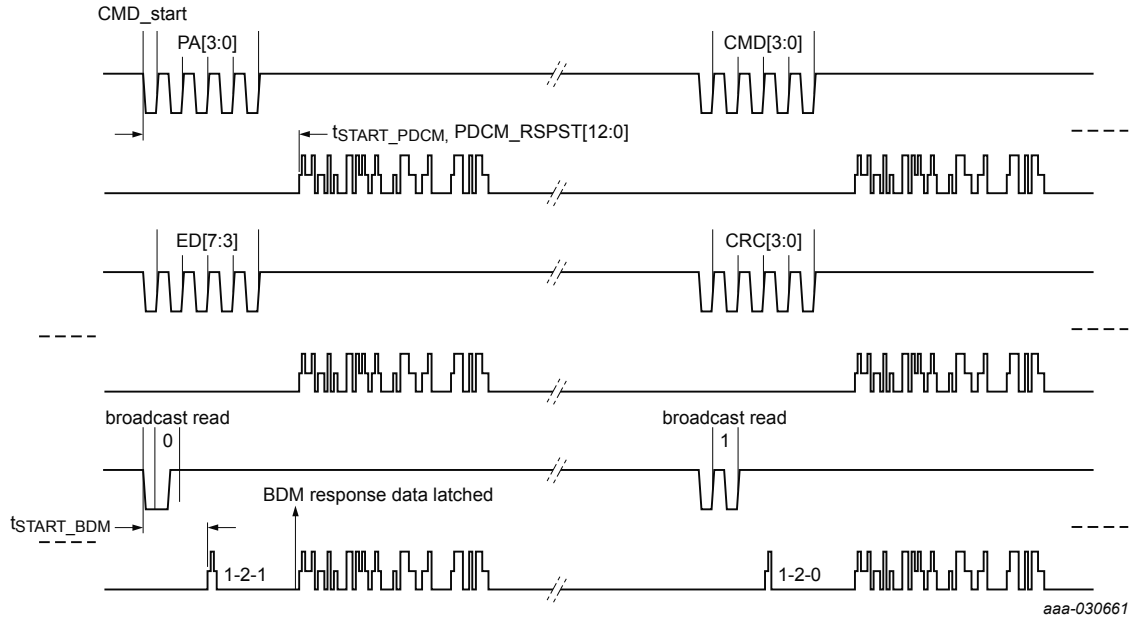
#### *9.4.4.3 Error checking*

The error checking for Background Diagnostic Mode responses is the same as used for Command and Response Mode, and described in Section 9.3.1.3: Error checking.

### 9.4.5 DSI3 background diagnostic mode timing

An example timing diagram for background diagnostic mode is shown in Figure 77. Background diagnostic mode timing diagram. In this example, BDM_FRAGSIZE is set to '1' (4 bits). Timing parameters are specified in Section 7.12: Dynamic electrical characteristics - DSI3.

Figure 77. **Background diagnostic mode timing diagram**



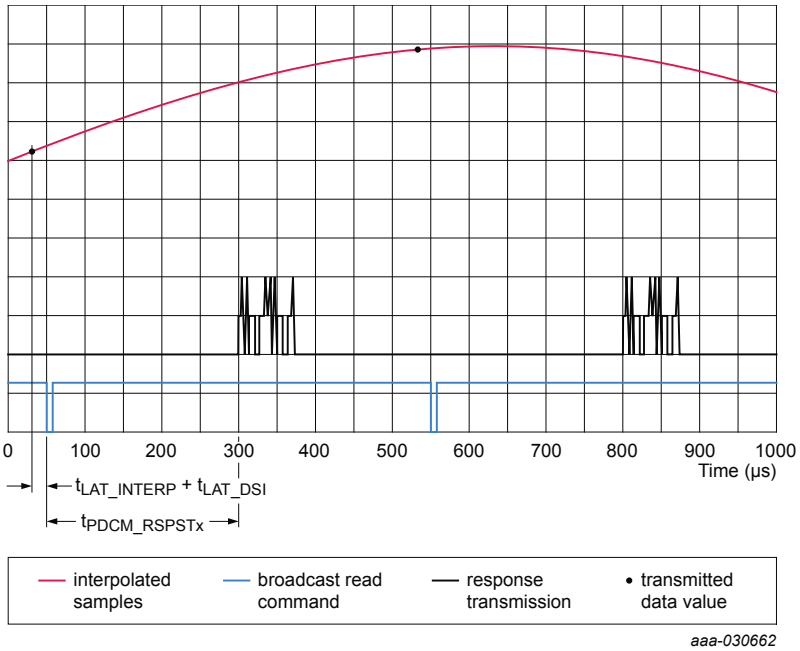

### 9.4.6 DSI3 periodic data collection mode and background diagnostic mode command summary

When periodic data collection mode is enabled, the background diagnostic mode supports the register read command as described in the command and response mode command summary, Section 9.3.4.1: Register read command. The register write command is not supported in background diagnostic mode.

### 9.4.7 DSI3 PDCM data transmission modes

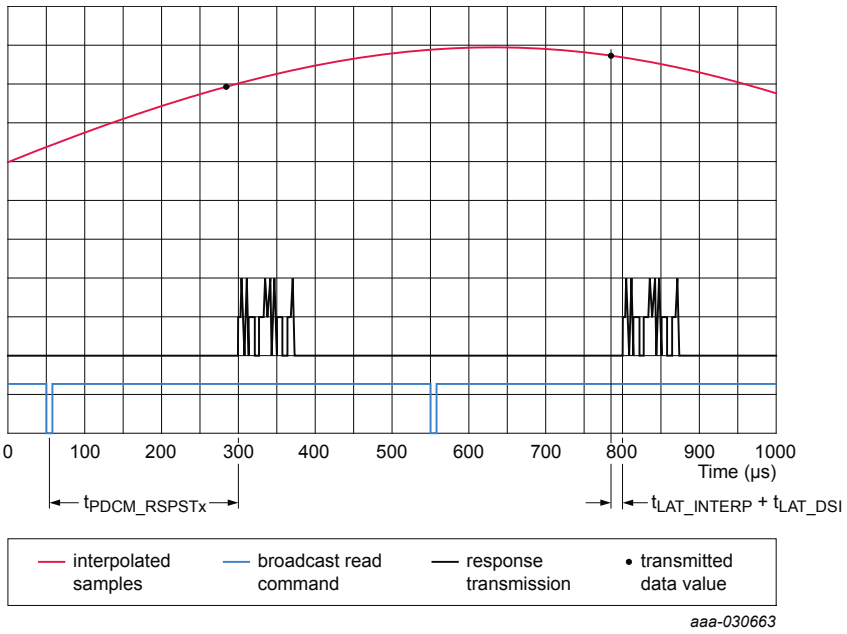
#### *9.4.7.1 Simultaneous sampling mode (SS_EN = 1)*

Figure 78. **Simultaneous sampling mode**



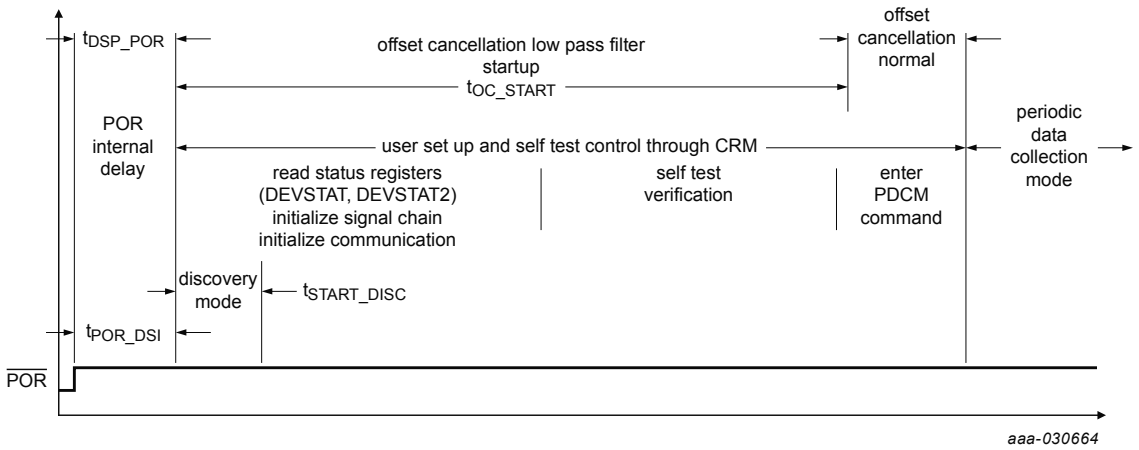
#### 9.4.7.2 *Synchronous sampling mode with minimum latency (SS_EN = 0)*

**Figure 79. Synchronous sampling mode with minimum latency**




## 9.5 Initialization timing

**Figure 80. Initialization timing**




## 9.6 Maximum number of devices on a network

The theoretical maximum number of devices on a DSI3 network is 16: 1 master and 15 slaves. The practical limit for the number of devices on a bus is dependent on the minimum common capability of the devices on the bus. The capability of the device is different depending on the bus configuration and operating mode. The impact of the device capability on the practical limit for the number of devices on the network is described in this section.

### 9.6.1 Pre-configured, parallel connected network

The number of devices in a pre-configured, parallel connected network is not directly limited by the capability of the device. The practical limit is determined by a combination of the following:

- The capability of the master device, including, but not limited to:
  - The bus operating voltage
  - The bus supply current
  - The bus current limit
  - The bit rate
  - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.

### 9.6.2 Bus switch connected daisy chain network

The number of devices in a bus switch connected daisy chain network is not directly limited by the capability of the device. The practical limit is determined by a combination of the following:

- The capability of the master device, including, but not limited to:
  - The bus operating voltage
  - The bus supply current
  - The bus current limit
  - The bit rate
  - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.
- The current handling capability and resulting voltage drop of the external bus switches in the network.

### 9.6.3 Resistor connected daisy chain network using discovery mode

The number of devices in a resistor connected daisy chain network is limited by the capability of the device. The maximum number of equivalent devices connected to the BUS_O pin of a device is 3. This is limited by the total quiescent current drawn from the BUS_O pin during Discovery Mode ($I_{BUS\_O\_q}$).

The practical limit is determined by a combination of the above restriction and the following:

- The capability of the master device, including, but not limited to:
  - The bus operating voltage
  - The bus supply current
  - The bus current limit
  - The bit rate
  - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.
- The maximum allowed quiescent current drawn from the BUS_O pin of other slaves in the system.
- The resulting voltage drop of the Discovery Mode resistors in all slaves in the network.

## 9.7 DSI3 exception handling

Table 260. Exception conditions and response summarizes the exception conditions detected by the device and the response for each exception.

**Table 260. Exception conditions and response**

| Condition | | Description | Device response |
|---|---|---|---|
| exception | PDCM enabled? | | |
| Power-On Reset | N/A | Power Applied | • See Section 9.5: Initialization timing<br>• ST_INCMPLT set, PDCM disabled. The device must be reinitialized |
| $V_{BUS\_I}$ Error | N/A | $V_{BUS\_I} < V_{BUS\_I\_UV\_F}$ | • Response Current Deactivated<br>• BUSIN_UV_ERR set, PDCM Status set as specified in Section 9.4.2.2: Response message format<br>• The device ignores commands in CRM |

| Condition | | Description | Device response |
|---|---|---|---|
| exception | PDCM enabled? | | |
| $V_{BUF}$ Error | N/A | $V_{BUF} < V_{BUF\_UV\_F}$ | • Response Current Deactivated<br>• VBUFUV_ERR set, PDCM Status set as specified in Section 9.4.2.2: Response message format<br>• The device ignores commands in CRM |
| Internal Regulator Error | N/A | Internal regulator under-voltage condition | • The device is held in Reset<br>• No response to DSI commands<br>• If activated, BUSSW_L is deactivated<br>• The device must be reinitialized when the internal regulator returns above the threshold |
| OTP Error Detection Fault<br>(Factory Array) | N/A | Error detected in factory programmed OTP array. | • Periodic Data Collection Mode response data set to error response<br>• F_OTP_ERR set, PDCM Status set as specified in Section 9.4.2.2: Response message format |
| OTP Error Detection Fault<br>(User Array) | N/A | Error detected in User programmed OTP array and the LOCK_U bit is set. | • Periodic Data Collection Mode response data set to error response<br>• U_OTP_ERR set, PDCM Status set as specified in Section 9.4.2.2: Response message format |
| User R/W Array Error Detection Fault | No | N/A | N/A |
| | Yes | Error detected in user read write registers and the ENDINIT bit is set. | • Periodic Data Collection Mode response data set to error response<br>• U_RW_ERR set, PDCM Status set as specified in Section 9.4.2.2: Response message format |
| Self-test Activated | No | ST activated during initialization | • Internal self-test circuitry enabled<br>• Self-test Activation Incomplete status cleared<br>• Sensor Data Registers (SNSDATAx_x) contain self-test active data<br>• ST_ACTIVE set |
| | Yes | ST activated in Periodic Data Collection Mode | • Periodic Data Collection Mode sensor response data normal<br>• Self-test Activation ignored |
| Self-test Never Activated after Reset | No | In initialization, before Self-test | • Normal Responses to Command and Response Mode |
| | Yes | In PDCM, Self-test incomplete | • Periodic Data Collection Mode sensor response data normal<br>• ST_INCMPLT set, PDCM Status set as specified in Section 9.4.2.2: Response message format |

### 9.7.1 Daisy chain and discovery mode error handling

Table 261. DSI3 error handling - discovery mode and daisy chain mode shows the effect of internal failure modes on the discovery and daisy chain initialization procedures.

**Table 261. DSI3 error handling - discovery mode and daisy chain mode**

| Error condition | Effect on discovery mode | Effect on daisy chain |
|---|---|---|
| Supply Error | Discovery Commands Ignored. The device does not participate in Discovery Mode | Daisy Chain Commands Ignored. The device will not participate in Daisy Chain |
| Memory Error | No Effect. The device attempts to participate in Discovery Mode as programmed. | No Effect. The device will attempt to participate in Daisy Chain as programmed. |
| Temperature Error | No Effect. The device will attempt to participate in Discovery Mode as programmed. | No Effect. The device will attempt to participate in Daisy Chain as programmed. |
| Communication Error (Internal) | No Effect. The device participates in Discovery Mode as programmed. | No Effect. The device will participate in Daisy Chain as programmed. |
| Offset Error | No Effect. The device will participate in Discovery Mode as programmed. | No Effect. The device will participate in Daisy Chain as programmed. |

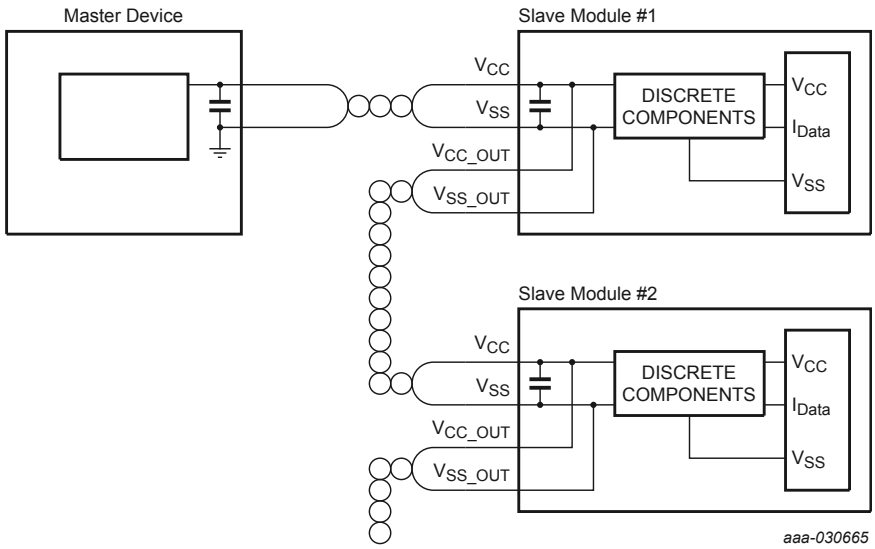
| Error condition | Effect on discovery mode | Effect on daisy chain |
|---|---|---|
| Self-test Incomplete or Self-test Active | Not Applicable. | Not Applicable. |
| Device Not Locked | No Effect. The device will participate in Discovery Mode as programmed. | No Effect. The device will participate in Daisy Chain as programmed. |

# 10 PSI5 protocol

## 10.1 Communication interface overview

The communication interface between a master device and this slave device in PSI5 mode is established via a PSI5 compatible 2-wire interface, with parallel or serial (daisy-chain) connections to the satellite modules. Figure 81. PSI5 satellite interface diagram shows one possible system configuration for multiple satellite modules in parallel.

**Figure 81. PSI5 satellite interface diagram**



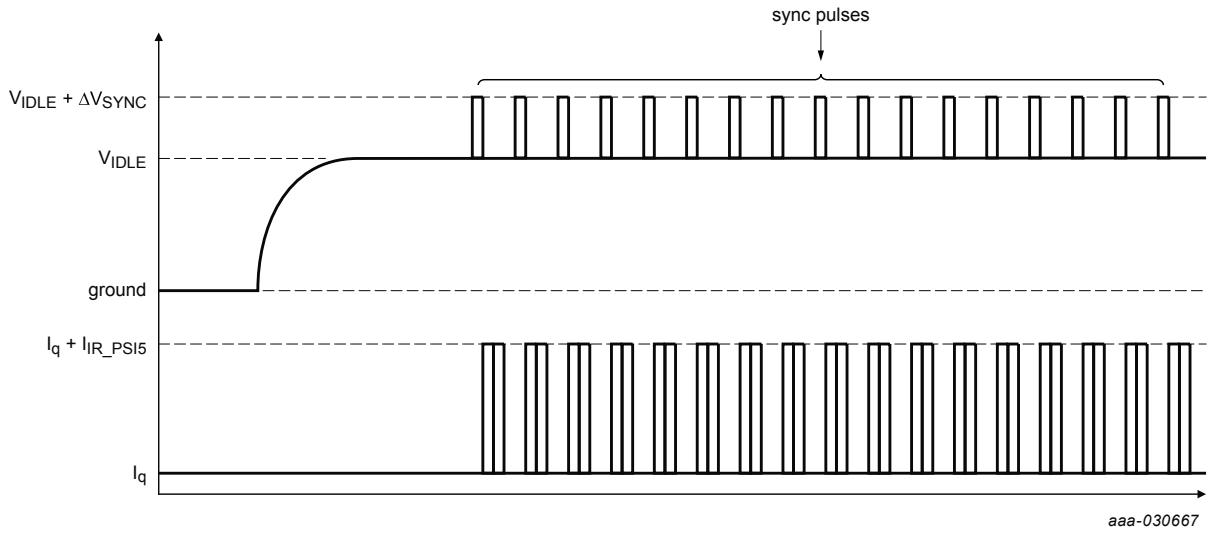

## 10.2 Data transmission physical layer

This device uses a two wire interface for both its power supply ($V_{CC}$), and data transmission (IDATA). The PSI5 master sup-plies a pre-regulated voltage to this device. Data transmissions and synchronization control from the PSI5 master to this device are accomplished via modulation of the supply voltage. Data transmissions from this device to the PSI5 master are accomplished via modulation of the current on the power supply line.

### 10.2.1 Synchronization pulse

The PSI5 master modulates the supply voltage in the positive direction to provide synchronization of the satellite sensor data. Upon reception of a synchronization pulse, this device delays a specified period of time, called a time slot, before transmitting sensor data. For more details regarding time slots, refer to Section 8.2.18: DSI3 and PSI5 start time registers (PDCM_RSPSTx_x), and Section 7.13: Dynamic electrical characteristics - PSI5.

**Figure 82. Synchronous communication overview**

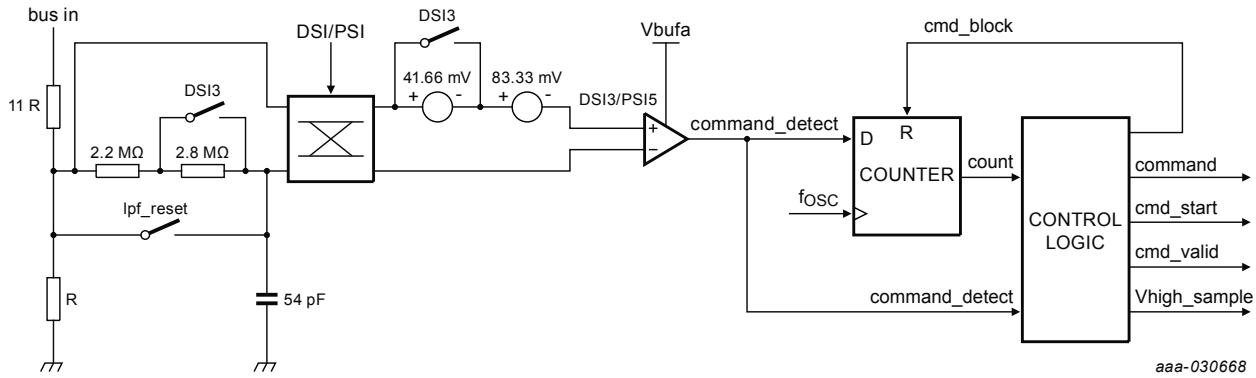



### 10.2.1.1 *Synchronization pulse detection*

The Synchronization (Sync) pulse detection block generates a valid synchronization pulse signal following the detection of an externally generated Sync pulse. This signal resets the Sync pulse time reference ($t_{TRIG}$), and initiates the timers associated with response messages.

The supply voltage can vary throughout the specified range, so the external Sync pulses may have different absolute volt-age levels. Thus, the Sync pulse detection threshold ($V_{CC\_SYNC}$) is dependent not only on the Sync pulse absolute voltage, but also on the supply voltage. Figure 83. Synchronization pulse detection circuit shows a block diagram of the Sync pulse detection circuit.

**Figure 83. Synchronization pulse detection circuit**




The start of a Sync pulse is detected when the comparator output is set. The comparator output is input into a counter, and the counter is updated at a fixed frequency. At a fixed time after the initial sync pulse detection, the counter is compared against a limit (the minimum value of $t_{SYNC}$). If the counter is above the limit, a valid sync pulse is detected.

If the Sync pulse is valid, the following occur:

1. The valid Sync pulse detection signal is set.
2. The detection counter is reset and disabled for $t_{SYNC\_OFF}$ (referenced from $t_{TRIG}$). $t_{SYNC\_OFF}$ can be programmed by the user via the PDCM_CMD_B_x registers. See Section 8.2.19: DSI3 and PSI5 command blocking time registers (PDCM_CMD_B_x) for details on the programmable option, and Section 7.13: Dynamic electrical characteristics - PSI5 for timing specifications for each option.
3. The Sync pulse detection low-pass filter is reset for a specified time ($t_{SYNC\_LPF\_RESET}$).

If the Sync pulse is invalid, all timers are reset, and the detector becomes sensitive within 2 µs.

The output of the comparator is monitored at the SampCLK frequency. Once the comparator output goes high, all of the internal timers are started, so that the $t_{TRIG}$ jitter is minimized.

**Figure 84. Synchronization pulse detection timing**

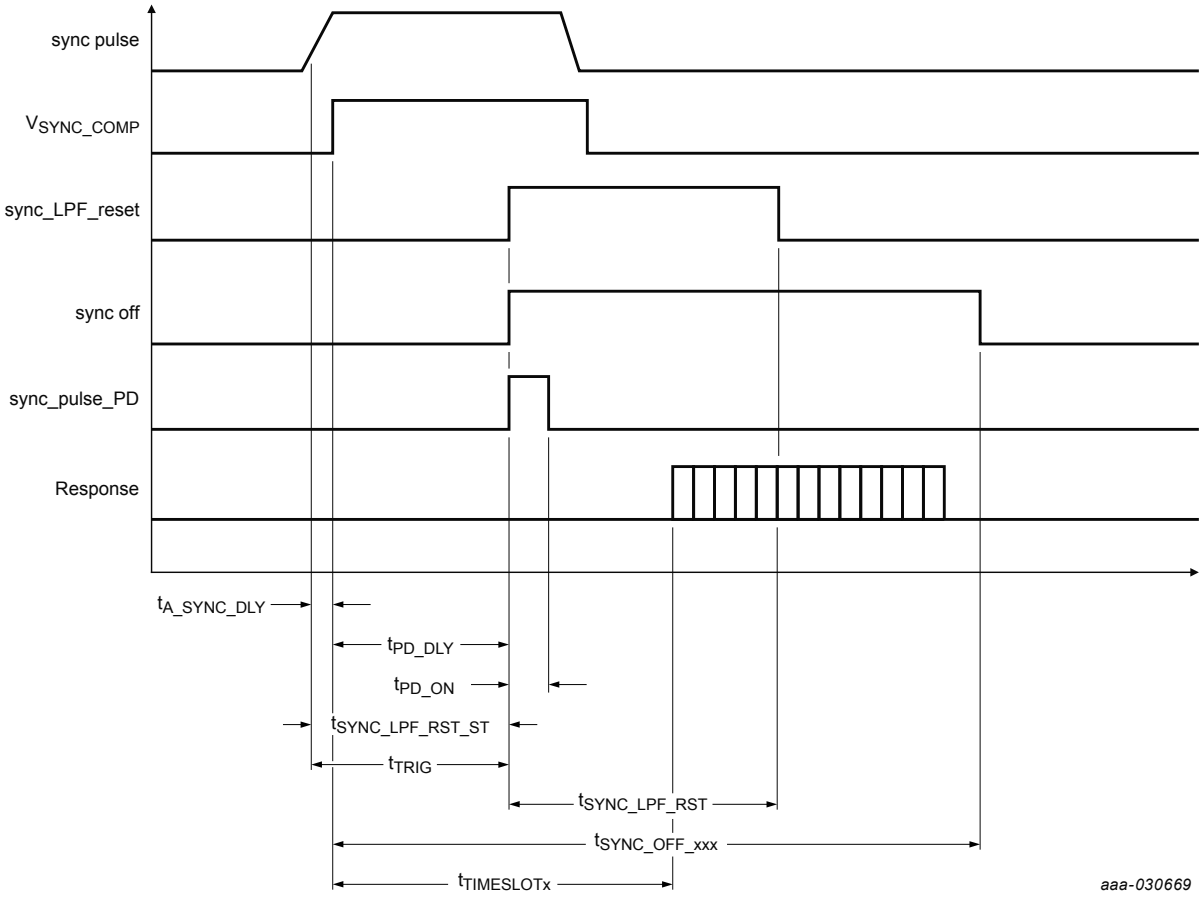
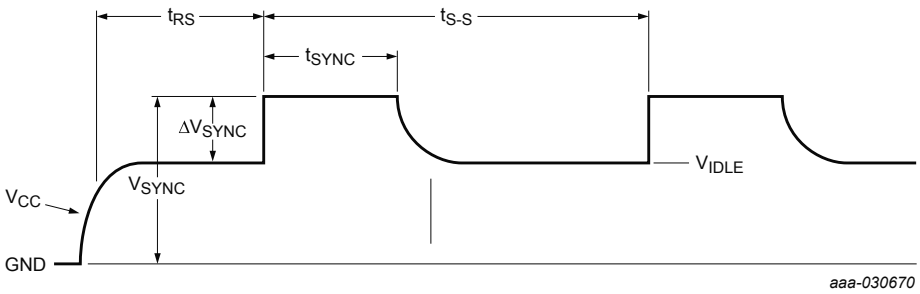



**Figure 85. Sync pulse characteristics**




### 10.2.1.2 *Synchronization pulse pulldown function*

The device includes an optional Sync pulse pulldown function for systems in which the master device does not include an active pull-down function. The device uses the modulation current pulldown circuit, which sinks $I_{R\_PSI5}$ additional current from the BUS_I pin. The pulldown current is activated after $t_{PD\_DLY}$ (referenced to $t_{TRIG}$), and is activated for $t_{PD\_ON}$.

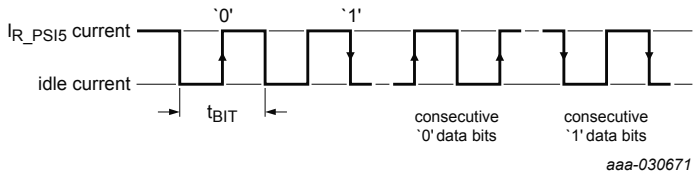
The Sync pulse pulldown function is disabled in Programming Mode, in Initialization Phase 1, and in Daisy Chain Mode until the Run Command is received.

## 10.3 Data transmission data link layer

### 10.3.1 Bit encoding

The device outputs data by modulation of the $V_{CC}$ current using Manchester Encoding. Data is stored in a transition occur-ring in the middle of the bit time. The signal idles at the normal quiescent supply current. A logic low is defined as an increase in current at the middle of a bit time. A logic high is defined as a decrease in current at the middle of a bit time. There is always a transition in the middle of the bit time. If consecutive "1" or "0" data are transmitted, a transition occurs at the start of a bit time.

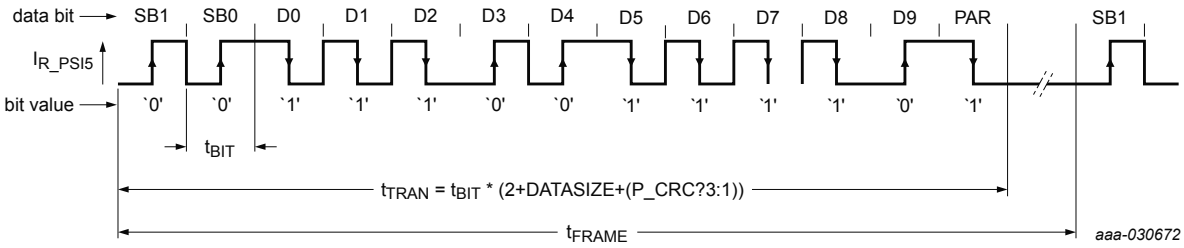
**Figure 86. Manchester data bit encoding**




### 10.3.2 PSI5 data transmission

PSI5 data transmission frames are composed of two start bits, a 10-bit data word, and error detection bit(s). Data words are transmitted least significant bit (LSB) first. A typical Manchester-encoded transmission frame is illustrated in Figure 87. Example Manchester encoded data transfer - PSI5-x10x.

**Figure 87. Example Manchester encoded data transfer - PSI5-x10x**




#### *10.3.2.1 PSI5-x10P transmission mode*

The device can be configured to transmit 10-bit data with parity by setting the PDCMFORMAT bits in the SOURCEID_x registers and the P_CRC bit in the PSI5_CFG register.

**Table 262. PSI5-x10P transmission mode**

| Start Bits | | Sensor data (See Section 8.6.4.9: Output scaling) | | | | | | | | | | Parity |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | P |

#### *10.3.2.2 PSI5-x10C transmission mode*

The device can be configured to transmit 10-bit data with 3-bit CRC by setting the PDCMFORMAT bits in the SOURCEID_x registers and the P_CRC bit in the PSI5_CFG register.

**Table 263. PSI5-x10C transmission mode**

| Start bits | | Sensor data (See Section 8.6.4.9: Output scaling) | | | | | | | | | | CRC | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | C2 | C1 | C0 |

#### 10.3.2.3 *PSI5-x16P transmission mode*

The device can be configured to transmit 16-bit data with parity by setting the PDCMFORMAT bits in the SOURCEID_x registers and the P_CRC bit in the PSI5_CFG register. In 16-bit mode, the 10-bit initialization and status data are is transmitted in the upper 10-bits of the data packet and the lower 6-bits are filled-up with D6 bit value all zeros.

**Table 264. PSI5-x16P transmission mode**

| Start bits | | Sensor data (See Section 8.6.4.9: Output scaling) | | | | | | | | | | | | | | | | Parity |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | P |
| Init Data | | D6 0 | D6 0 | D6 0 | D6 0 | D6 0 | D6 0 | 10-bit Initialization Data as specified in Section 10.4.2.1: PSI5 initialization phase 2 data transmissions | | | | | | | | | | P |
| Status Data | | D6 | D6 | D6 | D6 | D6 | D6 | 10-bit Status Data as specified Section 10.3.4: PSI5 data field and data range values | | | | | | | | | | P |

#### 10.3.2.4 *PSI5-x16C transmission mode*

The device can be configured to transmit 16-bit data with 3-bit CRC by setting the PDCMFORMAT bits in the SOURCEID_x registers and the P_CRC bit in the PSI5_CFG register. In 16-bit mode, the 10-bit initialization and status data are is transmitted in the upper 10-bits of the data packet and the lower 6-bits are filled-up with D6 bit value all zeros.

**Table 265. PSI5-x16C transmission mode**

| Start bits | | Sensor data (See Section 8.6.4.9: Output scaling) | | | | | | | | | | | | | | | | CRC | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | C2 | C1 | C0 |
| Init Data | | D6 0 | D6 0 | D6 0 | D6 0 | D6 0 | D6 0 | 10-bit Initialization Data as specified in Section 10.4.2.1: PSI5 initialization phase 2 data transmissions | | | | | | | | | | C2 | C1 | C0 |
| Status Data | | D6 | D6 | D6 | D6 | D6 | D6 | 10-bit Status Data as specified Section 10.3.4: PSI5 data field and data range values | | | | | | | | | | C2 | C1 | C0 |

### 10.3.3 Error detection

Error detection of the transmitted data is accomplished via either a parity bit, or a 3-bit CRC. The type of error detection used is selected by the P_CRC bit in the PSI5_CFG register.

#### 10.3.3.1 *Parity error detection*

When parity error detection is selected, even parity is employed. The number of logic '1' bits in the transmitted message must be an even number.

#### 10.3.3.2 *3-bit CRC error detection*

When CRC error detection is selected, a 3-bit CRC is appended to each response message. The 3-bit CRC uses a generator polynomial of $g(x) = X^3+X+1$, with a non-direct seed value = '111'. Message data from the transmitted message is read into the CRC calculator LSB first, and the data is augmented with '000'. Start bits are not used in the CRC calculation. Table 266. PSI5 3-bit CRC calculation examples shows some example CRC calculation values for 10-bit data transmissions.

**Table 266. PSI5 3-bit CRC calculation examples**

| Data transmitted | | | | | | | | | | | CRC | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HEX | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | C2 | C1 | C0 |
| 0x000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0x0CC | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0x151 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| Data transmitted | | | | | | | | | | | CRC | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HEX | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | C2 | C1 | C0 |
| 0x1E0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0x1F4 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0x220 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0x275 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0x333 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0x3FF | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

### 10.3.4 PSI5 data field and data range values

Table 267. PSI5 data values shows the details for each data range. The PSI5 data field size is defined by the PDCMFORMAT bits in the SOURCEID_x registers as described in Section 8.2.13.2: PDCM format control bits (PDCMFORMAT[2:0]).

**Table 267. PSI5 data values**

| 16-bit data values | | 10-bit data value | | | Description (EMSG_EXT = 1 in PSI5_CFG) | Description (EMSG_EXT = 0 in PSI5_CFG) |
|---|---|---|---|---|---|---|
| Dec | Hex | Dec | Binary | Hex | | |
| +32704 | 7FFF<br>7FC0 | +511 | | 1FF | Reserved | Reserved |
| +32640 | 7F80 | +510 | | 1FE | | |
| +32576 | 7F7F<br>7F40 | +509 | | 1FD | | |
| +32512 | 7F00 | +508 | | 1FC | | |
| +32448 | 7EFF<br>7EC0 | +507 | | 1FB | | |
| +32384 | 7E80 | +506 | | 1FA | | |
| +32320 | 7E7F<br>7E40 | +505 | | 1F9 | | |
| +32256 | 7E00 | +504 | | 1F8 | | |
| +32192 | 7DFF<br>7DC0 | +503 | | 1F7 | | |
| +32128 | 7D80 | +502 | | 1F6 | | |
| +32064 | 7D7F<br>7D40 | +501 | | 1F5 | | |
| +32000 | 7D00 | +500 | | 1F4 | Reserved | Sensor Defect Error |
| +31936 | 7CFF<br>7CC0 | +499 | | 1F3 | Reserved | Reserved |
| +31872 | 7C80 | +498 | | 1F2 | | |
| +31808 | 7C7F<br>7C40 | +497 | | 1F1 | | |
| +31744 | 7C00 | +496 | | 1F0 | | |
| +31680 | 7BFF<br>7BC0 | +495 | | 1EF | Communication Error (OSCTRAIN_ERR bit) | Reserved (Error Mapped to 0x1F4) |

| 16-bit data values | | 10-bit data value | | | Description (EMSG_EXT = 1 in PSI5_CFG) | Description (EMSG_EXT = 0 in PSI5_CFG) |
|---|---|---|---|---|---|---|
| Dec | Hex | Dec | Binary | Hex | | |
| +31616 | 7B80 | +494 | | 1EE | Test Mode Enabled (TESTMODE bit set) | Reserved (Error Mapped to 0x1F4) |
| +31552 | 7B40 | +493 | | 1ED | Offset Error (CH0 or CH1 OFFSET_ERR bit set) | |
| +31488 | 7B00 | +492 | | 1EC | Temperature Error (TEMP0_ERR or TEMP1_ERR bit set) | |
| +31424 | 7AFF<br>7AC0 | +491 | | 1EB | Memory Error (F_OTP_ERR, U_OTP_ERR or U_RW_ERR set) | |
| +31360 | 7A80 | +490 | | 1EA | Sensor Self-test Error (CH0 or CH1 ST_ERROR bit set) | Sensor Self-test Error |
| +31296 | 7A7F<br>7A40 | +489 | | 1E9 | Reserved | Reserved |
| +31232 | 7A00 | +488 | | 1E8 | Sensor Busy | Sensor Busy |
| +31168 | 79FF<br>79C0 | +487 | | 1E7 | Sensor Ready | Sensor Ready |
| +31104 | 7980 | +486 | | 1E6 | Sensor Ready, but Unlocked | Sensor Ready, but Unlocked |
| +31040 | 797F<br>7940 | +485 | | 1E5 | Reserved | Reserved |
| +30976 | 7900 | +484 | | 1E4 | | |
| +30912 | 78FF<br>78C0 | +483 | | 1E3 | | |
| NA | NA | +482 | | 1E2 | Bidirectional Communication: RC "Error" | Bidirectional Communication: RC "Error" |
| NA | NA | +481 | | 1E1 | Bidirectional Communication: RC "OK" | Bidirectional Communication: RC "OK" |
| +30720 | 7800 | +480 | | 1E0 | Maximum positive sensor value | Maximum positive sensor value |
| .<br>.<br>. | .<br>.<br>. | .<br>.<br>. | | .<br>.<br>. | Positive sensor values | Positive sensor values |
| +129 to +192 | 0081 to 00C0 | +3 | | 003 | | |
| +65 to +128 | 0041 to 0080 | +2 | | 002 | | |
| +1 to +64 | 0001 to 0040 | +1 | | 001 | | |
| 0 | 0000 | 0 | | 000 | Zero | Zero |
| –1 to –64 | FFFF to FFC0 | –1 | | 3FF | Negative sensor values | Negative sensor values |
| –65 to –128 | FFBF to FF80 | –2 | | 3FE | | |
| –129 to –192 | FF7F to FF40 | –3 | | 3FD | | |
| .<br>.<br>. | .<br>.<br>. | .<br>.<br>. | | .<br>.<br>. | | |
| –30720 | 8800 | –480 | | 220 | Maximum negative sensor value | Maximum negative sensor value |

| 16-bit data values | | 10-bit data value | | | Description (EMSG_EXT = 1 in PSI5_CFG) | Description (EMSG_EXT = 0 in PSI5_CFG) |
|---|---|---|---|---|---|---|
| Dec | Hex | Dec | Binary | Hex | | |
| –30784 | 87FF<br>87C0 | –481 | 1000011111 | 21F | | |
| .<br>.<br>. | .<br>.<br>. | .<br>.<br>. | .<br>.<br>. | .<br>.<br>. | Initialization Data Codes<br>10-bit Status Data Nibble 1 - 16 (0000 - 1111) (Dx) | |
| –31744 | 8400 | –496 | 1000010000 | 210 | | |
| –31808 | 83FF<br>83C0 | –497 | 1000001111 | 20F | | |
| .<br>.<br>. | .<br>.<br>. | .<br>.<br>. | .<br>.<br>. | .<br>.<br>. | Initialization Data IDs<br>Block ID 1 - 16 (10-bit Mode) (IDx) | |
| –32767 | 8000 | –512 | 1000000000 | 200 | | |

## 10.4 Initialization

Following power-up, the device proceeds through an initialization process which is divided into 3 phases:

- Initialization Phase 1: No Data transmissions occur
- Initialization Phase 2: Sensor self-test and transmission of configuration information
- Initialization Phase 3: Transmission of the "Sensor Busy" and / or "Sensor Ready" / "Sensor Defect" messages

Once initialization is completed the device begins normal mode operation, which continues as long as the supply voltage remains within the specified limits.

In asynchronous mode, initialization data is transmitted for Source ID 0 only.

In synchronous mode, the same initialization data is transmitted for each enabled Source ID.

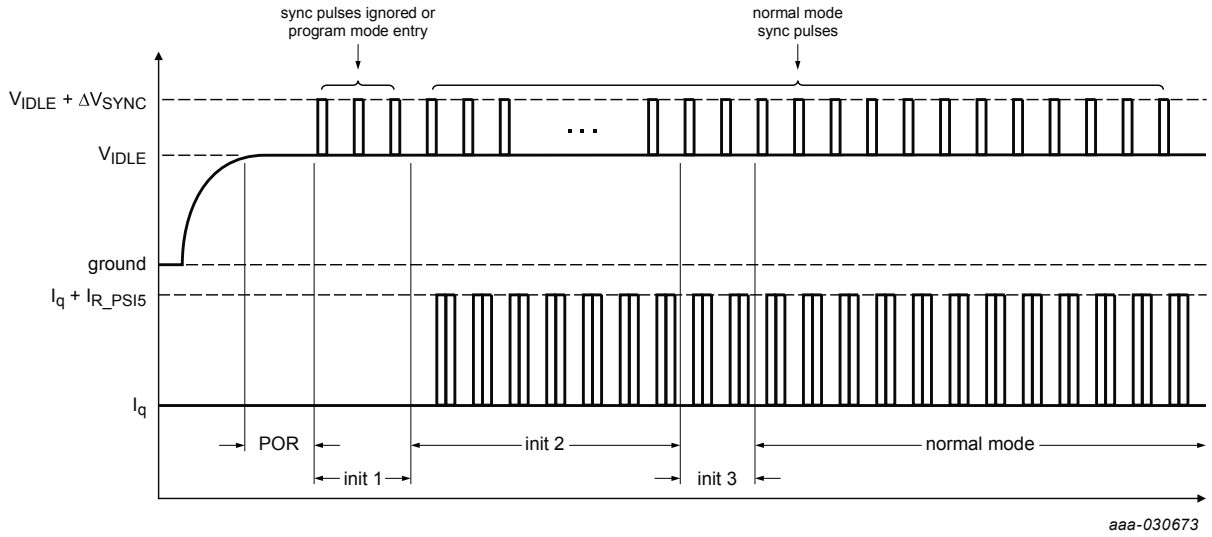
In synchronous mode, the initialization data is transmitted independently for each channel.

In daisy chain mode, initialization data is transmitted in the Source ID 0 time slot as defined by the sensor address as documented in Section 10.8: Daisy chain mode.

In daisy chain mode, initialization data is transmitted in the Source ID 0 and Source ID 2 time slot as defined by the sensor address as documented in Section 10.8: Daisy chain mode.

In Dual Transmission mode, initialization data is transmitted for both Source ID 0 and Source ID 2 in the Source ID 0 timeslot as documented in Section 10.7: Dual transmission mode.

**Figure 88. PSI5 sensor 10-bit initialization**




During PSI5 initialization, the device completes an internal initialization process consisting of the following:

- Power-on reset
- Device Initialization
- Program mode entry verification
- Offset cancellation low-pass filter initialization
- Self-test

Figure 89. PSI5 initialization timing, synchronous mode shows the timing for internal and external initialization in synchronous mode. Figure 90. PSI5 initialization timing, asynchronous mode shows the timing for internal and external initialization in asynchronous mode. Timing parameters are specified in Section 7.13: Dynamic electrical characteristics - PSI5.

**Figure 89. PSI5 initialization timing, synchronous mode**

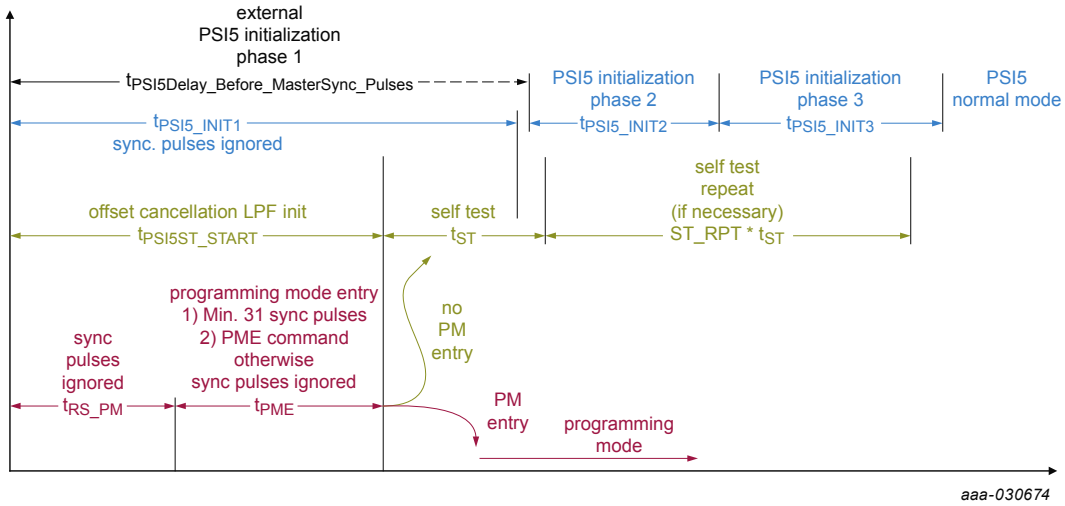
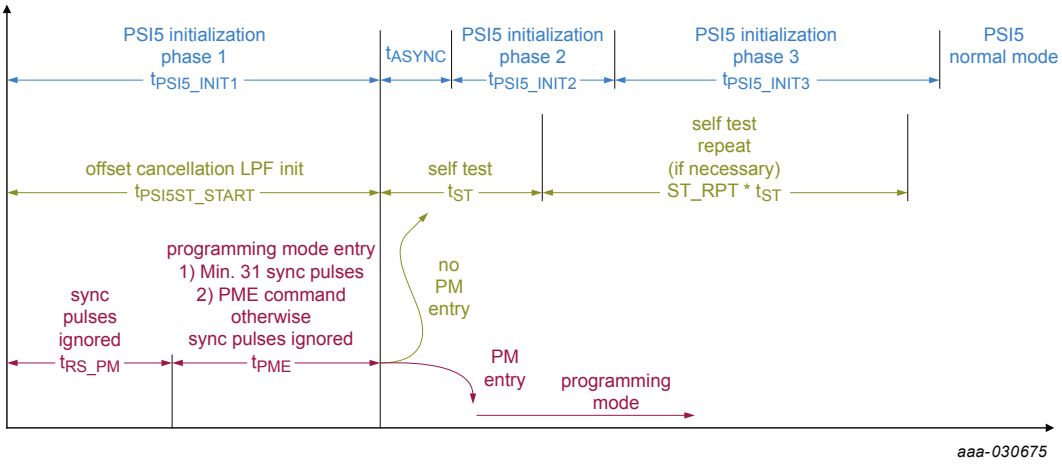


Figure 90. **PSI5 initialization timing, asynchronous mode**




### 10.4.1 PSI5 initialization phase 1

During PSI5 initialization phase 1, the device begins internal initialization and self-checks, but transmits no data. Initialization begins with this sequence, shown in Figure 89. PSI5 initialization timing, synchronous mode:

1. Internal delay to ensure analog circuitry has stabilized ($t_{POR\_PSI5}$)
2. Offset cancellation low-pass filter initialization begins ($t_{PSI5ST\_START}$)
3. Monitor for the Programming Mode Entry Sequence ($t_{PME}$)
4. If the Programming Mode Entry Sequence is not detected, the device enters Initialization Phase 2 ($t_{PSI5\_INIT2}$)

### 10.4.2 PSI5 initialization phase 2

During PSI5 initialization phase 2, the device continues its internal selfchecks and transmits the PSI5 initialization phase 2 data. Initialization data is transmitted using the initialization data codes and IDs specified in Table 267. PSI5 data values, and in the order shown in Table 268. PSI5 initialization phase 2 data transmission order.

Table 268. **PSI5 initialization phase 2 data transmission order**

| D1 | | | | | | | D2 | | | | | | | ... | D32 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $ID1_1$ | $D1_1$ | $ID1_2$ | $D1_2$ | ... | $ID1_k$ | $D1_k$ | $ID2_1$ | $D2_1$ | $ID2_2$ | $D2_2$ | ... | $ID2_k$ | $D2_k$ | ... | $ID32_1$ | $D32_1$ | $ID32_2$ | $D32_2$ | ... | $ID32_k$ | $D32_k$ |
| Repeat k times | | | | | | | Repeat k times | | | | | | | ... | Repeat k times | | | | | | |

The Initialization phase 2 time is calculated using Eq. (17).

$$t_{Phase2} = Trans_{Nibble} \times k \times (DataFields) \times t_{S-S} \quad (17)$$

Where:

| | | |
|---|---|---|
| $Trans_{Nibble}$ | = | # of Transmissions per Data Nibble<br>2: 1 for ID, and 1 for Data |
| $k$ | = | The repetition rate for the data fields |
| *Data Fields* | = | 32 data fields or 48 data fields (if INIT2_EXT is set) |
| $t_{S-S}$ | = | Sync Pulse Period |

#### 10.4.2.1 *PSI5 initialization phase 2 data transmissions*

In PSI5 initialization phase 2, the device transmits a sequence of sensor specific configuration and serial number information. The transmission data is in conformance with the PSI5 [5] specification, and AKLV27 [3] . Unique data content is transmitted for each channel. The data content and transmission format is shown in Table 270. Channel 0 PSI5 initialization phase 2 data and Table 271. Channel 1 PSI5 Initialization Phase 2 Data . Table 269. Initialization phase 2 time shows the phase 2 timing for different operating modes. Times are calculated using the equation in Section 10.4.2: PSI5 initialization phase 2.

**Table 269. Initialization phase 2 time**

| Operating mode | Repetition rate (k) | # of transmissions | Nominal phase 2 time |
|---|---|---|---|
| Asynchronous Mode (228 µs) | 8 | 512 | 116.7 ms |
| Synchronous Mode (500 µs) | 4 | 256 | 128.0 ms |

**Table 270. Channel 0 PSI5 initialization phase 2 data**

| PSI5 field ID # | PSI5 nibble ID # | Page address | PSI5 nibble address | Register address | PSI5 description | Value |
|---|---|---|---|---|---|---|
| F1 | D1 | 0 | 0000 | USERDATA_0[3:0] | User Specific Data | User |
| F2 | D2, D3 | | 0001, 0010 | NA | Number of Data Blocks: 32: INIT2_EXT = 0, 48: INIT2_EXT = 1 | 0010 0000 or 0011 0000 |
| F3 | D4, D5 | | 0011, 0100 | USERDATA_1[3:0], USERDATA_1[7:4] | User Specific Data | User |
| F4 | D6, D7 | | 0101, 0110 | USERDATA_2[3:0], USERDATA_2[7:4] | User Specific Data | User |
| F5 | D8 | | 0111 | USERDATA_3[3:0] | User Specific Data | User |
| | D9 | | 1000 | USERDATA_3[7:4] | User Specific Data | User |
| F6 | D10 | | 1001 | USERDATA_4[3:0] | User Specific Data | User |
| | D11 | | 1010 | USERDATA_4[7:4] | User Specific Data | User |
| F7 | D12 | | 1011 | USERDATA_5[3:0] | User Specific Data | User |
| | D13 | | 1100 | USERDATA_5[7:4] | User Specific Data | User |
| | D14 | | 1101 | USERDATA_6[3:0] | User Specific Data | User |
| F8 | D15 | | 1110 | USERDATA_7[3:0] | User Specific Data | User |
| | D16 | | 1111 | USERDATA_7[7:4] | User Specific Data | User |
| | D17 | 1 | 0000 | USERDATA_8[3:0] | User Specific Data | User |
| | D18 | | 0001 | USERDATA_8[7:4] | User Specific Data | User |
| F9 | D19 | | 0010 | SN4[7:4] or USERDATA_6[7:4] | Data determined by PSI5_INIT2_D19 in TIMING_CFG2 register | User |
| | D20 | | 0011 | SN4[3:0] or USERDATA_E[7:4] | Data determined by PSI5_INIT2_D19 in TIMING_CFG2 register | User |
| | D21 | | 0100 | SN3[7:4] | Device Serial Number | Factory |
| | D22 | | 0101 | SN3[3:0] | Device Serial Number | Factory |
| | D23 | | 0110 | SN2[7:4] | Device Serial Number | Factory |
| | D24 | | 0111 | SN2[3:0] | Device Serial Number | Factory |
| | D25 | | 1000 | SN1[7:4] | Device Serial Number | Factory |
| | D26 | | 1001 | SN1[3:0] | Device Serial Number | Factory |
| | D27 | | 1010 | SN0[7:4] | Device Serial Number | Factory |
| | D28 | | 1011 | SN0[3:0] | Device Serial Number | Factory |
| | D29 | | 1100 | PN1[3:0] | Device Part Number | Factory |
| | D30 | | 1101 | PN0[7:4] | Device Part Number | Factory |
| | D31 | | 1110 | PN0[3:0] | Device Part Number | Factory |
| | D32 | | 1111 | USERDATA_6[7:4] | User Specific Data | User |
| F10 | D33 | 2 | 0000 | CH0_STAVG_P[7:4] | Channel 0 Positive Self-test, High Nibble | Varies |
| | D34 | | 0001 | CH0_STAVG_P[3:0] | Channel 0 Positive Self-test, Low Nibble | Varies |
| | D35 | | 0010 | CH0_STOFFSET_P[7:4] | Channel 0 Post Positive Self-test Offset, High Nibble | Varies |
| | D36 | | 0011 | CH0_STOFFSET_P[3:0] | Channel 0 Post Positive Self-test Offset, Low Nibble | Varies |
| | D37 | | 0100 | CH0_STAVG_N[7:4] | Channel 0 Negative Self-test, High Nibble | Varies |
| | D38 | | 0101 | CH0_STAVG_N[3:0] | Channel 0 Negative Self-test, Low Nibble | Varies |

| PSI5 field ID # | PSI5 nibble ID # | Page address | PSI5 nibble address | Register address | PSI5 description | Value |
|---|---|---|---|---|---|---|
| F10 | D39 | 2 | 0110 | CH0_STOFFSET_N[7:4] | Channel 0 Post Negative Self-test Offset, High Nibble | Varies |
| | D40 | | 0111 | CH0_STOFFSET_N[3:0] | Channel 0 Post Negative Self-test Offset, Low Nibble | Varies |
| | D41 | | 1000 | RESERVED | | RESERVED |
| | D42 | | 1001 | RESERVED | | RESERVED |
| | D43 | | 1010 | RESERVED | | RESERVED |
| | D44 | | 1011 | RESERVED | | RESERVED |
| | D45 | | 1100 | RESERVED | | RESERVED |
| | D46 | | 1101 | RESERVED | | RESERVED |
| | D47 | | 1110 | RESERVED | | RESERVED |
| | D48 | | 1111 | RESERVED | | RESERVED |
| F10 | D33 | 2 | 0000 | CH0_STAVG_P[7:4] | Channel 0 Positive Self-test, High Nibble | Varies |
| | D34 | | 0001 | CH0_STAVG_P[3:0] | Channel 0 Positive Self-test, Low Nibble | Varies |
| | D35 | | 0010 | CH0_STOFFSET_P[7:4] | Channel 0 Post Positive Self-test Offset, High Nibble | Varies |
| | D36 | | 0011 | CH0_STOFFSET_P[3:0] | Channel 0 Post Positive Self-test Offset, Low Nibble | Varies |
| | D37 | | 0100 | CH0_STAVG_N[7:4] | Channel 0 Negative Self-test, High Nibble | Varies |
| | D38 | | 0101 | CH0_STAVG_N[3:0] | Channel 0 Negative Self-test, Low Nibble | Varies |
| | D39 | | 0110 | CH0_STOFFSET_N[7:4] | Channel 0 Post Negative Self-test Offset, High Nibble | Varies |
| | D40 | | 0111 | CH0_STOFFSET_N[3:0] | Channel 0 Post Negative Self-test Offset, Low Nibble | Varies |
| | D41 | | 1000 | CH1_STAVG_P[7:4] | Channel 1 Positive Self-test, High Nibble | Varies |
| | D42 | | 1001 | CH1_STAVG_P[3:0] | Channel 1 Positive Self-test, Low Nibble | Varies |
| | D43 | | 1010 | CH1_STOFFSET_P[7:4] | Channel 1 Post Positive Self-test Offset, High Nibble | Varies |
| | D44 | | 1011 | CH1_STOFFSET_P[3:0] | Channel 1 Post Positive Self-test Offset, Low Nibble | Varies |
| | D45 | | 1100 | CH1_STAVG_N[7:4] | Channel 1 Negative Self-test, High Nibble | Varies |
| | D46 | | 1101 | CH1_STAVG_N[3:0] | Channel 1 Negative Self-test, Low Nibble | Varies |
| | D47 | | 1110 | CH1_STOFFSET_N[7:4] | Channel 1 Post Negative Self-test Offset, High Nibble | Varies |
| | D48 | | 1111 | CH1_STOFFSET_N[3:0] | Channel 1 Post Negative Self-test Offset, Low Nibble | Varies |

## Table 271. Channel 1 PSI5 Initialization Phase 2 Data

| PSI5 field ID # | PSI5 nibble ID # | Page address | PSI5 nibble address | Register address | Description | Value |
|---|---|---|---|---|---|---|
| F1 | D1 | 0 | 0000 | USERDATA_0[7:4] | User Specific Data | User |
| F2 | D2, D3 | | 0001, 0010 | NA | Number of Data Blocks: 32: INIT2_EXT = 0, 48: INIT2_EXT = 1 | 0010 0000 or 0011 0000 |
| F3 | D4, D5 | | 0011, 0100 | USERDATA_9[3:0], USERDATA_9[7:4] | User Specific Data | User |
| F4 | D6, D7 | | 0101, 0110 | USERDATA_A[3:0], USERDATA_A[7:4] | User Specific Data | User |
| F5 | D8 | | 0111 | USERDATA_B[3:0] | User Specific Data | User |
| | D9 | | 1000 | USERDATA_B[7:4] | User Specific Data | User |
| F6 | D10 | | 1001 | USERDATA_C[3:0] | User Specific Data | User |
| | D11 | | 1010 | USERDATA_C[7:4] | User Specific Data | User |
| F7 | D12 | | 1011 | USERDATA_D[3:0] | User Specific Data | User |
| | D13 | | 1100 | USERDATA_D[7:4] | User Specific Data | User |
| | D14 | | 1101 | USERDATA_E[3:0] | User Specific Data | User |
| F8 | D15 | | 1110 | USERDATA_7[3:0] | User Specific Data | User |
| | D16 | | 1111 | USERDATA_7[7:4] | User Specific Data | User |
| | D17 | 1 | 0000 | USERDATA_8[3:0] | User Specific Data | User |
| | D18 | | 0001 | USERDATA_8[7:4] | User Specific Data | User |
| F9 | D19 | | 0010 | SN4[7:4] or USERDATA_6[7:4] | Data determined by PSI5_INIT2_D19 in TIMING_CFG2 register | User |
| | D20 | | 0011 | SN4[3:0] or USERDATA_E[7:4] | Data determined by PSI5_INIT2_D19 in TIMING_CFG2 register | User |
| | D21 | | 0100 | SN3[7:4] | Device Serial Number | Factory |
| | D22 | | 0101 | SN3[3:0] | Device Serial Number | Factory |
| | D23 | | 0110 | SN2[7:4] | Device Serial Number | Factory |
| | D24 | | 0111 | SN2[3:0] | Device Serial Number | Factory |

| PSI5 field ID # | PSI5 nibble ID # | Page address | PSI5 nibble address | Register address | Description | Value |
|---|---|---|---|---|---|---|
| F9 | D25 | 1 | 1000 | SN1[7:4] | Device Serial Number | Factory |
| | D26 | | 1001 | SN1[3:0] | Device Serial Number | Factory |
| | D27 | | 1010 | SN0[7:4] | Device Serial Number | Factory |
| | D28 | | 1011 | SN0[3:0] | Device Serial Number | Factory |
| | D29 | | 1100 | PN1[3:0] | Device Part Number | Factory |
| | D30 | | 1101 | PN0[7:4] | Device Part Number | Factory |
| | D31 | | 1110 | PN0[3:0] | Device Part Number | Factory |
| | D32 | | 1111 | USERDATA_E[7:4] | User Specific Data | User |
| F10 | D33 | 2 | 0000 | CH0_STAVG_P[7:4] | Channel 0 Positive Self-test, High Nibble | Varies |
| | D34 | | 0001 | CH0_STAVG_P[3:0] | Channel 0 Positive Self-test, Low Nibble | Varies |
| | D35 | | 0010 | CH0_STOFFSET_P[7:4] | Channel 0 Post Positive Self-test Offset, High Nibble | Varies |
| | D36 | | 0011 | CH0_STOFFSET_P[3:0] | Channel 0 Post Positive Self-test Offset, Low Nibble | Varies |
| | D37 | | 0100 | CH0_STAVG_N[7:4] | Channel 0 Negative Self-test, High Nibble | Varies |
| | D38 | | 0101 | CH0_STAVG_N[3:0] | Channel 0 Negative Self-test, Low Nibble | Varies |
| | D39 | | 0110 | CH0_STOFFSET_N[7:4] | Channel 0 Post Negative Self-test Offset, High Nibble | Varies |
| | D40 | | 0111 | CH0_STOFFSET_N[3:0] | Channel 0 Post Negative Self-test Offset, Low Nibble | Varies |
| | D41 | | 1000 | CH1_STAVG_P[7:4] | Channel 1 Positive Self-test, High Nibble | Varies |
| | D42 | | 1001 | CH1_STAVG_P[3:0] | Channel 1 Positive Self-test, Low Nibble | Varies |
| | D43 | | 1010 | CH1_STOFFSET_P[7:4] | Channel 1 Post Positive Self-test Offset, High Nibble | Varies |
| | D44 | | 1011 | CH1_STOFFSET_P[3:0] | Channel 1 Post Positive Self-test Offset, Low Nibble | Varies |
| | D45 | | 1100 | CH1_STAVG_N[7:4] | Channel 1 Negative Self-test, High Nibble | Varies |
| | D46 | | 1101 | CH1_STAVG_N[3:0] | Channel 1 Negative Self-test, Low Nibble | Varies |
| | D47 | | 1110 | CH1_STOFFSET_N[7:4] | Channel 1 Post Negative Self-test Offset, High Nibble | Varies |
| | D48 | | 1111 | CH1_STOFFSET_N[3:0] | Channel 1 Post Negative Self-test Offset, Low Nibble | Varies |

*Note: Offset and self-test data in Field ID #10 is only transmitted if the internal self-test for the associated channel has completed and has passed before F10, D33 is to be transmitted. This can only occur if the internal self-test sequence passes the first time. If F10, D33 is to be transmitted before the internal self-test has completed for a specific channel, the latest self-test, and offset values are transmitted.*

*Note: If self-test has completed all retries and has failed before F10, D33 is to be transmitted, F10, D33 - D48 will include self-test data from the last failed attempt.*

*Note: In PSI5 asynchronous mode, self-test will not be complete prior to the transmission of the F10. Setting the INIT2_EXT bit will result in invalid self-test data in D33 and D34 (0x0 values).*

*Note: Constant values are transmitted for all fields marked as "RESERVED"*

### 10.4.3 Internal self-test

Once Initialization Phase 1 completes, the device begins its internal self-test as described in Section 8.6.2.5: PSI5 automatic startup self-test procedure . If self-test fails, the device repeats self-test up to ST_RPT times.

### 10.4.4 Initialization phase 3

During PSI5 initialization phase 3, the device completes its internal self-checks, and transmits a combination of "Sensor Busy" or "Sensor Ready" messages as defined in Table 267. PSI5 data values. The number of "Sensor Busy" messages transmitted in initialization phase 3 varies depending on the mode of operation, and the number of self-test repetitions. Self-test is repeated on failure up to ST_RPT times to provide immunity to misuse inputs during initialization. Self-test terminates successfully after one successful self-test sequence.

Once internal self-test is completed, the device transmits 2 "Sensor Ready" commands.

*Note: Self-test repeats are handled independently for each channel. However, both channels will exit initialization phase 3 simultaneously. If only one channel is repeating self-tests, both channels transmit "Sensor Busy" commands until either self-test has passed on both channels or the total number of repeats have completed.*

The ENDINIT bit is automatically set when the device exits Initialization Phase 3.

## 10.5 Normal mode

### 10.5.1 Asynchronous mode

The device can be programmed to respond in asynchronous mode as specified in Section 8.2.18.1: Periodic data collection mode response start time (PDCM_RSPSTx[12:0]).

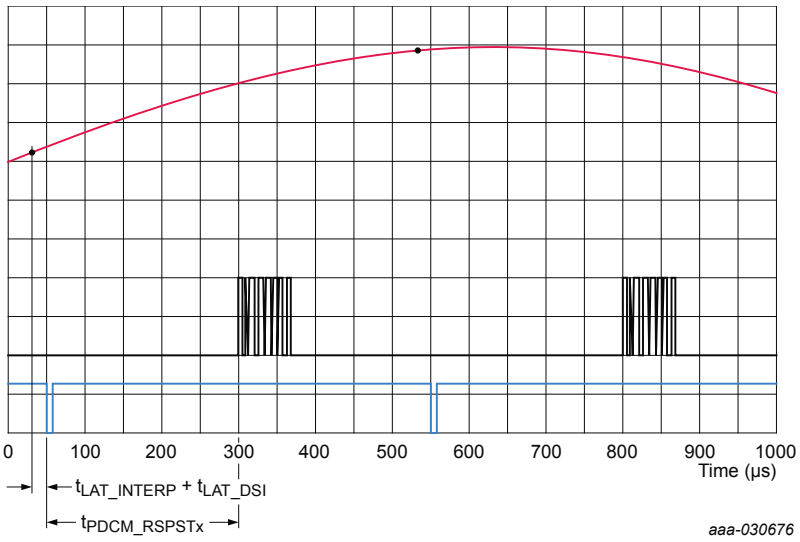
In asynchronous mode, the device transmits data at a fixed rate ($t_{ASYNC}$) and will not respond to normal sync pulses. However, during initialization phase 1, the device will monitor sync pulses to decode the programming mode entry command and allow entry into programming mode.

### 10.5.2 Simultaneous sampling mode

The device can be programmed to respond in simultaneous sampling mode by programming the SS_EN bit to "Simultaneous Sampling Mode".

In simultaneous sampling mode, the most recent interpolated sensor data sample is latched at $t_{TRIG}$ (rising edge of Sync Pulse) and transmitted starting at the time programmed in the PDCM_RSPSTx registers, relative to $t_{TRIG}$.

**Figure 91. Simultaneous sampling mode**

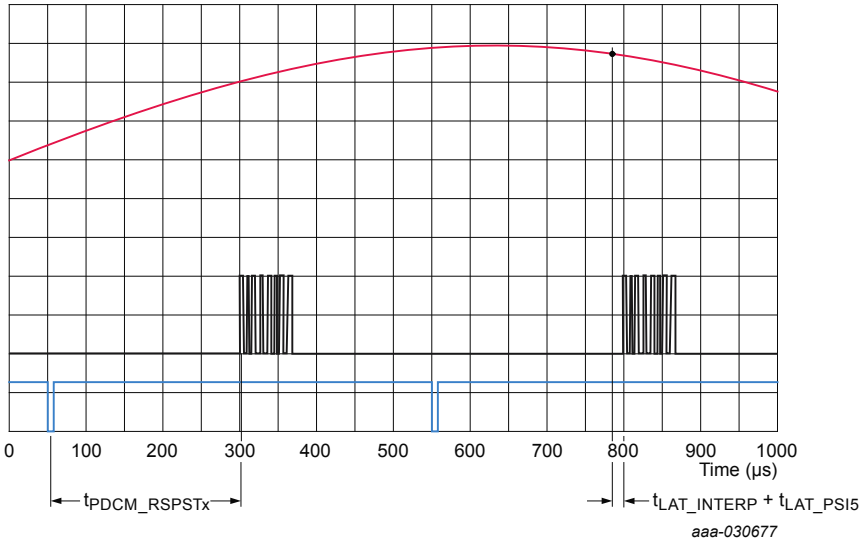



### 10.5.3 Synchronous sampling mode with minimum latency

The device can be programmed to respond in synchronous sampling mode with minimum latency by programming the SS_EN bit to "Synchronous Sampling Mode".

In synchronous sampling mode, the most recent interpolated sensor data sample is latched at the time programmed in the PDCM_RSPSTx registers, relative to $t_{TRIG}$ (rising edge of Sync pulse). The data is transmitted starting at the time programmed in the PDCM_RSPSTx registers, relative to $t_{TRIG}$.

Figure 92. **Synchronous sampling mode with minimum latency**




## 10.6 PSI5 default mode (un-programmed PSI5 device)

Un-programmed NXLS96xxx PSI5 devices include a default PSI5 transmission mode. The devices will respond to PSI5 sync pulses and transmit data in PSI5-P16C-500/2L mode with the minimum user gain and the default 400 Hz, 4-Pole low-pass filter. Table 272. Default PSI5-P16C transmission mode shows the default PSI5 response transmission, Table 273. Default PSI5-P16C transmission mode timing parameters shows the PSI5 timing parameters, and Table 274. Default PSI5-P16C transmission mode, High g sensor data configuration and Table 275. Default PSI5-P16C transmission mode, Medium g sensor data configuration show the sensor data configuration details for each channel.

The default settings apply until the UF2 user OTP memory is written and the UF2 block is locked.

Figure 93. **PSI5 default mode transmission**

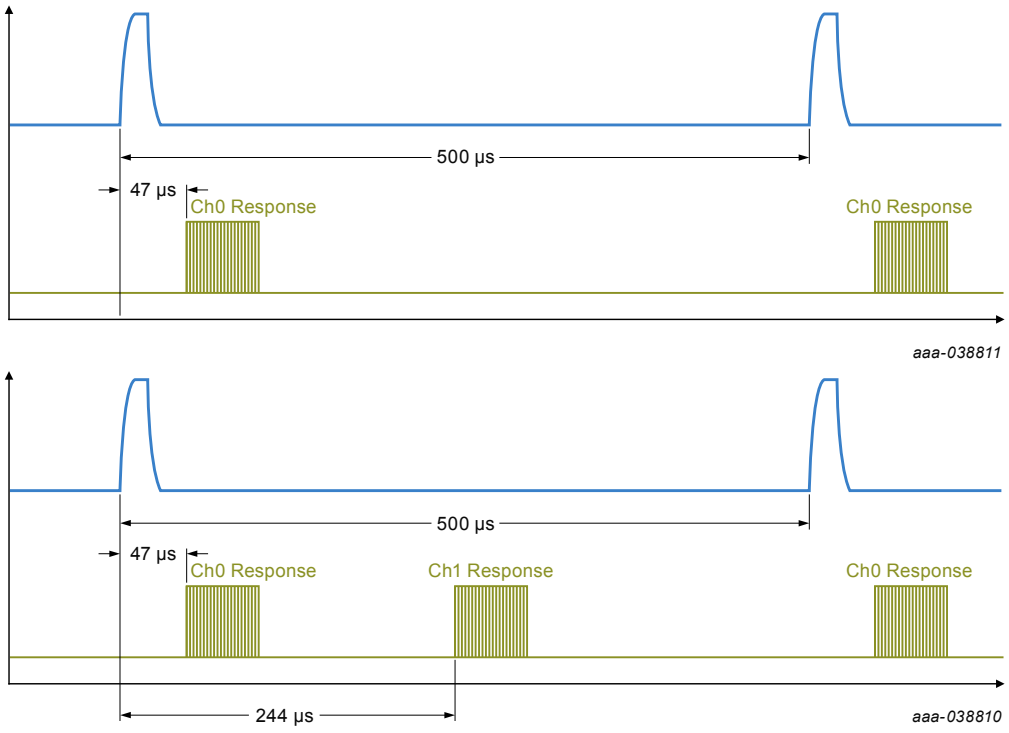


**Table 272. Default PSI5-P16C transmission mode**

| Start bits | | Sensor data (See Section 8.6.4.9: Output scaling) | | | | | | | | | | | | | | | | CRC | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | C2 | C1 | C0 |
| Init Data | | 0 | 0 | 0 | 0 | 0 | 0 | 10-bit Initialization Data as specified in Section 10.4.2.1: PSI5 initialization phase 2 data transmissions | | | | | | | | | | C2 | C1 | C0 |

**Table 273. Default PSI5-P16C transmission mode timing parameters**

| Parameter | Default typical value | Default register bit values |
|---|---|---|
| Ch0 Time Slot | 47 µs | $27, $26: $PDCM_RSPST0 = 0x002F |
| Ch1 Time Slot | 244 µs | $2B, $2A: $PDCM_RSPST1 = 0x00F4 |
| Data Size | 16-bit | $1A: SOURCEID_0[6:4] = 3'b100 |
| Error Checking | 3-bit CRC | $25: PSI5_CFG[2] = 1'b1 |
| Baud Rate | Low Baud Rate: 125 kB/s, Bit Time = 8.0 µs | $23: CHIPTIME[3:0] = 3'b1000 |

**Table 274. Default PSI5-P16C transmission mode, High g sensor data configuration**

| Parameter | Value | Default register bit values |
|---|---|---|
| Sensor Data Range | 702.6 g | $40, $48: CH0_CFG_U1 CHx_CFG_U1[1:0] = 2'b00 |
| Sensor Data Sensitivity | 43.79 LSB/g | $41, $49: CH0_CFG_U2 CHx_CFG_U2[7:0] = 0x00 |
| Sensor data low-pass filter | 400 Hz, 4-Pole LPF | $40, $48: CH0_CFG_U1 CHx_CFG_U1[7:4] = 4'b0000 |
| Sensor data offset cancellation | 0.04 Hz, 1-Pole HPF with Rate Limiting Enabled | $43, $4B: CH0_CFG_U4 CHx_CFG_U4[5:4] = 2'b00 |

**Table 275. Default PSI5-P16C transmission mode, Medium g sensor data configuration**

| Parameter | Value | Default register bit values |
|---|---|---|
| Sensor data range | 232.6 g | $40, $48: CH0_CFG_U1 CHx_CFG_U1[1:0] = 2'b00 |
| Sensor data sensitivity | 132.06 LSB/g | $41, $49: CH0_CFG_U2 CHx_CFG_U2[7:0] = 0x00 |
| Sensor data low-pass filter | 400 Hz, 4-Pole LPF | $40, $48: CH0_CFG_U1 CHx_CFG_U1[7:4] = 4'b0000 |
| Sensor data offset cancellation | 0.04 Hz, 1-Pole HPF with Rate Limiting Enabled | $43, $4B: CH0_CFG_U4 CHx_CFG_U4[5:4] = 2'b00 |

## 10.7 Dual transmission mode

The device can be programmed to transmit both channel 0 and channel 1 data in one data packet if the DUALTRANS bit is set in the PSI5_CFG register. In dual transmission mode, the source identification settings specified in Section 8.2.17.4: Dual transmission mode (DUALTRANS) determine the data transmitted as shown in Table 276. Dual transmission mode 10-bit transmission data with parity through Table 279. Dual transmission mode 16-bit transmission data with CRC.

**Table 276. Dual transmission mode 10-bit transmission data with parity**

| SID1_EN | SID0_EN | Response start time | Response format | | | |
|---|---|---|---|---|---|---|
| 0 | 0 | PDCM_RSTST0 | No Transmission | | | |
| | | PDCM_RSTST1 | No Transmission | | | |
| 0 | 1 | PDCM_RSTST0 | Start Bits | CH1_SNSDATA0 | CH0_SNSDATA0 | Parity |

| SID1_EN | SID0_EN | Response start time | Response format | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | PDCM_RSTST0 | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | P |
| | | PDCM_RSTST1 | No Transmission | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | PDCM_RSTST0 | No Transmission | | | | | | | | | | | | | | | | | | | | | | |
| | | PDCM_RSTST1 | Start Bits | | CH1_SNSDATA1 | | | | | | | | | | CH0_SNSDATA1 | | | | | | | | | | Parity |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | P |
| 1 | 1 | PDCM_RSTST0 | Start Bits | | CH1_SNSDATA0 | | | | | | | | | | CH0_SNSDATA0 | | | | | | | | | | Parity |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | P |
| | | PDCM_RSTST1 | Start Bits | | CH1_SNSDATA1 | | | | | | | | | | CH0_SNSDATA1 | | | | | | | | | | Parity |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | P |

## Table 277. Dual transmission mode 10-bit transmission data with CRC

| SID1_EN | SID0_EN | Response start time | Response format | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | PDCM_RSTST0 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | |
| | | PDCM_RSTST1 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | PDCM_RSTST0 | Start Bits | | CH1_SNSDATA0 | | | | | | | | | | CH0_SNSDATA0 | | | | | | | | | | CRC | | |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | C2 | C1 | C0 |
| | | PDCM_RSTST1 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | PDCM_RSTST0 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | |
| | | PDCM_RSTST1 | Start Bits | | CH1_SNSDATA1 | | | | | | | | | | CH0_SNSDATA1 | | | | | | | | | | CRC | | |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | C2 | C1 | C0 |
| 1 | 1 | PDCM_RSTST0 | Start Bits | | CH1_SNSDATA0 | | | | | | | | | | CH0_SNSDATA0 | | | | | | | | | | CRC | | |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | C2 | C1 | C0 |
| | | PDCM_RSTST1 | Start Bits | | CH1_SNSDATA1 | | | | | | | | | | CH0_SNSDATA1 | | | | | | | | | | CRC | | |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | C2 | C1 | C0 |

## Table 278. Dual transmission mode 16-bit transmission data with parity

| SID1_EN | SID0_EN | Response start time | Response format | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | PDCM_RSTST0 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | PDCM_RSTST1 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | PDCM_RSTST0 | Start | | CH1_SNSDATA0 | | | | | | | | | | | | | | | | CH0_SNSDATA0 | | | | | | | | | | | | | | | | P |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | P |
| | | PDCM_RSTST1 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | PDCM_RSTST0 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | PDCM_RSTST1 | Start | | CH1_SNSDATA1 | | | | | | | | | | | | | | | | CH0_SNSDATA1 | | | | | | | | | | | | | | | | P |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | P |
| 1 | 1 | PDCM_RSTST0 | Start | | CH1_SNSDATA0 | | | | | | | | | | | | | | | | CH0_SNSDATA0 | | | | | | | | | | | | | | | | P |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | P |
| | | PDCM_RSTST1 | Start | | CH1_SNSDATA1 | | | | | | | | | | | | | | | | CH0_SNSDATA1 | | | | | | | | | | | | | | | | P |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | P |

## Table 279. Dual transmission mode 16-bit transmission data with CRC

| SID1_EN | SID0_EN | Response start time | Response format | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | PDCM_RSTST0 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | PDCM_RSTST1 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | PDCM_RSTST0 | Start | | CH1_SNSDATA0 | | | | | | | | | | | | | | | | CH0_SNSDATA0 | | | | | | | | | | | | | | | | CRC | | |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | C2 | C1 | C0 |
| | | PDCM_RSTST1 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | PDCM_RSTST0 | No Transmission | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | PDCM_RSTST1 | Start | | CH1_SNSDATA1 | | | | | | | | | | | | | | | | CH0_SNSDATA1 | | | | | | | | | | | | | | | | CRC | | |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | C2 | C1 | C0 |
| 1 | 1 | PDCM_RSTST0 | Start | | CH1_SNSDATA0 | | | | | | | | | | | | | | | | CH0_SNSDATA0 | | | | | | | | | | | | | | | | CRC | | |

| SID1_EN | SID0_EN | Response start time | Response format | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | PDCM_RSTST0 | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | C2 | C1 | C0 |
| | | PDCM_RSTST1 | Start | | CH1_SNSDATA1 | | | | | | | | | | | | | | | | CH0_SNSDATA1 | | | | | | | | | | | | | | | | CRC | | |
| | | | S2 | S1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | C2 | C1 | C0 |

## 10.8 Daisy chain mode

The device can be programmed to operate in daisy chain mode by setting the DAISY_CHAIN bit in the PSI5_CFG register. Daisy chain mode can be programmed to operate in either "Simultaneous Sampling Mode", or "Synchronous Sampling Mode" by setting the SS_EN bit to the desired operating mode. In simultaneous sampling mode, the most recent interpolated sensor data sample is latched at $t_{TRIG}$ (rising edge of Sync Pulse). In synchronous sampling mode, the most recent interpolated sensor data sample is latched at the transmission time associated with the programmed sensor address, relative to $t_{TRIG}$ (rising edge of Sync pulse).

When programmed to operate in daisy chain mode, the device follows the procedure:

1. After a power on delay of $t_{RS_PM}$, the device waits for a PSI5 "Set Address" command defined in Table 281. Daisy chain programming commands and responses and Table 282. Daisy chain programming response code definitions.
   a. The Set Address command must be preceded by at least 31 and no more than 60 consecutive sync pulses. All other commands must be preceded by either 31 consecutive sync pulses or 5 consecutive missing sync pulses.
   b. The Daisy Chain Programming command and response formats are defined in Section 10.10.2: PSI5 programming mode - data link layer using a sync pulse period of $t_{s\text{-}s_DC}$. The response settings are defined in Table 295. Programming mode via PSI5 response message settings, with the exception of the time slot.
   c. The response to the PSI5 Set Address command and all other valid commands uses the Source ID 0, address-based time slot specified in Table 283. Valid daisy chain addresses.
   d. If a framing error or CRC error is detected on a received command, the device does not respond.
2. After receiving a valid address and completing the response, the device will decode and respond to all Table 281. Daisy chain programming commands and responses commands sent to the sensor address it is set to. All responses are transmitted in the address-based time slot specified in Table 283. Valid daisy chain addresses.
3. When the "Run Mode" command is received, the device responds to the command using the address-based time slot(s) specified in Table 283. Valid daisy chain addresses. The device then ignores all commands and proceeds through Initialization Phase 2 and Initialization Phase 3 in response to sync pulses. The following response format is used, regardless of the state of the relevant bits in the Device Configuration Registers:

**Table 280. Daisy chain: Run mode configuration**

| Parameter | Reference | Value |
|---|---|---|
| Time Slot | Section 8.2.18.1: Periodic data collection mode response start time (PDCM_RSPSTx[12:0]) | Address-based time slot(s) specified in Table 283. Valid daisy chain addresses |
| Data Size | Section 8.2.13.2: PDCM format control bits (PDCMFORMAT[2:0]) | Data size controlled by the PDCMFORMAT bits |
| Error Checking | Section 8.2.17.6: PSI5 response message error detection selection bit (P_CRC) | Even Parity |
| Baud Rate | Section 8.2.15.4: Chip time (CHIPTIME) | Baud Rate controlled by the CHIPTIME bits |

- Upon completion of Initialization Phase 3, the ENDINIT bit is set, the device enters normal mode and responds to all sync pulses with sensor data according to Table 281. Daisy chain programming commands and responses,Table 282. Daisy chain programming response code definitions, and Table 283. Valid daisy chain addresses.

**Table 281. Daisy chain programming commands and responses**

| CMD type | SAdr | | | FC | | | Command | Response (OK) | |
|---|---|---|---|---|---|---|---|---|---|
| | A2 | A1 | A0 | F2 | F1 | F0 | | RC | RD1 |
| Short | 0 | 0 | 0 | A2 | A1 | A0 | Set Sensor Address (Daisy Chain) | OK | SAdr |
| Short | 1 | 1 | 1 | 0 | 0 | 0 | Broadcast Message - "Run Mode" | OK | 0x000 |
| Short | SAdr = 1, 2, 3, 4, 5, 6 | | | 0 | 0 | 0 | Activate Low Side Bus Switch | OK | 0x000 |
| Short | SAdr = 1, 2, 3, 4, 5, 6 | | | 1 | 1 | 1 | Deactivate Low Side Bus Switch | OK | 0x111 |
| Short | SAdr = 1, 2, 3, 4, 5, 6 | | | A2 | A1 | A0 | Set Sensor Address (Daisy Chain) | OK | SAdr |

**Table 282. Daisy chain programming response code definitions**

| Response code | Definition | Value |
|---|---|---|
| RC = OK | Command Message Received Properly. | 0x1E1 |
| RC = Error | Error during transmission of Command Message. | 0x1E2 |
| SAdr | Programmed Sensor Address, prepended with logic zeros. | Varies |

**Table 283. Valid daisy chain addresses**

| Sensor address (SAdr) | | | Description | Time slot Source ID 0 |
|---|---|---|---|---|
| A2 | A1 | A0 | | |
| 0 | 0 | 0 | Un-programmed sensor | N/A |
| 0 | 0 | 1 | Sensor Address 1 | $t_{TIMESLOT\_DC0}$ |
| 0 | 1 | 0 | Sensor Address 2 | $t_{TIMESLOT\_DC1\_L}$ |
| 0 | 1 | 1 | Sensor Address 3 | $t_{TIMESLOT\_DC2\_L}$ |
| 1 | 0 | 0 | Sensor Address 4 | $t_{TIMESLOT\_DC1\_H}$ |
| 1 | 0 | 1 | Sensor Address 5 | $t_{TIMESLOT\_DC2\_H}$ |
| 1 | 1 | 0 | Sensor Address 6 | $t_{TIMESLOT\_DC3\_H}$ |
| 1 | 1 | 1 | N/A | N/A |

| Sensor address (SAdr) | | | Description | Time slot source ID 0 | Time slot source ID 2 |
|---|---|---|---|---|---|
| A2 | A1 | A0 | | | |
| 0 | 0 | 0 | Un-programmed sensor | N/A | N/A |
| 0 | 0 | 1 | Sensor Address 1 | $t_{TIMESLOT\_DC0}$ | $t_{TIMESLOT\_DC1\_L}$ |
| 0 | 1 | 0 | Sensor Address 2 | $t_{TIMESLOT\_DC1\_L}$ | $t_{TIMESLOT\_DC2\_L}$ |
| 0 | 1 | 1 | Sensor Address 3 | $t_{TIMESLOT\_DC2\_L}$ | $t_{TIMESLOT\_DC0}$ |
| 1 | 0 | 0 | Sensor Address 4 | $t_{TIMESLOT\_DC1\_H}$ | $t_{TIMESLOT\_DC2\_H}$ |
| 1 | 0 | 1 | Sensor Address 5 | $t_{TIMESLOT\_DC2\_H}$ | $t_{TIMESLOT\_DC3\_H}$ |
| 1 | 1 | 0 | Sensor Address 6 | $t_{TIMESLOT\_DC3\_H}$ | $t_{TIMESLOT\_DC0}$ |
| 1 | 1 | 1 | N/A | N/A | N/A |

*Note: Writes to Sensor Address 7 are ignored.*

*Note: If a successful programming mode entry command is received prior to a set address, daisy chain mode is disabled.*

## 10.9 Error handling

### 10.9.1 Daisy chain error handling

Table 284. Daisy chain error handling shows the effect of internal failure modes on the daisy chain initialization procedure.

**Table 284. Daisy chain error handling**

| Error condition | Effect on daisy chain |
|---|---|
| Supply Error | Daisy chain commands ignored. The device will not participate in daisy chain. |
| Communication Error | No effect. The device will participate in Daisy Chain as programmed. |
| Test Mode Enabled | Daisy chain commands ignored. The device will not participate in daisy chain. |
| Offset Error | No effect. The device will participate in daisy chain as programmed. |
| Temperature Error | No effect. The device will participate in daisy chain as programmed. |
| Memory Error | No effect. The device will participate in daisy chain as programmed. |
| Self-test Error | No effect. The device will participate in daisy chain as programmed. |
| Device Not Locked | No effect. The device will participate in daisy chain as programmed. |

### 10.9.2 Initialization phase 2 error handling

Table 285. Initialization phase 2 error handling shows the effect of internal failure modes on the initialization phase 2 transmissions. Some errors occurring in initialization phase 2 will prevent entry into initialization phase 3. Once the error is no longer present, the device will complete initialization phase 2 as necessary and then transition to initialization phase 3.

**Table 285. Initialization phase 2 error handling**

| Error condition | Effect on initialization phase 2 |
|---|---|
| Supply Error | Temporary, Sync Pulses Ignored |
| Communication Error | No Effect |
| Test Mode Enabled | No Effect |
| Offset Error | No Effect |
| Temperature Error | No Effect. The device will attempt to transmit Initialization Phase 2 data. |
| Memory Error | No Effect. The device will attempt to transmit Initialization Phase 2 data. |
| Self-test Error | No Effect |
| Device Not Locked | No Effect |

### 10.9.3 Initialization phase 3 error handling

Table 286. Initialization phase 3 error handling shows the effect of internal failure modes on the initialization phase 3 procedures. Some errors occurring in initialization phase 3 will prevent entry into run mode until the error is no longer present. Once the error is no longer present, one or more Sensor Ready commands are transmitted before entering Run Mode.

**Table 286. Initialization phase 3 error handling**

| Error condition | Effect on initialization phase 3 |
|---|---|
| Supply Error | Temporary, Sync Pulses Ignored |
| Communication Error | No Effect |
| Test Mode Enabled | No Effect |
| Offset Error | No Effect |

| Error condition | Effect on initialization phase 3 |
|---|---|
| Temperature Error | No Effect. The device will attempt to transmit Initialization Phase 3 data. |
| Memory Error | No Effect. The device will attempt to transmit Initialization Phase 3 data. |
| Self-test Error | No Effect |
| Device Not Locked | Sensor Ready replaced with Sensor Ready, but Not Locked Transmission (UF2 Region is un-programmed) |

### 10.9.4 Normal mode error handling with internal error automatic clearing

Section 10.9.4.1: Standard error reporting and Section 10.9.4.2: PSI5 error extension option summarize the error reporting if the PSI5_ERRLATCH bit is not set. A single error transmission clears the device status allowing for temporary error conditions to be cleared once the error condition is removed.

#### *10.9.4.1 Standard error reporting*

Table 287. Standard error reporting summarizes the error reporting in normal mode if the PSI5 error extension option is disabled.

**Table 287. Standard error reporting**

| Error condition | Error code | Error response |
|---|---|---|
| Supply Error | NA | Temporary (Normal transmissions continue once condition is removed) |
| Communication Error | 0x1F4 | Temporary (Normal transmissions continue once condition is removed) |
| Test Mode Enabled | | Temporary (Normal transmissions continue once condition is removed) |
| Offset Error | | Temporary (Normal transmissions continue once condition is removed)(1) |
| Temperature Error | | Temporary (Normal transmissions continue once condition is removed) |
| Memory Error | | Latched until reset |
| Self-test Error | 0x1EA | Latched until reset(2) |
| Device Not Locked | NA | NA |

1. *An offset error on either channel results in an offset error response from both channels.*
2. *A self-test error on either channel results in a self-test error response from both channels.*

#### *10.9.4.2 PSI5 error extension option*

If the PSI5 error extension option is enabled, additional error reporting is available as shown in Table 288. PSI5 error extension option.

**Table 288. PSI5 error extension option**

| Error condition | Error code | Error response |
|---|---|---|
| Supply Error | NA | Temporary (Normal transmissions continue once condition is removed) |
| Communication Error | 0x1EF | Temporary (Normal transmissions continue once condition is removed) |
| Test Mode Enabled | 0x1EE | Temporary (Normal transmissions continue once condition is removed) |
| Offset Error | 0x1ED | Temporary (Normal transmissions continue once condition is removed)(1) |
| Temperature Error | 0x1EC | Temporary (Normal transmissions continue once condition is removed) |
| Memory Error | 0x1EB | Latched until reset |
| Self-test Error | 0x1EA | Latched until reset(2) |
| Device Not Locked | NA | NA |

1. *An offset error on either channel results in an offset error response from both channels.*
2. *A self-test error on either channel results in a self-test error response from both channels.*

### 10.9.5 Normal mode error handling with internal error latching

Section 10.9.5.1: Standard error reporting and Section 10.9.5.2: PSI5 error extension option summarize the error reporting if the PSI5_ERRLATCH bit is set. Internal errors are latched until reset.

#### *10.9.5.1 Standard error reporting*

Table 289. Standard error reporting summarizes the error reporting in normal mode if the PSI5 Error Extension option is disabled.

**Table 289. Standard error reporting**

| Error condition | Error code | Error response |
|---|---|---|
| Supply Error | NA | Temporary (Normal transmissions continue once condition is removed) |
| Communication Error | 0x1F4 | Temporary (Normal transmissions continue once condition is removed) |
| Test Mode Enabled | | Latched until reset |
| Offset Error | | Latched until reset.(1) |
| Temperature Error | | Latched until reset |
| Memory Error | | Latched until reset |
| Self-test Error | 0x1EA | Latched until reset.(2) |
| Device Not Locked | NA | NA |

1. *An offset error on either channel results in an offset error response from both channels.*
2. *A self-test error on either channel results in a self-test error response from both channels.*

#### *10.9.5.2 PSI5 error extension option*

If the PSI5 error extension option is enabled, additional error reporting is available as shown in Table 290. PSI5 error extension option.

**Table 290. PSI5 error extension option**

| Error condition | Error code | Error response |
|---|---|---|
| Supply Error | NA | Temporary (Normal transmissions continue once condition is removed) |
| Communication Error | 0x1EF | Temporary (Normal transmissions continue once condition is removed) |
| Test Mode Enabled | 0x1EE | Latched until reset |
| Offset Error | 0x1ED | Latched until reset.(1) |
| Temperature Error | 0x1EC | Latched until reset |
| Memory Error | 0x1EB | Latched until reset |
| Self-test Error | 0x1EA | Latched until reset.(2) |
| Device Not Locked | NA | NA |

1. *An offset error on either channel results in an offset error response from both channels.*
2. *A self-test error on either channel results in a self-test error response from both channels.*

## 10.10 PSI5 programming mode

PSI5 Programming mode is a synchronous communication mode that allows for bidirectional communication with the device. Programming mode is intended for factory programming of the OTP array and reading of diagnostic information. It is not intended for use in normal operation.

### 10.10.1 PSI5 programming mode entry

The device enters programming mode if and only if the following sequence occurs:

1. At least 31 sync pulses are detected, directly preceding the Programming Mode Entry Short Command during the Programming Mode Entry Window shown in Figure 89. PSI5 initialization timing, synchronous mode.
   – The window timing is defined in Section 7.13: Dynamic electrical characteristics - PSI5 ($t_{PME}$).
   – The Sync pulses and Programming Mode Entry command must be received with a sync pulse period of $t_{S\text{-}S\_PM}$

If the Programming Mode entry requirement is not met:

1. Programming Mode Entry is blocked until the device is reset.
2. The device proceeds with PSI5 Initialization Phase 2, and PSI5 Initialization Phase 3.
3. The device enters normal mode, and responds as programmed to normal sync pulses.

If the Programming Mode entry requirement is met:

1. Normal transmissions to sync pulses are terminated.
2. The device will detect commands if the start condition is met as described in Section 10.10.2.2: PSI5 programming mode - command message format.
3. The device responds only to valid PSI5 Short and XLong Commands addressed to Sensor Address '001', as defined in Section 10.10.3: PSI5 programming mode command and response summary.

## 10.10.2 PSI5 programming mode - data link layer

### *10.10.2.1 PSI5 programming mode - command bit encoding*

Commands messages are transmitted via the modulation of the supply voltage. The presence of a sync pulse is a logic '1' and the absence of a sync pulse is a logic '0'. Sync pulses are expected at a rate of $t_{S\text{-}S\_PM}$.

### *10.10.2.2 PSI5 programming mode - command message format*

Once programming mode is enabled, command message data frames consist of a start condition, 3 Start Bits (S[2:0]), a 3-bit sensor address (SAdr[2:0]), a 3-bit function code (FC[2:0]), an optional register address (RAdr[7:0]), an optional data field (D[7:0]), and a 3-bit CRC (C[2:0]. The start condition consists of one of the following:

1. A minimum of 5 consecutive logic '0's (with no sync bits)
2. A minimum of 31 consecutive logic '1's (this includes logic '1's transmitted for the previous response)

The command message format is shown in Table 292. Programming mode via PSI5 command data format - response.

**Table 291. Programming mode via PSI5 command data format**

| Start bits | | | Sensor Addr | | | Function code | | | Register address | | | | | | | | | | | Data | | | | CRC | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S2 | S1 | S0 | SA0 | SA1 | SA2 | FC0 | FC1 | FC2 | RA0 | RA1 | RA2 | RA3 | RA4 | RA5 | RA6 | RA7 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | C2 | C1 | C0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| | | | | | | | | | | | | | | | | | | | | | | | | | CRC | | |
| | | | | | | | | | | | | | | | | | Data to be written to register (optional) | | | | | | | | | | |
| | | | | | | | | | Register Address (optional) | | | | | | | | | | | | | | | | | | |
| | | | | | | Function Codes (See Section 10.10.3: PSI5 programming mode command and response summary) | | | | | | | | | | | | | | | | | | | | | |
| | | | Sensor Address - Fixed at 001 | | | | | | | | | | | | | | | | | | | | | | | | |
| Start Bit Sequence = 010 | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Table 292. Programming mode via PSI5 command data format - response**

| Response | | |
|---|---|---|
| RC | RD1 | RD0 |
| $3FF | $3FF | $3FF |

Bit stuffing is necessary to maintain a synchronized timebase between the command master and the device. A logic '1' Sync bit is added every fourth bit in the command message to ensure that there will never be more than 3 logic '0' bits in a row.

**Table 293. Programming mode via PSI5 XLONG command data format with sync bits**

| Start bits | | | | Sensor address | | | | Function code | | | | Register address | | | | | | | | | Data | | | | | | | | | | | CRC | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S2 | S1 | S0 | Sy | SA0 | SA1 | SA2 | Sy | FC0 | FC1 | FC2 | Sy | RA0 | RA1 | RA2 | Sy | RA3 | RA4 | RA5 | Sy | RA6 | RA7 | D0 | Sy | D1 | D2 | D3 | Sy | D4 | D5 | D6 | Sy | D7 | C2 | C1 | Sy | C0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |

**Table 294. Programming mode via PSI5 XLONG command data format with sync bits - response**

| Response | | |
|---|---|---|
| RC | RD1 | RD0 |
| $1E2 | $3FF | $3FF |

Once a command is received and verified, the device expects 2 to 3 consecutive sync pulses (depending upon the command message lengths described in Table 295. Programming mode via PSI5 response message settings). There is no delay restriction between the command and the first sync pulse for the response. Once the first sync pulse for the response is received, each successive response sync pulse must be received within the programming mode sync pulse period specified ($t_{S\text{-}S\_PM}$) or a framing error may occur.

For each of these sync pulses, The device will respond with the following settings:

**Table 295. Programming mode via PSI5 response message settings**

| Parameter | Value |
|---|---|
| Time Slot | $t_{TIMESLOT\_DC0}$ |
| Data Size | 10-bit data |
| Error Checking | Even Parity |
| Baud Rate | 125 kBd |
| Sync Pulse Pulldown | Disabled |

### 10.10.2.3 *Short frame command and response format*

Short frames are the simplest type of command message. No data is transmitted in a short frame command. Only specific instructions are performed in response to short frame commands. The short frame format is shown in Table 296. Programming mode via PSI5 short command. Short frame commands and responses are defined in Section 10.10.3: PSI5 programming mode command and response summary.

The device only supports a short command for programming mode entry.

**Table 296. Programming mode via PSI5 short command**

| Start bits | | | | Sensor address | | | | Function code | | | | CRC | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S2 | S1 | S0 | Sy | SA0 | SA1 | SA2 | Sy | FC0 | FC1 | FC2 | Sy | C2 | C1 | C0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

**Table 297. Response format**

| Response | |
|---|---|
| RC | RD1 |
| $1E2 | $3FF |

### 10.10.2.4 *Long frame command and response format*

Long frames allow for the transmission of data nibbles for register writes. The device can provide register data in response to a read or write request. the long frame format is shown in Table 298. Programming mode via PSI5 long command. The device does not support the long frame command.

**Table 298. Programming mode via PSI5 long command**

| Start Bits | | | | Sensor Address | | | | Function Code | | | | Register Address | | | | | | | | Data | | | | | | CRC | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S2 | S1 | S0 | Sy | SA0 | SA1 | SA2 | Sy | FC0 | FC1 | FC2 | Sy | RA0 | RA1 | RA2 | Sy | RA3 | RA4 | RA5 | Sy | D0 | D1 | D2 | Sy | D3 | C2 | C1 | Sy | C0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |

**Table 299. Response format**

| Response | | |
|---|---|---|
| RC | RD1 | RD0 |
| $1E2 | $3FF | $3FF |

### 10.10.2.5 *Extra long frame command and response format*

Extra long frames allow for the transmission of address and data bytes for register reads and writes. The device can provide register data in response to a read or write request. The extra long frame format is shown in Table 300. Programming mode via PSI5 long command. Extra long frame commands and responses are defined in Section 10.10.3: PSI5 programming mode command and response summary.

The device supports register read and register write extra long commands.

**Table 300. Programming mode via PSI5 long command**

| Start Bits | | | | Sensor Address | | | | Function Code | | | | Register Address | | | | | | | | | Data | | | | | | | | | CRC | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S2 | S1 | S0 | Sy | SA0 | SA1 | SA2 | Sy | FC0 | FC1 | FC2 | Sy | RA0 | RA1 | RA2 | Sy | RA3 | RA4 | RA5 | Sy | RA6 | RA7 | D0 | Sy | D1 | D2 | D3 | Sy | D4 | D5 | D6 | Sy | D7 | C2 | C1 | Sy | C0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |

**Table 301. Response format**

| Response | | |
|---|---|---|
| RC | RD1 | RD0 |
| $1E2 | $3FF | $3FF |

### 10.10.2.6 *Command message CRC*

Programming mode command error checking is accomplished by a 3-bit CRC. The 3-bit CRC is calculated using all message bits except start bits and sync bits. The CRC verification uses a generator polynomial of g(x) = $X^3$+X+1, with a non-direct seed value = '111'. The message data is provided to the CRC calculator in the order received (LSB first, SAdr, FC, RAdr, Data), and then augmented with '000'. Table 266. PSI5 3-bit CRC calculation examples shows some example CRC calculation values for 10-bit data transmissions.

The calculated CRC is then compared against the received 3-bit CRC (received MSB first). If a CRC mismatch is detected, the device responds with a CRC Error response as defined in Section 10.10.4: Programming mode via PSI5 error response summary.

### 10.10.2.7 *Command sync pulse blanking time*

In programming mode and programming mode entry, the device employs a fixed sync pulse blanking time of $t_{SYNC\_OFF\_250}$ regardless of the state of the PDCM_CMD_B register value.

### 10.10.2.8 *Command timeout*

In the event that the device does not detect a sync pulse within a 4-bit window time, the command reception will be terminated and the device will respond to the next sync pulse with a Short Frame Framing Error response as defined in Section 10.10.4: Programming mode via PSI5 error response summary.

### 10.10.3 PSI5 programming mode command and response summary

**Table 302. Programming mode via PSI5 commands and responses**

| CMD type | SAdr | FC FC[2:0] | Command | Register address | Data field | Response (OK) | | | Response (Error) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | RC | RD1 | RD0 | RC | RD1 | RD0 |
| Short | 001 | 100 | Invalid Command | N/A | N/A | No Response | | | No Response | | |
| Short | | 101 | Invalid Command | N/A | N/A | No Response | | | No Response | | |
| Short | | 110 | Invalid Command | N/A | N/A | No Response | | | No Response | | |
| Short | | 111 | Enter Programming Mode | N/A | N/A | OK | 0x0CA | N/A | No Response | | |
| Long | | 010 | Invalid Command | N/A | N/A | No Response | | | No Response | | |
| Long | | 011 | Invalid Command | N/A | N/A | No Response | | | No Response | | |
| XLong | | 000 | Read register located at address RA7:RA0 | Varies | Varies | OK | RData | RData+1 | Error | ErrN | 0x000 |
| XLong | | 001 | Write WData to register RA7:RA0 | Varies | Varies | OK | WData | RA7:RA0 | Error | ErrN | 0x000 |

**Table 303. Programming mode via PSI5 response code definitions**

| Response code | Definition | Value |
|---|---|---|
| RC = OK | Command Message Received Properly | 0x1E1 |
| RC = Error | Error during transmission of Command Message | 0x1E2 |
| RData | Byte Contents of Register located at address RA7:RA1 with RA0 = 0 (Low Byte) | Varies |
| RData + 1 | Byte Contents of Register located at address RA7:RA1 with RA0 = 1 (High Byte) | Varies |
| WData | Byte Contents of Register located at address RA7:RA0 | Varies |

### 10.10.4 Programming mode via PSI5 error response summary

**Table 304. Error response summary**

| ErrN | Mnemonic | Description | Supported |
|---|---|---|---|
| 0000 | General | General Error | No |
| 0001 | Framing | Framing Error (4 consecutive zeros) | Yes |
| 0010 | CRC | CRC Error on Received Message | Yes |
| 0011 | Address | Sensor Address Not Supported | No (Invalid Address is ignored) |
| 0100 | FC | Function Code Not Supported | No (N/A) |
| 0101 | Reserved | Reserved | No |
| 0110 | | | |
| 0111 | | | |
| 1000 | Reserved | Reserved | No |
| 1001 | | | |
| 1010 | | | |
| 1011 | | | |
| 1100 | | | |
| 1101 | | | |
| 1110 | | | |
| 1111 | | | |

ErrN is transmitted in the 4 LSBs of RD1. All other bits in the response data field are set to '0'.

## 10.11 PSI5 OTP programming procedure

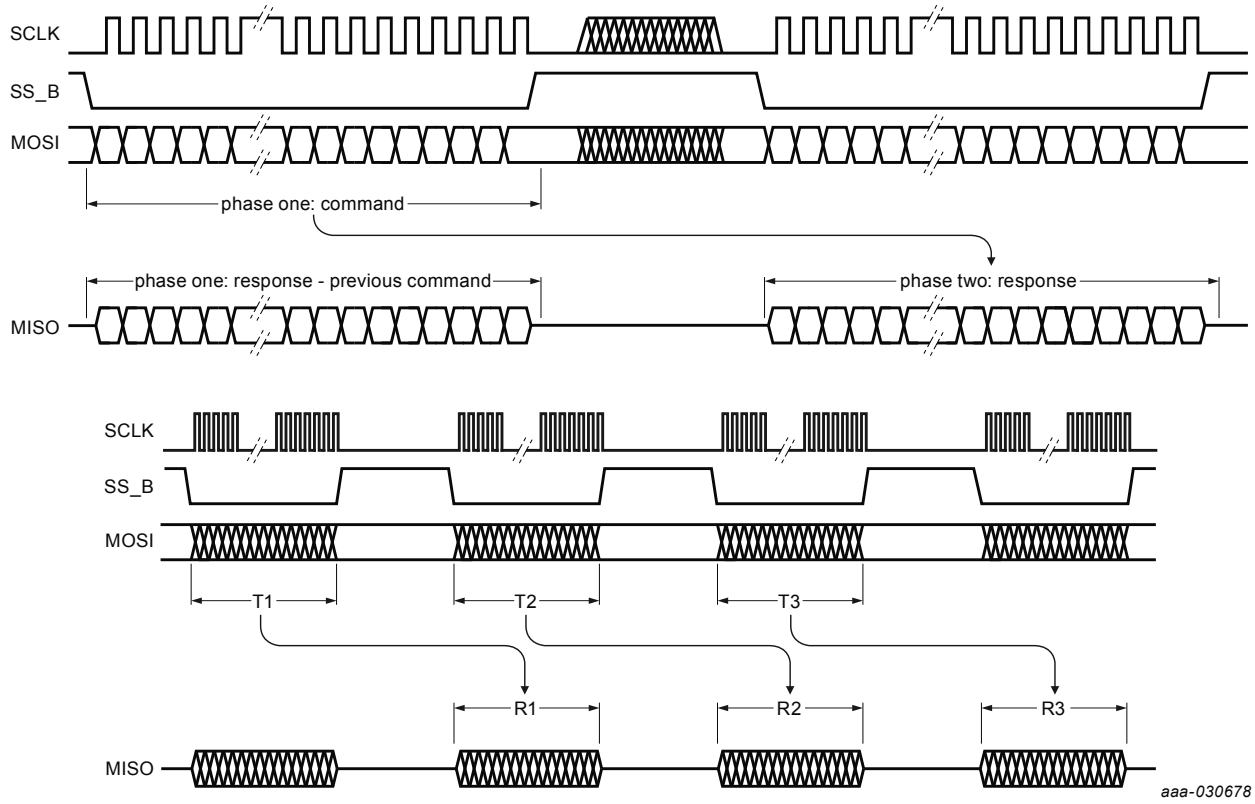
1. Enter programming mode.
2. Set $V_{CC} = V_{PP}$
3. Load desired data into the desired registers using PSI5 Write commands.
4. Write the necessary OTP program sequence to the WRITE_OTP_EN register for the desired OTP region to be written.
5. Delay $t_{PROG\_TIME}$ after the completion of the Write OTP program to allow for completion of the OTP writes.
6. Read the DEVSTAT and DEVSTAT2 registers to confirm that no errors occurred during the OTP writes.
7. Read back the register values that were written and compare to the desired values to confirm successful OTP writes.

Refer to the PSI5 OTP Programming Procedure Application Note for further details on OTP programming.

# 11 Standard 32-bit SPI protocol

The device includes a standard SPI protocol requiring 32-bit data packets. The device is a slave device requires that the base clock value be low (CPOL = 0) with data captured on the rising edge of the clock and data propagated on the falling edge of the clock (CPHA = 0). The most significant bit is transferred first (MSB first). SPI transfers are completed through a sequence of two phases. During the first phase, the command is transmitted from the SPI master to the device. During the second phase, response data is transmitted from the slave device. MOSI and SCLK transitions are ignored when SS_B is not asserted.

**Figure 94. Standard 32-bit SPI protocol timing diagram**




## 11.1 SPI command format

**Table 305. SPI command format**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Register Access Command | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Fixed Bits: Must = 0x0 | | | | Register Address | | | | | | | | Register Data | | | | | | | | 8-bit CRC | | | | | | | |
| C[3:0] | | | | 0 | 0 | 0 | 0 | RA[7:1] | | | | | | | RA[0] | RD[7:0] | | | | | | | | CRC[7:0] | | | | | | | |
| Sensor Data Command | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Fixed Bits: Must = 0x00000 | | | | | | | | | | | | | | | | | | | | 8-bit CRC | | | | | | | |
| C[3:0] | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CRC[7:0] | | | | | | | |

## 11.2 SPI response format

**Table 306. SPI response format**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Response to Register Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Unused Data = 0x0 | | Register Data: Contents of RA[7:1] High Byte | | | | | | | | Register Data: Contents of RA[7:1] Low Byte | | | | | | | | 8-bit CRC | | | | | | | |
| C[0] | C[3] | C[2] | C[1] | ST[1:0] | | 0 | 0 | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | CRC[7:0] | | | | | | | |
| Response to Sensor Data Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Sensor Data | | | | | | | | | | | | | | | | Detail Status | | 8-bit CRC | | | | | | | |
| C[0] | C[3] | C[2] | C[1] | ST[1:0] | | SD[11:0] | | | | | | | | | | | | Optional SD resolution | | | | SF[1:0] | | CRC[7:0] | | | | | | | |
| Error Response to Register Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Unused Data = 0x0 | | Register Data: Contents of RA[7:1] High Byte | | | | | | | | Register Data: Contents of RA[7:1] Low Byte | | | | | | | | 8-bit CRC | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | CRC[7:0] | | | | | | | |
| Error Response to Sensor Data Request With Sensor Data | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Sensor Data | | | | | | | | | | | | | | | | Detail Status | | 8-bit CRC | | | | | | | |
| C[0] | C[3] | C[2] | C[1] | 1 | 1 | SD[11:0] | | | | | | | | | | | | Optional SD resolution | | | | SF[1:0] | | CRC[7:0] | | | | | | | |
| Error Response to Sensor Data Request Without Sensor Data | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | x | Unused Data = 0x0000 | | | | | | | | | | | | | | | Detail Status | | 8-bit CRC | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SF[1:0] | | CRC[7:0] | | | | | | | |

## 11.3 Command summary

**Table 307. Command summary**

| C[3:0] | | | | Command type | Data source SOURCEID[2:0] = C[3:1] | Reference |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Unused Command (Reserved for Error Response) | Not Applicable | Not Applicable |
| 0 | 0 | 0 | 1 | Sensor Data Request | SOURCEID[3:0] = 0x0 | Section 11.3.3: Sensor data request commands |
| 0 | 0 | 1 | 0 | Reserved Command | Not Applicable | Not Applicable |
| 0 | 0 | 1 | 1 | Sensor Data Request | SOURCEID[3:0] = 0x1 | Section 11.3.3: Sensor data request commands |
| 0 | 1 | 0 | 0 | Reserved Command | Not Applicable | Not Applicable |
| 0 | 1 | 0 | 1 | Sensor Data Request | SOURCEID[3:0] = 0x2 | Section 11.3.3: Sensor data request commands |
| 0 | 1 | 1 | 0 | Reserved Command | Not Applicable | Not Applicable |
| 0 | 1 | 1 | 1 | Sensor Data Request | SOURCEID[3:0] = 0x3 | Section 11.3.3: Sensor data request commands |
| 1 | 0 | 0 | 0 | Register Write Request | Not Applicable | Section 11.3.2: Register write command |
| 1 | 0 | 0 | 1 | Sensor Data Request | SOURCEID[3:0] = 0x4 | Section 11.3.3: Sensor data request commands |
| 1 | 0 | 1 | 0 | Reserved Command | Not Applicable | Not Applicable |
| 1 | 0 | 1 | 1 | Sensor Data Request | SOURCEID[3:0] = 0x5 | Section 11.3.3: Sensor data request commands |
| 1 | 1 | 0 | 0 | Register Read Request | Not Applicable | Section 11.3.1: Register read command |

| C[3:0] | | | | Command type | Data source<br>SOURCEID[2:0] = C[3:1] | Reference |
|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | Sensor Data Request | SOURCEID[3:0] = 0x6 | Section 11.3.3: Sensor data request commands |
| 1 | 1 | 1 | 0 | Reserved Command | Not Applicable | Not Applicable |
| 1 | 1 | 1 | 1 | Sensor Data Request | SOURCEID[3:0] = 0x7 | Section 11.3.3: Sensor data request commands |

### 11.3.1 Register read command

The device supports a Register Read command. The Register Read command uses the upper 7 bits of the addresses defined in Section 8.1: User accessible data array to address two 8-bit registers in the register map. The response to the command includes the con-tents of RA[7:1] high byte (RA[0] = 1) in the upper byte and the contents of RA[7:1] low byte (RA[0] = 0) in the lower byte.

The response to a register read command is shown in Section 11.3.1.2: Register read response message format. The response is transmitted on the next SPI message if and only if all of the following conditions are met:

- No SPI Error is detected (See Section 11.5.6: SPI error)
- No MISO Error is detected (See Section 11.5.7: SPI data output verification error)

If the conditions are met, the device responds to the register read request as shown in Section 11.3.1.2: Register read response message format. Otherwise, the device responds with the Error Response as defined in Section 11.5.4: Alternative detailed status field reporting. The Register Read response includes the register contents at the rising edge of SS_B for the Register Read command.

#### *11.3.1.1 Register read command message format*

**Table 308. Register read command message format**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command C[3:0] | | | | Fixed Bits: Must = 0x0 | | | | Register Address | | | | | | | | Register Data | | | | | | | | 8-bit CRC | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | RA[7:1] | | | | | | | RA[0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CRC[7:0] | | | | | | | |

**Table 309. Register read command message format description**

| Bit field | Definition |
|---|---|
| C[3:0] | Register Read Command = '1100' |
| RA[7:1] | RA[7:1] contains the word address of the register to be read. |
| CRC[7:0] | CRC. See Section 11.4: Error checking |

#### *11.3.1.2 Register read response message format*

**Table 310. Register read response message format**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command C[0], [3:1] | | | | Basic Status | | Unused Data = 0x0 | | Register Data: Contents of RA[7:1] High Byte | | | | | | | | Register Data: Contents of RA[7:1] Low Byte | | | | | | | | 8-bit CRC | | | | | | | |
| 0 | 1 | 1 | 0 | | | 0 | 0 | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | CRC[7:0] | | | | | | | |

**Table 311. Register read response message format description**

| Bit field | Definition |
|---|---|
| C[0], [3:1] | Register Read Command = '0110' |

| Bit field | Definition |
|---|---|
| ST[1:0] | Status. See Section 11.5.1: Standard basic status reporting field |
| RD[15:8] | The contents of the register addressed by RA[7:1] High Byte (RA[0] = 1) |
| RD[7:0] | The contents of the register addressed by RA[7:1] Low Byte (RA[0] = 0) |
| CRC[7:0] | CRC. See Section 11.4: Error checking |

### 11.3.2 Register write command

The device supports a Register Write command. The Register Write command writes the value specified in RD[7:0] to the register addressed by RA[7:0]. The response to the command includes the new contents of RA[7:1] high byte (RA[0] = 1) in the upper byte and the contents of RA[7:1] low byte (RA[0] = 0) in the lower byte.

The response to a register write command is shown in Section 11.3.2.2: Register write response message format. The register write is executed and a response is transmitted on the next SPI message if and only if all of the following conditions are met:

- No SPI Error is detected (See Section 11.5.6: SPI error)
- The ENDINIT bit is cleared
  - This applies to all registers with the exception of the RESET[1:0] bits in the DEVLOCK_WR register

If the conditions are met, the register write is executed and the device responds to the register write request as shown in Section 11.3.2.2: Register write response message format. Otherwise, no register is written and the device responds with the Error Response as defined in Section 11.2: SPI response format. The register is not written until the transfer during which the register write was requested has been completed.

A register write command to a read-only register will not execute, but will result in a valid response.

#### *11.3.2.1 Register write command message format*

**Table 312. Register write command message format**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command C[3:0] | | | | Fixed Bits: Must = 0x0 | | | | Register Address | | | | | | | | Register Data | | | | | | | | 8-bit CRC | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RA[7:1] | | | | | | | RA[0] | RD[7:0] | | | | | | | | CRC[7:0] | | | | | | | |

**Table 313. Register write command message format description**

| Bit field | Definition |
|---|---|
| C[3:0] | Register Write Command = '1000' |
| RA[7:0] | RA[7:1] contains the byte address of the register to be written. |
| RD[7:0] | RD[7:0] contains the data byte to be written to address RA[7:0] |
| CRC[7:0] | CRC. See Section 11.4: Error checking |

#### *11.3.2.2 Register write response message format*

**Table 314. Register write response message format**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command C[0], [3:1] | | | | Basic Status | | Unused Data = 0x0 | | Register Data: Contents of RA[7:1] High Byte | | | | | | | | Register Data: Contents of RA[7:1] Low Byte | | | | | | | | 8-bit CRC | | | | | | | |
| 0 | 1 | 0 | 0 | ST[1:0] | | 0 | 0 | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | CRC[7:0] | | | | | | | |

**Table 315. Register write response message format description**

| Bit field | Definition |
|---|---|
| C[0], [3:1] | Register Write Command = '0100' |
| ST[1:0] | Status. See Section 11.5.1: Standard basic status reporting field |
| RD[15:8] | The contents of the register addressed by RA[7:1] High Byte (RA[0] = 1) |
| RD[7:0] | The contents of the register addressed by RA[7:1] Low Byte (RA[0] = 0) |
| CRC[7:0] | CRC. See Section 11.4: Error checking |

### 11.3.3 Sensor data request commands

The device supports standard sensor data request commands. The sensor data request command format is described in Section 11.3.3.1: Sensor data request command message format. The response to a sensor data request is shown in Section 11.3.3.2: Sensor data request response message format. The response is transmitted on the next SPI message subject to the error handling conditions specified in Section 11.5: Exception handling. The sensor data included in the response is the sensor data at the falling edge of SS_B for the Sensor Data Request response.

#### *11.3.3.1 Sensor data request command message format*

**Table 316. Sensor data request command message format**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | | | | Fixed Bits: Must = 0x00000 | | | | | | | | | | | | | | | | | | | | 8-bit CRC | | | | | | | |
| C[3:0] | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CRC[7:0] | | | | | | | |

**Table 317. Sensor data request command message format description**

| Bit field | Definition |
|---|---|
| C[0] | Sensor Data Request Command = '1' |
| C[3:1] = SOURCEID[2:0] | Source Identification code for the requested sensor data. See Section 8.2.13: Source identification registers (SOURCEID_x). |
| CRC[7:0] | CRC. See Section 11.4: Error checking |

#### *11.3.3.2 Sensor data request response message format*

**Table 318. Sensor data request response message format**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command C[0], [3:1] | | | | Basic Status | | Sensor Data | | | | | | | | | | | | | | | | Detail Status | | 8-bit CRC | | | | | | | |
| 1 | C[3] | C[2] | C[1] | ST[1:0] | | SD[11:0] | | | | | | | | | | | | Optional SD resolution | | | | SF[1:0] | | CRC[7:0] | | | | | | | |

**Table 319. Sensor data request response message format description**

| Bit field | Definition |
|---|---|
| C[0] | Sensor Data Request Command = '1' |
| C[3:1] = SOURCEID[2:0] | Source Identification code for the requested sensor data. See Section 8.2.13: Source identification registers (SOURCEID_x). |
| ST[1:0] | Basic Status. See Section 11.5.1: Standard basic status reporting field |
| SD[11:0] | Sensor Data. See Section 8.6.4.9: Output scaling |

| Bit field | Definition |
|---|---|
| Optional SD Resolution | Optional for 16-bit Sensor Data. See Section 8.6.4.9: Output scaling |
| SF[1:0] | Detailed Status. See Section 11.5.3: Standard detailed status field reporting |
| CRC[7:0] | CRC. See Section 11.4: Error checking |

### 11.3.4 Reserved commands

The device responds to reserved commands on the next SPI message subject to the error handling conditions specified in Section 11.5: Exception handling.

#### *11.3.4.1 Reserved command message format*

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | | | | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8-bit CRC | | | | | | | |
| 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | |
| 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | |
| 0 | 1 | 0 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | |
| 0 | 1 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | |
| 1 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | |
| 1 | 1 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | |

| Bit field | Definition |
|---|---|
| C[3:0] | Reserved Command |
| CRC[7:0] | CRC. See Section 11.4: Error checking |

#### *11.3.4.2 Reserved command response message format*

**Table 320. Reserved command response message format**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command Echo | | | | Data | | | | | | | | | | | | | | | | | | | | 8-bit CRC | | | | | | | |
| x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | |

**Table 321. Reserved command response message format description**

| Bit field | Definition |
|---|---|
| Command Echo | Reserved Command Echo - Undefined |
| Data | Response Data - Undefined |
| CRC[7:0] | CRC. See Section 11.4: Error checking |

## 11.4 Error checking

### 11.4.1 Default 8-bit CRC

#### *11.4.1.1 Command error checking*

The device calculates an 8-bit CRC on the entire 32-bits of each command. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message. If the calculated CRC does not match the transmitted CRC, the command is ignored and the device responds with the SPI Error response.

The CRC decoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
4. If the shift register contains all zeros, the CRC is correct.
5. If the shift register contains a value other than zero, the CRC is incorrect.

The CRC polynomial and seed are shown in Table 322. SPI command message CRC.

**Table 322. SPI command message CRC**

| SPICRCSEED[3:0] | Default polynomial | Default non-direct seed |
|---|---|---|
| 0000 | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 |
| Non-Zero | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 SPICRCSEED[3:0] |

Some example CRC calculations are shown in Table 324. SPI 8-bit CRC calculation examples.

#### 11.4.1.2 *Response error checking*

The device calculates a CRC on the entire 32-bits of each response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC Encoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds eight zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and seed are shown in Table 323. SPI CRC polynomial and seed.

**Table 323. SPI CRC polynomial and seed**

| SPICRCSEED[3:0] | Default polynomial | Default non-direct seed |
|---|---|---|
| 0000 | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 |
| Non-Zero | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 SPICRCSEED[3:0] |

Some example CRC calculations are shown in Table 324. SPI 8-bit CRC calculation examples.

**Table 324. SPI 8-bit CRC calculation examples**

| Polynomial | Seed | Bits[31:28] | Bits[27:24] | Bits[23:16] | Bits[15:8] | Bits[7:0] |
|---|---|---|---|---|---|---|
| | | Command | 0x0 | Register address | Register data | 8-bit CRC |
| $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 | 0x8 | 0x0 | 22 | C1 | 0xBD |
| $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 | 0x4 | 0x0 | 1F | C1 | 0x57 |
| $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 | 0xC | 0x0 | 22 | 00 | 0x66 |
| $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 | 0x6 | 0x0 | 1F | C1 | 0xB8 |
| $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 | 0x4 | 0x0 | FF | 5A | 0xE5 |
| $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 | 0xC | 0x0 | 3E | 00 | 0x13 |
| $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 | 0x6 | 0x0 | FF | 5A | 0x0A |

### 11.4.2 Selectable 4-bit CRC

The user can select a 4-bit CRC instead of the default 8-bit CRC for the SPI by programming the SPI_CFG register as described in Section 8.2.20: SPI configuration control register.

#### *11.4.2.1 SPI command format with 4-bit CRC*

**Table 325. SPI command format with 4-bit CRC**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Register Access Command | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Fixed Bits: Must = 0x0 | | | | Register Address | | | | | | | | Register Data | | | | | | | | Fixed Bits: Must = 0x0 | | | | 4-bit CRC | | | |
| C[3:0] | | | | 0 | 0 | 0 | 0 | RA[7:1] | | | | | | | RA[0] | RD[7:0] | | | | | | | | 0 | 0 | 0 | 0 | CRC[3:0] | | | |
| Sensor Data Command | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Fixed Bits: Must = 0x00000 | | | | | | | | | | | | | | | | | | | | Fixed Bits: Must = 0x0 | | | | 4-bit CRC | | | |
| C[3:0] | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CRC[3:0] | | | |

#### *11.4.2.2 SPI response format with 4-bit CRC*

**Table 326. SPI response format with 4-bit CRC**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Response to Register Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Unused Data = 0x0 | | Register Data: Contents of RA[7:1] High Byte | | | | | | | | Register Data: Contents of RA[7:1] Low Byte | | | | | | | | Unused Data = 0x0 | | | | 4-bit CRC | | | |
| C[0] | C[3] | C[2] | C[1] | ST[1:0] | | 0 | 0 | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | 0 | 0 | 0 | 0 | CRC[3:0] | | | |
| Response to Sensor Data Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Sensor Data | | | | | | | | | | | | | | | | Detail Status | | KAC | | | | 4-bit CRC | | | |
| C[0] | C[3] | C[2] | C[1] | ST[1:0] | | SD[11:0] | | | | | | | | | | | | Optional SD resolution | | | | SF[1:0] | | KAC[3:0] | | | | CRC[3:0] | | | |
| Error Response to Register Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Unused Data = 0x0 | | Register Data: Contents of RA[7:1] High Byte | | | | | | | | Register Data: Contents of RA[7:1] Low Byte | | | | | | | | Unused Data = 0x0 | | | | 4-bit CRC | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | 0 | 0 | 0 | 0 | CRC[3:0] | | | |
| Error Response to Sensor Data Request With Sensor Data | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Sensor Data | | | | | | | | | | | | | | | | Detail Status | | KAC | | | | 4-bit CRC | | | |
| C[0] | C[3] | C[2] | C[1] | 1 | 1 | SD[11:0] | | | | | | | | | | | | Optional SD resolution | | | | SF[1:0] | | KAC[3:0] | | | | CRC[3:0] | | | |
| Error Response to Sensor Data Request Without Sensor Data | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | x | Unused Data = 0x0000 | | | | | | | | | | | | | | | Detail Status | | Unused Data = 0x0 | | | | 4-bit CRC | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SF[1:0] | | 0 | 0 | 0 | 0 | CRC[3:0] | | | |

#### *11.4.2.3 Command error checking with 4-bit CRC*

The device calculates a 4-bit CRC on the entire 32-bits of each command. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message. If the calculated CRC does not match the transmitted CRC, the command is ignored and the device responds with the SPI Error response.

The CRC decoding procedure is:

1. A seed value determined by the SPICRCSEED[3:0] value in the SPI_CFG register is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.

4. If the shift register contains all zeros, the CRC is correct.
5. If the shift register contains a value other than zero, the CRC is incorrect.

The CRC polynomial and seed are shown in Table 327. SPI command message CRC, 4 bit.

**Table 327. SPI command message CRC, 4 bit**

| Default polynomial | Non-direct seed |
|---|---|
| $x^4 + 1$ | SPICRCSEED[3:0] |

#### 11.4.2.4 *Response error checking with 4-bit CRC*

The device calculates a CRC on the entire 32-bits of each response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC Encoding procedure is:

1. A seed value determined by the SPICRCSEED[3:0] value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds four zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and seed are shown in Table 328. SPI response message CRC, 4-bit.

**Table 328. SPI response message CRC, 4-bit**

| Default polynomial | Non-direct seed |
|---|---|
| $x^4 + 1$ | SPICRCSEED[3:0] |

#### 11.4.2.5 *Message counter (KAC) with 4-bit CRC*

If the 4-bit CRC is enabled, a 4-bit message counter field (KAC) is added to the Sensor Data Request Response. The message counter field is a 4-bit rolling message counter that is independently incremented for each SOURCEID. The initial value of the counter is '0001'.

#### 11.4.2.6 *Example 4-bit CRC calculations*

Some example CRC calculations for 32-bit SPI commands are shown in Table 329. SPI 4-bit CRC calculation examples.

**Table 329. SPI 4-bit CRC calculation examples**

| Polynomial | Seed | Bits[31:28] | Bits[27:24] | Bits[23:16] | Bits[15:8] | Bits[7:4] | Bits[3:0] |
|---|---|---|---|---|---|---|---|
| | | Command | 0x0 | Register address | Register data | 0x0 | 4-bit CRC |
| $x^4 + 1$ | 1010 | 0x8 | 0x0 | 22 | C1 | 0x0 | 0xF |
| $x^4 + 1$ | 1010 | 0x4 | 0x0 | 1F | C1 | 0x0 | 0xD |
| $x^4 + 1$ | 1010 | 0xC | 0x0 | 22 | 00 | 0x0 | 0x6 |
| $x^4 + 1$ | 1010 | 0x6 | 0x0 | 1F | C1 | 0x0 | 0xF |
| $x^4 + 1$ | 1010 | 0x4 | 0x0 | FF | 5A | 0x0 | 0x1 |
| $x^4 + 1$ | 1010 | 0xC | 0x0 | 3E | 00 | 0x0 | 0xB |
| $x^4 + 1$ | 1010 | 0x6 | 0x0 | FF | 5A | 0x0 | 0x3 |

### 11.4.3 Selectable 3-bit CRC

The user can select a 3-bit CRC instead of the default 8-bit CRC for the SPI by programming the SPI_CFG register as described in Section 8.2.20: SPI configuration control register.

#### *11.4.3.1 SPI command format with 3-bit CRC*

**Table 330. SPI command format with 3-bit CRC**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Register Access Command | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Fixed Bits: Must = 0x0 | | | | Register Address | | | | | | | | Register Data | | | | | | | | Fixed Bits: Must = 0x00 | | | | | 3-bit CRC | | |
| C[3:0] | | | | 0 | 0 | 0 | 0 | RA[7:1] | | | | | | | RA[0] | RD[7:0] | | | | | | | | 0 | 0 | 0 | 0 | 0 | CRC[2:0] | | |
| Sensor Data Command | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Fixed Bits: Must = 0x00000 | | | | | | | | | | | | | | | | | | | | Fixed Bits: Must = 0x00 | | | | | 3-bit CRC | | |
| C[3:0] | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CRC[2:0] | | |

#### *11.4.3.2 SPI response format with 3-bit CRC*

**Table 331. SPI response format with 3-bit CRC**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Response to Register Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Unused Data = 0x0 | | Register Data: Contents of RA[7:1] High Byte | | | | | | | | Register Data: Contents of RA[7:1] Low Byte | | | | | | | | Unused Data = 0x00 | | | | | 3-bit CRC | | |
| C[0] | C[3] | C[2] | C[1] | ST[1:0] | | 0 | 0 | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | 0 | 0 | 0 | 0 | 0 | CRC[2:0] | | |
| Response to Sensor Data Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Sensor Data | | | | | | | | | | | | | | | | Detail Status | | KAC | | | | 1 | 3-bit CRC | | |
| C[0] | C[3] | C[2] | C[1] | ST[1:0] | | SD[11:0] | | | | | | | | | | | | Optional SD resolution | | | | SF[1:0] | | KAC[3:0] | | | | 1 | CRC[2:0] | | |
| Error Response to Register Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Unused Data = 0x0 | | Register Data: Contents of RA[7:1] High Byte | | | | | | | | Register Data: Contents of RA[7:1] Low Byte | | | | | | | | Unused Data = 0x00 | | | | | 3-bit CRC | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | 0 | 0 | 0 | 0 | 0 | CRC[2:0] | | |
| Error Response to Sensor Data Request With Sensor Data | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Sensor Data | | | | | | | | | | | | | | | | Detail Status | | KAC | | | | 1 | 3-bit CRC | | |
| C[0] | C[3] | C[2] | C[1] | 1 | 1 | SD[11:0] | | | | | | | | | | | | Optional SD resolution | | | | SF[1:0] | | KAC[3:0] | | | | 1 | CRC[2:0] | | |
| Error Response to Sensor Data Request Without Sensor Data | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | x | Unused Data = 0x0000 | | | | | | | | | | | | | | | Detail Status | | Unused Data = 0x00 | | | | | 3-bit CRC | | |
| 0 | 0 | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SF[1:0] | | 0 | 0 | 0 | 0 | 0 | CRC[2:0] | | |

#### *11.4.3.3 Command error checking with 3-bit CRC*

The device calculates a 3-bit CRC on the entire 32-bits of each command. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message. If the calculated CRC does not match the transmitted CRC, the command is ignored and the device responds with the SPI Error response.

The CRC decoding procedure is:

1. A seed value determined by the SPICRCSEED[2:0] value in the SPI_CFG register is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.

4. If the shift register contains all zeros, the CRC is correct.
5. If the shift register contains a value other than zero, the CRC is incorrect.

The CRC polynomial and seed are shown in Table 332. SPI command message CRC, 3 bit.

**Table 332. SPI command message CRC, 3 bit**

| Default polynomial | Non-direct seed |
|---|---|
| $x^3 + x + 1$ | SPICRCSEED[2:0] |

Some example CRC calculations are shown in Table 266. PSI5 3-bit CRC calculation examples.

#### 11.4.3.4 *Response error checking with 3-bit CRC*

The device calculates a CRC on the entire 32-bits of each response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC encoding procedure is:

1. A seed value determined by the SPICRCSEED[2:0] value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds three zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and seed are shown in Table 333. SPI response message CRC, 3-bit.

**Table 333. SPI response message CRC, 3-bit**

| Default polynomial | Non-direct seed |
|---|---|
| $x^3 + x + 1$ | SPICRCSEED[2:0] |

#### 11.4.3.5 *Message (KAC) with 3-bit CRC*

If the 3-bit CRC is enabled, a 4-bit message counter field (KAC) is added to the Sensor Data Request Response. The message counter field is a 4-bit rolling message counter that is independently incremented for each SOURCEID. The initial value of the counter is '0001'.

#### 11.4.3.6 *Example 3-bit CRC calculations*

Some example CRC calculations for 32-bit SPI commands are shown in Table 334. SPI 3-bit CRC calculation examples.

**Table 334. SPI 3-bit CRC calculation examples**

| Polynomial | Seed | Bits[31:28] | Bits[27:24] | Bits[23:16] | Bits[15:8] | Bits[7:3] | Bits[2:0] |
|---|---|---|---|---|---|---|---|
| | | Command (Hex) | 0x0 (Hex) | Register address (Hex) | Register data (Hex) | 0b00000 (Binary) | 3-bit CRC (Binary) |
| $x^3 + x + 1$ | 111 | 0x8 | 0x0 | 22 | C1 | 0b00000 | 0b100 |
| $x^3 + x + 1$ | 111 | 0x4 | 0x0 | 1F | C1 | 0b00000 | 0b010 |
| $x^3 + x + 1$ | 111 | 0xC | 0x0 | 22 | 00 | 0b00000 | 0b001 |
| $x^3 + x + 1$ | 111 | 0x6 | 0x0 | 1F | C1 | 0b00000 | 0b000 |
| $x^3 + x + 1$ | 111 | 0x4 | 0x0 | FF | 5A | 0b00000 | 0b000 |
| $x^3 + x + 1$ | 111 | 0xC | 0x0 | 3E | 00 | 0b00000 | 0b101 |

| Polynomial | Seed | Bits[31:28] | Bits[27:24] | Bits[23:16] | Bits[15:8] | Bits[7:3] | Bits[2:0] |
|---|---|---|---|---|---|---|---|
| | | Command (Hex) | 0x0 (Hex) | Register address (Hex) | Register data (Hex) | 0b00000 (Binary) | 3-bit CRC (Binary) |
| $x^3 + x + 1$ | 111 | 0x6 | 0x0 | FF | 5A | 0b00000 | 0b010 |

## 11.5 Exception handling

### 11.5.1 Standard basic status reporting field

All responses include a basic status field (ST[1:0]) that includes the general status of the device and transmitted data as described in Table 335. Basic status field for responses to register commands and Table 336. Basic status field for responses to sensor data request commands. The contents of the basic status field is a representation of the device status at the rising edge of SS_B for the previous SPI command.

#### *11.5.1.1 Basic status field for responses to register commands*

**Table 335. Basic status field for responses to register commands**

| ST[1:0] | | Status | Description | Priority |
|---|---|---|---|---|
| 0 | 0 | Device in Initialization | ENDINIT Not Set | 3 |
| 0 | 1 | Normal Mode | ENDINIT Set | 4 |
| 1 | 0 | Self-test | ST_CTRL[3:0] not equal to '0000' for any channel | 2 |
| 1 | 1 | Internal Error Present | See Figure 95. Internal status mapping and SPI basic status content | 1 |

#### *11.5.1.2 Basic status field for responses to sensor data request commands*

**Table 336. Basic status field for responses to sensor data request commands**

| ST[1:0] | | Status | Description | SF[1:0] | | Sensor data field | Priority |
|---|---|---|---|---|---|---|---|
| 0 | 0 | Device in Initialization | ENDINIT Not Set | 0 | 0 | Sensor Data | 3 |
| 0 | 1 | Normal Mode | ENDINIT Set | 0 | 0 | Sensor Data | 4 |
| 1 | 0 | Self-test | ST_CTRL[3:0] not equal to '0000' for the associated channel | 0 | 0 | Sensor Data | 2 |
| 1 | 1 | Internal Error Present | See Section 11.5.3: Standard detailed status field reporting | See Section 11.5.3: Standard detailed status field reporting | | See Section 11.5.3: Standard detailed status field reporting | 1 |

### 11.5.2 Alternative basic status reporting field

If the SPI_STATUS bit is set in the SPI_CFG register, the basic status reporting is as shown in Table 337. Alternative basic status reporting field.

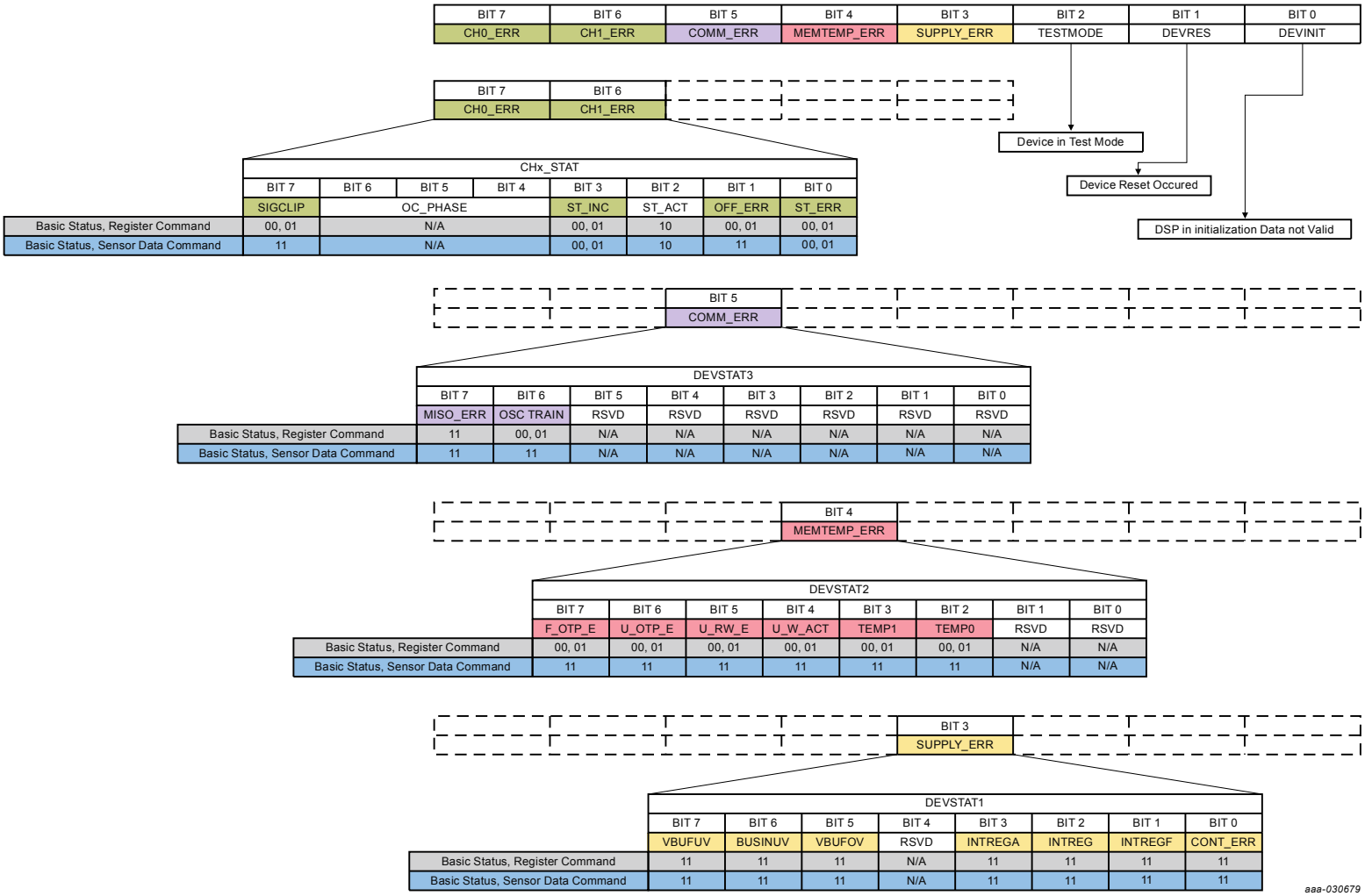
**Table 337. Alternative basic status reporting field**

| ST[1:0] | | Status | Description | SF[1:0] | | Sensor data field | Priority |
|---|---|---|---|---|---|---|---|
| 0 | 0 | Device in Initialization | ENDINIT Not Set | 0 | 0 | Sensor Data | 3 |
| 0 | 1 | Normal Mode | ENDINIT Set | 0 | 0 | Sensor Data | 4 |
| 1 | 0 | Self-test | ST_CTRL[3:0] not equal to '0000' for the associated channel for dual axis | 0 | 0 | Sensor Data | 2 |

| ST[1:0] | | Status | Description | SF[1:0] | Sensor data field | Priority |
|---|---|---|---|---|---|---|
| 1 | 1 | Internal Error Present | See Section 11.5.4: Alternative detailed status field reporting | See Section 11.5.4: Alternative detailed status field reporting | See Section 11.5.4: Alternative detailed status field reporting | 1 |

Figure 95. Internal status mapping and SPI basic status content shows the internal device status mapping by register and the basic status field contents by response type.

**Figure 95. Internal status mapping and SPI basic status content**




## 11.5.3 Standard detailed status field reporting

The response to sensor data requests includes a detailed status field (SF[1:0]). If the Basic Status indicates an internal error, the contents of the detailed status field provide additional information regarding the error status. The contents of the detailed status field is a representation of the device status at the rising edge of SS_B for the previous SPI command.

**Table 338. SPI error response status field definition**

| ST[1:0] | | SF[1:0] | | Status sources | DEVSTAT state | SUPERR_DIS state | Error priority | Command echo field (Source ID) | Sensor data request commands<br>Sensor data field value | Register access command response | PCM | ARM |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | Oscillator Training Error | Bit set in DEVSTAT3 | N/A | 11 | C[0], C[3:1] | Sensor Data | Normal | No Effect | No Effect |
| | | | | Offset Error | Bit set in CHx_STAT: | N/A | 10 | C[0], C[3:1] | Sensor Data | Normal | No Effect | No Effect |

| ST[1:0] | | SF[1:0] | | Status sources | DEVSTAT state | SUPERR_DIS state | Error priority | Command echo field (Source ID) | Sensor data request commands<br>Sensor data field value | Register access command response | PCM | ARM |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | | SIGNALCLIP or OFF-SET_ERR | | | | | | | |
| | | | | Temperature Error | Bit set in DEVSTAT2 | N/A | 9 | C[0], C[3:1] | Sensor Data | Normal | No Effect | No Effect |
| 1 | 1 | 0 | 1 | User OTP Memory Error (UF0 or UF1) | U_OTP_ERR set in DEVSTAT2 | N/A | 8 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | Normal | No Effect | Frozen |
| | | | | User R/W Memory Error (UF2) | U_RW_ERR set in DEVSTAT2 | N/A | 7 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | Normal | No Effect | Frozen |
| | | | | ST OTP Memory Error | F_OTP_ERR set in DEVSTAT2 | N/A | 6 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | Normal | No Effect | Frozen |
| 1 | 1 | 1 | 0 | Test Mode Active | TESTMODE bit set in DEVSTAT | N/A | 5 | 0x0 | All zero response | | No Effect | Frozen |
| | | | | Supply Error | Bit set in DEVSTAT1 | 0 | 4 | 0x0 | All zero response until the supply monitor timer expires<br>An Error Code is transmitted for a minimum of one transmission<br>(See Section 8.2.2.5: Supply error flag (SUPPLY_ERR)) | | Disabled | Frozen |
| | | | | | | 1 | 4 | 0x0 | All zero response until the supply monitor timer expires<br>(See Section 8.2.2.5: Supply error flag (SUPPLY_ERR)) | | | Frozen |
| | | | | Reset Error | DEVRES set | N/A | 3 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | | No Effect | Frozen |
| 1 | 1 | 1 | 1 | MISO Error | Bit set in DEVSTAT3 | N/A | 2 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | Error response | No Effect | Frozen |
| | | | | SPI Error | N/A | N/A | 1 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | Error response | No Effect | Frozen |

### 11.5.4 Alternative detailed status field reporting

The response to sensor data requests includes a detailed status field (SF[1:0]). If the Basic Status indicates an internal error, the contents of the detailed status field provide additional information regarding the error status. The contents of the detailed status field is a representation of the device status at the rising edge of SS_B for the previous SPI command.

If the SPI_STATUS bit is set in the SPI_CFG register, the basic status reporting is shown in Table 339. Alternate SPI error response status field definition.

**Table 339. Alternate SPI error response status field definition**

| ST[1:0] | | SF[1:0] | | Status sources | DEVSTAT state | SUPERR_DIS state | Error priority | Command echo field (Source ID) | Sensor data request commands<br>Sensor data field value | Register access command response | PCM | ARM |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | Oscillator Training Error | Bit set in DEVSTAT3 | N/A | 11 | C[0], C[3:1] | Sensor Data | Normal | No Effect | No effect |
| | | | | Offset Error | Bit set in CHx_STAT:<br>OFFSET_ERR | N/A | 10 | C[0], C[3:1] | Sensor Data | Normal | No Effect | No effect |
| | | | | Temperature Error | Bit set in DEVSTAT2 | N/A | 9 | C[0], C[3:1] | Sensor Data | Normal | No Effect | No effect |
| 1 | 1 | 0 | 1 | User OTP Memory Error (UF0 or UF1) | U_OTP_ERR set in DEVSTAT2 | N/A | 8 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | Normal | No Effect | Frozen |
| | | | | User R/W Memory Error (UF2) | U_RW_ERR set in DEVSTAT2 | N/A | 7 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | Normal | No Effect | Frozen |
| | | | | ST OTP Memory Error | F_OTP_ERR set in DEVSTAT2 | N/A | 6 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | Normal | No Effect | Frozen |
| 1 | 1 | 1 | 0 | Test Mode Active | TESTMODE bit set in DEVSTAT | N/A | 5 | 0x0 | All zero response | | No Effect | Frozen |
| | | | | Supply Error | Bit set in DEVSTAT1 | 0 | 4 | 0x0 | All zero response until the supply monitor timer expires<br>An Error Code is transmitted for a minimum of one transmission<br>(See Section 8.2.2.5: Supply error flag (SUPPLY_ERR)) | | Disabled | Frozen |
| | | | | | | 1 | 4 | 0x0 | All zero response until the supply monitor timer expires<br>(See Section 8.2.2.5: Supply error flag (SUPPLY_ERR)) | | | Frozen |
| | | | | Reset Error | DEVRES set | N/A | 3 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | | No Effect | Frozen |
| 1 | 1 | 1 | 1 | MISO Error | Bit set in DEVSTAT3 | N/A | 2 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | Error response | No Effect | Frozen |
| | | | | SPI Error | N/A | N/A | 1 | 0x0 | The Sensor Data Field Error Code is transmitted for a minimum of one transmission | Error response | No Effect | Frozen |

### 11.5.5 Error responses

**Table 340. Error responses**

| MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Error Response to Register Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Unused Data = 0x0 | | Register Data: Contents of RA[7:1] High Byte | | | | | | | | Register Data: Contents of RA[7:1] Low Byte | | | | | | | | 8-bit CRC | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | CRC[7:0] | | | | | | | |
| Error Response to Sensor Data Request With Sensor Data | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | Sensor Data | | | | | | | | | | | | | | | | Detail Status | | 8-bit CRC | | | | | | | |
| C[0] | C[3] | C[2] | C[1] | 1 | 1 | SD[11:0] | | | | | | | | | | | | Optional SD resolution | | | | SF[1:0] | | CRC[7:0] | | | | | | | |
| Error Response to Sensor Data Request Without Sensor Data | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | | | Basic Status | | x | Unused Data = 0x0000 | | | | | | | | | | | | | | | Detail Status | | 8-bit CRC | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SF[1:0] | | CRC[7:0] | | | | | | | |

**Table 341. Error response description**

| Bit field | Definition |
|---|---|
| C[3:0] | Command bits: all 0s or a command echo |
| SD[11:0] | Sensor Data or the Sensor Data Field Error Code.<br>• For unsigned data, the Sensor Data Field Error Code is 0x000<br>• For signed data, the Sensor Data Field Error Code is 0x800<br>See Section 11.5.3: Standard detailed status field reporting for Sensor Data Request commands.<br>For all other commands, all bits are '0'. |
| SF[3:0] | Status. See Section 11.5.3: Standard detailed status field reporting |

### 11.5.6 SPI error

The following external SPI conditions result in a SPI error:

- SCLK is high when SS_B is asserted
- The number of SCLK rising edges detected while SS_B is asserted is not equal to 0 or 32
- SCLK is high when SS_B is deasserted
- A command message CRC error is detected (MOSI)
- A Sensor Data Request is received for a SOURCEID that is not enabled
- A Register Write command to any register other than the DEVLOCK_WR register is received while ENDINIT is set.

If a SPI error is detected, the device responds with the Error Response as described in Section 11.5.4: Alternative detailed status field reporting with the Detailed Status Field set to "SPI Error" as defined in Section 11.5.3: Standard detailed status field reporting.

### 11.5.7 SPI data output verification error

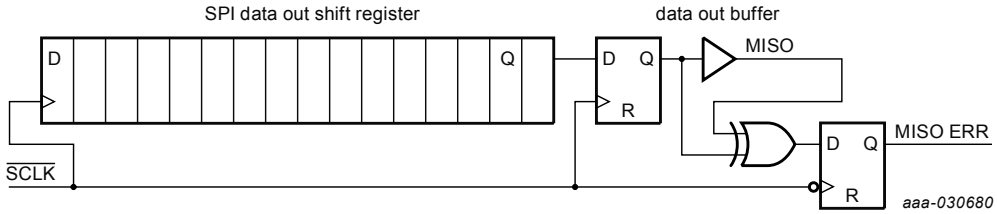
The device includes a function to verify the integrity of the data output to the MISO pin. The function compares the data transmitted on the MISO pin to the data intended to be transmitted. If any one bit doesn't match, a SPI MISO Mismatch Fault is detected and the MISO_ERR flag in the DEVSTAT3 register is set.

If a valid sensor data request message is received during the SPI transfer with the MISO mismatch failure, the request is ignored and the device responds with the Error Response as described in Section 11.5.4: Alternative detailed status field reporting with the Detailed Status Field set to "SPI Error" as defined in Section 11.5.3: Standard detailed status field reporting. during the subsequent SPI message.

If a valid register write request message is received during the SPI transfer with the MISO mismatch failure, the register write is completed as requested, but the device responds with the Error Response as described in Section 11.5.4: Alternative detailed status field reporting with the Detailed Status Field set to "SPI Error" as defined in Section 11.5.3: Standard detailed status field reporting. during the subsequent SPI message.

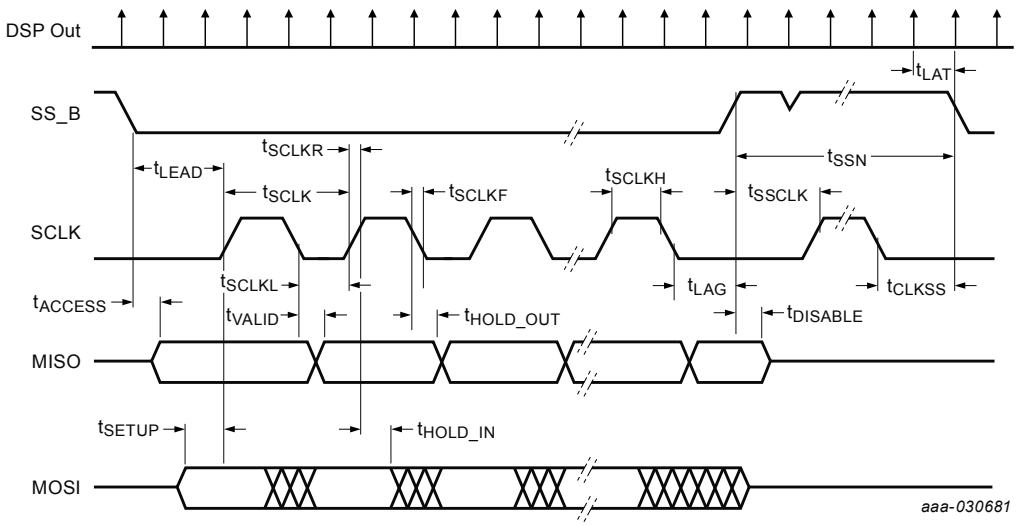
If a valid register read request message is received during the SPI transfer with the MISO mismatch failure, the register read is ignored and the device responds with the Error Response as described in Section 11.5.4: Alternative detailed status field reporting with the Detailed Status Field set to "SPI Error" as defined in Section 11.5.3: Standard detailed status field reporting. during the subsequent SPI message.

**Figure 96. SPI data output verification**




## 11.6 SPI timing diagram

**Figure 97. SPI timing diagram**



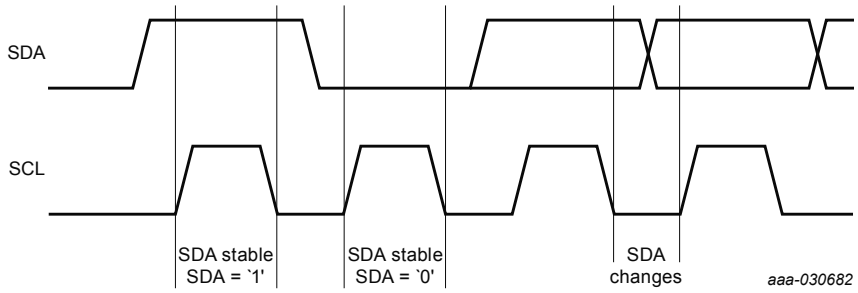
# 12 Inter-integrated circuit (I²C) interface

The device includes an interface compliant to the I²C bus specification UM10204 [1] . The device operates in slave mode and includes support for Standard Mode, Fast Mode, and Fast Mode Plus although the maximum practical operating frequency for I²C in a given system implementation depends on several factors including the pull-up resistor values and the total bus capacitance.

## 12.1 I²C bit transmissions

The state of SDA when SCL is high determines the bit value being transmitted. SDA must be stable when SCL is high and change when SCL is low as shown in Figure 99. I²C start condition. After the START signal has been transmitted by the master, the bus is considered busy. Timing for the start condition is specified in Section 7.15: Dynamic electrical characteristics - I²C.

**Figure 98. I²C bit transmissions**

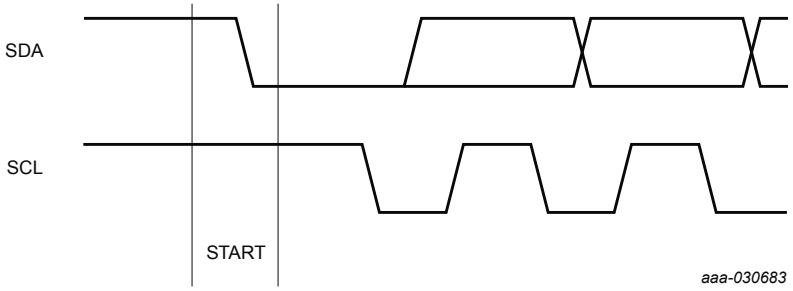



## 12.2 I²C start condition

A bus operation is always started with a start condition (START) from the master. A START is defined as a high to low transition on SDA while SCL is high as shown in Figure 99. I²C start condition. After the START signal has been transmitted by the master, the bus is considered busy. Timing for the start condition is specified in Section 7.15: Dynamic electrical characteristics - I²C.

A start condition (START) and a repeat START condition (rSTART) are identical.

**Figure 99. I²C start condition**

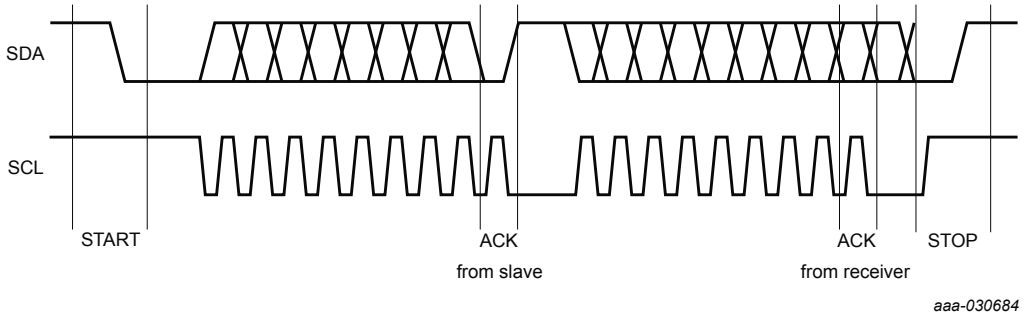



## 12.3 I²C byte transmissions

Data transfers are completed in byte increments. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit (Section 12.4: I²C acknowledge and not acknowledge transmissions) from the receiver. Data is transferred with the Most Significant Bit (MSB) first (Figure 100. I²C byte transmissions). The master generates all clock pulses, including the ninth clock for the Acknowledge bit. Timing for the byte transmissions is specified in Section 7.15: Dynamic electrical characteristics - I²C.

All functions for this device are completed within the Acknowledge clock pulse. Clock Stretching is not used.

Figure 100. **I²C byte transmissions**




## 12.4 I²C acknowledge and not acknowledge transmissions

Each byte must be followed by an Acknowledge bit (ACK) from the receiver. For an ACK, the transmitter releases SDA during the acknowledge clock pulse and the receiver pulls SDA low during the high portion of the clock pulse. Set-up and hold times as specified in Section 7.15: Dynamic electrical characteristics - I²C must also be taken into account.

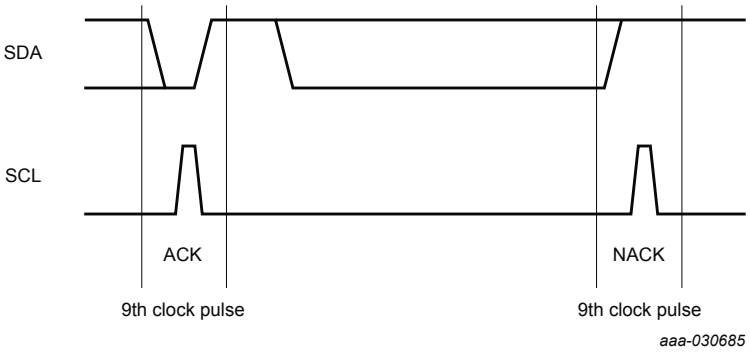
For a Not Acknowledge bit (NACK), SDA remains high during the entire acknowledge clock pulse. Five conditions lead to a NACK:

1. No receiver is present on the bus with the transmitted address.
2. The addressed receiver is unable to receive or transmit because it is performing some real-time function and is not ready to start communication with the master.
3. The receiver receives unrecognized data or commands.
4. The receiver cannot receive any more data bytes.
5. The master-receiver signals the end of the transfer to the slave transmitter.

Following a Not Acknowledge bit, the master can transmit either a STOP to terminate the transfer, or a repeated START to initiate a new transfer.

An example ACK and NACK are shown in Figure 101. I²C acknowledge and not acknowledge transmission.

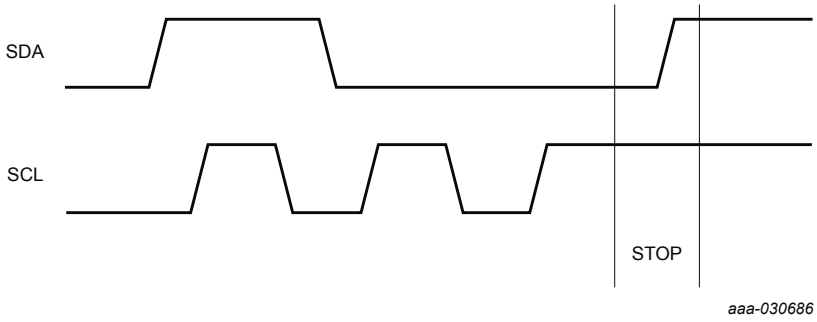
Figure 101. **I²C acknowledge and not acknowledge transmission**




## 12.5 I²C stop condition

A bus operation is always terminated with a stop condition (STOP) from the master. A STOP is defined as a Low to high transition on SDA while SCL is high as shown in Figure 102. I²C stop condition. After the STOP has been transmitted by the master, the bus is considered free. Timing for the stop condition is specified in Section 7.15: Dynamic electrical characteristics - I²C.

Figure 102. **I²C stop condition**




## 12.6 I²C register transfers

### 12.6.1 Register write transfers

The device supports I²C register write data transfers. Register write data transfers are constructed as follows:

1. The master transmits a START condition
2. The master transmits the 7-bit slave address
3. The master transmits a '0' for the Read/Write Bit to indicate a Write operation
4. The slave transmits an ACK
5. The master transmits the register address to be written
6. The slave transmits an ACK
7. The master transmits the data byte to be written to the register address
8. The slave transmits an ACK
9. The master transmits a STOP condition

| S | Slave address | $\overline{W}$ | A | Register address | A | REGISTER DATA | A | P |
|---|---|---|---|---|---|---|---|---|

Master transmission
Slave transmission

The device automatically increments the register address allowing for multiple register writes to be completed in one trans-action. In this case, the register write data transfers are constructed as follows:

1. The master transmits a START condition
2. The master transmits the 7-bit slave address
3. The master transmits a '0' for the Read/Write Bit to indicate a Write operation
4. The slave transmits an ACK
5. The master transmits the register address to be written
6. The slave transmits an ACK
7. The master transmits the data byte to be written to the register address
8. The slave transmits an ACK
9. The master transmits the data byte to be written to the register address +1
10. The slave transmits an ACK
11. Repeat 9. and 10. until all registers are written
12. The master transmits a STOP condition

### 12.6.2 Register read transfers

The device supports I²C register read data transfers. Register read data transfers are constructed as follows:

1. The master transmits a START condition
2. The master transmits the 7-bit slave address
3. The master transmits a '0' for the Read/Write Bit to indicate a Write operation

4. The slave transmits an ACK
5. The master transmits the register address to be read
6. The slave transmits an ACK
7. The master transmits a repeat START condition
8. The master transmits the 7-bit slave address
9. The master transmits a '1' for the Read/Write Bit to indicate a Read operation
10. The slave transmits an ACK
11. The slave transmits the data from the register addressed
12. The master transmits a NACK
13. The master transmits a STOP condition




The device automatically increments the register address allowing for multiple register reads to be completed in one trans-action. In this case, the register read data transfers are constructed as follows:

1. The master transmits a START condition
2. The master transmits the 7-bit slave address
3. The master transmits a '0' for the Read/Write Bit to indicate a Write operation
4. The slave transmits an ACK
5. The master transmits the register address to be read
6. The slave transmits an ACK
7. The master transmits a repeat START condition
8. The master transmits the 7-bit slave address
9. The master transmits a '1' for the Read/Write Bit to indicate a Read operation
10. The slave transmits an ACK
11. The slave transmits the data from the register addressed
12. The master transmits an ACK
13. The slave transmits the data byte from register address +1
14. Repeat 12. and 13. until all registers are read
15. The master transmits a NACK
16. The master transmits a STOP condition

### 12.6.3 Sensor data register read wraparound options

The device includes automatic sensor data register read wrap around features to optimize the number of I²C transactions necessary for continuous reads of sensor data.

#### *12.6.3.1 Single channel register read wraparound*

Depending on the state of the SIDx_EN bits in the channel 0 and channel 1 SOURCEID_0 and SOURCEID_1 registers, the register address automatically wraps back to the DEVSTAT_COPY register as shown in Table 342. Single channel register read wrap around Table 343. Dual channel register read wrap around.

**Table 342. Single channel register read wrap around**

| Ch0 SID1_EN | Ch0 SID0_EN | Address increment and wrap around effect | Optimized register read sequence |
|---|---|---|---|
| 0 | 0 | Address wraps around from $FF to $00 | None |
| 0 | 1 | Address wraps from $63 (CH0_SNSDATA0_H) to $61 (DEVSTAT_COPY) | DEVSTAT_COPY, |

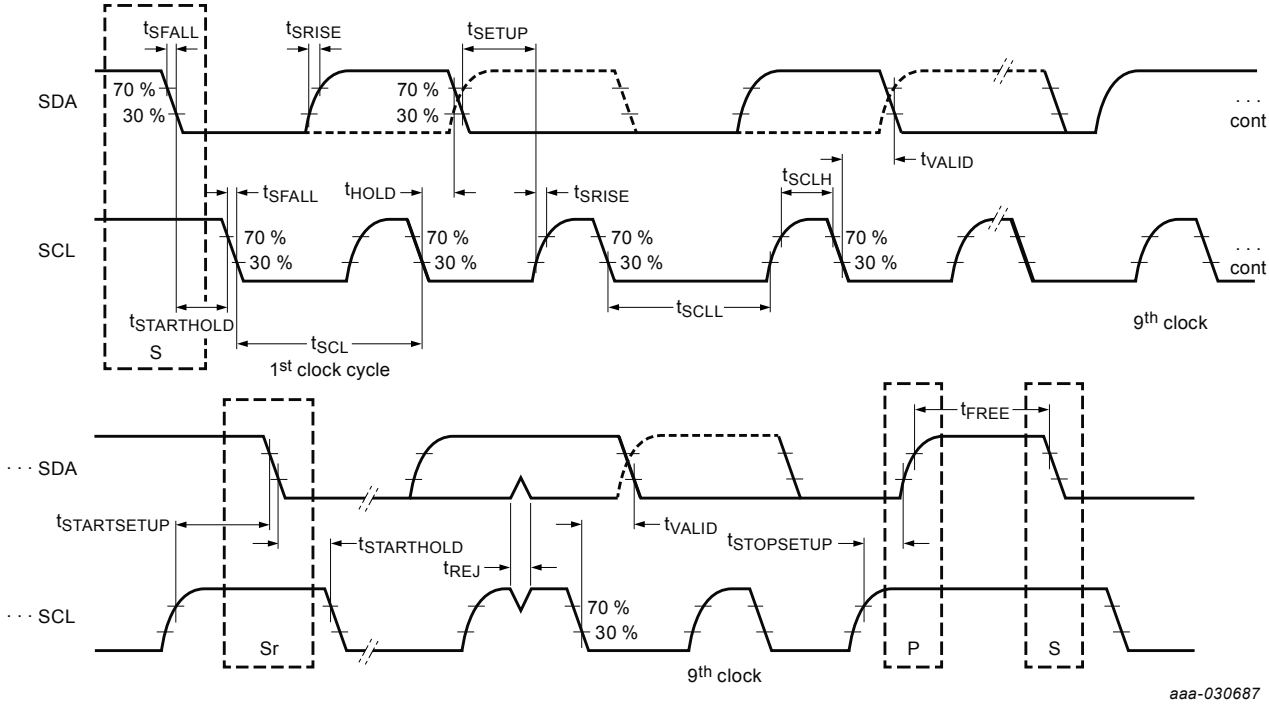
| Ch0 SID1_EN | Ch0 SID0_EN | Address increment and wrap around effect | Optimized register read sequence |
|---|---|---|---|
| | | | CH0_SNSDATA0_L, CH0_SNSDATA0_H |
| 1 | x | Address wraps from $65 (CH0_SNSDATA1_H) to $61 (DEVSTAT_COPY) | DEVSTAT_COPY,<br>CH0_SNSDATA0_L, CH0_SNSDATA0_H,<br>CH0_SNSDATA1_L, CH0_SNSDATA1_H |

**Table 343. Dual channel register read wrap around**

| Ch1 SID1_EN | Ch1 SID0_EN | Ch0 SID1_EN | Ch0 SID0_EN | Address increment and wrap around effect | Optimized register read sequence |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Address wraps around from $FF to $00 | None |
| 0 | 0 | 0 | 1 | Address wraps from $63 (CH0_SNSDATA0_H) to $61 (DEVSTAT_COPY) | DEVSTAT_COPY,<br>CH0_SNSDATA0_L, CH0_SNSDATA0_H |
| 0 | 0 | 1 | x | Address wraps from $65 (CH0_SNSDATA1_H) to $61 (DEVSTAT_COPY) | DEVSTAT_COPY,<br>CH0_SNSDATA0_L, CH0_SNSDATA0_H,<br>CH0_SNSDATA1_L, CH0_SNSDATA1_H |
| 0 | 1 | x | x | Address jumps from $65 (CH0_SNSDATA1_H) to $72 (CH1_SNSDATA0_L)<br>Address wraps from $73 (CH1_SNSDATA1_H) to $61 (DEVSTAT_COPY) | DEVSTAT_COPY,<br>CH0_SNSDATA0_L, CH0_SNSDATA0_H,<br>CH0_SNSDATA1_L, CH0_SNSDATA1_H,<br>CH1_SNSDATA0_L, CH1_SNSDATA0_H |
| 1 | x | x | x | Address jumps from $65 (CH0_SNSDATA1_H) to $72 (CH1_SNSDATA0_L)<br>Address wraps from $75 (CH1_SNSDATA1_H) to $61 (DEVSTAT_COPY) | DEVSTAT_COPY,<br>CH0_SNSDATA0_L, CH0_SNSDATA0_H,<br>CH0_SNSDATA1_L, CH0_SNSDATA1_H,<br>CH1_SNSDATA0_L, CH1_SNSDATA0_H,<br>CH1_SNSDATA1_L, CH1_SNSDATA1_H |

## 12.7 I²C timing diagram

Figure 103. I²C timing diagram



# 13 Package outlines

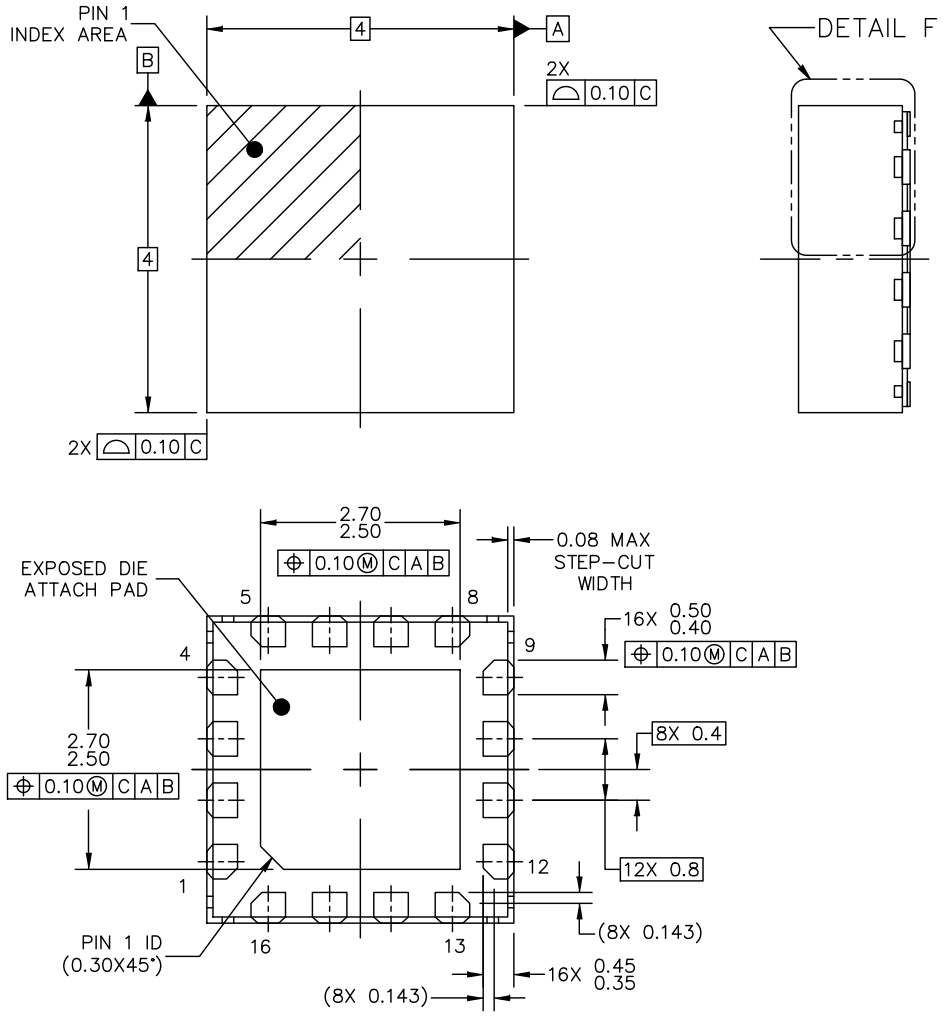
## 13.1 Package outline - LQFN16 (step-cut wettable flank)

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**Figure 104. Package outline for LQFN16 (step-cut wettable flank)**

H-PQFN-16 I/O STEP-CUT WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688-1(SC)




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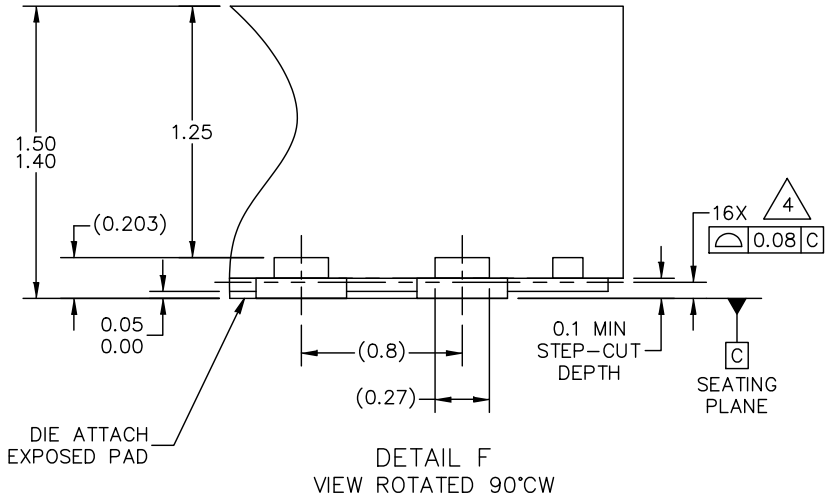
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|---|---|---|---|---|

**Figure 105. Package outline detail for LQFN16 (step-cut wettable flank)**

H–PQFN–16 I/O STEP–CUT WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688–1(SC)




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|---|---|---|---|---|

**Figure 106. Package outline notes for LQFN16 (step-cut wettable flank)**

H–PQFN–16 I/O STEP–CUT WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688–1(SC)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MINIMUM METAL GAP SHOULD BE 0.15 MM.
6. RECOMMENDED STENCIL AND SOLDER PASTED AREA ARE IN SHEET 3 TO 5.

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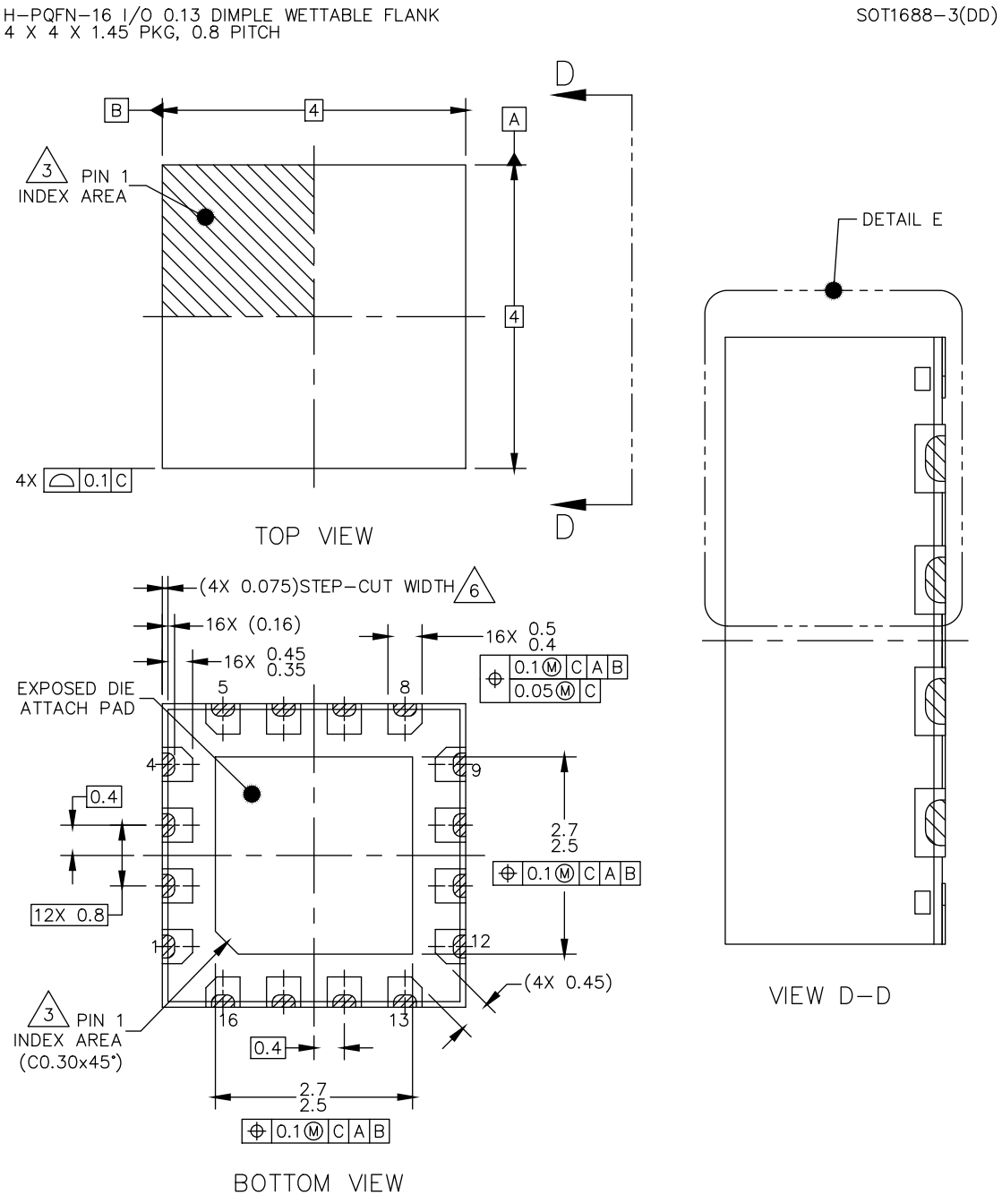
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|---|---|---|---|---|

## 13.2 Package outline - LQFN16 (dimple deburr wettable flank)

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**Figure 107. Package outline for LQFN16 (dimple deburr wettable flank)**




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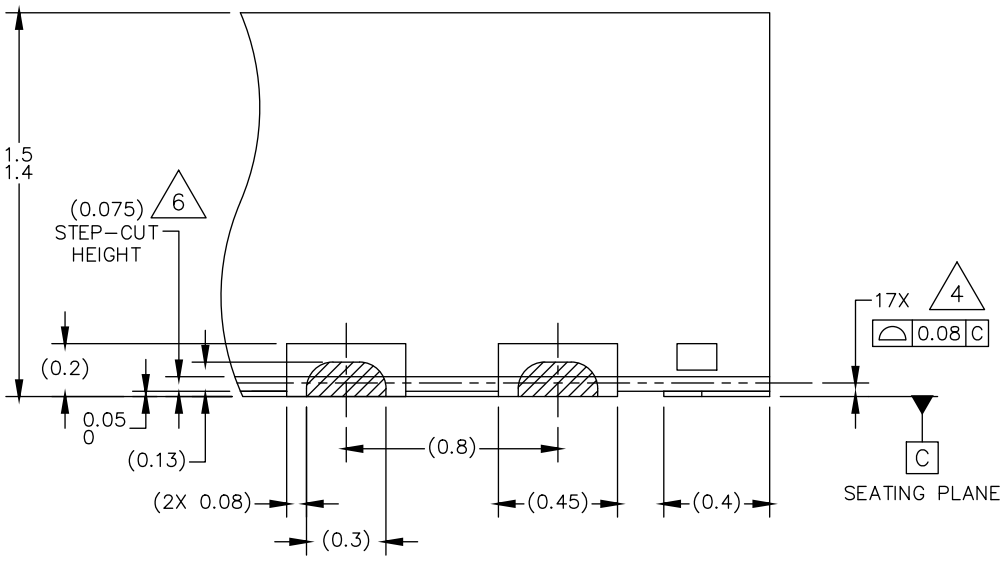
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|---|---|---|---|---|

**Figure 108. Package outline detail for LQFN16 (dimple deburr wettable flank)**

H–PQFN–16 I/O 0.13 DIMPLE WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688–3(DD)




DETAIL E
VIEW ROTATED 90° CW

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|---|---|---|---|---|

**Figure 109. Package outline notes for LQFN16 (dimple deburr wettable flank)**

H–PQFN–16 I/O 0.13 DIMPLE WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688–3(DD)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.25 MM.
6. STEP–CUT IS APPLIED FOR BURR REMOVAL ONLY.

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|---|---|---|---|---|

# 14 Soldering

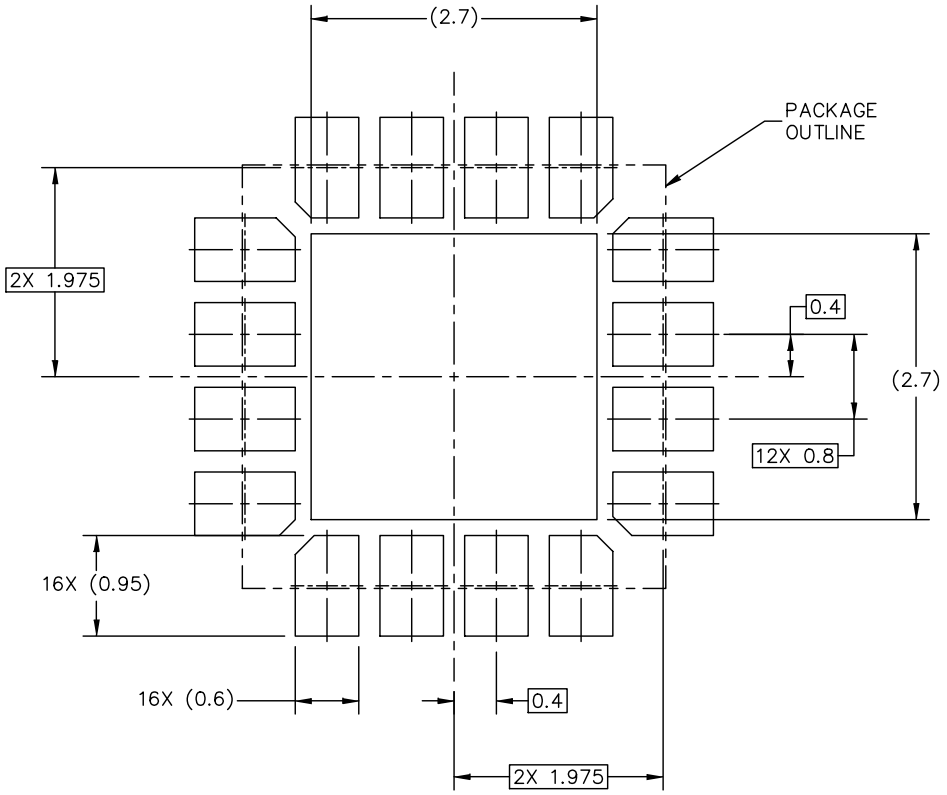
## 14.1 Soldering HLQFN16 (step-cut wettable flank)

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**Figure 110. Reflow soldering footprint part 1 for HLQFN16 (step-cut wettable flank)**

H−PQFN−16 I/O STEP−CUT WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

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RECOMMENDED SOLDER MASK OPENING PATTERN

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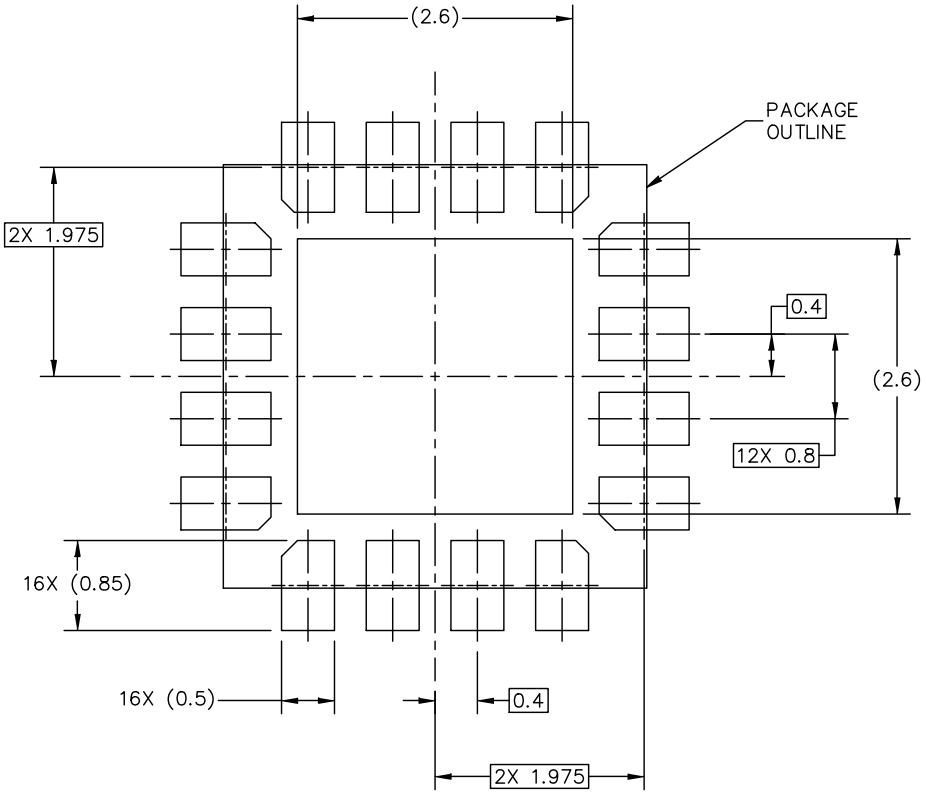
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|---|---|---|---|---|

**Figure 111. Reflow soldering footprint part 2 for HLQFN16 (step-cut wettable flank)**

H−PQFN−16 I/O STEP−CUT WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

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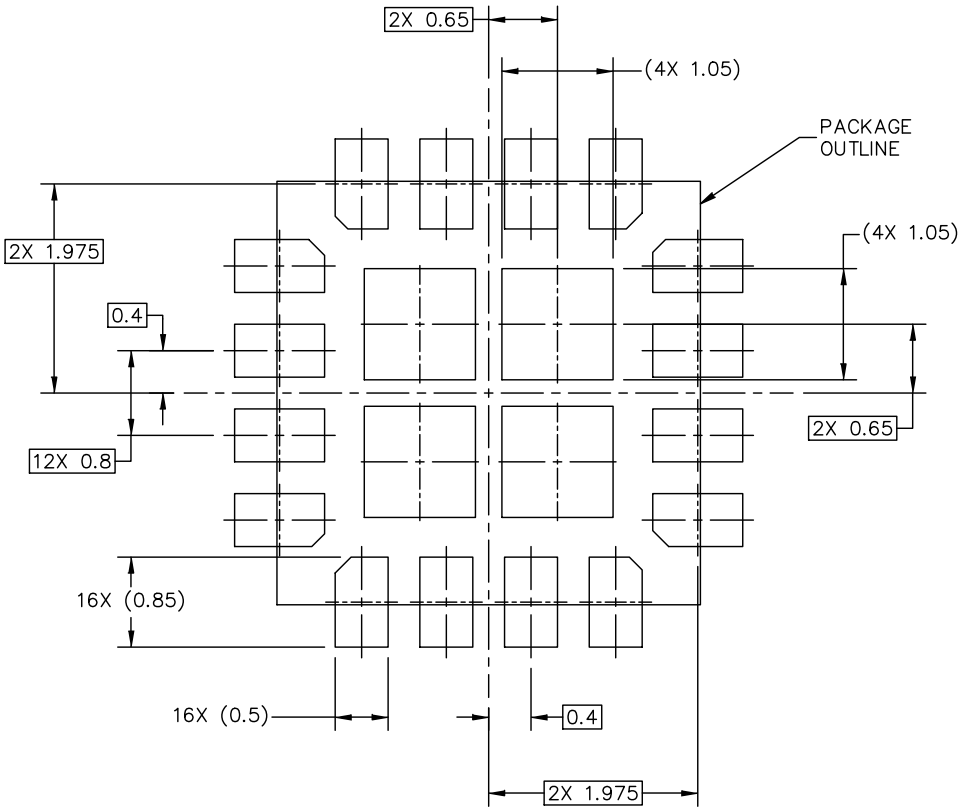
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|---|---|---|---|---|

**Figure 112. Reflow soldering footprint part 3 for HLQFN16 (step-cut wettable flank)**

H−PQFN−16 I/O STEP−CUT WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688−1(SC)




RECOMMENDED STENCIL THICKNESS 0.125 OR 0.150

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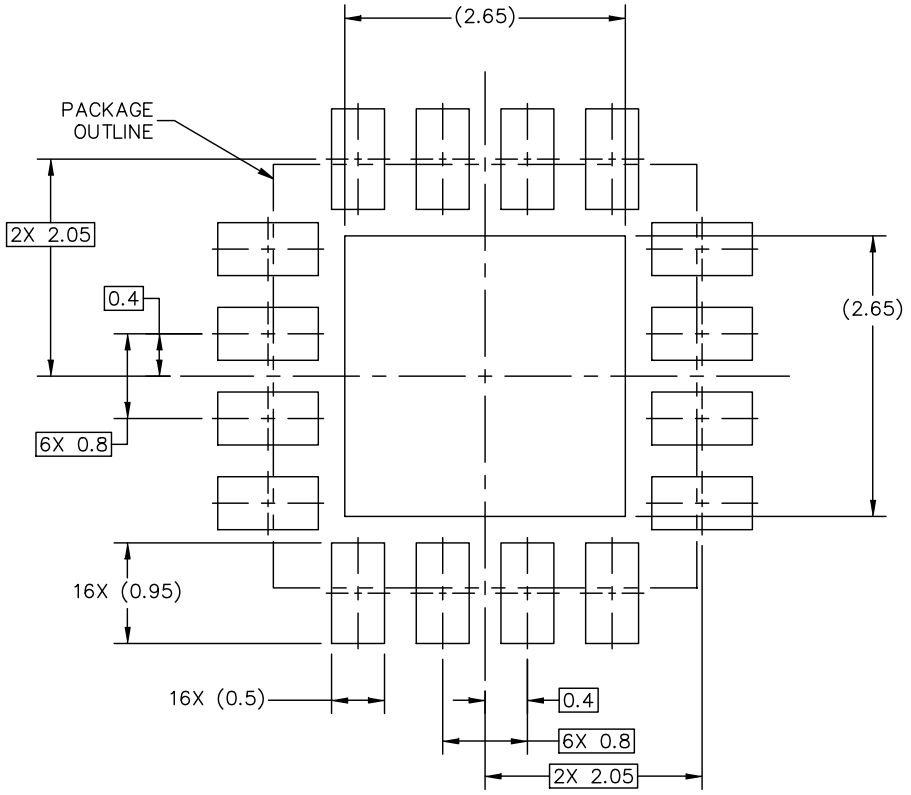
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|---|---|---|---|---|

**Figure 113. Reflow soldering footprint part 4 for HLQFN16 (step-cut wettable flank)**

H−PQFN−16 I/O STEP−CUT WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

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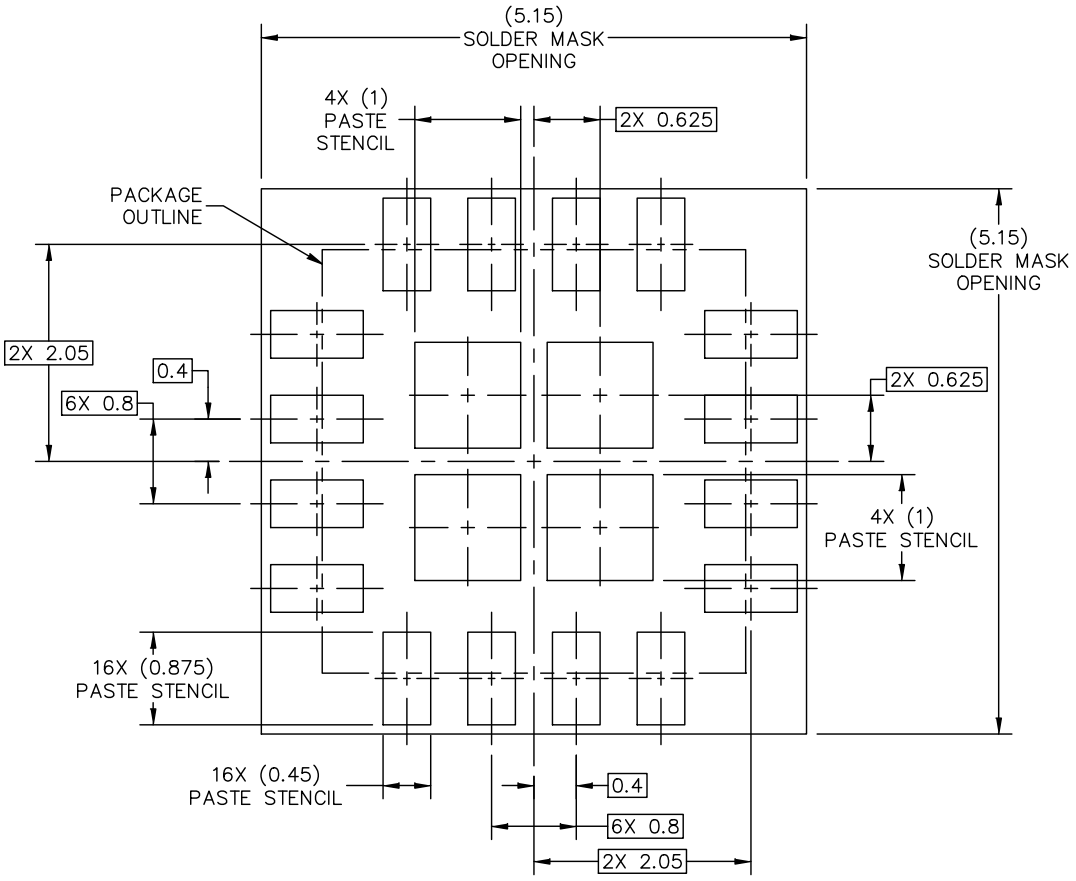
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|---|---|---|---|---|

**Figure 114. Reflow soldering footprint part 5 for HLQFN16 (step-cut wettable flank)**

H−PQFN−16 I/O STEP−CUT WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688−1(SC)




RECOMMENDED STENCIL THICKNESS 0.125 OR 0.150

ALTERNATE SOLDER MASK OPENING AND PASTE STENCIL DESIGN GUIDELINES

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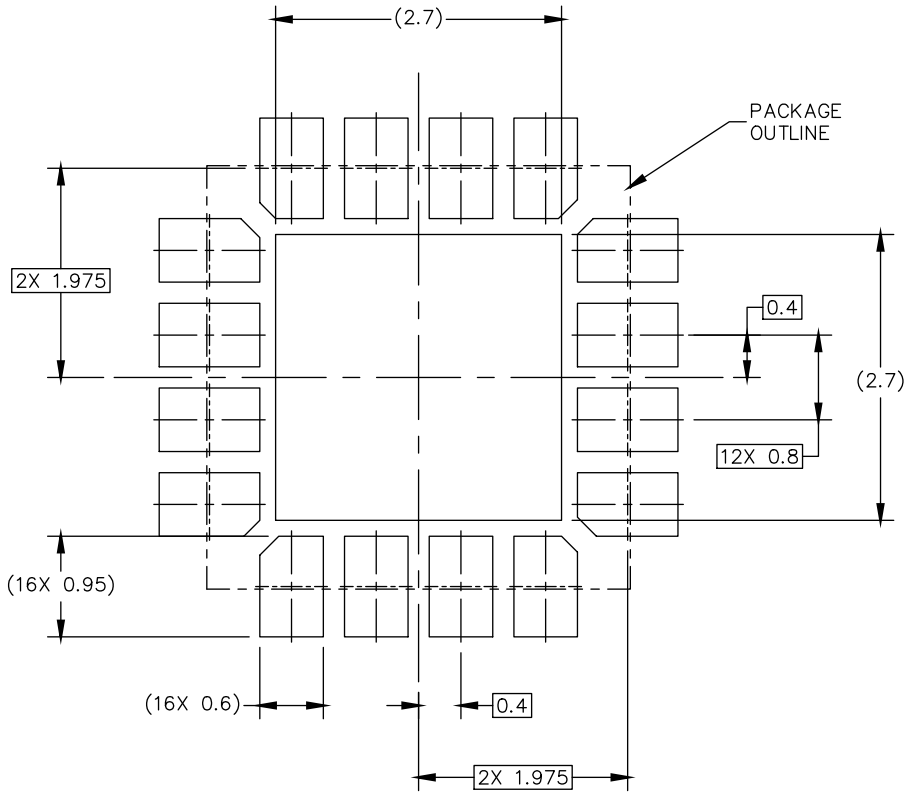
## 14.2 Soldering HLQFN16 (dimple deburr wettable flank)

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**Figure 115. Reflow soldering footprint part 1 for HLQFN16 (dimple deburr wettable flank)**

H–PQFN–16 I/O 0.13 DIMPLE WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688–3(DD)




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RECOMMENDED SOLDER MASK OPENING PATTERN

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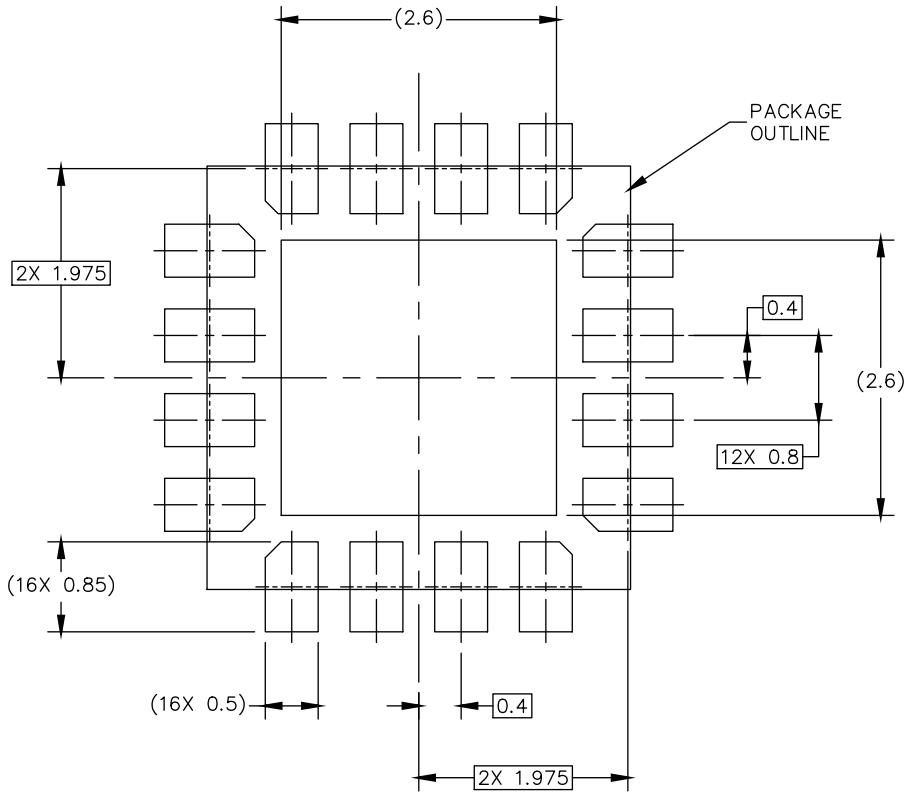
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|---|---|---|---|---|

**Figure 116. Reflow soldering footprint part 2 for HLQFN16 (dimple deburr wettable flank)**

H−PQFN−16 I/O 0.13 DIMPLE WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688−3(DD)




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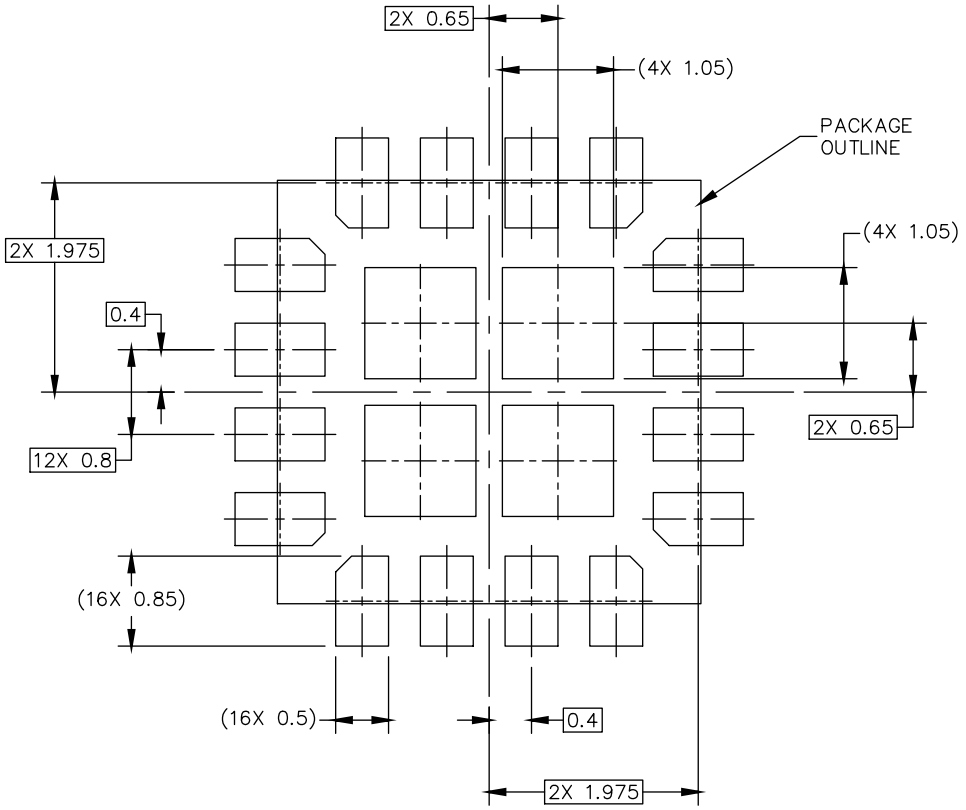
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**Figure 117. Reflow soldering footprint part 3 for HLQFN16 (dimple deburr wettable flank)**

H−PQFN−16 I/O 0.13 DIMPLE WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688−3(DD)




RECOMMENDED STENCIL THICKNESS 0.125 OR 0.150

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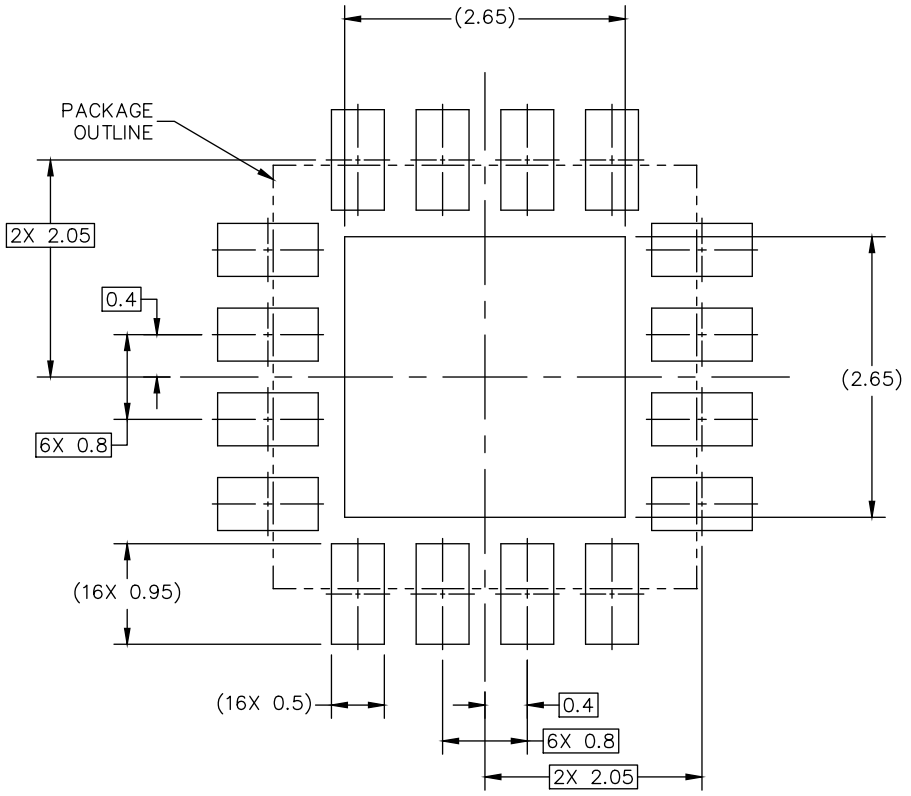
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**Figure 118. Reflow soldering footprint part 4 for HLQFN16 (dimple deburr wettable flank)**

H−PQFN−16 I/O 0.13 DIMPLE WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688−3(DD)




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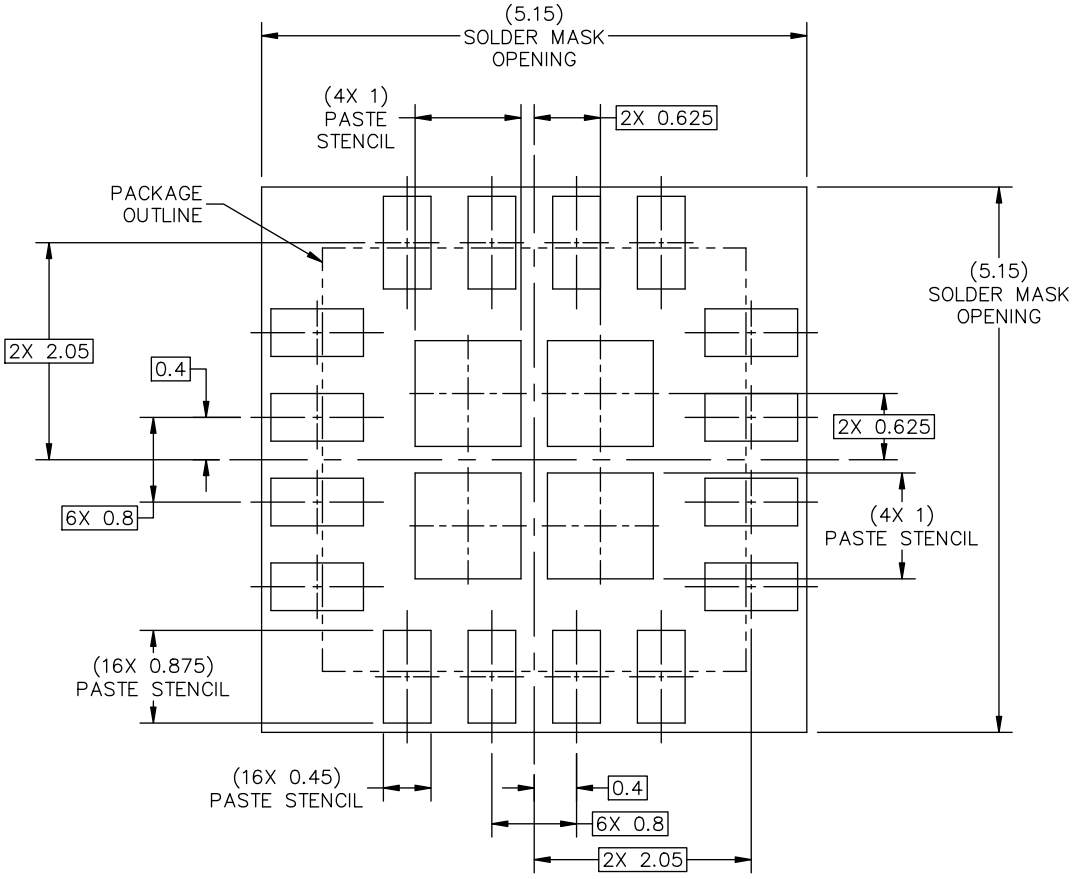
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|---|---|---|---|---|

**Figure 119. Reflow soldering footprint part 5 for HLQFN16 (dimple deburr wettable flank)**

H−PQFN−16 I/O 0.13 DIMPLE WETTABLE FLANK
4 X 4 X 1.45 PKG, 0.8 PITCH

SOT1688−3(DD)




RECOMMENDED STENCIL THICKNESS 0.125 OR 0.150

ALTERNATE SOLDER MASK OPENING AND PASTE STENCIL DESIGN GUIDELINES

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## Revision history

Table 344. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 12-Jun-2026 | 1 | Initial release from ST, rebranded NXP document |

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