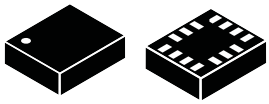
LSM6DSOP

iNEMO inertial module: always-on 3D accelerometer and 3D gyroscope

Datasheet - production data



LGA-14L
(2.5 x 3 x 0.83 mm) typ.

Features

- Power consumption: 0.55 mA in combo high-performance mode
- “Always-on" experience with low power consumption for both accelerometer and gyroscope
- Smart FIFO up to 9 kbytes
- ±2/±4/±8/±16 *g* full scale
- ±125/±250/±500/±1000/±2000 dps full scale
- Analog supply voltage: 1.71 V to 3.6 V
- Independent IO supply (1.62 V)
- Compact footprint: 2.5 mm x 3 mm x 0.83 mm
- SPI / I²C serial interface with main processor data synchronization
- Standard interrupts: wakeup, 6D/4D orientation, activity/inactivity recognition, stationary/motion detection
- Programmable Finite State Machine: accelerometer, gyroscope
- Embedded temperature sensor
- ECOPACK, RoHS and “Green” compliant

Applications

- Specific for smart pen applications

Description

The LSM6DSOP is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope boosting performance at 0.55 mA in high-performance mode and enabling always-on low-power features for an optimal motion experience for the consumer.

The LSM6DSOP has been designed for smart pen applications, offering multiple power modes and also real, virtual and batch sensors with 9 kbytes for dynamic data batching. ST’s family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LSM6DSOP has a full-scale acceleration range of ±2/±4/±8/±16 *g* and an angular rate range of ±125/±250/±500/±1000/±2000 dps.

High robustness to mechanical shock makes the LSM6DSOP the preferred choice of system designers for the creation and manufacturing of reliable products. The LSM6DSOP is available in a plastic land grid array (LGA) package.

For further information, please contact your local ST sales office or your distributor.

Table 1. Device summary

Part number	Temp. range [°C]	Package	Packing
LSM6DSOPTR	-40 to +85	LGA-14L (2.5x3x0.83 mm)	Tape & Reel

This is information on a product in full production. www.st.com

Contents

1 **Overview** 13

2 **Embedded low-power features** 14

2.1 Finite State Machine 14

3 **Pin description** 16

3.1 Pin connections 17

4 **Module specifications** 18

4.1 Mechanical characteristics 18

4.2 Electrical characteristics 21

4.3 Temperature sensor characteristics 22

4.4 Communication interface characteristics 23

4.4.1 SPI - serial peripheral interface 23

4.4.2 I²C - inter-IC control interface 24

4.5 Absolute maximum ratings 25

4.6 Terminology 26

4.6.1 Sensitivity 26

4.6.2 Zero-g and zero-rate level 26

5 **Digital interfaces** 27

5.1 I²C/SPI interface 27

5.1.1 I²C serial interface 27

5.1.2 SPI bus interface 30

6 **Functionality** 34

6.1 Operating modes 34

6.2 Accelerometer power modes 34

6.2.1 Accelerometer ultra-low-power mode 34

6.3 Gyroscope power modes 35

6.4 Block diagram of filters 35

6.4.1 Block diagrams of the accelerometer filters 35

6.4.2 Block diagrams of the gyroscope filters 37

6.5 FIFO 38
6.5.1 Bypass mode 39
6.5.2 FIFO mode 39
6.5.3 Continuous mode 39
6.5.4 Continuous-to-FIFO mode 39
6.5.5 Bypass-to-Continuous mode 40
6.5.6 Bypass-to-FIFO mode 40
6.5.7 FIFO reading procedure 40

7 Application hints 41
7.1 LSM6DSOP electrical connections 41

8 Register mapping 44

9 Register description 47
9.1 FUNC_CFG_ACCESS (01h) 47
9.2 PIN_CTRL (02h) 47
9.3 FIFO_CTRL1 (07h) 48
9.4 FIFO_CTRL2 (08h) 48
9.5 FIFO_CTRL3 (09h) 49
9.6 FIFO_CTRL4 (0Ah) 50
9.7 COUNTER_BDR_REG1 (0Bh) 51
9.8 COUNTER_BDR_REG2 (0Ch) 51
9.9 INT_CTRL (0Dh) 52
9.10 WHO_AM_I (0Fh) 52
9.11 CTRL1_XL (10h) 53
9.12 CTRL2_G (11h) 54
9.13 CTRL3_C (12h) 55
9.14 CTRL4_C (13h) 56
9.15 CTRL5_C (14h) 57
9.16 CTRL6_C (15h) 58
9.17 CTRL7_G (16h) 59
9.18 CTRL8_XL (17h) 60
9.19 CTRL9_XL (18h) 62
9.20 CTRL10_C (19h) 62

9.21 ALL_INT_SRC (1Ah) . . . 63
9.22 WAKE_UP_SRC (1Bh) . . . 63
9.23 D6D_SRC (1Dh) . . . 64
9.24 STATUS_REG (1Eh) . . . 64
9.25 OUT_TEMP_L (20h), OUT_TEMP_H (21h) . . . 65
9.26 OUTX_L_G (22h) and OUTX_H_G (23h) . . . 65
9.27 OUTY_L_G (24h) and OUTY_H_G (25h) . . . 65
9.28 OUTZ_L_G (26h) and OUTZ_H_G (27h) . . . 66
9.29 OUTX_L_A (28h) and OUTX_H_A (29h) . . . 66
9.30 OUTY_L_A (2Ah) and OUTY_H_A (2Bh) . . . 67
9.31 OUTZ_L_A (2Ch) and OUTZ_H_A (2Dh) . . . 67
9.32 EMB_FUNC_STATUS_MAINPAGE (35h) . . . 68
9.33 FSM_STATUS_A_MAINPAGE (36h) . . . 68
9.34 FSM_STATUS_B_MAINPAGE (37h) . . . 69
9.35 FIFO_STATUS1 (3Ah) . . . 69
9.36 FIFO_STATUS2 (3Bh) . . . 70
9.37 TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h) . . . 71
9.38 LIR_CONFIG (56h) . . . 71
9.39 INT_CFG (58h) . . . 72
9.40 THS_6D (59h) . . . 72
9.41 WAKE_UP_THS (5Bh) . . . 73
9.42 WAKE_UP_DUR (5Ch) . . . 73
9.43 MD1_CFG (5Eh) . . . 74
9.44 INT_PD_CFG (62h) . . . 75
9.45 INTERNAL_FREQ_FINE (63h) . . . 75
9.46 X_OFS_USR (73h) . . . 75
9.47 Y_OFS_USR (74h) . . . 76
9.48 Z_OFS_USR (75h) . . . 76
9.49 FIFO_DATA_OUT_TAG (78h) . . . 76
9.50 FIFO_DATA_OUT_X_L (79h) and FIFO_DATA_OUT_X_H (7Ah) . . . 78
9.51 FIFO_DATA_OUT_Y_L (7Bh) and FIFO_DATA_OUT_Y_H (7Ch) . . . 78
9.52 FIFO_DATA_OUT_Z_L (7Dh) and FIFO_DATA_OUT_Z_H (7Eh) . . . 78

10 Embedded functions register mapping 79

11 Embedded functions register description 81

11.1 PAGE_SEL (02h) 81
11.2 EMB_FUNC_EN_B (05h) 81
11.3 PAGE_ADDRESS (08h) 81
11.4 PAGE_VALUE (09h) 82
11.5 EMB_FUNC_INT (0Ah) 82
11.6 FSM_INT_A (0Bh) 83
11.7 FSM_INT_B (0Ch) 84
11.8 EMB_FUNC_STATUS (12h) 85
11.9 FSM_STATUS_A (13h) 85
11.10 FSM_STATUS_B (14h) 86
11.11 PAGE_RW (17h) 86
11.12 FSM_ENABLE_A (46h) 87
11.13 FSM_ENABLE_B (47h) 87
11.14 FSM_LONG_COUNTER_L (48h) and FSM_LONG_COUNTER_H (49h) 88
11.15 FSM_LONG_COUNTER_CLEAR (4Ah) 88
11.16 FSM_OUTS1 (4Ch) 89
11.17 FSM_OUTS2 (4Dh) 89
11.18 FSM_OUTS3 (4Eh) 90
11.19 FSM_OUTS4 (4Fh) 90
11.20 FSM_OUTS5 (50h) 91
11.21 FSM_OUTS6 (51h) 91
11.22 FSM_OUTS7 (52h) 92
11.23 FSM_OUTS8 (53h) 92
11.24 FSM_OUTS9 (54h) 93
11.25 FSM_OUTS10 (55h) 93
11.26 FSM_OUTS11 (56h) 94
11.27 FSM_OUTS12 (57h) 94
11.28 FSM_OUTS13 (58h) 95
11.29 FSM_OUTS14 (59h) 95
11.30 FSM_OUTS15 (5Ah) 96

11.31 FSM_OUTS16 (5Bh) 96
11.32 EMB_FUNC_ODR_CFG_B (5Fh) 97
11.33 EMB_FUNC_INIT_B (67h) 97

12 Embedded advanced features pages 98

13 Embedded advanced features register description 99
13.1 Page 1 - Embedded advanced features registers 99
13.1.1 FSM_LC_TIMEOUT_L (7Ah) and FSM_LC_TIMEOUT_H (7Bh) 99
13.1.2 FSM_PROGRAMS (7Ch) 99
13.1.3 FSM_START_ADD_L (7Eh) and FSM_START_ADD_H (7Fh) 100

14 Pull-up configuration register 101
14.1 PU_CONFIG (14h) 101

15 Soldering information 102

16 Package information 103
16.1 LGA-14L package information 103
16.2 LGA-14 packing information 104

17 Revision history 106

List of tables

Table 1. Device summary . . . 1
Table 2. Pin description . . . 17
Table 3. Mechanical characteristics . . . 18
Table 4. Electrical characteristics . . . 21
Table 5. Temperature sensor characteristics . . . 22
Table 6. SPI slave timing values (in mode 3) . . . 23
Table 7. I²C slave timing values . . . 24
Table 8. Absolute maximum ratings . . . 25
Table 9. Serial interface pin description . . . 27
Table 10. I²C terminology . . . 27
Table 11. SAD+Read/Write patterns . . . 28
Table 12. Transfer when master is writing one byte to slave . . . 28
Table 13. Transfer when master is writing multiple bytes to slave . . . 28
Table 14. Transfer when master is receiving (reading) one byte of data from slave . . . 29
Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave . . . 29
Table 16. Gyroscope LPF2 bandwidth selection . . . 37
Table 17. Internal pin status . . . 42
Table 18. Registers address map . . . 44
Table 19. FUNC_CFG_ACCESS register . . . 47
Table 20. FUNC_CFG_ACCESS register description . . . 47
Table 21. PIN_CTRL register . . . 47
Table 22. PIN_CTRL register description . . . 47
Table 23. FIFO_CTRL1 register . . . 48
Table 24. FIFO_CTRL1 register description . . . 48
Table 25. FIFO_CTRL2 register . . . 48
Table 26. FIFO_CTRL2 register description . . . 48
Table 27. FIFO_CTRL3 register . . . 49
Table 28. FIFO_CTRL3 register description . . . 49
Table 29. FIFO_CTRL4 register . . . 50
Table 30. FIFO_CTRL4 register description . . . 50
Table 31. COUNTER_BDR_REG1 register . . . 51
Table 32. COUNTER_BDR_REG1 register description . . . 51
Table 33. COUNTER_BDR_REG2 register . . . 51
Table 34. COUNTER_BDR_REG2 register description . . . 51
Table 35. INT_CTRL register . . . 52
Table 36. INT_CTRL register description . . . 52
Table 37. WhoAmI register . . . 52
Table 38. CTRL1_XL register . . . 53
Table 39. CTRL1_XL register description . . . 53
Table 40. Accelerometer ODR register setting . . . 53
Table 41. Accelerometer full-scale selection . . . 53
Table 42. CTRL2_G register . . . 54
Table 43. CTRL2_G register description . . . 54
Table 44. Gyroscope ODR configuration setting . . . 54
Table 45. CTRL3_C register . . . 55
Table 46. CTRL3_C register description . . . 55
Table 47. CTRL4_C register . . . 56
Table 48. CTRL4_C register description . . . 56

Table 49. CTRL5_C register . . . 57
Table 50. CTRL5_C register description . . . 57
Table 51. Angular rate sensor self-test mode selection . . . 57
Table 52. Linear acceleration sensor self-test mode selection . . . 57
Table 53. CTRL6_C register . . . 58
Table 54. CTRL6_C register description . . . 58
Table 55. Gyroscope LPF1 bandwidth selection . . . 58
Table 56. CTRL7_G register . . . 59
Table 57. CTRL7_G register description . . . 59
Table 58. CTRL8_XL register . . . 60
Table 59. CTRL8_XL register description . . . 60
Table 60. Accelerometer bandwidth configurations . . . 60
Table 61. CTRL9_XL register . . . 62
Table 62. CTRL9_XL register description . . . 62
Table 63. CTRL10_C register . . . 62
Table 64. CTRL10_C register description . . . 62
Table 65. ALL_INT_SRC register . . . 63
Table 66. ALL_INT_SRC register description . . . 63
Table 67. WAKE_UP_SRC register . . . 63
Table 68. WAKE_UP_SRC register description . . . 63
Table 69. D6D_SRC register . . . 64
Table 70. D6D_SRC register description . . . 64
Table 71. STATUS_REG register . . . 64
Table 72. STATUS_REG register description . . . 64
Table 73. OUT_TEMP_L register . . . 65
Table 74. OUT_TEMP_H register . . . 65
Table 75. OUT_TEMP register description . . . 65
Table 76. OUTX_L_G register . . . 65
Table 77. OUTX_H_G register . . . 65
Table 78. OUTX_H_G register description . . . 65
Table 79. OUTY_L_G register . . . 65
Table 80. OUTY_H_G register . . . 65
Table 81. OUTY_H_G register description . . . 65
Table 82. OUTZ_L_G register . . . 66
Table 83. OUTZ_H_G register . . . 66
Table 84. OUTZ_H_G register description . . . 66
Table 85. OUTX_L_A register . . . 66
Table 86. OUTX_H_A register . . . 66
Table 87. OUTX_H_A register description . . . 66
Table 88. OUTY_L_A register . . . 67
Table 89. OUTY_H_A register . . . 67
Table 90. OUTY_H_A register description . . . 67
Table 91. OUTZ_L_A register . . . 67
Table 92. OUTZ_H_A register . . . 67
Table 93. OUTZ_H_A register description . . . 67
Table 94. EMB_FUNC_STATUS_MAINPAGE register . . . 68
Table 95. EMB_FUNC_STATUS_MAINPAGE register description . . . 68
Table 96. FSM_STATUS_A_MAINPAGE register . . . 68
Table 97. FSM_STATUS_A_MAINPAGE register description . . . 68
Table 98. FSM_STATUS_B_MAINPAGE register . . . 69
Table 99. FSM_STATUS_B_MAINPAGE register description . . . 69
Table 100. FIFO_STATUS1 register . . . 69

Table 101. FIFO_STATUS1 register description . . . 69
Table 102. FIFO_STATUS2 register. . . . 70
Table 103. FIFO_STATUS2 register description . . . 70
Table 104. TIMESTAMP output registers . . . 71
Table 105. TIMESTAMP output register description. . . . 71
Table 106. LIR_CONFIG register . . . 71
Table 107. LIR_CONFIG register description . . . 71
Table 108. INT_CFG register . . . 72
Table 109. INT_CFG register description . . . 72
Table 110. THS_6D register . . . 72
Table 111. THS_6D register description. . . . 72
Table 112. Threshold for D4D/D6D function. . . . 72
Table 113. WAKE_UP_THS register . . . 73
Table 114. WAKE_UP_THS register description . . . 73
Table 115. WAKE_UP_DUR register . . . 73
Table 116. WAKE_UP_DUR register description . . . 73
Table 117. MD1_CFG register . . . 74
Table 118. MD1_CFG register description . . . 74
Table 119. INT_PD_CFG register. . . . 75
Table 120. INT_PD_CFG register description . . . 75
Table 121. INTERNAL_FREQ_FINE register . . . 75
Table 122. INTERNAL_FREQ_FINE register description. . . . 75
Table 123. X_OFS_USR register . . . 75
Table 124. X_OFS_USR register description . . . 75
Table 125. Y_OFS_USR register . . . 76
Table 126. Y_OFS_USR register description . . . 76
Table 127. Z_OFS_USR register . . . 76
Table 128. Z_OFS_USR register description . . . 76
Table 129. FIFO_DATA_OUT_TAG register . . . 76
Table 130. FIFO_DATA_OUT_TAG register description . . . 76
Table 131. FIFO tag . . . 77
Table 132. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L registers . . . 78
Table 133. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L register description . . . 78
Table 134. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L registers . . . 78
Table 135. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L register description . . . 78
Table 136. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L registers . . . 78
Table 137. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L register description. . . . 78
Table 138. Register address map - embedded functions . . . 79
Table 139. PAGE_SEL register . . . 81
Table 140. PAGE_SEL register description . . . 81
Table 141. EMB_FUNC_EN_B register . . . 81
Table 142. EMB_FUNC_EN_B register description . . . 81
Table 143. PAGE_ADDRESS register . . . 81
Table 144. PAGE_ADDRESS register description . . . 81
Table 145. PAGE_VALUE register . . . 82
Table 146. PAGE_VALUE register description. . . . 82
Table 147. EMB_FUNC_INT register . . . 82
Table 148. EMB_FUNC_INT register description . . . 82
Table 149. FSM_INT_A register . . . 83
Table 150. FSM_INT_A register description. . . . 83
Table 151. FSM_INT_B register . . . 84
Table 152. FSM_INT_B register description. . . . 84

Table 153. EMB_FUNC_STATUS register . . . 85
Table 154. EMB_FUNC_STATUS register description . . . 85
Table 155. FSM_STATUS_A register . . . 85
Table 156. FSM_STATUS_A register description . . . 85
Table 157. FSM_STATUS_B register . . . 86
Table 158. FSM_STATUS_B register description . . . 86
Table 159. PAGE_RW register . . . 86
Table 160. PAGE_RW register description . . . 86
Table 161. FSM_ENABLE_A register . . . 87
Table 162. FSM_ENABLE_A register description . . . 87
Table 163. FSM_ENABLE_B register . . . 87
Table 164. FSM_ENABLE_B register description . . . 87
Table 165. FSM_LONG_COUNTER_L register . . . 88
Table 166. FSM_LONG_COUNTER_L register description . . . 88
Table 167. FSM_LONG_COUNTER_H register . . . 88
Table 168. FSM_LONG_COUNTER_H register description . . . 88
Table 169. FSM_LONG_COUNTER_CLEAR register . . . 88
Table 170. FSM_LONG_COUNTER_CLEAR register description . . . 88
Table 171. FSM_OUTS1 register . . . 89
Table 172. FSM_OUTS1 register description . . . 89
Table 173. FSM_OUTS2 register . . . 89
Table 174. FSM_OUTS2 register description . . . 89
Table 175. FSM_OUTS3 register . . . 90
Table 176. FSM_OUTS3 register description . . . 90
Table 177. FSM_OUTS4 register . . . 90
Table 178. FSM_OUTS4 register description . . . 90
Table 179. FSM_OUTS5 register . . . 91
Table 180. FSM_OUTS5 register description . . . 91
Table 181. FSM_OUTS6 register . . . 91
Table 182. FSM_OUTS6 register description . . . 91
Table 183. FSM_OUTS7 register . . . 92
Table 184. FSM_OUTS7 register description . . . 92
Table 185. FSM_OUTS8 register . . . 92
Table 186. FSM_OUTS8 register description . . . 92
Table 187. FSM_OUTS9 register . . . 93
Table 188. FSM_OUTS9 register description . . . 93
Table 189. FSM_OUTS10 register . . . 93
Table 190. FSM_OUTS10 register description . . . 93
Table 191. FSM_OUTS11 register . . . 94
Table 192. FSM_OUTS11 register description . . . 94
Table 193. FSM_OUTS12 register . . . 94
Table 194. FSM_OUTS12 register description . . . 94
Table 195. FSM_OUTS13 register . . . 95
Table 196. FSM_OUTS13 register description . . . 95
Table 197. FSM_OUTS14 register . . . 95
Table 198. FSM_OUTS14 register description . . . 95
Table 199. FSM_OUTS15 register . . . 96
Table 200. FSM_OUTS15 register description . . . 96
Table 201. FSM_OUTS16 register . . . 96
Table 202. FSM_OUTS16 register description . . . 96
Table 203. EMB_FUNC_ODR_CFG_B register . . . 97
Table 204. EMB_FUNC_ODR_CFG_B register description . . . 97

Table 205. EMB_FUNC_INIT_B register . . . 97
Table 206. EMB_FUNC_INIT_B register description . . . 97
Table 207. Register address map - embedded advanced features page 1 . . . 98
Table 208. FSM_LC_TIMEOUT_L register. . . . 99
Table 209. FSM_LC_TIMEOUT_L register description . . . 99
Table 210. FSM_LC_TIMEOUT_H register . . . 99
Table 211. FSM_LC_TIMEOUT_H register description . . . 99
Table 212. FSM_PROGRAMS register . . . 99
Table 213. FSM_PROGRAMS register description . . . 99
Table 214. FSM_START_ADD_L register . . . 100
Table 215. FSM_START_ADD_L register description . . . 100
Table 216. FSM_START_ADD_H register . . . 100
Table 217. FSM_START_ADD_H register description . . . 100
Table 218. Pull-up configuration register . . . 101
Table 219. PU_CONFIG register . . . 101
Table 220. PU_CONFIG register description . . . 101
Table 221. Reel dimensions for carrier tape of LGA-14 package . . . 105
Table 222. Document revision history. . . . 106

List of figures

Figure 1. Generic state machine . . . 14
Figure 2. State machine in the LSM6DSOP . . . 15
Figure 3. Pin connections . . . 16
Figure 4. LSM6DSOP connections . . . 17
Figure 5. SPI slave timing diagram (in mode 3) . . . 23
Figure 6. I²C slave timing diagram . . . 24
Figure 7. Read and write protocol (in mode 3) . . . 30
Figure 8. SPI read protocol (in mode 3) . . . 31
Figure 9. Multiple byte SPI read protocol (2-byte example) (in mode 3) . . . 31
Figure 10. SPI write protocol (in mode 3) . . . 32
Figure 11. Multiple byte SPI write protocol (2-byte example) (in mode 3) . . . 32
Figure 12. SPI read protocol in 3-wire mode (in mode 3) . . . 33
Figure 13. Block diagram of filters . . . 35
Figure 14. Accelerometer chain . . . 35
Figure 15. Accelerometer composite filter . . . 36
Figure 16. Gyroscope digital chain . . . 37
Figure 17. LSM6DSOP electrical connections . . . 41
Figure 18. Accelerometer block diagram . . . 61
Figure 19. LGA-14L 2.5x3x0.86 mm package outline and mechanical data . . . 103
Figure 20. Carrier tape information for LGA-14 package . . . 104
Figure 21. LGA-14 package orientation in carrier tape . . . 104
Figure 22. Reel information for carrier tape of LGA-14 package . . . 105

1 Overview

The LSM6DSOP is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope, designed for smart pen applications.

The LSM6DSOP delivers best-in-class motion sensing that can detect orientation and gestures in order to empower application developers and consumers with features and capabilities that are more sophisticated than simply orienting their devices to portrait and landscape mode.

The event-detection interrupts enable efficient and reliable motion tracking and contextual awareness, implementing hardware recognition of 6D orientation, activity or inactivity, stationary/motion detection and wakeup events.

The LSM6DSOP supports main OS requirements, offering real, virtual and batch mode sensors.

Up to 9 kbytes of FIFO with compression and dynamic allocation of significant data allows overall power saving of the system.

Like the entire portfolio of MEMS sensor modules, the LSM6DSOP leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LSM6DSOP is available in a small plastic land grid array (LGA) package of 2.5 x 3.0 x 0.83 mm to address ultra-compact solutions.

2 Embedded low-power features

The LSM6DSOP features the following on-chip functions:

- 9 kbytes data buffering, data can be compressed two or three times
  - 100% efficiency with flexible configurations and partitioning
  - Possibility to store timestamp
- Event-detection interrupts (fully configurable):
  - Wakeup
  - 6D orientation
  - Activity/inactivity recognition
  - Stationary/Motion detection
- Specific IP blocks with negligible power consumption and high-performance:
  - Finite State Machine (FSM) for accelerometer, gyroscope

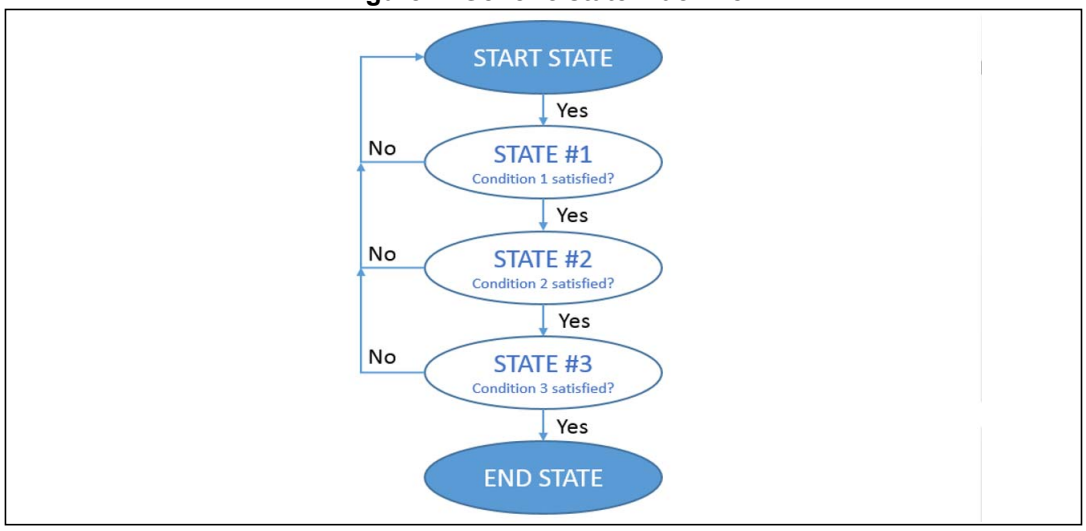
2.1 Finite State Machine

The LSM6DSOP can be configured to generate interrupt signals activated by user-defined motion patterns. To do this, up to 16 embedded finite state machines can be programmed independently for motion detection such as glance gestures, absolute wrist tilt, shake and double-shake detection.

Definition of Finite State Machine

A state machine is a mathematical abstraction used to design logic connections. It is a behavioral model composed of a finite number of states and transitions between states, similar to a flow chart in which one can inspect the way logic runs when certain conditions are met. The state machine begins with a start state, goes to different states through transitions dependent on the inputs, and can finally end in a specific state (called stop state). The current state is determined by the past states of the system. *Figure 1: Generic state machine* shows a generic state machine.

Figure 1. Generic state machine

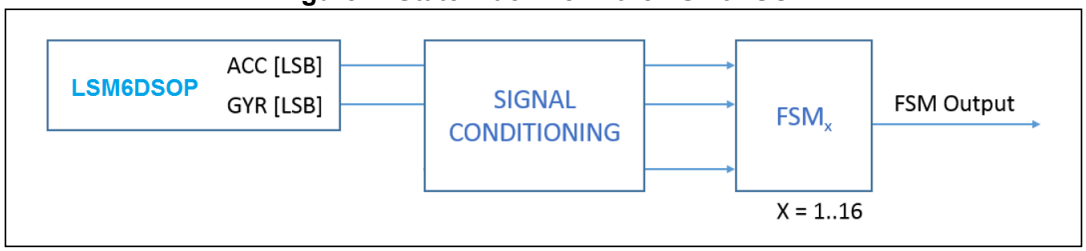


Finite State Machine in the LSM6DSOP

The LSM6DSOP works as a combo accelerometer-gyroscope sensor, generating acceleration and angular rate output data.

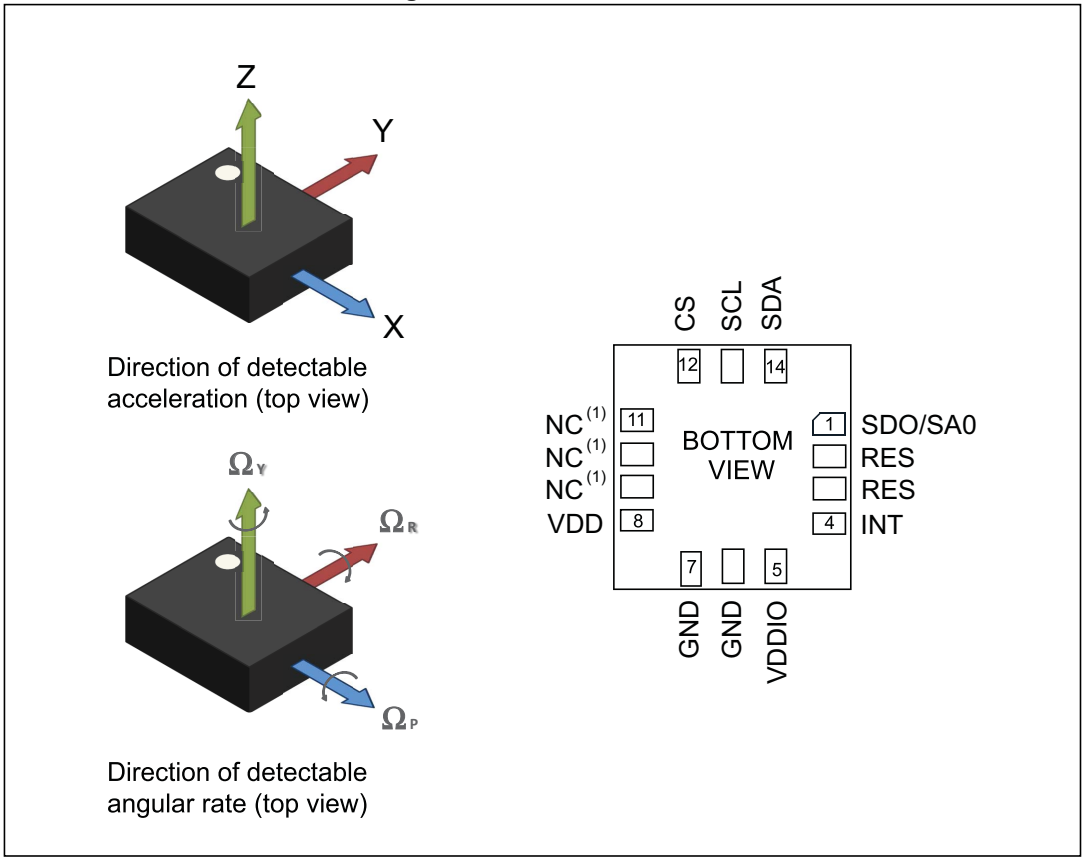
All 16 finite state machines are independent: each one has its dedicated memory area and it is independently executed. An interrupt is generated when the end state is reached or when some specific command is performed.

Figure 2. State machine in the LSM6DSOP



3 Pin description

Figure 3. Pin connections



1. Leave pin electrically unconnected and soldered to PCB.

Table 2. Pin description

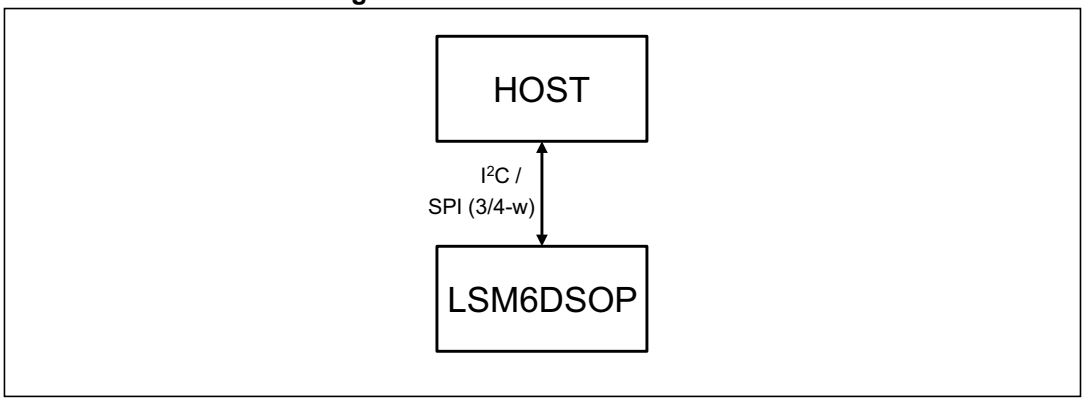
Pin#	Name	Function
1	SDO	SPI 4-wire interface serial data output (SDO)
	SA0	I²C least significant bit of the device address (SA0)
2	RES	Connect to VDDIO or GND
3	RES	Connect to VDDIO or GND
4	INT(1)	Programmable interrupt
5	VDDIO(2)	Power supply for I/O pins
6	GND	0 V supply
7	GND	0 V supply
8	VDD(2)	Power supply
9	NC	Leave unconnected(3)
10	NC	Leave unconnected(3)
11	NC	Leave unconnected(3)
12	CS	I²C / SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
13	SCL	I²C serial clock (SCL) SPI serial port clock (SPC)
14	SDA	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

1. INT must be set to '0' or left unconnected during power-on.
2. Recommended 100 nF filter capacitor.
3. Leave pin electrically unconnected and soldered to PCB.

3.1 Pin connections

The LSM6DSOP offers an I²C slave interface or SPI (3- and 4-wire) serial interface.

Figure 4. LSM6DSOP connections



4 Module specifications

4.1 Mechanical characteristics

@ Vdd = 1.8 V, T = 25 °C, unless otherwise noted.

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
				±16		
G_FS	Angular rate measurement range			±125		dps
				±250		
				±500		
				±1000		
				±2000		
LA_So	Linear acceleration sensitivity(2)	FS = ±2 *g*		0.061		mg/LSB
		FS = ±4 *g*		0.122		
		FS = ±8 *g*		0.244		
		FS = ±16 *g*		0.488		
G_So	Angular rate sensitivity(2)	FS = ±125 dps		4.375		mdps/LSB
		FS = ±250 dps		8.75		
		FS = ±500 dps		17.50		
		FS = ±1000 dps		35		
		FS = ±2000 dps		70		
LA_SoDr	Linear acceleration sensitivity change vs. temperature(3)	from -40° to +85° C		±0.01		%/°C
G_SoDr	Angular rate sensitivity change vs. temperature(3)	from -40° to +85° C		±0.007		%/°C
High-performance mode (HPM)						
LA_TyOff	Linear acceleration zero-*g* level offset accuracy(4)			20		m*g*
G_TyOff	Angular rate zero-rate level (4)			1		dps
Advanced power cycling mode (APC)						
LA_TyOff	Linear acceleration zero-*g* level offset accuracy(4)			20		m*g*
G_TyOff	Angular rate zero-rate level (4)			1		dps

Table 3. Mechanical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_OffDr	Linear acceleration zero-*g* level change vs. temperature(3)			±0.1		m*g*/ °C
G_OffDr	Angular rate typical zero-rate level change vs. temperature(3)			±0.015		dps/°C
Rn	Rate noise density in high-performance mode(5)			3.8		mdps/√Hz
APC_{RMS}(6)	Gyroscope RMS noise in APC mode			60		mdps
An	Acceleration noise density in high-performance mode(7)	FS = ±2 *g*		70		µ*g*/√Hz
RMS	Acceleration RMS noise in normal/low-power mode(8)(9)	FS = ±2 *g*		1.8		m*g*(RMS)
	Acceleration RMS noise in ultra-low-power mode(8)(9)			5.5		
	Acceleration RMS noise in advanced power cycling mode			5.5		
LA_ODR	Linear acceleration output data rate			1.6(10) 12.5 26 52 104 208 416 833 1666 3332 6664		Hz
G_ODR	Angular rate output data rate			12.5 26 52 104 208 416 833 1666 3332 6664		
Vst	Linear acceleration self-test output change(11)(12)(13)		50		1700	m*g*
	Angular rate self-test output change(14)(15)	FS = ±250 dps	20		80	dps
		FS = ±2000 dps	150		700	dps
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Sensitivity values after factory calibration test and trimming.

3. Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples. Not measured during final test for production.
4. Values after factory calibration test and trimming.
5. Gyroscope rate noise density in high-performance mode is independent of the ODR and FS setting.
6. For further information, please contact your local ST sales office or your distributor.
7. Accelerometer noise density in high-performance mode is independent of the ODR.
8. Accelerometer RMS noise in normal/low-power/ultra-low-power mode is independent of the ODR.
9. Noise RMS related to BW = ODR/2.
10. This ODR is available when the accelerometer is in low-power mode.
11. The sign of the linear acceleration self-test output change is defined by the STx_XL bits in a dedicated register for all axes.
12. The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 0.061 m*g* at ±2 *g* full scale.
13. Accelerometer self-test limits are full-scale independent.
14. The sign of the angular rate self-test output change is defined by the STx_G bits in a dedicated register for all axes.
15. The angular rate self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 70 mdps at ±2000 dps full scale.

4.2 Electrical characteristics

@ Vdd = 1.8 V, T = 25 °C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.71	1.8	3.6	V
Vdd_IO	Power supply for I/O		1.62		3.6	V
IddHP	Gyroscope and accelerometer current consumption in high-performance mode			0.55		mA
IddAPC	Gyroscope and accelerometer current consumption in advanced power cycling mode(2)			245		µA
LA_IddHP	Accelerometer current consumption in high-performance mode			170		µA
LA_IddLP	Accelerometer current consumption in low-power mode	ODR = 52 Hz ODR = 1.6 Hz		26 4.5		µA
LA_IddULP	Accelerometer current consumption in ultra-low-power mode	ODR = 52 Hz ODR = 1.6 Hz		9.5 4.4		µA
		ODR = 26 Hz(2)		7		µA
IddPD	Gyroscope and accelerometer current consumption during power-down(2)			3		µA
Ton	Turn-on time			35	70	ms
V_{IH}	Digital high-level input voltage		0.7 * VDD_IO			V
V_{IL}	Digital low-level input voltage				0.3 * VDD_IO	V
V_{OH}	High-level output voltage	I_{OH} = 4 mA(3)	VDD_IO - 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA(3)			0.2	V
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Data based on characterization results.
3. 4 mA is the maximum driving capability, i.e. the maximum DC current that can be sourced/sunk by the digital pin in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.

4.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TODR(2)	Temperature refresh rate			52		Hz
Toff	Temperature offset(3)		-15		+15	°C
TSen	Temperature sensitivity			256		LSB/°C
TST	Temperature stabilization time(4)				500	µs
T_ADC_res	Temperature ADC resolution			16		bit
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. When the accelerometer is in Low-Power mode or Ultra-Low-Power mode and the gyroscope part is turned off, the TODR value is equal to the accelerometer ODR.
3. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
4. Time from power ON to valid data based on characterization data.

4.4 Communication interface characteristics

4.4.1 SPI - serial peripheral interface

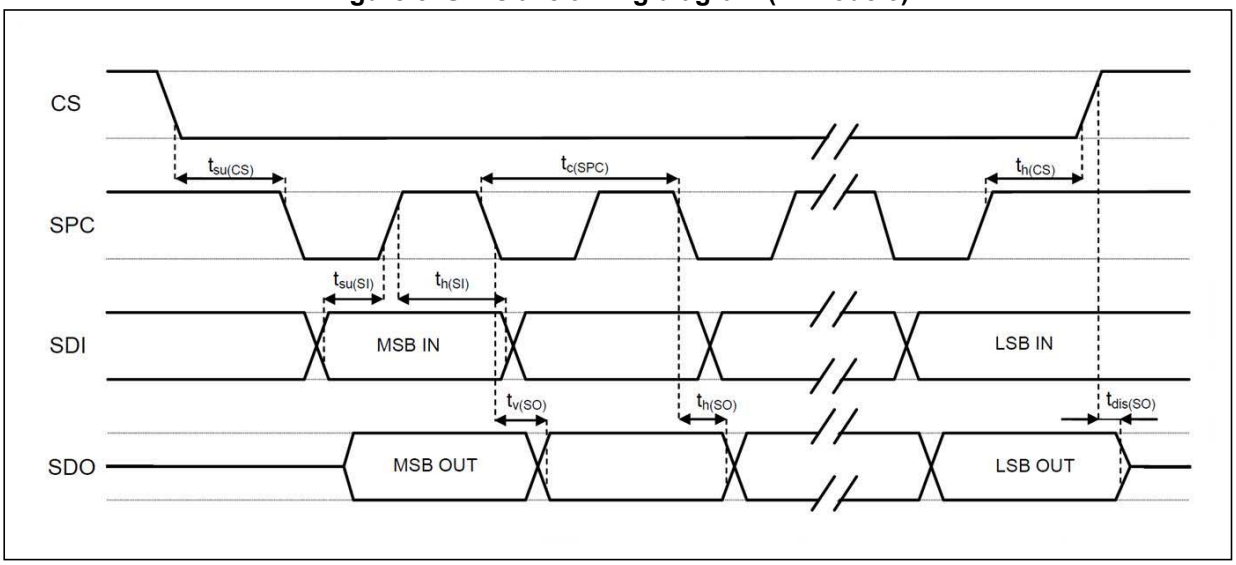
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values (in mode 3)

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 5. SPI slave timing diagram (in mode 3)



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

4.4.2 I²C - inter-IC control interface

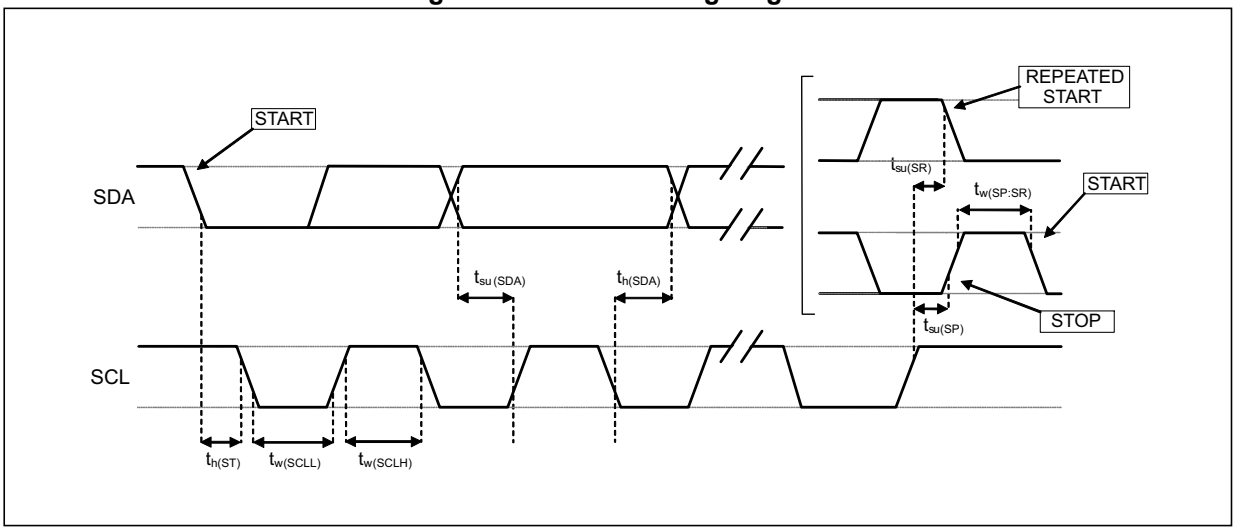
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode(1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 6. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

4.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration *g* for 0.2 ms	20,000	*g*
ESD	Electrostatic discharge protection (HBM)	2	kV
Vin	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4.6 Terminology

4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see *Table 3*).

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time (see *Table 3*).

4.6.2 Zero-*g* and zero-rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in *Table 3*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time (see *Table 3*).

5 Digital interfaces

5.1 I²C/SPI interface

The registers embedded inside the LSM6DSOP may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The serial interfaces are mapped onto the same pins. To select/exploit the I²C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 9. Serial interface pin description

Pin name	Pin description
CS	SPI enable I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
SCL/SPC	I²C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I²C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO/SA0	SPI Serial Data Output (SDO) I²C less significant bit of the device address

5.1.1 I²C serial interface

The LSM6DSOP I²C is a bus slave. The I²C is employed to write the data to the registers, whose content can also be read back.

The relevant I²C terminology is provided in the table below.

Table 10. I²C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the Serial DAta line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both the lines are high.

The I²C interface is implemented with fast mode (400 kHz) I²C standards as well as with standard mode.

In order to disable the I²C block, (I2C_disable) = 1 must be written in *CTRL4_C (13h)*.

I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave ADdress (SAD) associated to the LSM6DSOP is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is '1' (address 1101011b); else if the SDO/SA0 pin is connected to ground, the LSb value is '0' (address 1101010b). This solution permits to connect and address two different inertial modules to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM6DSOP behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The increment of the address is configured by the *CTRL3_C (12h)* (IF_INC).

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 11* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 11. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

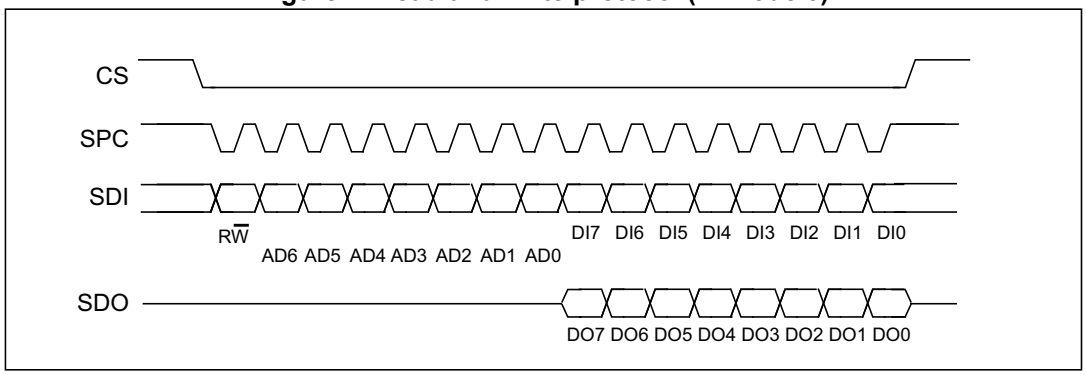
In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

5.1.2 SPI bus interface

The LSM6DSOP SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface communicates to the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 7. Read and write protocol (in mode 3)



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

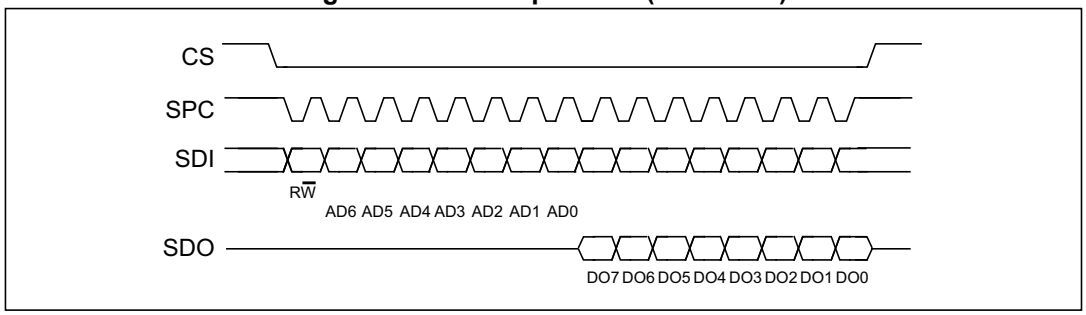
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the *CTRL3_C (12h)* (IF_INC) bit is ‘0’, the address used to read/write data remains the same for every block. When the *CTRL3_C (12h)* (IF_INC) bit is ‘1’, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

SPI read

Figure 8. SPI read protocol (in mode 3)



The SPI Read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

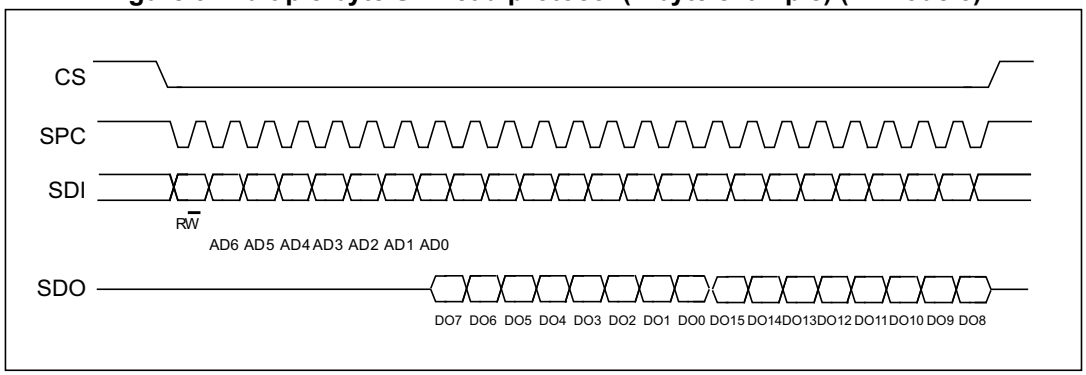
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

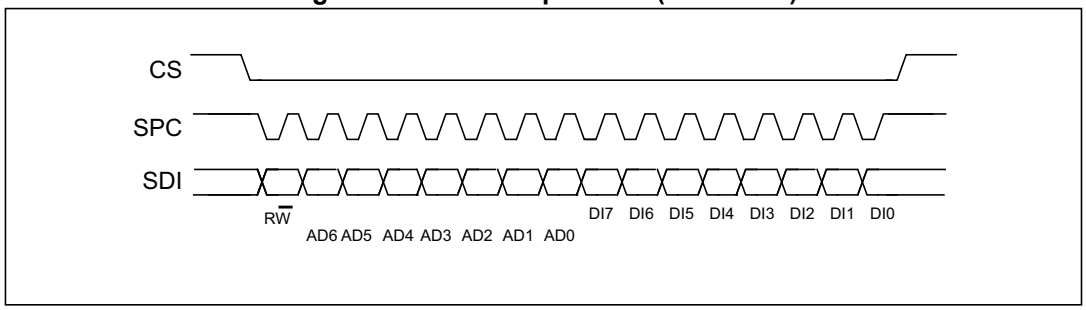
bit 16-...: data DO(...-8). Further data in multiple byte reads.

Figure 9. Multiple byte SPI read protocol (2-byte example) (in mode 3)



SPI write

Figure 10. SPI write protocol (in mode 3)



The SPI Write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

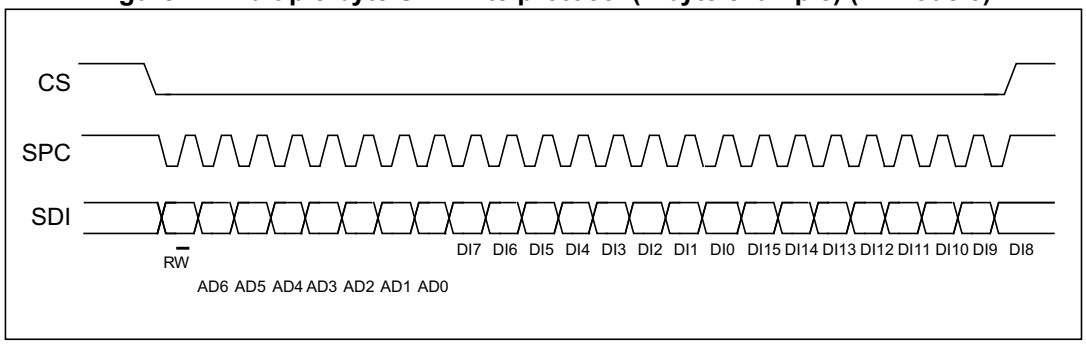
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

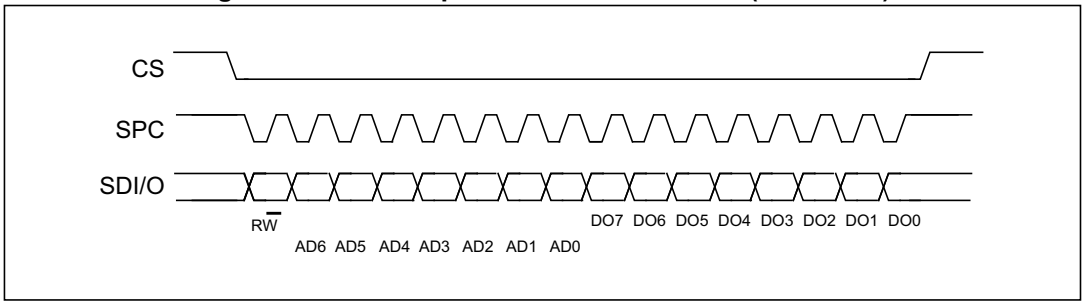
Figure 11. Multiple byte SPI write protocol (2-byte example) (in mode 3)



SPI read in 3-wire mode

A 3-wire mode is entered by setting the *CTRL3_C (12h)* (SIM) bit equal to '1' (SPI serial interface mode selection).

Figure 12. SPI read protocol in 3-wire mode (in mode 3)



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

6 Functionality

6.1 Operating modes

In the LSM6DSOP, the accelerometer and the gyroscope can be turned on/off independently of each other and are allowed to have different ODRs and power modes.

The LSM6DSOP has three operating modes available:

- only accelerometer active and gyroscope in power-down
- only gyroscope active and accelerometer in power-down
- both accelerometer and gyroscope sensors active with independent ODR

The accelerometer is activated from power-down by writing ODR_XL[3:0] in *CTRL1_XL (10h)* while the gyroscope is activated from power-down by writing ODR_G[3:0] in *CTRL2_G (11h)*. For combo-mode the ODRs are totally independent.

6.2 Accelerometer power modes

In the LSM6DSOP, the accelerometer can be configured in five different operating modes: power-down, ultra-low-power, low-power, normal mode and high-performance mode. The operating mode selected depends on the value of the XL_HM_MODE bit in *CTRL6_C (15h)*. If XL_HM_MODE is set to '0', high-performance mode is valid for all ODRs (from 12.5 Hz up to 6.66 kHz).

To enable the low-power and normal mode, the XL_HM_MODE bit has to be set to '1'. Low-power mode is available for lower ODRs (1.6, 12.5, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

6.2.1 Accelerometer ultra-low-power mode

The LSM6DSOP can be configured in ultra-low-power (ULP) mode by setting the XL_ULP_EN bit to 1 in *CTRL5_C (14h)* register. This mode can be used in accelerometer-only mode (gyroscope sensor must be configured in power-down mode) and for ODR_XL values between 1.6 Hz and 208 Hz.

When ULP mode is intended to be used, the bit XL_HM_MODE must be set to 0.

When ULP mode is switched ON/OFF, the accelerometer must be configured in power-down condition.

The embedded functions based on accelerometer data (6D/4D, wake-up, activity/inactivity) and the FIFO batching functionality are still supported when ULP mode is enabled.

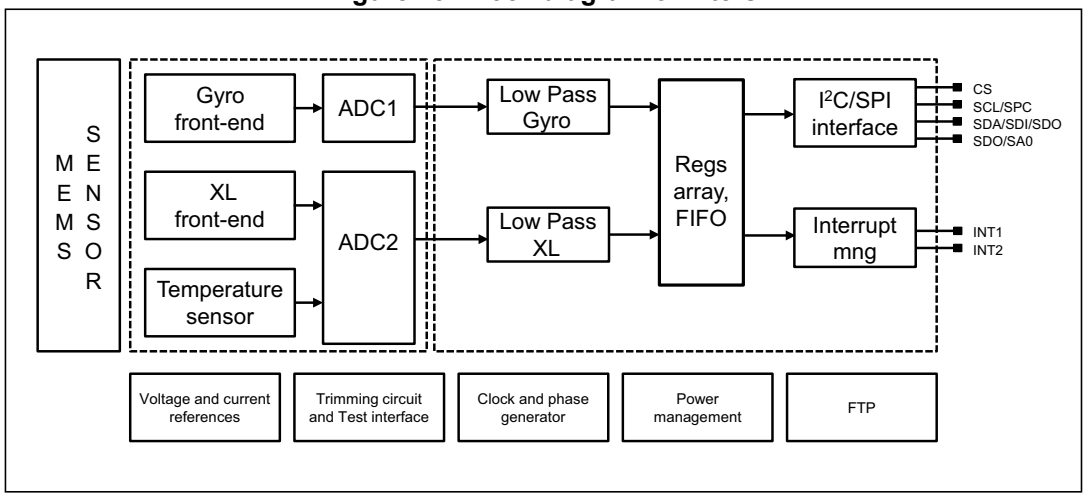
6.3 Gyroscope power modes

In the LSM6DSOP, the gyroscope can be configured in four different operating modes: power-down, low-power, normal mode and high-performance mode. The operating mode selected depends on the value of the G_HM_MODE bit in *CTRL7_G (16h)*. If G_HM_MODE is set to '0', high-performance mode is valid for all ODRs (from 12.5 Hz up to 6.66 kHz).

To enable the low-power and normal mode, the G_HM_MODE bit has to be set to '1'. Low-power mode is available for lower ODRs (12.5, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

6.4 Block diagram of filters

Figure 13. Block diagram of filters



6.4.1 Block diagrams of the accelerometer filters

In the LSM6DSOP, the filtering chain for the accelerometer part is composed of the following:

- Analog filter (anti-aliasing)
- Digital filter (LPF1)
- Composite filter

Details of the block diagram appear in the following figure.

Figure 14. Accelerometer chain

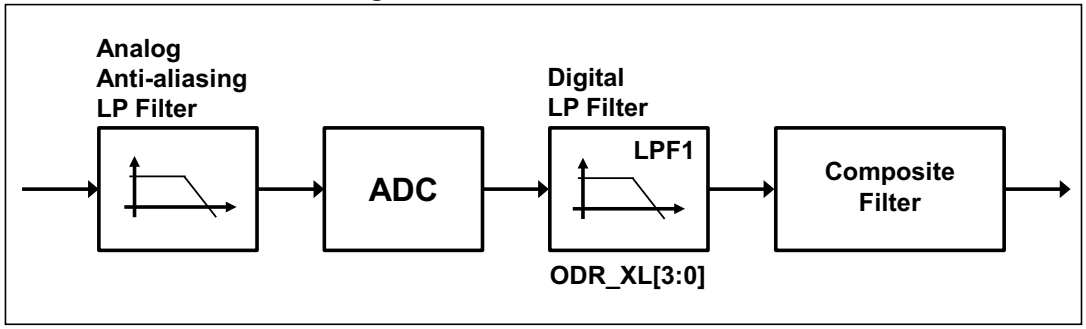
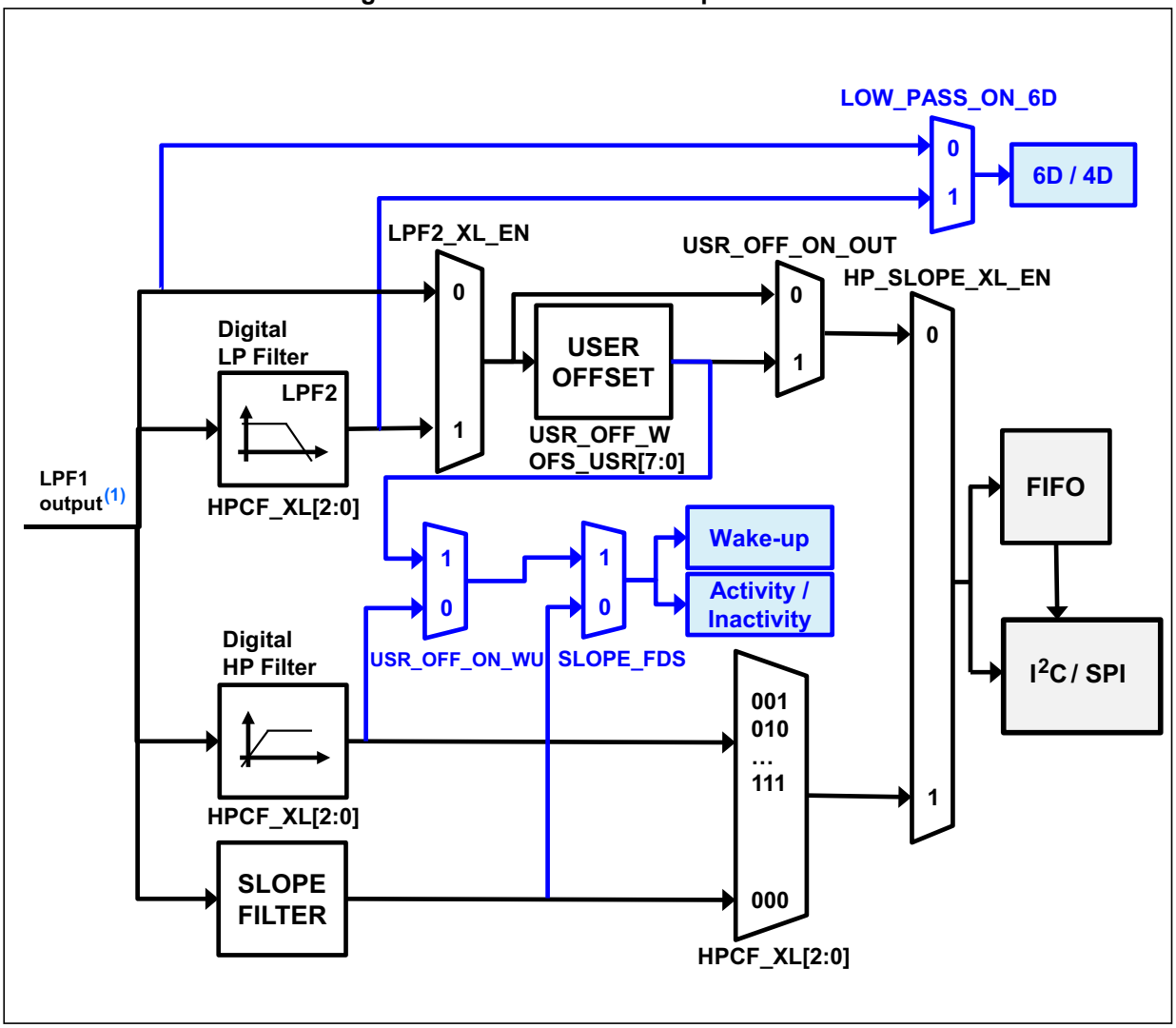


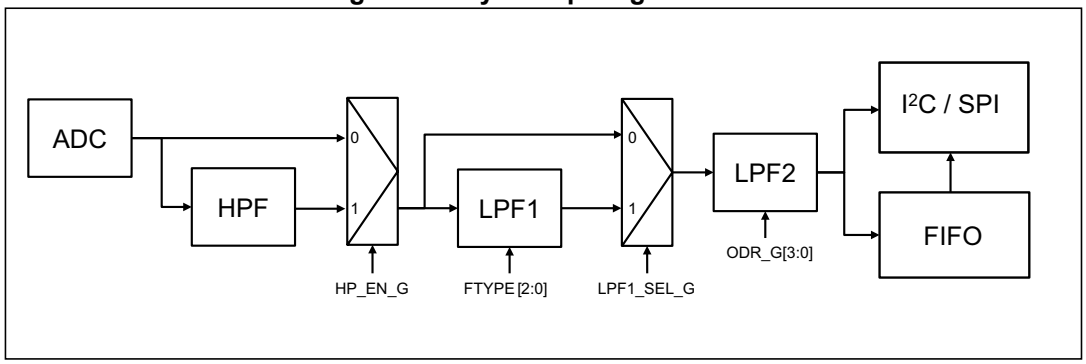
Figure 15. Accelerometer composite filter



1. The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode. This value is equal to 700 Hz when the accelerometer is in low-power or normal mode.

6.4.2 Block diagrams of the gyroscope filters

Figure 16. Gyroscope digital chain



The digital LPF2 filter cannot be configured by the user and its cutoff frequency depends on the selected gyroscope ODR, as indicated in the following table.

Table 16. Gyroscope LPF2 bandwidth selection

Gyroscope ODR [Hz]	LPF2 cutoff [Hz]
12.5	4.2
26	8.3
52	16.6
104	33.0
208	66.8
417	135.9
833	295.5
1667	1108.1
3333	1320.7
6667	1441.8

6.5 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but It can wake up only when needed and burst the significant data out from the FIFO.

The LSM6DSOP embeds 3 kbytes of data in FIFO (up to 9 kbytes with the compression feature enabled) to store the following data:

- Gyroscope
- Accelerometer
- Timestamp
- Temperature

Writing data in the FIFO can be configured to be triggered by the accelerometer / gyroscope data-ready signal

The applications have maximum flexibility in choosing the rate of batching for physical sensors with FIFO-dedicated configurations: accelerometer, gyroscope and temperature sensor batching rates can be selected by the user. It is possible to select decimation for timestamp batching in FIFO with a factor of 1, 8, or 32.

The reconstruction of a FIFO stream is a simple task thanks to the FIFO_DATA_OUT_TAG byte that allows recognizing the meaning of a word in FIFO.

FIFO allows correct reconstruction of the timestamp information for each sensor stored in FIFO. If a change in the ODR or BDR (Batching Data Rate) configuration is performed, the application can correctly reconstruct the timestamp and know exactly when the change was applied without disabling FIFO batching. FIFO stores information of the new configuration and timestamp in which the change was applied in the device.

Finally, FIFO embeds a compression algorithm that the user can enable in order to have up to 9 kbytes data stored in FIFO and take advantage of interface communication length for FIFO flushing and communication power consumption.

The programmable FIFO watermark threshold can be set in *FIFO_CTRL1 (07h)* and *FIFO_CTRL2 (08h)* using the WTM[8:0] bits. To monitor the FIFO status, dedicated registers (*FIFO_STATUS1 (3Ah)*, *FIFO_STATUS2 (3Bh)*) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO watermark status and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT pin of these status events, the configuration can be set in *INT_CTRL (0Dh)* and *INT_CTRL register description*.

The FIFO buffer can be configured according to six different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous mode
- Bypass-to-FIFO mode

Each mode is selected by the FIFO_MODE_[2:0] bits in the *FIFO_CTRL4 (0Ah)* register.

6.5.1 Bypass mode

In Bypass mode (*FIFO_CTRL4 (0Ah)*(FIFO_MODE_[2:0] = 000), the FIFO is not operational and it remains empty. Bypass mode is also used to reset the FIFO when in FIFO mode.

6.5.2 FIFO mode

In FIFO mode (*FIFO_CTRL4 (0Ah)*(FIFO_MODE_[2:0] = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, Bypass mode should be selected by writing *FIFO_CTRL4 (0Ah)*(FIFO_MODE_[2:0]) to '000'. After this reset command, it is possible to restart FIFO mode by writing *FIFO_CTRL4 (0Ah)*(FIFO_MODE_[2:0]) to '001'.

The FIFO buffer memorizes up to 9 kbytes of data (with compression enabled) but the depth of the FIFO can be resized by setting the WTM [8:0] bits in *FIFO_CTRL1 (07h)* and *FIFO_CTRL2 (08h)*. If the STOP_ON_WTM bit in *FIFO_CTRL2 (08h)* is set to '1', FIFO depth is limited up to the WTM [8:0] bits in *FIFO_CTRL1 (07h)* and *FIFO_CTRL2 (08h)*.

6.5.3 Continuous mode

Continuous mode (*FIFO_CTRL4 (0Ah)*(FIFO_MODE_[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag *FIFO_STATUS2 (3Bh)*(FIFO_WTM_IA) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO_CTRL1 (07h)* and *FIFO_CTRL2 (08h)*(WTM [8:0]).

It is possible to route the FIFO_WTM_IA flag to *FIFO_CTRL2 (08h)* to the INT pin by writing in register *INT_CTRL (0Dh)*(INT_FIFO_TH) = '1'.

A full-flag interrupt can be enabled, *INT_CTRL (0Dh)*(INT_FIFO_FULL) = '1', in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the FIFO_OVR_IA flag in *FIFO_STATUS2 (3Bh)* is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in*FIFO_STATUS1 (3Ah)* and *FIFO_STATUS2 (3Bh)*(DIFF_FIFO_[9:0]).

6.5.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (*FIFO_CTRL4 (0Ah)*(FIFO_MODE_[2:0] = 011), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- D6D

When the selected trigger bit is equal to '1', FIFO operates in FIFO mode.

When the selected trigger bit is equal to '0', FIFO operates in Continuous mode.

6.5.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO_CTRL4 (0Ah)*(FIFO_MODE_[2:0] = '100'), data measurement storage inside FIFO operates in Continuous mode when selected triggers are equal to '1', otherwise FIFO content is reset (Bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- D6D

6.5.6 Bypass-to-FIFO mode

In Bypass-to-FIFO mode (*FIFO_CTRL4 (0Ah)*(FIFO_MODE_[2:0] = '111'), data measurement storage inside FIFO operates in FIFO mode when selected triggers are equal to '1', otherwise FIFO content is reset (Bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- D6D

6.5.7 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers and each FIFO word is composed of 7 bytes: one tag byte (*FIFO_DATA_OUT_TAG (78h)*, in order to identify the sensor, and 6 bytes of fixed data (FIFO_DATA_OUT registers from (79h) to (7Eh)).

The DIFF_FIFO_[9:0] field in the *FIFO_STATUS1 (3Ah)* and *FIFO_STATUS2 (3Bh)* registers contains the number of words (1 byte TAG + 6 bytes DATA) collected in FIFO.

In addition, it is possible to configure a counter of the batch events of accelerometer or gyroscope sensors. The flag COUNTER_BDR_IA in *FIFO_STATUS2 (3Bh)* alerts that the counter reaches a selectable threshold (CNT_BDR_TH_[10:0] field in *COUNTER_BDR_REG1 (0Bh)* and *COUNTER_BDR_REG2 (0Ch)*). This allows triggering the reading of FIFO with the desired latency of one single sensor. The sensor is selectable using the TRIG_COUNTER_BDR bit in *COUNTER_BDR_REG1 (0Bh)*. As for the other FIFO status events, the flag COUNTER_BDR_IA can be routed on the INT pin by asserting the corresponding bit (INT_CNT_BDR of *INT_CTRL (0Dh)*.

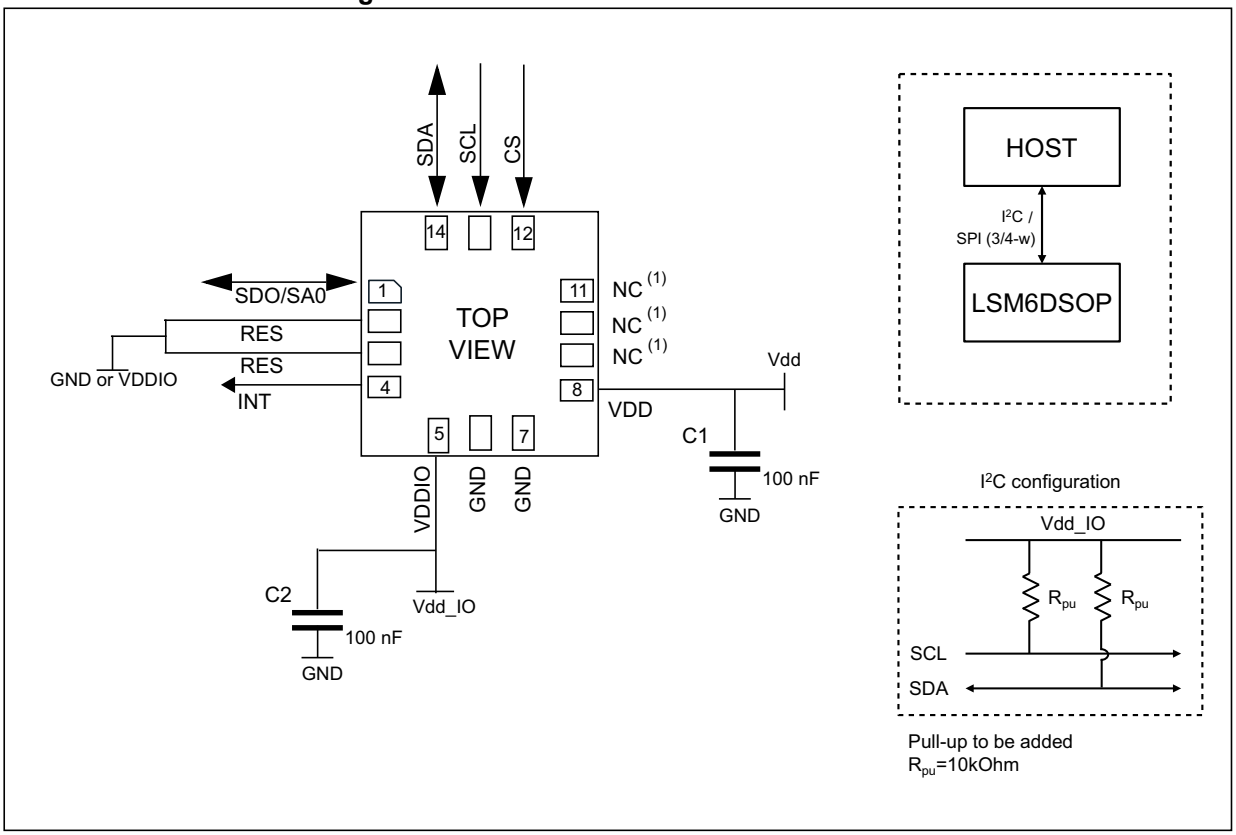
In order to maximize the amount of accelerometer and gyroscope data in FIFO, the user can enable the compression algorithm by setting to 1 both the FIFO_COMPR_EN bit in *EMB_FUNC_EN_B (05h)* (embedded functions registers bank) and the FIFO_COMPR_RT_EN bit in *FIFO_CTRL2 (08h)*. When compression is enabled, it is also possible to force writing non-compressed data at a selectable rate using the UNCOPTR_RATE_[1:0] field in *FIFO_CTRL2 (08h)*.

Meta information about accelerometer and gyroscope sensor configuration changes can be managed by enabling the ODR_CHG_EN bit in *FIFO_CTRL2 (08h)*.

7 Application hints

7.1 LSM6DSOP electrical connections

Figure 17. LSM6DSOP electrical connections



1. Leave pin electrically unconnected and soldered to PCB.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 *nF* ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the I²C/SPI interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the I²C/SPI interface.

The procedure to correctly initialize the device is as follows:

1. INT: Leave unconnected or connect with external pull-down during power-on. Pull-up must be avoided on this pin.
2. Properly configure the device:
   a) SPI case: I2C_disable = 1 in *CTRL4_C (13h)* and DEVICE_CONF = 1 in *CTRL9_XL (18h)*.
   b) I²C case: I2C_disable = 0 (default) in *CTRL4_C (13h)* and DEVICE_CONF = 1 in *CTRL9_XL (18h)*.

Table 17. Internal pin status

pin#	Name	Pin function	Pin status
1	SDO	SPI 4-wire interface serial data output (SDO)	Default: input without pull-up. Pull-up is enabled if bit SDO_PU_EN = 1 in reg 02h.
	SA0	I²C least significant bit of the device address (SA0)	
2	RES	Connect to VDDIO or GND	Default: input without pull-up. Pull-up is enabled if bit PU_EN = 1 in reg 14h in pull-up configuration registers (see Note to enable pull-up).
3	RES	Connect to VDDIO or GND	Default: input without pull-up. Pull-up is enabled if bit PU_EN = 1 in reg 14h in pull-up configuration registers (see Note to enable pull-up).
4	INT	Programmable interrupt	Default: input with pull-down(1)
5	VDDIO	Power supply for I/O pins	
6	GND	0 V supply	
7	GND	0 V supply	
8	VDD	Power supply	
9	NC	Leave unconnected	Default: output forced to ground
10	NC	Leave unconnected	Default: input with pull-up
11	NC	Leave unconnected	Default: input with pull-up
12	CS	I²C/SPI mode selection (1:SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)	Default: input with pull-up. Pull-up is disabled if bit I2C_disable = 1 in reg 13h and DEVICE_CONF = 1 in reg 18h.
13	SCL	I²C / SPI serial port clock (SPC)	Default: input without pull-up
14	SDA	I²C (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	Default: input without pull-up

1. INT must be set to '0' or left unconnected during power-on.

Internal pull-up value is from 30 kΩ to 50 kΩ, depending on VDDIO.

Note: The procedure to enable the pull-up on pins 2 and 3 is as follows:

1. *Write 40h in register at address 01h (enable access to PU_CONFIG (14h))*
2. *Write 08h in register at address 14h (enable the pull-up on pins 2 and 3)*
3. *Write 00h in register at address 01h (disable access to PU_CONFIG (14h))*

8 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

Table 18. Registers address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
FUNC_CFG_ACCESS	RW	01	00000001	00000000	
PIN_CTRL	RW	02	00000010	00111111	
RESERVED	-	03-06			
FIFO_CTRL1	RW	07	00000111	00000000	
FIFO_CTRL2	RW	08	00001000	00000000	
FIFO_CTRL3	RW	09	00001001	00000000	
FIFO_CTRL4	RW	0A	00001010	00000000	
COUNTER_BDR_REG1	RW	0B	00001011	00000000	
COUNTER_BDR_REG2	RW	0C	00001100	00000000	
INT_CTRL	RW	0D	00001101	00000000	
RESERVED	-	0E	00001110		
WHO_AM_I	R	0F	00001111	01101100	
CTRL1_XL	RW	10	00010000	00000000	
CTRL2_G	RW	11	00010001	00000000	
CTRL3_C	RW	12	00010010	00000100	
CTRL4_C	RW	13	00010011	00000000	
CTRL5_C	RW	14	00010100	00000000	
CTRL6_C	RW	15	00010101	00000000	
CTRL7_G	RW	16	00010110	00000000	
CTRL8_XL	RW	17	0001 0111	00000000	
CTRL9_XL	RW	18	00011000	11100000	
CTRL10_C	RW	19	00011001	00000000	
ALL_INT_SRC	R	1A	00011010	output	
WAKE_UP_SRC	R	1B	00011011	output	
RESERVED	-	1C	00011100		
D6D_SRC	R	1D	00011101	output	
STATUS_REG	R	1E	00011110	output	
RESERVED	-	1F	00011111		
OUT_TEMP_L	R	20	00100000	output	

Table 18. Registers address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
OUT_TEMP_H	R	21	00100001	output	
OUTX_L_G	R	22	00100010	output	
OUTX_H_G	R	23	00100011	output	
OUTY_L_G	R	24	00100100	output	
OUTY_H_G	R	25	00100101	output	
OUTZ_L_G	R	26	00100110	output	
OUTZ_H_G	R	27	00100111	output	
OUTX_L_A	R	28	00101000	output	
OUTX_H_A	R	29	00101001	output	
OUTY_L_A	R	2A	00101010	output	
OUTY_H_A	R	2B	00101011	output	
OUTZ_L_A	R	2C	00101100	output	
OUTZ_H_A	R	2D	00101101	output	
RESERVED	-	2E-34			
EMB_FUNC_STATUS_ MAINPAGE	R	35	00110101	output	
FSM_STATUS_A_ MAINPAGE	R	36	00110110	output	
FSM_STATUS_B_ MAINPAGE	R	37	00110111	output	
RESERVED	-	38-39			
FIFO_STATUS1	R	3A	00111010	output	
FIFO_STATUS2	R	3B	00111011	output	
RESERVED	-	3C-3F			
TIMESTAMP0	R	40	01000000	output	
TIMESTAMP1	R	41	01000001	output	
TIMESTAMP2	R	42	01000010	output	
TIMESTAMP3	R	43	01000011	output	
RESERVED	-	44-55			
LIR_CONFIG	RW	56	01010110	00000000	
RESERVED	-	57	01010111		
INT_CFG	RW	58	01011000	00000000	
THS_6D	RW	59	01011001	00000000	
RESERVED	-	5A	01011010		
WAKE_UP_THS	RW	5B	01011011	00000000	

Table 18. Registers address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
WAKE_UP_DUR	RW	5C	01011100	00000000	
RESERVED	-	5D	01011101		
MD1_CFG	RW	5E	01011110	00000000	
RESERVED	-	5F-61		00000000	
INT_PD_CFG	RW	62	01100010	00000000	
INTERNAL_FREQ_FINE	R	63	01100011	output	
RESERVED	-	64-72			
X_OFS_USR	RW	73	01110011	00000000	
Y_OFS_USR	RW	74	01110100	00000000	
Z_OFS_USR	RW	75	01110101	00000000	
RESERVED	-	76-77			
FIFO_DATA_OUT_TAG	R	78	01111000	output	
FIFO_DATA_OUT_X_L	R	79	01111001	output	
FIFO_DATA_OUT_X_H	R	7A	01111010	output	
FIFO_DATA_OUT_Y_L	R	7B	01111011	output	
FIFO_DATA_OUT_Y_H	R	7C	01111100	output	
FIFO_DATA_OUT_Z_L	R	7D	01111101	output	
FIFO_DATA_OUT_Z_H	R	7E	01111110	output	

9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

9.1 FUNC_CFG_ACCESS (01h)

Enable embedded functions register (r/w)

Table 19. FUNC_CFG_ACCESS register

FUNC_CFG_ACCESS	PU_REG_ACCESS	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 20. FUNC_CFG_ACCESS register description

FUNC_CFG_ACCESS	Enable access to the embedded functions configuration registers(1). Default value: 0
PU_REG_ACCESS	Enable access to *PU_CONFIG (14h)*. Default value: 0

1. Details concerning the embedded functions configuration registers are available in *Section 10: Embedded functions register mapping* and *Section 11: Embedded functions register description*.

9.2 PIN_CTRL (02h)

SDO pin pull-up enable/disable register (r/w)

Table 21. PIN_CTRL register

0(1)	SDO_PU_EN	1(2)	1(2)	1(2)	1(2)	1(2)	1(2)

1. This bit must be set to '0' for the correct operation of the device.
2. This bit must be set to '1' for the correct operation of the device.

Table 22. PIN_CTRL register description

SDO_PU_EN	Enable pull-up on SDO pin (0: SDO pin pull-up disconnected (default); 1: SDO pin with pull-up)

9.3 FIFO_CTRL1 (07h)

FIFO control register 1 (r/w)

Table 23. FIFO_CTRL1 register

WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

Table 24. FIFO_CTRL1 register description

WTM[7:0]	FIFO watermark threshold, in conjunction with WTM8 in *FIFO_CTRL2 (08h)* 1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level.

9.4 FIFO_CTRL2 (08h)

FIFO control register 2 (r/w)

Table 25. FIFO_CTRL2 register

STOP_ON_WTM	FIFO_COMPR_RT_EN	0(1)	ODRCHG_EN	0(1)	UNCOPTR_RATE_1	UNCOPTR_RATE_0	WTM8

1. This bit must be set to '0' for the correct operation of the device.

Table 26. FIFO_CTRL2 register description

STOP_ON_WTM	Sensing chain FIFO stop values memorization at threshold level (0: FIFO depth is not limited (default); 1: FIFO depth is limited to threshold level, defined in *FIFO_CTRL1 (07h)* and *FIFO_CTRL2 (08h)*)
FIFO_COMPR_RT_EN(1)	Enables/Disables compression algorithm runtime
ODRCHG_EN	Enables ODR CHANGE virtual sensor to be batched in FIFO
UNCOPTR_RATE_[1:0]	This field configures the compression algorithm to write non-compressed data at each rate. (0: Non-compressed data writing is not forced; 1: Non-compressed data every 8 batch data rate; 2: Non-compressed data every 16 batch data rate; 3: Non-compressed data every 32 batch data rate)
WTM8	FIFO watermark threshold, in conjunction with WTM_FIFO[7:0] in *FIFO_CTRL1 (07h)* 1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level.

1. This bit is effective if the FIFO_COMPR_EN bit of *EMB_FUNC_EN_B (05h)* is set to 1.

9.5 FIFO_CTRL3 (09h)

FIFO control register 3 (r/w)

Table 27. FIFO_CTRL3 register

BDR_ GY_3	BDR_ GY_2	BDR_ GY_1	BDR_ GY_0	BDR_ XL_3	BDR_ XL_2	BDR_ XL_1	BDR_ XL_0

Table 28. FIFO_CTRL3 register description

BDR_GY_[3:0]	Selects Batching Data Rate (writing frequency in FIFO) for gyroscope data. (0000: Gyro not batched in FIFO (default); 0001: 12.5 Hz; 0010: 26 Hz; 0011: 52 Hz; 0100: 104 Hz; 0101: 208 Hz; 0110: 417 Hz; 0111: 833 Hz; 1000: 1667 Hz; 1001: 3333 Hz; 1010: 6667 Hz; 1011: 6.5 Hz; 1100-1111: not allowed)
BDR_XL_[3:0]	Selects Batching Data Rate (writing frequency in FIFO) for accelerometer data. (0000: Accelerometer not batched in FIFO (default); 0001: 12.5 Hz; 0010: 26 Hz; 0011: 52 Hz; 0100: 104 Hz; 0101: 208 Hz; 0110: 417 Hz; 0111: 833 Hz; 1000: 1667 Hz; 1001: 3333 Hz; 1010: 6667 Hz; 1011: 1.6 Hz; 1100-1111: not allowed)

9.6 FIFO_CTRL4 (0Ah)

FIFO control register 4 (r/w)

Table 29. FIFO_CTRL4 register

DEC_TS_ BATCH_1	DEC_TS_ BATCH_0	ODR_T_ BATCH_1	ODR_T_ BATCH_0	0(1)	FIFO_ MODE2	FIFO_ MODE1	FIFO_ MODE0

1. This bit must be set to '0' for the correct operation of the device.

Table 30. FIFO_CTRL4 register description

DEC_TS_ BATCH_[1:0]	Selects decimation for timestamp batching in FIFO. Writing rate will be the maximum rate between XL and GYRO BDR divided by decimation decoder. (00: Timestamp not batched in FIFO (default); 01: Decimation 1: max(BDR_XL[Hz],BDR_GY[Hz]) [Hz]; 10: Decimation 8: max(BDR_XL[Hz],BDR_GY[Hz])/8 [Hz]; 11: Decimation 32: max(BDR_XL[Hz],BDR_GY[Hz])/32 [Hz])
ODR_T_ BATCH_[1:0]	Selects batching data rate (writing frequency in FIFO) for temperature data (00: Temperature not batched in FIFO (default); 01: 1.6 Hz; 10: 12.5 Hz; 11: 52 Hz)
FIFO_ MODE[2:0]	FIFO mode selection (000: Bypass mode: FIFO disabled; 001: FIFO mode: stops collecting data when FIFO is full; 010: Reserved; 011: Continuous-to-FIFO mode: Continuous mode until trigger is deasserted, then FIFO mode; 100: Bypass-to-Continuous mode: Bypass mode until trigger is deasserted, then Continuous mode; 101: Reserved; 110: Continuous mode: if the FIFO is full, the new sample overwrites the older one; 111: Bypass-to-FIFO mode: Bypass mode until trigger is deasserted, then FIFO mode.)

9.7 COUNTER_BDR_REG1 (0Bh)

Counter batch data rate register 1 (r/w)

Table 31. COUNTER_BDR_REG1 register

dataready_pulsed	RST_COUNTER_BDR	TRIG_COUNTER_BDR	0(1)	0(1)	CNT_BDR_TH_10	CNT_BDR_TH_9	CNT_BDR_TH_8

1. This bit must be set to '0' for the correct operation of the device.

Table 32. COUNTER_BDR_REG1 register description

dataready_pulsed	Enables pulsed data-ready mode (0: Data-ready latched mode (returns to 0 only after an interface reading) (default); 1: Data-ready pulsed mode (the data ready pulses are 75 µs long)
RST_COUNTER_BDR	Resets the internal counter of batching events for a single sensor. This bit is automatically reset to zero if it was set to '1'.
TRIG_COUNTER_BDR	Selects the trigger for the internal counter of batching events between XL and gyro. (0: XL batching event; 1: GYRO batching event)
CNT_BDR_TH_[10:8]	In conjunction with CNT_BDR_TH_[7:0] in *COUNTER_BDR_REG2 (0Ch)*, sets the threshold for the internal counter of batching events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in *FIFO_STATUS2 (3Bh)* is set to '1'.

9.8 COUNTER_BDR_REG2 (0Ch)

Counter batch data rate register 2 (r/w)

Table 33. COUNTER_BDR_REG2 register

CNT_BDR_TH_7	CNT_BDR_TH_6	CNT_BDR_TH_5	CNT_BDR_TH_4	CNT_BDR_TH_3	CNT_BDR_TH_2	CNT_BDR_TH_1	CNT_BDR_TH_0

Table 34. COUNTER_BDR_REG2 register description

CNT_BDR_TH_[7:0]	In conjunction with CNT_BDR_TH_[10:8] in *COUNTER_BDR_REG1 (0Bh)*, sets the threshold for the internal counter of batching events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in *FIFO_STATUS2 (3Bh)* is set to '1'.

9.9 INT_CTRL (0Dh)

INT pin control register (r/w)

Table 35. INT_CTRL register

DEN_ DRDY_ flag	INT_CNT_ BDR	INT_ FIFO _FULL	INT_ FIFO_ OVR	INT_ FIFO_TH	INT_ BOOT	INT_ DRDY_G	INT_ DRDY_XL

Table 36. INT_CTRL register description

DEN_DRDY_flag	Sends DEN_DRDY (DEN stamped on Sensor Data flag) to INT pin
INT_CNT_BDR	Enables COUNTER_BDR_IA interrupt on INT
INT_FIFO_FULL	Enables FIFO full flag interrupt on INT pin.
INT_FIFO_OVR	Enables FIFO overrun interrupt on INT pin.
INT_FIFO_TH	Enables FIFO threshold interrupt on INT pin.
INT_BOOT	Enables boot status on INT pin
INT_DRDY_G	Enables gyroscope data-ready interrupt on INT pin.
INT_DRDY_XL	Enables accelerometer data-ready interrupt on INT pin.

9.10 WHO_AM_I (0Fh)

WHO_AM_I register (r). This is a read-only register. Its value is fixed at 6Ch.

Table 37. WhoAmI register

0	1	1	0	1	1	0	0

9.11 CTRL1_XL (10h)

Accelerometer control register 1 (r/w)

Table 38. CTRL1_XL register

ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	FS1_XL	FS0_XL	LPF2_XL_EN	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 39. CTRL1_XL register description

ODR_XL[3:0]	Accelerometer ODR selection (see *Table 40*)
FS[1:0]_XL	Accelerometer full-scale selection (see *Table 41*)
LPF2_XL_EN	Accelerometer high-resolution selection (0: output from first stage digital filtering selected (default); 1: output from LPF2 second filtering stage selected)

Table 40. Accelerometer ODR register setting

ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	ODR selection [Hz] when XL_HM_MODE = 1 in *CTRL6_C (15h)*	ODR selection [Hz] when XL_HM_MODE = 0 in *CTRL6_C (15h)*
0	0	0	0	Power-down	Power-down
1	0	1	1	1.6 Hz (low power only)	12.5 Hz (high performance)
0	0	0	1	12.5 Hz (low power)	12.5 Hz (high performance)
0	0	1	0	26 Hz (low power)	26 Hz (high performance)
0	0	1	1	52 Hz (low power)	52 Hz (high performance)
0	1	0	0	104 Hz (normal mode)	104 Hz (high performance)
0	1	0	1	208 Hz (normal mode)	208 Hz (high performance)
0	1	1	0	416 Hz (high performance)	416 Hz (high performance)
0	1	1	1	833 Hz (high performance)	833 Hz (high performance)
1	0	0	0	1.66 kHz (high performance)	1.66 kHz (high performance)
1	0	0	1	3.33 kHz (high performance)	3.33 kHz (high performance)
1	0	1	0	6.66 kHz (high performance)	6.66 kHz (high performance)
1	1	x	x	Not allowed	Not allowed

Table 41. Accelerometer full-scale selection

FS[1:0]_XL	XL_FS_MODE = '0' in *CTRL8_XL (17h)*	XL_FS_MODE = '1' in *CTRL8_XL (17h)*
00 (default)	±2 *g*	±2 *g*
01	±16 *g*	±2 *g*
10	±4 *g*	±4 *g*
11	±8 *g*	±8 *g*

9.12 CTRL2_G (11h)

Gyroscope control register 2 (r/w)

Table 42. CTRL2_G register

ODR_G3	ODR_G2	ODR_G1	ODR_G0	FS1_G	FS0_G	FS_125	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 43. CTRL2_G register description

ODR_G[3:0]	Gyroscope output data rate selection. Default value: 0000 (Refer to *Table 44*)
FS[1:0]_G	Gyroscope chain full-scale selection (00: ±250 dps; 01: ±500 dps; 10: ±1000 dps; 11: ±2000 dps)
FS_125	Selects gyro chain full-scale ±125 dps (0: FS selected through bits FS[1:0]_G; 1: FS set to ±125 dps)

Table 44. Gyroscope ODR configuration setting

ODR_G3	ODR_G2	ODR_G1	ODR_G0	ODR [Hz] when G_HM_MODE = 1 in *CTRL7_G (16h)*	ODR [Hz] when G_HM_MODE = 0 in *CTRL7_G (16h)*
0	0	0	0	Power down	Power down
0	0	0	1	12.5 Hz (low power)	12.5 Hz (high performance)
0	0	1	0	26 Hz (low power)	26 Hz (high performance)
0	0	1	1	52 Hz (low power)	52 Hz (high performance)
0	1	0	0	104 Hz (normal mode)	104 Hz (high performance)
0	1	0	1	208 Hz (normal mode)	208 Hz (high performance)
0	1	1	0	416 Hz (high performance)	416 Hz (high performance)
0	1	1	1	833 Hz (high performance)	833 Hz (high performance)
1	0	0	0	1.66 kHz (high performance)	1.66 kHz (high performance)
1	0	0	1	3.33 kHz (high performance	3.33 kHz (high performance)
1	0	1	0	6.66 kHz (high performance	6.66 kHz (high performance)
1	0	1	1	Not available	Not available

9.13 CTRL3_C (12h)

Control register 3 (r/w)

Table 45. CTRL3_C register

BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_INC	0(1)	SW_RESET

1. This bit must be set to '0' for the correct operation of the device.

Table 46. CTRL3_C register description

BOOT	Reboots memory content. Default value: 0 (0: normal mode; 1: reboot memory content) This bit is automatically cleared.
BDU	Block Data Update. Default value: 0 (0: continuous update; 1: output registers are not updated until MSB and LSB have been read)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active high; 1: interrupt output pins active low)
PP_OD	Push-pull/open-drain selection on INT pin. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
IF_INC	Register address automatically incremented during a multiple byte access with a serial interface (I²C or SPI). Default value: 1 (0: disabled; 1: enabled)
SW_RESET	Software reset. Default value: 0 (0: normal mode; 1: reset device) This bit is automatically cleared.

9.14 CTRL4_C (13h)

Control register 4 (r/w)

Table 47. CTRL4_C register

0(1)	SLEEP_G	0(1)	0(1)	DRDY_ MASK	I2C_disable	LPF1_ SEL_G	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 48. CTRL4_C register description

SLEEP_G	Enables gyroscope Sleep mode. Default value:0 (0: disabled; 1: enabled)
DRDY_MASK	Enables data available (0: disabled; 1: mask DRDY on pin (both XL & Gyro) until filter settling ends (XL and Gyro independently masked).
I2C_disable	Disables I²C interface. Default value: 0 (0: SPI and I²C interfaces enabled (default); 1: I²C interface disabled)
LPF1_SEL_G	Enables gyroscope digital LPF1; the bandwidth can be selected through FTYPE [2:0] in *CTRL6_C (15h)*. (0: disabled; 1: enabled)

9.15 CTRL5_C (14h)

Control register 5 (r/w)

Table 49. CTRL5_C register

XL_ULP_EN	ROUNDING1	ROUNDING0	0(1)	ST1_G	ST0_G	ST1_XL	ST0_XL

1. This bit must be set to '0' for the correct operation of the device.

Table 50. CTRL5_C register description

XL_ULP_EN	Accelerometer ultra-low-power mode enable(1). Default value: 0 (0: Ultra-low-power mode disabled; 1: Ultra-low-power mode enabled)
ROUNDING[1:0]	Circular burst-mode (rounding) read from the output registers. Default value: 00 (00: no rounding; 01: accelerometer only; 10: gyroscope only; 11: gyroscope + accelerometer)
ST[1:0]_G	Angular rate sensor self-test enable. Default value: 00 (00: Self-test disabled; Other: refer to *Table 51*)
ST[1:0]_XL	Linear acceleration sensor self-test enable. Default value: 00 (00: Self-test disabled; Other: refer to *Table 52*)

1. Further details about the accelerometer ultra-low-power mode are provided in *Section 6.2.1: Accelerometer ultra-low-power mode*.

Table 51. Angular rate sensor self-test mode selection

ST1_G	ST0_G	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Not allowed
1	1	Negative sign self-test

Table 52. Linear acceleration sensor self-test mode selection

ST1_XL	ST0_XL	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

9.16 CTRL6_C (15h)

Control register 6 (r/w)

Table 53. CTRL6_C register

0(1)	0(1)	0(1)	XL_HM_MODE	USR_ OFF_W	FTYPE_2	FTYPE_1	FTYPE_0

1. This bit must be set to '0' for the correct operation of the device.

Table 54. CTRL6_C register description

XL_HM_MODE	High-performance operating mode disable for accelerometer. Default value: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled)
USR_OFF_W	Weight of XL user offset bits of registers *X_OFS_USR (73h)*, *Y_OFS_USR (74h)*, *Z_OFS_USR (75h)* (0 = 2^{-10} *g*/LSB; 1 = 2^{-6} *g*/LSB)
FTYPE[2:0]	Gyroscope's low-pass filter (LPF1) bandwidth selection *Table 55* shows the selectable bandwidth values.

Table 55. Gyroscope LPF1 bandwidth selection

FTYPE [2:0]	12.5 Hz	26 Hz	52 Hz	104 Hz	208 Hz	416 Hz	833 Hz	1.67 kHz	3.33 kHz	6.67 kHz
000	4.2	8.3	16.6	33.0	67.0	136.6	239.2	304.2	328.5	335.5
001	4.2	8.3	16.6	33.0	67.0	130.5	192.4	220.7	229.6	232.0
010	4.2	8.3	16.6	33.0	67.0	120.3	154.2	166.6	170.1	171.1
011	4.2	8.3	16.6	33.0	67.0	137.1	281.8	453.2	559.2	609.0
100	4.2	8.3	16.7	33.0	62.4	86.7	96.6	99.6	NA	NA
101	4.2	8.3	16.8	31.0	43.2	48.0	49.4	49.8	NA	NA
110	4.1	7.8	13.4	19.0	23.1	24.6	25.0	25.1	NA	NA
111	3.9	6.7	9.7	11.5	12.2	12.4	12.5	12.5	NA	NA

9.17 CTRL7_G (16h)

Control register 7 (r/w)

Table 56. CTRL7_G register

G_HM_ MODE	HP_EN_G	HPM1_G	HPM0_G	0(1)	0(1)	USR_ OFF_ON _ OUT	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 57. CTRL7_G register description

G_HM_MODE	Disables high-performance operating mode for gyroscope. Default: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled)
HP_EN_G	Enables gyroscope digital high-pass filter. The filter is enabled only if the gyro is in HP mode. Default value: 0 (0: HPF disabled; 1: HPF enabled)
HPM_G[1:0]	Gyroscope digital HP filter cutoff selection. Default: 00 (00: 16 mHz; 01: 65 mHz; 10: 260 mHz; 11: 1.04 Hz)
USR_OFF_ ON_ OUT	Enables accelerometer user offset correction block; it's valid for the low-pass path - see *Figure 15: Accelerometer composite filter*. Default value: 0 (0: accelerometer user offset correction block bypassed; 1: accelerometer user offset correction block enabled)

9.18 CTRL8_XL (17h)

Control register 8 (r/w)

Table 58. CTRL8_XL register

HPCF_XL_2	HPCF_XL_1	HPCF_XL_0	HP_REF_MODE_XL	FASTSETTL_MODE_XL	HP_SLOPE_XL_EN	0(1)	LOW_PASS_ON_6D

1. This bit must be set to '0' for the correct operation of the device.

Table 59. CTRL8_XL register description

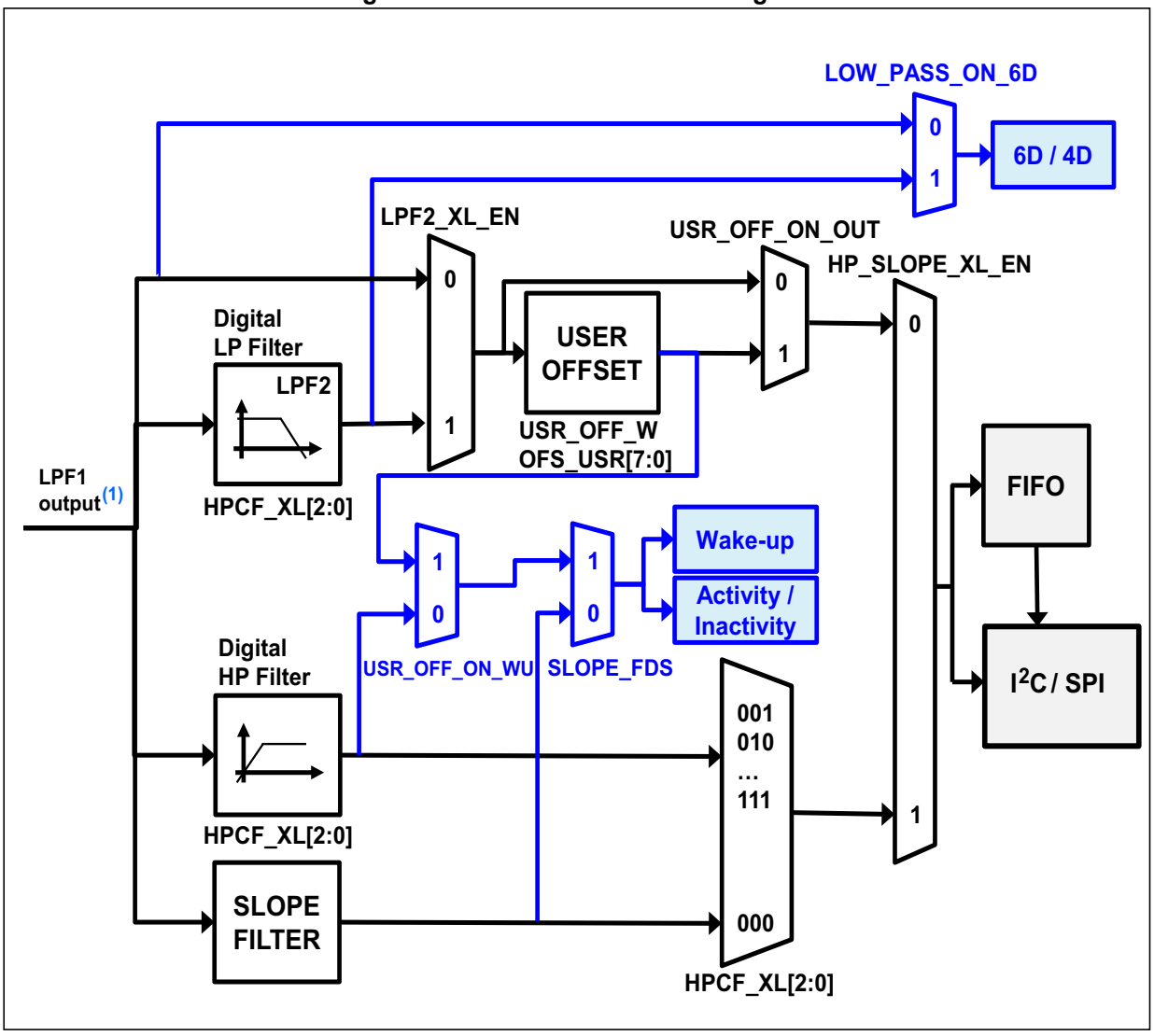
HPCF_XL_[2:0]	Accelerometer LPF2 and HP filter configuration and cutoff setting. Refer to *Table 60*.
HP_REF_MODE_XL	Enables accelerometer high-pass filter reference mode (valid for high-pass path - HP_SLOPE_XL_EN bit must be '1'). Default value: 0 (0: disabled, 1: enabled(1))
FASTSETTL_MODE_XL	Enables accelerometer LPF2 and HPF fast-settling mode. The filter sets the second samples after writing this bit. Active only during device exit from power-down mode. Default value: 0 (0: disabled, 1: enabled)
HP_SLOPE_XL_EN	Accelerometer slope filter / high-pass filter selection. Refer to *Figure 18*.
LOW_PASS_ON_6D	LPF2 on 6D function selection. Refer to *Figure 18*. Default value: 0 (0: ODR/2 low-pass filtered data sent to 6D interrupt function; 1: LPF2 output data sent to 6D interrupt function)

1. When enabled, the first output data have to be discarded.

Table 60. Accelerometer bandwidth configurations

Filter type	HP_SLOPE_XL_EN	LPF2_XL_EN	HPCF_XL_[2:0]	Bandwidth
Low pass	0	0	-	ODR/2
		1	000	ODR/4
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800
High pass	1	-	000	SLOPE (ODR/4)
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800

Figure 18. Accelerometer block diagram



9.19 CTRL9_XL (18h)

Control register 9 (r/w)

Table 61. CTRL9_XL register

1(1)	1(1)	1(1)	0(2)	0(2)	0(2)	DEVICE_CONF	0(2)

1. This bit must be set to '1' for the correct operation of the device.
2. This bit must be set to '0' for the correct operation of the device.

Table 62. CTRL9_XL register description

DEVICE_CONF	Enables the proper device configuration. Default value: 0 It is recommended to always set this bit to 1 during device configuration. (0: default; 1: enabled)

9.20 CTRL10_C (19h)

Control register 10 (r/w)

Table 63. CTRL10_C register

0(1)	0(1)	TIMESTAMP_EN	0(1)	0(1)	0(1)	0(1)	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 64. CTRL10_C register description

TIMESTAMP_EN	Enables timestamp counter. default value: 0 (0: disabled; 1: enabled) The counter is readable in *TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)*.

9.21 ALL_INT_SRC (1Ah)

Source register for all interrupts (r)

Table 65. ALL_INT_SRC register

TIMESTAMP_ ENDCOUNT	0	SLEEP_ CHANGE_IA	D6D_IA	0	0	WU_IA	0

Table 66. ALL_INT_SRC register description

TIMESTAMP_ENDCOUNT	Alerts timestamp overflow within 6.4 ms
SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
D6D_IA	Interrupt active for change in position of portrait, landscape, face-up, face-down. Default value: 0 (0: change in position not detected; 1: change in position detected)
WU_IA	Wake-up event status. Default value: 0 (0: event not detected, 1: event detected)

9.22 WAKE_UP_SRC (1Bh)

Wake-up interrupt source register (r)

Table 67. WAKE_UP_SRC register

0	SLEEP_ CHANGE_IA	0	SLEEP_ STATE	WU_IA	X_WU	Y_WU	Z_WU

Table 68. WAKE_UP_SRC register description

SLEEP_ CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
SLEEP_ STATE	Sleep status bit. Default value: 0 (0: Activity status; 1: Inactivity status)
WU_IA	Wakeup event detection status. Default value: 0 (0: wakeup event not detected; 1: wakeup event detected.)
X_WU	Wakeup event detection status on X-axis. Default value: 0 (0: wakeup event on X-axis not detected; 1: wakeup event on X-axis detected)
Y_WU	Wakeup event detection status on Y-axis. Default value: 0 (0: wakeup event on Y-axis not detected; 1: wakeup event on Y-axis detected)
Z_WU	Wakeup event detection status on Z-axis. Default value: 0 (0: wakeup event on Z-axis not detected; 1: wakeup event on Z-axis detected)

9.23 D6D_SRC (1Dh)

Portrait, landscape, face-up and face-down source register (r)

Table 69. D6D_SRC register

0	D6D_IA	ZH	ZL	YH	YL	XH	XL

Table 70. D6D_SRC register description

D6D_IA	Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0 (0: change position not detected; 1: change position detected)
ZH	Z-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
ZL	Z-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
YH	Y-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over-threshold) detected)
YL	Y-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
XH	X-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
XL	X-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)

9.24 STATUS_REG (1Eh)

Status register (r).

Table 71. STATUS_REG register

0	0	0	0	0	TDA	GDA	XLDA

Table 72. STATUS_REG register description

TDA	Temperature new data available. Default: 0 (0: no set of data is available at temperature sensor output; 1: a new set of data is available at temperature sensor output)
GDA	Gyroscope new data available. Default value: 0 (0: no set of data available at gyroscope output; 1: a new set of data is available at gyroscope output)
XLDA	Accelerometer new data available. Default value: 0 (0: no set of data available at accelerometer output; 1: a new set of data is available at accelerometer output)

9.25 OUT_TEMP_L (20h), OUT_TEMP_H (21h)

Temperature data output register (r). L and H registers together express a 16-bit word in two's complement.

Table 73. OUT_TEMP_L register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 74. OUT_TEMP_H register

Temp15	Temp14	Temp13	Temp12	Temp11	Temp10	Temp9	Temp8

Table 75. OUT_TEMP register description

Temp[15:0]	Temperature sensor output data The value is expressed as two's complement sign extended on the MSB.

9.26 OUTX_L_G (22h) and OUTX_H_G (23h)

Angular rate sensor pitch axis (X) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

Table 76. OUTX_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 77. OUTX_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 78. OUTX_H_G register description

D[15:0]	Pitch axis (X) angular rate value

9.27 OUTY_L_G (24h) and OUTY_H_G (25h)

Angular rate sensor roll axis (Y) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

Table 79. OUTY_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 80. OUTY_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 81. OUTY_H_G register description

D[15:0]	Roll axis (Y) angular rate value

9.28 OUTZ_L_G (26h) and OUTZ_H_G (27h)

Angular rate sensor yaw axis (Z) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

Table 82. OUTZ_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 83. OUTZ_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 84. OUTZ_H_G register description

D[15:0]	Yaw axis (Z) angular rate value

9.29 OUTX_L_A (28h) and OUTX_H_A (29h)

Linear acceleration sensor X-axis output register (r). The value is expressed as a 16-bit word in two's complement.

Table 85. OUTX_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 86. OUTX_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 87. OUTX_H_A register description

D[15:0]	X-axis linear acceleration value.

9.30 OUTY_L_A (2Ah) and OUTY_H_A (2Bh)

Linear acceleration sensor Y-axis output register (r). The value is expressed as a 16-bit word in two's complement.

Table 88. OUTY_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 89. OUTY_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 90. OUTY_H_A register description

D[15:0]	Y-axis linear acceleration value

9.31 OUTZ_L_A (2Ch) and OUTZ_H_A (2Dh)

Linear acceleration sensor Z-axis output register (r). The value is expressed as a 16-bit word in two's complement.

Table 91. OUTZ_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 92. OUTZ_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 93. OUTZ_H_A register description

D[15:0]	Z-axis linear acceleration value

9.32 EMB_FUNC_STATUS_MAINPAGE (35h)

Embedded function status register (r).

Table 94. EMB_FUNC_STATUS_MAINPAGE register

IS_FSM_LC	0	0	0	0	0	0	0

Table 95. EMB_FUNC_STATUS_MAINPAGE register description

IS_FSM_LC	Interrupt status bit for FSM long counter timeout interrupt event. (1: interrupt detected; 0: no interrupt)

9.33 FSM_STATUS_A_MAINPAGE (36h)

Finite State Machine status register (r).

Table 96. FSM_STATUS_A_MAINPAGE register

IS_FSM8	IS_FSM7	IS_FSM6	IS_FSM5	IS_FSM4	IS_FSM3	IS_FSM2	IS_FSM1

Table 97. FSM_STATUS_A_MAINPAGE register description

IS_FSM8	Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM7	Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM6	Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM5	Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM4	Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM3	Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM2	Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM1	Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt)

9.34 FSM_STATUS_B_MAINPAGE (37h)

Finite State Machine status register (r).

Table 98. FSM_STATUS_B_MAINPAGE register

IS_FSM16	IS_FSM15	IS_FSM14	IS_FSM13	IS_FSM12	IS_FSM11	IS_FSM10	IS_FSM9

Table 99. FSM_STATUS_B_MAINPAGE register description

IS_FSM16	Interrupt status bit for FSM16 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM15	Interrupt status bit for FSM15 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM14	Interrupt status bit for FSM14 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM13	Interrupt status bit for FSM13 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM12	Interrupt status bit for FSM12 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM11	Interrupt status bit for FSM11 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM10	Interrupt status bit for FSM10 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM9	Interrupt status bit for FSM9 interrupt event. (1: interrupt detected; 0: no interrupt)

9.35 FIFO_STATUS1 (3Ah)

FIFO status register 1 (r)

Table 100. FIFO_STATUS1 register

DIFF_ FIFO_7	DIFF_ FIFO_6	DIFF_ FIFO_5	DIFF_ FIFO_4	DIFF_ FIFO_3	DIFF_ FIFO_2	DIFF_ FIFO_1	DIFF_ FIFO_0

Table 101. FIFO_STATUS1 register description

DIFF_ FIFO_[7:0]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO In conjunction with DIFF_FIFO[9:8] in *FIFO_STATUS2 (3Bh).*

9.36 FIFO_STATUS2 (3Bh)

FIFO status register 2 (r)

Table 102. FIFO_STATUS2 register

FIFO_ WTM_IA	FIFO_ OVR_IA	FIFO_ FULL_IA	COUNTER _BDR_IA	FIFO_OVR_ LATCHED	0	DIFF_ FIFO_9	DIFF_ FIFO_8

Table 103. FIFO_STATUS2 register description

FIFO_ WTM_IA	FIFO watermark status. Default value: 0 (0: FIFO filling is lower than WTM; 1: FIFO filling is equal to or greater than WTM) Watermark is set through bits WTM[8:0] in *FIFO_CTRL2 (08h)* and *FIFO_CTRL1 (07h)*.
FIFO_ OVR_IA	FIFO overrun status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled)
FIFO_ FULL_IA	Smart FIFO full status. Default value: 0 (0: FIFO is not full; 1: FIFO will be full at the next ODR)
COUNTER_ BDR_IA	Counter BDR reaches the CNT_BDR_TH_[10:0] threshold set in *COUNTER_BDR_REG1 (0Bh)* and *COUNTER_BDR_REG2 (0Ch)*. Default value: 0 This bit is reset when these registers are read.
FIFO_OVR_ LATCHED	Latched FIFO overrun status. Default value: 0 This bit is reset when this register is read.
DIFF_ FIFO_[9:8]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO. Default value: 00 In conjunction with DIFF_FIFO[7:0] in *FIFO_STATUS1 (3Ah)*

9.37 TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)

Timestamp first data output register (r). The value is expressed as a 32-bit word and the bit resolution is 25 µs.

Table 104. TIMESTAMP output registers

D31	D30	D29	D28	D27	D26	D25	D24
D23	D22	D21	D20	D19	D18	D17	D16
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 105. TIMESTAMP output register description

D[31:0]	Timestamp output registers: 1LSB = 25 µs

9.38 LIR_CONFIG (56h)

Activity/inactivity functions, configuration of filtering (r/w).

Table 106. LIR_CONFIG register

0(1)	INT_CLR_ON_READ	SLEEP_STATUS_ON_INT	SLOPE_FDS	0(1)	0(1)	0(1)	LIR

1. This bit must be set to '0' for the correct operation of the device.

Table 107. LIR_CONFIG register description

INT_CLR_ON_READ	This bit allows immediately clearing the latched interrupts of an event detection upon the read of the corresponding status register. It must be set to 1 together with LIR. Default value: 0 (0: latched interrupt signal cleared at the end of the ODR period; 1: latched interrupt signal immediately cleared)
SLEEP_STATUS_ON_INT	Activity/inactivity interrupt mode configuration. If the INT_SLEEP_CHANGE bit is enabled, drives the sleep status or sleep change on the INT pin. Default value: 0 (0: sleep change notification on INT pin; 1: sleep status reported on INT pin)
SLOPE_FDS	HPF or SLOPE filter selection on wake-up and Activity/Inactivity functions. Default value: 0 (0: SLOPE filter applied; 1: HPF applied)
LIR	Latched Interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)

9.39 INT_CFG (58h)

Enables interrupt and inactivity functions (r/w).

Table 108. INT_CFG register

INTERRUPTS_ ENABLE	INACT_ EN1	INACT_ EN0	0(1)	0(1)	0(1)	0(1)	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 109. INT_CFG register description

INTERRUPTS_ ENABLE	Enable basic interrupts (6D/4D, wake-up, inactivity). Default value: 0 (0: interrupt disabled; 1: interrupt enabled)
INACT_EN[1:0]	Enable activity/inactivity (sleep) function. Default value: 00 (00: stationary/motion-only interrupts generated, XL and gyro do not change; 01: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro does not change; 10: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro to sleep mode; 11: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro to power-down mode)

9.40 THS_6D (59h)

Portrait/landscape position and 4D/6D function threshold register (r/w).

Table 110. THS_6D register

D4D_ EN	SIXD_ THS1	SIXD_ THS0	0(1)	0(1)	0(1)	0(1)	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 111. THS_6D register description

D4D_EN	4D orientation detection enable. Z-axis position detection is disabled. Default value: 0 (0: disabled; 1: enabled)
SIXD_THS[1:0]	Threshold for 4D/6D function. Default value: 00 For details, refer to *Table 112*.

Table 112. Threshold for D4D/D6D function

SIXD_THS[1:0]	Threshold value
00	80 degrees
01	70 degrees
10	60 degrees
11	50 degrees

9.41 WAKE_UP_THS (5Bh)

Wake-up configuration (r/w)

Table 113. WAKE_UP_THS register

0(1)	USR_OFF_ON_WU	WK_THS5	WK_THS4	WK_THS3	WK_THS2	WK_THS1	WK_THS0

1. This bit must be set to '0' for the correct operation of the device.

Table 114. WAKE_UP_THS register description

USR_OFF_ON_WU	Drives the low-pass filtered data with user offset correction (instead of high-pass filtered data) to the wakeup function.
WK_THS[5:0]	Threshold for wakeup: 1 LSB weight depends on WAKE_THS_W in *WAKE_UP_DUR (5Ch)*. Default value: 000000

9.42 WAKE_UP_DUR (5Ch)

Wakeup and sleep mode functions duration setting register (r/w)

Table 115. WAKE_UP_DUR register

0(1)	WAKE_DUR1	WAKE_DUR0	WAKE_THS_W	SLEEP_DUR3	SLEEP_DUR2	SLEEP_DUR1	SLEEP_DUR0

1. This bit must be set to '0' for the correct operation of the device.

Table 116. WAKE_UP_DUR register description

WAKE_DUR[1:0]	Wake up duration event. Default: 00 1LSB = 1 ODR_time
WAKE_THS_W	Weight of 1 LSB of wakeup threshold. Default: 0 (0: 1 LSB = FS_XL / (2^6); 1: 1 LSB = FS_XL / (2^8))
SLEEP_DUR[3:0]	Duration to go in sleep mode. Default value: 0000 (this corresponds to 16 ODR) 1 LSB = 512 ODR

9.43 MD1_CFG (5Eh)

Functions routing on INT register (r/w)

Table 117. MD1_CFG register

INT_ SLEEP_ CHANGE	0(1)	INT_WU	0(1)	0(1)	INT_6D	INT_EMB_ FUNC	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 118. MD1_CFG register description

INT_SLEEP_ CHANGE(1)	Routing of activity/inactivity recognition event on INT. Default: 0 (0: routing of activity/inactivity event on INT disabled; 1: routing of activity/inactivity event on INT enabled)
INT_WU	Routing of wakeup event on INT. Default value: 0 (0: routing of wakeup event on INT disabled; 1: routing of wakeup event on INT enabled)
INT_6D	Routing of 6D event on INT. Default value: 0 (0: routing of 6D event on INT disabled; 1: routing of 6D event on INT enabled)
INT_EMB_FUNC	Routing of embedded functions event on INT. Default value: 0 (0: routing of embedded functions event on INT disabled; 1: routing embedded functions event on INT enabled)

1. Activity/Inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in *LIR_CONFIG (56h)* register.

9.44 INT_PD_CFG (62h)

INT pull-down register (r/w)

Table 119. INT_PD_CFG register

0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	PD_DIS_INT

1. This bit must be set to '0' for the correct operation of the device.

Table 120. INT_PD_CFG register description

PD_DIS_INT	This bit allows disabling the INT pull-down. (0: Pull-down on INT enabled (pull-down is effectively connected only when no interrupts are routed to the INT pin); 1: Pull-down on INT disabled (pull-down not connected).

9.45 INTERNAL_FREQ_FINE (63h)

Internal frequency register (r)

Table 121. INTERNAL_FREQ_FINE register

FREQ_FINE7	FREQ_FINE6	FREQ_FINE5	FREQ_FINE4	FREQ_FINE3	FREQ_FINE2	FREQ_FINE1	FREQ_FINE0

Table 122. INTERNAL_FREQ_FINE register description

FREQ_FINE[7:0]	Difference in percentage of the effective ODR (and timestamp rate) with respect to the typical. Step: 0.15%. 8-bit format, 2's complement.

9.46 X_OFS_USR (73h)

Accelerometer X-axis user offset correction (r/w). The offset value set in the X_OFS_USR offset register is internally subtracted from the acceleration value measured on the X-axis.

Table 123. X_OFS_USR register

X_OFS_USR_7	X_OFS_USR_6	X_OFS_USR_5	X_OFS_USR_4	X_OFS_USR_3	X_OFS_USR_2	X_OFS_USR_1	X_OFS_USR_0

Table 124. X_OFS_USR register description

X_OFS_USR_[7:0]	Accelerometer X-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in *CTRL6_C (15h)*. The value must be in the range [-127 127].

9.47 Y_OFS_USR (74h)

Accelerometer Y-axis user offset correction (r/w). The offset value set in the Y_OFS_USR offset register is internally subtracted from the acceleration value measured on the Y-axis.

Table 125. Y_OFS_USR register

Y_OFS_USR_7	Y_OFS_USR_6	Y_OFS_USR_5	Y_OFS_USR_4	Y_OFS_USR_3	Y_OFS_USR_2	Y_OFS_USR_1	Y_OFS_USR_0

Table 126. Y_OFS_USR register description

Y_OFS_USR_[7:0]	Accelerometer Y-axis user offset calibration expressed in 2's complement, weight depends on USR_OFF_W in *CTRL6_C (15h)*. The value must be in the range [-127, +127].

9.48 Z_OFS_USR (75h)

Accelerometer Z-axis user offset correction (r/w). The offset value set in the Z_OFS_USR offset register is internally subtracted from the acceleration value measured on the Z-axis.

Table 127. Z_OFS_USR register

Z_OFS_USR_7	Z_OFS_USR_6	Z_OFS_USR_5	Z_OFS_USR_4	Z_OFS_USR_3	Z_OFS_USR_2	Z_OFS_USR_1	Z_OFS_USR_0

Table 128. Z_OFS_USR register description

Z_OFS_USR_[7:0]	Accelerometer Z-axis user offset calibration expressed in 2's complement, weight depends on USR_OFF_W in *CTRL6_C (15h)*. The value must be in the range [-127, +127].

9.49 FIFO_DATA_OUT_TAG (78h)

FIFO tag register (r)

Table 129. FIFO_DATA_OUT_TAG register

TAG_SENSOR_4	TAG_SENSOR_3	TAG_SENSOR_2	TAG_SENSOR_1	TAG_SENSOR_0	TAG_CNT_1	TAG_CNT_0	TAG_PARITY

Table 130. FIFO_DATA_OUT_TAG register description

TAG_SENSOR_[4:0]	FIFO tag: identifies the sensor in: *FIFO_DATA_OUT_X_L (79h) and FIFO_DATA_OUT_X_H (7Ah)*, *FIFO_DATA_OUT_Y_L (7Bh) and FIFO_DATA_OUT_Y_H (7Ch)*, and *FIFO_DATA_OUT_Z_L (7Dh) and FIFO_DATA_OUT_Z_H (7Eh)* For details, refer to *Table 131: FIFO tag*
TAG_CNT_[1:0]	2-bit counter which identifies sensor time slot
TAG_PARITY	Parity check of TAG content

Table 131. FIFO tag

TAG_SENSOR_[4:0]	Sensor name
0x01	Gyroscope NC
0x02	Accelerometer NC
0x03	Temperature
0x04	Timestamp
0x05	CFG_Change
0x06	Accelerometer NC_T_2
0x07	Accelerometer NC_T_1
0x08	Accelerometer 2xC
0x09	Accelerometer 3xC
0x0A	Gyroscope NC_T_2
0x0B	Gyroscope NC_T_1
0x0C	Gyroscope 2xC
0x0D	Gyroscope 3xC

9.50 FIFO_DATA_OUT_X_L (79h) and FIFO_DATA_OUT_X_H (7Ah)

FIFO data output X (r)

Table 132. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 133. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L register description

D[15:0]	FIFO X-axis output

9.51 FIFO_DATA_OUT_Y_L (7Bh) and FIFO_DATA_OUT_Y_H (7Ch)

FIFO data output Y (r)

Table 134. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 135. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L register description

D[15:0]	FIFO Y-axis output

9.52 FIFO_DATA_OUT_Z_L (7Dh) and FIFO_DATA_OUT_Z_H (7Eh)

FIFO data output Z (r)

Table 136. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 137. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L register description

D[15:0]	FIFO Z-axis output

10 Embedded functions register mapping

The table given below provides a list of the registers for the embedded functions available in the device and the corresponding addresses. Embedded functions registers are accessible when FUNC_CFG_EN is set to '1' in *FUNC_CFG_ACCESS (01h)*.

Table 138. Register address map - embedded functions

Name	Type	Register address		Default	Comment
		Hex	Binary		
PAGE_SEL	r/w	02	00000010	00000001	
RESERVED	-	04	00000100		
EMB_FUNC_EN_B	r/w	05	00000101	00000000	
PAGE_ADDRESS	r/w	08	00001000	00000000	
PAGE_VALUE	r/w	09	00001001	00000000	
EMB_FUNC_INT	r/w	0A	00001010	00000000	
FSM_INT_A	r/w	0B	00001011	00000000	
FSM_INT_B	r/w	0C	00001100	00000000	
RESERVED	-	0E-10			
EMB_FUNC_STATUS	r	12	00010010	output	
FSM_STATUS_A	r	13	00010011	output	
FSM_STATUS_B	r	14	00010100	output	
PAGE_RW	r/w	17	00010111	00000000	
RESERVED	-	18-44			
FSM_ENABLE_A	r/w	46	01000110	00000000	
FSM_ENABLE_B	r/w	47	01000111	00000000	
FSM_LONG_COUNTER_L	r/w	48	01001000	00000000	
FSM_LONG_COUNTER_H	r/w	49	01001001	00000000	
FSM_LONG_COUNTER_CLEAR	r/w	4A	01001010	00000000	
FSM_OUTS1	r	4C	01001100	output	
FSM_OUTS2	r	4D	01001101	output	
FSM_OUTS3	r	4E	01001110	output	
FSM_OUTS4	r	4F	01001111	output	
FSM_OUTS5	r	50	01010000	output	
FSM_OUTS6	r	51	01010001	output	
FSM_OUTS7	r	52	01010010	output	
FSM_OUTS8	r	53	01010011	output	
FSM_OUTS9	r	54	01010100	output	

Table 138. Register address map - embedded functions (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
FSM_OUTS10	r	55	01010101	output	
FSM_OUTS11	r	56	01010110	output	
FSM_OUTS12	r	57	01010111	output	
FSM_OUTS13	r	58	01011000	output	
FSM_OUTS14	r	59	01011001	output	
FSM_OUTS15	r	5A	01011010	output	
FSM_OUTS16	r	5B	01011011	output	
RESERVED	-	5E	01011110		
EMB_FUNC_ODR_CFG_B	r/w	5F	01011111	01001011	
RESERVED	-	62-66			
EMB_FUNC_INIT_B	r/w	67	01100111	00000000	

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

11 Embedded functions register description

11.1 PAGE_SEL (02h)

Enable advanced features dedicated page (r/w)

Table 139. PAGE_SEL register

PAGE_SEL3	PAGE_SEL2	PAGE_SEL1	PAGE_SEL0	0(1)	0(1)	0(1)	1(2)

1. This bit must be set to '0' for the correct operation of the device.
2. This bit must be set to '1' for the correct operation of the device.

Table 140. PAGE_SEL register description

PAGE_SEL[3:0]	Select the advanced features dedicated page Default value: 0000

11.2 EMB_FUNC_EN_B (05h)

Embedded functions enable register (r/w)

Table 141. EMB_FUNC_EN_B register

0(1)	0(1)	0(1)	0(1)	FIFO_COMPR_EN	0(1)	0(1)	FSM_EN

1. This bit must be set to '0' for the correct operation of the device.

Table 142. EMB_FUNC_EN_B register description

FIFO_COMPR_EN(1)	Enable FIFO compression feature. Default value: 0 (0: FIFO compression feature disabled; 1: FIFO compression feature enabled)
FSM_EN	Enable Finite State Machine (FSM) feature. Default value: 0 (0: FSM feature disabled; 1: FSM feature enabled)

1. This bit is effective if the FIFO_COMPR_RT_EN bit of *FIFO_CTRL2 (08h)* is set to 1.

11.3 PAGE_ADDRESS (08h)

Page address register (r/w)

Table 143. PAGE_ADDRESS register

PAGE_ADDR7	PAGE_ADDR6	PAGE_ADDR5	PAGE_ADDR4	PAGE_ADDR3	PAGE_ADDR2	PAGE_ADDR1	PAGE_ADDR0

Table 144. PAGE_ADDRESS register description

PAGE_ADDR[7:0]	After setting the bit PAGE_WRITE / PAGE_READ in register *PAGE_RW (17h)*, this register is used to set the address of the register to be written/read in the advanced features page selected through the bits PAGE_SEL[3:0] in register *PAGE_SEL (02h)*.

11.4 PAGE_VALUE (09h)

Page value register (r/w)

Table 145. PAGE_VALUE register

PAGE_ VALUE7	PAGE_ VALUE6	PAGE_ VALUE5	PAGE_ VALUE4	PAGE_ VALUE3	PAGE_ VALUE2	PAGE_ VALUE1	PAGE_ VALUE0

Table 146. PAGE_VALUE register description

PAGE_VALUE[7:0]	These bits are used to write (if the bit PAGE_WRITE = 1 in register *PAGE_RW (17h)*) or read (if the bit PAGE_READ = 1 in register *PAGE_RW (17h)*) the data at the address PAGE_ADDR[7:0] of the selected advanced features page.

11.5 EMB_FUNC_INT (0Ah)

INT pin control register (r/w)

Each bit in this register enables a signal to be carried over INT. The pin's output will supply the OR combination of the selected signals.

Table 147. EMB_FUNC_INT register

INT_ FSM_ LC	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 148. EMB_FUNC_INT register description

INT_FSM_LC(1)	Routing of FSM long counter timeout interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)

1. This bit is effective if the INT_EMB_FUNC bit of *MD1_CFG (5Eh)* is set to 1.

11.6 FSM_INT_A (0Bh)

INT pin control register (r/w).

Each bit in this register enables a signal to be carried over INT. The pin's output will supply the OR combination of the selected signals.

Table 149. FSM_INT_A register

INT_ FSM8	INT_ FSM7	INT_ FSM6	INT_ FSM5	INT_ FSM4	INT_ FSM3	INT_ FSM2	INT_ FSM1

Table 150. FSM_INT_A register description

INT_FSM8(1)	Routing of FSM8 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM7(1)	Routing of FSM7 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM6(1)	Routing of FSM6 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM5(1)	Routing of FSM5 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM4(1)	Routing of FSM4 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM3(1)	Routing of FSM3 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM2(1)	Routing of FSM2 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM1(1)	Routing of FSM1 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)

1. This bit is effective if the INT_EMB_FUNC bit of *MD1_CFG (5Eh)* is set to 1.

11.7 FSM_INT_B (0Ch)

INT pin control register (r/w).

Each bit in this register enables a signal to be carried over INT. The pin's output will supply the OR combination of the selected signals.

Table 151. FSM_INT_B register

INT_ FSM16	INT_ FSM15	INT_ FSM14	INT_ FSM13	INT_ FSM12	INT_ FSM11	INT_ FSM10	INT_ FSM9

Table 152. FSM_INT_B register description

INT_FSM16(1)	Routing of FSM16 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM15(1)	Routing of FSM15 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM14(1)	Routing of FSM14 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM13(1)	Routing of FSM13 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM12(1)	Routing of FSM12 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM11(1)	Routing of FSM11 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM10(1)	Routing of FSM10 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)
INT_FSM9(1)	Routing of FSM9 interrupt event on INT. Default value: 0 (0: routing on INT disabled; 1: routing on INT enabled)

1. This bit is effective if the INT_EMB_FUNC bit of *MD1_CFG (5Eh)* is set to 1.

11.8 EMB_FUNC_STATUS (12h)

Embedded function status register (r).

Table 153. EMB_FUNC_STATUS register

IS_FSM_LC	0	0	0	0	0	0	0

Table 154. EMB_FUNC_STATUS register description

IS_FSM_LC	Interrupt status bit for FSM long counter timeout interrupt event. (1: interrupt detected; 0: no interrupt)

11.9 FSM_STATUS_A (13h)

Finite State Machine status register (r).

Table 155. FSM_STATUS_A register

IS_FSM8	IS_FSM7	IS_FSM6	IS_FSM5	IS_FSM4	IS_FSM3	IS_FSM2	IS_FSM1

Table 156. FSM_STATUS_A register description

IS_FSM8	Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM7	Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM6	Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM5	Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM4	Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM3	Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM2	Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM1	Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt)

11.10 FSM_STATUS_B (14h)

Finite State Machine status register (r).

Table 157. FSM_STATUS_B register

IS_FSM16	IS_FSM15	IS_FSM14	IS_FSM13	IS_FSM12	IS_FSM11	IS_FSM10	IS_FSM9

Table 158. FSM_STATUS_B register description

IS_FSM16	Interrupt status bit for FSM16 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM15	Interrupt status bit for FSM15 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM14	Interrupt status bit for FSM14 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM13	Interrupt status bit for FSM13 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM12	Interrupt status bit for FSM12 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM11	Interrupt status bit for FSM11 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM10	Interrupt status bit for FSM10 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM9	Interrupt status bit for FSM9 interrupt event. (1: interrupt detected; 0: no interrupt)

11.11 PAGE_RW (17h)

Enable read and write mode of advanced features dedicated page (r/w)

Table 159. PAGE_RW register

EMB_ FUNC_LIR	PAGE_ WRITE	PAGE_ READ	0(1)	0(1)	0(1)	0(1)	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 160. PAGE_RW register description

EMB_FUNC_LIR	Latched Interrupt mode for Embedded Functions. Default value: 0 (0: Embedded Functions interrupt request not latched; 1: Embedded Functions interrupt request latched)
PAGE_WRITE	Enable writes to the selected advanced features dedicated page(1). Default value: 0 (1: enable; 0: disable)
PAGE_READ	Enable reads from the selected advanced features dedicated page(1). Default value: 0 (1: enable; 0: disable)

1. Page selected by PAGE_SEL[3:0] in *PAGE_SEL (02h)* register.

11.12 FSM_ENABLE_A (46h)

FSM enable register (r/w).

Table 161. FSM_ENABLE_A register

FSM8_EN	FSM7_EN	FSM6_EN	FSM5_EN	FSM4_EN	FSM3_EN	FSM2_EN	FSM1_EN

Table 162. FSM_ENABLE_A register description

FSM8_EN	FSM8 enable. Default value: 0 (0: FSM8 disabled; 1: FSM8 enabled)
FSM7_EN	FSM7 enable. Default value: 0 (0: FSM7 disabled; 1: FSM7 enabled)
FSM6_EN	FSM6 enable. Default value: 0 (0: FSM6 disabled; 1: FSM6 enabled)
FSM5_EN	FSM5 enable. Default value: 0 (0: FSM5 disabled; 1: FSM5 enabled)
FSM4_EN	FSM4 enable. Default value: 0 (0: FSM4 disabled; 1: FSM4 enabled)
FSM3_EN	FSM3 enable. Default value: 0 (0: FSM3 disabled; 1: FSM3 enabled)
FSM2_EN	FSM2 enable. Default value: 0 (0: FSM2 disabled; 1: FSM2 enabled)
FSM1_EN	FSM1 enable. Default value: 0 (0: FSM1 disabled; 1: FSM1 enabled)

11.13 FSM_ENABLE_B (47h)

FSM enable register (r/w).

Table 163. FSM_ENABLE_B register

FSM16_EN	FSM15_EN	FSM14_EN	FSM13_EN	FSM12_EN	FSM11_EN	FSM10_EN	FSM9_EN

Table 164. FSM_ENABLE_B register description

FSM16_EN	FSM16 enable. Default value: 0 (0: FSM16 disabled; 1: FSM16 enabled)
FSM15_EN	FSM15 enable. Default value: 0 (0: FSM15 disabled; 1: FSM15 enabled)
FSM14_EN	FSM14 enable. Default value: 0 (0: FSM14 disabled; 1: FSM14 enabled)
FSM13_EN	FSM13 enable. Default value: 0 (0: FSM13 disabled; 1: FSM13 enabled)
FSM12_EN	FSM12 enable. Default value: 0 (0: FSM12 disabled; 1: FSM12 enabled)
FSM11_EN	FSM11 enable. Default value: 0 (0: FSM11 disabled; 1: FSM11 enabled)
FSM10_EN	FSM10 enable. Default value: 0 (0: FSM10 disabled; 1: FSM10 enabled)
FSM9_EN	FSM9 enable. Default value: 0 (0: FSM9 disabled; 1: FSM9 enabled)

11.14 FSM_LONG_COUNTER_L (48h) and FSM_LONG_COUNTER_H (49h)

FSM long counter status register (r/w).

Long counter value is an unsigned integer value (16-bit format); this value can be reset using the LC_CLEAR bit in *FSM_LONG_COUNTER_CLEAR (4Ah)* register.

Table 165. FSM_LONG_COUNTER_L register

FSM_LC_7	FSM_LC_6	FSM_LC_5	FSM_LC_4	FSM_LC_3	FSM_LC_2	FSM_LC_1	FSM_LC_0

Table 166. FSM_LONG_COUNTER_L register description

FSM_LC_[7:0]	Long counter current value (LSbyte). Default value: 00000000

Table 167. FSM_LONG_COUNTER_H register

FSM_LC_15	FSM_LC_14	FSM_LC_13	FSM_LC_12	FSM_LC_11	FSM_LC_10	FSM_LC_9	FSM_LC_8

Table 168. FSM_LONG_COUNTER_H register description

FSM_LC_[15:8]	Long counter current value (MSbyte). Default value: 00000000

11.15 FSM_LONG_COUNTER_CLEAR (4Ah)

FSM long counter reset register (r/w).

Table 169. FSM_LONG_COUNTER_CLEAR register

0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	FSM_LC_CLEARED	FSM_LC_CLEAR

1. This bit must be set to '0' for the correct operation of the device.

Table 170. FSM_LONG_COUNTER_CLEAR register description

FSM_LC_CLEARED	This read-only bit is automatically set to 1 when the long counter reset is done. Default value: 0
FSM_LC_CLEAR	Clear FSM long counter value. Default value: 0

11.16 FSM_OUTS1 (4Ch)

FSM1 output register (r).

Table 171. FSM_OUTS1 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 172. FSM_OUTS1 register description

P_X	FSM1 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM1 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM1 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM1 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM1 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM1 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM1 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM1 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.17 FSM_OUTS2 (4Dh)

FSM2 output register (r).

Table 173. FSM_OUTS2 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 174. FSM_OUTS2 register description

P_X	FSM2 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM2 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM2 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM2 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM2 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM2 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM2 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM2 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.18 FSM_OUTS3 (4Eh)

FSM3 output register (r).

Table 175. FSM_OUTS3 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 176. FSM_OUTS3 register description

P_X	FSM3 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM3 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM3 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM3 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM3 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM3 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM3 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM3 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.19 FSM_OUTS4 (4Fh)

FSM4 output register (r).

Table 177. FSM_OUTS4 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 178. FSM_OUTS4 register description

P_X	FSM4 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM4 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM4 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM4 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM4 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM4 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM4 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM4 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.20 FSM_OUTS5 (50h)

FSM5 output register (r).

Table 179. FSM_OUTS5 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 180. FSM_OUTS5 register description

P_X	FSM5 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM5 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM5 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM5 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM5 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM5 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM5 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM5 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.21 FSM_OUTS6 (51h)

FSM6 output register (r).

Table 181. FSM_OUTS6 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 182. FSM_OUTS6 register description

P_X	FSM6 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM6 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM6 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM6 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM6 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM6 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM6 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM6 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.22 FSM_OUTS7 (52h)

FSM7 output register (r).

Table 183. FSM_OUTS7 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 184. FSM_OUTS7 register description

P_X	FSM7 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM7 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM7 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM7 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM7 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM7 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM7 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM7 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.23 FSM_OUTS8 (53h)

FSM8 output register (r).

Table 185. FSM_OUTS8 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 186. FSM_OUTS8 register description

P_X	FSM8 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM8 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM8 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM8 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM8 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM8 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM8 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM8 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.24 FSM_OUTS9 (54h)

FSM9 output register (r).

Table 187. FSM_OUTS9 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 188. FSM_OUTS9 register description

P_X	FSM9 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM9 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM9 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM9 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM9 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM9 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM9 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM9 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.25 FSM_OUTS10 (55h)

FSM10 output register (r).

Table 189. FSM_OUTS10 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 190. FSM_OUTS10 register description

P_X	FSM10 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM10 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM10 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM10 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM10 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM10 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM10 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM10 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.26 FSM_OUTS11 (56h)

FSM11 output register (r).

Table 191. FSM_OUTS11 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 192. FSM_OUTS11 register description

P_X	FSM11 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM11 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM11 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM11 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM11 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM11 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM11 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM11 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.27 FSM_OUTS12 (57h)

FSM12 output register (r).

Table 193. FSM_OUTS12 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 194. FSM_OUTS12 register description

P_X	FSM12 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM12 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM12 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM12 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM12 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM12 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM12 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM12 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.28 FSM_OUTS13 (58h)

FSM13 output register (r).

Table 195. FSM_OUTS13 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 196. FSM_OUTS13 register description

P_X	FSM13 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM13 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM13 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM13 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM13 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM13 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM13 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM13 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.29 FSM_OUTS14 (59h)

FSM14 output register (r).

Table 197. FSM_OUTS14 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 198. FSM_OUTS14 register description

P_X	FSM14 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM14 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM14 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM14 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM14 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM14 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM14 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM14 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.30 FSM_OUTS15 (5Ah)

FSM15 output register (r).

Table 199. FSM_OUTS15 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 200. FSM_OUTS15 register description

P_X	FSM15 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM15 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM15 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM15 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM15 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM15 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM15 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM15 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.31 FSM_OUTS16 (5Bh)

FSM16 output register (r).

Table 201. FSM_OUTS16 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 202. FSM_OUTS16 register description

P_X	FSM16 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM16 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM16 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM16 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM16 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM16 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM16 output: positive event detected on the vector. (0: event not detected; 1: event detected
N_V	FSM16 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.32 EMB_FUNC_ODR_CFG_B (5Fh)

Finite State Machine output data rate configuration register (r/w).

Table 203. EMB_FUNC_ODR_CFG_B register

0(1)	1(2)	0(1)	FSM_ ODR1	FSM_ ODR0	0(1)	1(2)	1(2)

1. This bit must be set to '0' for the correct operation of the device.
2. This bit must be set to '1' for the correct operation of the device.

Table 204. EMB_FUNC_ODR_CFG_B register description

FSM_ODR[1:0]	Finite State Machine ODR configuration: (00: 12.5 Hz; 01: 26 Hz (default); 10: 52 Hz; 11: 104 Hz)

11.33 EMB_FUNC_INIT_B (67h)

Embedded functions initialization register (r/w)

Table 205. EMB_FUNC_INIT_B register

0(1)	0(1)	0(1)	0(1)	FIFO_ COMPR_ INIT	0(1)	0(1)	FSM_INIT

1. This bit must be set to '0' for the correct operation of the device.

Table 206. EMB_FUNC_INIT_B register description

FIFO_COMPR_INIT	FIFO compression feature initialization request. Default value: 0
FSM_INIT	FSM initialization request. Default value: 0

12 Embedded advanced features pages

The table given below provides a list of the registers for the embedded advanced features page 1. These registers are accessible when PAGE_SEL[3:0] are set to 0001 in *PAGE_SEL (02h)*.

Table 207. Register address map - embedded advanced features page 1

Name	Type	Register address		Default	Comment
		Hex	Binary		
FSM_LC_TIMEOUT_L	r/w	7A	01111010	00000000	
FSM_LC_TIMEOUT_H	r/w	7B	01111011	00000000	
FSM_PROGRAMS	r/w	7C	01111100	00000000	
FSM_START_ADD_L	r/w	7E	01111110	00000000	
FSM_START_ADD_H	r/w	7F	01111111	00000000	

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

13 Embedded advanced features register description

13.1 Page 1 - Embedded advanced features registers

13.1.1 FSM_LC_TIMEOUT_L (7Ah) and FSM_LC_TIMEOUT_H (7Bh)

FSM long counter timeout register (r/w).

The long counter timeout value is an unsigned integer value (16-bit format). When the long counter value reached this value, the FSM generates an interrupt.

Table 208. FSM_LC_TIMEOUT_L register

FSM_LC_TIMEOUT 7	FSM_LC_TIMEOUT 6	FSM_LC_TIMEOUT 5	FSM_LC_TIMEOUT 4	FSM_LC_TIMEOUT 3	FSM_LC_TIMEOUT 2	FSM_LC_TIMEOUT 1	FSM_LC_TIMEOUT 0

Table 209. FSM_LC_TIMEOUT_L register description

FSM_LC_TIMEOUT[7:0]	FSM long counter timeout value (LSbyte). Default value: 00000000

Table 210. FSM_LC_TIMEOUT_H register

FSM_LC_TIMEOUT 15	FSM_LC_TIMEOUT 14	FSM_LC_TIMEOUT 13	FSM_LC_TIMEOUT 12	FSM_LC_TIMEOUT 11	FSM_LC_TIMEOUT 10	FSM_LC_TIMEOUT 9	FSM_LC_TIMEOUT 8

Table 211. FSM_LC_TIMEOUT_H register description

FSM_LC_TIMEOUT[15:8]	FSM long counter timeout value (MSbyte). Default value: 00000000

13.1.2 FSM_PROGRAMS (7Ch)

FSM number of programs register (r/w).

Table 212. FSM_PROGRAMS register

FSM_N_PROG7	FSM_N_PROG6	FSM_N_PROG5	FSM_N_PROG4	FSM_N_PROG3	FSM_N_PROG2	FSM_N_PROG1	FSM_N_PROG0

Table 213. FSM_PROGRAMS register description

FSM_N_PROG[7:0]	Number of FSM programs; must be less than or equal to 16. Default value: 00000000

13.1.3 FSM_START_ADD_L (7Eh) and FSM_START_ADD_H (7Fh)

FSM start address register (r/w). First available address is 0x033C.

Table 214. FSM_START_ADD_L register

FSM_ START7	FSM_ START6	FSM_ START5	FSM_ START4	FSM_ START3	FSM_ START2	FSM_ START1	FSM_ START0

Table 215. FSM_START_ADD_L register description

FSM_START[7:0]	FSM start address value (LSbyte). Default value: 00000000

Table 216. FSM_START_ADD_H register

FSM_ START15	FSM_ START14	FSM_ START13	FSM_ START12	FSM_ START11	FSM_ START10	FSM_ START9	FSM_ START8

Table 217. FSM_START_ADD_H register description

FSM_START[15:8]	FSM start address value (MSbyte). Default value: 00000000

14 Pull-up configuration register

The PU_CONFIG register is accessible when PU_REG_ACCESS is set to '1' in *FUNC_CFG_ACCESS (01h)*.

Table 218. Pull-up configuration register

Name	Type	Register address		Default	Comment
		Hex	Binary		
PU_CONFIG	rw	14	00010100	00000000	

14.1 PU_CONFIG (14h)

Pull-up configuration register (r/w)

Table 219. PU_CONFIG register

0(1)	0(1)	0(1)	0(1)	PU_EN	0(1)	0(1)	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 220. PU_CONFIG register description

PU_EN	Pull-up enable for pin 2 and pin 3. Default value: 0 (0: internal pull-up disabled; 1: internal pull-up enabled)

15 Soldering information

The LGA package is compliant with the ECOPACK, RoHS and "Green" standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

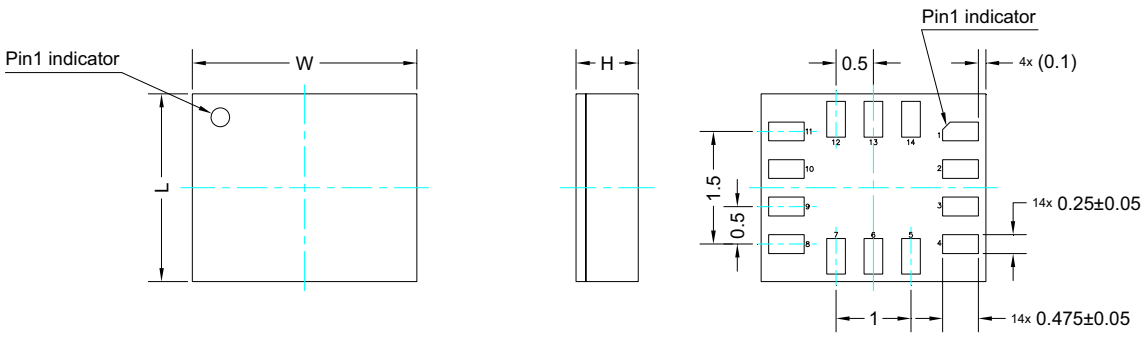
Land pattern and soldering recommendations are available at www.st.com/mems.

16 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com.
ECOPACK is an ST trademark.

16.1 LGA-14L package information

Figure 19. LGA-14L 2.5x3x0.86 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General tolerance is +/-0.1mm unless otherwise specified

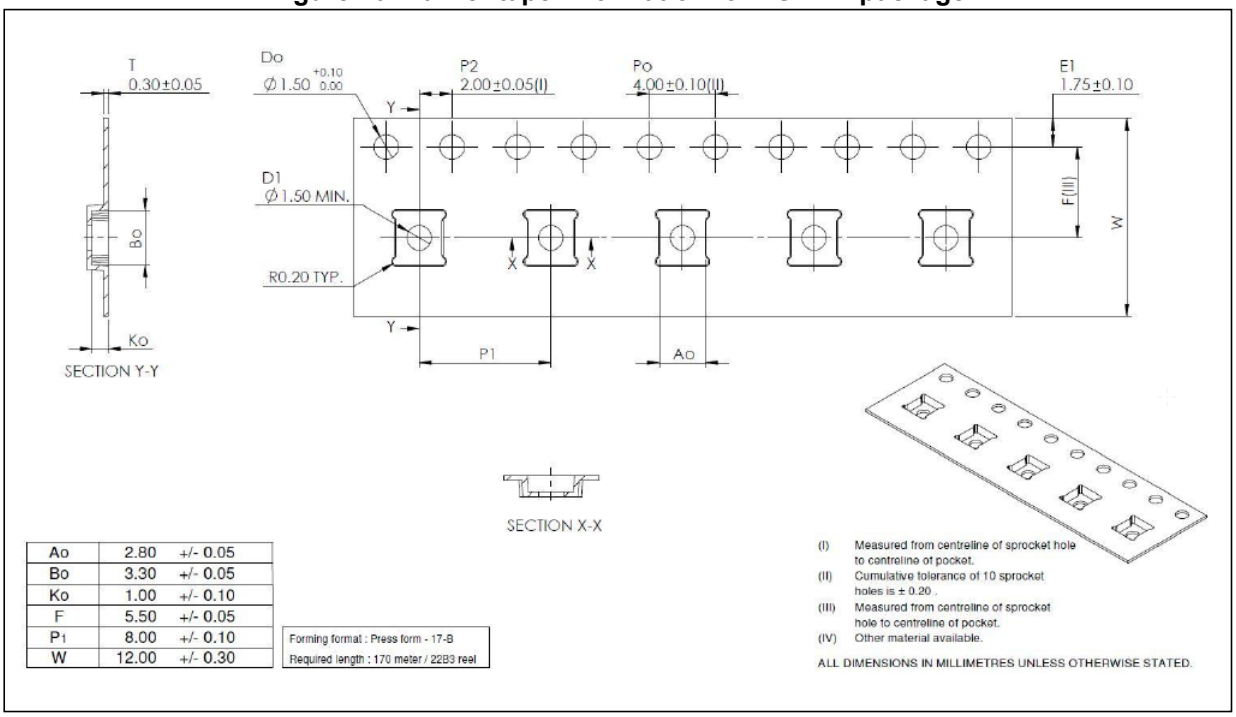
OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.50	±0.1
Width [W]	3.00	±0.1
Height [H]	0.86	MAX

DM00249496_1

16.2 LGA-14 packing information

Figure 20. Carrier tape information for LGA-14 package



Ao	2.80	+/- 0.05
Bo	3.30	+/- 0.05
Ko	1.00	+/- 0.10
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

Figure 21. LGA-14 package orientation in carrier tape

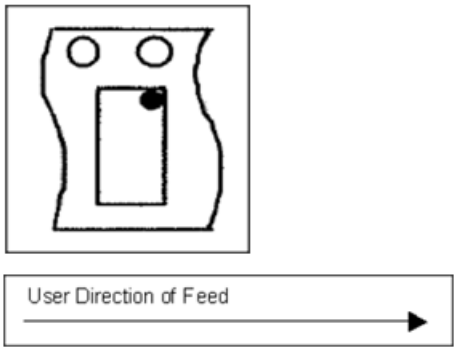


Figure 22. Reel information for carrier tape of LGA-14 package

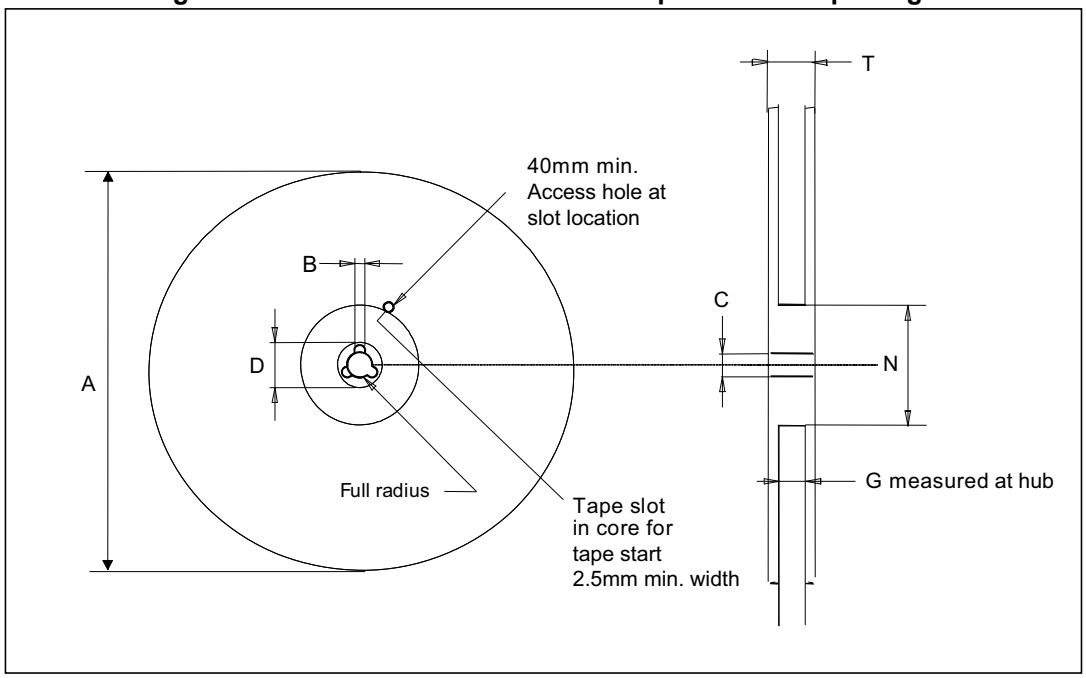


Table 221. Reel dimensions for carrier tape of LGA-14 package

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

17 Revision history

Table 222. Document revision history

Date	Revision	Changes
17-Feb-2020	5	First public release

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