

The ABLIC Inc. HDL6M05543 is a quad, true 5-level RTZ, high-voltage, high-speed ultrasound pulser. The HDL6M05543 comprises logic interfaces, level translators, MOSFET gate drive buffers with floating voltage regulators, high-voltage, high-current MOSFETs, and active T/R switches.

Functions

- Quad true 5-level pulser with active T/R switch with 3-input per channel

Features

- 0 to $\pm 100\text{V}$ output voltage
- $\pm 2\text{A}$ source and sink peak current for the 1st high-voltage (HV) pulses (V_{PP1}/V_{NN1})
- $\pm 2\text{A}$ source and sink peak current with $\pm 1\text{A}$ active clamp for the 2nd HV pulses (V_{PP2}/V_{NN2})
- $\pm 2\text{A}$ source and sink peak current for active ground clamp
- 250Ω ($\pm 0.1\text{A}$) active ground clamp without blocking diode for anti-leakage (Analog SW type)
- Embedded floating voltage regulators
- Symmetrical positive and negative pulse waveforms for low 2nd order harmonic distortion
- Up to 200MHz LVDS/LVCMOS clock with 2-bit edge control (transparent mode available)
- 10Ω active T/R switch with 2-bit turn-on timing control
- 20MHz output frequency @ $\pm 60\text{V}$ output, 220pF load
- 1.8V to 5V CMOS logic interface
- Noise-cut diodes at each HV output
- 4-mode output current control for the 2nd HV rail
- Automatic thermal protection with indicator
- Power-up/down reset function for free power sequencing and for fail-safe in abrupt power drop
- Latch-up free, low crosstalk between channels by SOI CMOS technology
- 64-lead 9x9mm QFN package (RoHS compliant)

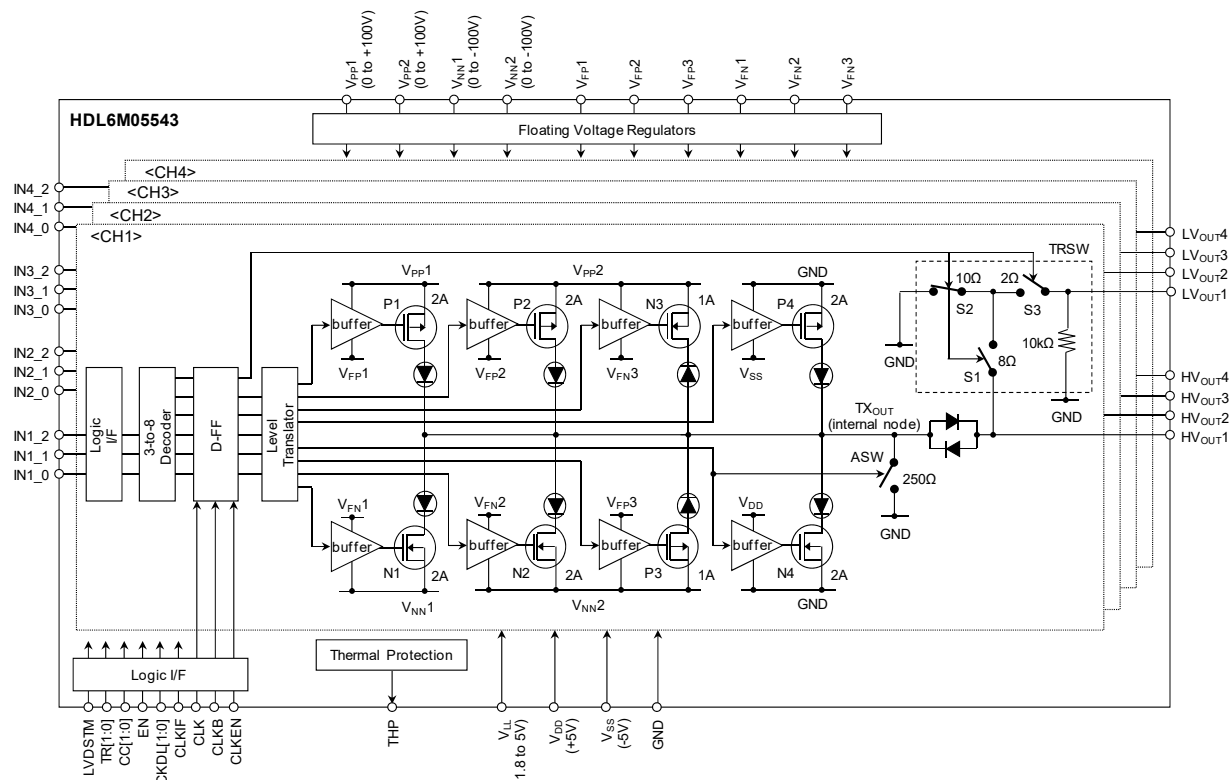


Fig.1 Block diagram

1. Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Logic supply voltage	V _{LL}	-0.4 to +7	V	
2	Positive supply voltage	V _{DD}	-0.4 to +7	V	
3	Negative supply voltage	V _{SS}	-7 to +0.4	V	
4	Positive high-voltage supplies	V _{PP1} , V _{PP2}	-0.5 to +105	V	
5	Negative high-voltage supplies	V _{NN1} , V _{NN2}	-105 to +0.5	V	
6	Positive high-voltage difference	(V _{PP1} -V _{PP2})	-105 to +105	V	
7	Negative high-voltage difference	(V _{NN1} -V _{NN2})	-105 to +105	V	
8	High-voltage outputs (x=1~4)	HV _{OUTX}	-105 to +105	V	
9	Low-voltage outputs (x=1~4)	LV _{OUTX}	-1 to +1	V	
10	THP (Thermal Protection) output	THP	-0.4 to +7	V	
11	All Logic input voltages (x=1~4)	INx [2:0], EN, CLKEN, CLK, CLKB, CLKIF, CKDL[1:0], CC[1:0], TR[1:0], LVDSTM	-0.4 to +7	V	
12	Operating junction temperature	T _{Jop}	-20 to +150	°C	
13	Operating free-air Temperature	T _A	0 to +75	°C	
14	Storage temperature	T _{STG}	-55 to +150	°C	
15	Maximum power dissipation	P _{Dmax}	4	W	

NOTE: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Logic Inputs, and Power sequencing

2.1 Operating Supply Voltages

Table 2 Operating Supply Voltages

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V _{LL}	2.4	2.5 to 3.3	3.6	V	Clock mode
			1.7	1.8 to 5	V _{DD}	V	Transparent mode
2	Positive supply voltage	V _{DD}	4.75	5	5.25	V	
3	Negative supply voltage	V _{SS}	-5.25	-5	-4.75	V	
4	Positive high-voltage supplies	V _{PP1} , V _{PP2}	0	-	100	V	
5	Negative high-voltage supplies	V _{NN1} , V _{NN2}	-100	-	0	V	
6	Positive high-voltage difference	(V _{PP1} -V _{PP2})	-100	-	100	V	
7	Negative high-voltage difference	(V _{NN1} -V _{NN2})	-100	-	100	V	
8	IC substrate voltage *	V _{SUB}	-	0	-	V	
9	V _{PPX} , V _{NNX} slew rate (x=1,2)	SR _{MAX}	-	-	25	V/ms	

NOTE: * The package exposed pad internally connected to the IC substrate must be soldered to the ground.

2.2 Logic Inputs

Clock (CLK) mode synchronizes data inputs INx_[2:0] (x=1~4) with a differential LVDS/CMOS clock. Transparent (TP) mode without using clock is also available.

CLK mode:

Set CLKEN=0. INx_[2:0] are decoded, clocked, level-translated, then sent to high-voltage output stage.

Differential clock input has two modes as shown below.

- LVDS CLK mode: set CLKIF=0. See Table 3 and 4 for the logic inputs, CLK, and CLKB.
- CMOS CLK mode: set CLKIF=1. See Table 3 for all the logic inputs.

TP mode:

Set CLKEN=CLKIF=1, CLK=CLKB=0. INx_[2:0] are decoded, level-translated, then sent to high-voltage output stage. See Table 3 for all the logic inputs.

Table 3 Logic Inputs

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level logic input voltage	V _{IH}	0.8V _{LL}	-	V _{LL}	V	
2	Low-level logic input voltage	V _{IL}	0	-	0.2V _{LL}	V	
3	Logic input capacitance	C _{IN}	-	3	-	pF	
4	Logic input high current *1	I _{IH}	-10	-	10	μA	
5	Logic input low current *2	I _{IL}	-10	-	10	μA	
6	Input rise/fall time	t _r , t _f	-	-	800	ps	CLK≥100MHz CMOS CLK mode
			-	-	2.0	ns	CLK<100MHz 10~90% CLK, CLKB, INx_[2:0]
7	Input clock frequency	f _{CLK}	-	-	200	MHz	CMOS CLK mode, CLK, CLKB,
8	Duty cycle	D _{CLK}	40	50	60	%	f _{CLK} =1/T, D _{CLK} =t/T, See Fig.3
9	Data Setup time	t _{SU}	1.4	-	-	ns	CLK mode, CKDL[1:0]='00'
10	Data Hold time	t _{HLD}	1.4	-	-	ns	INx_[2:0] to CLK/CLKB, See Fig.3

NOTE:

*1) TR[1:0], CKDL[1:0], and LVDSTM have 50μA leak at V_{LL}=2.5V due to 50kΩ internal pull-down resistor.

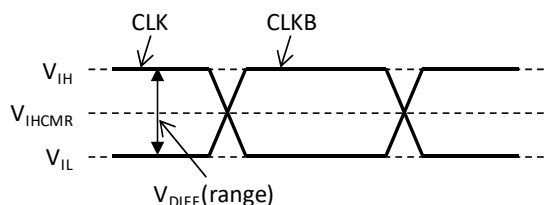
*2) EN, CC[1:0], CLKEN, and CLKIF have 50μA leak at V_{LL}=2.5V due to 50kΩ internal pull-up resistor.

Table 4 LVDS Clock Inputs (CLK, CLKB)

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level input voltage	V _{IH}	1.265	-	-	V	V _{IHCMR} (Typ)+V _{DIFF} (Min)/2
2	Low-level input voltage	V _{IL}	-	-	1.135	V	V _{IHCMR} (Typ)-V _{DIFF} (Min)/2
3	Differential input voltage range	V _{DIFF} (range)	0.13	0.35	0.49	±V	same as CLK,CLKB voltage swing See Fig.2
4	Differential input voltage peak to peak swing	V _{DIFF} (p-p)	0.26	0.7	0.98	V _{pp}	CLK-CLKB differential peak-to-peak voltage swing, See Fig.2
5	Input voltage common mode range	V _{IHCMR}	0.84	1.2	1.56	V	
6	Differential input impedance	R _{IN}	85	100	115	Ω	LVDSTM=1
7	High-level input current	I _{IH}	-	-	5.8	mA	
8	Low-level input current	I _{IL}	-	-	5.8	mA	
9	Input rise/fall time	t _r , t _f	-	-	600	ps	20% to 80% of V _{DIFF}
10	Input clock frequency	f _{CLK}	-	-	200	MHz	LVDS CLK mode, CLK, CLKB,
11	Duty cycle	D _{CLK}	40	50	60	%	f _{CLK} =1/T, D _{CLK} =t/T, See Fig.3

NOTE: Please refer to table 3 for the logic inputs other than CLK, CLKB in LVDS CLK mode.

Differential input voltage range ($V_{DIFF(range)}$)



Differential input voltage peak to peak swing ($V_{DIFF(p-p)}$)

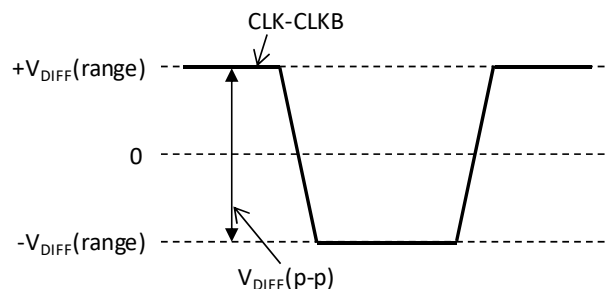
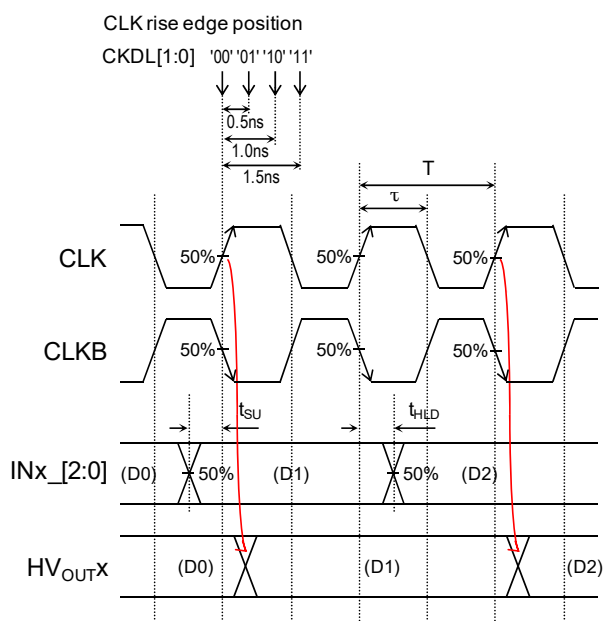


Fig.2 LVDS clock inputs

LVDS/CMOS CLK mode (CLKEN=0)



TP mode (CLKEN=1)

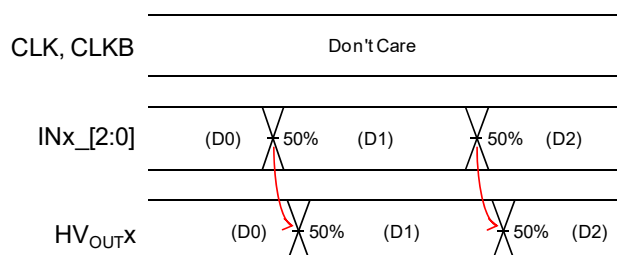


Fig.3 Setup/Hold Time

2.3 Power Supply Sequencing

Embedded low-voltage (LV) power-up/down reset function provides free power supply sequencing.

It also provides fail-safe system in abrupt LV power supply drop.

When any one of LV power supplies is turned off during operation, all internal circuits will be immediately reset, and both inputs and outputs will be disabled.

Once all LV power supplies are restored, both inputs and outputs will be enabled.

3. Typical Application Circuit

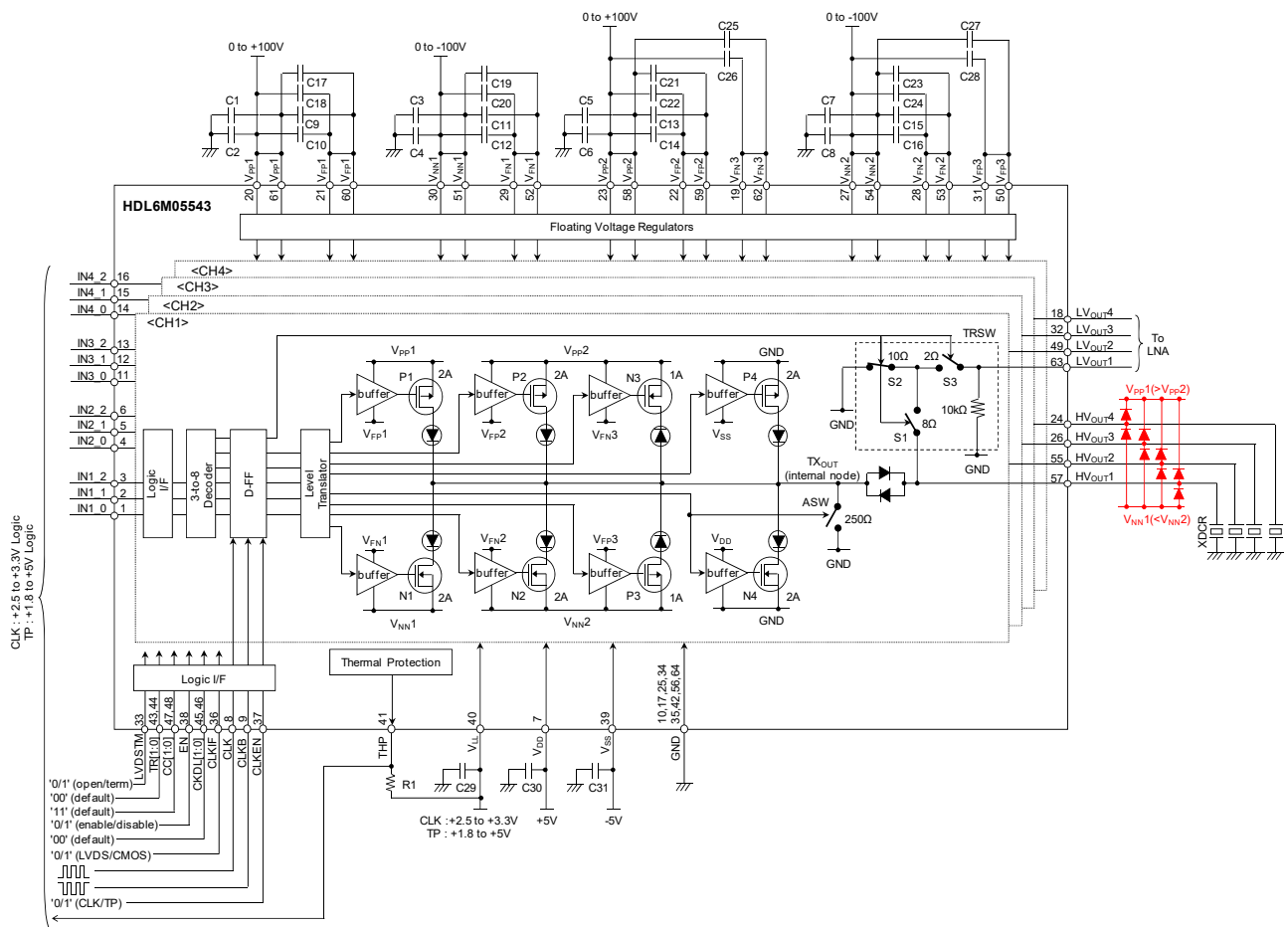


Fig.4 Typical Application Circuit

Note:

1. High-voltage power supply pins, V_{PPX}/V_{NNX} ($x=1,2$), can draw fast transient currents up to $\pm 2.0A$. Therefore, ceramic capacitors of $\geq 200V$ $0.1\mu F$ to $1\mu F$ (C1~8) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of $\geq 16V$ $10\mu F$ (C9~16), $\geq 16V$ $100nF$ (C17~28), and $\geq 16V$ $0.1\mu F$ to $1\mu F$ (C29~31) should also be connected between high-voltage power supply pins and corresponding floating voltage pins V_{PPX}/V_{FNX} , and low-voltage power supply pins for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. Please refer to Mode Control Tables for detailed CC[1:0], TR[1:0], and CKDL[1:0] setting.
6. High-voltage diodes (e.g. BAV23S) between HV_{OUTX} and V_{PP1}/V_{NN1} (highest voltage) are recommended to clamp excessive voltage overshoot caused by reverberation.

4. Electrical Characteristics

4.1 Operating Supply Currents

Table 5 Operating Supply Currents

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $T_A=25^{\circ}C$, $CLK=CLKB=100MHz/0(CLKEN=0/1)$, $TR[1:0]=CKDL[1:0]='00'$,
 HV_{OUT} load= $220pF//200\Omega$, LV_{OUT} load= $47pF//200\Omega$, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	V_{LL} current	TP	I_{LLQD}	-	0.0	-	mA	Quiescent current-1 $EN=1$ (Disable) $INx_ [2:0]='000'$ Current mode 3 ($CC[1:0]='11'$) $V_{PP1}/V_{NN1}=+/-100V$ $V_{PP2}/V_{NN2}=+/-100V$
		LVDS CLK		-	0.1	-	mA	
		CMOS CLK		-	0.05	-	mA	
2	V_{DD} current	TP	I_{DDQD}	-	2.4	-	mA	
		LVDS CLK		-	2.4	-	mA	
		CMOS CLK		-	2.4	-	mA	
3	V_{SS} current		I_{SSQD}	-	0.62	-	mA	
4	V_{PP1} current		I_{PP1QD}	-	0.04	-	mA	
5	V_{NN1} current		I_{NN1QD}	-	0.04	-	mA	
6	V_{PP2} current		I_{PP2QD}	-	0.04	-	mA	
7	V_{NN2} current		I_{NN2QD}	-	0.04	-	mA	
8	V_{LL} current	TP	I_{LLQE}	-	0.05	-	mA	Quiescent current-2 $EN=0$ (Enable) $INx_ [2:0]='000'$ Current mode 3 ($CC[1:0]='11'$) $V_{PP1}/V_{NN1}=+/-100V$ $V_{PP2}/V_{NN2}=+/-100V$
		LVDS CLK		-	0.15	-	mA	
		CMOS CLK		-	0.1	-	mA	
9	V_{DD} current	TP	I_{DDQE}	-	3	-	mA	
		LVDS CLK		-	15	-	mA	
		CMOS CLK		-	13	-	mA	
10	V_{SS} current		I_{SSQE}	-	0.9	-	mA	
11	V_{PP1} current		I_{PP1QE}	-	0.16	-	mA	
12	V_{NN1} current		I_{NN1QE}	-	0.16	-	mA	
13	V_{PP2} current		I_{PP2QE}	-	0.16	-	mA	
14	V_{NN2} current		I_{NN2QE}	-	0.16	-	mA	
15	V_{LL} current	TP	I_{LLPW}	-	0.05	-	mA	PW operating current $EN=0$ Current mode 3 ($CC[1:0]='11'$) 4-channel active Bipolar 3-level 2-cycle P1/N1-drive $f=5MHz$, $PRT=200\mu s$ $V_{PP1}/V_{NN1}=+/-60V$ $V_{PP2}/V_{NN2}=+/-60V$
		LVDS CLK		-	0.15	-	mA	
		CMOS CLK		-	0.1	-	mA	
16	V_{DD} current	TP	I_{DDPW}	-	6.5	-	mA	
		LVDS CLK		-	22	-	mA	
		CMOS CLK		-	20	-	mA	
17	V_{SS} current		I_{SSPW}	-	5.5	-	mA	
18	V_{PP1} current		I_{PP1PW}	-	2.2	-	mA	
19	V_{NN1} current		I_{NN1PW}	-	2.4	-	mA	
20	V_{PP2} current		I_{PP2PW}	-	0.16	-	mA	
21	V_{NN2} current		I_{NN2PW}	-	0.16	-	mA	

Table 5 Operating Supply Currents (continued)

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
22	V _{LL} current	TP	I _{LLCW3}	-	0.18	-	mA	CW operating current-1 EN=0 Current mode 3 (CC[1:0]='11') 4-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz V _{PP1} /V _{NN1} =+/-5V V _{PP2} /V _{NN2} =+/-5V
		LVDS CLK		-	0.26	-	mA	
		CMOS CLK		-	0.21	-	mA	
23	V _{DD} current	TP	I _{DDCW3}	-	20	-	mA	
		LVDS CLK		-	35	-	mA	
		CMOS CLK		-	33	-	mA	
24	V _{SS} current		I _{SSCW3}	-	15	-	mA	
25	V _{PP1} current		I _{PP1CW3}	-	0.16	-	mA	
26	V _{NN1} current		I _{NN1CW3}	-	0.16	-	mA	
27	V _{PP2} current		I _{PP2CW3}	-	84	-	mA	
28	V _{NN2} current		I _{NN2CW3}	-	86	-	mA	
29	V _{LL} current	TP	I _{LLCW2}	-	0.27	-	mA	CW operating current-2 EN=0 Current mode 2 (CC[1:0]='10') 4-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz V _{PP1} /V _{NN1} =+/-5V V _{PP2} /V _{NN2} =+/-5V
		LVDS CLK		-	0.3	-	mA	
		CMOS CLK		-	0.26	-	mA	
30	V _{DD} current	TP	I _{DDCW2}	-	19	-	mA	
		LVDS CLK		-	35	-	mA	
		CMOS CLK		-	33	-	mA	
31	V _{SS} current		I _{SSCW2}	-	13	-	mA	
32	V _{PP1} current		I _{PP1CW2}	-	0.16	-	mA	
33	V _{NN1} current		I _{NN1CW2}	-	0.16	-	mA	
34	V _{PP2} current		I _{PP2CW2}	-	80	-	mA	
35	V _{NN2} current		I _{NN2CW2}	-	83	-	mA	
36	V _{LL} current	TP	I _{LLCW1}	-	0.22	-	mA	CW operating current-3 EN=0 Current mode 1 (CC[1:0]='01') 4-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz V _{PP1} /V _{NN1} =+/-5V V _{PP2} /V _{NN2} =+/-5V
		LVDS CLK		-	0.30	-	mA	
		CMOS CLK		-	0.26	-	mA	
37	V _{DD} current	TP	I _{DDCW1}	-	15	-	mA	
		LVDS CLK		-	31	-	mA	
		CMOS CLK		-	29	-	mA	
38	V _{SS} current		I _{SSCW1}	-	10	-	mA	
39	V _{PP1} current		I _{PP1CW1}	-	0.16	-	mA	
40	V _{NN1} current		I _{NN1CW1}	-	0.16	-	mA	
41	V _{PP2} current		I _{PP2CW1}	-	77	-	mA	
42	V _{NN2} current		I _{NN2CW1}	-	80	-	mA	
43	V _{LL} current	TP	I _{LLCW0}	-	0.31	-	mA	CW operating current-4 EN=0 Current mode 0 (CC[1:0]='00') 4-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz V _{PP1} /V _{NN1} =+/-5V V _{PP2} /V _{NN2} =+/-5V
		LVDS CLK		-	0.35	-	mA	
		CMOS CLK		-	0.31	-	mA	
44	V _{DD} current	TP	I _{DDCW0}	-	12	-	mA	
		LVDS CLK		-	28	-	mA	
		CMOS CLK		-	26	-	mA	
45	V _{SS} current		I _{SSCW0}	-	7.9	-	mA	
46	V _{PP1} current		I _{PP1CW0}	-	0.16	-	mA	
47	V _{NN1} current		I _{NN1CW0}	-	0.16	-	mA	
48	V _{PP2} current		I _{PP2CW0}	-	67	-	mA	
49	V _{NN2} current		I _{NN2CW0}	-	70	-	mA	

4.2 Static Characteristics

Table 6 Static Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	HV _{OUTX} output voltage range	HV _{OUTX}	-100	-	+100	V	
2	HV _{OUTX} high-side peak current	I _{OH}	-	2.0	-	A	P1 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V
			-	2.0	-	A	P2 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V Current mode 3 (CC[1:0]='11')
			-	1.5	-	A	P2 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V Current mode 2 (CC[1:0]='10')
			-	1.0	-	A	P2 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V Current mode 1 (CC[1:0]='01')
			-	0.5	-	A	P2 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V Current mode 0 (CC[1:0]='00')
			-	1.0	-	A	N3 active, V _{PP1} /V _{NN1} =+/-80V, V _{PP2} /V _{NN2} =+/-20V, Current mode 3
3	HV _{OUTX} high-side GND clamp peak current	I _{OHCL}	-	2.0	-	A	N4 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V
4	HV _{OUTX} low-side peak current	I _{OL}	-	2.0	-	A	N1 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V
			-	2.0	-	A	N2 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V Current mode 3 (CC[1:0]='11')
			-	1.5	-	A	N2 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V Current mode 2 (CC[1:0]='10')
			-	1.0	-	A	N2 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V Current mode 1 (CC[1:0]='01')
			-	0.5	-	A	N2 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V Current mode 0 (CC[1:0]='00')
			-	1.0	-	A	P3 active, V _{PP1} /V _{NN1} =+/-80V, V _{PP2} /V _{NN2} =+/-20V, Current mode 3
5	HV _{OUTX} low-side GND clamp peak current	I _{OLCL}	-	2.0	-	A	P4 active, V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-60V
6	HV _{OUTX} high-side on-resistance	R _{ONH}	-	11	-	Ω	P1 active, I _{OH} =100mA
			-	11	-	Ω	P2/N3 active, I _{OH} =100mA Current mode 3 (CC[1:0]='11')
			-	13	-	Ω	P2 active, I _{OH} =100mA Current mode 2 (CC[1:0]='10')
			-	19	-	Ω	P2 active, I _{OH} =100mA Current mode 1 (CC[1:0]='01')
			-	32	-	Ω	P2 active, I _{OH} =100mA Current mode 0 (CC[1:0]='00')
7	HV _{OUTX} high-side GND clamp on-resistance	R _{ONHCL}	-	10	-	Ω	N4 active, I _{OHCL} =100mA
8	HV _{OUTX} low-side on-resistance	R _{ONL}	-	10	-	Ω	N1 active, I _{OL} =100mA
			-	10	-	Ω	N2/P3 active, I _{OL} =100mA Current mode 3 (CC[1:0]='11')
			-	12	-	Ω	N2 active, I _{OL} =100mA Current mode 2 (CC[1:0]='10')
			-	18	-	Ω	N2 active, I _{OL} =100mA Current mode 1 (CC[1:0]='01')
			-	30	-	Ω	N2 active, I _{OL} =100mA Current mode 0 (CC[1:0]='00')
9	HV _{OUTX} low-side GND clamp on-resistance	R _{ONLCL}	-	11	-	Ω	P4 active, I _{OLCL} =100mA
10	HV _{OUTX} off-capacitance	CHV _{OFF}	-	40	-	pF	TX _{OUTX} =HiZ, TRSW=off

4.3 Dynamic Characteristics

Table 7 Dynamic Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$, $T_A=25^{\circ}C$, $TR[1:0]=CKDL[1:0]='00'$, $CC[1:0]='11'$,
CLK=CLKB=100MHz/0(CLKEN=0/1), HV_{OUT} load=220pF//200Ω, LV_{OUT} load=47pF//200Ω, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions			
				Min	Typ	Max					
1	Output frequency		f _{OUT}	-	20	-	MHz				
2	Output rise propagation delay	TP mode	t _{dr}	-	31	-	ns	See Fig.5			
		CLK mode		-	39	-	ns				
3	Output fall propagation delay	TP mode	t _{df}	-	31	-	ns				
		CLK mode		-	39	-	ns				
4	Output rise propagation delay clamp	TP mode	t _{drCL}	-	31	-	ns				
		CLK mode		-	39	-	ns				
5	Output fall propagation delay clamp	TP mode	t _{dfCL}	-	31	-	ns				
		CLK mode		-	39	-	ns				
6	Propagation delay matching		Δt _d	-	±1	±3	ns				
7	Output rise time		t _r	-	16	-	ns	P1 active	See Fig.5		
				-	16	-	ns	P2 active, CC[1:0]='11'			
				-	19	-	ns	P2 active, CC[1:0]='10'			
				-	27	-	ns	P2 active, CC[1:0]='01'			
				-	52	-	ns	P2 active, CC[1:0]='00'			
			t _{rCL}	-	10	-	ns	P4 active			
8	Output fall time		t _f	-	16	-	ns	N1 active			
				-	16	-	ns	N2 active, CC[1:0]='11'			
				-	19	-	ns	N2 active, CC[1:0]='10'			
				-	27	-	ns	N2 active, CC[1:0]='01'			
				-	52	-	ns	N2 active, CC[1:0]='00'			
			t _{rCL}	-	10	-	ns	N4 active			
9	2 nd harmonic distortion		HD2	-	-40	-	dBc	Bipolar, 2-cyc, f _{OUT} =5MHz			
10	Pulse cancellation		HDPC	-	-40	-	dBc	See Fig.6			
			HDPC2	-	-40	-	dBc				
11	RMS output jitter		t _j	-	10	-	ps	Bipolar CW, f _{OUT} =5MHz V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-5V			
12	Crosstalk between channels		X _{TLK}	-	-70	-	dB	f _{OUT} =5MHz, 10V _{p-p} , HV _{OUT} load=50Ω			
13	Output enable time	TP	t _{EN}	-	28	-	ns	See Fig.7			
		LVDS CLK		-	600	-	ns				
		CMOS CLK		-	600	-	ns				
14	Output disable time		t _{DS}	-	36	-	ns				
15	Clock mode enable time		t _{CLKEN}	-	600	-	ns				
16	Clock mode disable time		t _{CLKDS}	-	36	-	ns				

4.4 Integrated Peripheral Circuits Characteristics

T/R Switch

Table 8 T/R Switch Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	LV _{OUTX} output voltage range	LV _{OUTX}	-0.85	-	+0.85	V	
2	TRSW on-resistance	R _{ONTR}	-	10	-	Ω	HV _{OUTX} =100mV, LV _{OUTX} =0V
3	TRSW on-capacitance	C _{ONTR}	-	15	-	pF	
4	TRSW off-resistance on HV _{OUTX}	R _{OFFTRHV}	1	-	-	MΩ	
5	TRSW off-resistance on LV _{OUTX}	R _{OFFTRLV}	8	10	12	kΩ	
6	Spike voltage on HV _{OUTX} and LV _{OUTX}	V _{TRN}	-	-	50	mV _{PP}	50pF//200Ω load on HV _{OUTX} 20pF//200Ω load on LV _{OUTX}
7	TRSW turn-on time	t _{dTRON}	-	400	-	ns	Logic input-to-ready for Rx signal See Fig.8
			-	500	-	ns	
			-	600	-	ns	
			-	700	-	ns	
8	TRSW turn-off time	t _{dTROFF}	-	50	100	ns	See Fig.8
9	Tx setup time	t _{TXSU}	100	-	-	ns	INx_[2:0]='100'(GND) for at least 100ns before Tx burst. See Fig.8

Analog Switch

Table 9 Analog Switch Characteristics

$T_A=25^{\circ}C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	ASW on-resistance	R _{ONASW}	-	250	-	Ω	

HV Blocking Diode

Table 10 Output HV Blocking Diode Characteristics

$T_A=25^{\circ}C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V _{FHVD}	-	1.0	-	V	I _F =100mA
			-	1.2	-	V	I _F =200mA
2	Reverse voltage	V _{RHVD}	200	-	-	V	I _R =1μA

LV Noise-cut Diode

Table 11 Output LV Noise-cut Diode Characteristics

$T_A=25^{\circ}C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V _{FLVD}	-	1.1	-	V	I _F =100mA
			-	1.25	-	V	I _F =200mA

Thermal Protection

Table 12 Thermal Protection Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, $V_{LL}=2.5V$, $I_{THP}=1mA$
4	THP temperature threshold	T_{THP}	100	110	120	$^{\circ}C$	
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	$^{\circ}C$	

5. Switching Time Diagram

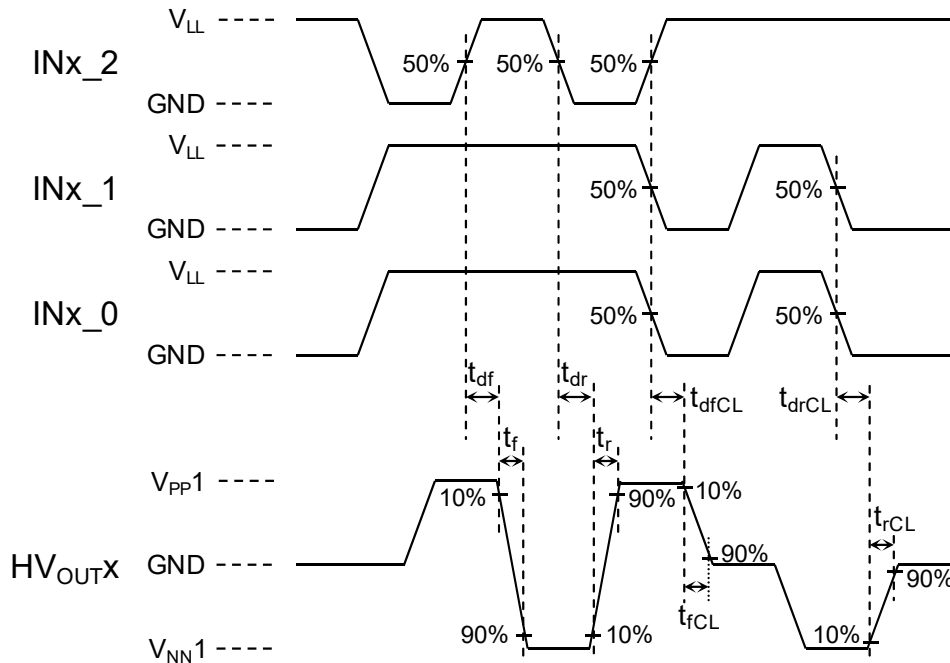
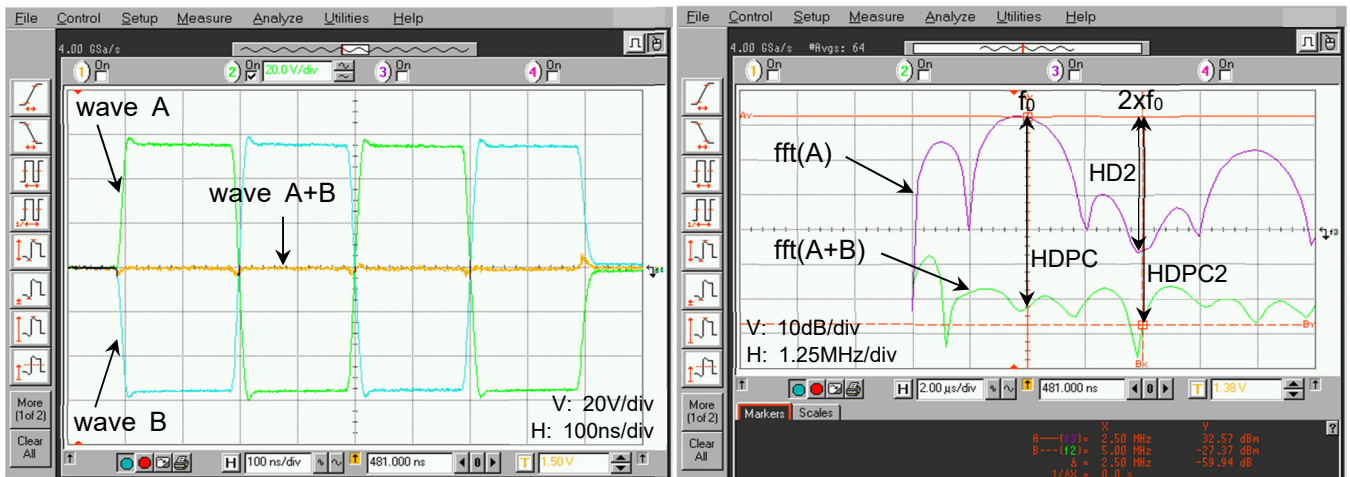


Fig.5 Propagation delay and Output rise/fall time



Example waveforms: $V_{PP}/V_{NN} = \pm 60V$, $f_0 = 2.5MHz$, 2-cycle, HV_{OUT} load = $220pF // 200\Omega$

Fig.6 2nd harmonic distortion and Pulse cancellation

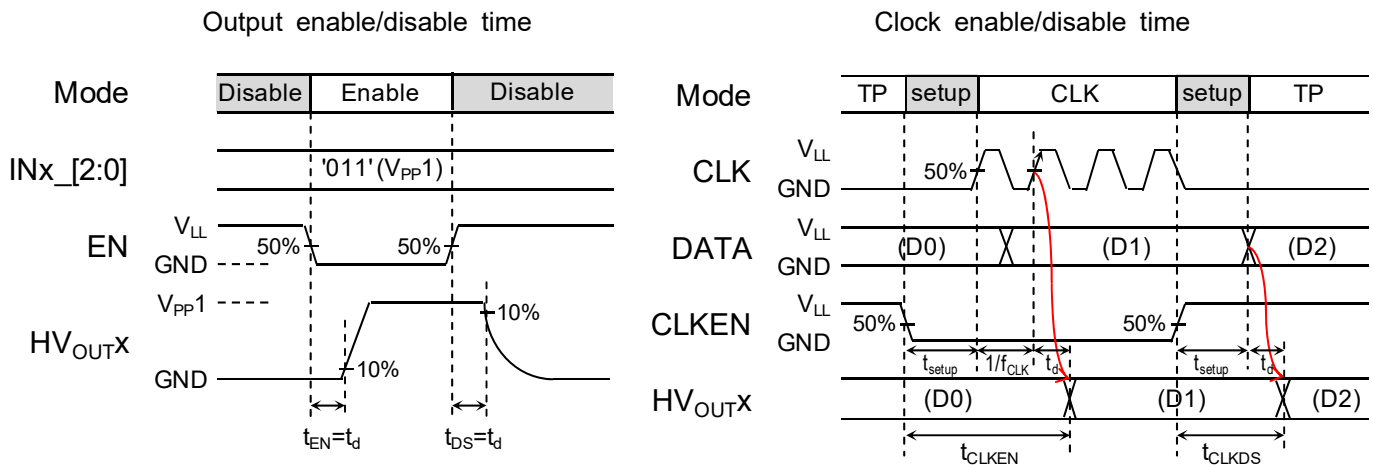


Fig.7 Output enable/disable and Clock enable/disable time

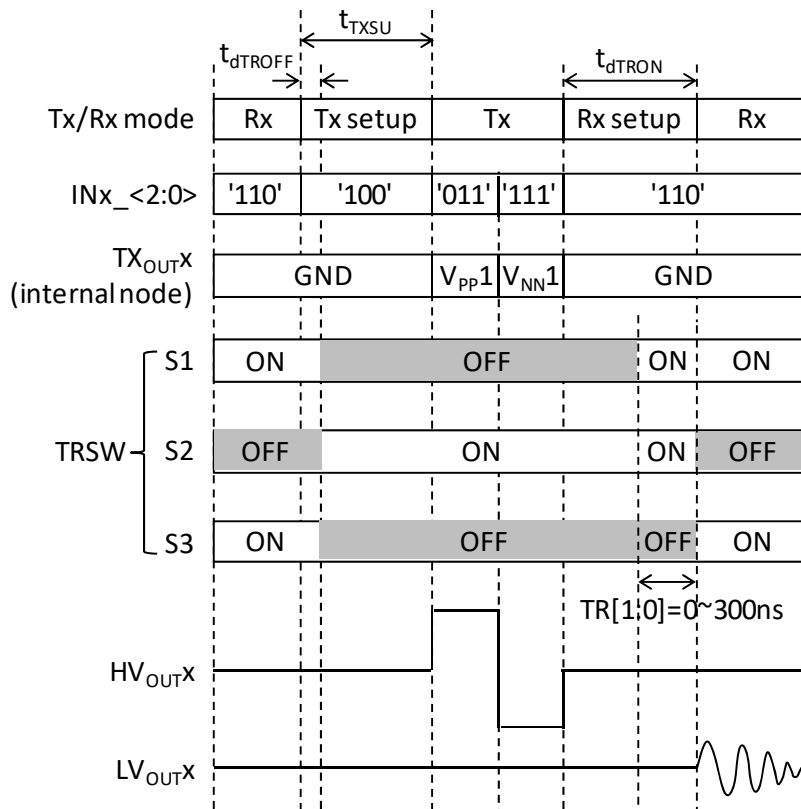


Fig.8 T/R Switch turn-on/off time

6. Truth Table and Mode Control tables

Table 13 Truth table

Logic Inputs				Internal MOSFET state												Output state	
EN	INx_2	INx_1	INx_0	P1 +HV1	N1 -HV1	P2 +HV2	N2 -HV2	P3 -HV2	N3 +HV2	P4 GND	N4 GND	ASW GND	TRSW			TX _{OUTX} (internal node)	LV _{OUTX}
0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	HiZ	10k Ω
0	0	0	1	OFF	OFF	ON	OFF	OFF	ON*	OFF	OFF	OFF	OFF	ON	OFF	+HV2	10k Ω
0	0	1	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	HiZ	HV _{OUTX}
0	0	1	1	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	+HV1	10k Ω
0	1	0	0	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	GND	10k Ω
0	1	0	1	OFF	OFF	OFF	ON	ON*	OFF	OFF	OFF	OFF	OFF	ON	OFF	-HV2	10k Ω
0	1	1	0	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	GND	HV _{OUTX}
0	1	1	1	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	-HV1	10k Ω
1	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	HiZ	10k Ω

Note: V_{PP1}/ V_{NN1}=+/-HV1, V_{PP2}/ V_{NN2}=+/-HV2, x=1~4

Note: When the current mode is other than 3 (CC[1:0]≠'11'), both P3 and N3 are always in off-state.

Table 14 P2/N2 drive current mode

Current Mode	CC1	CC0	I _{out} [A]	
			P2	N2
0	0	0	0.5	0.5
1	0	1	1	1
2	1	0	1.5	1.5
3	1	1	2	2

Note:

Recommended mode is as follows:

- Current mode 2 or 3 for high amplitude short cycle pulse waveforms, or for driving heavy load
- Current mode 0 or 1 for low amplitude long pulse train waveforms (e.g. CW), or for driving light load

Table 15 TRSW S1-S2 turn-on overlap time control mode

TRSW Control Mode	TR1	TR0	S1-S2 ON overlap time [ns]
0	0	0	0 (default)
1	0	1	100
2	1	0	200
3	1	1	300

Note: Detailed switching time diagram is shown in Fig.8.

Table 16 Clock edge timing control mode

CLK Edge Control Mode	CKDL1	CKDL0	CLK edge [ns]
0	0	0	0 (default)
1	0	1	0.5
2	1	0	1
3	1	1	1.5

Note: Detailed switching time diagram is shown in Fig.3.

7. Pin Configuration

Table 17 Pin Configuration

Pin#	Pin Name	I/O	Function
1	IN1_0	I	The least significant bit of logic input of channel 1
2	IN1_1	I	The 2nd significant bit of logic input of channel 1
3	IN1_2	I	The most significant bit of logic input of channel 1
4	IN2_0	I	The least significant bit of logic input of channel 2
5	IN2_1	I	The 2nd significant bit of logic input of channel 2
6	IN2_2	I	The most significant bit of logic input of channel 2
7	V _{DD}	-	Positive low voltage power supply (+5V)
8	CLK	I	Positive clock input (up to 200MHz)
9	CLKB	I	Negative clock Input (up to 200MHz)
10	GND	-	Drive power ground (0V)
11	IN3_0	I	The least significant bit of logic input of channel 3
12	IN3_1	I	The 2nd significant bit of logic input of channel 3
13	IN3_2	I	The most significant bit of logic input of channel 3
14	IN4_0	I	The least significant bit of logic input of channel 4
15	IN4_1	I	The 2nd significant bit of logic input of channel 4
16	IN4_2	I	The most significant bit of logic input of channel 4
17	GND	-	Drive power ground (0V)
18	LV _{OUT4}	O	Low voltage output of channel 4
19	V _{FN3}	-	Built-in power supply for N-MOS (N3) gate drive
20	V _{PP1}	-	Positive high voltage power supply 1 (0 to +100V)
21	V _{FP1}	-	Built-in power supply for P-MOS (P1) gate drive
22	V _{FP2}	-	Built-in power supply for P-MOS (P2) gate drive
23	V _{PP2}	-	Positive high voltage power supply 2 (0 to +100V)
24	HV _{OUT4}	O	High voltage output of channel 4
25	GND	-	Drive power ground (0V)
26	HV _{OUT3}	O	High voltage output of channel 3
27	V _{NN2}	-	Negative high voltage power supply 2 (0 to -100V)
28	V _{FN2}	-	Built-in power supply for N-MOS (N2) gate drive
29	V _{FN1}	-	Built-in power supply for N-MOS (N1) gate drive
30	V _{NN1}	-	Negative high voltage power supply 1 (0 to -100V)
31	V _{FP3}	-	Built-in power supply for P-MOS (P3) gate drive
32	LV _{OUT3}	O	Low voltage output of channel 3

Table 17 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
33	LVDSTM	-	Control of LVDS termination between CLK and CLKB, Hi=embedded 100 Ω , Low=open (50k Ω internal pull-down resistor)
34	GND	-	Drive power ground (0V)
35	GND	-	Drive power ground (0V)
36	CLKIF	I	Control of clock interface, Hi=differential CMOS, Low=LVDS (50k Ω internal pull-up resistor)
37	CLKEN	I	Control of clock enable, Hi=clock disable, Low=clock enable (50k Ω internal pull-up resistor)
38	EN	I	Control of drive output enable, Hi=off, Low=on (50k Ω internal pull-up resistor)
39	V _{SS}	-	Negative low voltage power supply (-5V)
40	V _{LL}	-	Positive voltage supply of logic input interface (1.8 to 5V)
41	THP	O	Thermal protection output flag, open N-MOS drain
42	GND	-	Drive power ground (0V)
43	TR0	I	Lower bit of control of T/R switch S1 and S2 turn-on overlap time (50k Ω internal pull-down resistor)
44	TR1	I	Upper bit of control of T/R switch S1 and S2 turn-on overlap time (50k Ω internal pull-down resistor)
45	CKDL0	I	Lower bit of control of clock edge timing (50k Ω internal pull-down resistor)
46	CKDL1	I	Upper bit of control of clock edge timing (50k Ω internal pull-down resistor)
47	CC0	I	Lower bit of control of P2/N2 drive current (50k Ω internal pull-up resistor)
48	CC1	I	Upper bit of control of P2/N2 drive current (50k Ω internal pull-up resistor)
49	LV _{OUT2}	O	Low voltage output of channel 2
50	V _{FP3}	-	Built-in power supply for P-MOS (P3) gate drive
51	V _{NN1}	-	Negative high voltage power supply 1 (0 to -100V)
52	V _{FN1}	-	Built-in power supply for N-MOS (N1) gate drive
53	V _{FN2}	-	Built-in power supply for N-MOS (N2) gate drive
54	V _{NN2}	-	Negative high voltage power supply 2 (0 to -100V)
55	HV _{OUT2}	O	High voltage output of channel 2
56	GND	-	Drive power ground (0V)
57	HV _{OUT1}	O	High voltage output of channel 1
58	V _{PP2}	-	Positive high voltage power supply 2 (0 to +100V)
59	V _{FP2}	-	Built-in power supply for P-MOS (P2) gate drive
60	V _{FP1}	-	Built-in power supply for P-MOS (P1) gate drive
61	V _{PP1}	-	Positive high voltage power supply 1 (0 to +100V)
62	V _{FN3}	-	Built-in power supply for N-MOS (N3) gate drive
63	LV _{OUT1}	O	Low voltage output of channel 1
64	GND	-	Drive power ground (0V)

■ Package

Table 18 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-64(0909)B	QN064-B-P-SD	QFN9x9-B-T-SD	QN064-B-M-S2	QN064-B-L-SD	QN064-B-K-SD

■ Storage, Mounting

1. Storage conditions

- 1.1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.
- 1.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering. It is necessary to check the package surface temperature (resin) before setting the temperature profile.

Fig. 9 shows the resistance to soldering heat condition for package (Reflow method).

Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

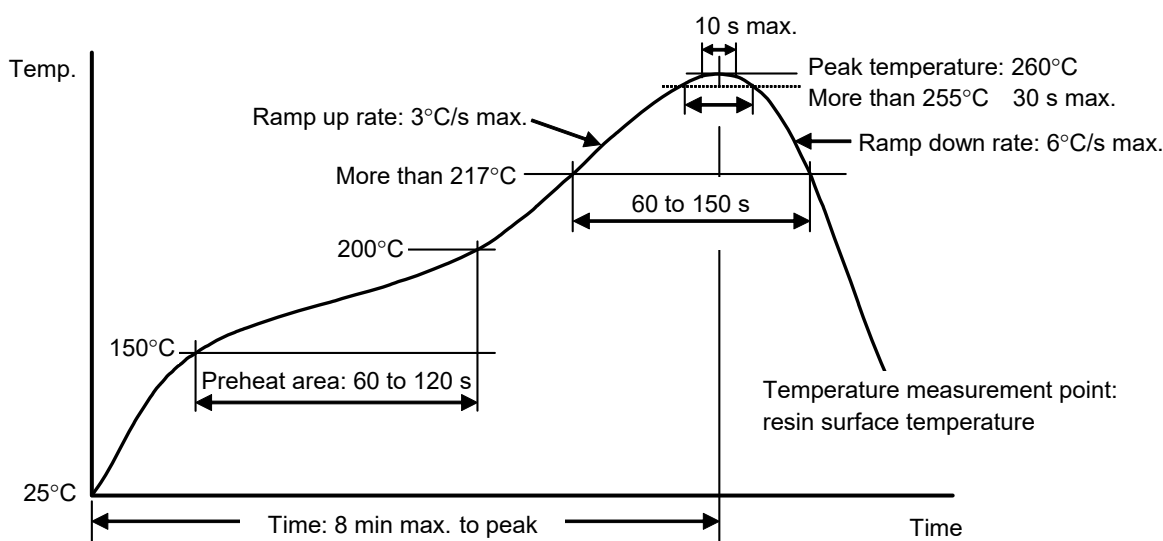


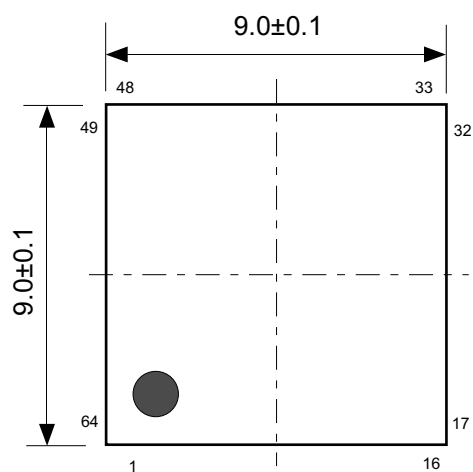
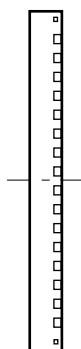
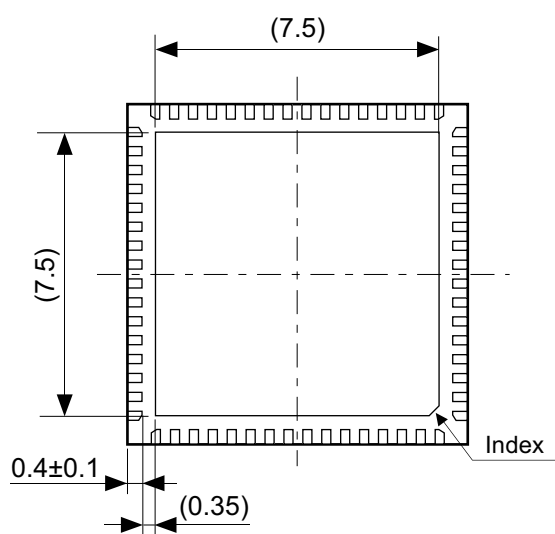
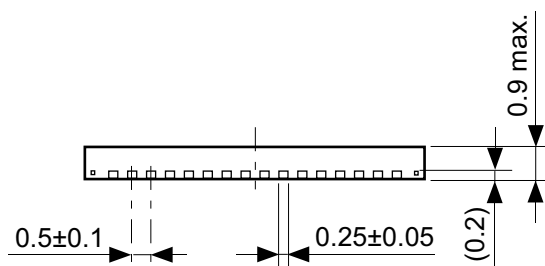
Fig.9 Resistance to Soldering Heat Condition for Package (Reflow Method)

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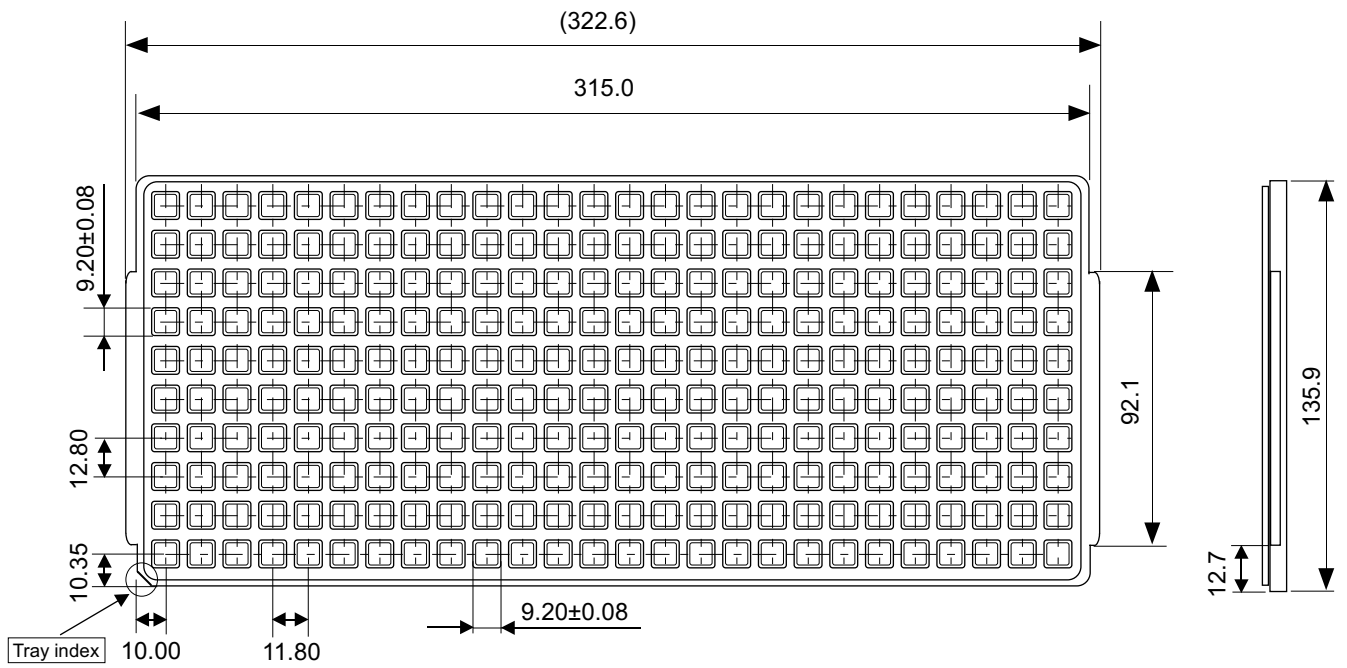
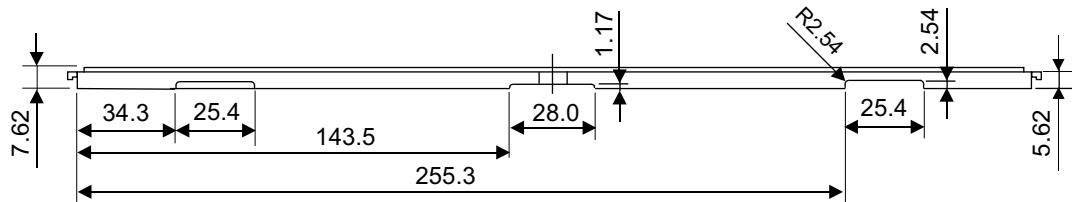
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 1. 2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.
 1. 3 Those who deal with products should be grounded through a large series impedance around 100k Ω to 1M Ω .
 1. 4 Prevent friction with other materials made with high polymer.
 1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.
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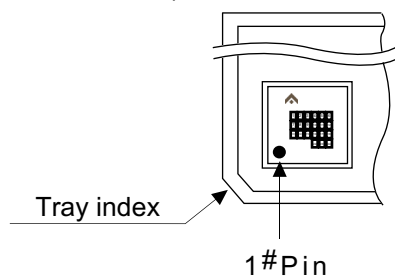


No. QN064-B-P-SD-2.0

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UNIT	mm
ABLIC Inc.	

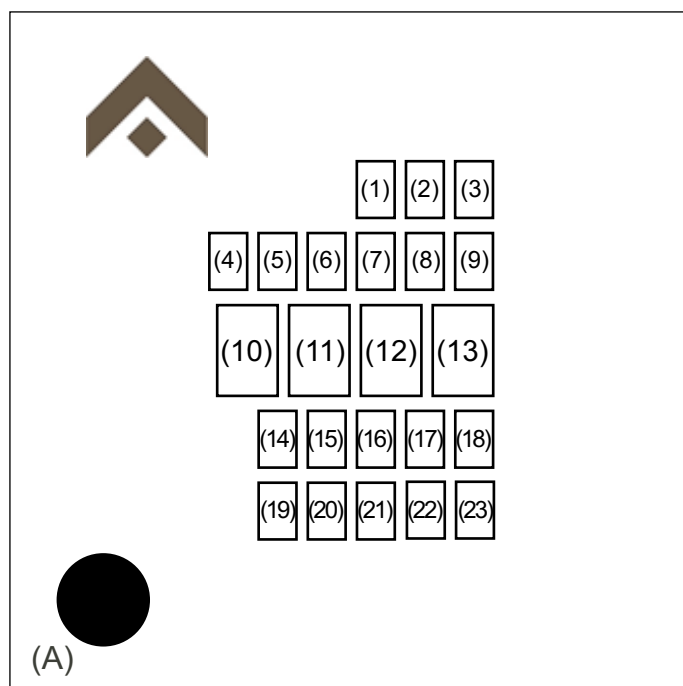


(Direction of IC in tray)



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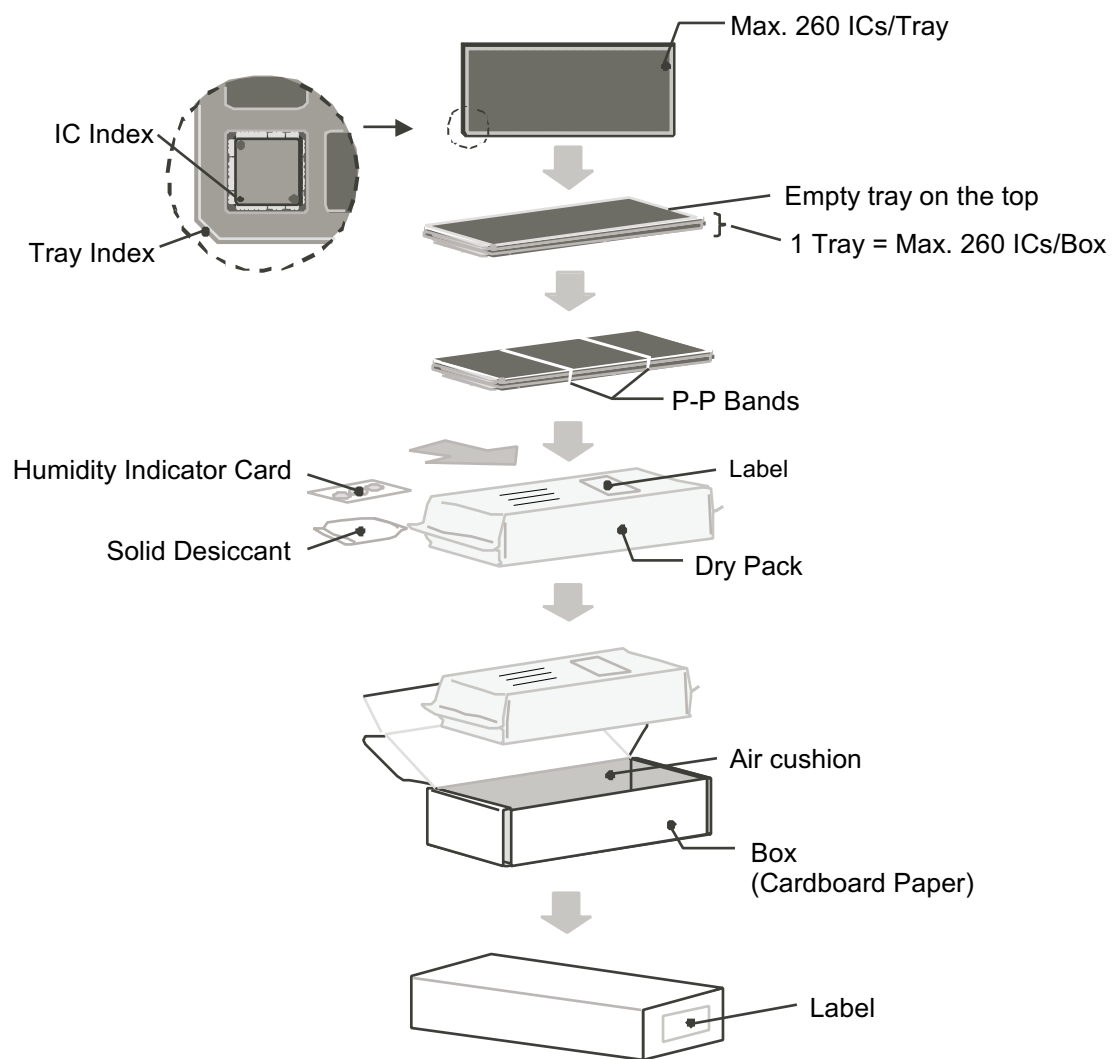
TITLE	QFN9x9-B-Tray		
No.	QFN9x9-B-T-SD-1.0		
ANGLE		QTY.	260
UNIT	mm		
ABLIC Inc.			



- (1) : Year of assembly
 (2) : Month of assembly
 (3) : Week of assembly
 (4) to (13) : Product code
 (14) to (23) : Quality control code
 (A) : 1-pin mark

No. QN064-B-M-S2-1.0

TITLE	QFN64-B-Markings (S-UM5543 / S-UM5584)		
No.	QN064-B-M-S2-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



No. QN064-B-K-SD-2.0

TITLE	QFN64-B -Packing Procedure
No.	QN064-B-K-SD-2.0
ANGLE	
UNIT	
ABLIC Inc.	

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10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
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14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

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