L9988

Datasheet

Automotive 12 V Li-Ion battery management system solution

Product status link

L9988

Product label

Features

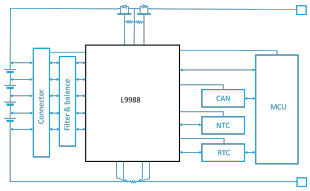
- AEC-Q100 grade 1 qualified
- Full ISO26262 compliant, ASIL-D systems ready
- [4 V÷28 V] Power supply operating range
- Voltage measurement:
  - 15-bit sigma delta ADC with programmable filter time with cutoff down to 30 Hz
  - Measures 4 single cell voltage, with over/under voltage detection and balance timeout protection
  - Measures stack voltage, with over/under voltage detection and plausibility check vs. sum of cells
  - Full 0÷5 V measurement range, with total error < ±2 mV in the [1.8 V÷4.5 V] range with -40°C ≤ T_J ≤ +105°C
- Current measurement:
  - 20-bit current sense ADC for battery current measurement (range ± 1500 A), with overcurrent protection
  - Total error < 0.23% for ±200 A, considering 100 µΩ R_{SHUNT} typical value (no spread contribution)
  - 20-bit Coulomb counting ADC for SoC estimation
  - Total error < 3.9% for ±100 mA in STANDBY MODE, considering 100 µΩ R_{SHUNT} typical value (no spread contribution)
  - Continuously short-circuit detection
- Passive cell balancing: max 200 mA, supporting time-continuous and PWM modes, with synchronized odd-even channels balance
- 4 analog inputs measure pack temperature via NTCs, with OT/UT detection; 2 GPIOs are available
- Ultralow power consumption of 190 µA in STANDBY MODE and 50 µA in SLEEP MODE
- Integrated PMIC with configurable regulators:
  - Boost preregulator to support system full operation at low battery level
  - V_{CORE} regulator for MCU supply [1.125 V÷5 V]
  - V_{CC} regulator for MCU ADCs supply [3.3 V/5 V]
  - Fixed 5 V regulator for external CAN power supply
  - V_{VSTBY} regulator for external RTC supply [3.3 V/5 V]
  - Fixed 5 V V_{VTREF} regulator to bias external NTCs
- Integrated dual high-side V_{GS} predriver:
  - Drive 2 independent groups back-to-back MOSFETs.
  - Switch OFF MOSFETs in case of SC during NORMAL and STANDBY MODE.
- Standard 4-wire, 4 MHz, 40-bit SPI interface for device configuration and diagnostics data read-out
- Watchdogs: Configurable double watchdog (Q&A WD and time windowed WD)
- Real-time clock: selectable timer from 1 s to 180 days
- Configurable wake-up monitoring OV/UV/OT/OVC/SC
- Hardware wake-up module: IGN level triggered and WAKE edge triggered

- Embedded NVM for configuration parameters storage and runtime configuration integrity check
- Hot plug robustness

Application

- 12 V vehicle starter and backup battery

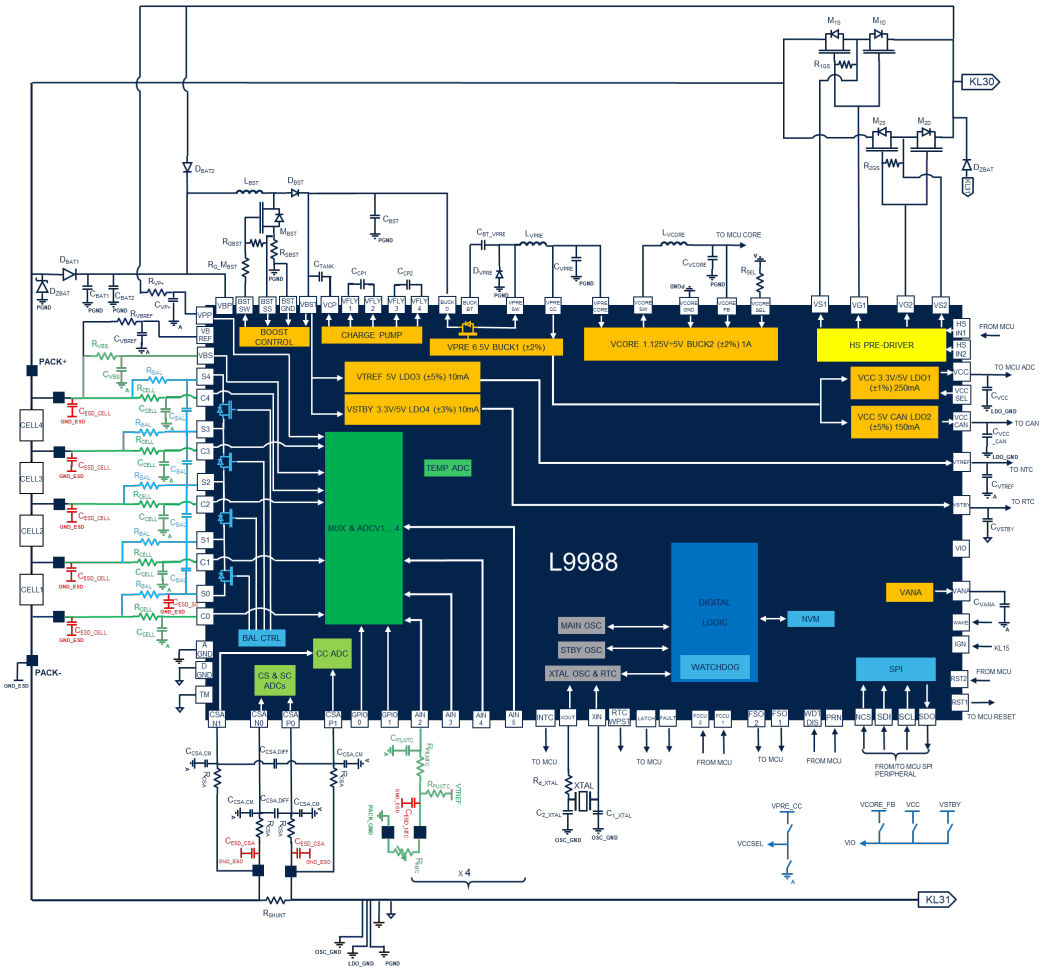
Figure 1. Typical application circuit



The L9988 is a multicell battery stack monitor that measures up to four series-connected battery cells with a total measurement error of less than 2 mV. The IC has one battery stack current measurement channel, which can support synchronous current and voltage measurement, performing Coulomb counting for SoC estimation. The L9988 includes both timed and PWM-based odd-even passive balancing for each cell. Four analog inputs for external NTC thermistor connection and two general-purpose I/O are available. The L9988 can be powered directly from the battery stack. Programmable voltage regulators can supply all the system components, including the MCU, CAN and NTCs. The IC also integrates a dual predriver for driving two independent groups of circuit breaker (CB) back-to-back MOSFETs to manage battery pack connection. IC configuration and information exchange with the MCU is performed via 4 MHz, 40-bit SPI. Relevant configurations stored in the internal NVM allow quick wake-up without reprogramming the IC. The L9988 has dedicated alert output pins to indicate fault state that makes the system more robust. A comprehensive set of safety mechanisms has been implemented to achieve ASIL-D targets.

1 Block diagram

Figure 2. **Block diagram**



2 Pin description

Figure 3. **Pinout**

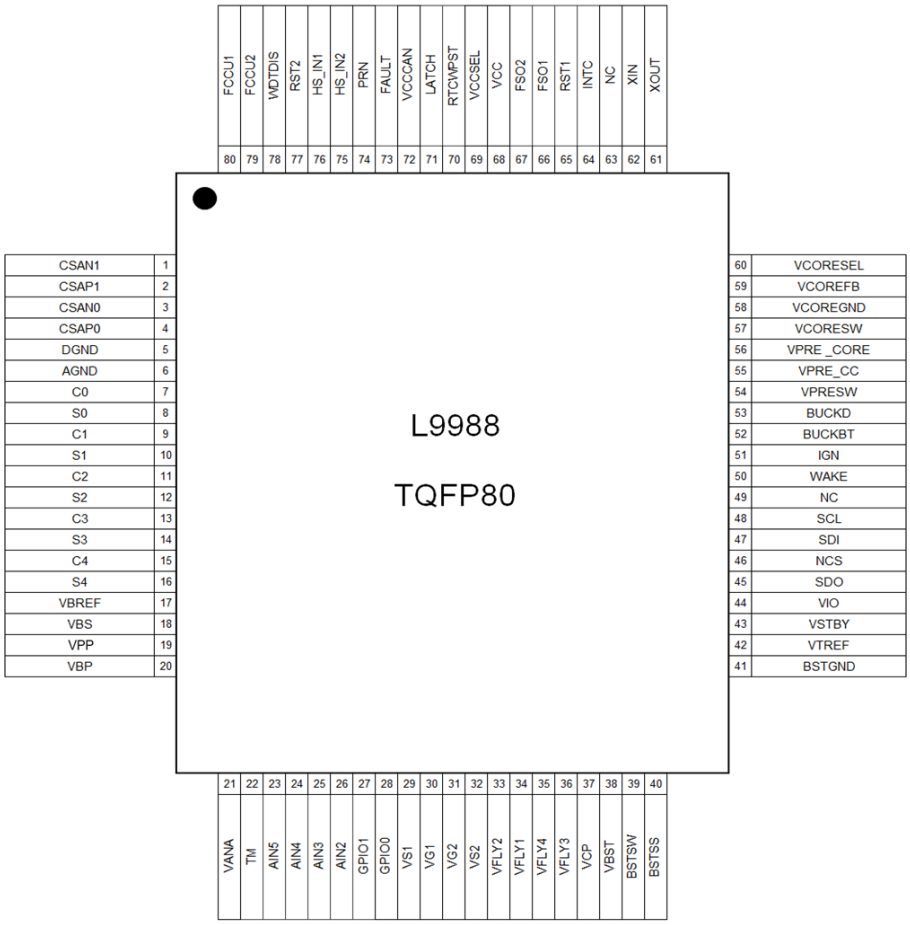


Table 1. **Pin description**

Pin #	Pin name	Description	Pin type (1)	Class (2)
1	CSAN1	Current sense amplifier negative differential input	A	L
2	CSAP1	Current sense amplifier positive differential input	A	L
3	CSAN0	Current sense amplifier negative differential input	A	L
4	CSAP0	Current sense amplifier positive differential input	A	L
5	DGND	Digital ground	GND	-
6	AGND	Analog ground	GND	-
7	C0	Cell sensing differential input	A	G
8	S0	Cell balancing line	A	G
9	C1	Cell sensing differential input	A	G
10	S1	Cell balancing line	A	G
11	C2	Cell sensing differential input	A	G
12	S2	Cell balancing line	A	G

Pin #	Pin name	Description	Pin type (1)	Class (2)
13	C3	Cell sensing differential input	A	G
14	S3	Cell balancing line	A	G
15	C4	Cell sensing differential input	A	G
16	S4	Cell balancing line	A	G
17	VBREF	Battery supply input for internal ADC reference	A	G
18	VBS	Battery sensing input	A	G
19	VPP	KL30 sensing input	A	G
20	VBP	Protected battery supply input	P	G
21	VANA	3.3 V internal analog LDO output voltage	P	L
22	TM	Test mode pin. Shorted to DGND ground in application	TM	-
23	AIN5	NTC sensing input	A	G
24	AIN4	NTC sensing input	A	G
25	AIN3	NTC sensing input	A	G
26	AIN2	NTC sensing input	A	G
27	GPIO1	General-purpose I/O	A/DI/DO	G
28	GPIO0	General-purpose I/O	A/DI/DO	G
29	VS1	MOS 1S-1D source	A	L
30	VG1	MOS 1S-1D gate	A	L
31	VG2	MOS 2S-2D gate	A	L
32	VS2	MOS 2S-2D source	A	L
33	VFLY2	Negative terminal of charge pump stage 1 flying capacitor	A	L
34	VFLY1	Positive terminal of charge pump stage 1 flying capacitor	A	L
35	VFLY4	Negative terminal of charge pump stage 2 flying capacitor	A	L
36	VFLY3	Positive terminal of charge pump stage 2 flying capacitor	A	L
37	VCP	charge pump output voltage	P	L
38	VBST	Boost output voltage	P	L
39	BSTSW	Boost switching terminal	A	L
40	BSTSS	Boost sensing terminal	A	L
41	BSTGND	Boost ground	GND	-
42	VTREF	5 V LDO3 output voltage Power supply for NTCs	P	L
43	VSTBY	3.3 V/5 V LDO4 output voltage. Power supply for external RTC (real-time clock)	P	L
44	VIO	Digital output buffers power supply	P	L
45	SDO	SPI serial data out	DO	L
46	NCS	SPI chip select	DI	L
47	SDI	SPI serial data in	DI	L
48	SCL	SPI serial clock	DI	L
49	NC	Not connect	NC	-
50	WAKE	Edge-triggered wake-up input	DI	G

Pin #	Pin name	Description	Pin type (1)	Class (2)
51	IGN	Level-triggered wake-up input (KL15)	DI	G
52	BUCKBT	Buck1 VPRE pre-regulator bootstrap pin	A	L
53	BUCKD	Buck1 VPRE pre-regulator input voltage	P	L
54	VPRESW	Buck1 VPRE pre-regulator switching node	A	L
55	VPRE_CC	Buck1 VPRE pre-regulator output voltage. Power supply for LDO1 VCC and LDO2 VCC CAN	P	L
56	VPRE_CORE	Buck1 VPRE pre-regulator output voltage. Power supply for Buck2 VCORE	P	L
57	VCORESW	Buck2 VCORE switching node	A	L
58	VCOREGND	Buck2 VCORE power ground	GND	-
59	VCOREFB	Buck2 VCORE feedback voltage. Since the buck does not require an external resistor divider, the VCOREFB pin voltage coincides with the regulated output voltage	P	L
60	VCORESEL	Buck2 VCORE output voltage selection pin	A	L
61	XOUT	Ext oscillator output	A	L
62	XIN	Ext oscillator input	A	L
63	NC	Not connect	NC	-
64	INTC	Interrupt pin	DO	L
65	RST1	Reset output. Reset MCU	DO	L
66	FSO1	Fail-safe output (active high)	DO	L
67	FSO2	Fail-safe output (active low)	DO	L
68	VCC	3.3 V/5 V LDO1 output voltage Power supply for MCU	P	L
69	VCC SEL	3.3 V/5 V LDO1 selection pin	DI	L
70	RTCWPST	RTC wake-up state	DO	L
71	LATCH	Latch interrupt output in case of short-circuit detection	DO	L
72	VCC CAN	5 V LDO2 output voltage Power supply for external CAN/LIN	P	L
73	FAULT	Fault interrupt output in case of OV/UV/OT etc. occur during voltage conversion routine, OVC/CC_WUP etc. occur during current conversion routine or the other detection described in detail in 4.12.1	DO	L
74	PRN	Watchdog pin	DI	L
75	HS_IN2	MOS 2S-2D command	DI	L
76	HS_IN1	MOS 1S-1D command	DI	L
77	RST2	Reset input. Reset device	DI	L
78	WDTDIS	Watchdog disable	DI	L
79	FCCU2	MCU Lock-step error detection	DI	L
80	FCCU1	MCU Lock-step error detection	DI	L
-	EP	Exposed pad. Connect to AGND	A	-

1. *Type: A = Analog, DI = Digital Input, DO = Digital Output, P = Power, GND=Ground, NC = Not Connect, TM = Test Mode*
2. *Class: G=Global, L=Local*

3 Product ratings

3.1 Operating range

Within the operating range, the part operates as specified and without parameter deviations. The device may not operate properly if maximum operating conditions are exceeded.

Once taken beyond the operative ratings and returned within, the part will recover with no damage or degradation, unless the AMRs are exceeded.

Additional supply voltage and temperature conditions are given separately at the beginning of each electrical specification table.

All voltages are related to the potential at substrate ground AGND, unless otherwise noted.

Table 2. Operating range

Symbol	Description	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Power supplies							
V_{VBP_SLEEP}	VBP: voltage range in SLEEP MODE	Global	vs. AGND SLEEP MODE	5.5 [*]	11.5	18.5	V
V_{VBP_STANDY}	VBP: voltage range in STANDBY MODE	Global	vs. AGND STANDBY MODE	5.5 [*]	11.5	18.5	V
V_{VBP_NORMAL}	VBP: voltage range in NORMAL MODE	Global	vs. AGND NORMAL MODE	5.5 [*] 4 [**] 7.2 [****]	11.5	27.5 [***]	V
V_{VBREF_SLEEP}	VBREF: voltage range in SLEEP MODE	Global	vs. AGND SLEEP MODE	6 [*]	12	19	V
$V_{VBREF_STANDBY}$	VBREF: voltage range in STANDBY MODE	Global	vs. AGND STANDBY MODE	6 [*]	12	19	V
V_{VBREF_NORMAL}	VBREF: voltage range in NORMAL MODE	Global	vs. AGND NORMAL MODE	6 [*] 4.5 [**]	12	28 [***]	V
[*]Self-discharge and maintain mode scenarios. Refer to Section 4.1.6.2. *[**]Crank and soft short-circuit scenarios. Refer to Section 4.1.6.4, Section 4.1.6.3* *[***]Jump start scenario.* *[****]When boost is disabled.* Considering V_{VBP} = MAX [(V_{VPP} - 0.5 V); (V_{VBS} – 0.5 V)], with 0.5 V = V_{DBAT1} = V_{DBAT2} , the maximum forward voltage of external diodes D_{BAT1}, D_{BAT2}							
V_{BSTSW}	BSTSW: voltage range	Local	vs. AGND	0		6	V
V_{BSTSS}	BSTSS: voltage range	Local	vs. AGND	0		0.31	V
$V_{VBST_BOOST_EN}$	VBST: voltage range with BOOST active	Local	vs. AGND		8.75 if Boost ACTIVED		V
$V_{VBST_BOOST_DIS}$	VBST: voltage range with BOOST not active	Local	vs. AGND	V_{VBP} – 0.5 if boost DISACTIVED [#]			
[#] Considering 0.5 V = V_{DBST}, the maximum forward voltage of external diode D_{BST}							
V_{VCP}	VCP: voltage range	Local	vs. AGND	V_{VBST} + 6		V_{VBST} + 16	V
V_{VFLY1}	VFLY1: voltage range	Local	vs. AGND	0		V_{VCP}	V
V_{VFLY2}	VFLY2: voltage range	Local	vs. AGND	0		V_{VCP}	V

Symbol	Description	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{VFLY3}	VFLY3: voltage range	Local	vs. AGND	0		V_{VCP}	V
V_{VFLY4}	VFLY4: voltage range	Local	vs. AGND	0		V_{VCP}	V
$V_{BUCKD_BOOST_EN}$	VBUCKD: voltage range with BOOST active	Local	vs. AGND		8.75 if boost ACTIVED		V
$V_{BUCKD_BOOST_DIS}$	VBUCKD: voltage range with BOOST not active	Local	vs. AGND	V_{VBP} – 0.5 if boost DISACTIVED [#]			
V_{BUCKBT}	VBUCKBT: voltage range	Local	vs. AGND		V_{VPRESW} + 3.3		V
V_{VPRESW}	VPRESW: voltage range	Local	vs. AGND	0		V_{BUCKD}	V
V_{VPRE}	VPRE_CC, VPRE_CORE: voltage range	Local	vs. AGND	6.3	6.5	6.7	V
The output pin of the VPRE regulator is split into the two pins VPRE_CC and VPRE_CORE to feed the VCORE regulator separately. In terms of voltages, we still have V_{VPRE_CC} = V_{VPRE_CORE} = V_{VPRE}. Therefore, the distinction between the two pins will be made only in the application field and in the block diagram							
$V_{VCORESW}$	VCORESW: voltage range	Local	vs. AGND	0		V_{VPRE}	V
$V_{VCOREFB}$	VCOREFB: voltage range	Local	vs. AGND		1.125, 1.2, 1.3, 1.5, 3.3, 5		V
$V_{VCORESEL}$	VCORESEL: voltage range	Local	vs. AGND	0		V_{VIO}	V
V_{VCC}	VCC: voltage range	Local	vs. AGND		3.3 / 5		V
V_{VCCCAN}	VCC CAN: voltage range	Local	vs. AGND		5		V
V_{VTREF}	VTREF: voltage range	Local	vs. AGND		5		V
V_{VSTBY}	VSTBY: voltage range	Local	vs. AGND		3.3 / 5		V
V_{VANA}	VANA: voltage range	Local	vs. AGND		3.45		V
V_{VIO}	VIO: voltage range	Local	vs. AGND	3.2	V_{VCC} or $V_{VCOREFB}$(^) or V_{VSTBY}, refer to 4.3.12		V
[^] To ensure a correct behavior of the internal circuitry, if VIO is connected to VCOREFB, $V_{VCOREFB}$ must be equal to 3.3 V or 5 V							
Grounds							
V_{DGND}	DGND: voltage range	Ground	vs. AGND	-0.1	0	0.1	V
V_{BSTGND}	BSTGND: voltage range	Ground	vs. AGND	-0.1	0	0.1	V
$V_{VCOREGND}$	VCOREGND: voltage range	Ground	vs. AGND	-0.1	0	0.1	V
Cell and battery sensing & balancing AFE							
V_{VPP_SLEEP}	VPP: voltage range in SLEEP MODE	Global	vs. AGND SLEEP MODE	6 [*]	12	19	V
$V_{VPP_STANDBY}$	VPP: voltage range in STANDBY MODE	Global	vs. AGND STANDBY MODE	6 [*]	12	19	V
V_{VPP_NORMAL}	VPP: voltage range in NORMAL MODE	Global	vs. AGND NORMAL MODE	6 [*] 4.5 [**]	12	28 [***]	V
[*]Self-discharge and maintain mode scenarios. Refer to Section 4.1.6.2.							
[**]Crank and soft short-circuit scenarios. Refer to Section 4.1.6.4, Section 4.1.6.3.							
[***]Jump start scenario.							
V_{VBS_SLEEP}	VBS: voltage range in SLEEP MODE	Global	vs. AGND	6 [*]	12	19	V

Symbol	Description	Parameter	Test conditions	Min.	Typ.	Max.	Unit
			SLEEP MODE				
$V_{VBS_STANDBY}$	VBS: voltage range in STANDBY MODE	Global	vs. AGND STANDBY MODE	6 [*]	12	19	V
V_{VBS_NORMAL}	VBS: voltage range in NORMAL MODE	Global	vs. AGND NORMAL MODE	6 [*] 4.5 [**]	12	28 [***]	V
V_{C0}	C0: voltage range	Global	vs. AGND	-0.2		0.2	V
V_{C1}	C1: voltage range	Global	vs. AGND	0		V_{VBS}	V
V_{C2}	C2: voltage range	Global	vs. AGND	0		V_{VBS}	V
V_{C3}	C3: voltage range	Global	vs. AGND	0		V_{VBS}	V
V_{C4}	C4: voltage range	Global	vs. AGND	0		V_{VBS}	V
V_{Cx} - V_{Cx-1}	Differential voltage between adjacent cell pins	-		0		5	V
V_{S0}	S0: voltage range	Global	vs. AGND	-0.2		5	V
V_{S1}	S1: voltage range	Global	vs. AGND	0		V_{VBS} - 4	V
V_{S2}	S2: voltage range	Global	vs. AGND	0		V_{VBS} - 4	V
V_{S3}	S3: voltage range	Global	vs. AGND	0		V_{VBS}	V
V_{S4}	S4: voltage range	Global	vs. AGND	0		V_{VBS}	V
V_{Sx} - V_{Sx-1}	Differential voltage between adjacent balancing pins	-		0		5	V
Current sensing AFE							
V_{CSAN0}, V_{CSAN1}	CSAN0, CSAN1: voltage range	Local	vs. AGND	Refer to: • $V_{CS_ABS_OR}$ in 4.7.1.1 for CS ADC • $V_{CC_ABS_OR}$ in 4.7.2.1 for CC ADC • $V_{SC_ABS_OR}$ in 4.8.3 for SC ADC			V
V_{CSAP0}, V_{CSAP1}	CSAP0, CSAP1: voltage range	Local	vs. AGND	Refer to: • $V_{CS_ABS_OR}$ in 4.7.1.1 for CS ADC • $V_{CC_ABS_OR}$ in 4.7.2.1 for CC ADC • $V_{SC_ABS_OR}$ in 4.8.3 for SC ADC			V
Gate pre-drivers							
V_{VS1}	VS1: voltage range	Local	vs. AGND	0		MAX (V_{VPP}; V_{VBS})	V
V_{VG1}	VG1: voltage range	Local	vs. AGND	V_{VS1}		min (V_{VCP}; V_{VS1}+12)	V
V_{VS2}	VS2: voltage range	Local	vs. AGND	0		MAX (V_{VPP}; V_{VBS})	V
V_{VG2}	VG2: voltage range	Local	vs. AGND	V_{VS2}		min (V_{VCP}; V_{VS2}+12)	V
GPIOs							
V_{GPIO0}, V_{GPIO1}	GPIO0, GPIO1: voltage range	Global	vs. AGND	0		V_{VTREF} if A V_{VIO} if DO V_{VCC} if DI	V

Symbol	Description	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Analog inputs							
V_{AIN2}, …, V_{AIN5}	AIN2, …, AIN5: voltage range	Global	vs. AGND	0		V_{VTREF}	V
XTAL Oscillator							
V_{XIN}	XIN: voltage range	Local	vs. AGND	0		3.6	V
V_{XOUT}	XOUT: voltage range	Local	vs. AGND	0		3.6	V
V_{XIN} - V_{XOUT}	Differential voltage between XIN and XOUT pins	-		-3.6		3.6	V
Digital							
V_{VCCSEL}	VCCSEL: voltage range	Local	vs. AGND	0		V_{VPRE}	V
V_{HS_IN1}	HS_IN1: voltage range	Local	vs. AGND	0		V_{VCC}	V
V_{HS_IN2}	HS_IN2: voltage range	Local	vs. AGND	0		V_{VCC}	V
V_{WAKE}	WAKE: voltage range	Global	vs. AGND	0		V_{VBP_NORMAL}	V
V_{IGN}	IGN: voltage range	Global	vs. AGND	0		V_{VBP_NORMAL}	V
V_{RST2}	RST2: voltage range	Local	vs. AGND	0		V_{VCC}	V
V_{RST1}	RST1: voltage range	Local	vs. AGND	0		V_{VIO}	V
V_{SDO}	SDO: voltage range	Local	vs. AGND	0		V_{VIO}	V
V_{SCL}	SCL: voltage range	Local	vs. AGND	0		V_{VCC}	V
V_{SDI}	SDI: voltage range	Local	vs. AGND	0		V_{VCC}	V
V_{NCS}	NCS: voltage range	Local	vs. AGND	0		V_{VCC}	V
V_{PRN}	PRN: voltage range	Local	vs. AGND	0		V_{VCC}	V
V_{WDTDIS}	WDTDIS: voltage range	Local	vs. AGND	0		V_{VCC}	V
V_{FSO1}	FSO1: voltage range	Local	vs. AGND	0		V_{VIO}	V
V_{FSO2}	FSO2: voltage range	Local	vs. AGND	0		V_{VIO}	V
V_{FCCU1}	FCCU1: voltage range	Local	vs. AGND	0		V_{VCC}	V
V_{FCCU2}	FCCU2: voltage range	Local	vs. AGND	0		V_{VCC}	V
V_{FAULT}	FAULT: voltage range	Local	vs. AGND	0		V_{VCC}	V
V_{LATCH}	LATCH: voltage range	Local	vs. AGND	0		V_{VIO}	V
$V_{RTCWPST}$	RTCWPST: voltage range	Local	vs. AGND	0		V_{VIO}	V
V_{INTC}	INTC: voltage range	Local	vs. AGND	0		V_{VIO}	V

3.2 Absolute Maximum Ratings (AMR)

Exceeding any Absolute Maximum Rating (AMR) may cause permanent damage to the integrated circuit.
All voltages are related to the substrate ground potential, AGND.

Table 3. Absolute maximum ratings

Symbol	Test conditions	Min.	Max.	Unit	Notes
Power supplies					
V_{VBP}	vs. AGND	-0.3	40	V	
V_{VREF}	vs. AGND	-0.3	40	V	
V_{VBP}-V_{C4}		-40	40	V	
V_{VBP}-V_{VBS}		-40	40	V	
V_{BSTSW}	vs. AGND	-0.3	20	V	
V_{BSTSS}	vs. AGND	-0.3	20	V	
V_{VBST}	vs. AGND	-0.3	40	V	
V_{VCP}	vs. AGND	V_{VBST} - 0.3	V_{VBST} + 20	V	
V_{VFLY1}	vs. AGND	V_{VBST} - 0.3	V_{VBST} + 20	V	
V_{VFLY2}	vs. AGND	MAX (- 0.3; V_{VBST} - 8)	V_{VBST} + 0.3	V	
V_{VFLY3}	vs. AGND	V_{VFLY1} - 0.3	V_{VBST} + 20	V	
V_{VFLY4}	vs. AGND	MAX (- 0.3; V_{VBST} - 8)	V_{VBST} + 0.3	V	
V_{BUCKD}	vs. AGND	-0.3	40	V	
V_{BUCKBT}	vs. AGND	-0.3	45	V	
V_{VPRESW}	vs. AGND	-0.3	40	V	-1 V Transient condition
V_{VPRE_CC}	vs. AGND	-0.3	20	V	
V_{VPRE_CORE}	vs. AGND	-0.3	20	V	
$V_{VCORESW}$	vs. AGND	-1	20	V	
$V_{VCOREFB}$	vs. AGND	-0.3	20	V	
$V_{VCORESEL}$	vs. AGND	-0.3	20	V	
V_{VCC}	vs. AGND	-0.3	20	V	
V_{VCCCAN}	vs. AGND	-0.3	20	V	
V_{VTREF}	vs. AGND	-0.3	20	V	
V_{VSTBY}	vs. AGND	-0.3	20	V	
V_{VANA}	vs. AGND	-0.3	4.6	V	
V_{VIO}	vs. AGND	-0.3	20	V	
Grounds					
V_{DGND}	vs. AGND	-0.3	0.3	V	
V_{BSTGND}	vs. AGND	-0.3	0.3	V	
$V_{VCOREGND}$	vs. AGND	-0.3	0.3	V	
Cell sensing & balancing AFE					
V_{VPP}	vs. AGND	-18 [*]	40	V	
V_{VBS}	vs. AGND	-0.3	40 [*]	V	

Symbol	Test conditions	Min.	Max.	Unit	Notes
[*] In the application scenario, the minimum value of V_{VPP} and the maximum value of V_{VBS} are mutually exclusive					
V_{C0}	C0 vs. AGND	-0.5	0.5	V	
V_{C1}	C1 vs. AGND	-0.3	40	V	
V_{C2}	C2 vs. AGND	-0.3	40	V	
V_{C3}	C3 vs. AGND	-0.3	40	V	
V_{C4}	C4 vs. AGND	-0.3	40	V	
V_{Cx} - V_{Cx-1}		-40	40	V	
V_{VBS} - V_{C4}		-40	40	V	
V_{S0}	S0 vs. AGND	-0.3	6.5	V	
V_{S1}	S1 vs. AGND	-0.3	20	V	
V_{S2}	S2 vs. AGND	-0.3	34	V	
V_{S3}	S3 vs. AGND	-0.3	40	V	
V_{S4}	S4 vs. AGND	-0.3	40	V	
V_{Sx} - V_{Sx-1}		-0.3	14	V	
V_{Cx} - V_{Sx}		-40	40	V	
Current sensing AFE					
V_{CSAN0}, V_{CSAN1}	vs. AGND	-0.5	4.6	V	
V_{CSAP0}, V_{CSAP1}	vs. AGND	-0.5	4.6	V	
V_{CSAPx} - V_{CSANx}		-4.6	4.6	V	
Gate pre-drivers					
V_{VS1}	vs. AGND	-18	40	V	
V_{VG1}	vs. AGND	V_{VS1}	min (V_{VCP}; V_{VS1}+20)	V	
V_{VS2}	vs. AGND	-18	40	V	
V_{VG2}	vs. AGND	V_{VS2}	min (V_{VCP}; V_{VS2}+20)	V	
GPIOs					
V_{GPIO0}, V_{GPIO1}	vs. AGND	-0.3	20	V	
Analog inputs					
V_{AIN2}, …, V_{AIN5}	vs. AGND	-0.3	20	V	
XTAL Oscillator					
V_{XIN}	vs. AGND	-0.3	4.6	V	
V_{XOUT}	vs. AGND	-0.3	4.6	V	
V_{XIN} - V_{XOUT}		-4.6	4.6	V	
Digital					
V_{VCCSEL}	vs. AGND	-0.3	20	V	
V_{HS_IN1}	vs. AGND	-0.3	20	V	
V_{HS_IN2}	vs. AGND	-0.3	20	V	
V_{WAKE}	vs. AGND	-0.3	40	V	
V_{IGN}	vs. AGND	-0.3	40	V	
V_{RST2}	vs. AGND	-0.3	20	V	

Symbol	Test conditions	Min.	Max.	Unit	Notes
V_{RST1}	vs. AGND	-0.3	V_{VIO} + 0.3	V	
V_{SDO}	vs. AGND	-0.3	V_{VIO} + 0.3	V	
V_{SCL}	vs. AGND	-0.3	20	V	
V_{SDI}	vs. AGND	-0.3	20	V	
V_{NCS}	vs. AGND	-0.3	20	V	
V_{PRN}	vs. AGND	-0.3	20	V	
V_{WDTDIS}	vs. AGND	-0.3	20	V	
V_{FSO1}	vs. AGND	-0.3	V_{VIO} + 0.3	V	
V_{FSO2}	vs. AGND	-0.3	V_{VIO} + 0.3	V	
V_{FCCU1}	vs. AGND	-0.3	20	V	
V_{FCCU2}	vs. AGND	-0.3	20	V	
V_{FAULT}	vs. AGND	-0.3	V_{VIO} + 0.3	V	
V_{LATCH}	vs. AGND	-0.3	V_{VIO} + 0.3	V	
$V_{RTCWPST}$	vs. AGND	-0.3	V_{VIO} + 0.3	V	
V_{INTC}	vs. AGND	-0.3	V_{VIO} + 0.3	V	

3.3 ESD ratings

Table 4. ESD ratings

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Notes
HBM_ESD(1)	Human body model	HBM (100 pF, 1.5 kΩ) done according to AEC-Q100-002	-2		2	kV	Class 2 (2)
HBM_ESD_GLOBAL(3)	Human body model	HBM (100 pF, 1.5 kΩ) done with all not zapped pins connected to ground	-4		4	kV	-
CDM_ESD	Charged device model	Test done according to AEC-Q100-011	-500		500	V	Class C2a (4)
CDM_COR_ESD	Charged device model for corner pins	Test done according to AEC-Q100-011	-750		750	V	Class C2b (4)
LUT	Latch up	Test done according to AEC-Q100-004	-100		100	mA	-

1. *Valid for all pins*
2. *According to ANSI/ESDA/JEDEC JS-001-2017*
3. *Valid for global pins (for classification refer to Table 1. Pin description)*
4. *According to ANSI/ESDA/JEDEC JS-002-2018*

3.4 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{amb}	Operating and testing temperature		-40		125	°C
T_J (1)	Junction temperature for all parameters		-40		150	°C
T_{stg}	Storage temperature		-40		150	°C
T_{std}	Thermal shut-down temperature (junction)		175		200	°C
T_{adc_acc}	Temperature ADC accuracy		-10		10	°C
T_{hys}	Thermal shut-down temperature hysteresis			10		°C
R_{TH_ja}	Junction to ambient thermal resistance	According JEDEC standard on 2s2p PCB		22		°C/W
R_{TH_jb}	Junction to board thermal resistance	According JEDEC standard on 2s2p PCB		8.3		°C/W
R_{TH_jc}	Junction to case thermal resistance	According JEDEC standard on 2s2p PCB		9.5		°C/W

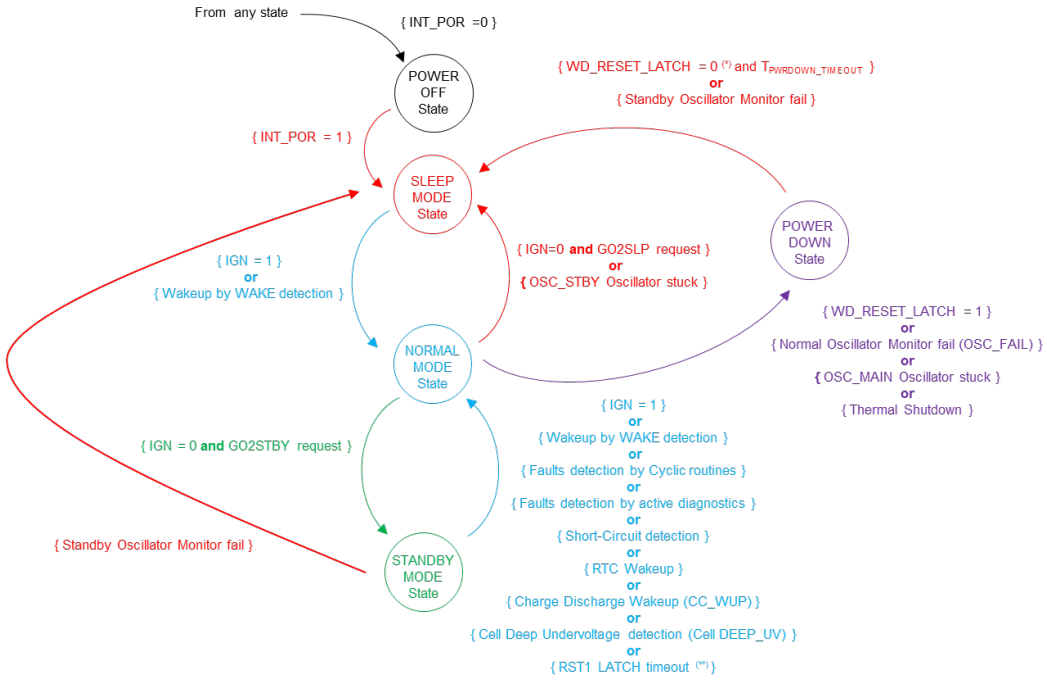
1. *In NORMAL MODE state, assuming a maximum ambient temperature T_{amb} = 75°C, and considering the reference application model (I_{NORMAL_MAX} = 20 mA defined in Section 4.2.1 ($I_{VBST_BASE_NORMAL}$ of Table 8) and R_{TH_ja} = 22°C/W), the increase due to power dissipation (with V_{VBP} = 18.5 V and a maximum balancing current of 200 mA flowing in each driver with R_{DSON_BAL} = 2 Ω (refer to Section 4.5.2) is approx. 40°C. So, in the worst-case scenario, the final junction temperature is well below the maximum allowed value of T_{J_MAX} = 150°C.*

4 Functional description

4.1 Device Functional States (FSM)

L9988 operates according to the following FSM.

Figure 4. Device FSM



(*)WD_RESET_LATCH is reset in POWER DOWN state in case IGN is LOW (in detail, when $V_{IGN} < V_{IGN_HIGH} - V_{IGN_HYS}$ for an interval longer than T_{IGN_FIL}, refer to Section 4.16).

(**)RST1 LATCH timeout will set WD_RESET_LATCH once device moves to NORMAL state (refer to Section 4.16.3) and then moves to POWER DOWN state.

The status of FSM is reported in the read only 4-bit field FSM_STATE in the GENERAL_REG register.

The following table summarizes the FSM behavior, describing the transitions and the resources active in each operating state.

Table 6. Device FSM

State	Purpose	Reached from	Condition	Active resources
POWER OFF	Device OFF	Any state	If INT_POR = 0 for an interval longer than $T_{POR_ASF_FIL_DET}$	None
SLEEP MODE	Ultra-low power state for managing long inactivity periods	POWER OFF	If INT_POR = 1 for an interval longer than $T_{POR_ASF_FIL_REL}$	Edge triggered wakeup input (WAKE) Level triggered wakeup input (IGN) Low frequency oscillator (OSC_STBY), only during T_{IGN_FIL} or T_{WAKE_FIL}, otherwise OFF Internal 3.3 V LDO Configuration/trimming available (after the NVM download during each SLEEP to NORMAL transition)
		NORMAL MODE	GO2SLP command received after $V_{IGN} < V_{IGN_HIGH} - V_{IGN_HYS}$ for an interval longer than T_{IGN_FIL} OSC_STBY oscillator stuck	
		STANDBY MODE	Standby oscillator monitor fail	

State	Purpose	Reached from	Condition	Active resources
SLEEP MODE	Ultra-low power state for managing long inactivity periods	POWER DOWN	WD_RESET_LATCH=0 and $T_{PWRDOWN_TIMEOUT}$ is elapsed Standby oscillator monitor fail	Edge triggered wakeup input (WAKE) Level triggered wakeup input (IGN) Low frequency oscillator (OSC_STBY), only during T_{IGN_FIL} or T_{WAKE_FIL}, otherwise OFF Internal 3.3 V LDO Configuration/trimming available (after the NVM download during each SLEEP to NORMAL transition)
STANDBY MODE	Low power state for managing battery idle state	NORMAL MODE	GO2STBY command received after $V_{IGN} < V_{IGN_HIGH} - V_{IGN_HYS}$ for an interval longer than T_{IGN_FIL}	All resources active in SLEEP MODE, plus the following: Voltage conversion routine (cyclically activated, configurable by SPI) Current conversion routine (cyclically activated, configurable by SPI) by CS ADC and CC ADC Short-circuit detection (if enabled) Standby oscillator monitor Cell balancing FETs (if enabled) LDO3 VTREF (cyclically activated) LDO4 VSTBY (if enabled) Internal analog LDO VANA (cyclically activated) Charge pump Internal RTC (if enabled) Low frequency oscillator (OSC_STBY) XTAL oscillator High frequency oscillator (OSC_MAIN) cyclically activated to perform voltage and current conversion routines CB drivers (following HS_CMD_IN1 and HS_CMD_IN2 bits,refer to Section 4.10.2 for details)
POWER DOWN	Safe state after critical failures	NORMAL MODE	WD_RESET_LATCH=1 (refer to Section 4.16 for detailed description) Normal oscillator monitor fail (OSC_FAIL=1) OSC_MAIN oscillator stuck Thermal shutdown	Short-circuit detection (if enabled) (*) Standby oscillator monitor Low frequency oscillator (OSC_STBY) XTAL oscillator High frequency oscillator (OSC_MAIN) Charge pump (*) CB drivers (following HS_CMD_IN1 and HS_CMD_IN2 bits,refer to Section 4.10.2 for details) (*) NVM fault internal upload (**) (*) *Active if condition is not thermal shutdown* (**) *Active if conditions are not thermal shutdown, OSC_FAIL=1 and OSC_MAIN stuck*
NORMAL MODE	Full operation	SLEEP MODE	Wakeup by WAKE detection	All resources active in SLEEP and STANDBY MODE, plus the following:

State	Purpose	Reached from	Condition	Active resources
NORMAL MODE	Full operation		If V_{IGN} > V_{IGN_HIGH} for an interval longer than T_{IGN_FIL}	Boost VBST Buck1 VPRE Buck2 VCORE LDO1 VCC LDO2 VCC CAN LDO3 VTREF (fully activated) NVM download only in SLEEP to NORMAL MODE transition High frequency oscillator (OSC_MAIN) always activated Normal oscillator monitor (replace the standby oscillator monitor) CB drivers (according to Table 70, refer to Section 4.10.2 for details) GPIOs Digital I/O SPI interface Watchdogs and MCU monitor NVM upload (on demand) Analog BIST (on demand)
		STANDBY MODE	Wakeup by WAKE detection If V_{IGN} > V_{IGN_HIGH} for an interval longer than T_{IGN_FIL} Faults detected by voltage conversion routine (refer to Section 4.4 for details) Faults detected by current conversion routine (refer to Section 4.7 for details) Faults detected by active diagnostics Short-circuit detection (if enabled) Charge/discharge Wakeup CC_WUP (if enabled) Internal RTC wakeup (if enabled) Cell deep UV detection (refer to Section 4.4.1.1) RST1 LATCH timeout	

4.1.1 POWER OFF state

In case INT_POR is detected LOW for an interval longer than $T_{POR_ASF_FIL_DET}$, the device is in POWER OFF state, with all the resources not available.

4.1.2 SLEEP MODE state

SLEEP MODE is an ultra-low power state for managing long inactivity periods.

In this state, only wakeup detections are available on the IGN and WAKE pins.

Internal 3.3 V regulators to supply logic are enabled, but all oscillators are OFF.

As soon as a transition is detected on the WAKE or IGN pin, the low frequency standby oscillator OSC_STBY is enabled to validate the wakeup source. In case the wakeup is not confirmed, the transition to NORMAL MODE is aborted, and OSC_STBY is turned OFF again to recover the ultra-low power condition.

Last downloaded trimming values and some configurations (indicated in the SPI register map) are maintained in the logic.

4.1.3 STANDBY MODE state

STANDBY MODE is a low power state for managing battery idle state.

Active functions in this state can be configured by the MCU during NORMAL MODE before the GO2STBY command, with a reduced power consumption according to the enabled resources.

The GO2STBY command is accepted only if the IGN is LOW.

In this state, wakeup detections are available on the IGN and WAKE pins to come back in NORMAL MODE. Other digital I/Os are not available.

Low frequency standby oscillator (OSC_STBY) and XTAL oscillator (with or without crystal) are enabled and monitored by each other.

Low frequency standby oscillator is used for charge pump, HS pre-drivers logic, wakeup detection, short-circuit detection and balancing (if running before the GO2STBY command).

XTAL oscillator is used for internal RTC, to cyclically activate the voltage and current conversion routines (during which high frequency oscillator is used), and for the VTREF LDO supplying the external NTC.

Once STANDBY MODE is reached, coulomb counter is reset, and voltage and current conversion routines start after a $T_{CYCLE_STANDBY}$, as described in Section 4.4 and Section 4.7.

4.1.4 POWER DOWN state

POWER DOWN safe state is reached from NORMAL MODE after the following critical failures:

1. Thermal shutdown
2. Persistent watchdog fails causing WD_RESET_LATCH (refer to Section 4.16 for detailed description)
3. Normal oscillator monitor fail
4. Main oscillator stuck

Once the state is reached because of thermal shutdown, the device turns OFF all the resources for $T_{PWRDOWN_TIMEOUT}$ to safely move to SLEEP MODE state and try to attempt a new power up if IGN is still detected HIGH.

For the other failures described above, the charge pump, SC detection and circuit breaker (CB) back-to-back MOSFETs can be kept ON (following HS_CMD_IN1 and HS_CMD_IN2 bits,refer to Section 4.10.2) for $T_{HSD_TIMEOUT}$ and then the device safely moves to SLEEP MODE state when $T_{PWRDOWN_TIMEOUT}$ is reached.

$T_{HSD_TIMEOUT}$ is configurable using the 4-bit HSD_TIMEOUT_CFG field, with default HSD_TIMEOUT_CFG = 1000 corresponds to a default $T_{HSD_TIMEOUT}$ =128 seconds.

Only in case the state is reached because of persistent watchdog fails causing WD_RESET_LATCH = 1, the device also automatically attempts a NVM fault internal upload as described in Section 4.17.4.

Low frequency standby oscillator (OSC_STBY) and XTAL oscillator (with or without crystal) are enabled and monitored by each other. In this state, the ongoing voltage conversion routine, current conversion routine and balancing are interrupted.

Table 7. Timeout in POWER DOWN state electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$T_{PWRDOWN_TIMEOUT}$	Internal timer for POWER DOWN transition			240		s	-
$T_{HSD_TIMEOUT}$	Time period during which the CB MOSFETs can be kept ON (4-bit) $T_{HSD_TIMEOUT}$ = 16 * CODE		0		240	s	-

4.1.5 NORMAL MODE state

This is the FULL OPERATIVE state of the device in which all functions are available and can be activated.

The trimming and configuration bits stored in the internal NVM are automatically downloaded at each SLEEP to NORMAL MODE transition.

During this transition, the device monitors VCCSEL and VCORESEL to properly configure the regulators to be powered up. The power-up sequence is performed as described in the timing diagrams in Section 4.1.6.

Once the NORMAL MODE state is reached, the voltage and current conversion routines wait for an MCU configuration to perform a start of conversion (SoC) on-demand by SPI or periodically by an internal timer. This is also needed to let the MCU voltage and current routine data readout (e.g. coulomb counting) measured during STANDBY MODE.

The other configurations and register map are kept in STANDBY to NORMAL MODE transition, while in SLEEP to NORMAL MODE transition, the configuration bits stored in NVM are downloaded into the register map.

Some self-test can be performed by MCU once RST1 is released, such as analog BIST or software self-check.

Digital I/Os are fully available.

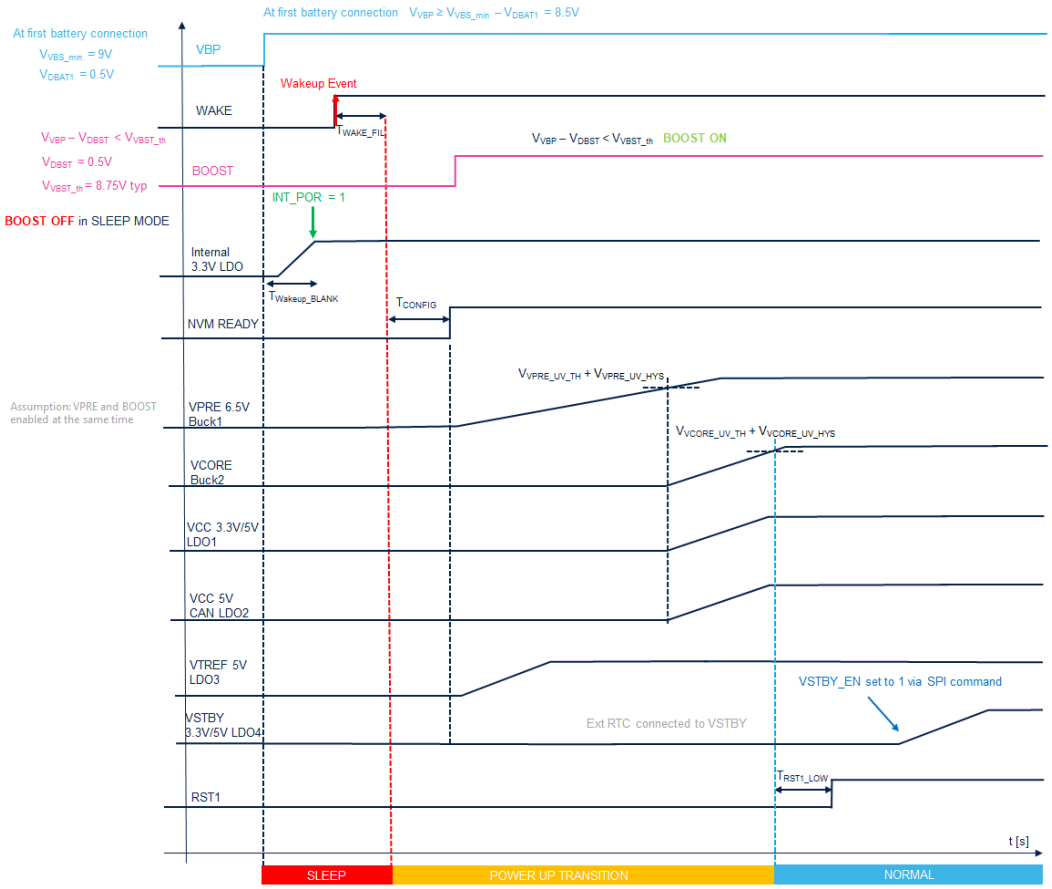
WD1 (if enabled) is automatically enabled once RST1 is released, with a long timeout to let the MCU complete the boot time and serve it properly. WD2 can be enabled by the MCU with the WDTDIS pin.

4.1.6 Power up sequences and scenarios

4.1.6.1 Power up after first battery connection

Figure 5 illustrates the timing diagram for a power-up sequence by wake detection after the first battery connection.

Figure 5. Power up by wake detection after first battery connection



In the timing diagram, T_{Wakeup_BLANK} (800µs) is the time required to activate internal 3.3 V LDO to detect wakeup event, while T_{CONFIG} (defined in Section 4.17.2.1) is the time required to turn on the entire internal power supply and to download trimming, Buck1 and LDO1,2,3,4 configurations from the first four sectors of the NVM (VCORE Buck2 is configured via VCORESEL pin, VCC LDO1 is configured via VCCSEL pin). T_{RST1_LOW} is the reset time de-assertion filter (maximum 1 ms, defined in Section 4.12.5.1).

After the wakeup event, the NORMAL state is reached through a power-up sequence whose duration can be calculated as follows:

$$T_{POWER_UP_SleepNormal} = T_{WAKE_FIL} + T_{CONFIG} + T_{VPRE_SOFT_START} + T_{VCORE_SOFT_START}$$

considering T_{WAKE_FIL} defined in Section 4.12.9.1

T_{CONFIG} defined in Section 4.17.2.1

$T_{VPRE_SOFT_START}$ defined in Section 4.3.4.2

$T_{VCORE_SOFT_START}$ defined in Section 4.3.5.2

Then, a power-up transition from SLEEP to NORMAL MODE is elapsed after $T_{POWER_UP_SleepNormal} < 5$ ms.

4.1.6.2 *SELF-DISCHARGE and deep undervoltage threshold*

Before describing the power-up sequence by wake detection in STANDBY MODE (refer to Section 4.1.6.3) or in SLEEP MODE (refer to Section 4.1.6.5), it is useful to focus on the minimum pack battery voltage **V_{VBS}** value defined in the operational range section (refer to Section 3.1) .

In detail,

- If **V_{VBS}≥ 7.6 V** (**V_{VBP}≥ 7.1 V**, being V_{VBP} = MAX [(V_{VPP} - 0.5 V); (V_{VBS} – 0.5 V)], with 0.5 V = V_{DBAT1} = V_{DBAT2} the maximum forward voltage of external diodes D_{BAT1}, D_{BAT2}), all functional operations of the device is guaranteed.
- If **6 V ≤ V_{VBS} < 7.6 V** (**5.5 V ≤ V_{VBP} < 7.1 V**), the functionality of the device is guaranteed but with a derating on the minimum V_{GS_ON} value for turning on the CB MOSFETs (refer to Table 71 in Section 4.10.3).

Therefore, despite constraints on the choice of external MOSFETs, it is possible to realize the power-up transition of the device from STANDY state or SLEEP state to NORMAL state starting with a minimum battery value **V_{VBS}** of **6 V**.

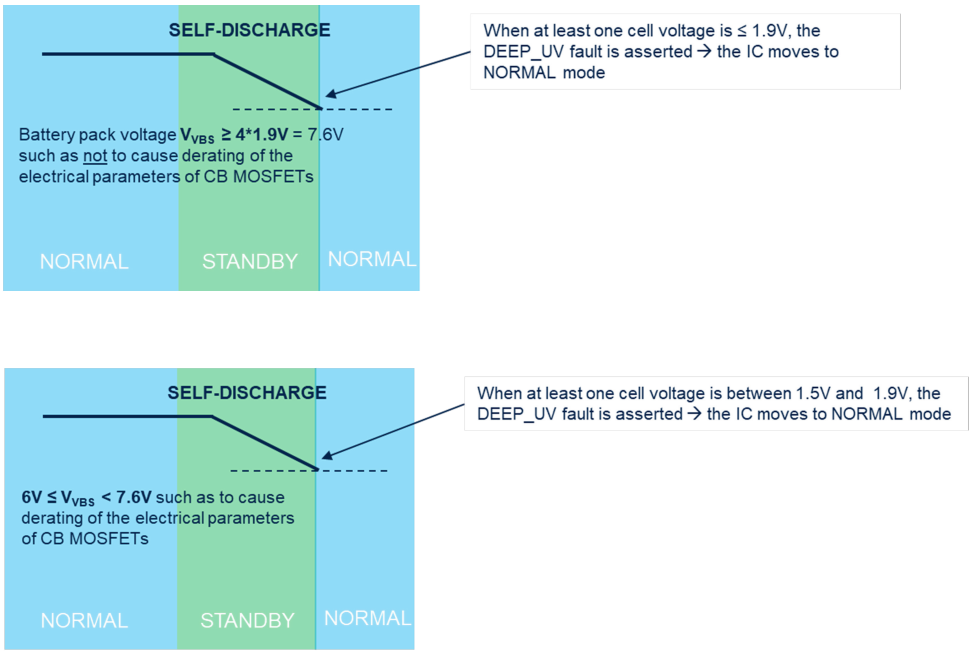
In STANDBY MODE, due to **SELF-DISCHARGE** represented in Figure 6, a cell **deep undervoltage** fault can be acknowledged if the voltage of one or more cells falls below a programmable threshold **$V_{CELL_DEEP_UV_TH}$**, (refer to Section 4.4.1.1).

In this safety relevant condition, the IC moves to NORMAL state, and the FAULT pin is asserted.

In the worst case scenario without derating, the voltage of all cells can reach **1.9 V**. In this case, the pack battery voltage is **7.6 V** and the transition to NORMAL state occurs as mentioned without derating.

However, taking derating into account, the voltage of all cells can reach **1.5 V**, from which the voltage of the battery pack equals to **6 V**.

Figure 6. SELF-DICHARGE scenario in STANDY MODE

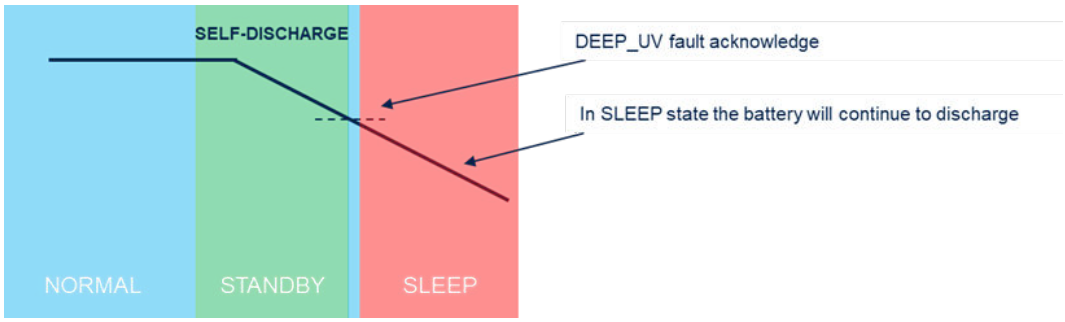


The transition to NORMAL state can be followed by the following scenarios:

- The device remains in NORMAL state, and the 12 V DC-DC charge, or another suitable 12 V charging source available in the specific vehicle architectures, is connected to recharge the battery through KL30, with one or both group of CB back-to-back MOSFETs **ON** (according to Table 70, refer to Section 4.10.2 for details). This scenario is represented in Figure 8 in Section 4.1.6.3.
- If it is not possible to guarantee safe charging of the battery, based on the FSM, after MCU acknowledge the IC moves to SLEEP MODE via a GO2SLP command by the MCU (refer to Section 4.1.8). In this scenario, represented in Figure 7, the battery continues to discharge, and the vehicle must be picked up by a tow truck and brought to the service.

In this last condition, referring to the block diagram of Figure 2, it is also possible to power the IC through KL30 with both groups of CB MOSFETs **OFF** (battery not charging) by using other power sources (e.g. 12 V Pb acid battery, other 12 V Li-on battery, DC-DC power source), in what can be called **MAINTAIN** mode (Figure 11). This guarantees a next power-up sequence by wake detection in SLEEP MODE and a subsequent transition to NORMAL MODE even with a very low battery (V_{VBS} < 6 V) and with the VBP pin powered externally.

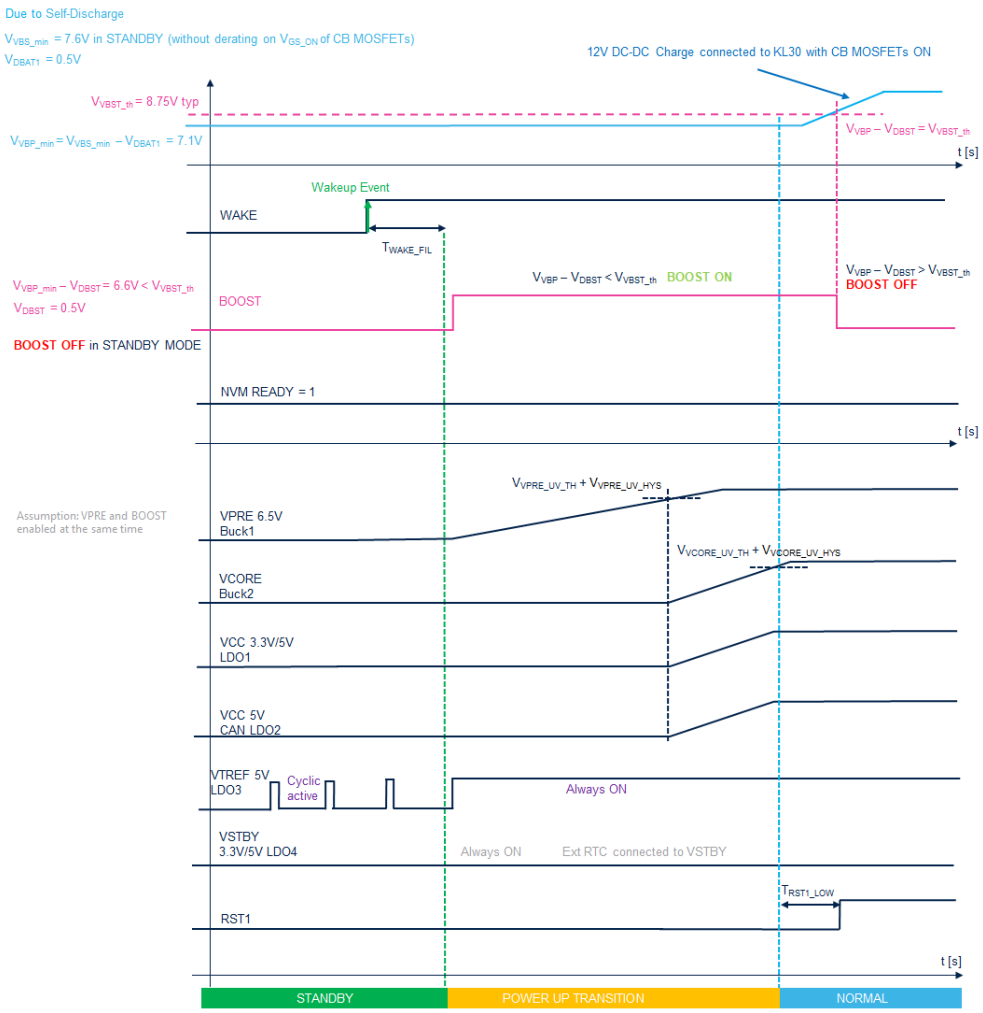
Figure 7. Transition to SLEEP MODE after DEEP_UV fault acknowledge in NORMAL MODE



4.1.6.3 *Power up in STANDBY MODE state*

Figure 8 illustrates the timing diagram for a power-up sequence by wake detection in STANDBY MODE and the scenario in which the 12 V DC-DC charge is connected through KL30 to recharge the battery after the device moves to NORMAL MODE.

Figure 8. Power up by wake detection in STANDBY MODE



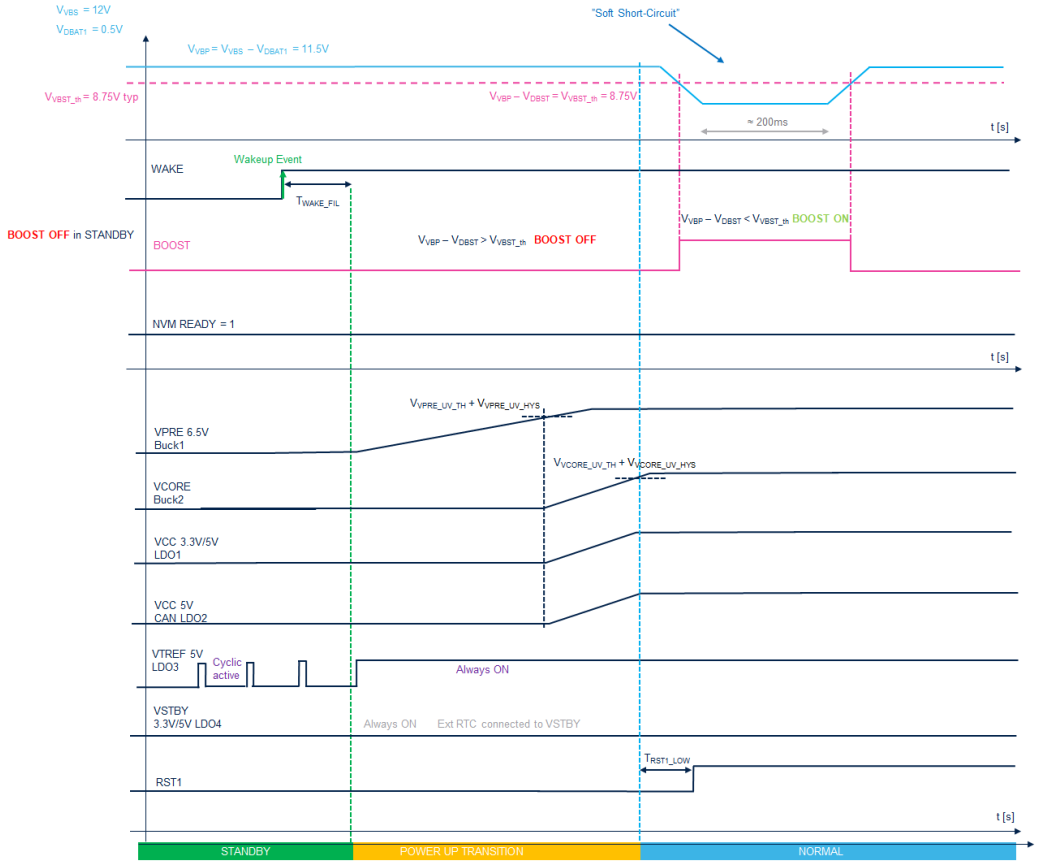
After the wakeup event, the NORMAL state is reached through a power-up sequence whose duration can be calculated as follows:

$T_{POWER_UP_StandbyNormal} = T_{WAKE_FIL} + T_{VPRE_SOFT_START} + T_{VCORE_SOFT_START} = T_{POWER_UP_SleepNormal} - T_{CONFIG}$

Figure 9 illustrates the timing diagram for a power-up sequence by wake detection in STANDBY MODE when the pack battery voltage V_{VBS} is well above the minimum voltage (e.g. 12 V). In this case, the transition to NORMAL MODE can be followed by a **SOFT SHORT-CIRCUIT** event.

This scenario may happen when other 12 V load connected to KL30 is shorted: voltage on KL30 can drop to a value close to **5 V** before the fuse on the 12 V load blows and the burn out occurs within 200 ms ÷ 380 ms. After the fuse has burned, the voltage on KL30 returns to its initial value.

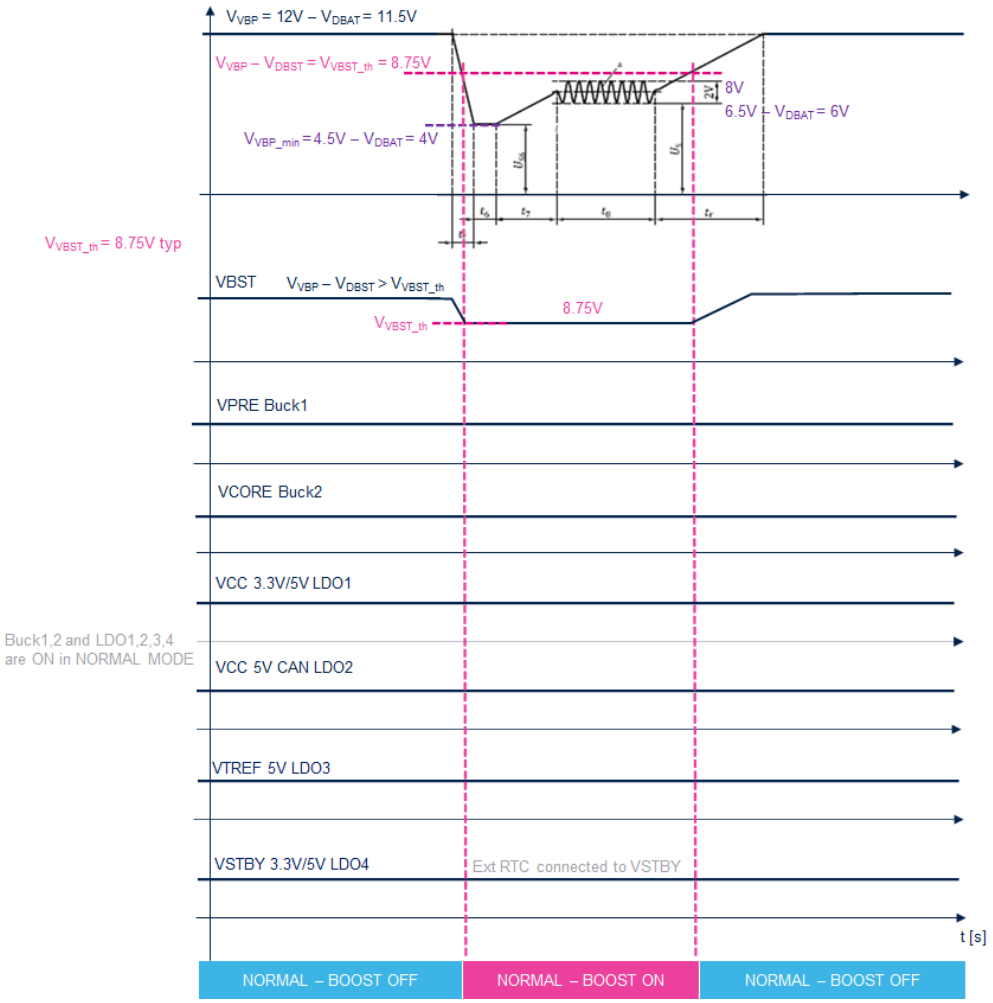
Figure 9. Power up by wake detection in STANDBY MODE and “soft short-circuit” event in NORMAL



4.1.6.4 *Crank pulse in NORMAL MODE state*

Figure 10 illustrates the timing diagram in case of a CRANK pulse in NORMAL MODE. The boost pre-regulator can support full system operation at a low battery voltage, allowing the system to pass the ISO16750-2 test.

Figure 10. Crank pulse in NORMAL MODE

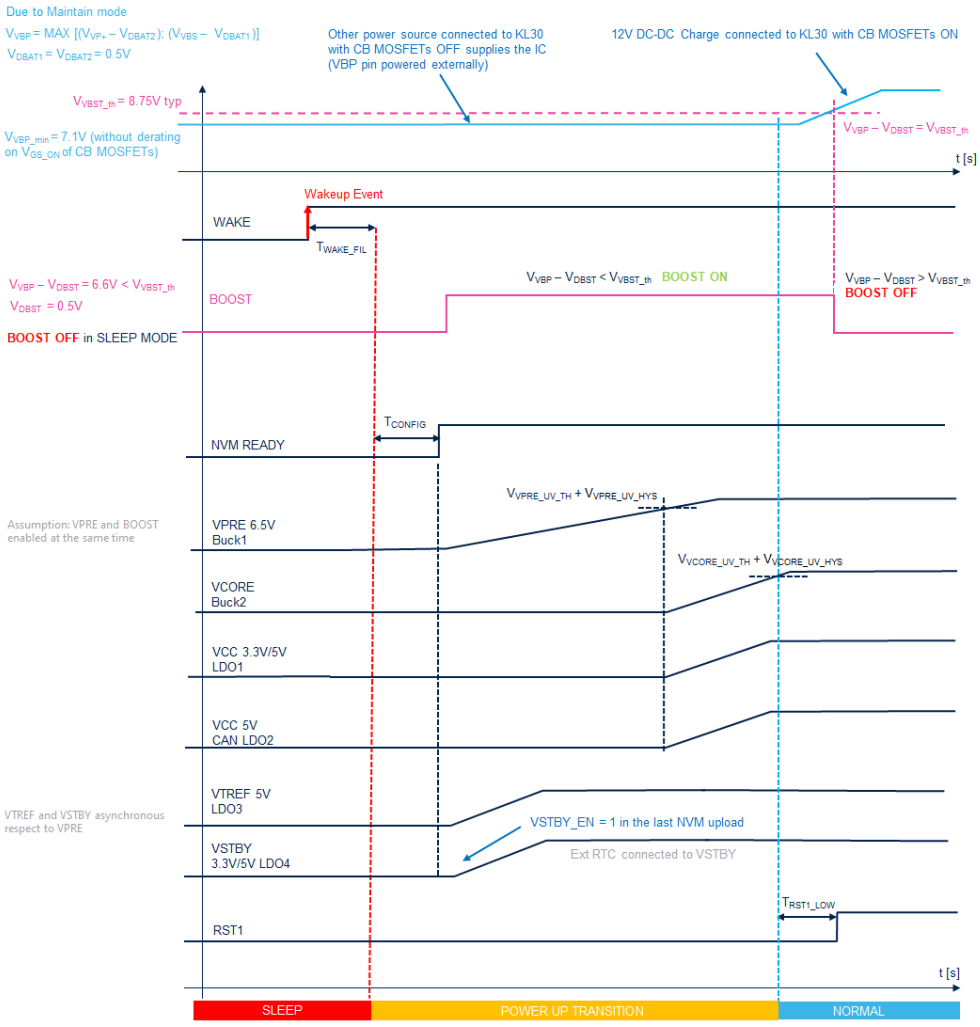


4.1.6.5 *Power up in SLEEP MODE state*

Figure 11 illustrates the timing diagram for a power-up sequence by wake detection in SLEEP MODE (no first battery connection) and the consecutive scenarios in which:

- Other power sources are connected to KL30 with both groups of CB MOSFETs OFF and supplies the IC (MAINTAIN mode during SLEEP MODE state and power-up transition)
- The 12 V DC-DC charge is connected to recharge the battery through KL30 with one or both groups of CB back-to-back MOSFETs ON after the device moves to NORMAL MODE.

Figure 11. Power up by wake detection in SLEEP MODE

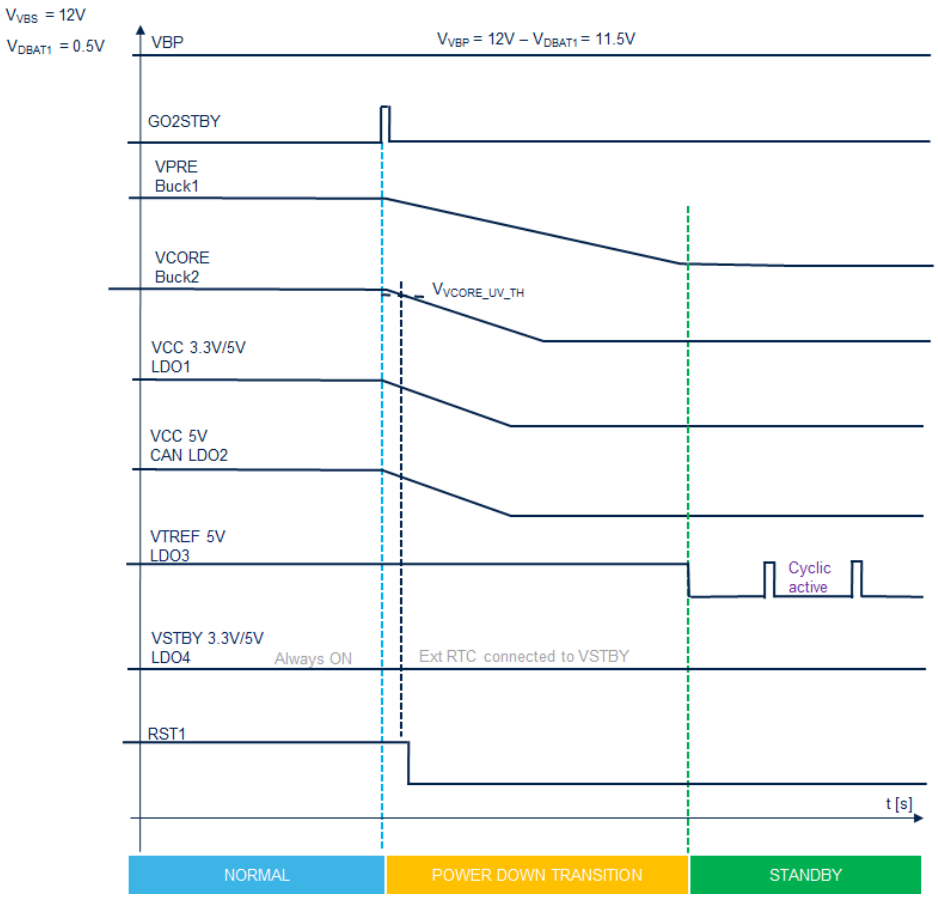


4.1.7 Power down - GO2STBY command

In case the GO2STBY command (0xDD written in the write only field SPECIAL_KEY in the SPECIAL_REG register) is received with IGN LOW, a power down is triggered to reach STANDBY condition. During power-down transition, wakeup sources are ignored until STANDBY state is reached.

Figure 12 illustrates the timing diagram for a power-down sequence by the GO2STBY command.

Figure 12. Power down by GO2STBY command

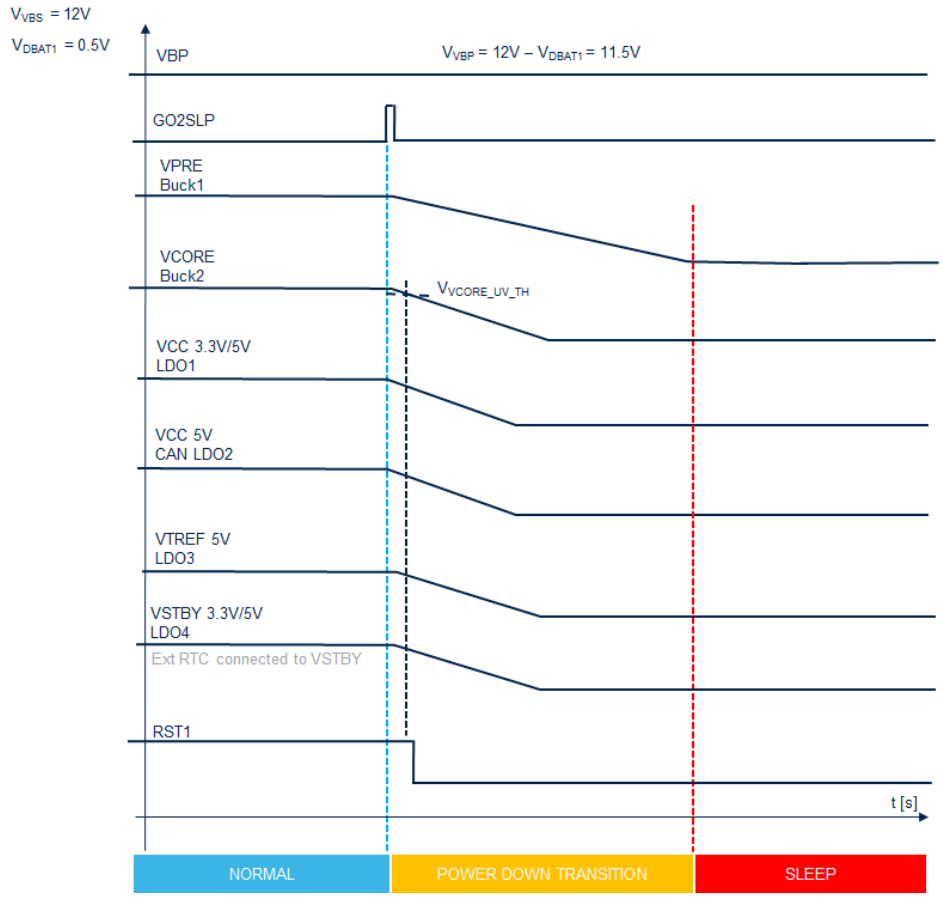


4.1.8 Power down - GO2SLP command

In case the GO2SLP command (0xCC written in the write only field SPECIAL_KEY in the SPECIAL_REG register) is received with IGN LOW, a power down is triggered. During power down transition, wakeup sources are ignored until SLEEP state is reached.

Figure 13 illustrates the timing diagram for a power-down sequence during wake detection or by the GO2SLP command.

Figure 13. Power down by GO2SLP command



During a power-down transition from NORMAL to SLEEP MODE, all regulators are turned OFF at the same time.

The SLEEP state is reached after $T_{POWER_DOWN_NormalSleep}$ < 36 ms.

Before a new power-up sequence can be started, all regulators must be “completely” switched OFF (and the load capacities must be completely discharged.

4.2 Power management

The L9988 is supplied by different pins according to the different functional states. The main supply voltage is the VBP pin, supplying circuitries that need to be active in low power states (SLEEP and STANDBY). When the device moves to NORMAL, the internal circuitry is mainly supplied via **buck pre-regulator (VPRE)**.

4.2.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 8. Power management electrical parameters

Symbol	Description	Test conditions	Min.	Typ.	Max.	Unit	PIN
$I_{VBP_BASE_SLEEP_85}$	Base current consumption from VBP pin in SLEEP state	-40°C ≤ T_J ≤ +85°C			4.5	µA	VBP
$I_{VBP_BASE_SLEEP_125}$	Base current consumption from VBP pin in SLEEP state	+85°C ≤ T_J ≤ +125°C			15	µA	VBP
$I_{VBP_BASE_SLEEP_150}$	Base current consumption from VBP pin in SLEEP state	+125°C ≤ T_J ≤ +150°C			15	µA	VBP
$I_{VBST_BASE_SLEEP}$	Base current consumption from VBST pin in SLEEP state				2	µA	VBST
$I_{VBP_BASE_STANDBY_85}$	Base current consumption from VBP pin in STANDBY state Note: Does not include CP monitor (active by default) CP monitor extra consumption is described below as $I_{VBST_DELTA_CP_UV_OV}$	-40°C ≤ T_J ≤ +85°C			155	µA	VBP
$I_{VBP_BASE_STANDBY_125}$	Base current consumption from VBP pin in STANDBY state Note: Does not include CP monitor (active by default) CP monitor extra consumption is described below as $I_{VBST_DELTA_CP_UV_OV}$	+85°C ≤ T_J ≤ +125°C			155	µA	VBP
$I_{VBP_BASE_STANDBY_150}$	Base current consumption from VBP pin in STANDBY state Note: Does not include CP monitor (active by default) CP monitor extra consumption is described below as $I_{VBST_DELTA_CP_UV_OV}$	+125°C ≤ T_J ≤ +150°C			160	µA	VBP
$I_{VBST_BASE_STANDBY}$	Base current consumption from VBST pin in STANDBY state				40	µA	VBST
$I_{VBP_BASE_NORMAL}$	Base current consumption from VBP pin in NORMAL state				10	mA	VBP
$I_{VBST_BUCKD_SUM_BASE_NORMAL}$	Base current consumption from VBST+BUCKD pin in NORMAL state, without gate current charge for boost and external MOS	BOOST OFF			10	mA	VBST BUCKD
$I_{VBREF_BASE_NORMAL}$	Base current consumption from VBREF pin in NORMAL state				1000	µA	VBREF
$I_{VBP_DELTA_CS}$	Delta current from VBP pin when the CS ADC is enabled	CS continuously converting			600	µA	VBP

Symbol	Description	Test conditions	Min.	Typ.	Max.	Unit	PIN
$I_{VBP_DELTA_CC}$	Delta current from VBP pin when the CC ADC is enabled	CC continuously converting			630	µA	VBP
$I_{VBP_DELTA_SC}$	Delta current from VBP pin when the SC ADC is enabled	SC continuously converting			60	µA	VBP
$I_{VBP_DELTA_ADCV}$	Delta current from VBP pin when one voltage ADC is converting	Voltage ADC continuously converting			800	µA	VBP
$I_{VIO_VBP_DELTA_GPIO}$	Delta current from VBP and VIO pin when one GPIO is programmed as digital output				420	µA	VBP VIO
$I_{VBP_DELTA_BALANCE_CHANNEL}$	Delta current from VBP pin when one balancing channel is programmed ON				15	µA	VBP
$I_{VBP_DELTA_BALANCE}$	Delta current from VBP pin when balancing functions are activated				20	µA	VBP
$I_{VBST_DELTA_VSTBY}$	Delta current from VBST pin to switch ON the VSTBY regulator				10	µA	VBST
$I_{VBST_DELTA_CP_UV_OV}$	Delta current from VBST pin when charge pump UV/OV monitor block is enabled				48	µA	VBST
$I_{VBP_DELTA_CYCLIC}$	Delta current from VBP pin needed during cyclic wake up for ADCs working				3.1	mA	VBP
$I_{VBREF_DELTA_CYCLIC}$	Delta current from VBREF pin needed during cyclic wake up for ADCs working				1000	µA	VBREF
$I_{VBST_DELTA_CBMOS}$	Delta current from VBST pin when one group of CB MOSFETs is turned ON	VG_n, n=1,2 actively pulled up			25	µA	VBST
$I_{VBP_DELTA_VBP_VBS_COMP}$	Delta current from VBP when VBP-VBS comparator is activated in STANDBY state	VBP-VBS comparator enabled			15	µA	VBP

During STANDBY operation, $I_{VBP_DELTA_CS}$, $I_{VBP_DELTA_CC}$, $I_{VBP_DELTA_ADCV}$, $I_{VBP_DELTA_CYCLIC}$ and $I_{VBREF_DELTA_CYCLIC}$ must be weighted over the proper duty cycle of activation to find the average current consumption.

In particular, with reference to Section 4.4 and Section 4.7,

- $I_{VBP_DELTA_CC}$ will be consumed for a time $T_{CC_ON} = (1+AZ_{config}) * (T_{CC_START} + T_{CC_FILTER_STANDBY} + T_{CC_CAL})$

  considering AZ_{config} described in detail in Section 4.7.2.4

- $I_{VBP_DELTA_CS}$ will be consumed for a time $T_{CS_ON} = T_{CC_ON} – (AZ_{config} * (T_{CC_START} + T_{CC_FILTER_STANDBY} + T_{CC_CAL}))$

  considering $T_{CS_FILTER} = T_{CC_FILTER_STANDBY}$ (CS and CC synchronous to automatically perform CS-CC x-check described in Section 4.7.3)

  $T_{CS_START} = T_{CC_START}$ (with $T_{CC_START_NORMAL} = T_{CC_START_STANDBY} = T_{CC_START}$ in Section 4.7.2.1)

  $T_{CS_CAL} = T_{CC_CAL}$ (with $T_{CC_CAL_NORMAL} = T_{CC_CAL_STANDBY} = T_{CC_CAL}$ in Section 4.7.2.1)

- $I_{VBP_DELTA_ADCV}$ will be consumed for a time $T_{ADCV_ON} = 8 * (T_{ADCV_START} + T_{ADCV_FILTER}) + 2 * T_{ADCV_CAL}$

  considering T_{ADCV_START}, T_{ADCV_FILTER}, T_{ADCV_CAL} defined in Section 4.4.1.2

- $I_{VBP_DELTA_CYCLIC}$ will be consumed for a time $T_{CYCLIC_ON} = MAX (T_{CC_ON}, T_{ADCV_ON}) + T_{WAKE}$

  considering T_{WAKE} defined in Section 4.4.1.2

$I_{VBREF_DELTA_CYCLIC}$ will be consumed for a time T_{CYCLIC_ON}

The duty-cycle activation can be calculated as the ratio between T_{CYCLIC_ON} and $T_{CYCLE_STANDBY}$ configured (refer to Section 4.13.1).

To have a proper assessment, it is needed to consider the current that flows in the external resistor placed between gate and source of external FET and the current load on VTREF regulator that is weighted on the D_{CYCLIC_ON}.

4.3 Power supply section

The L9988 is equipped with a comprehensive set of power supply units for feeding both internal and external components.

4.3.1 Main supply (VBP)

The VBP pin is the main supply. This line:

- Feeds the **boost pre-regulator (VBST)**
- Feeds all the internal low-power states circuitry

4.3.1.1 Diagnostics

The IC performs undervoltage and overvoltage detection at the VBP pin; these diagnostics are available only in NORMAL state and are listed in the table below.

Table 9. VBP pin diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VBP Undervoltage	• If V_{VBP} falls below $V_{VBP_UV_TH}$ for an interval longer than $T_{VBP_UV_FIL}$, the boost is ON and no undervoltage has been detected at the VBST pin, the VBP_UV fault is acknowledged	• The VBP_UV flag is set • FAULT pin is asserted	• If V_{VBP} rises above $V_{VBP_UV_TH}$ + $V_{VBP_UV_HYS}$ for an interval longer than $T_{VBP_UV_FIL}$, the VBP_UV flag can be cleared by MCU	• FAULT pin is released	• Blanked during power-up sequence, until NORMAL state is reached from SLEEP state • None
VBP Overvoltage	• If V_{VBP} rises above $V_{VBP_OV_TH}$ for an interval longer than $T_{VBP_OV_FIL}$, the VBP_OV fault is acknowledged	• The VBP_OV flag is set • FSO1, FSO2 lines are asserted	• If V_{VBP} falls below $V_{VBP_OV_TH}$ - $V_{VBP_OV_HYS}$ for an interval longer than $T_{VBP_OV_FIL}$, the VBP_OV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• None

4.3.1.2 VBP, VBS comparison

The IC includes an analog comparator to check the voltage difference between VBP and VBS pins.

The comparator can be enabled in NORMAL state by setting via SPI, the dedicated bit VBP_VBS_COMP_EN before a transition to STANDBY MODE.

The main feature of such a comparator is that, in STANDBY MODE, it allows checking the voltages V_{VBP} and V_{VBS} ,moving the IC to NORMAL MODE to assert the FAULT pin in case of fault, regardless of the execution of the voltage conversion routine and therefore also in a scenario in which VOLT_STEP and DIAG_STEP (defined in Section 4.4) are equal to 0.

This diagnostic covers the failure detailed in the following table.

Table 10. VBP-VBS comparison diagnostic

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VBP-VBS compare fail	If $V_{VBP} – V_{VBS}$ rises above $V_{VBP_VBS_TH}$ for an interval longer than T_{COMP_FIL}, the VBP_VBS_COMP_FAIL fault is acknowledged	• The VBP_VBS_COMP_FAIL flag is set • If in NORMAL, the FAULT pin is asserted • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted	If $V_{VBP} – V_{VBS}$ falls below $V_{VBP_VBS_TH}$ - $V_{VBP_VBS_HYS}$ for an interval longer than T_{COMP_FIL}, the VBP_VBS_COMP_FAILflag can be cleared by MCU	FAULT pin is released	VBP_VBS_COMP_EN=0 masks diagnostic execution. When disabled, the VBP_VBS_COMP_FAIL flag can always be cleared

4.3.1.3 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 11. VBP electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{VBP_UV_TH}$	VBP undervoltage detection Threshold voltage	Boost is ON and no undervoltage has been detected at the VBST pin	4.5		6	V	VBP
$V_{VBP_UV_HYS}$	VBP undervoltage detection Hysteresis voltage			300		mV	VBP
$T_{VBP_UV_FIL}$	VBP undervoltage detection Filter time		5		15	µs	VBP
T_{VBP_BLK}	VBP under/over voltage blanking time upon transition from SLEEP/STBY to NORMAL state			1.6		ms	VBP
$V_{VBP_OV_TH}$	VBP overvoltage detection Threshold voltage		29		32	V	VBP
$V_{VBP_OV_HYS}$	VBP overvoltage detection Hysteresis voltage		300		550	mV	VBP
$T_{VBP_OV_FIL}$	VBP overvoltage detection Filter time		5		15	µs	VBP
$V_{VBP_VBS_TH}$	Analog VBP-VBS compare Threshold voltage	V_{VBP} - V_{VBS}	1.5	2	2.5	V	VBP VBS
$V_{VBP_VBS_HYS}$	Analog VBP-VBS comparator Hysteresis voltage		130		280	mV	VBP VBS
T_{COMP_FIL}	Analog VBP-VBS comparator Filter time			1		ms	VBP VBS

4.3.2 Boost pre-regulator (VBST)

The boost pre-regulator:

- Is fed by the reverse protected battery line **(VBP)**
- Feeds the **charge pump (VCP)**
- Feeds the **buck1 pre-regulator (VPRE)**
- Feeds the **5 V thermistor bias LDO3 (VTREF)**
- Feeds the **3.3 V/5 V standby LDO4 (VSTBY)**

The boost pre-regulator can support full system operation at low battery voltage, allowing the system to pass ISO 16750-2 (Level II) cold cranking tests.

VBST is a boost converter with an external n-MOSFET to generate the output voltage of 8.75 V in case of weak battery condition. The boost activation is configured via SPI with a dedicated bit BOOST_EN (default BOOST_EN = 1). Every time the device enters SLEEP MODE, BOOST_EN is set to its default value. When disabled, the internal driver keep the external FET OFF.

The parameters of the pre-boost regulator can be guaranteed when VBP goes down to 4 V during the cranking phase (refer to Section 4.1.6 for CRANK scenario in NORMAL MODE) and during short-circuit event.

4.3.2.1 Diagnostics

This boost is equipped with undervoltage and overvoltage detection, available only in NORMAL state, and listed in the table below.

Table 12. VBST diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VBST undervoltage	• If V_{VBST} falls below $V_{VBST_UV_TH}$ for an interval longer than $T_{VBST_UV_FIL}$, the VBST_UV fault is acknowledged	• The VBST_UV flag is set • FAULT pin is asserted	• If V_{VBST} rises above $V_{VBST_UV_TH}$ + $V_{VBST_UV_HYS}$ for an interval longer than $T_{VBST_UV_FIL}$, the VBST_UV flag can be cleared by MCU	• FAULT pin is released	• Blanked during power-up sequence, until NORMAL state is reached • When BOOST_EN=0, the VBST diagnostic is masked, the VBST_UV flag can always be cleared
VBST overvoltage	• If V_{VBST} rises above $V_{VBST_OV_TH}$ for an interval longer than $T_{VBST_OV_FIL}$, the VBST_OV fault is acknowledged	• The VBST_OV flag is set • FSO1, FSO2 lines are asserted	• If V_{VBST} falls below $V_{VBST_OV_TH}$ - $V_{VBST_OV_HYS}$ for an interval longer than $T_{VBST_OV_FIL}$, the VBST_OV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• When BOOST_EN=0, the VBST diagnostic is masked, the VBST_OV flag can always be cleared
VBST overcurrent	• If V_{BSTSS} rises above $V_{BOOST_OVC_TH}$ for N_{OVC_TH} consecutive PWM switching cycles, the VBST_OVC fault is acknowledged	• The VBST_OVC flag is set • Boost is turned OFF	• After N_{OVC_TH} PWM cycles the Boost is turned ON and the VBST_OVC flag can be cleared by MCU	• None	• When BOOST_EN=0, the VBST diagnostic is masked, the VBST_OVC flag can always be cleared

It is also protected against overcurrent by means of overcurrent (OVC) detection circuit.

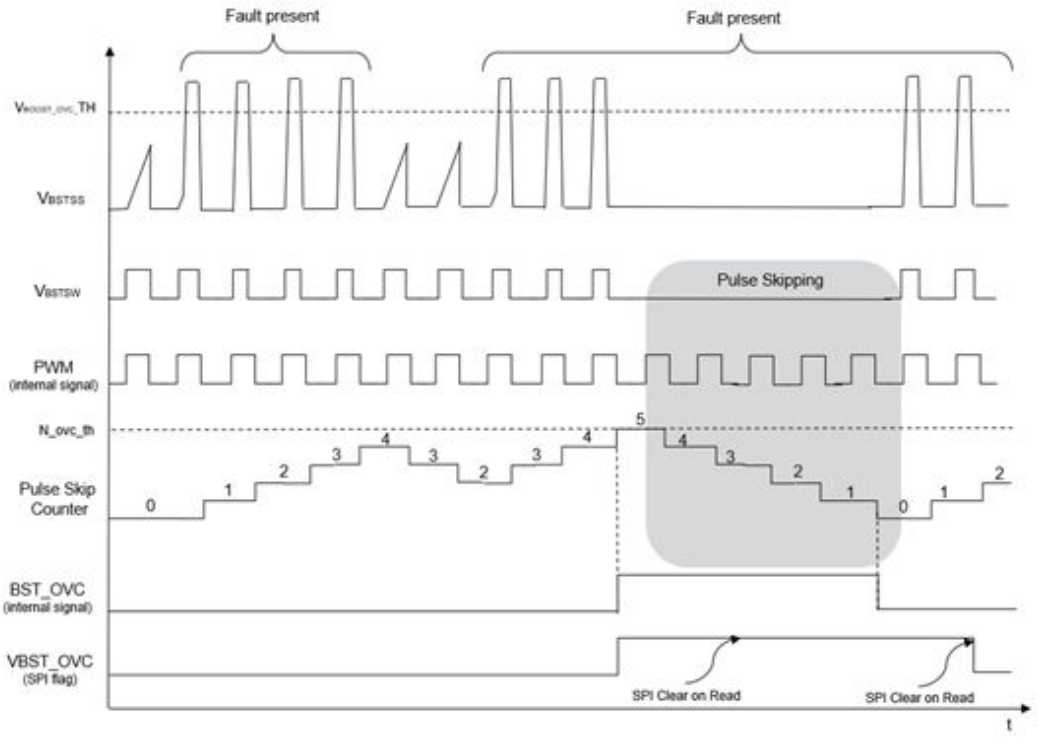
Current flowing in the external FET is sensed through a shunt resistor $\mathbf{R_{SBST}}$. The voltage drop across the shunt resistor, $\mathbf{V_{BSTSS}}$, is monitored and, when it exceeds the $\mathbf{V_{BOOST_OVC_TH}}$ threshold, a single overcurrent event occurs. In case of a persistent overcurrent event, an up/down counter protects the external FET from excessive inrush energy:

- When an OVC event occurs during a PWM switching cycle, the counter is incremented by 1

- When no OVC event occurs during a PWM switching cycle, the counter is decremented by 1
- If the counter is below the **N_{OVC_TH}** threshold, the output re-engagement after an OVC event occurs upon next PWM switching cycle

If the counter reaches the **N_{OVC_TH}** threshold, the flag **VBST_OVC** is set, and the external FET is held OFF for **N_{OVC_TH}** PWM cycles and then released.

Figure 14. Boost overcurrent protection - pulse skipping re-engagement timing diagram



4.3.2.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: VBP according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 13. VBST electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{VBST_TH}	Boost unmask/ mask threshold	When $V_{VBST} < V_{VBST_TH}$, the boost starts for time T_{ON}. When $V_{VBST} \geq V_{VBST_TH}$, the boost is masked after T_{ON} is completed. T_{ON} depends on different duty cycle, $T_{ON} = 1/f_{sw_BOOST}$ * duty cycle	8.5	8.75	9	V	VBST
f_{SW_BOOST}	Switching frequency	34 cycles of 16 MHz main clock		470.6		KHz	BSTSW
I_{BSTSW_LEAK}	BSTSW pin leakage current	From 0 V to MAX voltage pin	-1.2		1.2	µA	BSTSW
V_{BSTSW}	Boost gate voltage			V_{VBST_TH}		V	BSTSW
I_{BOOST_SOURCE}	Boost driver source current	V_{VBST} = 8.5 V, V_{BSTSW} = 0 V	-80	-60	-40	mA	BSTSW

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
I_{BOOST_SINK}	Boost driver sink current	V_{VBST} = 8.5 V, V_{BSTSW} = 0 V	40	60	80	mA	BSTSW
$I_{BOOST_OVC_TH}$	Boost overcurrent detection Threshold current	Application info, shunt resistor R_{SBST} = 100 mΩ +/- 10%	2.7	2.9	3.1	A	BSTSS
$V_{BOOST_OVC_TH}$	Boost overcurrent detection Threshold voltage	Application info $I_{BOOST_OVC_TH}$ * R_{SBST}	270	290	310	mV	BSTSS
N_{OVC_TH}	Up/down OVC filter counter threshold			5		-	-
$V_{VBST_UV_TH}$	VBST undervoltage detection Threshold voltage		6.7	6.9	7.2	V	VBST
$V_{VBST_UV_HYS}$	VBST undervoltage detection Hysteresis voltage		370	400	450	mV	VBST
$T_{VBST_UV_FIL}$	VBST undervoltage detection Filter Time		5		15	µs	VBST
$V_{VBST_OV_TH}$	VBST overvoltage detection Threshold voltage	Boost OFF	28	30	32	V	VBST
$V_{VBST_OV_HYS}$	VBST overvoltage detection Hysteresis voltage		300		550	mV	VBST
$T_{VBST_OV_FIL}$	VBST overvoltage detection Filter time		5		15	µs	VBST
$T_{VBST_UV_BLK}$	VBST UV blanking time upon transition to NORMAL state	***Tested in SCAN***	1000		1500	µs	VBST
$M_{BST}_Q_G$	External FET M_{BST} gate charge	Application info		7		nC	VBST
$M_{BST}_C_{iss}$	External FET M_{BST} input capacitor	Application info		860		pF	VBST
$R_G_M_{BST}$	External FET M_{BST} gate serial resistor	Application info			10	Ω	VBST
R_{GBST}	External FET M_{BST} gate pull down resistor	Application info		220		kΩ	BSTSS BSTSW
R_{SBST}	External shunt resistor	Application info	-10%	100	+10%	mΩ	BSTSS BSTGND
C_{BST}	Output capacitance	Application info	-20%	18.8 (4*4.7)	+20%	µF	VBST
ESR_C_{BST}	Output capacitor ESR (for each capacitor)	Application info		3		mΩ	VBST

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
L_{BST}	Boost inductor	Application info	2.2	4.7	10	µH	VBST
DCR_L_{BST}	Inductor DC resistance	Application info		20	40	mΩ	VBST

4.3.3 Charge pump (VCP)

This charge pump:

- Is fed by **boost pre-regulator (VBST)** if active, otherwise by the reverse protected battery line **(VBP)**
- Feeds the internal analog circuitry for biasing of the **gate pre-drivers**
- Feeds the internal analog circuitry for biasing of the **cell balancing FETs (Sx)**
- Feeds the internal analog circuitry for biasing the stages executing the voltage conversion routine

4.3.3.1 Diagnostics

The charge pump is equipped with UV/OV detection, available both in NORMAL and STANDBY state according to the VCP_DIAG_DIS bit (default VCP_DIAG_DIS = 0). These diagnostics can be enabled or disabled by setting VCP_DIAG_DIS in NORMAL state via an SPI command.

Table 14. Charge pump diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
CP undervoltage	• If the V_{VCP} voltage falls below $V_{VCP_UV_TH}$ for an interval longer than $T_{VCP_UV_FIL}$, the VCP_UV fault is acknowledged.	• The VCP_UV flag is set • If in STANDBY, the IC moves to NORMAL and FSO1, FSO2 lines are asserted • If in NORMAL, FSO1, FSO2 lines are asserted • Cell balancing FETs are kept OFF • Both group of CB MOSFETs are turned OFF	• If the V_{VCP} voltage rises above $V_{VCP_UV_TH}$ + $V_{VCP_UV_HYS}$ for an interval longer than $T_{VCP_UV_FIL}$, the VCP_UV flag can be cleared by MCU	• FSO1, FSO2 lines are released • Cell balancing FETs are released (if enabled) • One or both groups of CB back-to-back MOSFETs are turned ON (according to Table 70 (Pre-drivers driving commands), refer to Section 4.10.2 for details)	• When VCP_DIAG_DIS=1, the charge pump diagnostic is masked, the VCP_UV flag can always be cleared • Blanked during power-up sequence, until NORMAL state is reached from SLEEP state • VCP_UV_BAL_MSK=1 masks reaction on balancing
CP overvoltage	• If the V_{VCP} rises above $V_{VCP_OV_TH}$ for an interval longer than $T_{VCP_OV_FIL}$, the VCP_OV fault is acknowledged	• The VCP_OV flag is set • If in STANDBY, the IC moves to NORMAL and FSO1, FSO2 lines are asserted • If in NORMAL, FSO1, FSO2 lines are asserted	• If the V_{VCP} falls below $V_{VCP_OV_TH}$ - $V_{VCP_OV_HYS}$ for an interval longer than $T_{VCP_OV_FIL}$, the VCP_OV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• When VCP_DIAG_DIS=1, the charge pump diagnostic and reaction on pre-drivers are disabled. The VCP_OV flag can always be cleared

4.3.3.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 15. Charge pump electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{VCP}	Regulated voltage	V_{VBST} in OR	V_{VBST} + 6		V_{VBST} + 16	V	VCP
C_{TANK}	External tank capacitor	Application info	-10%	680	+10%	nF	VCP
C_{CP1}	External flying capacitor	Application info	-30%	33	+30%	nF	VFLY1 VFLY2
C_{CP2}	External flying capacitor	Application info	-30%	33	+30%	nF	VFLY3 VFLY4
f_{VCP}	Switching frequency	Design info		62.5		KHz	VCP
$V_{VCP_UV_TH}$	Charge pump UV threshold		V_{VBST} + 3.6		V_{VBST} + 5	V	VCP
$V_{VCP_UV_HYS}$	Charge pump UV threshold hysteresis		170		350	mV	VCP
$T_{VCP_UV_FIL}$	Charge pump UV filter time		10		15	µs	VCP
$V_{VCP_OV_TH}$	Charge pump OV threshold		V_{VBST}+15.5		V_{VBST}+20.5	V	VCP
$V_{VCP_OV_HYS}$	Charge pump OV threshold hysteresis		170	300	400	mV	VCP
$T_{VCP_OV_FIL}$	Charge pump OV filter time		10		15	µs	VCP
$T_{VCP_UV_BLK}$	VCP UV blanking time upon transition from SLEEP to NORMAL state			10		ms	VCP

4.3.4 Buck1 pre-regulator (VPRE)

This buck pre-regulator:

- Is fed by the **boost pre-regulator (VBST)** if active, otherwise by the reverse protected battery line **(VBP)**
- Feeds the **buck2 1.125 V-5 V regulator (VCORE)**
- Feeds the **3.3 V/5 V LDO1 (VCC)**
- Feeds the **5 V LDO2 (VCC CAN)**

The VPRE is a buck switching regulator controller with synchronous rectification, which contributes to high power efficiency. This regulator has a soft-start function to prevent the inrush current to the VPRE pin; it regulates the V_{VPRE} and guarantees the I_{VPRE_LIM} current limitation. To protect power stages from temperature overheat, a dedicated thermal sensor is present in the layout sensing FET temperature. If overtemperature is detected, the regulator is switched OFF and restarts with its power-up sequence after the fault disappears. In low power modes (SLEEP and STANDBY), the VPRE is switched OFF.

4.3.4.1 Diagnostics

The VPRE pre-regulator has a dedicated overvoltage, undervoltage and overtemperature diagnostics, available only in NORMAL state and listed in the following table.

Table 16. Buck pre-regulator diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VPRE overvoltage	• If V_{VPRE} rises above $V_{VPRE_OV_TH}$ for an interval longer than $T_{VPRE_OV_FIL}$, the VPRE_OV fault is acknowledged	• The VPRE_OV flag is set • FSO1, FSO2 lines are asserted	• If V_{VPRE} falls below $V_{VPRE_OV_TH}$ - $V_{VPRE_OV_HYS}$ for an interval longer than $T_{VPRE_OV_FIL}$, the VPRE_OV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• None
VPRE undervoltage	• If V_{VPRE} falls below $V_{VPRE_UV_TH}$ for an interval longer than $T_{VPRE_UV_FIL}$, the VPRE_UV fault is acknowledged	• The VPRE_UV flag is set • FSO1, FSO2 lines are asserted • Buck2 (VCORE), LDO1 (VCC) and LDO2 (VCC CAN) are turned OFF	• If V_{VPRE} rises above $V_{VPRE_UV_TH}$ + $V_{VPRE_UV_HYS}$ for an interval longer than $T_{VPRE_UV_FIL}$, the VPRE_UV flag can be cleared by MCU • Buck2 (VCORE), LDO1 (VCC) and LDO2 (VCC CAN) are turned ON	• FSO1, FSO2 lines are released	• Blanked during the power-up sequence, until NORMAL state is reached • VPRE_UV_MASK=1 masks diagnostic execution
VPRE overtemperature	• If $TEMP_{VPRE}$ rises above $TEMP_{VPRE_OT_TH}$ for an interval longer than $T_{VPRE_OT_FIL}$, the VPRE_OT fault is acknowledged	• The VPRE_OT flag is set • FSO1, FSO2 lines are asserted • Buck1 (VPRE), buck2 (VCORE), LDO1 (VCC) and LDO2 (VCC CAN) are turned OFF	• If $TEMP_{VPRE}$ falls below $TEMP_{VPRE_OT_TH}$ - $TEMP_{VPRE_OT_HYS}$ for an interval longer than $T_{VPRE_OT_FIL}$, the VPRE_OT flag can be cleared by MCU • Buck1 (VPRE), buck2 (VCORE), LDO1 (VCC) and LDO2 (VCC CAN) are turned ON	• FSO1, FSO2 lines are released	• None

4.3.4.2 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

(*) The output pin of the VPRE regulator is split into two pins VPRE_CC (to feed the VCC and VCC_CAN) and VPRE_CORE (to feed the VCORE). In terms of voltages, we still have $V_{VPRE_CC} = V_{VPRE_CORE} = V_{VPRE}$. Therefore, for simplicity, only the "VPRE" pin is referenced in the table.

Table 17. VPRE electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	UNIT	PIN (1)
V_{VPRE}	Regulated voltage	NORMAL, All operating lines and loads	6.3	6.5	6.7	V	VPRE
f_{SW_VPRE}	VPRE switching frequency			420		KHz	VPRESW

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	UNIT	PIN (1)
I_{VPRE_LOAD}	VPRE output load current				1	A	VPRE
I_{VPRE_LIM}	VPRE output current limitation	NORMAL, V_{VPRE} = 0V	1.3	1.55	1.8	A	VPRE
V_{VPRE_LOAD}	VPRE static load regulation voltage	Load current step: $I_{VPRE_LOAD} = 50mA \rightarrow 1A$	-10		10	mV	VPRE
V_{VPRE_LINE}	VPRE static line regulation voltage	Battery voltage step: $V_{VBST} = 6.9V \rightarrow 12V$	-10		10	mV	VPRE
$V_{VPRE_LOAD_TRAN}$	VPRE transient load regulation	Load current step: $I_{VPRE_LOAD} = 50mA \rightarrow 1A$ and back $\frac{dI}{dt} = 0.475\frac{A}{\mu s}$	-15		15	%	VPRE
$V_{VPRE_LINE_TRAN}$	VPRE transient line regulation	Battery voltage step: $V_{VBST} = 6.9V \rightarrow 12V$ and back $\frac{dV}{dt} = 0.1\frac{V}{\mu s}$	-5		5	%	VPRE
V_{VPRE_PSRR}	VPRE power supply rejection ratio	V_{VBST_NOISE} = 1.4 V_{pp}, f_{NOISE} = 470.6 KHz, guaranteed by design	38			dB	VPRE
$V_{VPRE_OV_TH}$	VPRE overvoltage detection Threshold voltage		7.8		8.4	V	VPRE
$V_{VPRE_UV_TH}$	VPRE undervoltage detection Threshold voltage		4.7		5.1	V	VPRE
$T_{VPRE_OV_FIL}$	VPRE overvoltage detection Filter time		10		20	µs	VPRE
$T_{VPRE_UV_FIL}$	VPRE undervoltage detection Filter time		10		20	µs	VPRE
$V_{VPRE_OV_HYS}$	VPRE overvoltage detection Hysteresis voltage		250		320	mV	VPRE
$V_{VPRE_UV_HYS}$	VPRE undervoltage detection Hysteresis voltage		210		250	mV	VPRE
$T_{VPRE_SOFT_START}$	VPRE soft start time	From 10% to 90% of V_{VPRE}, guaranteed by design I_{VPRE_LOAD} = 50 mA, C_{VPRE} = 20 µF	250	300	350	µs	VPRE
$T_{VPRE_UV_BLK}$	VPRE UV blanking time upon transition to NORMAL state		1200		2000	µs	VPRE
$TEMP_{VPRE_OT_TH}$	VPRE overtemperature detection Threshold voltage		180	190	200	°C	VPRE
$TEMP_{VPRE_OT_HYS}$	VPRE overtemperature detection Hysteresis voltage		5	6	7	°C	VPRE
$T_{VPRE_OT_FIL}$	VPRE overtemperature detection Filter time		2		72	µs	VPRE
η_{VPRE}	VPRE buck efficiency	Application info, using recommended BOM	85			%	
C_{VPRE}	VPRE External output capacitance (decoupling capacitors in parallel)	Application info	-10%	20 (2 * 10)	+10%	µF	VPRE
ESR_C_{VPRE}	Output capacitor ESR (for each capacitor)	Application info		4		mΩ	VPRE

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	UNIT	PIN (1)
L_{VPRE}	VPRE external output inductor	Application info	-20%	22	+20%	µH	VPRE VPRESW
DCR_L_{VPRE}	Inductor DC resistance	Application info	-20%	26.3	+20%	mΩ	VPRE VPRESW
C_{BT_VPRE}	VPRE External bootstrap capacitor	Application info	-20%	0.47	+20%	µF	BUCKBT VPRESW
$ESR_C_{BT_VPRE}$	Bootstrap capacitor ESR	Application info		10		mΩ	BUCKBT VPRESW

1. *The output pin of the VPRE regulator is split into two pins VPRE_CC (to feed the VCC and VCC_CAN) and VPRE_CORE (to feed the VCORE). In terms of voltages, we still have VVPRE_CC = VVPRE_CORE = VVPRE. Therefore, for simplicity, only the "VPRE" pin is referenced in the table.*

4.3.5 Buck2 regulator 1.125 V-5 V (VCORE)

This buck regulator:

- Is fed by **buck1 pre-regulator (VPRE)**
- Is used to feed the MCU core.
- Output could be set in the range (1.125 V-5 V)
- Can be used to feed the **digital output buffer supply**(VIO)

The VCORE is a synchronous buck regulator with integrated MOSFETs for core application. The frequency is fixed to 420 KHz, and it is based on a peak current mode loop. Soft-start and slope compensation (fixed slope) functions are available; the pulse-skip function is enabled by default. It is also equipped with a current limitation protection and protected against temperature overheat by means of overtemperature detection circuit.

In low power modes (SLEEP and STANDBY), the VCORE is switched OFF.

The regulator is equipped with a configuration pin, VCORESEL. By connecting an external resistance with the defined value between the VCORESEL pin and ground allows the selection of six regulated output voltages.

The VCORE voltage selection is performed at every transition from SLEEP to NORMAL MODE (refer to Section 4.1.6) in the $\mathbf{T_{VCORESEL_CONV}}$interval after the $\mathbf{T_{NVM_TRIM}}$ (defined in Section 4.17.2.1). The VCORE configuration is available for MCU readout via SPI through the VCORE_SEL_ECHO bit

Table 18. Selection resistor values

VCORE_SEL_ECHO	Conditions	Comment
000	VCORE_SEL pin shorted to GND	VCORE switched OFF, RST1 asserted
001	R_{SEL} = 10 KΩ ±1% (1)	V_{VCORE} = 1.125 V
010	R_{SEL} = 20 KΩ ±1% (1)	V_{VCORE} =1.2 V
011	R_{SEL} = 30 KΩ ±1% (1)	V_{VCORE} = 1.3 V
100	R_{SEL} = 39 KΩ ±1% (1)	V_{VCORE} = 1.5 V
101	R_{SEL} = 51 KΩ ±1% (1)	V_{VCORE} = 3.3 V
110	R_{SEL} = 68 KΩ ±1% (1)	V_{VCORE} = 5 V
111	VCORE_SEL pin open	VCORE switched OFF, RST1 asserted

1. *Customer must guarantee a proper dedicated ground connection at PCB level from GND of selection resistances to GND pin of the device to avoid unwanted ground shift that can affect conversion.*

Since the buck does not require an external resistor divider, the VCOREFB pin voltage $V_{VCOREFB}$ coincides with the regulated output voltage, named V_{VCORE}.

Application note: in case the VCORESEL pin is faulty, shorted to GND or open, the IC latches a permanent VCORE undervoltage, keeping the RST1 asserted (see Section 4.16.3).

4.3.5.1 *Diagnostics*

This buck is equipped with UV/OV/OT detection, available only in NORMAL state, and listed in the following table.

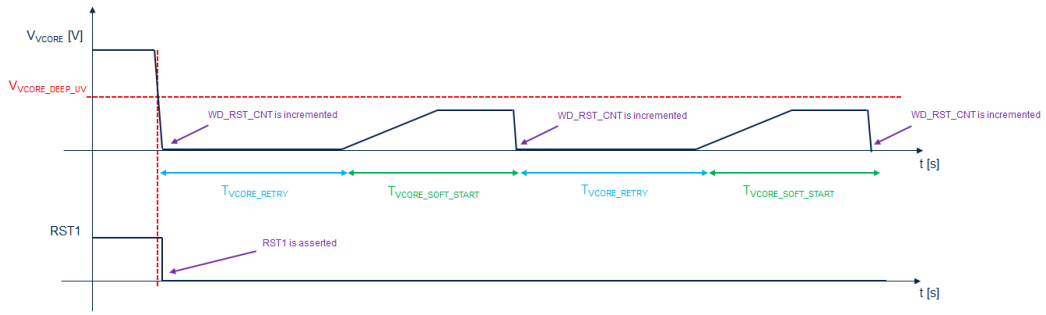
Table 19. VCORE regulator diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VCORE overvoltage	• If V_{VCORE} rises above $V_{VCORE_OV_TH}$ for an interval longer than $T_{VCORE_OV_FIL}$, the VCORE_OV fault is acknowledged	• The VCORE_OV flag is set • FSO1, FSO2 lines are asserted • VCORE is switched OFF • RST1 pin is asserted	• If V_{VCORE} falls below $V_{VCORE_OV_TH}$ - $V_{VCORE_OV_HYS}$ for an interval longer than $T_{VCORE_OV_FIL}$, the VCORE_OV flag can be cleared by MCU • VCORE is switched ON • RST1 pin is released after T_{RST1_LOW}	• FSO1, FSO2 lines are released	• None
VCORE undervoltage	• If V_{VCORE} falls below the $V_{VCORE_UV_TH}$ for an interval longer than $T_{VCORE_UV_FIL}$, the VCORE_UV fault is acknowledged	• The VCORE_UV flag is set • FSO1, FSO2 lines are asserted • RST1 pin is asserted	• If V_{VCORE} rises above $V_{VCORE_UV_TH}$ + $V_{VCORE_UV_HYS}$ for an interval longer than $T_{VCORE_UV_FIL}$, the VCORE_UV flag can be cleared by MCU • RST1 pin is released after T_{RST1_LOW}	• FSO1, FSO2 lines are released	• Blanked during power-up sequence, until NORMAL state is reached
VCORE deep undervoltage	• If V_{VCORE} falls below the $V_{VCORE_DEEP_UV_TH}$ for an interval longer than $T_{VCORE_DEEP_UV_FIL}$, the VCORE_DEEP_UV fault is acknowledged	• The VCORE_DEEP_UV flag is set • FSO1, FSO2 lines are asserted • VCORE is switched OFF • RST1 pin is asserted and WD_RST_CNT is incremented	• If V_{VCORE} rises above $V_{VCORE_DEEP_UV_TH}$ + $V_{VCORE_DEEP_UV_HYS}$ for an interval longer than $T_{VCORE_DEEP_UV_FIL}$, the VCORE_DEEP_UV flag can be cleared by MCU • VCORE is switched ON after the retry time T_{VCORE_RETRY} • RST1 pin is released after T_{RST1_LOW} from VCORE UV and VCORE_DEEP_UV disappear	• FSO1, FSO2 lines are released	• Blanked during power-up sequence, until NORMAL state is reached
VCORE overtemperature	• If $TEMP_{VCORE}$ rises above $TEMP_{VCORE_OT_TH}$ for an interval longer than $T_{VCORE_OT_FIL}$, the VCORE_OT fault is acknowledged	• The VCORE_OT flag is set • FSO1, FSO2 lines are asserted • VCORE is switched OFF • RST1 pin is asserted and WD_RST_CNT is incremented	• If $TEMP_{VCORE}$ falls below $TEMP_{VCORE_OT_TH}$ - $TEMP_{VCORE_OT_HYS}$ for an interval longer than $T_{VCORE_OT_FIL}$, the VCORE_OT flag can be cleared by MCU • VCORE is switched ON after the retry time T_{VCORE_RETRY} • RST1 pin is released after T_{RST1_LOW} from VCORE OT disappear and VCORE retry is completed	• FSO1, FSO2 lines are released	• None

In case of the VCORE_DEEP_UV or VCORE_OT, the VCORE is switched OFF for the T_{VCORE_RETRY} duration, the RST1 pin is asserted and the WD_RST_CNT is incremented. Then the VCORE is switched ON again for the $T_{VCORE_SOFT_START}$ time. If these faults occur multiple times and the WD_RST_CNT reaches WD_RST_CNT_MAX, the bit WD_RESET_LATCH is set, and the device moves to POWER DOWN state.

The value of the WD_RST_CNT is available for the MCU read out on WD_RST_CNT_STATUS in the WDT_STATUS_2 register. To reset this counter, if needed, the MCU can invoke a special key word by writing 0xFC in the special register 0x1D.

Figure 15. VCORE retry



4.3.5.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 20. VCORE electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{VCORE1}	Regulated voltage	Considering output voltage tolerance and ripple, R_{SEL} = 10 KΩ	1.09	1.125	1.16	V	VCOREFB
V_{VCORE2}	Regulated voltage	Considering output voltage tolerance and ripple, R_{SEL} = 20 KΩ	1.16	1.2	1.24	V	VCOREFB
V_{VCORE3}	Regulated voltage	Considering output voltage tolerance and ripple, R_{SEL} = 30 KΩ	1.26	1.3	1.34	V	VCOREFB
V_{VCORE4}	Regulated voltage	Considering output voltage tolerance and ripple, R_{SEL} = 39 KΩ	1.45	1.5	1.55	V	VCOREFB
V_{VCORE5}	Regulated voltage	Considering output voltage tolerance and ripple, R_{SEL} = 51 KΩ	3.25	3.3	3.35	V	VCOREFB
V_{VCORE6}	Regulated voltage	Considering output voltage tolerance and ripple, R_{SEL} = 68 KΩ	4.92	5	5.08	V	VCOREFB
$T_{VCORESEL_CONV}$	Time required for the VCORESEL voltage conversion only during SLEEP to NORMAL MODE transition.			1024		µs	VCORESEL
f_{SW_VCORE}	VCORE switching frequency			420		KHz	VCOREFB
V_{VCORE_LOAD}	VCORE static load regulation voltage	Load current step: $I_{VCORE_LOAD} = 10mA \rightarrow 750mA$	-6		6	mV	VCOREFB
V_{VCORE_LINE}	VCORE static line regulation voltage	V_{VPRE} voltage step: $V_{VPRE} = 6.5V \rightarrow 16.5V$	-6		6	mV	VCOREFB
$V_{VCORE_LOAD_TRAN}$	VCORE transient load regulation	Load current step: $I_{VCORE_LOAD} = 10mA \rightarrow 750mA$ and back $\frac{dI}{dt} = 1\frac{A}{\mu s}$	-5		5	%	VCOREFB

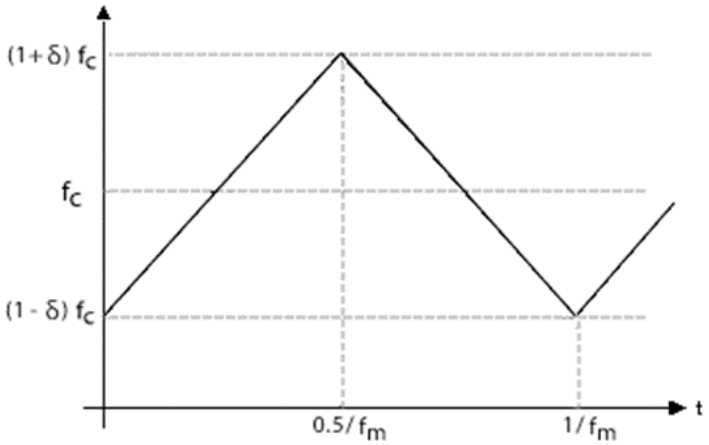
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{VCORE_LINE_TRAN}$	VCORE transient line regulation	V_{VPRE} voltage step: $V_{VPRE} = 6.5V \rightarrow 16.5V$ and back $\frac{dV}{dt} = 10\frac{V}{\mu s}$	-5		5	%	VCOREFB
V_{VCORE_PSRR}	VCORE power supply rejection ratio	V_{VPRE_NOISE} = 700 mV_{pp}, f_{NOISE} = 420 KHz, guaranteed by design	50			dB	VCOREFB
I_{VCORE_LOAD}	VCORE output load current		0.01		1	A	VCOREFB
I_{VCORE_LIM}	VCORE output current limitation	NORMAL, V_{VCORE} = 0 V	1.29	1.5	1.65	A	VCOREFB
η_{VCORE1}	VCORE buck efficiency	Application info, using recommended BOM V_{VCORE1} = 1.125 V	70			%	VCOREFB
η_{VCORE2}	VCORE buck efficiency	Application info, using recommended BOM V_{VCORE2} = 1.2 V	70			%	VCOREFB
η_{VCORE3}	VCORE buck efficiency	Application info, using recommended BOM V_{VCORE3} = 1.3 V	70			%	VCOREFB
η_{VCORE4}	VCORE buck efficiency	Application info, using recommended BOM V_{VCORE4} = 1.5 V	75			%	VCOREFB
η_{VCORE5}	VCORE buck efficiency	Application info, using recommended BOM V_{VCORE5} = 3.3 V	85			%	VCOREFB
η_{VCORE6}	VCORE buck efficiency	Application info, using recommended BOM V_{VCORE6} = 5 V	90			%	VCOREFB
$V_{VCORE_OV_TH}$	VCORE overvoltage detection Threshold voltage		V_{VCORE} * 1.11	V_{VCORE} * 1.15	V_{VCORE} * 1.19	V	VCOREFB
$V_{VCORE_UV_TH}$	VCORE undervoltage detection Threshold voltage		V_{VCORE} * 0.86	V_{VCORE} * 0.9	V_{VCORE} * 0.95	V	VCOREFB
$V_{VCORE_DEEP_UV_TH}$	VCORE deep undervoltage detection Threshold voltage		V_{VCORE} * 0.59	V_{VCORE} * 0.6	V_{VCORE} * 0.65	V	VCOREFB
$T_{VCORE_OV_FIL}$	VCORE overvoltage detection Filter time		15		25	µs	VCOREFB
$T_{VCORE_UV_FIL}$	VCORE undervoltage detection Filter time		15		25	µs	VCOREFB
$T_{VCORE_DEEP_UV_FIL}$	VCORE deep undervoltage detection Filter time		15		25	µs	VCOREFB
$V_{VCORE_OV_HYS}$	VCORE overvoltage detection Hysteresis voltage		2		2.4	%	VCOREFB

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{VCORE_UV_HYS}$	VCORE undervoltage detection Hysteresis voltage		2.5		2.8	%	VCOREFB
$V_{VCORE_DEEP_UV_HYS}$	VCORE deep undervoltage detection Hysteresis voltage		3.2		4	%	VCOREFB
T_{VCORE_RETRY}	VCORE shutdown duration before it is automatically switched ON following VCORE_DEEP_UV or VCORE_OT detection		1		2	ms	VCOREFB
$T_{VCORE_UV_BLK}$	VCORE UV blanking time upon transition to NORMAL state		1600		2200	µs	VCOREFB
$T_{VCORE_SOFT_START}$	VCORE soft start time	From 10% to 90% of V_{VCORE}, guaranteed by design I_{VCORE_LOAD} = 10 mA, C_{VCORE} = 68 µF	0.9		1.6	ms	VCOREFB
$TEMP_{VCORE_OT_TH}$	VCORE overtemperature detection threshold		180	190	200	°C	VCOREFB
$TEMP_{VCORE_OT_HYS}$	VCORE Overtemperature detection hysteresis		5	6	7	°C	VCOREFB
$T_{VCORE_OT_FIL}$	VCORE overtemperature detection Filter time		2		72	µs	VCOREFB
L_{VCORE}	VCORE external coil	Application info	-20%	22	+20%	µH	VCORESW VCOREFB
DCR_L_{VCORE}	Inductor DC resistance	Application info		135	149	mΩ	VCORESW VCOREFB
C_{VCORE}	VCORE external output capacitor	Application info	-20%	68	+20%	µF	VCOREFB
ESR_C_{VCORE}	Output capacitor ESR	Application info		1		mΩ	VCOREFB

4.3.6 Spread spectrum modulation

The IC implements a frequency modulation of the switching frequency f_{SW_VPRE} and f_{SW_VCORE} of VPRE and VCORE buck regulators.

Figure 16. **Spread spectrum modulation waveform**



The spread spectrum modulation (SSM) function allows to reduce the emission around frequency f_C = f_{SW_VPRE} = f_{SW_VCORE} = 420 KHz that is modulated by a triangular signal with frequency fm and spreading range δ.

The SSM can be enabled in NORMAL MODE by setting via SPI, the dedicated bit CLK_SS_BUCK_EN as follows:

- if CLK_SS_BUCK_EN = 0, SSM disabled (Default)
- if CLK_SS_BUCK_EN = 1, SSM enabled

4.3.6.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 21. **SSM electrical parameters**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
δ	Spread spectrum modulation spreading range		1.5		3	%
f_m	Spread spectrum modulation frequency			9.4		KHz

4.3.7 3.3 V/5 V LDO1 (VCC)

This LDO:

- Is fed by **buck1 pre-regulator (VPRE)**
- Is used to feed the MCU ADCs
- Can be used to feed the **digital output buffer supply (**VIO)
- Can be configured by the VCCSEL pin:
  - if VCCSEL = 0, which is the pin is connected to AGND, V_{VCC} = 3.3 V
  - if VCCSEL = 1, which is the pin is connected to VPRE_CC pin, V_{VCC} = 5V

This regulator has a soft-start function to prevent the inrush current to the VCC pin; it regulates the V_{VCC} and guarantees I_{VCC_LOAD} output current capability and I_{VCC_LIM} current limitation. It is also protected against temperature overheating by means of overtemperature detection circuit. In low power modes (SLEEP and STANDBY), the VCC is switched OFF. The VCC configuration (VCCSEL_ECHO) is latched during the transition from SLEEP to NORMAL MODE (refer to Section 4.1.6) and it is available for the MCU readout. The external connection of the VCCSEL pin is figured in Section 4.12.11.

4.3.7.1 *Diagnostics*

This LDO is equipped with the UV/OV/OT detection, available only in NORMAL state and listed in the following table.

Table 22. VCC LDO1 diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VCC undervoltage	• If V_{VCC} falls below $V_{VCC_UV_TH}$ for an interval longer than $T_{VCC_UV_FIL}$, the VCC_UV fault is acknowledged	• The VCC_UV flag is set • FSO1, FSO2 lines are asserted	• If V_{VCC} rises above $V_{VCC_UV_TH}$ + $V_{VCC_UV_HYS}$ for an interval longer than $T_{VCC_UV_FIL}$, the VCC_UV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• Blanked during power-up sequence, until NORMAL state is reached
VCC overvoltage	• If V_{VCC} rises above $V_{VCC_OV_TH}$ for an interval longer than $T_{VCC_OV_FIL}$, the VCC_ OV fault is acknowledged	• The VCC_OV flag is set • FSO1, FSO2 lines are asserted	• If V_{VCC} falls below $V_{VCC_OV_TH}$ - $V_{VCC_OV_HYS}$ for an interval longer than $T_{VCC_OV_FIL}$, the VCC_OV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• None
VCC overtemperature	• If $TEMP_{VCC}$ rises above $TEMP_{VCC_OT_TH}$ for an interval longer than $T_{VCC_OT_FIL}$, the VCC_OT fault is acknowledged	• The VCC_OT flag is set • FSO1, FSO2 lines are asserted • VCC is switched OFF	• If $TEMP_{VCC}$ falls below $TEMP_{VCC_OT_TH}$ - $TEMP_{VCC_OT_HYS}$ for an interval longer than $T_{VCC_OT_FIL}$, the VCC_OT flag can be cleared by MCU • VCC is switched ON	• FSO1, FSO2 lines are released	• None

4.3.7.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 23. VCC LDO1 electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{VCC1}	Regulated voltage with VCCSEL = 1	NORMAL, All operating lines and loads	-1%	5	+1%	V	VCC
V_{VCC0}	Regulated voltage with VCCSEL = 0	NORMAL, All operating lines and loads	-1%	3.3	+1%	V	VCC
I_{VCC_LOAD}	VCC output load current		0.01		250	mA	VCC
I_{VCC_LIM}	VCC output current limitation	NORMAL, V_{VCC} = 0 V	270		450	mA	VCC
$T_{VCC_SOFT_START}$	VCC soft start time	From 10% to 90% of V_{VCC}, guaranteed by design I_{VCC_LOAD} = 10 mA, C_{VCC} = 10 µF	150		450	µs	VCC
V_{VCC_LOAD}	VCC static load regulation voltage	Load current step: $I_{VCC_LOAD} = 10mA \rightarrow 250mA$			15	mV	VCC
V_{VCC_LINE}	VCC static line regulation voltage	V_{VPRE} voltage step: $V_{VPRE} = 6.5V \rightarrow 16.5V$			15	mV	VCC
$V_{VCC_LOAD_TRAN}$	VCC transient load regulation	Load current step: $I_{VCC_LOAD} = 10mA \rightarrow 250mA$ and back $\frac{dI}{dt} = 10\frac{mA}{\mu s}$	-8.5		8.5	%	VCC

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{VCC_LINE_TRAN}$	VCC transient line regulation	V_{VPRE} voltage step: $V_{VPRE} = 6.5V \rightarrow 16.5V$ and back $\frac{dV}{dt} = 10\frac{V}{\mu s}$	-5		5	%	VCC
V_{VCC_PSRR}	VCC power supply rejection ratio	V_{VPRE_NOISE} = 100 mV_{pp}, f_{NOISE} = 400 KHz, guaranteed by design	40			dB	VCC
$V_{VCC1_UV_TH}$	VCC1 undervoltage detection threshold	Rail 5 V	V_{VCC1} * 0.88		V_{VCC1} * 0.945	V	VCC
$V_{VCC1_OV_TH}$	VCC1 overvoltage detection threshold	Rail 5 V	V_{VCC1} * 1.09		V_{VCC1} * 1.20	V	VCC
$V_{VCC0_UV_TH}$	VCC0 undervoltage detection threshold	Rail 3. 3V	V_{VCC0} * 0.88		V_{VCC0} * 0.945	V	VCC
$V_{VCC0_OV_TH}$	VCC0 overvoltage detection threshold	Rail 3.3 V	V_{VCC0} * 1.12		V_{VCC0} * 1.23	V	VCC
$V_{VCC1_OV_HYS}$	VCC1 overvoltage detection Hysteresis voltage	Rail 5 V	50		100	mV	VCC
$V_{VCC0_OV_HYS}$	VCC0 overvoltage detection Hysteresis voltage	Rail 3.3 V	35		65	mV	VCC
$V_{VCC1_UV_HYS}$	VCC1 undervoltage detection Hysteresis voltage	Rail 5 V	90		130	mV	VCC
$V_{VCC0_UV_HYS}$	VCC0 undervoltage detection Hysteresis voltage	Rail 3.3 V	70		100	mV	VCC
$T_{VCC_OV_FIL}$	VCC OV detection Filter time		60		100	µs	VCC
$T_{VCC_UV_FIL}$	VCC UV detection Filter time		60		100	µs	VCC
$T_{VCC_UV_BLK}$	VCC UV blanking time upon transition to NORMAL state		1.3		2.0	ms	VCC
$TEMP_{VCC_OT_TH}$	VCC overtemperature detection threshold		180	190	200	°C	VCC
$TEMP_{VCC_OT_HYS}$	VCC overtemperature detection hysteresis		5	6	7	°C	VCC
$T_{VCC_OT_FIL}$	VCC overtemperature detection Filter time		2		72	µs	VCC
C_{VCC}	External output capacitor	Application info	-20%	10	+20%	µF	VCC
ESR_C_{VCC}	Output capacitor ESR	Application info		5		mΩ	VCC

4.3.8 5V LDO2 (VCC CAN)

This LDO:

- Is fed by **buck1 pre-regulator (VPRE)**
- Is used to feed the external CAN.

This regulator has a soft-start function to prevent the inrush current to VCC CAN pin; it regulates the V_{VCC_CAN} and guarantees the $I_{VCC_CAN_LOAD}$ output current capability and the $I_{VCC_CAN_LIM}$ current limitation. It is also protected against temperature overheating by means of overtemperature detection circuit. In low power modes (SLEEP and STANDBY), VCC CAN is switched OFF.

4.3.8.1 *Diagnostics*

This LDO is equipped with the UV/OV/OT detection, available only in NORMAL state and listed in the following table.

Table 24. VCC CAN LDO2 diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VCC CAN undervoltage	• If V_{VCC_CAN} falls below $V_{VCC_CAN_UV_TH}$ for an interval longer than $T_{VCC_CAN_UV_FIL}$, the VCC_CAN_UV fault is acknowledged	• The VCC_CAN_UV flag is set • FSO1, FSO2 lines are asserted	• If V_{VCC_CAN} rises above $V_{VCC_CAN_UV_TH}$ + $V_{VCC_CAN_UV_HYS}$ for an interval longer than $T_{VCC_CAN_UV_FIL}$, the VCC_CAN_UV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• Blanked during power-up sequence, until NORMAL state is reached
VCC CAN overvoltage	• If V_{VCC_CAN} rises above $V_{VCC_CAN_OV_TH}$ for an interval longer than $T_{VCC_CAN_OV_FIL}$, the VCC_CAN_OV fault is acknowledged	• The VCC_CAN_OV flag is set • FSO1, FSO2 lines are asserted	• If V_{VCC_CAN} falls below $V_{VCC_CAN_OV_TH}$ - $V_{VCC_CAN_OV_HYS}$ for an interval longer than $T_{VCC_CAN_OV_FIL}$, the VCC_CAN_OV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• None
VCC CAN overtemperature	• If $TEMP_{VCC_CAN}$ rises above $TEMP_{VCC_CAN_OT_TH}$ for an interval longer than $T_{VCC_CAN_OT_FIL}$, the VCC_CAN_OT fault is acknowledged	• The VCC_CAN_OT flag is set • FSO1, FSO2 lines are asserted • VCC_CAN is switched OFF	• If $TEMP_{VCC_CAN}$ falls below $TEMP_{VCC_CAN_OT_TH}$ - $TEMP_{VCC_CAN_OT_HYS}$ for an interval longer than $T_{VCC_CAN_OT_FIL}$, the VCC_CAN_OT flag can be cleared by MCU • VCC_CAN is switched ON	• FSO1, FSO2 lines are released	• None

4.3.8.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 25. VCC CAN LDO2 electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{VCC_CAN}	Regulated voltage	NORMAL, All operating lines and loads	-5%	5	+5%	V	VCC CAN
$I_{VCC_CAN_LOAD}$	VCC CAN output load current		0.01		150	mA	VCC CAN
$I_{VCC_CAN_LIM}$	VCC CAN output current limitation	NORMAL, V_{VCC_CAN} = 0 V	160		300	mA	VCC CAN
$T_{VCC_CAN_SOFT_START}$	VCC CAN soft start time	From 10% to 90% of V_{VCC_CAN}, guaranteed by design $I_{VCC_CAN_LOAD}$ = 10 mA, C_{VCC_CAN} = 10 µF	150		450	µs	VCC CAN
$V_{VCC_CAN_LOAD}$	VCC CAN static load regulation voltage	Load current step: $I_{VCC_CAN_LOAD} = 10mA \rightarrow 150mA$			20	mV	VCC CAN
$V_{VCC_CAN_LINE}$	VCC CAN static line regulation voltage	V_{VPRE} voltage step: $V_{VPRE} = 6.5V \rightarrow 16.5V$			15	mV	VCC CAN

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{VCC_CAN_LOAD_TRAN}$	VCC CAN transient load regulation	Load current step: $I_{VCC_CAN_LOAD} = 10mA \rightarrow 75mA$ and back $\frac{dI}{dt} = 10\frac{mA}{\mu s}$	-5		5	%	VCC CAN
$V_{VCC_CAN_LINE_TRAN}$	VCC CAN transient line regulation	V_{VPRE} voltage step: $V_{VPRE} = 6.5V \rightarrow 16.5V$ and back $\frac{dV}{dt} = 10\frac{V}{\mu s}$	-5		5	%	VCC CAN
$V_{VCC_CAN_PSRR}$	VCC CAN power supply rejection ratio	V_{VPRE_NOISE} = 100 mV_{pp}, f_{NOISE} = 400 KHz, guaranteed by design	30			dB	VCCCAN
$V_{VCC_CAN_OV_TH}$	VCC CAN overvoltage detection threshold		V_{VCC_CAN} *1.08		V_{VCC_CAN} *1.16	V	VCC CAN
$V_{VCC_CAN_UV_TH}$	VCC CAN undervoltage detection threshold		V_{VCC_CAN}*0.88		V_{VCC_CAN} *0.95	V	VCC CAN
$V_{VCC_CAN_OV_HYS}$	VCC CAN overvoltage detection Hysteresis voltage		50		100	mV	VCC CAN
$V_{VCC_CAN_UV_HYS}$	VCC CAN undervoltage detection Hysteresis voltage		90		130	mV	VCC CAN
$T_{VCC_CAN_OV_FIL}$	VCC CAN OV detection Filter time		60		100	µs	VCC CAN
$T_{VCC_CAN_UV_FIL}$	VCC CAN UV detection Filter time		60		100	µs	VCC CAN
$T_{VCC_CAN_UV_BLK}$	VCC CAN UV blanking time upon transition to NORMAL state		1.3		2.0	ms	VCCCAN
$TEMP_{VCC_CAN_OT_TH}$	VCC CAN overtemperature detection threshold		180	190	200	°C	VCC CAN
$TEMP_{VCC_CAN_OT_HYS}$	VCC CAN overtemperature detection hysteresis		5	6	7	°C	VCC CAN
$T_{VCC_CAN_OT_FIL}$	VCC CAN overtemperature detection Filter time		2		72	µs	VCC CAN
C_{VCC_CAN}	External output capacitor	Application info	-20%	10	+20%	µF	VCCCAN
$ESR_C_{VCC_CAN}$	Output capacitor ESR	Application info		5		mΩ	VCCCAN

4.3.9 5 V thermistor bias LDO3 (VTREF)

This LDO:

- Is fed by the **boost pre-regulator (VBST)** if active, otherwise by the reverse protected battery line **(VBP)**
- Is used for biasing external NTCs via pull-up resistors

This regulator is switched OFF in SLEEP MODE, while in STANDBY MODE it is cyclically activated for a time interval T_{VTREF_ON} in the period T_{VTREF} defined by the internal RTC.

Due to this, the cell temperature monitor (Section 4.4.4), the GPIO absolute conversion (Section 4.4.5), and the open load diagnostics (Section 4.4.3, Section 4.4.6, Section 4.4.7) shall be performed within the T_{VTREF_ON}. Therefore, considering the $T_{ADCV_CYCLIC_ON} = T_{WAKE} + 8*(T_{ADCV_START} + T_{ADCV_FILTER})+2*T_{ADCV_CAL}$ defined in Section 4.4, it must be $T_{VTREF_ON} > T_{ADCV_CYCLIC_ON}$.

4.3.9.1 *Diagnostics*

This LDO is equipped with the UV/OV/OT detection, available both in NORMAL and STANDBY state and listed in the following table, and short-circuit protection.

Table 26. VTREF diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VTREF undervoltage	• If the V_{VTREF} voltage falls below $V_{VTREF_UV_TH}$ for an interval longer than $T_{VTREF_UV_FIL}$, the VTREF_UV fault is acknowledged.	• The VTREF_UV flag is set • If in STANDBY, the IC moves to NORMAL and FSO1, FSO2 lines are asserted • If in NORMAL, FSO1, FSO2 lines are asserted	• If the V_{VTREF} voltage rises above $V_{VTREF_UV_TH}$ + $V_{VTREF_UV_HYS}$ for an interval longer than $T_{VTREF_UV_FIL}$, the VTREF_UV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• Blanked during power-up sequence, until NORMAL state is reached from SLEEP state • Blanked during its power-up when cyclically activated in STANDBY state
VTREF overvoltage	• If the V_{VTREF} voltage rises above $V_{VTREF_OV_TH}$ for an interval longer than $T_{VTREF_OV_FIL}$, the VTREF_OV fault is acknowledged.	• The VTREF_OV flag is set • If in STANDBY, the IC moves to NORMAL and FSO1, FSO2 lines are asserted • If in NORMAL, FSO1, FSO2 lines are asserted	• If the V_{VTREF} voltage falls below $V_{VTREF_OV_TH}$ - $V_{VTREF_OV_HYS}$ for an interval longer than $T_{VTREF_OV_FIL}$, the VTREF_OV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• None
VTREF overtemperature	• If the $TEMP_{VTREF}$ rises above $TEMP_{VTREF_OT_TH}$ for an interval longer than $T_{VTREF_OT_FIL}$, the VTREF_OT fault is acknowledged	• The VTREF_OT flag is set • If in STANDBY, the IC moves to NORMAL and FSO1, FSO2 lines are asserted • If in NORMAL, FSO1, FSO2 lines are asserted • VTREF is switched OFF	• If the $TEMP_{VTREF}$ falls below $TEMP_{VTREF_OT_TH}$ - $TEMP_{VTREF_OT_HYS}$ for an interval longer than $T_{VTREF_OT_FIL}$, the VTREF_OT flag can be cleared by MCU • VTREF is switched ON	• FSO1, FSO2 lines are released	• None

4.3.9.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2, 6 V < V_{VBST} < 40 V; T_J according to the operating range in Table 5.

Table 27. VTREF electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{VTREF_NORMAL}	Regulated voltage in NORMAL	NORMAL, All operating lines and loads	-5%	5	+5%	V	VTREF
$V_{VTREF_STANDBY}$	Regulated voltage in STANDBY	STANDBY	-6%	5	+6%	V	VTREF
T_{VTREF}	VTREF time period	STANDBY, defined by internal RTC		$T_{CYCLE_STANDBY}$		s	VTREF
D_{VTREF_ON}	VTREF duty cycle	STANDBY, $T_{VTREF_ON} = T_{VTREF} * D_{VTREF_ON}$		$T_{VTREF_ON} / T_{CYCLE_STANDBY}$		-	VTREF
I_{VTREF_LOAD}	VTREF output load current		0.01		10	mA	VTREF
I_{VTREF_LIM}	VTREF output current limitation	NORMAL, V_{VTREF} = 0 V	80		220	mA	VTREF
V_{VTREF_LOAD}	VTREF static load regulation voltage	Load current step: $I_{VTREF_LOAD} = 10\mu A \rightarrow 10.01mA$			100	mV	VTREF
V_{VTREF_LINE}	VTREF static line regulation voltage	Battery voltage step: $V_{VBST} = 6V \rightarrow 20V$			100	mV	VTREF
$V_{VTREF_LOAD_TRAN}$	VTREF transient load regulation	Load current step: $I_{VTREF_LOAD} = 10\mu A \rightarrow 10.01mA$ and back $\frac{dI}{dt} = 1\frac{A}{\mu s}$	-5		5	%	VTREF
$V_{VTREF_LINE_TRAN}$	VTREF transient line regulation	Battery voltage step: $V_{VBST} = 6V \rightarrow 20V$ and back $\frac{dV}{dt} = 10\frac{V}{\mu s}$	-5		5	%	VTREF
V_{VTREF_PSRR}	VTREF power supply rejection ratio	V_{VBST_NOISE} = 100 mV_{pp}, f_{NOISE} = 400 KHz, guaranteed by design	40			dB	VTREF
$T_{VTREF_SOFT_START}$	VTREF soft start time	From 10% to 90% of V_{VTREF}, guaranteed by design I_{VTREF_LOAD} = 10 mA, C_{VTREF} = 2 µF	150		450	µs	VTREF
$V_{VTREF_OV_TH}$	VTREF overvoltage detection threshold		V_{VTREF} * 1.07		V_{VTREF} * 1.19	V	VTREF
$V_{VTREF_UV_TH}$	VTREF undervoltage detection threshold		V_{VTREF} * 0.85		V_{VTREF} * 0.96	V	VTREF

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{VTREF_OV_HYS}$	VTREF overvoltage detection Hysteresis voltage		60		120	mV	VTREF
$V_{VTREF_UV_HYS}$	VTREF undervoltage detection Hysteresis voltage		60		110	mV	VTREF
$T_{VTREF_OV_FIL}$	VTREF OV detection Filter time		60		100	µs	VTREF
$T_{VTREF_UV_FIL}$	VTREF UV detection Filter time		60		100	µs	VTREF
$T_{VTREF_UV_BLK}$	VTREF UV blanking time upon transition from SLEEP to NORMAL state and during cyclic activation in STANDBY state		1.3		2.0	ms	VTREF
$TEMP_{VTREF_OT_TH}$	VTREF overtemperature detection threshold		180	190	200	°C	VTREF
$TEMP_{VTREF_OT_HYS}$	VTREF overtemperature detection hysteresis		5	6	7	°C	VTREF
$T_{VTREF_OT_FIL}$	VTREF overtemperature detection Filter time		2		72	µs	VTREF
C_{VTREF}	External output capacitance	Application info	-30%	2 (2 * 1)	+30%	µF	VTREF
ESR_C_{VTREF}	Output capacitor ESR (for each capacitor)	Application info			15	mΩ	VTREF

4.3.10 3.3 V/5 V standby LDO4 (VSTBY)

This LDO:

- Is fed by the **boost pre-regulator (VBST)** if active, otherwise by the reverse protected battery line **(VBP)**
- Feeds the **external** real time clock
- Can be used to feed the **digital output buffer supply (VIO)**
- Is disabled by default (according to VSTBY_EN bit) and enabled via SPI during NORMAL MODE
- Is configured via SPI using the VSTBY_SEL bit:
  - if VSTBY_SEL = 0 (default), V_{VSTBY} = 3.3 V
  - if VSTBY_SEL = 1, V_{VSTBY} = 5 V

This regulator is switched OFF in SLEEP MODE and POWER DOWN MODE. The first power up (refer to Section 4.1.6.1) is performed with VSTBY disabled (VSTBY_EN = 0). In NORMAL MODE, if an external RTC is connected to the VSTBY pin, MCU can first configure VSTBY_SEL and then enable the regulator by setting VSTBY_EN = 1. The NVM upload of the configuration of the LDO4 can be performed at the end of the first full configuration of the device by the MCU. After the NVM upload with VSTBY_EN = 1 and VSTBY_SEL properly configurated, all the future power-ups are performed with automatic VSTBY enabling, with configured setpoint 3.3 V or 5 V (refer to Section 4.1.6.5). It is also protected against temperature overheating by means of overtemperature detection circuit.

4.3.10.1 *Diagnostics*

This LDO is equipped with UV/OV/OT detection, available both in NORMAL and STANDBY state and listed in the following table.

Table 28. VSTBY diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VSTBY Undervoltage	• If the V_{VSTBY} voltage falls below $V_{VSTBY_UV_TH}$ for an interval longer than $T_{VSTBY_UV_FIL}$, the VSTBY_UV fault is acknowledged.	• The VSTBY_UV flag is set • If in STANDBY, the IC moves to NORMAL and FSO1, FSO2 lines are asserted • If in NORMAL, FSO1, FSO2 lines are asserted	• If the V_{VSTBY} voltage rises above $V_{VSTBY_UV_TH}$ + $V_{VSTBY_UV_HYS}$ for an interval longer than $T_{VSTBY_UV_FIL}$, the VSTBY_UV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• Blanked during power-up sequence, until NORMAL state is reached from SLEEP state • When VSTBY_EN=0, the VSTBY diagnostic is masked, the VSTBY_UV flag can always be cleared
VSTBY Overvoltage	• If the V_{VSTBY} voltage rises above $V_{VSTBY_OV_TH}$ for an interval longer than $T_{VSTBY_OV_FIL}$, the VSTBY_ OV fault is acknowledged	• The VSTBY_ OV flag is set • If in STANDBY, the IC moves to NORMAL and FSO1, FSO2 lines are asserted • If in NORMAL, FSO1, FSO2 lines are asserted	• If the V_{VSTBY} voltage falls below $V_{VSTBY_OV_TH}$ - $V_{VSTBY_OV_HYS}$ for an interval longer than $T_{VSTBY_OV_FIL}$, the VSTBY_ OV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• When VSTBY_EN=0, the VSTBY diagnostic is masked, the VSTBY_OV flag can always be cleared
VSTBY Overtemperature	• If $TEMP_{VSTBY}$ rises above $TEMP_{VSTBY_OT_TH}$ for an interval longer than $T_{VSTBY_OT_FIL}$, the VSTBY_OT fault is acknowledged	• The VSTBY_OT flag is set • If in STANDBY, the IC moves to NORMAL and FSO1, FSO2 lines are asserted • If in NORMAL, FSO1, FSO2 lines are asserted • VSTBY is switched OFF	• If $TEMP_{VSTBY}$ falls below $TEMP_{VSTBY_OT_TH}$ - $TEMP_{VSTBY_OT_HYS}$ for an interval longer than $T_{VSTBY_OT_FIL}$, the VSTBY_OT flag can be cleared by MCU • VSTBY is switched ON	• FSO1, FSO2 lines are released	• When VSTBY_EN=0, the VSTBY diagnostic is masked, the VSTBY_OT flag can always be cleared

4.3.10.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2, 6 V < V_{VBST} < 40 V; T_J according to the operating range in Table 5.

Table 29. VSTBY electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{VSTBY0}	Regulated voltage		3.201	3.3	3.399	V	VSTBY
V_{VSTBY1}	Regulated voltage		4.85	5	5.15	V	VSTBY
I_{VSTBY_LOAD}	Output load current		0.0005		10	mA	VSTBY
I_{VSTBY_LIM}	Output current limitation	NORMAL, V_{VSTBY} = 0 V	85		185	mA	VSTBY
V_{VSTBY_LOAD}	VSTBY static Load regulation voltage	Load current step: $I_{VSTBY_LOAD} = 10\mu A \rightarrow 10.01mA$			100	mV	VSTBY
V_{VSTBY_LINE}	VSTBY static line regulation voltage	Battery voltage step: $V_{VBST} = 6V \rightarrow 20V$			100	mV	VSTBY
$V_{VSTBY_LOAD_TRAN}$	VSTBY transient load regulation	Load current step: $I_{VSTBY_LOAD} = 10\mu A \rightarrow 10.01mA$ and back $\frac{dI}{dt} = 1\frac{A}{\mu s}$	-5		5	%	VSTBY
$V_{VSTBY_LINE_TRAN}$	VSTBY transient line regulation	Battery voltage step: $V_{VBST} = 6V \rightarrow 20V$ and back $\frac{dV}{dt} = 10\frac{V}{\mu s}$	-5		5	%	VSTBY
V_{VSTBY_PSRR}	VSTBY power supply rejection ratio	V_{VBST_NOISE} = 100 mV_{pp}, f_{NOISE} = 400 KHz, Guaranteed by design	40			dB	VSTBY
$T_{VSTBY_SOFT_START}$	VSTBY soft start time	From 10% to 90% of V_{VSTBY}. Guaranteed by design I_{VSTBY_LOAD} = 10 mA, C_{VSTBY}= 4.7 µF	150		430	µs	VSTBY

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{VSTBY0_UV_TH}$	VSTBY0 undervoltage detection threshold	Rail 3.3 V	V_{VSTBY0}* 0.75		V_{VSTBY0}* 0.90	V	VSTBY
$V_{VSTBY1_UV_TH}$	VSTBY1 undervoltage detection threshold	Rail 5 V	V_{VSTBY1}* 0.70		V_{VSTBY1}* 0.87	V	VSTBY
$T_{VSTBY_UV_FIL}$	VSTBY UV detection filter time in NORMAL state		15		25	µs	VSTBY
$V_{VSTBY0_UV_HYS}$	VSTBY0 undervoltage detection Hysteresis voltage	Rail 3.3 V	40		80	mV	VSTBY
$V_{VSTBY1_UV_HYS}$	VSTBY1 undervoltage detection Hysteresis voltage	Rail 5 V	50		120	mV	VSTBY
$T_{VSTBY_UV_BLK}$	VSTBY UV blanking time upon transition from SLEEP to NORMAL state		1300		2000	µs	VSTBY
$V_{VSTBY0_OV_TH}$	VSTBY0 overvoltage detection threshold	Rail 3.3 V	V_{VSTBY0}* 1.05		V_{VSTBY0}* 1.17	V	VSTBY
$V_{VSTBY1_OV_TH}$	VSTBY1 overvoltage detection threshold	Rail 5 V	V_{VSTBY1}* 1.05		V_{VSTBY1}* 1.17	V	VSTBY
$T_{VSTBY_OV_FIL}$	VSTBY OV detection filter time		15		25	µs	VSTBY
$V_{VSTBY0_OV_HYS}$	VSTBY0 overvoltage detection Hysteresis voltage	Rail 3.3 V	20		60	mV	VSTBY
$V_{VSTBY1_OV_HYS}$	VSTBY1 overvoltage detection Hysteresis voltage	Rail 5 V	50		100	mV	VSTBY
$TEMP_{VSTBY_OT_TH}$	VSTBY overtemperature detection threshold		180	190	200	°C	VSTBY

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$TEMP_{VSTBY_OT_HYS}$	VSTBY overtemperature detection Hysteresis voltage		5	6	7	°C	VSTBY
$T_{VSTBY_OT_FIL}$	VSTBY Overtemperature detection Filter time		2		72	µs	VSTBY
C_{VSTBY}	External output capacitor	Application info	-10%	4.7	+10%	µF	VSTBY
ESR_C_{VSTBY}	Output capacitor ESR	Application info		3		mΩ	VSTBY

4.3.11 Internal analog LDO (VANA)

This internal LDO:

- Is fed by the **Main Supply (VBP)**
- Is used for supplying internal circuitry in STANDBY state (cyclically activated) and in NORMAL state

4.3.11.1 Diagnostics

This LDO is equipped with UV/OV/OT detection, available both in NORMAL and STANDBY state and listed in the following table.

Table 30. VANA diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VANA undervoltage	• If the V_{VANA} voltage falls below $V_{VANA_UV_TH}$ for an interval longer than $T_{VANA_UV_FIL}$, the VANA_UV fault is acknowledged.	• The VANA_UV flag is set • If in STANDBY, the IC moves to NORMAL and FSO1, FSO2 lines are asserted • If in NORMAL, FSO1, FSO2 lines are asserted	• If the V_{VANA} voltage rises above $V_{VANA_UV_TH}$ + $V_{VANA_UV_HYS}$ for an interval longer than $T_{VANA_UV_FIL}$, the VANA_UV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• Blanked during power-up sequence, until NORMAL state is reached from SLEEP state • Blanked during its power-up when cyclically activated in STANDBY state

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VANA overvoltage	• If the V_{VANA} voltage rises above $V_{VANA_OV_TH}$ for an interval longer than $T_{VANA_OV_FIL}$, the VANA_ OV fault is acknowledged	• The VANA_ OV flag is set • If in STANDBY, the IC moves to NORMAL and FSO1, FSO2 lines are asserted • If in NORMAL, FSO1, FSO2 lines are asserted	• If the V_{VANA} voltage falls below $V_{VANA_OV_TH}$ - $V_{VANA_OV_HYS}$ for an interval longer than $T_{VANA_OV_FIL}$, the VANA_ OV flag can be cleared by MCU	• FSO1, FSO2 lines are released	• None
VANA overtemperature	• If $TEMP_{VANA}$ rises above $TEMP_{VANA_OT_TH}$ for an interval longer than $T_{VANA_OT_FIL}$, the VANA_OT fault is acknowledged	• The VANA_OT flag is set • If in STANDBY, the IC moves to NORMAL and FSO1, FSO2 lines are asserted • If in NORMAL, FSO1, FSO2 lines are asserted • VANA is switched OFF	• If $TEMP_{VANA}$ falls below $TEMP_{VANA_OT_TH}$ - $TEMP_{VANA_OT_HYS}$ for an interval longer than $T_{VANA_OT_FIL}$, the VANA_OT flag can be cleared by MCU • VANA is switched ON	• FSO1, FSO2 lines are released	• None

4.3.11.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: VBP according to the operating range inTable 2; T_J according to the operating range in Table 5.

Table 31. VANA electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{VANA}	Regulated voltage	NORMAL, All operating lines and loads	-3%	3.45	+3%	V	VANA
$I_{VANA_INT_LOAD}$	VANA internal load current		0.01		10	mA	VANA
I_{VANA_LIM}	VANA output current limitation	NORMAL, V_{VANA} = 0 V	25		48	mA	VANA
V_{VANA_PSRR}	VANA power supply rejection ratio	V_{VBP_NOISE} = 100 mV_{pp}, f_{NOISE} = 400 KHz, Guaranteed by design	40			dB	VANA
$T_{VANA_SOFT_START}$	VANA soft start time	From 10% to 90% of V_{VANA}. Guaranteed by design I_{VANA_LOAD} = 10 mA, C_{VANA} = 2.2 µF	195		390	µs	VANA
$V_{VANA_OV_TH}$	VANA overvoltage detection threshold		3.6	3.75	3.9	V	VANA
$V_{VANA_UV_TH}$	VANA undervoltage detection threshold		2.6	2.75	2.9	V	VANA
$V_{VANA_OV_HYS}$	VANA overvoltage detection Hysteresis voltage		33		52	mV	VANA
$V_{VANA_UV_HYS}$	VANA undervoltage detection Hysteresis voltage		50		90	mV	VANA
$T_{VANA_OV_FIL}$	VANA OV detection Filter time		15		25	µs	VANA
$T_{VANA_UV_FIL}$	VANA UV detection Filter time		15		25	µs	VANA
$T_{VANA_UV_BLK}$	VANA UV blanking time upon transition from SLEEP to NORMAL state and during cyclic activation in STANDBY state		1300		2000	µs	VANA
$TEMP_{VANA_OT_TH}$	VANA overtemperature detection threshold		182	190	198	°C	VANA
$TEMP_{VANA_OT_HYS}$	VANA overtemperature detection Hysteresis voltage		9	10	11	°C	VANA
$T_{VANA_OT_FIL}$	VANA overtemperature detection Filter time		2		72	µs	VANA
C_{VANA}	External output capacitor	Application info	-30%	2.2	+30%	µF	VANA
ESR_C_{VANA}	Output capacitor ESR	Application info			6	mΩ	VANA

4.3.12 Digital output buffer supply (VIO)

This supply line:

- Is fed by the external supply line: **LDO1 (VCC)** or **LDO4 (VSTBY)** or **Buck2 (VCORE)**
- Is used for supplying all digital output buffers.

To ensure a correct behavior of the internal circuitry, if the VIO is connected to the VCOREFB pin, $V_{VCOREFB}$ must be equal to 3.3 V or 5 V (refer to Section 4.3.5).

4.3.13 Internal power on reset (INT_POR)

The internal supply voltage line for internal circuitries is monitored by means of a dedicated UV diagnostic to detect abnormal low-level events either caused by VBP drop or internal faults.

If UV detection INT_POR event occurs for an interval longer than $T_{POR_ASF_FIL_DET}$, the flag INT_POR is set and the L9988 is sent to POWER OFF state.

4.3.13.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 32. Internal power on reset electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{INT_POR_TH}$	INT_POR threshold voltage				4	V	VBP
$V_{INT_POR_HY}$	INT_POR threshold voltage hysteresis		50	90		mV	VBP
$T_{POR_ASF_FIL_REL}$	INT_POR release filter time		2	4	7	us	VBP
$T_{POR_ASF_FIL_DET}$	INT_POR detection filter time		2	8	18	us	VBP

4.3.14 Analog Built-In-Selt-Test (ABIST)

An analog built-in-self-test (ABIST) procedure is implemented to check safety relevant circuitries of the analog monitors on the L9988.

The ABIST activation procedure can be requested by setting via SPI, the write-only field ABIST_START in the VCR_FAULT_INJ_ABIST register.

After a T_{ABIST} interval, the ABIST procedure stops and the clear-on-read SPI field ABIST_END is set in the VCR_FAULT_INJ_ABIST register.

Table 33. ABIST electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
T_{ABIST}	ABIST procedure duration	All output buffers in steady ON state	0.7		1.1	ms	-

The results of the ABIST procedure are then written into the clear-on-read SPI field ABIST_FAIL in the VCR_FAULT_INJ_ABIST register:

- If ABIST_END = 1 and ABIST_FAIL = 0, the ABIST procedure ended, and NO stuck fault is detected on analog monitors under test.
- If ABIST_END = 1 and ABIST_FAIL = 1, the ABIST procedure ended, and a stuck fault is detected on one or more analog monitors under test.

During the ABIST procedure, the functionality of the involved monitoring unit is suspended for the entire duration of the procedure (T_{ABIST}). As a consequence, any fault event occurring when the ABIST is running is ignored.

Analog BIST is performed on the following comparators.

Table 34. List of comparators covered by ABIST

Comparator	Diagnostics
VBP undervoltage	VBP_UV
VBP overvoltage	VBP_OV
VANA undervoltage	VANA_UV
VANA overvoltage	VANA_OV
VCC undervoltage	VCC_UV
VCC overvoltage	VCC_OV
VCC CAN undervoltage	VCC-CAN_UV
VCC CAN overvoltage	VCC_CAN_OV

Comparator	Diagnostics
VTREF undervoltage	VTREF_UV
VTREF overvoltage	VTREF_OV
VSTBY undervoltage	VSTBY_UV
VSTBY overvoltage	VSTBY_OV
VPRE undervoltage	VPRE_UV
VPRE overvoltage	VPRE_OV
VBST undervoltage	VBST_UV
VBST overvoltage	VBST_OV
VCORE undervoltage	VCORE_UV
VCORE Deep undervoltage	VCORE_DEEP UV
VCORE overvoltage	VCORE_OV
VCP undervoltage	VCP_UV
VCP overvoltage	VCP_OV
Ground loss	GND_LOSS

4.4 Voltage Conversion Routine (VCR)

While in NORMAL or in STANDBY state, the L9988 monitors the cells and battery pack voltage, the four analog inputs connected to the external NTCs and the two GPIOs with four independent 15-bit ADCs (one ADC per each cell).

The ADCs have been designed to guarantee an accurate measurement in the [-40°C; +105°C] junction temperature range, with a maximum error of ±2 mV in the [1.8 V÷4.5 V] voltage range.

During the Voltage Conversion Routine (VCR), the IC also ensures the safe detection of dangerous events such as OV/UV/OT/UT.

When in NORMAL state, the task execution is triggered by setting the Start of Conversion (SOC) command on-demand by SPI or periodically and automatically by an internal timer.

A single acquisition starts T_{ADCV_START} after the receipt of the Start of Conversion (SOC) trigger command. It lasts T_{ADCV_FILTER}, which is programmable using the **ADCV_FIL** 3-bit field. Moreover, a third time T_{ADCV_CAL} is necessary to post-elaborate the conversion data.

The conversion time is $T_{ADCV_CONV} = T_{ADCV_START} + T_{ADCV_FILTER} + T_{ADCV_CAL}$

With reference to Figure 17, using the four ADCs in parallel, the total conversion time for cell voltage monitor (Cx), battery stack voltage measurement (VBS, VPP), cell temperature monitor (AINx - NTCx) and the GPIO conversion/monitor (GPIOx) is $T_{ADCV_CONV_TOT} = 3*(T_{ADCV_START} + T_{ADCV_FILTER}) + T_{ADCV_CAL}$

With reference to Figure 18, the time required to perform the internal and open diagnostics, assuming $T_{ADCV_OPEN_DIAG} = T_{ADCV_FILTER}$, is $T_{DIAG} = 2*(T_{ADCV_START} + T_{ADCV_FILTER}) + 3*(T_{ADCV_START} + T_{ADCV_OPEN_DIAG}) + T_{ADCV_CAL} = 5*(T_{ADCV_START} + T_{ADCV_FILTER}) + T_{ADCV_CAL}$

Then, a voltage conversion routine lasts a time equal to $T_{ADCV_ON} = T_{ADCV_CONV_TOT} + T_{DIAG} = 8*(T_{ADCV_START} + T_{ADCV_FILTER}) + 2*T_{ADCV_CAL}$

Both SOC commands are detailed below:

1. Start of Conversion (SOC) command by SPI
   - The MCU can send a SOC command, by writing the write-only field SPI_SOC in the CONV_SOC register, according to the T_{CS_CONV} (defined in Section 4.7.1) and the T_{ADCV_ON} time. Note that the voltage conversion routine is synchronized with the current conversion routine: the start of conversion of cells 1,2,3,4 is generated synchronously (in parallel) to the current sense ADC sampling trigger.
   - A new SOC command cannot interrupt or restart an ongoing conversion, and the command is discarded.
   - After the end of voltage and current routines, the MCU can read the SPI registers with diagnostic results and conversions.
   - Diagnostics are executed only after the SOC command.

Figure 17. Timing diagram of voltage conversion step (VOLT STEP) in VCR

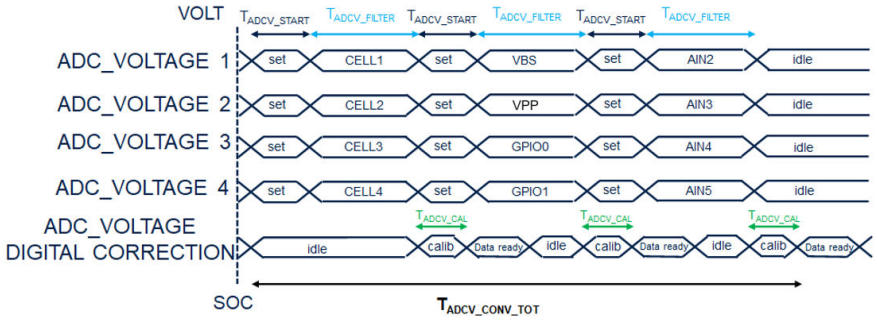
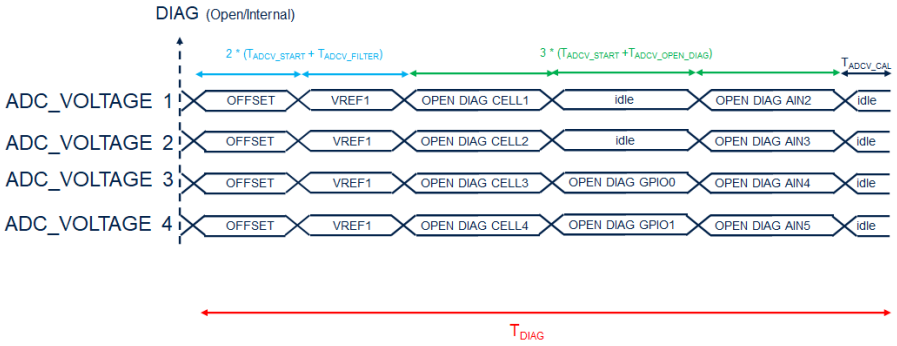


Figure 18. Timing diagram of the internal and open diagnostics steps (DIAG STEP) in VCR



2. Start of Conversion (SOC) command by internal timer
   - The MCU can configure an internal timer (using the HF main oscillator) to send a periodic SOC command every T_{CYCLE_NORMAL}, which is programmable using the 3-bit **CYCLE_NORMAL** field.
   - To synchronize internal routines with readout, the IC generates an interrupt at end of routines to let the MCU SPI readout.
   - Diagnostics are executed automatically each T_{CYCLE_NORMAL} (flag set during single step),
   - If the SOC internal timer is disabled during T_{CYCLE_NORMAL}, the routine is not interrupted until its end. After that, a new SOC by SPI is accepted.

   An example of timing diagram of SOC command by internal timer is shown in Section 4.7.1

Table 35. T_{CYCLE_NORMAL} setting

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
T_{CYCLE_NORMAL}	Internal timer for SOC cycled activation (3-bit)	CYCLE_NORMAL = 000		Continuously running		-	-
		CYCLE_NORMAL = 001	9.4	10	10.8	ms	-
		CYCLE_NORMAL = 010	18.9	20	21.6	ms	-
		CYCLE_NORMAL = 011	37.9	40	43.1	ms	-

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
T_{CYCLE_NORMAL}	Internal timer for SOC cycled activation (3-bit)	CYCLE_NORMAL = 100	75.8	80	86.1	ms	-
		CYCLE_NORMAL = 101	151.6	160	172.2	ms	-
		CYCLE_NORMAL = 110	303.3	320	344.3	ms	-
		CYCLE_NORMAL = 111	606.6	640	688.5	ms	-

MCU can switch from one to the other mode by the SPI configuration bit **SOC_SEL**. If SOC_SEL = 0 (default), the VCR is triggered by the SPI command. If SOC_SEL = 1, the VCR is cyclically executed every $\mathbf{T_{CYCLE_NORMAL}}$ seconds.

SOC_SEL is automatically reset to 0 in STANDBY MODE to disable $\mathbf{T_{CYCLE_NORMAL}}$ trigger and let the new $\mathbf{T_{CYCLE_STANDBY}}$ (defined below) periodicity. In this way, as soon as the device exit from STANDBY MODE going to NORMAL MODE, the VCR routine is waiting for the new SOC by SPI or enables the internal timer again by setting SOC_SEL =1

If the periodic SOC is selected, a SOC by SPI is no longer accepted and the internal mechanism starts at the end of the current routine if running. If the periodic SOC is disabled, a SOC by SPI is accepted after the end of the last running routine, otherwise ignored.

No shadow register memory is implemented, register map values are updated as soon as the conversions are ready. Therefore, the MCU can synchronize readout considering routines duration after a SOC by SPI or configuring interrupt generation for SOC by internal timer.

In summary, with a SOC by SPI, the conversion trigger and individual steps can be enabled/disabled programming via SPI, the corresponding bits:

- **VOLT_STEP = 1** enables the cell voltage monitor (Cx), the battery stack voltage measurement (VBS, VPP), the cell temperature monitor (AINx - NTCx), and the GPIO conversion/monitor (GPIOx).
- **DIAG_STEP = 1** enables the VREF1, VREF2 internal voltage reference diagnostics (VREF1 or VREF2 depending on the ADC_SWAP bit setting, refer to Section 4.4.9), OFFSET diagnostic and the open diagnostics on the figure above.

The status of the routine is reported by the VCR_BUSY flag: when set, the routine is ongoing. In case a single routine step does not end within $T_{VCR_TIMEOUT}$, the VCR_FAIL latch is set (cleared upon read).

On the other hand, with SOC by internal timer, the voltage conversion routine is fixed, and all the steps are performed every $\mathbf{T_{CYCLE_NORMAL}}$.

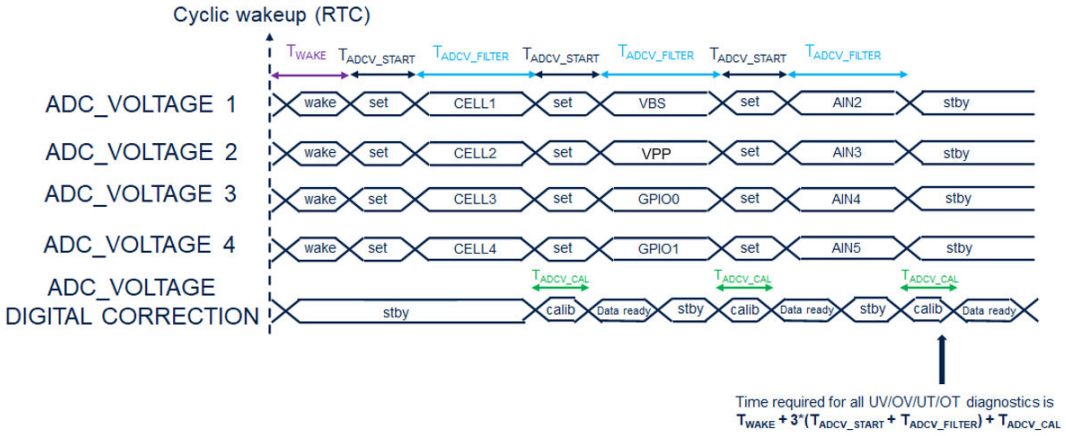
For safety reasons, some internal ADCs blocks are redundant and compared each other (refer to Section 4.4.9). In case of mismatch, the flag VCR_RED_CHECK_FAIL is set, and the measurements are not reliable.

When the device is in STANDBY, the voltage conversion routine is periodically executed every $\mathbf{T_{CYCLE_STANDBY}}$ second (e.g. 1s, defined by the internal real time clock RTC; refer to Section 4.13.1) according to VOLT_STEP and DIAG_STEP bits.

In this period, the time required for all conversions and diagnostics is $\mathbf{T_{ADCV_CYCLIC_ON}} = \mathbf{T_{WAKE}} + \mathbf{T_{ADCV_ON}} = \mathbf{T_{WAKE}} + \mathbf{T_{ADCV_CONV_TOT}} + \mathbf{T_{DIAG}} = \mathbf{T_{WAKE}} + 8*(\mathbf{T_{ADCV_START}} + \mathbf{T_{ADCV_FILTER}}) + 2*\mathbf{T_{ADCV_CAL}}$

In Figure 19, the timing diagram shows the cyclic wakeup of the voltage ADCs (in STANDBY MODE) to perform all the conversions and the UV/OV/UT/OT diagnostics in $\mathbf{T_{WAKE}} + \mathbf{T_{ADCV_CONV_TOT}} = \mathbf{T_{WAKE}} + 3*(\mathbf{T_{ADCV_START}} + \mathbf{T_{ADCV_FILTER}}) + \mathbf{T_{ADCV_CAL}}$ seconds.

Figure 19. Timing Diagram of cycling conversion and UV/OV/UT/OT diagnostics in STANDBY



With reference to Figure 17 and Figure 18,note that:

- If all VCELL<x>_EN (defined in Section 4.4.1) are configured to 0 and a VCR is triggered, the measurement of differential voltages at Cx pins (CELLx in the figure) is skipped during the VOLT_STEP (if enabled). In this case, the cell open load diagnostics (OPEN DIAG CELLx in the figure) during DIAG_STEP (if enabled) are also skipped.
- If VBS_EN = 0, VPP_EN = 0 (defined in Section 4.4.2), GPIO0 and GPIO1 are configured as digital input/output (refer to Section 4.9), and a VCR is triggered, the measurement step related to VBS, VPP, GPIO0 and GPIO1 is skipped during VOLT_STEP (if enabled). In this case, the related OPEN DIAG diagnostics during DIAG_STEP (if enabled) are also skipped.
- If all NTC<x>_EN (defined in Section 4.4.4, related to AIN2, …, AIN5) are configured to 0 and a VCR is triggered, the NTCs voltage conversion is skipped during VOLT_STEP (if enabled). In this case, the AIN open load diagnostics (OPEN DIAG AINx in the figure) during DIAG_STEP (if enabled) are also skipped.
- The OFFSET and VREF1&VREF2 steps (refer to Section 4.4.8: ADC Built-In-Self-Test (ADCV BIST)) are always executed during DIAG_STEP (if enabled) when the VCR is triggered.

4.4.1 Cell voltage monitor (Cx)

During cell voltage monitoring step (VOLT_STEP = 1), the voltage conversion routine measures differential voltages at Cx pins and stores results in **VCELL<x>_MEAS** registers, along with the corresponding **DATA_READY<x>** bit. Such latch is set upon the generation of a new measurement result, and it is cleared upon read. A cell is converted only if its corresponding VCELL<x>_EN bit is set to 1. By default, all cells are disabled.

The IC also performs the digital sum of cells allowing the plausibility check vs. VBS (Section 4.4.2.1). Such digital sum of cells is stored in the **VCELL_SUM_MEAS** register.

4.4.1.1 Diagnostics

The IC features a comprehensive set of diagnostics based on cell voltage acquisition triggered by the VCR. Each diagnostic has been designed to address specific application cases and shall always be validated in conjunction with other safety mechanisms covering failures in the external analog front-end or internal conversion path.

Diagnostics with configurable threshold have a proper resolution defined in the electrical parameters in Section 4.4.1.2.

For example, considering the cell undervoltage UV diagnostic, to set the $\mathbf{V_{CELL_UV_TH}}$ threshold equal to 2 V,

$\mathbf{V_{CELL_UV_TH} = 64 * V_{ADCV_RES}}$ *** (9-bit CELL_UV_TH register CODE converted in decimal value)**, in which

$V_{ADCV_RES} = 6/2^{15}$ V

9-bit CELL_UV_TH register CODE = 0xAB = 171

Therefore, $V_{CELL_UV_TH} = 64 * 6/2^{15} * 171 = 2$ V

To calculate the differential voltages measured at the Cx pins in the voltage conversion routine, for example VCELL1_CONV, follow the calculation below.

$\mathbf{V_{CELL1_CONV} = V_{ADCV_RES}}$ * (**15-bit VCELL1_MEAS register CODE converted in decimal value**), in which

$V_{ADCV_RES} = 6/2^{15}$ V

15-bit VCELL1_MEAS register CODE = 0x44AB = 17579

Therefore, V_{CELL1_CONV} = 6/2^{15} * 17579 = 3.21881 V

This diagnostic covers the failures listed in the following table.

Table 36. Cell voltage monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Cell undervoltage	• If the V_{Cx} – V_{Cx-1} voltage falls below $V_{CELL_UV_TH}$, the CELL<x>_UV fault is acknowledged.	• The CELL<x>_UV flag is set • Balancing is turned OFF on the affected cell • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the V_{Cx} – V_{Cx-1} voltage rises above $V_{CELL_UV_TH}$, the CELL<x>_UV flag can be cleared by MCU	• Balancing is resumed on the affected cell (unless MCU has disabled it) • FAULT pin is released	• When VCELL<x>_EN=0, the CELL<x> voltage monitor diagnostic is masked, the CELL<x>_UV flag can always be cleared • CELL_UV_BAL_MSK=1 masks reaction on balancing FETs • VCELL_UV_MSK=1 • If in STANDBY, masks the IC transition to NORMAL and the reaction on the FAULT line • If in NORMAL, masks the reaction on the FAULT line • VCELL_FAULT_MSK=1 masks reaction on the FAULT line
Cell deep undervoltage	• If the V_{Cx} – V_{Cx-1} voltage falls below $V_{CELL_DEEP_UV_TH}$, the CELL<x>_DEEP_UV fault is acknowledged.	• The CELL<x>_DEEP_UV flag is set Balancing is turned OFF on the affected cell • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the V_{Cx} – V_{Cx-1} voltage rises above $V_{CELL_DEEP_UV_TH}$, the CELL<x>_DEEP_UV flag can be cleared by MCU	• Balancing is resumed on the affected cell (unless MCU has disabled it) • FAULT pin is released	• When VCELL<x>_EN=0, the CELL<x> voltage monitor diagnostic is masked, the CELL<x>_DEEP_UV flag can always be cleared • CELL_DEEP_UV_BAL_MSK=1 masks reaction on balancing FETs • VCELL_FAULT_MSK=1 masks reaction on the FAULT line

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Cell overvoltage	• If the V_{Cx} – V_{Cx-1} voltage rises above $V_{CELL_OV_TH}$, the CELL<x>_OV fault is acknowledged.	• The CELL<x>_OV flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the V_{Cx} – V_{Cx-1} voltage falls below $V_{CELL_OV_TH}$, the CELL<x>_OV flag can be cleared by MCU	• FAULT pin is released	• When VCELL<x>_EN=0, the CELL<x> voltage monitor diagnostic is masked, the CELL<x>_OV flag can always be cleared • VCELL_FAULT_MSK=1 masks reaction on the FAULT line
Cell balancing undervoltage	• If the V_{Cx} – V_{Cx-1} voltage falls below $V_{CELL_BAL_UV_TH}$, the CELL<x>_BAL_UV fault is acknowledged.	• The CELL<x>_BAL_UV flag is set • Balancing is frozen on the affected cell • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the V_{Cx} – V_{Cx-1} voltage rises above $V_{CELL_BAL_UV_TH}$, the CELL<x>_BAL_UV flag can be cleared by MCU	• Balancing is resumed on the affected cell (unless MCU has disabled it) • FAULT pin is released	• When VCELL<x>_EN=0, the CELL<x> voltage monitor diagnostic is masked, the CELL<x>_BAL_UV flag can always be cleared • BAL_UV_BAL_MSK=1 masks reaction on balancing FETs • VCELL_FAULT_MSK=1 masks reaction on the FAULT line
Sum undervoltage	• If the sum of cell voltage falls below $V_{SUM_UV_TH}$, the SUM_UV fault is acknowledged.	• The SUM_UV flag is set • Balancing is frozen on all cells • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the sum of cell voltage rises above $V_{SUM_UV_TH}$, the SUM_UV flag can be cleared by MCU	• Balancing is resumed on all cells (unless MCU has disabled it) • FAULT pin is released	• When all VCELL<1,2,3,4>_EN=0, the CELL<x> voltage monitor diagnostic is masked, the SUM_UV flag can always be cleared • SUM_UV_BAL_MASK=1 masks reaction on balancing FETs • VCELL_FAULT_MSK=1 masks reaction on the FAULT line

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Sum overvoltage	• If the sum of cell voltage rises above $V_{SUM_OV_TH}$, the SUM_OV fault is acknowledged.	• The SUM_OV flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the sum of cell voltage falls below $V_{SUM_OV_TH}$, the SUM_OV flag can be cleared by MCU	• FAULT pin is released	• When all VCELL<1,2,3,4>_EN=0, the CELL<x> voltage monitor diagnostic is masked, the SUM_OV flag can always be cleared • VCELL_FAULT_MSK=1 masks reaction on the FAULT line

4.4.1.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 37. Cell voltage monitor electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
N_{BIT_ADCV}	ADC bit number	Design info		15		bit	Cx, VBS, VPP, AINx, GPIOx
$V_{ADCV_DIFF_FS}$	ADC full scale differential input voltage	Design info	0		6	V	Cx
$V_{ADCV_DIFF_OP}$	ADC operating differential input voltage	Design info	0.1		5	V	Cx
V_{ADCV_RES}	ADC resolution (LSB)	Design info. LSB calculated on DIFF_FS		$6/2^{15}$		V	Cx
$V_{CELL_SUM_RES}$	Cell sum voltage measurement resolution, $V_{CELL_SUM_RES} = V_{ADCV_RES}$	Design info		$6/2^{15}$		V	Cx
$I_{CELL_LEAK_105}$	Cx pins leakage current (low)	-40°C ≤ T_J ≤ +105°C			200	nA	Cx
$I_{CELL_LEAK_125}$	Cx pins leakage current (high)	+105°C ≤ T_J ≤ +125°C			300	nA	Cx
$R_{CELL_DIFF_IN}$	Cell differential input impedance between adjacent Cx pins	V_{CELL} = 5 V	10			MΩ	Cx
T_{ADCV_START}	ADC settling time	Guaranteed by SCAN		60		µs	Cx, VBS, VPP, AINx, GPIOx
T_{ADCV_CAL}	ADC post-calibration time, applied after every conversion	Guaranteed by SCAN		24	70	µs	Cx, VBS, VPP, AINx, GPIOx
$T_{ADCV_FILTER_000}$	Voltage ADC filter time	ADCV_FIL = 000		136		µs	Cx, VBS, VPP, AINx, GPIOx
$T_{ADCV_FILTER_001}$		ADCV_FIL = 001		264		µs	
$T_{ADCV_FILTER_010}$		ADCV_FIL = 010		1.04		ms	
$T_{ADCV_FILTER_011}$		ADCV_FIL = 011		2.08		ms	
$T_{ADCV_FILTER_100}$		ADCV_FIL = 100		4.16		ms	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$T_{ADCV_FILTER_101}$	Voltage ADC filter time	ADCV_FIL = 101		8.32		ms	Cx, VBS, VPP, AINx, GPIOx
$T_{ADCV_FILTER_110}$		ADCV_FIL = 110		16.64		ms	
$T_{ADCV_FILTER_111}$		ADCV_FIL = 111		66.56		ms	
T_{WAKE}	Time to wake up internal circuitry for cycling conversions in STANDBY			1		ms	-
$T_{VCR_TIMEOUT}$	Single routine step timeout	Guaranteed by SCAN		75		ms	-
$V_{ADCV_TOTAL_ERR0_105}$	ADC total conversion error, including post-soldering and ageing effects (1)	0.1 V ≤ V_{CELL} < 2 V, -40°C ≤ T_J ≤ +105°C	-1		1	mV	Cx
$V_{ADCV_TOTAL_ERR1_105}$	ADC total conversion error, including post-soldering and ageing effects (1)	2 V ≤ V_{CELL} < 3.4 V, -40°C ≤ T_J ≤ +105°C	-1.5		1.5	mV	Cx
$V_{ADCV_TOTAL_ERR2_105}$	ADC total conversion error, including post-soldering and ageing effects(1)	3.4 V ≤ V_{CELL} < 4.5 V, -40°C ≤ T_J ≤ +105°C	-2		2	mV	Cx
$V_{ADCV_TOTAL_ERR3_105}$	ADC total conversion error, including post-soldering and ageing effects(1)	4.5 V ≤ V_{CELL} < 5 V, -40°C ≤ T_J ≤ +105°C	-2.2		2.2	mV	Cx
$V_{ADCV_TOTAL_ERR0_125}$	ADC total conversion error, including post-soldering and ageing effects (1)	0.1 V ≤ V_{CELL} < 2 V, +105°C ≤ T_J ≤ +125°C	-1.2		1.2	mV	Cx
$V_{ADCV_TOTAL_ERR1_125}$	ADC total conversion error, including post-soldering and ageing effects (1)	2 V ≤ V_{CELL} < 3.4 V, +105°C ≤ T_J ≤ +125°C	-2		2	mV	Cx
$V_{ADCV_TOTAL_ERR2_125}$	ADC total conversion error, including post-soldering and ageing effects(1)	3.4 V ≤ V_{CELL} < 4.5 V, +105°C ≤ T_J ≤ +125°C	-2.5		2.5	mV	Cx
$V_{ADCV_TOTAL_ERR3_125}$	ADC total conversion error, including post-soldering and ageing effects(1)	4.5 V ≤ V_{CELL} < 5 V, +105°C ≤ T_J ≤ +125°C	-3		3	mV	Cx
$V_{ADCV_TOTAL_ERR0_150}$	ADC total conversion error, including post-soldering and ageing effects (1)	0.1 V ≤ V_{CELL} < 2 V, +125°C ≤ T_J ≤ +150°C	-4		4	mV	Cx
$V_{ADCV_TOTAL_ERR1_150}$	ADC total conversion error, including post-soldering and ageing effects (1)	2 V ≤ V_{CELL} < 3.4 V, +125°C ≤ T_J ≤ +150°C	-6		6	mV	Cx
$V_{ADCV_TOTAL_ERR2_150}$	ADC total conversion error, including post-soldering and ageing effects(1)	3.4 V ≤ V_{CELL} < 4.5 V, +125°C ≤ T_J ≤ +150°C	-9		9	mV	Cx
$V_{ADCV_TOTAL_ERR3_150}$	ADC total conversion error, including post-soldering and ageing effects(1)	4.5 V ≤ V_{CELL} < 5 V, +125°C ≤ T_J ≤ +150°C	-11		11	mV	Cx
$V_{ADCV_NOISE_000}$	Standard deviation over a population of 100 samples	ADCV_FIL = 000			1000	μV_{RMS}	Cx
$V_{ADCV_NOISE_001}$		ADCV_FIL = 001			400	μV_{RMS}	
$V_{ADCV_NOISE_010}$		ADCV_FIL = 010			150	μV_{RMS}	
$V_{ADCV_NOISE_011}$		ADCV_FIL = 011			150	μV_{RMS}	
$V_{ADCV_NOISE_100}$		ADCV_FIL = 100			100	μV_{RMS}	
$V_{ADCV_NOISE_101}$		ADCV_FIL = 101			100	μV_{RMS}	
$V_{ADCV_NOISE_110}$		ADCV_FIL = 110			100	μV_{RMS}	
$V_{ADCV_NOISE_111}$		ADCV_FIL = 111			100	μV_{RMS}	
$V_{CELL_UV_TH}$	Programmable cell undervoltage threshold (9 bit), $V_{CELL_{UV_{TH}}} = 64V_{ADCV_{RES}} * CODE$	CELL_UV_TH	0		6	V	Cx
$V_{CELL_DEEP_UV_TH}$	Programmable cell deep undervoltage threshold (9 bit), $V_{CELL_{DEEP_UV_{TH}}} = 64V_{ADCV_{RES}} * CODE$	CELL_DEEP_UV_TH	0		6	V	Cx
$V_{CELL_OV_TH}$	Programmable cell overvoltage threshold (9 bit), $V_{CELL_{OV_{TH}}} = V_{CELL_{UV_{TH}}} + 64V_{ADCV_{RES}} * CODE$	CELL_OV_TH	0		12	V	Cx

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{BAL_UV_TH}$	Programmable balance undervoltage threshold (9 bit), $V_{BAL_{UV_{TH}}} = 64V_{ADCV_{RES}} * CODE$	BAL_UV_TH	0		6	V	Cx
$V_{SUM_UV_TH}$	Programmable sum of cells undervoltage threshold (9 bit) $V_{SUM_{UV_{TH}}} = 256V_{ADCV_{RES}} * CODE$	SUM_UV_TH	0		24	V	Cx
$V_{SUM_OV_TH}$	Programmable sum of cells overvoltage threshold (9 bit), $V_{SUM_{OV_{TH}}} = V_{SUM_{UV_{TH}}} + 256V_{ADCV_{RES}} * CODE$	SUM_OV_TH	0		48	V	Cx

1. *[1]. Single shot samples are characterized by a superimposed gaussian noise, with zero-mean and VADCV_NOISE standard deviation*

4.4.2 Battery stack voltage measurement (VBS, VPP)

The IC performs battery stack voltage sensing via a dedicated VBS input.

Results are stored in the **VBS_MEAS** register and can be compared by the MCU to the digital sum of cells to perform plausibility checks. The result is stored along with the corresponding DATA_READY bit. Such latch is set upon the generation of a new measurement result, and it is cleared upon read.

To limit the current consumption, the internal divider is normally kept disconnected from the VBS. It is connected only during voltage conversion routine task execution.

The VBS measurement can be enabled by setting the VBS_EN bit.

During the voltage conversion routine, the voltage at the VPP pin connected to KL30 is also detected.

Results are stored in the **VPP_MEAS** register and can be compared by the MCU to the VBS to perform plausibility checks. The result is stored along with the corresponding DATA_READY bit. Such latch is set upon the generation of a new measurement result, and it is cleared upon read.

The VPP measurement can be enabled by setting the VPP_EN bit.

To calculate the voltages measured at the VBS pin in the voltage conversion routine for example, follow the calculation below.

V_{VBS_MEAS} = $V_{ADCV_BATT_RES}$ * (15-bit VBS_MEAS register CODE converted in decimal value), in which

$V_{ADCV_BATT_RES} = 24/2^{15}$ V

15-bit VBS_MEAS register CODE = 0x4094 = 16532

Therefore, $V_{VBS_MEAS} = 24/2^{15} * 16532 = 12.11$ V

4.4.2.1 *Diagnostics*

The IC features a comprehensive set of diagnostics based on direct battery stack voltage acquisition. Each diagnostic has been designed to address specific application cases and shall always be validated in conjunction with other safety mechanism covering failures in the external analog front-end or internal conversion path.

Table 38. Battery stack voltage diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VBS overvoltage	• If the V_{VBS} voltage rises above $V_{VBS_OV_TH}$, the VBS_OV fault is acknowledged	• The VBS_OV flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the V_{VBS} voltage falls below $V_{VBS_OV_TH}$, the VBS_OV flag can be cleared by MCU	• FAULT pin is released	• When VBS_EN=0, the VBS voltage diagnostic is masked, the VBS_OV flag can always be cleared • VBS_FAULT_MSK=1 masks reaction on the FAULT line
VBS undervoltage	• If the V_{VBS} voltage falls below $V_{VBS_UV_TH}$, the VBS_UV fault is acknowledged	• The VBS_UV flag is set • Balancing is turned OFF on all cells • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the V_{VBS} voltage rises above $V_{VBS_UV_TH}$, the VBS_UV flag can be cleared by MCU	• Balancing is resumed (unless MCU has disabled it) • FAULT pin is released	• When VBS_EN=0, the VBS voltage diagnostic is masked, the VBS_UV flag can always be cleared • VBS_UV_BAL_MASK=1 masks reaction on balancing FETs • VBS_FAULT_MSK=1 masks reaction on the FAULT line
Plausibility check VBS vs. Sum of cells	• If the | VBS_MEAS - VCELL_SUM_MEAS| difference is greater than $V_{VBS_SUM_TH}$, the VBS_SUM_FAIL fault is acknowledged	• The VBS_SUM_FAIL flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the | VBS_MEAS - VCELL_SUM_MEAS| difference is smaller than $V_{VBS_SUM_TH}$, the VBS_SUM_FAIL flag can be cleared by MCU	• FAULT pin is released	• When VBS_EN=0, the VBS voltage diagnostic is masked, the VBS_SUM_FAIL flag can always be cleared • VBS_FAULT_MSK=1 masks reaction on the FAULT line

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VPP overvoltage	• If the V_{VPP} voltage rises above $V_{VPP_OV_TH}$, the VPP_OV fault is acknowledged	• The VPP_OV flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the V_{VPP} voltage falls below $V_{VPP_OV_TH}$, the VPP_OV flag can be cleared by MCU	• FAULT pin is released	• When VPP_EN=0, the VPP voltage diagnostic is masked, the VPP_OV flag can always be cleared • VPP_FAULT_MSK=1 masks reaction on the FAULT line
VPP undervoltage	• If the V_{VPP} voltage falls below $V_{VPP_UV_TH}$, the VPP_UV fault is acknowledged	• The VPP_UV flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the V_{VPP} voltage rises above $V_{VPP_UV_TH}$, the VPP_UV flag can be cleared by MCU	• FAULT pin is released	• When VPP_EN=0, the VPP voltage diagnostic is masked, the VPP_UV flag can always be cleared • VPP_FAULT_MSK=1 masks reaction on the FAULT line
Plausibility check VBS vs. VPP	• If the V_{VPP} - V_{VBS} is greater than $V_{VBS_VPP_TH}$, the VBS_VPP_FAIL fault is acknowledged	• The VBS_VPP_FAIL flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT is pin asserted	• If the V_{VPP} - V_{VBS} is smaller than $V_{VBS_VPP_TH}$, the VBS_VPP_FAIL flag can be cleared by MCU	• FAULT pin is • released	• When VBS_EN=0 and/or VPP_EN=0, the VPP and VBS voltage diagnostic are masked, the VBS_VPP_FAIL flag can always be cleared • When VPP_FAULT_MSK=1 and/or VBS_FAULT_MSK=1, it masks reaction on the FAULT line

4.4.2.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 39. Battery stack monitor external parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$N_{BIT_ADCV_BATT}$	ADC bit number	Design info		15		bit	VBS VPP
$V_{ADCV_BATT_DIFF_OP}$	ADC operating differential input voltage	Design info	4		20	V	VBS VPP
$V_{ADCV_BATT_DIFF_FS}$	ADC full scale differential input voltage	Design info	0		24	V	VBS VPP
$V_{ADCV_BATT_RES}$	ADC resolution (LSB)	Design info. LSB calculated on DIFF_FS		$24/2^{15}$		V	VBS VPP

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
R_{VBS_IN}	VBS input impedance	Guaranteed by design	0.9			MΩ	VBS
R_{VPP_IN}	VPP input impedance	Guaranteed by design	0.9			MΩ	VPP
$V_{ADCV_BATT_TOTAL_ERR_105}$	ADC total conversion error, including post-soldering and ageing effects(1)	6 V < V_{VPP},V_{VBS} < 20 V, -40°C ≤ T_J ≤ +105°C	-50		50	mV	VBS VPP
$V_{ADCV_BATT_TOTAL_ERR_125}$	ADC total conversion error, including post-soldering and ageing effects(1)	6 V < V_{VPP},V_{VBS} < 20 V, +105°C ≤ T_J ≤ +125°C	-75		75	mV	VBS VPP
$V_{ADCV_BATT_TOTAL_ERR_150}$	ADC total conversion error, including post-soldering and ageing effects(1)	6 V < V_{VPP},V_{VBS} < 20 V, +125°C ≤ T_J ≤ +150°C	-100		100	mV	VBS VPP
$V_{VBS_UV_TH}$	Programmable stack undervoltage threshold (8 bit), $V_{VBS_{UV_{TH}}} = 128V_{ADCV_BATT_{RES}} * CODE$	VBS_UV_TH	0		24	V	VBS
$V_{VBS_OV_TH}$	Programmable stack overvoltage threshold (8 bit), $V_{VBS_{OV_{TH}}} = V_{VBS_{UV_{TH}}} + 128V_{ADCV_BATT_{RES}} * CODE$	VBS_OV_TH	0		48	V	VBS
$V_{VBS_SUM_TH}$	Programmable threshold for the maximum mismatch between VBS and sum of cells (4 bit), $V_{VBS_{SUM_{TH}}} = 32V_{ADCV_BATT_{RES}} * CODE$	VBS_SUM_TH	0		351.6	mV	Cx, VBS
$V_{VPP_UV_TH}$	Programmable VPP undervoltage threshold (8 bit), $V_{VP+UV_{TH}} = 128V_{ADCV_BATT_{RES}} * CODE$	VPP_UV_TH	0		24	V	VPP
$V_{VPP_OV_TH}$	Programmable VPP overvoltage threshold (8 bit), $V_{VP+OV_{TH}} = V_{VP+UV_{TH}} + 128V_{ADCV_BATT_{RES}} * CODE$	VPP_OV_TH	0		48	V	VPP
$V_{VBS_VPP_TH}$	Programmable threshold for the maximum mismatch between VBS and VPP (4 bit), $V_{VBS_{VPP_{TH}}} = 512V_{ADCV_BATT_{RES}} * CODE$	VBS_VPP_TH	0		5.625	V	VBB VPP
$V_{ADCV_BATT_NOISE_000}$	Standard deviation over a population of 100 samples	ADCV_FIL = 000			5	mV_{RMS}	VBSVPP
$V_{ADCV_BATT_NOISE_001}$		ADCV_FIL = 001			2	mV_{RMS}	
$V_{ADCV_BATT_NOISE_010}$		ADCV_FIL = 010			1	mV_{RMS}	
$V_{ADCV_BATT_NOISE_011}$		ADCV_FIL = 011			0.75	mV_{RMS}	
$V_{ADCV_BATT_NOISE_100}$		ADCV_FIL = 100			0.75	mV_{RMS}	
$V_{ADCV_BATT_NOISE_101}$		ADCV_FIL = 101			0.5	mV_{RMS}	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{ADCV_BATT_NOISE_110}$	Standard deviation over a population of 100 samples	ADCV_FIL = 110			0.5	mV_{RMS}	VBSVPP
$V_{ADCV_BATT_NOISE_111}$		ADCV_FIL = 111			0.5	mV_{RMS}	

1. *[1]. Single shot samples are characterized by a superimposed gaussian noise, with zero-mean and VADCV_BATT_NOISE standard deviation*

4.4.3 Cell open load diagnostic

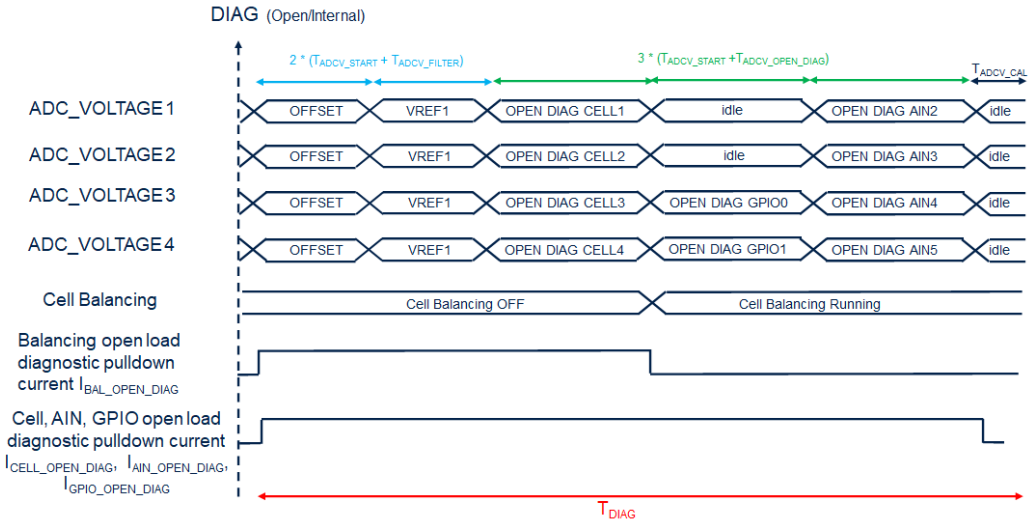
This diagnostic allows detecting open load failures on cell sensing lines (Cx) and cell balancing lines (Sx). When triggered by the command DIAG_STEP = 1, the following diagnostic routine is executed in parallel on all cell analog front-end pins:

- The diagnostic currents are enabled on the Cx pins and Sx pins
  - $I_{CELL_OPEN_DIAG}$ pulldown current is enabled on the C_X pins ranging from 1 to 4
  - $I_{BAL_OPEN_DIAG}$ pulldown current is enabled on the corresponding S_X pins ranging from 1 to 4
  - $I_{CELL_OPEN_DIAG_FIRST}$ pullup current is enabled on the C0 pin
  - $I_{BAL_OPEN_DIAG_FIRST}$ pullup current is enabled on the S0 pin
- The IC performs a conversion of the cell voltage at the C_X pins using the temporal window **T_{ADCV_START}+ $T_{ADCV_OPEN_DIAG}$** (see Figure 20) and unmasks the balancing open comparator at the S_X pins. Diagnostic information is processed as summarized in the following table.

The VBS channel features an internal resistive pulldown that discharges the VBS node to ground in case of open failure. Such failure results in plausibility check fail of VBS vs. sum of cells (refer to Section 4.4.2).

In Figure 20, the timing diagram shows the internal and open diagnostics steps in the voltage conversion routine, with a focus on the pulldown current$I_{CELL_OPEN_DIAG}$, $I_{AIN_OPEN_DIAG}$ (refer to Section 4.4.6), $I_{GPIO_OPEN_DIAG}$ (refer to Section 4.4.7) for cell, AIN, GPIO open load diagnostic respectively and $I_{BAL_OPEN_DIAG}$for balancing open load diagnostic.

Figure 20. Timing Diagram of the DIAG STEP in VCR with cell, AIN, GPIO and balancing open load diagnostic pulldown current



4.4.3.1 *Diagnostics*

Table 40. Cell open load diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Cell open	• The V_{Cx} – V_{Cx-1} voltage falls below $V_{Cx_OPEN_TH}$ • The V_{Sx} – V_{Sx-1} voltage is above $V_{Sx_OPEN_TH}$	• The CELL_OPEN_DIAG <x> code is set to '01' • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• The diagnostic step is re-executed at the next VCR trigger, and the diagnostic ends with no failure. Then CELL_OPEN_DIAG <x>=00 is automatically reported by the routine	• FAULT pin is released	• When VCELL<x>_EN=0, the CELL<x> open load diagnostic is masked, the CELL_OPEN_DIAG <x> field is always reported as "00" (no error code) when executing the diagnostic step
Balancing open	• The V_{Cx} – V_{Cx-1} voltage is above $V_{Cx_OPEN_TH}$ • The V_{Sx} – V_{Sx-1} voltage falls below $V_{Sx_OPEN_TH}$	• The CELL_OPEN_DIAG <x> code is set to '10' • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• The diagnostic step is re-executed at the next VCR trigger, and the diagnostic ends with no failure. Then CELL_OPEN_DIAG <x>=00 is automatically reported by the routine	• FAULT pin is released	• When VCELL<x>_EN=0, the CELL<x> open load diagnostic is masked, the CELL_OPEN_DIAG <x> field is always reported as "00" (no error code) when executing the diagnostic step
PCB open	• The V_{Cx} – V_{Cx-1} voltage falls below $V_{Cx_OPEN_TH}$ • The V_{Sx} – V_{Sx-1} voltage falls below $V_{Sx_OPEN_TH}$	• The CELL_OPEN_DIAG <x> code is set to '11' • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• The diagnostic step is re-executed at the next VCR trigger, and the diagnostic ends with no failure. Then CELL_OPEN_DIAG <x>=00 is automatically reported by the routine	• FAULT pin is released	• When VCELL<x>_EN=0, the CELL<x> open load diagnostic is masked, the CELL_OPEN_DIAG <x> field is always reported as "00" (no error code) when executing the diagnostic step
S0 open	• The V_{S0} voltage rises above $V_{SFIRST_OPEN_TH}$	• The SFIRST_OPEN flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• The diagnostic step is re-executed at the next VCR trigger, and the diagnostic ends with no failure. Then SFIRST_OPEN is automatically reported by the routine	• FAULT pin is released	• Non maskable
C0 open	• The V_{C0} voltage rises above $V_{C0_OPEN_TH}$	• The C0_OPEN flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• The diagnostic step is re-executed at the next VCR trigger, and the diagnostic ends with no failure. Then C0_OPEN is automatically reported by the routine	• FAULT pin is released	• Non maskable

4.4.3.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 41. Cell open load diagnostic electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$I_{CELL_OPEN_DIAG}$	Cell open load diagnostic pulldown current	$V_{Cx} \geq 1.5$ V	50		150	µA	C1 to C4
$I_{BAL_OPEN_DIAG}$	Balancing open load diagnostic pulldown current	$V_{Sx} \geq 1.5$ V	200		400	µA	S1 to S4
$I_{CELL_OPEN_DIAG_FIRST}$	Cell open load diagnostic pullup current applied to C0 pin of the first connected channel	$V_{C0} \geq 0.6$ V	-80		-20	µA	C0
$I_{BAL_OPEN_DIAG_FIRST}$	Balancing open load diagnostic pullup current applied to S0 pin of the first connected channel	$V_{S0} \geq 0.6$ V	-80		-20	µA	S0
$V_{Cx_OPEN_TH}$	Programmable cell open load threshold (4 bit), $V_{C_{OPEN_{TH}}} = 2048 V_{ADCV_{RES}} * CODE$	CX_OPEN_TH	0		5.625	V	Cx
$V_{Sx_OPEN_TH}$	Balancing open load threshold, differential comparator between S_X and S_{X-1}, x=1,4		0.4		0.8	V	S1 to S4
$V_{SFIRST_OPEN_TH}$	Balancing open load threshold, comparator between S0 and AGND		540	600	660	mV	S0
$V_{C0_OPEN_TH}$	Cell open load threshold, comparator between C0 and AGND		170		225	mV	C0
$T_{Sx_OPEN_FIL}$	Balancing open load comparators filter time		16		22	µs	Sx
$T_{C0_OPEN_FIL}$	C0 open load comparator filter time		16		22	µs	C0
$T_{ADCV_OPEN_DIAG_000}$	Cell open load diagnostic filter time (1)	ADCV_FIL = 000		136		µs	C1 to C4, AINx, GPIOx
$T_{ADCV_OPEN_DIAG_001}$		ADCV_FIL = 001		264		µs	
$T_{ADCV_OPEN_DIAG_010}$		ADCV_FIL = 010		1.04		ms	
$T_{ADCV_OPEN_DIAG_011}$		ADCV_FIL = 011		2.08		ms	
$T_{ADCV_OPEN_DIAG_100}$		ADCV_FIL = 100		4.16		ms	
$T_{ADCV_OPEN_DIAG_101}$		ADCV_FIL = 101		8.32		ms	
$T_{ADCV_OPEN_DIAG_110}$		ADCV_FIL = 110		16.64		ms	
$T_{ADCV_OPEN_DIAG_111}$		ADCV_FIL = 111		66.56		ms	

1. *Note that TADCV_OPEN_DIAG _xxx is equal to TADCV_FILTER_xxx of Table 37 in Section 4.4.1.2*

4.4.4 Cell temperature monitor (AINx - NTCx)

The NTC voltage conversion step monitors external temperature sensors connected to the analog inputs AIN2, …, AIN5 and, if applicable, to GPIO0 and GPIO1 configured as AI (refer to Section 4.9). For best performance, it is recommended:

- to supply NTCs usingVTREF
- to configure GPIO0 and GPIO1 for ratio-metric measurement as described in Section 4.9. On the other hand, for AIN2, …, AIN5, the ratio-metric measurement is inherent.

NTC measurements are stored in the corresponding NTC<x>_MEAS (x = 2, …, 5) and NTC<x>_GPIO<x>_MEAS (x = 0, 1) registers along with the corresponding DATA_READY<x> bit. Such latch is set upon the generation of a new measurement result, and it is cleared upon read. Each analog input AINx is converted only if its corresponding NTC<x>_EN bit is set to 1 (x = 2, …, 5). By default, all analog inputs are disabled. Unused analog inputs (AINx) and unused GPIOs (GPIO0, GPIO1) programmed as analog input, shall be connected to AGND.

Since in STANDBY MODE VTREF is cyclically activated for a time interval $T_{\mathbf{VTREF_ON}}$ in the period $\mathbf{T_{VTREF}}$ (defined by the internal RTC), the cell temperature monitor, the GPIO absolute conversion (refer to Section 4.4.5) and the open load diagnostics (refer to Section 4.4.6, Section 4.4.7) shall be performed within the $\mathbf{T_{VTREF_ON}}$. Therefore, considering the $\mathbf{T_{ADCV_CYCLIC_ON}} = \mathbf{T_{WAKE}} + 8*(\mathbf{T_{ADCV_START}} + \mathbf{T_{ADCV_FILTER}})+2*\mathbf{T_{ADCV_CAL}}$ defined in 4.4, it must be $\mathbf{T_{VTREF_ON}} > \mathbf{T_{ADCV_CYCLIC_ON}}$.

To calculate the NTC measurements at the AINx pins in the voltage conversion routine for example, AINx_MEAS, follow the calculation below.

$\mathbf{V_{AINx_MEAS}} = \mathbf{V_{ADCV_NTC_RES}}$ *** (15-bit AINx_MEAS register CODE converted in decimal value)**, in which

$V_{ADCV_NTC_RES} = 1.2*V_{VTREF}/2^{15}$ V

15-bit AINx_MEAS register CODE = 0x3555 = 13653

Therefore, $V_{AINx_MEAS} = 1.2*V_{VTREF}/2^{15} * 13653 = (16383.6*V_{VTREF}/2^{15})$ V

4.4.4.1 Diagnostics

Table 42. **Cell temperature diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
NTC AINx overtemperature (x = 2, …, 5)	• If the AINx voltage falls below $V_{NTCx_OT_TH}$,the NTC<x>_OT fault is acknowledged	• The NTC<x>_OT flag is set • Balancing is frozen on all cells • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• For channels configured as balancing cooldown (BAL_COOLDOWN_EN<x> = 1), if the AINx voltage rises above $V_{NTCx_OT_TH}$ + $V_{NTC_OT_HYS}$, the NTC<x>_OT flag can be cleared by MCU • For channels configured as cell NTCs (BAL_COOLDOWN_EN<x> = 0), if the AINx voltage rises above $V_{NTCx_OT_TH}$,the NTC<x>_OT flag can be cleared by MCU	• For channels configured as balancing cooldown (BAL_COOLDOWN_EN<x> = 1), the balancing is automatically re-engaged if the release condition is verified, even without NTC<x>_OT flag clear • For channels configured as cell NTCs (BAL_COOLDOWN_EN<x> = 0), the balancing is re-engaged only when NTC<x>_OT flag is cleared • FAULT pin is released	• When NTC<x>_EN=0 , the NTC<x> temperature diagnostics is masked, the NTC<x>_OT flag can always be cleared • NTC<x>_OT_BAL_MSK=1 masks reaction on balancing pin

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
NTC GPIOx overtemperature (x = 0, 1)	• If the GPIOx voltage falls below $V_{NTCx_OT_GPIOx_UV_TH}$,the NTC<x>_OT_GPIO<x>_UV fault is acknowledged	• The NTC<x>_OT_GPIO<x>_UV flag is set • Balancing is frozen on all cells • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• For channels configured as balancing cooldown (BAL_COOLDOWN_EN<x> = 1), if the GPIOx voltage rises above $V_{NTCx_OT_GPIOx_UV_TH}$ + $V_{NTC_OT_HYS}$ the NTC<x>_OT_GPIO<x>_UV flag can be cleared by MCU • For channels configured as cell NTCs (BAL_COOLDOWN_EN<x> = 0), if the GPIOx voltage rises above $V_{NTCx_OT_GPIOx_UV_TH}$,the NTC<x>_OT_GPIO<x>_UV flag can be cleared by MCU	• For channels configured as balancing cooldown (BAL_COOLDOWN_EN<x> = 1), the balancing is automatically re-engaged if the release condition is verified, even without NTC<x>_OT_GPIO<x>_UV flag clear • For channels configured as cell NTCs (BAL_COOLDOWN_EN<x> = 0), the balancing is re-engaged only when NTC<x>_OT_GPIO<x>_UV flag is cleared • FAULT pin is released	• GPIO<x>_CONF different than 00/01 masks measurement execution. In this case, the NTC<x>_OT_GPIO<x>_UV flag can always be cleared • NTC<x>_OT_BAL_MSK=1 masks reaction on balancing pin
NTC AINx fast charge overtemperature (x = 2, …, 5)	• If the AINx voltage falls below $V_{NTCx_FASTCHG_OT_GPIOx_WARN_UV_TH}$,the NTC<x>_FASTCHG_OT fault is acknowledged	• The NTC<x>_FASTCHG_OT flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the AINx voltage rises above $V_{NTCx_FASTCHG_OT_GPIOx_WARN_UV_TH}$,the NTC<x>_FASTCHG_OT flag can be cleared by MCU	• FAULT pin is released	• When NTC<x>_EN=0, the NTC<x> temperature diagnostics is masked, the NTC<x>_FASTCHG_OT flag can always be cleared
NTC GPIOx fast charge overtemperature (x = 0, 1)	• If the GPIOx voltage falls below $V_{NTCx_FASTCHG_OT_GPIOx_WARN_UV_TH}$,the NTC<x>_FASTCHG_OT_GPIO<x>_WARN_UV fault is acknowledged	• The NTC<x>_FASTCHG_OT_GPIO<x>_WARN_UV flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the GPIOx voltage rises above $V_{NTCx_FASTCHG_OT_GPIOx_WARN_UV_TH}$,the NTC<x>_FASTCHG_OT_GPIO<x>_WARN_UV flag can be cleared by MCU	• FAULT pin is released	• GPIO<x>_CONF different than 00/01 masks measurement execution. In this case, the NTC<x>_FASTCHG_OT_GPIO<x>_WARN_UV flag can always be cleared

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
NTC AINx under temperature (x = 2, …, 5)	• If the AINx voltage rises above $V_{NTCx_UT_TH}$,the NTC<x>_UT fault is acknowledged	• The NTC<x>_UT flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the AINx voltage falls below $V_{NTCx_UT_TH}$,the NTC<x>_UT flag can be cleared by MCU	• FAULT pin is released	• When NTC<x>_EN=0, the NTC<x> temperature diagnostics is masked, the NTC<x>_UT flag can always be cleared
NTC GPIOx under temperature (x = 0, 1)	• If the GPIOx voltage rises above $V_{NTCx_UT_GPIOx_OV_TH}$,the NTC<x>_UT_GPIO<x>_OV fault is acknowledged	• The NTC<x>_UT_GPIO<x>_OV flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the GPIOx voltage falls below $V_{NTCx_UT_GPIOx_OV_TH}$,the NTC<x>_UT_GPIO<x>_OV flag can be cleared by MCU	• FAULT pin is released	• GPIO<x>_CONF different than 00/01 masks measurement execution. In this case, the NTC<x>_UT_GPIO<x>_OV flag can always be cleared

4.4.4.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 43. NTC measurement electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
$N_{BIT_ADCV_NTC}$	ADC bit number	Design info		15		bit	AINx, GPIOx
$V_{ADCV_NTC_DIFF_FS}$	ADC full scale differential input voltage	Design info	0		$1.2*V_{VTREF}$	V	AINx, GPIOx
$V_{ADCV_NTC_DIFF_OP}$	ADC operating differential input voltage	Design info	$V_{VTREF}/50$		V_{VTREF}	V	AINx, GPIOx
$V_{ADCV_NTC_RES}$	ADC resolution (LSB)	Design info. LSB calculated on DIFF_FS		$1.2*V_{VTREF}/2^{15}$		V	AINx, GPIOx
$I_{NTC_LEAK_105}$	NTC pins leakage current (low)	$-40°C \le T_J \le +105°C$			150	nA	AINx, GPIOx
$I_{NTC_LEAK_125}$	NTC pins leakage current (high)	$+105°C \le T_J \le +125°C$			300	nA	AINx, GPIOx
$V_{ADCV_NTC_OFFSET_105}$	ADC offset conversion error, including post-soldering and ageing effects(1)	$-40°C \le T_J \le +105°C$	-4		4	LSB	AINx, GPIOx
$V_{ADCV_NTC_GAIN_105}$	ADC gain conversion error, including post-soldering and ageing effects(1)	$-40°C \le T_J \le +105°C$	-0.1		0.1	%	AINx, GPIOx
$V_{ADCV_NTC_OFFSET_125}$	ADC offset conversion error, including post-soldering and ageing effects(1)	$+105°C \le T_J \le +125°C$	-5		5	LSB	AINx, GPIOx
$V_{ADCV_NTC_GAIN_125}$	ADC gain conversion error, including post-soldering and ageing effects(1)	$+105°C \le T_J \le +125°C$	-0.2		0.2	%	AINx, GPIOx
$V_{ADCV_NTC_OFFSET_150}$	ADC offset conversion error, including post-soldering and ageing effects(1)	$+125°C \le T_J \le +150°C$	-6		6	LSB	AINx, GPIOx
$V_{ADCV_NTC_GAIN_150}$	ADC gain conversion error, including post-soldering and ageing effects(1)	$+125°C \le T_J \le +150°C$	-0.5		0.5	%	AINx, GPIOx
$V_{ADCV_NTC_NOISE_000}$	Standard deviation over a population of 100 samples	ADCV_FIL = 000			6	LSB_{RMS}	AINx, GPIOx
$V_{ADCV_NTC_NOISE_001}$		ADCV_FIL = 001			2	LSB_{RMS}	
$V_{ADCV_NTC_NOISE_010}$		ADCV_FIL = 010			1	LSB_{RMS}	
$V_{ADCV_NTC_NOISE_011}$		ADCV_FIL = 011			1	LSB_{RMS}	
$V_{ADCV_NTC_NOISE_100}$		ADCV_FIL = 100			1	LSB_{RMS}	
$V_{ADCV_NTC_NOISE_101}$		ADCV_FIL = 101			1	LSB_{RMS}	
$V_{ADCV_NTC_NOISE_110}$		ADCV_FIL = 110			1	LSB_{RMS}	
$V_{ADCV_NTC_NOISE_111}$		ADCV_FIL = 111			1	LSB_{RMS}	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
$V_{NTC_OT_TH}$	Programmable NTC AINx OT threshold (8 bit, one threshold for each channel (x = 2, …, 5)), $V_{NTC_{OT_{TH}}} = 32V_{ADCV_NTC_{RES}} * CODE$	NTC<x>_OT_TH	0		$(1.2*V_{VTREF}/2^{15}) * 32 * (2^8-1)$	V	AINx
$V_{NTC_OT_HYS}$	Programmable NTC OT threshold hysteresis (4 bit, steps of 128LSB), $V_{NTC_{OT_{HYS}}} = 128V_{ADCV_NTC_{RES}} * CODE$	NTC_TH_HYS	0		$(1.2*V_{VTREF}/2^{15}) * 128 * (2^4-1)$	V	AINx
$V_{NTC_OT_GPIO_UV_TH}$	Programmable NTC GPIOx OT threshold (8 bit, one threshold for each channel (x = 0, 1)), $V_{NTC_{OTGPIO_{UV_{TH}}}} = 32V_{ADCV_NTC_{RES}} * CODE$	NTC<x>_OT_GPIO<x>_UV_TH	0		$(1.2*V_{VTREF}/2^{15}) * 32 * (2^8-1)$	V	GPIOx
$V_{NTC_FASTCHG_OT_GPIO_WARN_UV_TH}$	Programmable NTC AINx fast charge OT threshold (5 bit, steps of 128LSB, one threshold for each channel (x = 2, …, 5)), $V_{NTC_{FASTCHG_{OTGPIO_{WARNG_{UV_{TH}}}}}} = V_{NTC_{OT_{TH}}} + 128V_{ADCV_NTC_{RES}} * CODE$	NTC<x>_FASTCHG_OT_GPIO<x>_WARN_UV_TH	0		$V_{NTC_OT_TH} + 128*(1.2*V_{VTREF}/2^{15}) * (2^5-1)$	V	AINx
$V_{NTC_FASTCHG_OT_GPIO_WARN_UV_TH}$	Programmable NTC GPIOx fast charge OT threshold (5 bit, steps of 128LSB, one threshold for each channel (x = 0, 1)), $V_{NTC_{FASTCHG_{OTGPIO_{WARNG_{UV_{TH}}}}}} = V_{NTC_{OTGPIO_{UV_{TH}}}} + 128V_{ADCV_NTC_{RES}} * CODE$	NTC<x>_FASTCHG_OT_GPIO<x>_WARN_UV_TH	0		$V_{NTC_OT_GPIO_UV_TH} + 128*(1.2*V_{VTREF}/2^{15}) * (2^5-1)$	V	GPIOx
$V_{NTC_UT_TH}$	Programmable NTC AINx UT threshold (8 bit, one threshold for each channel (x = 2, …, 5)), $V_{NTC_{UT_{TH}}} = 128V_{ADCV_NTC_{RES}} * CODE$	NTC<x>_UT_TH	0		$(1.2*V_{VTREF}/2^{15}) * 128 * (2^8-1)$	V	AINx
$V_{NTC_UT_GPIO_OV_TH}$	Programmable NTC GPIOx UT threshold (8 bit, one threshold for each channel (x = 0, 1)), $V_{NTC_{UTGPIO_{OV_{TH}}}} = 128V_{ADCV_NTC_{RES}} * CODE$	NTC<x>_UT_GPIO<x>_OV_TH	0		$(1.2*V_{VTREF}/2^{15}) * 128 * (2^8-1)$	V	GPIOx

1. *[1]. Single-shot samples are characterized by a superimposed Gaussian noise, with zero-mean and VADCV_NTC_NOISE standard deviation*

4.4.5 GPIO absolute conversion (GPIOx)

During the conversion step, the GPIO0 and GPIO1 can also be used to convert signals from sensors other than NTCs. To do so, GPIOs shall be configured for absolute measurement (refer to Section 4.9). GPIO measurements are stored in the corresponding NTC<x>_GPIO<x>_MEAS (x = 0, 1) registers along with the corresponding DATA_READY<x> bit. This latch is set upon the generation of a new measurement result, and it is cleared upon read. Unused GPIOs shall be connected to AGND. They shall be left programmed as analog input (refer to Section 4.9).

To calculate the GPIO absolute measurements at GPIOx pins in the voltage conversion routine, for example, AINx_GPIOx_MEAS, see below for calculation.

$V_{AINx_GPIOx_MEAS}$ = $V_{ADCV_NTC_RES}$ * (15-bit AINx_GPIOx_MEAS register CODE converted in decimal value), in which

$V_{ADCV_GPIO_RES} = 6/2^{15}$ **V**

15-bit AINx_GPIOx_MEAS register CODE = 0x3555 = 13653

Therefore, $V_{AINx_GPIOx_MEAS} = 6/2^{15} * 13653 = 2.499V$.

4.4.5.1 Diagnostics

Table 44. GPIO conversion diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
GPIOx Undervoltage (x = 0, 1)	• If the GPIOx voltage falls below $V_{NTCx_OT_GPIOx_UV_TH}$ the NTC<x>_OT_GPIO<x>_UV fault is acknowledged	• The NTC<x>_OT_GPIO<x>_UV flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the GPIOx voltage rises above $V_{NTCx_OT_GPIOx_UV_TH}$ the NTC<x>_OT_GPIO<x>_UV flag can be cleared by MCU	• FAULT pin is released	• GPIO<x>_CONF different than 00/01 masks measurement execution. In this case the NTC<x>_OT_GPIO<x>_UV flag can always be cleared
GPIOx Warn Undervoltage (x = 0, 1)	• If the GPIOx voltage falls below $V_{NTCx_FASTCHG_OT_GPIOx_WARN_UV_TH}$ the NTC<x>_FASTCHG_OT_GPIO<x>_WARN_UV fault is acknowledged	• The NTC<x>_FASTCHG_OT_GPIO<x>_WARN_UV flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the GPIOx voltage rises above $V_{NTCx_FASTCHG_OT_GPIOx_WARN_UV_TH}$ the NTC<x>_FASTCHG_OT_GPIO<x>_WARN_UV flag can be cleared by MCU	• FAULT pin is released	• GPIO<x>_CONF different than 00/01 masks measurement execution. In this case the NTC<x>_FASTCHG_OT_GPIO<x>_WARN_UV flag can always be cleared
GPIOx Overvoltage (x = 0, 1)	• If the GPIOx voltage rises above $V_{NTCx_UT_GPIOx_OV_TH}$ the NTC<x>_UT_GPIO<x>_OV fault is acknowledged	• The NTC<x>_UT_GPIO<x>_OV flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If the GPIOx voltage rises above $V_{NTCx_UT_GPIOx_OV_TH}$ the NTC<x>_UT_GPIO<x>_OV flag can be cleared by MCU	• FAULT pin is released	• GPIO<x>_CONF different than 00/01 masks measurement execution. In this case the NTC<x>_UT_GPIO<x>_OV flag can always be cleared

4.4.5.2 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 45. GPIO measurement electrical parameters (absolute)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
$N_{BIT_ADCV_GPIO}$	ADC bit number	Design info		15		bit	GPIOx
$V_{ADCV_GPIO_DIFF_FS}$	ADC full-scale differential input voltage	Design info	0		6	V	GPIOx
$V_{ADCV_GPIO_DIFF_OP}$	ADC operating differential input voltage	Design info	0.1		5	V	GPIOx
$V_{ADCV_GPIO_RES}$	ADC resolution (LSB)	Design info. LSB calculated on DIFF_FS		$6/2^{15}$		V	GPIOx

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
$I_{GPIO_LEAK_105}$	GPIO pins leakage current (low)	-40°C ≤ T_J ≤ +105°C			150	nA	GPIOx
$I_{GPIO_LEAK_125}$	GPIO pins leakage current (high)	+105°C ≤ T_J ≤+125°C			300	nA	GPIOx
$V_{ADCV_GPIO_NOISE_000}$	Standard deviation over a population of 100 samples	ADCV_FIL = 000			1000	μV_{RMS}	GPIOx
$V_{ADCV_GPIO_NOISE_001}$		ADCV_FIL = 001			400	μV_{RMS}	
$V_{ADCV_GPIO_NOISE_010}$		ADCV_FIL = 010			150	μV_{RMS}	
$V_{ADCV_GPIO_NOISE_011}$		ADCV_FIL = 011			150	μV_{RMS}	
$V_{ADCV_GPIO_NOISE_100}$		ADCV_FIL = 100			100	μV_{RMS}	
$V_{ADCV_GPIO_NOISE_101}$		ADCV_FIL = 101			100	μV_{RMS}	
$V_{ADCV_GPIO_NOISE_110}$		ADCV_FIL = 110			100	μV_{RMS}	
$V_{ADCV_GPIO_NOISE_111}$		ADCV_FIL = 111			100	μV_{RMS}	
$V_{ADCV_GPIO_TOTAL_ERR_125}$	ADC total conversion error, including post-soldering and ageing effects[1]	0V < V_{GPIO} < 5V, -40°C≤ T_J ≤+125°C	-6		6	mV	GPIOx
$V_{NTC_OT_GPIO_UV_TH}$	Programmable GPIOx UV threshold (8 bit, one threshold for each channel, (x = 0, 1)), $V_{NTC_{OT}GPIO_{UV_{TH}}} = 32V_{ADCV_GPIO_{RES}} * CODE$	NTC<x>_OT_GPIO<x>_UV_TH	0		$(6/2^{15})$ * 32 * (2^8-1)	V	GPIOx
$V_{NTC_FASTCHG_OT_GPIO_WARN_UV_TH}$	Programmable GPIOx warn UV OT threshold (5 bit, steps of 128LSB, one threshold for each channel, (x = 0, 1)), $V_{NTC_{FASTCHG_{OT}GPIO_{WARNG_{UV_{TH}}}}} = V_{NTC_{OT}GPIO_{UV_{TH}}} + 128V_{ADCV_NTC_{RES}} * CODE$	NTC_FASTCHG_OT_GPIO_WARN_UV_TH	0		$V_{NTC_OT_GPIO_UV_TH}$ + 128*(1.2*V_{VTREF}/2^{15}) * (2^5-1)	V	GPIOx
$V_{NTC_UT_GPIO_OV_TH}$	Programmable GPIOx OV threshold (8 bit, one threshold for each channel, (x = 0, 1)), $V_{NTC_{UT}GPIO_{OV_{TH}}} = 128V_{ADCV_GPIO_{RES}} * CODE$	NTC<x>_UT_GPIO<x>_OV_TH	0		$(6/2^{15})$ * 128 * (2^8-1)	V	GPIOx

1. *[1]. Single-shot samples are characterized by a superimposed Gaussian noise, with zero-mean and VADCV_GPIO_NOISE standard deviation*

4.4.6 AIN open load diagnostic

This diagnostic allows detecting open load failures on the analog inputs AIN2, …, AIN5 connected to the NTCs. When triggered by the command DIAG_STEP = 1, the following diagnostic routine is executed in parallel on all analog input pins (see Figure 18 in Section 4.4):

- The $I_{AIN_OPEN_DIAG}$ pulld-own current is enabled on the AINx pins
- The IC performs absolute conversion of the AINx pin using the temporal window **T_{ADCV_START}**+ **$T_{ADCV_OPEN_DIAG}$**, and processes the information as indicated in the following table.

The AIN open load diagnostics step in the voltage conversion routine, with a focus on the pull-down current $I_{AIN_OPEN_DIAG}$,is shown in Figure 20 in Section 4.4.3.

4.4.6.1 Diagnostics

Table 46. AIN open load diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
AIN open (x = 2, …, 5)	• If the AIN_X voltage falls below $V_{AIN_OPEN_TH}$, the AIN<x>_OPEN fault is acknowledged	• The AIN<x>_OPEN flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• The AIN<x>_OPEN field can always be cleared on read	• FAULT pin is released	• When NTC<x>_EN=0, the AIN<x> open load diagnostic is masked, the AIN<x>_OPEN flag can always be cleared

4.4.6.2 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 47. AIN open load diagnostic electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$I_{AIN_OPEN_DIAG}$	AIN open load diagnostic pull-down current	$V_{AINx} \geq 1.5$ V	10		100	µA	AINx
$V_{AIN_OPEN_TH}$	AIN open load threshold			200		mV	AINx

4.4.7 GPIO open load diagnostic

This diagnostic allows detecting open load failures on GPIO0 and GPIO1 if configured as analog inputs (GPIO<x>_CONF = 00/01, x = 0,1). When triggered by the command DIAG_STEP = 1, the following diagnostic routine is executed in parallel on the GPIOs (see Figure 18 in Section 4.4):

- The $I_{GPIO_OPEN_DIAG}$ pull-down current is enabled on the GPIOx pins
- The IC performs absolute conversion of the GPIOx pin (regardless of the GPIO<x>_CONF setting) using the temporal window $\mathbf{T_{ADCV_START}+T_{ADCV_OPEN_DIAG}}$, and processes the information as indicated in the following table.

The GPIO open load diagnostics step in the voltage conversion routine, with a focus on the pull-down current $I_{GPIO_OPEN_DIAG}$, is shown in Figure 20 in Section 4.4.3.

4.4.7.1 Diagnostics

Table 48. GPIO open load diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
GPIOx open (x = 0, 1)	• If the $GPIO_X$ voltage falls below $V_{GPIO_OPEN_TH}$, the AIN<x>_GPIO<x>_OPEN fault is acknowledged	• The AIN<x>_GPIO<x>_OPEN flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• The AIN<x>_GPIO<x>_OPEN field can always be cleared on read	• FAULT pin is released	• GPIO<x>_CONF different than 00/01 masks diagnostic execution, in this case the AIN<x>_GPIO<x>_OPEN flag can always be cleared

4.4.7.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 49. GPIO open load diagnostic electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$I_{GPIO_OPEN_DIAG}$	GPIO open load diagnostic pull-down current	$V_{GPIOx} \geq 1.5V$	10		100	µA	GPIOx
$V_{GPIO_OPEN_TH}$	GPIO open load threshold			200		mV	GPIOx

4.4.8 ADC Built-In-Self-Test (ADCV BIST)

The L9988 allows testing the integrity of the ADCs. The routine is designed to validate the full ADC input characteristics using a two setpoint check, covering both offset and gain errors.

This diagnostic is executed in parallel on all ADCs.

The combination of Built-In-Self-Test (BIST) and GPIO/AIN Open Load Diagnostic also covers the integrity of the GPIOx and AINx conversion paths.

When the DIAG_STEP = 1 in the voltage conversion routine, the following procedure is executed:

Procedure 1 – ADCV BIST

1. The pins are disconnected from the inputs and an internal short-circuit is applied between the corresponding differential inputs
2. The L9988 converts the input above using the configured filter time T_{ADCV_FILTER} window and checks if the error is bigger than $V_{OFFSET_BIST_TH}$
3. The pins are kept disconnected from the inputs and an internal reference voltage (VREF1 and VREF2 depending on the setting of ADC_SWAP bit) is applied between the corresponding differential inputs
4. The L9988 converts the input above using the configured filter time T_{ADCV_FILTER} window and checks if the error is bigger than $V_{GAIN_BIST_TH}$.

If an error is detected in step 2 or 4, the corresponding VCR_BIST_FAIL 4-bit field is set.

4.4.8.1 *Fault injection*

To allow MCU self-testing of recovery procedures, the VCR_FAULT_INJ field allows injecting a BIST fail on every ADC.

If VCR_FAULT_INJ = 1, the BIST fault injection is also performed on the redundant internal blocks. The expected result of fault injection diagnostic is:

- VCR_BIST_FAIL = 1111
- VCR_RED_CHECK_FAIL = 1

VCR_FAULT_INJ is cleared automatically at the end of the voltage conversion routine.

To clear VCR_BIST_FAIL and VCR_RED_CHECK_FAIL, a new voltage conversion routine (with DIAG_STEP = 1) without fault injection is needed.

4.4.8.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 50. ADCV BIST electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{OFFSET_BIST_TH}$	ADC conversion error threshold for the offset check of the BIST phase				15	mV	-
$V_{GAIN_BIST_TH}$	ADC conversion error threshold for the gain check of the BIST phase				15	mV	-

4.4.9 ADC Swapping (ADCV SWAP)

To ensure redundancy, each even/odd ADC pair can be swapped after the execution of the voltage conversion routine by programming **ADC_SWAP = 1** in the Start of Conversion (SOC) frame. This happens for all cell voltages (cell 1, …, cell 4), all analog inputs (AIN2, …, AIN5) and GPIOs (GPIO0, GPIO1).

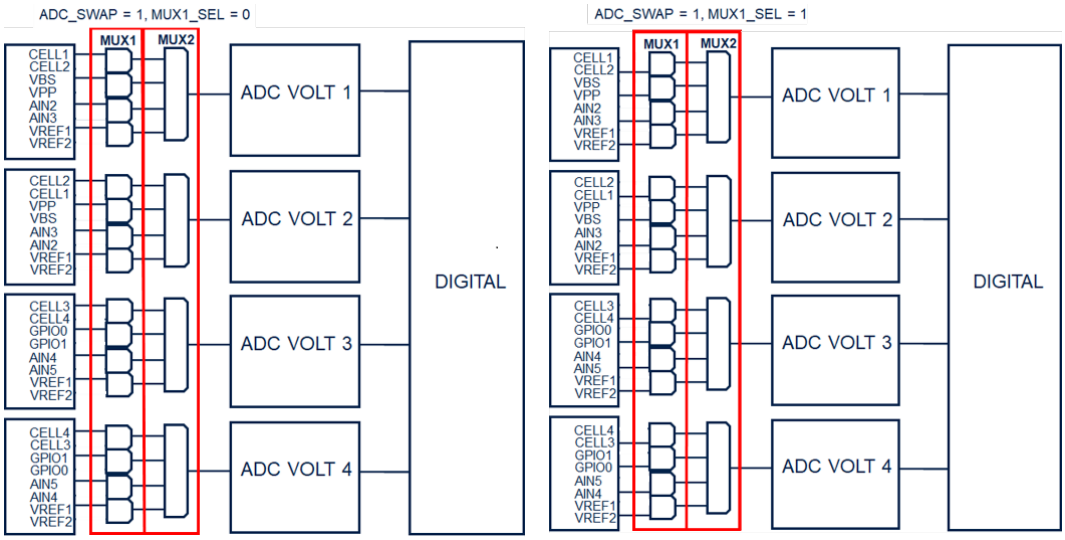
Since even/odd ADC pairs are referenced to independent voltages, this ensures full redundancy for both voltage and temperature measurements. ADC swapping also ensures that redundant measurements are executed with the same functional accuracy. Additionally, all redundant conversion paths are checked as discussed in the Built-In-Self-Test (BIST) section.

If one ADC of the even/odd pair is faulty, this feature allows keeping the OV/UV/OT/UT detection functionality by swapping the ADCs at each iteration of the voltage conversion routine.

In the register map, the bit SWAP_ECHO will toggle at the end of the voltage conversion routine if the ADC_SWAP bit was set to 1 in the SOC request frame. This will return the current status of the ADC swapping selector.

In case the ADC_SWAP bit is set to 0, the ADC swapping is disabled as soon as the voltage conversion routine is finished and reported in SWAP_ECHO.

Figure 21. **ADC swapping**



MUX1 is managed by the internal signal **MUX1_SEL** according to the ADC_SWAP configuration bit:

- If ADC_SWAP=0, MUX1_SEL is always set to 0 and ADCs convert first MUX1 inputs
- If ADC_SWAP=1 MUX1_SEL continuously toggle between 0 and 1 at the end of each VCR

Regarding the MUX2 selector, it is controlled by the voltage conversion routine internal logic allowing for the consecutive different channel conversion (for example, considering ADC_VOLTAGE 1, the first conversation is CELL1, next convention is VBS and so on, according to the MUX2 selector).

Figure 22. **MUX1_SEL behavior**

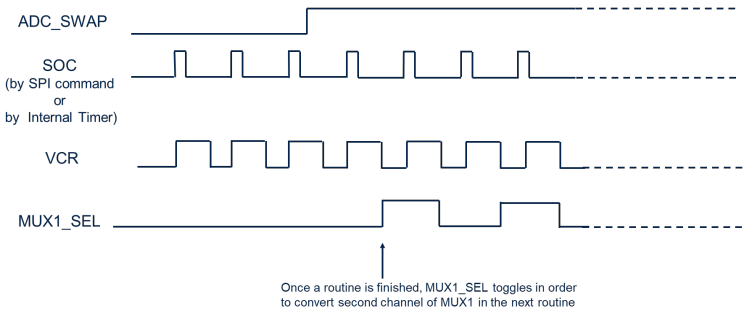


Figure 23. Timing diagram of two consecutive voltage conversion steps if ADC_SWAP = 1

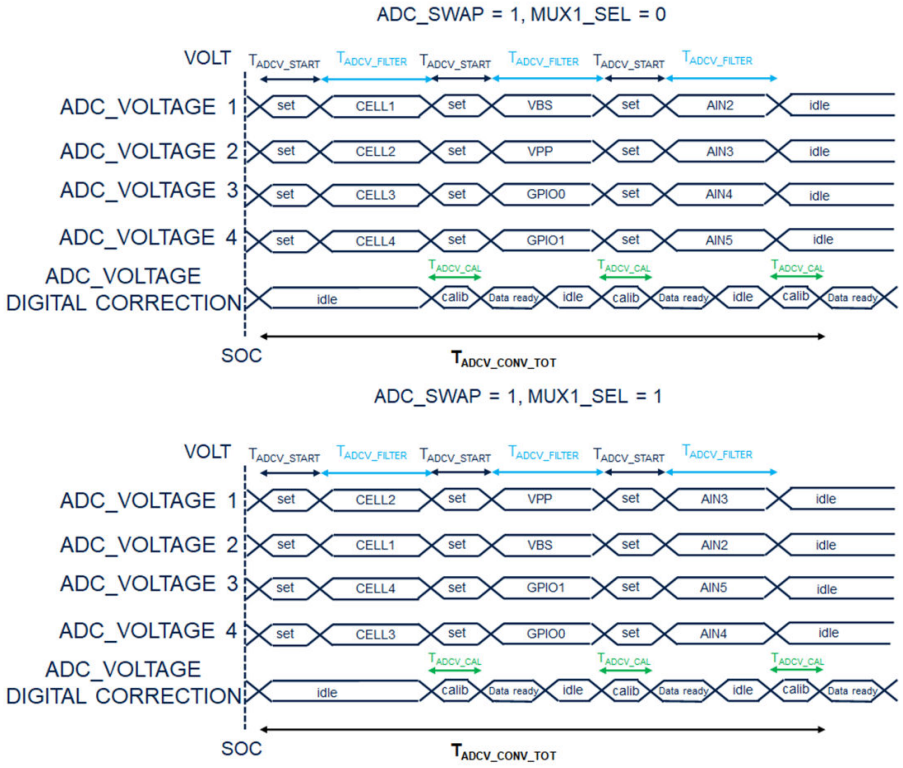
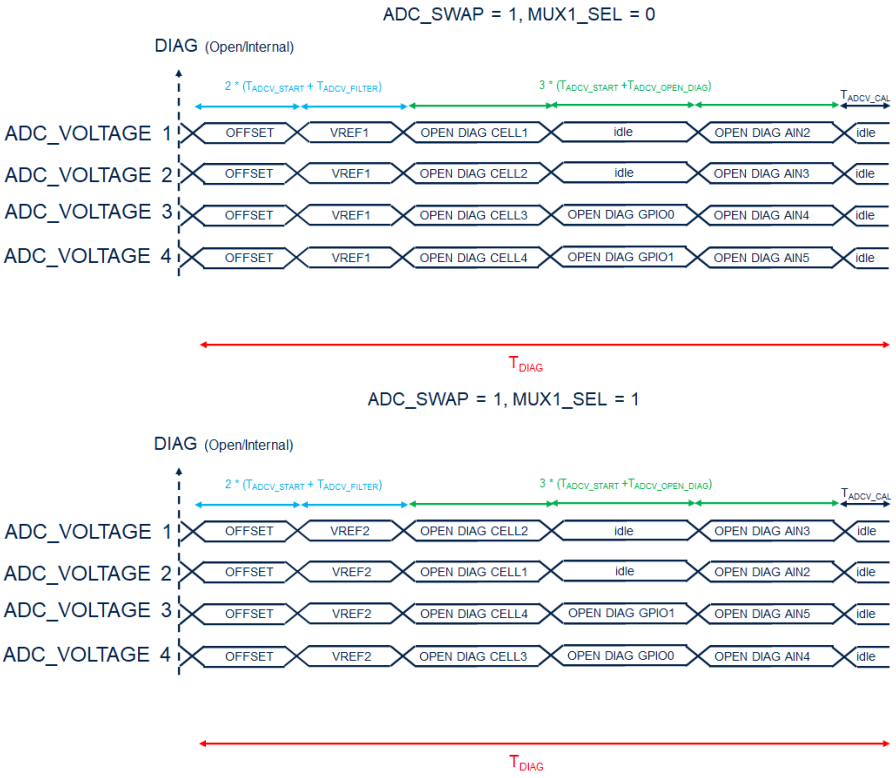


Figure 24. Timing diagram of two consecutive diagnostics steps in VCR if ADC_SWAP = 1



4.4.10 Gain adjustment (GAIN ADJ)

To ensure accuracy in the device lifetime also considering ADCs components ageing, the device embeds a self-gain adjustment function.

This procedure is performed automatically in parallel to the ADCV BIST step, and to cover all the ADCs, two voltage conversion routines with DIAG_STEP =1 and ADC_SWAP = 1 (refer to Figure 24) are needed; furthermore, the gain adjustment effect is visible after these two VCRs.

The accuracy performances reported in Table 39, Table 41, Table 43 and Table 45 are obtained by performing the gain adjustment steps every transition in NORMAL mode and TJ variation of 10deg. The gain adjustment is implemented in NORMAL mode and in STANDBY mode for the whole device lifetime.

4.5 Cell balancing FETs (Sx)

The L9988 provides passive internal balancing, allowing the discharging of cells by means of external resistors.

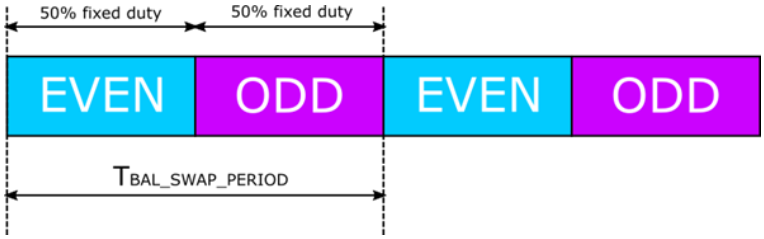
4.5.1 Balancing modes

The IC implements both **Timed** and **PWM-Based** balancing modes. They can be selected through the BAL_MODE bit, which is latched at the beginning of the balancing (BAL_START 0 → 1) and cannot be changed on-the-fly while balancing is running.

To allow balancing both odd and even cells in a single thread, the balancing controller offers the possibility of enabling a time-window multiplexing strategy. The MCU may enable the odd/even swapping by programming BAL_SWAP = 1 and configuring the swapping period through the BAL_SWAP_PERIOD field. The BAL_SWAP setting is latched upon balancing start (BAL_START 0 → 1) and cannot be updated on-the-fly.

The BAL_SWAP_PERIOD can instead be updated on-the-fly and the change will take effect after $T_{BAL_SWAP_UPDATE}$.

Figure 25. Balancing swap strategy



4.5.1.1 *Timed*

The timed mode is recommended for long, pre-calculated balancing intervals. To configure and launch it, follow this procedure:

Procedure 2 – Timed balancing setup

1. Program BAL_MODE = 0
2. Select the cells to be discharged programming BAL<x>_ON = 1
3. Set the balancing timer pre-scaler programming BAL_PRE_SCAL
4. Program the timer threshold (BAL<x>_TH) for each enabled cell
5. (optional) Enable the balancing swap programming BAL_SWAP = 1 and configuring the BAL_SWAP_PERIOD field to select how often the balancing automatically toggles from even to odd cells.
6. Start the balancing programming BAL_START = 1.
7. The internal balancing timer is reset and started. It is then continuously compared to each channel threshold to evaluate the balancing stop condition (BAL_TIMER >= BAL<x>_TH). The timer status is reported in the BAL_TIMER register.

Note: Since the common BAL_TIMER keeps running while even/odd channels are in their OFF phase, the BAL<x>_TH thresholds shall be programmed considering the 50% duty-cycle due to the odd/even swap activity. Therefore, the threshold shall be set at twice the effective calculated balancing period.

Once the balancing is running on a cell:

- The MCU may temporarily pause/re-engage it toggling the BAL<x>_ON bit. This is only valid for channels that were initially set for balancing, meaning that their corresponding enabled bit (BAL<x>_ON) was set to '1' upon the BAL_START 0 → 1 transition. To add new channels to the balancing, the thread has to be restarted applying the new configuration and toggling the BAL_START bit.
  - Additionally, certain failures (e.g. NTC OT, Cell UV, Cell Balancing UV, etc.) have the same effect as a pause commanded by the MCU. If a failure is present, balancing is inhibited. It is released when the fault disappears, and corresponding flag is cleared by the MCU, unless something different is indicated in the dedicated section (refer to BAL OVC in Section 4.5.3.1 section).
- The MCU may update the BAL<x>_TH threshold anytime
  - To restart balancing on a cell whose threshold has already been exceeded, simply read the BAL_TIMER and update the BAL<x>_TH accordingly

$$BAL_{XTHNEW} = BAL_{TIMER} + \Delta BAL_{XTH} \quad (1)$$

- The MCU may stop balancing anytime programming BAL_START = 0
  - In this case, BAL_TIMER will be forced to saturate to its upper bound, so that the stop condition is verified on all cells.

4.5.1.2 *PWM-based*

The IC also enables individual cell balancing with a programmable PWM duty-cycle. The PWM period is fixed to $T_{BAL_PWM_PERIOD}$, while the duty-cycle can be dynamically adjusted via SW programming the $T_{BAL_PWM_DUTY}$ in 32 steps.

The PWM-based mode is recommended for real-time balancing strategies. The following procedure shall be executed to initiate and manage the PWM balancing task:

Procedure 3 – PWM-based balancing setup

1. Program BAL_MODE = 1
2. Select the cells to be discharged by programming BAL<x>_ON = 1
3. Program the cell duty-cycle in respect to $T_{BAL_PWM_PERIOD}$, writing the BAL<x>_TH register. The LSBs of these registers are reused to define the duty-cycle.
4. (optional) Enable the balancing swap by programming BAL_SWAP = 1 and configuring the BAL_SWAP_PERIOD field to select how often the balancing automatically toggles from even to odd cells. The swap period timer is designed to be an integer multiple of $T_{BAL_PWM_PERIOD}$, so that swapping always occurs at the beginning of a PWM cycle and no truncated PWM periods happen.
5. Program the safety timer watchdog threshold $T_{BAL_TIMER_MAX}$ in the BAL_TIMER_MAX_TH register. This will define the maximum task duration.
6. Start the balancing programming BAL_START = 1. Balancing on individual channels can then be fine-tuned by changing the BAL<x>_TH (sampled every $T_{BAL_PWM_PERIOD}$) and BAL<x>_ON, but the safety timer will keep running in the background. The safety timer status is reported in the BAL_TIMER register.

Note: When enabling the balancing swap, the effective cell balancing duty-cycle will be half the programmed one. For instance, programming a 100% duty-cycle on a cell will result in the cell being balanced 50% of the time.

Note: In case balancing swap is disabled (BAL_SWAP = 0), balancing adjacent cells results in an increment in the balancing current (approximately twice the single cell current). The overcurrent protection might be inadvertently triggered.

Once the balancing is running on a cell:

- The MCU may temporarily pause/re-engage it toggling the BAL<x>_ON bit. This is only valid for channels that were initially set for balancing, meaning that their corresponding enabled bit (BAL<x>_ON) was set to '1' upon the BAL_START 0 → 1 transition. To add new channels to the balancing, the thread must be restarted by applying the new configuration and toggling the BAL_START bit.
  - Additionally, certain failures (e.g., NTC OT, Cell UV, Cell Balancing UV, etc.) have the same effect as a pause commanded by the MCU. If failure is present, balancing is inhibited. It is released when the fault disappears, and the corresponding flag is cleared by the MCU, unless something different is indicated in the dedicated section (refer to BAL OVC in Section 4.5.3.1 section).
- The MCU may update the PWM duty-cycle by writing the BAL<x>_TH time.
  - The modification will take effect at the end of the ongoing PWM cycle.
- The MCU may update the BAL_TIMER_MAX_TH threshold anytime
- The MCU may stop balancing anytime by programming BAL_START = 0.
  - In this case, BAL_TIMER will be forced to saturate to its upper bound, so that the stop condition is verified on all cells.

4.5.2 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 51. Balancing electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
R_{DSON_BAL}	Balancing FET resistance	NORMAL, T_J = 150°C			2	Ω	Sx
I_{BAL}	Balancing current	Design Info			200	mA	Sx
$I_{BAL_LEAK_CONV}$	Balancing leakage current when converting				150	nA	Sx
T_{BAL_FALL}	Balancing FET V_{DS} fall time	From BAL<x> ON command to 10% of VDS 1V < V_{CELL} < 5V C_{BAL} = 68nF, R_{BAL} = 22Ω			10	µs	Sx
T_{BAL_RISE}	Balancing FET V_{DS} rise time	From BAL<x> OFF command to 90% of VDS 1V < V_{CELL} < 5V C_{BAL} = 68nF, R_{BAL} = 22Ω			25	µs	Sx
$T_{BAL_TIMER_0}$	Balancing timer threshold BAL<x>_TH (7 bit), $T_{BAL_{TIMER}} = 512s * CODE$	BAL_PRE_SCAL = 1	0		65024	s	Sx
$T_{BAL_TIMER_1}$	Balancing timer threshold BAL<x>_TH (7 bit), $T_{BALTIMER} = 4s * CODE$	BAL_PRE_SCAL = 0	0		508	s	Sx
$T_{BAL_SWAP_PERIOD}$	Balancing swap period between even and odd channels, available in Timed mode BAL_SWAP_PERIOD (3 bit), $T_{BALSWAPPERIOD} = 4s * 2^{CODE}$	Guaranteed by SCAN	4		512	s	Sx
$T_{BAL_SWAP_UPDATE}$	Balancing swap period settling time	Guaranteed by SCAN	3.5		555	s	Sx
$T_{BAL_PWM_PERIOD}$	Balancing base period for PWM mode	Guaranteed by SCAN	-8%	32	+8%	s	Sx
$T_{BAL_PWM_DUTY}$	Balancing ON period for PWM mode BAL<x>_TH(4:0) (5 bit), $T_{BAL_{PWM_{DUTY}}} = 1s * \left(CODE + 1\right)$	Guaranteed by SCAN	1		32	s	Sx
$T_{BAL_TIMER_MAX}$	Safety timer watchdog threshold used in PWM mode BAL_TIMER_MAX_TH (16 bit), $T_{BAL_{TIMER_{MAX}}} = 1s * CODE$	Guaranteed by SCAN	0		65535	s	Sx

4.5.3 Balancing Overcurrent detection (BAL OVC)

Balancing FETs are protected with overcurrent detection via VDS monitor:

This diagnostic is always active when balancing is enabled (STANDBY and NORMAL MODE) and covers the failures listed in the following table.

4.5.3.1 Diagnostics

Table 52. Balancing diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
BAL OVC	• When the balancing channel is turned ON, in case the FET current rises above I_{BAL_OC} for an interval longer than T_{BAL_OC}, the BAL<x>_OVC fault is acknowledged	• The BAL<x>_OVC flag is set • The balancing FET is turned OFF and BAL<x>_ON is reset • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• When the FET is in the OFF state, the BAL<x>_OVC flag can be cleared by MCU	• The Balancing FET is kept OFF and shall be re-engaged setting the BAL<x>_ON bit to 1 again • FAULT pin is released	• When BAL<x>_ON=0, the BAL<x> balancing diagnostic is masked, the BAL<x>_OVC flag can always be cleared • BAL_OVC_BAL_MSK=1 masks reaction on balancing pins (Sx)

4.5.3.2 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 53. Balancing overcurrent detection electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
I_{BAL_OC}	Balancing overcurrent threshold		400		1000	mA	Sx
T_{BAL_OC}	Balancing overcurrent filter time		16		22	µs	Sx

4.6 Ground loss detection (GND LOSS)

The L9988 implements two separated ground reference pins, a Digital Ground (DGND) dedicated as reference for the noisy internal analog/digital circuitry and an Analog Ground (AGND) dedicated to the low-power and sensitive internal analog circuitry.

A monitoring unit to detect disconnection of the digital ground affecting ground references is implemented. The GND LOSS monitor is active in NORMAL and STANDBY mode.

If $V_{DGND} - V_{AGND} \geq V_{TH_GND_LOSS}$ occurs for an interval longer than $T_{GND_LOSS_FIL}$, the GND_LOSS flag is set.

4.6.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 54. ADCV BIST electrical parameters

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	PIN
$V_{TH_GND_LOSS}$	Ground loss detection threshold		0.1	0.25	0.4	V	-
$T_{GND_LOSS_FIL}$	Ground loss filter time			300		µs	-

4.7 Current Conversion Routine (CCR)

The IC features a double pair of CSA pins, CSAN0/1 and CSAP0/1, which can be used

- to sense the instantaneous pack current with a(n) (over) current sense ADC **CS**
- to perform Coulomb Counting with a second independent ADC **CC**

4.7.1 (Over) Current Sense ADC (CS ADC)

The L9988 integrates a 20-bit fully differential sigma-delta ADC **CS** operating on the CSAP0 and CSAN0 pins and capable of performing acquisition of the pack instantaneous current using an external shunt resistor connected between the pins.

With a R_{SHUNT} equal to 100 µΩ, the CS can measure an operative current included in the range of (-1500A, 1500A) and a full-scale current between (-1800A, 1800A).

This CS can be enabled by programming CS_EN = 1.

The acquisition starts $\mathbf{T_{CS_START}}$ after the receival of the Start of Conversion (SOC) trigger command. It lasts $\mathbf{T_{CS_FILTER}}$, which is programmable using the **CS_FIL** 3-bit field. Moreover, a third time $\mathbf{T_{CS_CAL}}$ is necessary to post-elaborate the conversion data.

The total conversion time is $\mathbf{T_{CS_CONV} = T_{CS_START} + T_{CS_FILTER} + T_{CS_CAL}}$

The result of the last instantaneous current acquisition is available in the **CS_MEAS** register field, along with the corresponding **CS_DATA_READY** bit (clear-on-read), and it is encoded in 2's complement. Register data is always available in NORMAL, but it is reset once the device moves to any low-power state.

To calculate the instantaneous current measured on the CSAP0 and CSAN0 pins in the current conversion routine, see below for calculation.

$CS_{MEAS} = V_{CS_RES}$ * (20-bit CS_MEAS register CODE converted in decimal value)/ R_{shunt},

in which

$V_{CS_RES} = 0.18/2^{19}$ V

R_{shunt} = 100 µΩ

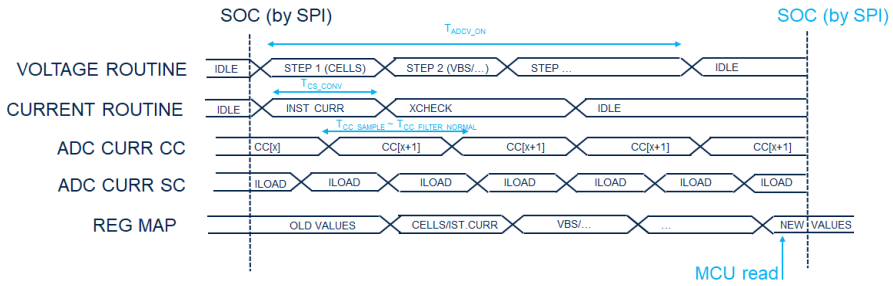
20-bit CS_MEAS register CODE = 0x23919 = 145689

Therefore, $V_{CS_MEAS} = (0.18/2^{19} * 145689) = 50$ mV and $CS_{MEAS} = V_{CS_MEAS} / R_{shunt} = 500$A

In NORMAL MODE, the instantaneous current measurement can be performed in the following way:

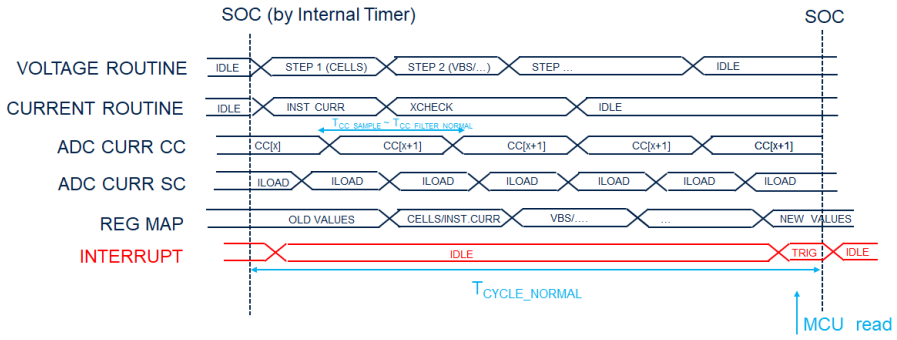
1. Start of Conversion (SOC) command by SPI
   - The MCU can send an SOC command, by writing the write-only field SPI_SOC in the CONV_SOC register, according to the T_{CS_CONV} and the T_{ADCV_ON} (defined in 4.4) time. Note that the voltage conversion routine is synchronized with the current conversion routine: the start of conversion of voltage cells is generated synchronously (in parallel) to the current sense ADC sampling trigger.
   - A new SOC command cannot interrupt or re-start an ongoing conversion, and the command is discarded.
   - After the end of voltage and current routines, the MCU can read the SPI registers with diagnostic results and conversions.
   - Diagnostics are executed only after SOC command, except for short-circuit detection (if enabled, continuously running)

Figure 26. Timing diagram of SOC command by SPI



2. Start of Conversion (SOC) command by internal timer
   - The MCU can configure an internal timer (using the HF main oscillator) to send a periodic SOC command every T_{CYCLE_NORMAL}, which is programmable using the 3-bit **CYCLE_NORMAL** field (refer to Section 4.4).
   - To synchronize internal routines with readout, the IC generates an interrupt at the end of routines to allow MCU SPI readout.
   - Diagnostics are executed automatically each T_{CYCLE_NORMAL}(flag set during single step),
   - except for short-circuit detection (if enabled, continuously running).
   - If the SOC internal timer is disabled during T_{CYCLE_NORMAL}, the routine will be not interrupted until its end. After that, a new SOC by SPI is accepted.

Figure 27. Timing Diagram of SOC command by Internal Timer



The MCU can switch from one mode to the other by the SPI configuration bit **SOC_SEL**. If SOC_SEL = 0 (default), the CCR is triggered by SPI command. If SOC_SEL = 1, the CCR is cyclically executed every T_{CYCLE_NORMAL} seconds.

SOC_SEL is automatically reset to 0 in STANDBY MODE to disable T_{CYCLE_NORMAL} trigger and allow the new $T_{CYCLE_STANDBY}$ (defined below) periodicity. In this way, as soon as the device exits STANDBY MODE going to NORMAL MODE, the CCR routine is waiting for a new SOC by SPI or enables again the internal timer setting SOC_SEL =1.

If the periodic SOC is selected, SOC by SPI will be no longer accepted and the internal mechanism starts at the end of current routine if running. If the periodic SOC is disabled, a SOC by SPI is accepted after the end of the last running routine, otherwise ignored.

No shadow register memory will be implemented, register map values are updated as soon as the conversions are ready. Therefore, the MCU can synchronize readout considering routine duration after a SOC by SPI or configuring interrupt generation for SOC by internal timer.

The status of the current routine is reported by the CCR_BUSY flag: when set, the routine is ongoing. In case a single routine step does not end within $T_{CCR_TIMEOUT}$, the CCR_FAIL latch is set (cleared upon read).

In STANDBY MODE, the CS will be cyclically activated for a duration $\mathbf{T_{CS_ON}}$(refer to Section 4.2.1) in the time period $\mathbf{T_{CYCLE_STANDBY}}$ (e.g.1s, defined by the Internal Real Time Clock RTC; refer to Section 4.13.1) to realize the cross-check (refer to Section 4.7.3) and the overcurrent detection (refer to Section 4.7.1.2).

Since in this state, the CS ADC and the CC ADC must be synchronous to automatically perform the cross-check, $\mathbf{T_{CS_FILTER}}$ must be aligned with the filter time $\mathbf{T_{CC_FILTER_STANDBY}}$of the Coulomb Counter defined in Section 4.7.2.1 (note that $T_{CC_FILTER_STANDBY}$ is a subset of T_{CS_FILTER}).

Then, $\mathbf{T_{CS_ON} = T_{CS_START} + T_{CS_FILTER} + T_{CS_CAL} = T_{CS_START} + T_{CC_FILTER_STANDBY} + T_{CS_CAL}}$

An example of a timing diagram of current conversion routine in STANDBY MODE with a focus on synchronism between CS and CC is shown in Section 4.7.2.

4.7.1.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range of Table 2; T_J according to the operating range of Table 5.

Table 55. Instantaneous current measurement electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{CS_DIFF_FS}$	CS ADC full scale differential input voltage, CSAP0 – CSAN0	Design info	-180		180	mV	CSAP0 CSAN0
$V_{CS_DIFF_OP}$	CS ADC operating differential input voltage, CSAP0 – CSAN0	Design info	-150		150	mV	CSAP0 CSAN0
$V_{CS_ABS_OR}$	Maximum differential voltage between CSAP0 or CSAN0 pin with respect to GND to have CS parameters guaranteed	Design info	-300		300	mV	CSAP0 CSAN0
N_{BIT_CS}	CS ADC bit number: encoding is in 2's complement	Design info		20		bit	CSAP0 CSAN0
V_{CS_RES}	CS ADC resolution	LSB calculated on DIFF_FS		$0.18/2^{20-1}$		V	CSAP0 CSAN0
T_{CS_START}	CS ADC settling time	Guaranteed by SCAN		60		µs	CSAP0 CSAN0
$T_{CS_FILTER_000}$	CS ADC filter time	CS_FIL = 000		136		µs	CSAP0 CSAN0
$T_{CS_FILTER_001}$		CS_FIL = 001		264		µs	
$T_{CS_FILTER_010}$		CS_FIL = 010		1.04		ms	
$T_{CS_FILTER_011}$		CS_FIL = 011		2.08		ms	
$T_{CS_FILTER_100}$		CS_FIL = 100		4.16		ms	
$T_{CS_FILTER_101}$		CS_FIL = 101		8.32		ms	
$T_{CS_FILTER_110}$		CS_FIL = 110		16.64		ms	
$T_{CS_FILTER_111}$		CS_FIL = 111		66.56		ms	
T_{CS_CAL}	CS ADC post-calibration time	Guaranteed by SCAN		27	35	µs	CSAP0 CSAN0

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$T_{CCR_TIMEOUT}$	Single routine step timeout	Guaranteed by SCAN		100		ms	-
CS_{OFFSET_ERR}	CS ADC offset error, including post-soldering and ageing effects(1)	CSAP0 and CSAN0 inputs shorted to GND on PCB. Guaranteed by test bench characterization	-6	0	6	LSB	CSAP0 CSAN0
$CS_{GAIN_ERR_105}$	CS ADC gain error, including nonlinearities, including post-soldering and ageing effects(1)	-40°C ≤ T_J ≤ +105°C	-0.1	0	0.1	%	CSAP0 CSAN0
$CS_{GAIN_ERR_125}$		+105°C ≤ T_J ≤ +125°C	-0.5	0	0.5	%	
$V_{CS_NOISE_000}$	Standard deviation over a population of 100 samples	CS_FIL = 000		9	16	μV_{RMS}	CSAP0 CSAN0
$V_{CS_NOISE_001}$		CS_FIL = 001		6.5	12	μV_{RMS}	
$V_{CS_NOISE_010}$		CS_FIL = 010		3.2	8	μV_{RMS}	
$V_{CS_NOISE_011}$		CS_FIL = 011		2.3	6.5	μV_{RMS}	
$V_{CS_NOISE_100}$		CS_FIL = 100		1.6	4.5	μV_{RMS}	
$V_{CS_NOISE_101}$		CS_FIL = 101		1.1	3	μV_{RMS}	
$V_{CS_NOISE_110}$		CS_FIL = 110		0.8	2.5	μV_{RMS}	
$V_{CS_NOISE_111}$		CS_FIL = 111		0.4	1.5	μV_{RMS}	
$CS_{LOW_RNG_ERR}$	CS total measurement error in low range including post-soldering and ageing effects	$\lvert V_{CSAP0} - V_{CSAN0} \rvert$ < 5mV, TJ ≤+105°C	-20.6		20.6	LSB	CSAP0 CSAN0

1. *Single-shot samples are characterized by a superimposed Gaussian noise, with zero-mean and VCS_NOISE standard deviation*

4.7.1.2 *Overcurrent detection (OVC)*

The IC can protect the battery pack from overcurrent events due to overload conditions, in both charge and discharge directions, by sensing the voltage across the external shunt resistor with the **current sense** ADC.

Overcurrent thresholds **$V_{OVC_CHG_TH}$** (charge) and **$V_{OVC_DCHG_TH}$** (discharge) can be programmed via SPI using the **OVC_CHG_TH** and **OVC_DCHG_TH** fields respectively.

This diagnostic can be enabled using the OVC_EN bit and it is available in both NORMAL and STANDBY states; if the CS detects an overcurrent condition in charge or discharge, the corresponding **OVC_CHG** and **OVC_DCHG** flags will be set. Propagation delay from diagnostic assertion to FAULT pin assertion is **$T_{OVC_REACT_NORMAL}$** in NORMAL and **$T_{OVC_REACT_STANDBY}$** in STANDBY.

To avoid false detections, overcurrent thresholds shall only be modified while OVC_EN = 0 and CS_EN = 0. This diagnostic is executed every time a new sample (requested by SOC in NORMAL MODE or by cross-check in STANDBY MODE) from CS ADC is available and covers the failures listed in the following table.

4.7.1.2.1 Diagnostics

Table 56. Overcurrent diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Overcurrent in charge	• If (V_{CSAP0} – V_{CSAN0}) < $V_{OVC_CHG_TH}$, the OVC_CHG fault is acknowledged.	• The OVC_CHG flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• If (V_{CSAP0} – V_{CSAN0}) > $V_{OVC_CHG_TH}$, the OVC_CHG flag can be cleared by MCU	• FAULT pin is released	• When CS_EN=0, the overcurrent diagnostic is masked, the OVC_CHG flag can always be cleared • When OVC_EN=0, the overcurrent diagnostic is masked, the OVC_CHG flag can always be cleared
Overcurrent in discharge	• If (V_{CSAP0} – V_{CSAN0}) > $V_{OVC_DCHG_TH}$, the OVC_DCHG fault is acknowledged.	• The OVC_DCHG flag is set • If in STANDBY, the IC moves to NORMAL and sends a FAULT signal • If in NORMAL, the FAULT line is asserted	• If (V_{CSAP0} – V_{CSAN0}) < $V_{OVC_DCHG_TH}$, the OVC_DCHG flag can be cleared by MCU	• FAULT pin is released	• When CS_EN=0, the overcurrent diagnostic is masked, the OVC_DCHG flag can always be cleared • When OVC_EN=0, the overcurrent diagnostic is masked, the OVC_DCHG flag can always be cleared

4.7.1.2.2 Electrical Parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range of Table 2; T_J according to the operating range of Table 5.

Table 57. Overcurrent electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{OVC_CHG_TH}$	Programmable overcurrent threshold in charge (16 bit); $V_{OVC_{CHG_{TH}}} = -8V_{CS_RES} * CODE$	OVC_CHG_TH	-180		0	mV	CSAP0 CSAN0
$V_{OVC_DCHG_TH}$	Programmable overcurrent threshold in discharge (16 bit); $V_{OVC_{DCHG_{TH}}} = 8V_{CS_RES} * CODE$	OVC_DCHG_TH	0		180	mV	CSAP0 CSAN0
$V_{OVC_TH_RES}$	Overcurrent thresholds resolution			2.746		µV	CSAP0 CSAN0
$T_{OVC_REACT_NORMAL}$	Overcurrent reaction time of FAULT pin	NORMAL MODE			1	µs	CSAP0 CSAN0 FAULT

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$T_{OVC_REACT_STANDBY_VIO_VSTBY}$	Overcurrent reaction time of FAULT pin	STANDBY MODE VIO connected to VSTBY, $T_{VSTBY_SOFT_START}$	1.15		1.43	ms	CSAP0 CSAN0 FAULT
$T_{OVC_REACT_STANDBY_VIO_VCORE}$		STANDBY MODE VIO connected to VCORE, $T_{VCORE_SOFT_START}$	1.9		2.6	ms	
$T_{OVC_REACT_STANDBY_VIO_VCC}$		STANDBY MODE VIO connected to VCC, $T_{VCC_SOFT_START}$	1.15		1.45	ms	

4.7.2 Coulomb Counting ADC (CC ADC)

For better monitoring of the state of battery (e.g. State of Charge (SoC)), the L9988 provides a Coulomb Counter block.

The Coulomb Counting operation requires the MCU to track the charge added/subtracted from the battery pack over time. The IC helps track the charge variation ΔQ in the battery pack by acquiring and accumulating the current.

The Coulomb Counting function exploits a dedicated ADC **CC** operating on the CSAP1 and CSAN1 pins. To enable it and the related accumulation function, the CC_EN bit must be set. The ADC will start acquiring data after the T_{CC_START} settling time.

Voltage samples measured on the 100µΩ RSHUNT are accumulated in the N_{ACC} (32-bit register, split in the **CC_MSB** and **CC_LSB** fields) after the T_{CC_SAMPLE}time, while the N_SAMPL_CNT (CC_SAMPL_CNT 24-bit register, split in **CC_SAMPL_CNT_MSB** and **CC_SAMPL_CNT_LSB**) counts the number of samples stored in the accumulator.

In NORMAL MODE, if the CC ADC is enabled, the Coulomb Counter is continuously running after the MCU start command by setting the bit **CC_START**, a new acquisition starts upon completion of the previous conversion and the T_{CC_SAMPLE} is aligned to the ADC filter time $T_{CC_FILTER_NORMAL}$ (defined by the internal HF oscillator), which is programmable using the **CC_FIL_NORMAL** 2-bit field. For the first current sample only, after the Coulomb Counter settling time $T_{CC_START_NORMAL}$, it is necessary the ADC filter settling time $T_{CC_FILTER_START_NORMAL}$. In this case, the MCU compensates externally the Coulomb Counter; in fact, the State of Charge is obtained considering the number of accumulated samples N_{SAMPLE_CNT} and the MCU internal timer (with the accuracy of MCU oscillator).

With a R_{SHUNT} equal to 100 µΩ, in NORMAL MODE the CC can accumulate an operative current included in the range of (-750A, 750A) and a full-scale current between (-900A, 900A).

To prevent temporal incoherence between samples accumulated in the Coulomb Counter registers, the $T_{CC_FILTER_NORMAL}$ setting is sampled upon CC_START setting. Changing $T_{CC_FILTER_NORMAL}$ on the fly is not allowed.

Figure 28. Coulomb Counter ADC block diagram

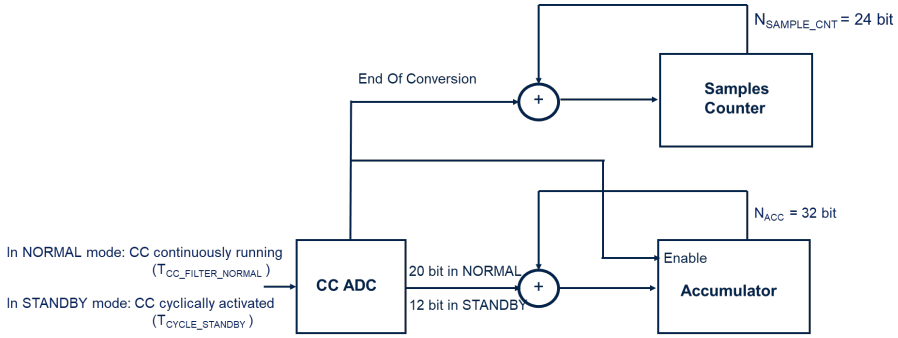
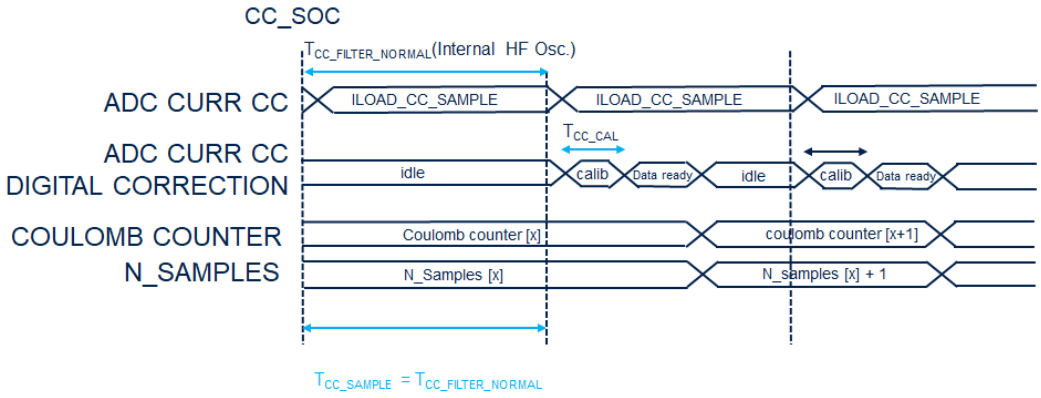


Figure 29. Timing diagram of Coulomb Counter accumulation in NORMAL MODE



The MCU shall periodically poll the Coulomb Counter to retrieve the charge information, but the accumulator size guarantees relaxed polling periods: if the Coulomb Counter reaches the maximum or minimum value, the flag **CC_ACC_SAT** is set to '1'. Meanwhile, the accumulation has stopped and **CC_MSB**, **CC_LSB** and **CC_SAMPL_CNT** are frozen.

The following procedure must be implemented to guarantee proper data synchronization between accumulator and sample counter:

Procedure 4 - Coulomb Counter readout

1. MCU reads **CC_MSB** field
   a. The **CC_MSB** is cleared upon read, the Coulomb Counter and the Sample Counter are reset and restart accumulation.
   b. A snapshot of **CC_LSB, CC_SAMPL_CNT_MSB, CC_SAMPL_CNT_LSB** is loaded into the corresponding registers
2. MCU reads the **CC_LSB**, **CC_SAMPL_CNT_MSB**, **CC_SAMPL_CNT_LSB** register (cleared upon read)

Periodical read of the Coulomb Counter can be useful for the following purposes:

- In algorithms relying directly on the CC for determining the SoC
- In algorithms exploiting Kalman filters for tracking the SoC. The periodical read of the CC helps evaluate the average current value, which can be used to adapt the process noise covariance matrix, thus improving the accuracy of the cell model estimators.

If the **Procedure 4** is executed using write commands instead of read commands, the accumulator registers will not be cleared, and it is possible to poll the Coulomb Counter without resetting it.

Disabling the Coulomb Counter by setting CC_EN = 0 does not reset the accumulator. The MCU shall follow the readout procedure described above to empty the Coulomb Counter.

The **CC_SAMPLE_SAT** flag reports the status of the samples counter. It saturates when the register holds $2^{NSAMPLE_CNT}$-1 and a new sample is generated. In this case, the **CC_SAMPLE_SAT** is set to '1'. Meanwhile, the accumulation has stopped and **CC_MSB**, **CC_LSB** and **CC_SAMPL_CNT** are frozen.

In STANDBY MODE, if the CC ADC is enabled, the Coulomb Counter is reset and then cyclically activated for a duration $\mathbf{T_{CC_ON}}$(defined in Section 4.2.1) in the time period $\mathbf{T_{CYCLE_STANDBY}}$. MCU can select this cycle time $\mathbf{T_{CYCLE_STANDBY}}$(by internal RTC) much longer (e.g. 1s) than $\mathbf{T_{CC_FILTER_STANDBY}}$ (defined by the internal HF oscillator and programmed using the **CC_FIL_STANDBY** 2-bit field) to reduce power consumption. $\mathbf{T_{CC_FILTER_STANDBY}}$ replaces $\mathbf{T_{CC_FILTER_NORMAL}}$ before the first trigger of the $\mathbf{T_{CYCLE_STANDBY}}$.

Furthermore, the MCU should select a proper threshold (Ext. Gain) for charge/discharge detection wake up (CC_WUP, refer to Section 4.7.2.2) considering cycle time.

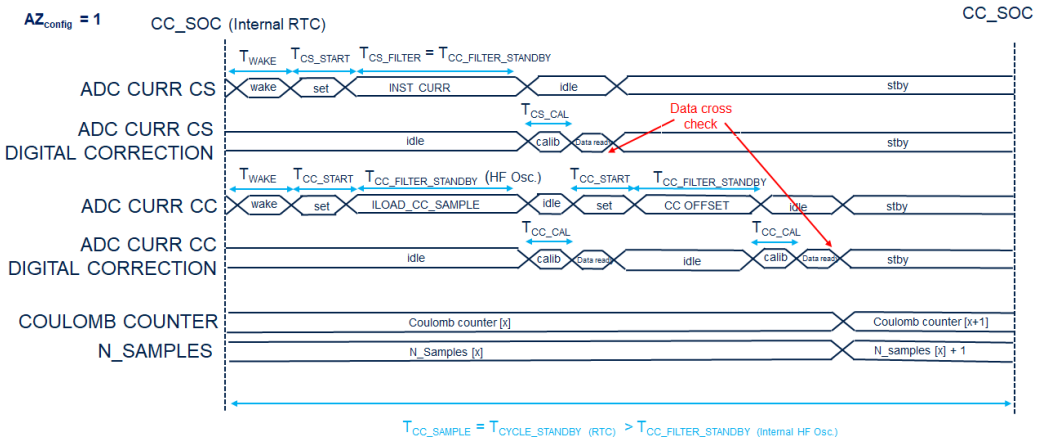
With a R_{SHUNT} equal to 100µΩ, in STANDBY MODE the CC can accumulate an operative current included in the range of (-1.5A, 1.5A) and a full-scale current between (-1.75A, 1.75A).

Note that the $\mathbf{T_{CYCLE_STANDBY}}$ is the same for voltage/current activation in STANDBY MODE.

With reference to Figure 31, and considering the Coulomb counting auto-zero feature described in Section 4.7.2.4,

T_{CC_ON}= (1 + AZ_{config}) * (T_{CC_START}+ $T_{CC_FILTER_STANDBY}$ + T_{CC_CAL}) = 2 * (T_{CC_START}+ $T_{CC_FILTER_STANDBY}$ + T_{CC_CAL})

Figure 30. Timing diagram of current sense measurement and Coulomb Counter accumulation in STANDBY MODE



4.7.2.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Accuracy data refers to a characterization method using single instantaneous samples. They shall not be derived from processing the accumulation results.

Table 58. Coulomb Counter electrical parameters in NORMAL MODE

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{CC_DIFF_FS_NORMAL}$	CC ADC full scale differential input voltage, CSAP1 - CSAN1	Design info	-90		90	mV	CSAP1 CSAN1
$V_{CC_DIFF_OP_NORMAL}$	CC ADC operating differential input voltage, CSAP1 - CSAN1	Design info	-75		75	mV	CSAP1 CSAN1
$V_{CC_ABS_OR_NORMAL}$	Maximum differential voltage between CSAP1 or CSAN1 pin with respect to GND to have CC parameter guaranteed	Design info	-200		200	mV	CSAP1 CSAN1
$N_{BIT_CC_NORMAL}$	CC ADC bit number: encoding is in 2's complement	Design info		20		bit	CSAP1 CSAN1
$V_{CC_RES_NORMAL}$	CC ADC resolution	LSB calculated on DIFF_FS_NORMAL		$0.09/2^{20-1}$		V	CSAP1 CSAN1
N_{ACC}	Coulomb Counter accumulator size	Design info		32		bit	CSAP1 CSAN1
$N_{_SAMPLE_CNT}$	Coulomb Counter sample counter size	Design info		24		bit	CSAP1 CSAN1
$T_{CC_START_NORMAL}$	Coulomb Counter settling time (1)	Guaranteed by SCAN		60		µs	CSAP1 CSAN1
$T_{CC_FILTER_START_NORMAL}$	ADC filter settling time	Guaranteed by SCAN		520		µs	CSAP1 CSAN1
$T_{CC_FILTER_NORMAL_00}$	Programmable ADC filter time for Coulomb Counter accumulator (2 bit) (2)	CC_FIL_NORMAL = 00		1.04		ms	CSAP1 CSAN1
$T_{CC_FILTER_NORMAL_01}$		CC_FIL_NORMAL = 01		2.08		ms	CSAP1 CSAN1

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$T_{CC_FILTER_NORMAL_10}$	Programmable ADC filter time for Coulomb Counter accumulator (2 bit) (2)	CC_FIL_NORMAL = 10		4.16		ms	CSAP1 CSAN1
$T_{CC_FILTER_NORMAL_11}$		CC_FIL_NORMAL = 11		8.32		ms	CSAP1 CSAN1
$T_{CC_CAL_NORMAL}$	CC ADC post-calibration time (1)	Guaranteed by SCAN		27	35	µs	CSAP1 CSAN1
$CC_{OFFSET_ERR_NORMAL}$	CC offset error, including post-soldering and ageing effects.(3)	CSAP1 and CSAN1 inputs shorted on PCB, with 0V common mode, Guaranteed by test bench characterization	-9		9	LSB	CSAP1 CSAN1
$CC_{GAIN_ERR_NORMAL_105}$	CC gain error, including non-linearities, including post-soldering and ageing effects.(3)	-40°C ≤ T_J ≤ +105°C	-0.1		0.1	%	CSAP1 CSAN1
$CC_{GAIN_ERR_NORMAL_125}$		+105°C ≤ T_J ≤ +125°C	-0.5		0.5	%	CSAP1 CSAN1
$V_{CC_NOISE_NORMAL_00}$	Standard deviation over a population of 100 samples. Design information only: SoC is assumed to be evaluated over a high number of samples reducing noise impact of a factor $\sqrt{N_{SAMPLE_CNT}}$	CC_FIL_NORMAL = 00		3.2	4	μV_{RMS}	CSAP1 CSAN1
$V_{CC_NOISE_NORMAL_01}$		CC_FIL_NORMAL = 01		2.3	3	μV_{RMS}	CSAP1 CSAN1
$V_{CC_NOISE_NORMAL_10}$		CC_FIL_NORMAL = 10		1.6	2	μV_{RMS}	CSAP1 CSAN1
$V_{CC_NOISE_NORMAL_11}$		CC_FIL_NORMAL = 11		1.1	1.5	μV_{RMS}	CSAP1 CSAN1
$CC_{LOW_RNG_ERR_NORM}$	CC total measurement error in low range including post-soldering end ageing effects	$\lvert V_{CSAP1} - V_{CSAN1} \rvert$ < 5mV, TJ ≤+105°C, NORMAL state	-38.1		38.1	LSB	CSAP1 CSAN1

1. *TCC_START_NORMAL = TCC_START_STANDBY and TCC_CAL_NORMAL = TCC_CAL_STANDBY as they share the same device blocks.*
2. *The possible values of TCC_FILTER are the same in NORMAL and STANDBY state since the same system blocks are shared, but it is possible to configure them independently of each other in NORMAL and in STANDBY state with the dedicated configuration bits, CC_FIL_NORMAL and CC_FIL_STANDBY respectively.*
3. *Single shot samples are characterized by a superimposed Gaussian noise, with zero-mean and VCC_NOISE_NORMAL standard deviation.*

Table 59. Coulomb Counter electrical parameters in STANDBY MODE

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{CC_DIFF_FS_STANDBY}$	CC ADC full scale differential input voltage, CSAP1 - CSAN1	Design info	$-V_{CC_DIFF_FS_NORMAL}/512$		$V_{CC_DIFF_FS_NORMAL}/512$	V	CSAP1 CSAN1
$V_{CC_DIFF_OP_STANDBY}$	CC ADC operating differential input voltage, CSAP1 - CSAN1	Design info	-150		150	µV	CSAP1 CSAN1
$V_{CC_ABS_OR_STANDBY}$	Maximum differential voltage between CSAP1 or CSAN1pin with respect to GND to have CC parameter guaranteed	Design info	-200		200	mV	CSAP1 CSAN1
$N_{BIT_CC_STANDBY}$	CC ADC bit number: encoding is in 2's complement	Design info		12		bit	CSAP1 CSAN1
$V_{CC_RES_STANDBY}$	CC ADC resolution	LSB calculated on DIFF_FS_NORMAL		$0.09/2^{20}$		V	CSAP1 CSAN1

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
N_{ACC}	Coulomb Counter accumulator size	Design info		32		bit	CSAP1 CSAN1
$N_{_SAMPLE_CNT}$	Coulomb Counter sample counter size	Design Info		24		bit	CSAP1 CSAN1
$T_{CC_START_STANDBY}$	Coulomb Counter settling time (1)	Guaranteed by SCAN		60		µs	CSAP1 CSAN1
$T_{CC_FILTER_STANDBY_00}$	Programmable ADC filter time for Coulomb Counter accumulator (2 bit) (2)	CC_FIL_ STANDBY = 00		1.04		ms	CSAP1 CSAN1
$T_{CC_FILTER_STANDBY_01}$		CC_FIL_ STANDBY = 01		2.08		ms	CSAP1 CSAN1
$T_{CC_FILTER_STANDBY_10}$		CC_FIL_ STANDBY = 10		4.16		ms	CSAP1 CSAN1
$T_{CC_FILTER_STANDBY_11}$		CC_FIL_ STANDBY = 11		8.32		ms	CSAP1 CSAN1
$T_{CC_CAL_STANDBY}$	CC ADC post-calibration time (1)	Guaranteed by SCAN		27	35	µs	CSAP1 CSAN1
$CC_{OFFSET_ERR_STANDBY}$	CC offset error, including post-soldering and ageing effects.(3)	CSAP1 and CSAN1 inputs shorted on PCB, with 0V common mode, Guaranteed by test bench characterization	-4		4	LSB	CSAP1 CSAN1
$CC_{GAIN_ERR_STANDBY_125}$	CC gain error, including non-linearities, including post-soldering and ageing effects(3)	-40°C ≤ T_J ≤ +125°C	-0.5		0.5	%	CSAP1 CSAN1
$V_{CC_NOISE_STANDBY_00}$	Standard deviation over a population of 100 samples. Design information only: SoC is assumed to be evaluated over a high number of samples reducing noise impact of a factor $\sqrt{N_{SAMPLE_CNT}}$	CC_FIL_ STANDBY = 00			2	μV_{RMS}	CSAP1 CSAN1
$V_{CC_NOISE_STANDBY_01}$		CC_FIL_ STANDBY = 01			1.5	μV_{RMS}	CSAP1 CSAN1
$V_{CC_NOISE_STANDBY_10}$		CC_FIL_ STANDBY = 10			1	μV_{RMS}	CSAP1 CSAN1
$V_{CC_NOISE_STANDBY_11}$		CC_FIL_ STANDBY = 11			0.5	μV_{RMS}	CSAP1 CSAN1
$CC_{LOW_RNG_ERR_STBY}$	CC total measurement error in low range including post-soldering end ageing effects	$\lvert V_{CSAP1} - V_{CSAN1} \rvert$ < 17.2µV, TJ ≤+105°C, STANBY state	-5		5	LSB	CSAP1 CSAN1

1. *TCC_START_NORMAL = TCC_START_STANDBY and TCC_CAL_NORMAL = TCC_CAL_STANDBY as they share the same device blocks.*
2. *The possible values of TCC_FILTER are the same in NORMAL and STANDBY state since the same system blocks are shared, but it is possible to configure them independently of each other in NORMAL and in STANDBY state with the dedicated configuration bits, CC_FIL_NORMAL and CC_FIL_STANDBY respectively.*
3. *Single shot samples are characterized by a superimposed Gaussian noise, with zero-mean and VCC_NOISE_STANDBY standard deviation.*

4.7.2.2 *CC state transition behavior - charge/discharge detection (CC_WUP)*

The L9988 can monitor pack current while in STANDBY state, in order to detect leakage conditions in both charge and discharge directions using the **Coulomb Counter** ADC. This diagnostic is not available in other FSM states.

This feature can be activated by having the Coulomb Counter enabled (CC_EN = 1) and programming CC_WUP_EN = 1 (enabling the wakeup source).

When the IC moves to STANDBY from NORMAL MODE

- The Coulomb Counting accumulator (**CC_MSB** and **CC_LSB**) and sample counter (**CC_SAMPLE_CNT**) are reset and disabled in order to start from a zero-charge initial condition.

While in STANDBY MODE:

- The Coulomb Counter accumulator (**CC_MSB** and **CC_LSB**) and sample counter (**CC_SAMPLE_CNT**) are kept ON
- The CC ADC cyclically (T_{CC_ON} in the time period $T_{CYCLE_STANDBY}$) monitors the voltage across the external shunt resistor (after the settling time T_{CC_START}), converting the CSAP1/CSAN1 pair with the programmed $T_{CC_FILTER_STANDBY}$filter time
- After a T_{CC_SAMPLE} = $T_{CYCLE_STANDBY}$, current samples are accumulated in the **CC_MSB** and **CC_LSB** registers and the counter **CC_SAMPLE_CNT** is incremented. The accumulation result is compared to the CC_WUP_THRESHOLD: if higher, a leakage is detected. The diagnostic covers both charge/discharge leakage as the check is performed on the absolute value of the signal. Leakage detection leads to self-wakeup in NORMAL state for FAULT pin assertion.

When the L9988 moves from STANDBY to NORMAL state:

- The CC ADC is disabled until the device completes the transition to NORMAL state
- At this point, the full-scale current range is changed, and the CC ADC stops working, waiting for an SPI command by the MCU using the **CC_START** bit . The accumulator maintains the stored data until the MCU clear request.
- The transition to NORMAL is over. The leakage diagnostic is disabled.

User SW can set the 8-bit **CC_WUP_TH** field, taking into account the $T_{CYCLE_STANDBY}$, to configure the threshold applied to the Coulomb Counter accumulator (**CC_MSB** and **CC_LSB**) for waking the system up.

4.7.2.2.1 Diagnostics

Table 60. Charge/discharge wakeup monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Charge/ discharge detection CC WUP	• If Coulomb Counter accumulator (CC_MSB and CC_LSB) reaches, or it is higher than CC_WUP_THRESHOLD, an excessive charge/discharge condition is detected • If CC_SAMPLE_CNT saturated • If CC_ACC_SAT is set to ‘1’	• The CC_WUP flag is set • The IC moves to NORMAL state • FAULT pin is asserted	• Once in NORMAL, the CC_WUP flag can be cleared by MCU	• FAULT pin is released	• When CC_EN=0, the Charge/Discharge Wakeup monitor diagnostic is masked, the CC_WUP flag can always be cleared • When CC_WUP_EN=0, the Charge/Discharge Wakeup monitor diagnostics is masked, the CC_WUP flag can always be cleared

4.7.2.2.2 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 61. Charge/discharge detection electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
CC_WUP_THRESHOLD	Coulomb Counter wakeup threshold CC_WUP_TH (8 bit) $CC_WUP_THRESHOLD = CODE * 2^{23}$	Guaranteed by SCAN	0		$255*2^{23}$	LSB(1)	CSAP1 CSAN1

1. *Refer to VCC_RES_ STANDBY.*

4.7.2.3 *Coulomb Counting redundancy check*

The Coulomb Counter accumulator (CC_MSB and CC_LSB) is redundant for safety reasons. So the current samples converted by the unique CC ADC connected to the CSAP1 and CSAN1 pins are accumulated in two accumulators monitoring each other. In case they return different values, the flag CC_RED_FAIL is set.

In NORMAL MODE, the CC_RED_FAIL flag will be set, and the FAULT pin will be asserted until the MCU clears the flag.

In STANDBY MODE, the CC_RED_FAIL will wake up the device, going to NORMAL MODE and triggering the FAULT pin until MCU readout.

This feature can be activated by having the Coulomb Counter enabled (CC_EN = 1) and programming CC_RED_FAIL_EN = 1 (enabling the wakeup source).

The MCU can send the CC_RED_FAIL_INJ command in NORMAL MODE to perform a fault injection in the redundant accumulator value. In this case, the CC_RED_FAIL is expected to be set by internal monitoring because of the difference between the two accumulators.

4.7.2.3.1 Diagnostics

Table 62. CC redundancy check diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
CC redundancy fail	• If the two Coulomb Counter accumulators return different values, the CC_RED_FAIL fault is acknowledged	• The CC_RED_FAIL flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• Once in NORMAL, the CC_RED_FAIL flag can be cleared by MCU	• FAULT pin is released	• When CC_EN=0, the CC redundancy check diagnostics is masked, the CC_RED_FAIL flag can always be cleared • When CC_RED_FAIL_EN=0, the CC redundancy check diagnostics is masked, the CC_RED_FAIL flag can always be cleared

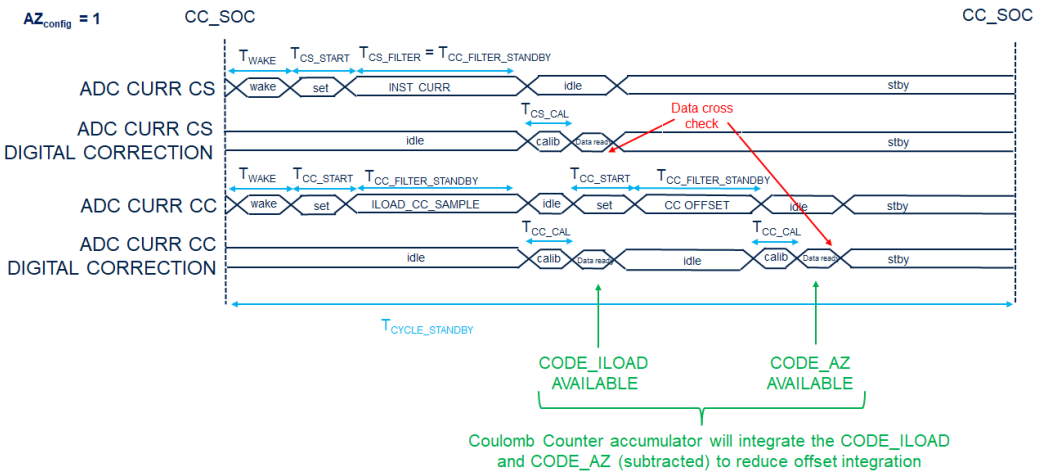
4.7.2.4 *Coulomb Counting Auto-Zero (AZ_{config})*

The IC features an auto-zero configuration to compensate for the offset on the Coulomb Counter input pins CSAN1 and CSAP1 only in STANDBY MODE and to obtain the electrical characteristics listed in Section 4.7.2.1.

With reference to the following figures, during $\mathbf{T_{CYCLE_STANDBY}}$ the Coulomb Counter is cyclically activated for a duration of $\mathbf{T_{CC_ON} = (1 + AZ_{config}) * (T_{CC_START} + T_{CC_FILTER_STANDBY} + T_{CC_CAL})}$.

Since the CS ADC and the CC ADC must be synchronous to automatically perform the cross-check, $\mathbf{T_{CS_FILTER}}$ must be aligned with the filter time $\mathbf{T_{CC_FILTER_STANDBY}}$, then $\mathbf{T_{CS_ON} = T_{CC_ON} - (AZ_{config} * (T_{CC_START} + T_{CC_FILTER_STANDBY} + T_{CC_CAL}))}$, considering also that $T_{CS_START} = T_{CC_START}$ (with $T_{CC_START_NORMAL} = T_{CC_START_STANDBY} = T_{CC_START}$ defined in Section 4.7.2.1) and $T_{CS_CAL} = T_{CC_CAL}$ (with $T_{CC_CAL_NORMAL} = T_{CC_CAL_STANDBY} = T_{CC_CAL}$ defined in Section 4.7.2.1).

Figure 31. **Timing diagram of current conversion routine in STANDBY MODE**



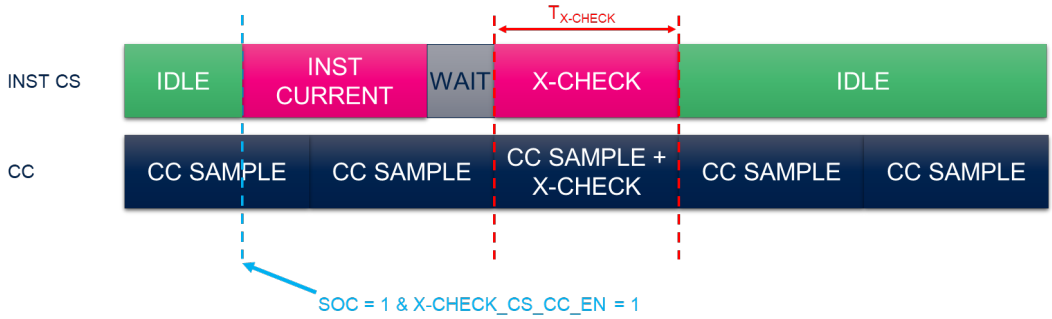
4.7.3 CS-CC cross-check (X-CHECK)

When both Instantaneous Current Measurement ADC (**CS** ADC) and Coulomb Counting ADC (**CC** ADC) are enabled (CS_EN = 1 and CC_EN = 1), a real-time cross-check between instantaneous samples can be performed, both in NORMAL and STANDBY MODE.

In NORMAL MODE, if the Coulomb Counter is continuously running after setting the CC_START bit, samples are cross-checked whenever the Start of Conversion (SOC) command is sent by the MCU via the SPI or by the internal timer (every T_{CYCLE_NORMAL}seconds), with the enable bit **XCHECK_CS_CC_EN = 1**. If the Coulomb Counter is not running, the cross-check is not executed.

Performing the x-check does not alter the instantaneous current measurement thread, nor the synchronicity with the cell voltage measurement. In fact, as shown in the following figure, the instantaneous current sample is acquired immediately, while the x-check is delayed, aligning the instantaneous CS to the Coulomb counter running in the background (CS and CC are asynchronous). On the other hand, T_{CS_FILTER} is automatically aligned with the filter time $T_{CC_FILTER_NORMAL}$when the x-check is performed

Figure 32. **CS & CC X-Check in NORMAL MODE**



The WAIT time duration can reach a maximum value of $T_{WAIT} = T_{CC_START_NORMAL} + T_{CC_FILTER_START_NORMAL} + T_{CC_FILTER_NORMAL}$.

The x-check conversion lasts for $T_{X\text{-}CHECK} = T_{CS_FILTER} = T_{CC_FILTER_NORMAL}$ (the result is available after the additional time required for the calibration $T_{CS_CAL} = T_{CC_CAL}$, with $T_{CC_CAL_NORMAL} = T_{CC_CAL_STANDBY} = T_{CC_CAL}$ defined in Section 4.7.2.1), and follows this strategy:

- If the absolute values of both samples are greater than 9350 LSB of CS ADC, the following condition will be checked:
  Equation 2 – Cross-check condition (high range)

$$\begin{cases} if \quad \left|CUR_{INST_{CS}}\right| \geq \left|CUR_{INST_{CC}}\right| = = > \left|CUR_{INST_{CS}} - CUR_{INST_{CC}}\right| \leq \frac{\left|CUR_{INST_{CS}}\right|}{X_{CHECK_{HIGH_{TH_NORMAL}}}} \\ if \quad \left|CUR_{INST_{CS}}\right| < \left|CUR_{INST_{CC}}\right| = = > \left|CUR_{INST_{CS}} - CUR_{INST_{CC}}\right| \leq \frac{\left|CUR_{INST_{CC}}\right|}{X_{CHECK_{HIGH_{TH_NORMAL}}}} \end{cases} \quad (2)$$

- If the absolute value of at least one sample is less than or equal to 9350 LSB of CS ADC, the following condition will be checked:
  Equation 3 – Cross-check condition (low range)

$$\left|CUR_{INST_{CS}} - CUR_{INST_{CC}}\right| \leq X_{CHECK_{LOW_{TH,NORMAL}}} \quad (3)$$

- The following out-of-range check is also executed:
  Equation 4 – Cross-check condition out of CC operative range (values are expressed in LSB of CS ADC)

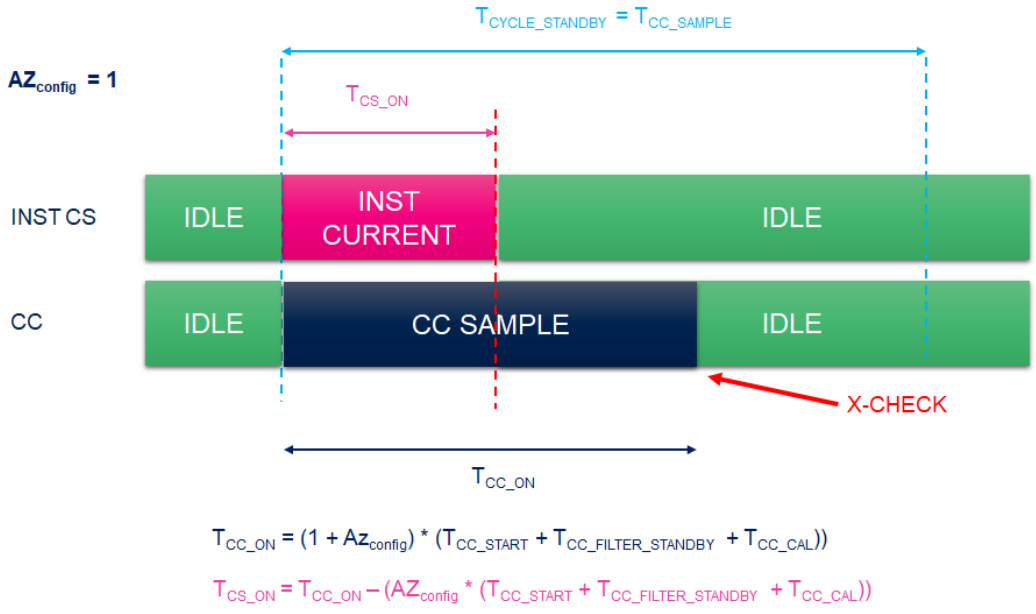
$$\begin{cases} \left|CUR_{INST_{CS}}\right| < 218543 - X_{CHECK_{OUT_{TH_NORMAL}}} \\ \left|CUR_{INST_{CC}}\right| < 218543 - X_{CHECK_{OUT_{TH_NORMAL}}} \end{cases} \quad (4)$$

To confirm the diagnostic execution, the **XCHECK_CS_CC_END** flag (cleared upon read) will be set when the check is over. In case one of the conditions above is not verified, the **XCHECK_CS_CC_FAIL** flag will be set (cleared upon read) and the FAULT pin is asserted. The cross-check circuit is duplicated to control its correct functionality. In case functional and redundant circuits give different results, **XCHECK_CS_CC_END_MISMATCH** and/or **XCHECK_CS_CC_FAIL_MISMATCH** (both cleared on read) are asserted.

During the cross-check execution, CC_EN and CS_EN settings must not be modified.

In STANDBY MODE, if **XCHECK_CS_CC_EN = 1**, the x-check is automatically performed upon each transition to $T_{CYCLE_STANDBY}$. In fact, as shown in the following figure, CS and CC are synchronous.

Figure 33. CS & CC X-Check in STANDBY MODE



In STANDBY MODE, the x-check conversion follows this strategy:

- If the absolute values of both samples are greater than 290 LSB of CS ADC and (X_CHECK_HIGH_TH_STBY = 10 or X_CHECK_HIGH_TH_STBY = 11) , the following condition will be checked:

Equation 5 – Cross-check condition (high range)

$$\begin{cases} if \quad \left|CUR_{INST_{CS}}\right| \geq \left|CUR_{INST_{CC}}\right| \; = \; = \; > \left|CUR_{INST_{CS}} - CUR_{INST_{CC}}\right| \leq \dfrac{\left|CUR_{INST_{CS}}\right|}{X_{CHECK_{HIGH_{TH_STBY}}}} \\ if \quad \left|CUR_{INST_{CS}}\right| < \left|CUR_{INST_{CC}}\right| \; = \; = \; > \left|CUR_{INST_{CS}} - CUR_{INST_{CC}}\right| \leq \dfrac{\left|CUR_{INST_{CC}}\right|}{X_{CHECK_{HIGH_{TH_STBY}}}} \end{cases} \quad (5)$$

- If the absolute value of at least one sample is less than or equal to 290 LSB of CS ADC or X_CHECK_HIGH_TH_STBY = 00 or X_CHECK_HIGH_TH_STBY = 01, the following condition will be checked:

Equation 6 – Cross-check condition (low range)

$$\left|CUR_{INST_{CS}} - CUR_{INST_{CC}}\right| \leq X_{CHECK_{LOW_{TH_STBY}}} \quad (6)$$

- The following out of range check is also executed:

Equation 7 – Cross-check condition out of CC operative range (values are expressed in LSB of CS ADC)

$$\begin{cases} \left|CUR_{INST_{CS}}\right| < 437 - X_{CHECK_{OUT_{TH_STBY}}} \\ \left|CUR_{INST_{CC}}\right| < 437 - X_{CHECK_{OUT_{TH_STBY}}} \end{cases} \quad (7)$$

To confirm the diagnostic execution, the **XCHECK_CS_CC_END** flag (cleared upon read) will be set when the check is over. In case one of the conditions above is not verified, the **XCHECK_CS_CC_FAIL** flag will be set (cleared upon read) and the IC moves to NORMAL MODE and the FAULT pin is asserted.

The behavior described above makes the out-of-range check usable as overcurrent detection criteria during STBY mode: in that case, the MCU is in charge of decoding the **XCHECK_CS_CC_FAIL** flag as an overcurrent condition.

4.7.3.1 *Diagnostics*

Table 63. Cross-check diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
X-CHECK CS-CC Fail	• If in NORMAL and Equations 2,3,4 are not verified, the XCHECK_CS_CC_FAIL fault is acknowledged • If in STANDBY and Equations 5,6,7 are not verified, the XCHECK_CS_CC_FAIL fault is acknowledged	• The XCHECK_CS_CC_FAIL flag is set • If in STANDBY, the IC moves to NORMAL and the FAULT pin is asserted • If in NORMAL, the FAULT pin is asserted	• Once in NORMAL, the XCHECK_CS_CC_FAIL flag can be cleared by MCU	• FAULT pin is released	• When XCHECK_CS_CC_EN = 0 the cross-check diagnostics is masked, the XCHECK_CS_CC_FAIL flag can always be cleared

4.7.3.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 64. X-check electrical parameters (values are expressed in LSB of CS ADC)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$X_{CHECK_LOW_TH_NORMAL_00}$	Programmable x-check threshold for low range (2 bit) in NORMAL MODE	X_CHECK_LOW_TH_NORMAL = 00 (default)		73		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_LOW_TH_NORMAL_01}$		X_CHECK_LOW_TH_NORMAL = 01		87		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_LOW_TH_NORMAL_10}$		X_CHECK_LOW_TH_NORMAL = 10		117		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_LOW_TH_NORMAL_11}$		X_CHECK_LOW_TH_NORMAL = 11		175		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_HIGH_TH_NORMAL_00}$	Programmable x-check threshold for high range (2 bit) in NORMAL MODE	X_CHECK_HIGH_TH_NORMAL = 00		128			CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_HIGH_TH_NORMAL_01}$		X_CHECK_HIGH_TH_NORMAL = 01 (default)		64			CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_HIGH_TH_NORMAL_10}$		X_CHECK_HIGH_TH_NORMAL = 10		32			CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_HIGH_TH_NORMAL_11}$		X_CHECK_HIGH_TH_NORMAL = 11		16			CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_OUT_TH_NORMAL_00}$	Programmable x-check threshold for out of CC operative scale range (2 bit) in NORMAL MODE	X_CHECK_OUT_TH_NORMAL = 00		0		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_OUT_TH_NORMAL_01}$		X_CHECK_OUT_TH_NORMAL = 01 (default)		14564		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_OUT_TH_NORMAL_10}$		X_CHECK_OUT_TH_NORMAL = 10		29127		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_OUT_TH_NORMAL_11}$		X_CHECK_OUT_TH_NORMAL = 11		72817		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_LOW_TH_STBY_00}$	Programmable x-check threshold for low range (2 bit) in STANDBY MODE	X_CHECK_LOW_TH_STBY = 00 (default)		58		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_LOW_TH_STBY_01}$		X_CHECK_LOW_TH_STBY = 01		73		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_LOW_TH_STBY_10}$		X_CHECK_LOW_TH_STBY = 10		87		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_LOW_TH_STBY_11}$		X_CHECK_LOW_TH_STBY = 11		117		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_HIGH_TH_STBY_00}$	Programmable x-check threshold for high range (2 bit) in STANDBY MODE	X_CHECK_HIGH_TH_STBY = 00		Follow Eq. (6)**– Cross-check condition (low range)**			CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_HIGH_TH_STBY_01}$		X_CHECK_HIGH_TH_STBY = 01 (default)		Follow Eq. (6) **– Cross-check condition (low range)**			CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_HIGH_TH_STBY_10}$		X_CHECK_HIGH_TH_STBY = 10		4			CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_HIGH_TH_STBY_11}$		X_CHECK_HIGH_TH_STBY = 11		2			CSAP0 CSAN0 CSAP1 CSAN1

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$X_{CHECK_OUT_TH_STBY_00}$	Programmable x-check threshold for out of CC operative scale range (2 bit) in STANDBY MODE	X_CHECK_OUT_TH_STBY = 00		0		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_OUT_TH_STBY_01}$		X_CHECK_OUT_TH_STBY = 01 (default)		29		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_OUT_TH_STBY_10}$		X_CHECK_OUT_TH_STANDBY = 10		73		LSB	CSAP0 CSAN0 CSAP1 CSAN1
$X_{CHECK_OUT_TH_STBY_11}$		X_CHECK_OUT_TH_STBY = 11		146		LSB	CSAP0 CSAN0 CSAP1 CSAN1

4.8 Short-Circuit detection (SC)

4.8.1 Short-Circuit ADC (SC ADC)

The L9988 protects the battery pack from dangerous short-circuit conditions by sensing the voltage across the external shunt resistor with a dedicated 10-bit ADC **SC,** which is continuously running and operates on the CSAP0 and CSAN0 pins.

Short-circuit thresholds $\mathbf{V_{SC_CHG_TH}}$ (charge) and $\mathbf{V_{SC_DCHG_TH}}$ (discharge) can be programmed via SPI using the 9-bit **SC_CHG_TH** and **SC_DCHG_TH** fields respectively.

The SC detection can be enabled by setting the SC_EN bit and it is continuously available in both NORMAL and STANDBY states. If the SC ADC detects a short-circuit in charge or discharge, the corresponding **SC_CHG** and **SC_DCHG** flags will be set; the propagation delay from diagnostic assertion to LATCH pin assertion is $\mathbf{T_{SC_LATCH_REACT_NORMAL}}$ in NORMAL and $\mathbf{T_{SC_LATCH_REACT_STANDBY}}$ in STANDBY.

With a R_{SHUNT} equal to 100 µΩ, the SC ADC can measure a full-scale current between (-3600 A, 3600 A).

To avoid false detections, short-circuit thresholds shall only be modified while SC_EN = 0. During NVM download, SC ADC is switched OFF even if SC_EN = 1. The diagnostic is executed every time a new sample from SC ADC is available and covers the failures listed in the following table.

4.8.2 Diagnostics

Table 65. Short-circuit detection

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Short Circuit in Charge	• If ($V_{CSAP0} - V_{CSAN0}$) < $V_{SC_CHG_TH}$, the SC_CHG fault is acknowledged.	• The SC_CHG flag is set • If in STANDBY, the IC moves to NORMAL and the LATCH pin is asserted • If in NORMAL, the LATCH pin is asserted • Both groups of CB MOSFETs are turned OFF	• If ($V_{CSAP0} - V_{CSAN0}$) > $V_{SC_CHG_TH}$, the SC_CHG flag can be cleared by MCU	• LATCH pin is released • One or both groups of CB back-to-back MOSFETs are turned ON (according to Table 70 (Pre-Drivers driving commands), refer to Section 4.10.2 for details)	• When SC_EN=0, the short-circuit detection is masked, the SC_CHG flag can always be cleared • SC_LATCH_MSK=1 masks reaction on the LATCH pin • SC_HS_MASK=1 masks reaction on the Pre-Drivers
Short Circuit in Discharge	• If ($V_{CSAP0} - V_{CSAN0}$) > $V_{SC_DCHG_TH}$, the SC_DCHG fault is acknowledged.	• The SC_DCHG flag is set • If in STANDBY, the IC moves to NORMAL and the LATCH pin is asserted • If in NORMAL, the LATCH pin is asserted • Both groups of CB MOSFETs are turned OFF	• If ($V_{CSAP0} - V_{CSAN0}$) < $V_{SC_DCHG_TH}$, the SC_DCHG flag can be cleared by MCU	• LATCH pin is released • One or both groups of CB back-to-back MOSFETs are turned ON (according to Table 70 (Pre-Drivers driving commands), refer to Section 4.10.2 for details)	• When SC_EN=0, the short-circuit detection is masked, the SC_DCHG flag can always be cleared • SC_LATCH_MSK=1 masks reaction on the LATCH pin • SC_HS_MASK=1 masks reaction on the Pre-Drivers

4.8.3 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 66. Short-circuit diagnostic electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{SC_DIFF_FS}$	SC ADC full scale differential input voltage, CSAP0 – CSAN0	Design info	-360		360	mV	CSAP0 CSAN0
$V_{SC_DIFF_OP}$	SC ADC operating differential input voltage, CSAP0 – CSAN0	Design info	-300		300	mV	CSAP0 CSAN0
$V_{SC_ABS_OR}$	Maximum differential voltage between CSAP0 or CSAN0 pin with respect to GND to have CS parameters guaranteed	Design info	-500		500	mV	CSAP0 CSAN0
N_{BIT_SC}	SC ADC bit number: encoding is in 2's complement	Design info		10		bit	CSAP0 CSAN0
V_{SC_RES}	SC ADC resolution	LSB calculated on DIFF_FS		$0.36/2^{10-1}$		V	CSAP0 CSAN0
T_{SC_CAL}	SC ADC post-calibration time	Guaranteed by SCAN		27		µs	CSAP0 CSAN0
SC_{OFFSET_ERR}	SC ADC offset error, including post-soldering and ageing effects(1)	CSAP0 and CSAN0 inputs shorted to GND on PCB. Guaranteed by test bench characterization	-1	0	1	LSB	CSAP0 CSAN0
SC_{GAIN_ERR}	SC ADC gain error, including non-linearities, including post-soldering and ageing effects(1)	-40°C ≤ T_J ≤ +125°C	-1	0	1	%	CSAP0 CSAN0
$V_{SC_CHG_TH}$	Programmable short-circuit threshold in charge (9 bit); $V_{SC_{CHG_{TH}}} = -V_{SC_RES} * CODE$	SC_CHG_TH	-359.29		0	mV	CSAP0 CSAN0
$V_{SC_DCHG_TH}$	Programmable short-circuit threshold in discharge (9 bit); $V_{SC_{DCHG_{TH}}} = -V_{SC_RES} * CODE$	SC_DCHG_TH	0		359.29	mV	CSAP0 CSAN0
$T_{SC_ADC_SWITCH_ON}$	SC ADC first activation time				300	µs	CSAP0 CSAN0
$T_{SC_ADC_REACT}$	SC ADC reaction time to SC_CHG and SC_DCHG flags setting				850	µs	CSAP0 CSAN0
$T_{SC_LATCH_REACT_NORMAL}$	Short-circuit reaction time of LATCH pin	NORMAL MODE			1	µs	CSAP0 CSAN0 LATCH
$T_{SC_LATCH_REACT_STANDBY_VIO_VSTBY}$		STANDBY MODE VIO connected to VSTBY, $T_{VSTBY_SOFT_START}$	1.15		1.43	ms	CSAP0 CSAN0 LATCH
$T_{SC_LATCH_REACT_STANDBY_VIO_VCORE}$		STANDBY MODE	1.9		2.6	ms	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
		VIO connected to VCORE, $T_{VCORE_SOFT_START}$					CSAP0
$T_{SC_LATCH_REACT_STANDBY_VIO_VCC}$		STANDBY MODE VIO connected to VCC, $T_{VCC_SOFT_START}$	1.15		1.45	ms	CSAN0 LATCH
$T_{SC_CBMOS_REACT}$	Short-circuit reaction time of turning OFF CB MOSFETs				1.06	ms	CSAP0 CSAN0 VGx VSx

1. *Single shot samples are characterized by a superimposed Gaussian noise, with zero-mean and VSC_NOISE standard deviation*

4.9 GPIOs

The device features 2 GPIOs configurable according to the table below. In detail, the GPIO0 and GPIO1 can be configured as digital input/output or analog input connected to the external NTC (or to another sensor) using the GPIO<x>_CONF 2-bit field. The GPIOs configured as input are protected against back-feeding towards VTREF and VCC in case of an external short-to-battery event.

Table 67. GPIO configuration

GPIO<x>_CONF	Configuration
00	ADC Input (absolute)
01 (default config, for pins not configured as alternate functions by default)	ADC Input (ratiometric)
10	Generic Digital Input
11	Generic Digital Output (push/pull)

GPIOs can be used as simple I/O driven/read via dedicated registers:

- When configured as digital output, the GPIOs can be driven according to the GPO<x> bit.
- The input buffer status can be read via the GPI<x> bit.
  - When configured as digital input, an internal weak pull-down/pull-up can be configured programming GPIO<x>_PU_PD.

Table 68. GPIO weak pull-up/pull-down configuration

GPIO<x>_PU_PD	Configuration
0 (default)	Weak pull-down ($R_{GPIO_WK_PD}$)
1	Weak pull-up ($R_{GPIO_WK_PU}$)

Unused GPIOs shall be connected to AGND. They shall be left programmed as analog input via GPIO<x>_CONF.

4.9.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 69. GPIOs electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{GPIO_OUT_HIGH}$	GPIO high output value	I_{SOURCE} = 2mA	V_{VIO}-0.4			V	GPIOx
$V_{GPIO_OUT_LOW}$	GPIO low output value	I_{SINK} = 2mA			0.4	V	GPIOx
$V_{GPIO_IN_HIGH}$	GPIO high input level		2			V	GPIOx
$V_{GPIO_IN_HYS}$	GPIO input buffer hysteresis		0.1		0.5	V	GPIOx
$R_{GPIO_WK_PU}$	GPIO weak pull-up resistor	GPIO<x>_PU_PD = 1	0.4	1	1.6	MΩ	GPIOx
$R_{GPIO_WK_PD}$	GPIO weak pull-down resistor	GPIO<x>_PU_PD = 0	0.4	1	1.6	MΩ	GPIOx
$R_{GPIO_EXT_PU}$	GPIO external pullup resistor for open-drain configuration	Application information	-1%	4.7	+1%	KΩ	GPIOx
C_{GPIO_EXT}	GPIO external bypass capacitor	Application information, including parasitics			150	pF	GPIOx
$I_{LEAK_GPIO_HiZ}$	GPIO leakage current in HiZ	PU/PD disabled, 0 < V_{GPIOx} < 5V	-0.5	0	0.5	µA	GPIOx
f_{SW_GPIO}	GPIO switching frequency				42	KHz	GPIOx

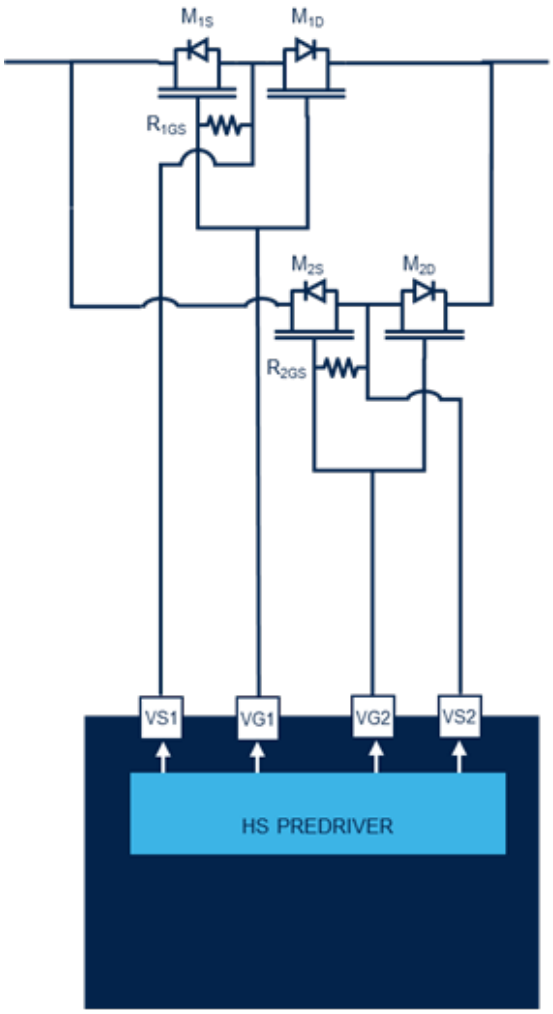
4.10 HS pre-drivers and CB MOSFETs

The L9988 integrates two high-side pre-driver stages designed to manage the opening/closing of a variable number N_{MOSFET} of couples of common-source back-to-back n-MOSFETs (Circuit Breaker (CB) MOSFETs, **MOS 1S-1D** and **MOS 2S-2D**) which provide the pack connection to external loads and the charger.

4.10.1 Driving output

The drivers control the **MOS 1S-1D** and **MOS 2S-2D** through direct gate charge/discharge of the MOSFETs gate-source voltage.

Figure 34. High-side CB back-to-back MOSFETs driving configuration



An external VGS pull-down resistance R_{1GS} and R_{2GS} shall be connected externally.

4.10.2 Driving commands

The MOSFET pairs are managed in the different states as follows:

- NORMAL MODE: MOS 1S-1D and MOS 2S-2D according to the table below
- STANDBY MODE and POWER DOWN MODE: the enabling bit HS_CMD_EN is automatically reset to keep MOS 1S-1D and MOS 2S-2D ON or OFF following the HS_CMD_IN1 and HS_CMD_IN2 bits
- SLEEP MODE: MOS 1S-1D and MOS 2S-2D always OFF

The driving of the high-side MOSFETs will be executed according to the following table, depending on:

- Detection of a Short-Circuit (SC) from the logic OR of SC_CHG and SC_DCHG bits, according to SC_HS_MASK (refer to Section 4.8.2)
- Detection of CP undervoltage from bit VCP_UV (refer to Section 4.3.2)
- Detection of MCU lock-step error from bit FCCU_FAIL, according to bit FCCU_REACT (refer to Section 4.12.4)
- The status of HS_IN1 and HS_IN2 pins when HS_CMD_EN=1 (refer to Table 70))

Table 70. Pre-drivers driving commands

Enable HS_CMD_EN	1	1	1	X	0
(SC = 1 AND SC_HS_MASK = 0) OR VCP_UV = 1 OR (FCCU_FAIL = 1 AND FCCU_REACT = 1)	0	0	0	1	0
HS_IN1	0	X	1	X	X
HS_IN2	X	0	1	X	X
MOS 1S-1D driving	According to HS_CMD_IN1	According to HS_CMD_IN1	OFF	OFF	According to HS_CMD_IN1
MOS 2S-2D driving	According to HS_CMD_IN2	According to HS_CMD_IN2	OFF	OFF	According to HS_CMD_IN2

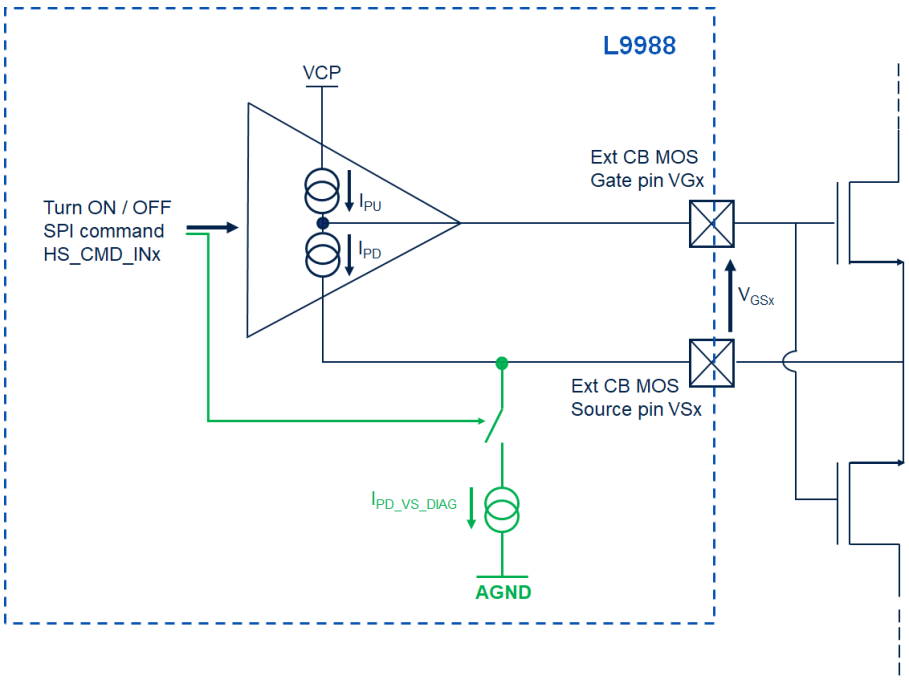
The meaning of the SPI commands HS_CMD_IN1 and HS_CMD_IN2 is as follows:

- HS_CMD_IN1 commands the MOS 1S-1D MOSFETs (logic '1' MOS ON; logic '0' MOS OFF)
- HS_CMD_IN2 commands the MOS 2S-2D MOSFETs (logic '1' MOS ON; logic '0' MOS OFF)

The direct gate control shall be intended as:

- ON state: (V(VGx) – V(VSx)) = $V_{GSx} > V_{GS_ON}$
- OFF state: (V(VGx) – V(VSx)) = $V_{GSx} < V_{GS_OFF}$

Figure 35. Pre-drivers principle architecture



4.10.3 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 71. Pre-drivers electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
C_{HSDRV_LOAD}	Equivalent capacitive load on VG1/VG2 pins (single couple of back-to-back MOS)	Application info, using recommended MOSFETs listed in Table 72		20	30	nF	VGx, VSx
V_{GS_ON}	VG1/VG2 ON voltage	V_{VBST} > 7V	8.5	10.5	12	V	VGx, VSx
$V_{GS_ON_LB}$ LB: LOW BATTERY	VG1/VG2 ON voltage	5V < V_{VBST} < 7V	6.2			V	VGx, VSx
V_{GS_OFF}	VG1/VG2 OFF voltage	I(CHG) = I(DCHG) = 0.450mA V(VSx) = 0V			100	mV	VGx, VSx
I_{PU}	VG1/VG2 Current source in steady state	V(VGx) - V(VSx) = 0V V(VSx) = 0V	0.15		0.69	mA	VGx, VSx
I_{PU_PEAK}	VG1/VG2 Current source peak	Design info	50		135	mA	VGx, VSx
I_{PD}	VG1/VG2 Current sink in steady state	V(VGx) - V(VSx) = 1.4V V(VSx) = 0V	40		330	mA	VGx, VSx
I_{PD_PEAK}	VG1/VG2 Current sink peak	Design info	230		590	mA	VGx, VSx
T_{HS_ON}	Turn-ON time	From received HS_INx command for the V_{GSx} transition from 0V to 7.2V, V(VSx) = 0V Cload(VG1) < 120nF Cload(VG2) = Cload(VG1) - 30nF (±2nF) using recommended MOSFETs listed in Table 72 Including digital synchronization jitter of HS_IN1 and HS_IN2 inputs			26	µs	VGx, VSx
$T_{HS_ON_MATCH}$	Turn-ON time match	Equal to T_{HS_ON}(VG2) - T_{HS_ON} (VG1) considering the worst case scenario of capacitive load mismatch where $N_{MOSFET1}$ = 4 and $N_{MOSFET2}$ = 3			10	µs	VGx, VSx
T_{HS_OFF}	Turn-OFF time	From received HS_INx command for the V_{GSx} transition from 10.5V to 100mV, V(VSx) = 0V Cload(VG1) < 120nF Cload(VG2) = Cload(VG1) - 30nF (±2nF) using recommended MOSFETs listed in Table 72 **including digital synchronization jitter of HS_IN1 and HS_IN2 inputs**			10	µs	VGx, VSx
$T_{HS_OFF_MATCH}$	Turn-OFF time match	Equal to T_{HS_OFF}(VG2) -T_{HS_OFF} (VG1) considering the worst case scenario of capacitive load mismatch where $N_{MOSFET1}$ = 4 and $N_{MOSFET2}$ = 3			1.6	µs	VGx, VSx
$N_{MOSFET1}$	Number of couples of MOSFETs connected to VG1		1		4		VGx, VSx

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$N_{MOSFET2}$	Number of couples of MOSFETs connected to VG2		1		3		VGx, VSx
$N_{MOSFET1-2}$	($N_{MOSFET1}$ - $N_{MOSFET2}$)		0		1		VGx, VSx
R_{1GS}, R_{2GS}	External VGS pulldown resistor	Application info	-20%	1	+20%	MΩ	VGx, VSx
$V_{HS_IN_H}$	HS_IN High level threshold	Tested in production	1.3		1.7	V	HS_IN1, HS_IN2
$V_{HS_IN_L}$	HS_IN Low level threshold	Tested in production	0.9		1.3	V	HS_IN1, HS_IN2

Note: External components are excluded from safety analysis. No internal diagnostics will be implemented in the device; ST will provide the failure rates to the system integrator, who will implement externally the safety mechanisms needed to reach the system ASIL target.

Table 72. Recommended external MOSFETs

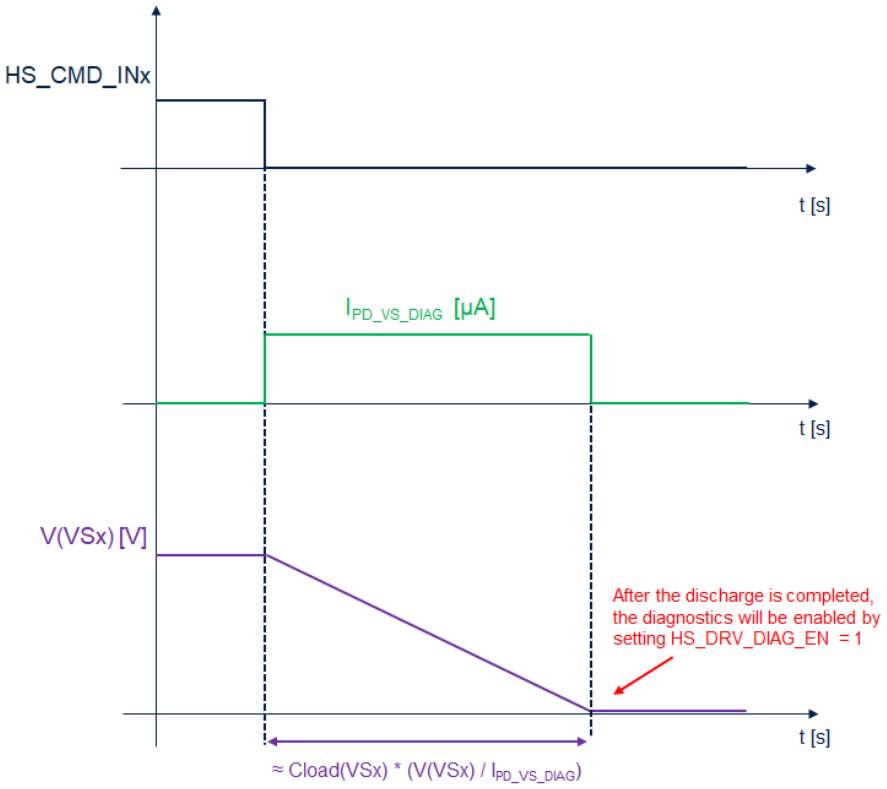
Part number	Maker	V_{DS_MAX} [V]	V_{GS_MAX} [V]	V_{GSth} [V]	I_D [A] @25°C	P_{TOT} [W] @25°C	R_{DSon} [mΩ] @V_{GS}=10V	Q_g [nC] @V_{GS}=10V
TPWR7904PB	Toshiba	40	20	2 min, 3 MAX	150	170	0.79	85
JMSL040SAGQ	JieJie Microelectronics	40	20	1.2 min, 2.5 MAX	349	139	0.75	116
STL325N4LF8AG	ST Microelectronics	40	16	1.2 min, 2 MAX	373	188	0.75	95
NVMFS5C410NL	ON Semiconductor	40	20	2 MAX	330	167	0.82	143

4.10.4 Diagnostics - VS1, VS2 ADC converters

The IC includes two dedicated ADC voltage converters used to measure the source voltage on pins VS1 and VS2 of each MOSFET back-to-back couple and to allow the MCU to perform a diagnostic of the CB MOSFETs status.

This measurement is available only in NORMAL MODE by setting the command HS_DRV_DIAG_EN = 1. The converted values are provided to the MCU in read-only registers VS1_ADC and VS2_ADC to perform a double check diagnostic of pre-drivers (in parallel with the conversions through external dedicated ADCs). In detail, to perform the diagnostics in NORMAL MODE, HS_CMD_INx is set to 0 and one of the two couples of common sources back-to-back CB MOSFETs is turned OFF for a certain period of time during which it is possible to check whether the source VSx is stuck by reading the value V(VSx) with the ADC. If everything is fine, the source will be discharged, and the conversion will be equal to 0V. To allow VSx to discharge during the diagnostic, a pull-down current $I_{PD_VS_DIAG}$ (refer to Figure 36) is automatically activated when HS_CMD_INx is set to 0 and the corresponding driver is turned OFF. Only after the discharge is completed (approximately after a time interval equal to [Cload(VSx) * (V(VSx) / $I_{PD_VS_DIAG}$)], with Cload(VSx) capacitive load connected to the VSx pin) will the diagnostics be enabled by setting HS_DRV_DIAG_EN to 1 and, at the end of the measurement, the VS1_DATA_READY and VS2_DATA_READY cleared on read registers are set.

Figure 36. **VS1, VS2 diagnostics scenario**



4.10.4.1 *VS1, VS2 ADC Built-In-Self-Test*

The L9988 allows testing the integrity of the VS1, VS2 ADCs setting the VS1_VS2_BIST_EN bit. During this procedure, the inputs of the ADCs are disconnected and a fixed voltage (ADC_VS_{RANGE} /2) is provided at the ADCs input; the results of the conversions are compared with an internal threshold and VS1_BIST_DONE, VS2_BIST_DONE cleared on read registers are set. The VS1_BIST_FAIL and VS2_BIST_FAIL cleared on read registers are set according to the BIST result.

4.10.4.2 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 73. **VS1, VS2 ADC converters electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$N_{BIT_ADC_VS}$	VS1, VS2 ADCs bit number			8		bit	VS1 VS2
ADC_VS_{RANGE}	VS1, VS2 ADCs voltage measurement range		0		25.6	V	VS1 VS2
ADC_VS_{RES}	VS1, VS2 ADCs resolution (LSB)	Design info. LSB calculated on ADC_VS_{RANGE}		100		mV	VS1 VS2
ADC_VS_{ACC1}	VS1, VS2 ADCs accuracy 1	0V < V(VSx) < 6V	-300		300	mV	VS1 VS2
ADC_VS_{ACC2}	VS1, VS2 ADCs accuracy 2	6V < V(VSx) < 19V	-5		+5	%	VS1 VS2
$T_{CONV_ADC_VS}$	VS1, VS2 ADCs total conversion time			128		µs	VS1 VS2
$I_{PD_VS_DIAG}$	Pull-down current for VSx discharge		40	50	60	µA	VS1 VS2

4.11 Oscillators

This section describes the device oscillators.

4.11.1 Low frequency standby oscillator (OSC_STBY)

The low frequency standby oscillator operates at f_{STBY_OSC} and is always active.

4.11.1.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 74. Standby oscillator electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
f_{STBY_OSC}	Oscillator frequency		-8%	500	+8%	KHz	-

4.11.2 High frequency main oscillator (OSC_MAIN)

The high frequency main oscillator operates at f_{MAIN_OSC} and is only active in NORMAL state and in POWER DOWN state.

4.11.2.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 75. Main oscillator electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
f_{MAIN_OSC}	Oscillator frequency		-6%	16	+6%	MHz	-

4.11.3 Normal oscillator monitor

When in NORMAL, the main and standby oscillators (OSC_MAIN and OSC_STBY) are monitoring each other. In case of frequency drift detection or main oscillator stuck, the OSC_FAIL flag is set (cleared upon read), **FSO1, FSO2** lines are asserted (both **LOW**) and the IC moves to POWER DOWN state.

In case the standby oscillator is stuck, the IC will move to SLEEP state. A new wakeup attempt can be detected as soon as the standby oscillator recovers.

If an oscillator is stuck, this is detected in $T_{OSC_STUCK_TIMEOUT}$.

The oscillator monitor is covered by BIST at each wakeup from low-power states. In case of failure, the CLK_MON_SELFTEST_FAIL is set (cleared upon read). This flag has to be checked at least 13 ms after the power-up.

It is possible to check the completion of the execution of oscillators monitor BIST through the flag CLK_MON_SELFTEST_DONE.

4.11.3.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 76. Normal oscillator monitor electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$f_{OSC_MON_ERR}$	Oscillator delta frequency threshold	Guaranteed by SCAN	20		40	%	-
$T_{OSC_STUCK_TIMEOUT}$	Oscillator stuck detection timeout	Guaranteed by SCAN		2		ms	-

4.11.4 XTAL oscillator

The L9988 is equipped with the XIN and XUOT pins that permit to connect an external XTAL oscillator (f_{XTAL}) used to provide the internal real time clock and the internal RTC wakeup.

In case the external crystal is not connected, the MCU can set the bit XTAL_DISABLE in NORMAL MODE to use an internal oscillator (f_{RTC_int}) with a relaxed accuracy during STANDBY MODE.

During STANDBY MODE, the XTAL oscillator working according to XTAL_DISABLE is monitored by the standby oscillator monitor as described in Section 4.11.5. In case XTAL_DISABLE = 0 and the crystal is not connected, the standby oscillator monitor fault is detected in STANDY MODE or in POWER DOWN MODE and the device moves to SLEEP MODE.

4.11.4.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 77. XTAL Oscillator electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
f_{XTAL}	Oscillator frequency with crystal	XTAL, C_{1_XTAL}, C_{2_XTAL}, R_{d_XTAL}: refer to Table 78	-0.5%	32.768	+0.5%	KHz	XIN XOUT
$T_{XTAL_STARTUP}$	XTAL Oscillator start up time	XTAL, C_{1_XTAL}, C_{2_XTAL}, R_{d_XTAL}: refer to Table 78			1	s	XIN XOUT
f_{RTC_int}	Oscillator frequency without crystal		-6%	32.768	+6%	KHz	-

Table 78. External components list for XTAL Oscillator

Symbol	Parameter	Typ. value	Unit	Tolerance	Thermal characteristics
R_{d_XTAL}	XTAL resistor connected to XOUT pin	330	KΩ	±5%	±50 ppm/K
C_{1_XTAL}	XTAL capacitor connected to XIN pin	82	pF	±5%	±30 ppm/K
C_{2_XTAL}	XTAL capacitor connected to R_{d_XTAL}	15	pF	±5%	±30 ppm/K
XTAL	XTAL crystal connected to XIN and XOUT pins	32.768	KHz	±50ppm	-

4.11.5 Standby oscillator monitor

When in STANDBY or in POWER DOWN MODE, the standby oscillator (OSC_STBY) and the XTAL oscillators are monitoring each other. In case of frequency drift detection, the device will move to SLEEP state.

Even if either of the two oscillators is stuck, the IC will move to SLEEP state.

A new wakeup attempt can be detected as soon as the standby oscillator recovers.

If an oscillator is stuck, this is detected in $T_{OSC_STUCK_TIMEOUT_STBY}$.

4.11.5.1 Electrical Parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 79. Standby Oscillator monitor electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$f_{OSC_MON_ERR_STBY}$	Oscillator delta frequency threshold	Guaranteed by SCAN	25		55	%	-
$T_{OSC_STUCK_TIMEOUT_STBY}$	Oscillator stuck detection timeout	Guaranteed by SCAN			100	ms	-

4.12 Digital I/O

4.12.1 Fault interrupt (FAULT)

FAULT is a push-pull output asserted in case of failures detected during the Voltage Conversion Routine (refer to Section 4.4), the Current Conversion Routine (refer to Section 4.8), the Cell Balancing (refer to Section 4.5) or related to Q&A Watchdog (refer to Section 4.16.1). It is intended to interrupt MCU activity upon failure detection. Several failures can be redirected to the FAULT line depending on their masking bit according to each diagnostic described in the dedicated sections.

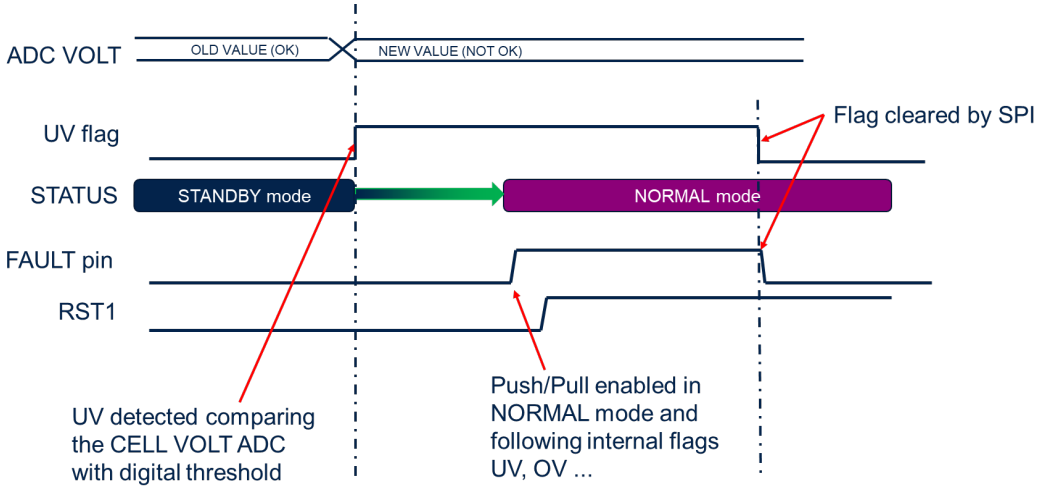
Table 80. FAULT interrupt pin

Pin name	Active level	Clear	Type	NORMAL	STANDBY	SLEEP
FAULT	HIGH	As soon as related SPI flags are properly cleared	Push-pull	Asserted after • Cells/VBS/VPP/GPIO monitor diagnostics fault, cell temperature monitor fault and Cell/AIN/GPIO open load diagnostics fault during VCR (if enabled, detection in NORMAL or STANDBY) • OVC detection, CC redundancy check, CS-CC cross-check during CCR (if enabled, detection in NORMAL or STANDBY) • Charge/discharge detection CC_WUP (if enabled, detection only in STANDBY) • Balancing OVC detection (if enabled, detection in NORMAL or STANDBY) • Q&A watchdog fail (if enabled, detection in NORMAL) • VBP-VBS compare fail (if enabled, detection in NORMAL or STANDBY) • Cyclic CRC error (if enabled, detection in NORMAL or STANDBY)	OFF	OFF

The FAULT pin is available in NORMAL MODE.

In the following figure, an example of cell UV diagnostic in STANDBY MODE triggering the FAULT pin after the transition in NORMAL MODE is illustrated.

Figure 37. Cell UV detection in STANDBY MODE



4.12.1.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 81. FAULT electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{FAULT_LOW}	FAULT low voltage	I_{FAULT} = 2mA			0.4	V	FAULT
V_{FAULT_HIGH}	FAULT high voltage	I_{FAULT} = 2mA	V_{VIO} – 0.4			V	FAULT

4.12.2 Latch interrupt (LATCH)

LATCH is a push-pull output asserted in case of failures related to the short-circuit detection (refer to Section 4.9). It is intended to interrupt MCU activity upon failure detection.

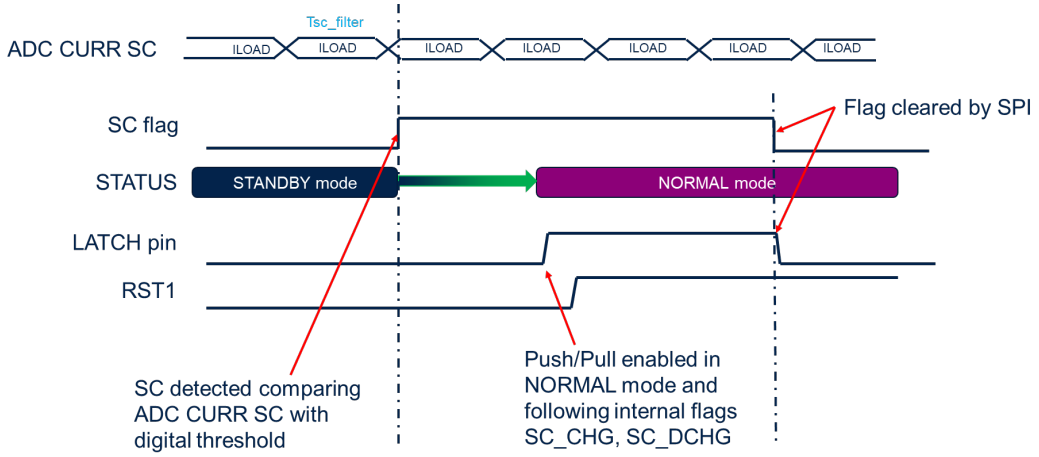
Table 82. LATCH interrupt pin

Pin name	Active level	Clear	Type	NORMAL	STANDBY	SLEEP
LATCH	HIGH	As soon as related SPI flags are properly cleared	Push-pull	Asserted after short-circuit detection (if enabled, detection in NORMAL or STANDBY)	OFF	OFF

The LATCH pin is available in NORMAL MODE.

In the following figure, an example of short-circuit detection in STANDBY MODE triggering the LATCH pin after the transition in NORMAL MODE is illustrated.

Figure 38. Short-circuit detection in STANDBY MODE



4.12.2.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 83. LATCH electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{LATCH_LOW}	LATCH low voltage	I_{LATCH} = 2mA			0.4	V	LATCH
V_{LATCH_HIGH}	LATCH high voltage	I_{LATCH} = 2mA	V_{VIO} – 0.4			V	LATCH

4.12.3 Fail Safe Output (FSO)

FSO is a push-pull output asserted in case of power supply failures or SPI ERROR or oscillator monitor faults in NORMAL MODE state. If enabled for LDO3 (VTREF) and LDO4 (VSTBY), detection is possible also in STANDBY MODE after the transition in NORMAL MODE. The pins FSO1 (active high) and FSO2 (active low) are driven with opposite polarity if VIO is in its operating range. The status of FSO1 and FSO2 pins filtered are available via SPI by reading the bits FSO1_ECHO and FSO2_ECHO (in NORMAL MODE).

Figure 39. FSO1 and FSO2 active level

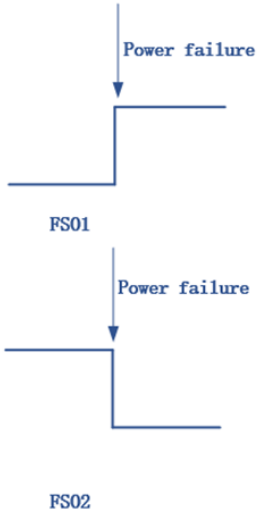


Table 84. Fail safe output FSO1, FSO2 pins

Pin name	Active level	Clear	Type	NORMAL	STANDBY	SLEEP	POWER DOWN
FSO1	HIGH	As soon as related SPI flags are properly cleared	Push-pull	Asserted in case of power supply diagnostics failures, SPI ERROR or normal oscillator monitor fail	OFF	OFF	LOW
FSO2	LOW	As soon as related SPI flags are properly cleared	Push-pull	Asserted in case of power supply diagnostics failures, SPI ERROR or normal oscillator monitor fail	OFF	OFF	LOW

4.12.3.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 85. FSO1, FSO2 electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{FSO_LOW}	FSO low voltage	I_{FSO} = 2mA			0.4	V	FSO1, FSO2
V_{FSO_HIGH}	FSO high voltage	I_{FSO} = 2mA	V_{VIO} – 0.4			V	FSO1, FSO2

4.12.4 MCU lock-step error detection (FCCU)

MCUs have an internal error checking logic reporting any misbehavior on clock, power-supply, ECC, memory, lock-step execution, etc. The status of such error-checking logic is reported by one or more MCU digital outputs that can be sensed by an external monitor to determine the MCU functional status.

The IC embeds such a monitoring unit, called FCCU, which can be enabled via FCCU_MON_EN. To prevent inadvertent RST1 assertion after having enabled the FCCU, all the enabled checkers shall be correctly served before their fault deglitch timer expires. Further details about normal conditions and fault deglitch timers are available in the checkers sub-paragraphs. Since the FCCU cannot be served if the MCU is under reset, the FCCU_MON_EN bit will automatically be reset by the IC whenever RST1 output is asserted.

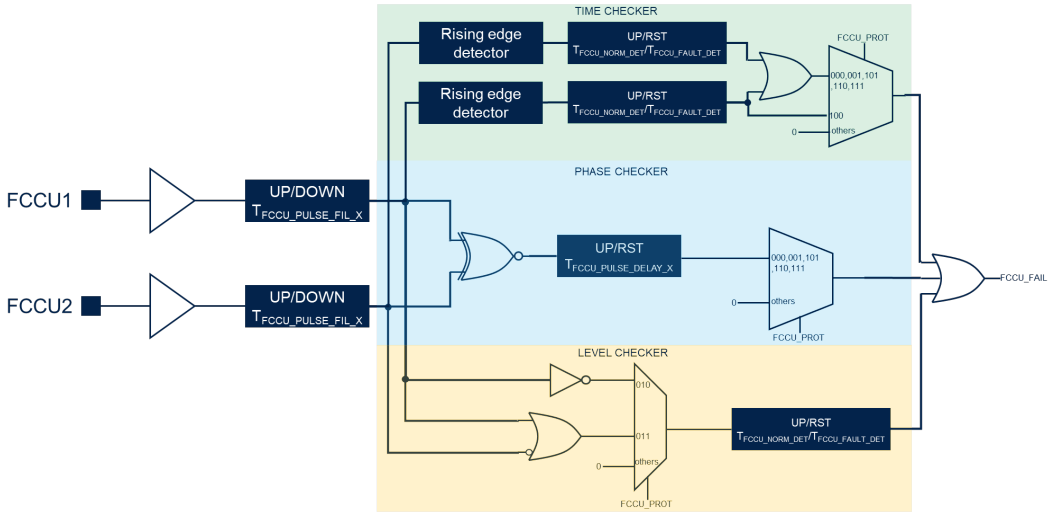
Signal output of the MCU error logic may vary according to different implementations. The FCCU offers programmability for adapting to different MCU models (FCCU_PROT).

The FCCU supports up to two monitor inputs: FCCU1 and FCCU2. Before being processed, signals input on the FCCU pins are first deglitched with an up/down counter $T_{FCCU_PULSE_FIL}$, programmable via FCCU_PLS_FLT.

Figure 40 describes the FCCU logic architecture, which is composed of the following parts:

- **Level checker**: checks coherency on FCCUx signal levels (available in both single-ended and differential versions)
- **Phase checker**: checks coherency on FCCUx relative signal phases (only available for differential protocols)
- **Time checker**: checks stuck @ faults on FCCUx signals (available in both single-ended and differential versions)

Figure 40. FCCU logic diagram



Depending on the configured FCCU_PROT, the logic blocks are treated as reported in the table below.

Table 86. FCCU checkers behavior according to FCCU_PROT configuration

FCCU_PROT	Level checker	Phase checker	Time checker	Recommended for
000, 001, 101, 110, 111	Disabled	Enabled	Enabled on both FCCU1/FCCU2	Dual-rail and time-switching protocols
010	Enabled on both FCCU1/FCCU2	Disabled	Disabled	Differential bi-stable protocol
011	Enabled on FCCU1	Disabled	Disabled	Single-ended bi-stable protocol
100	Disabled	Disabled	Enabled on FCCU1	Single-ended time-switching protocol

When either of the enabled blocks sets its error output, the event will be latched in the FCCU_FAIL flag. The IC will react by turning off the circuit breakers after T_{FCCU_DELAY} (programmable via FCCU_DELAY). Such a reaction can be masked by setting FCCU_REACT = 0.

4.12.4.1 *Level checker*

When enabled, this block checks the level of the deglitched signals according to the following truth tables.

Table 87. Level checker behavior for FCCU_PROT = 010

FCCU1	FCCU2	Output
0	1	No error
X	X	Error

Table 88. Level checker behavior for FCCU_PROT = 011

FCCU1	Output
0	Error
1	No error

If the error condition lasts longer than $T_{FCCU_FAULT_DET}$ (programmable via FCCU_FAULT_DET_TIME), the block will set its error output. Conversely, if the error condition is removed for longer than $T_{FCCU_NORM_DET}$ (programmable via FCCU_NORM_DET_TIME), the block error output will be reset.

4.12.4.2 *Phase checker*

When enabled, this block checks that signals on FCCU1 and FCCU2 are in counter-phase. If levels overlap for longer than $T_{FCCU_PULSE_DELAY}$ (programmable via FCCU_PLS_DLY), the block will set its error output. Conversely, if the error condition is removed for longer than $T_{FCCU_NORM_DET}$ (programmable via FCCU_NORM_DET_TIME), the block error output will be reset.

4.12.4.3 *Time checker*

When enabled, the time checker block verifies whether the input signal period is within defined limits. This is done counting the time between two signal rising edges. When using the smallest deglitch filter ($T_{FCCU_PULSE_FIL_0}$), minimum detectable pulse duration is $T_{FCCU_PULSE_DET}$.

Table 89. Time checker behavior for FCCU_PROT = 000, 001, 101, 110, 111

FCCU1	FCCU2	Output
Period ≤ $T_{FCCU_NORM_DET}$	Period ≤ $T_{FCCU_NORM_DET}$	No error
Period ≤ $T_{FCCU_NORM_DET}$	Period > $T_{FCCU_FAULT_DET}$	Error
Period > $T_{FCCU_FAULT_DET}$	Period ≤ $T_{FCCU_NORM_DET}$	Error
Period > $T_{FCCU_FAULT_DET}$	Period > $T_{FCCU_FAULT_DET}$	Error

Table 90. Time checker behavior for FCCU_PROT = 100

FCCU1	Output
Period ≤ $T_{FCCU_NORM_DET}$	No error
Period > $T_{FCCU_FAULT_DET}$	Error

If the error condition lasts longer than $T_{FCCU_FAULT_DET}$ (programmable via FCCU_FAULT_DET_TIME), the block will set its error output. Conversely, if the error condition is removed for longer than $T_{FCCU_NORM_DET}$ (programmable via FCCU_NORM_DET_TIME), the block error output will be reset.

4.12.4.4 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 91. FCCU1, FCCU2 electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{FCCU_HIGH}	FCCU high voltage		2			V	FCCU1, FCCU2
V_{FCCU_HYS}	FCCU hysteresis voltage		0.1		0.5	V	FCCU1, FCCU2
R_{FCCU_PD}	FCCU pull-down resistor		0.4	1	1.6	MΩ	FCCU1, FCCU2
$T_{FCCU_NORM_DET_00}$	FCCU Normal state detection time	FCCU_NORM_DET_TIME = 00		1		ms	FCCU1, FCCU2
$T_{FCCU_NORM_DET_01}$	FCCU Normal state detection time	FCCU_NORM_DET_TIME = 01		32		ms	FCCU1, FCCU2
$T_{FCCU_NORM_DET_10}$	FCCU Normal state detection time	FCCU_NORM_DET_TIME = 10		60		ms	FCCU1, FCCU2
$T_{FCCU_NORM_DET_11}$	FCCU Normal state detection time	FCCU_NORM_DET_TIME = 11		180		ms	FCCU1, FCCU2
$T_{FCCU_FAULT_DET_00}$	FCCU Fault state detection time	FCCU_FAULT_DET_TIME = 00		1		ms	FCCU1, FCCU2
$T_{FCCU_FAULT_DET_01}$	FCCU Fault state detection time	FCCU_FAULT_DET_TIME = 01		32		ms	FCCU1, FCCU2
$T_{FCCU_FAULT_DET_10}$	FCCU Fault state detection time	FCCU_FAULT_DET_TIME = 10		60		ms	FCCU1, FCCU2
$T_{FCCU_FAULT_DET_11}$	FCCU Fault state detection time	FCCU_FAULT_DET_TIME = 11		180		ms	FCCU1, FCCU2
$T_{FCCU_PULSE_DELAY_0}$	Phase shift detection time	FCCU_PLS_DLY = 0		2		µs	FCCU1, FCCU2
$T_{FCCU_PULSE_DELAY_1}$	Phase shift detection time	FCCU_PLS_DLY = 1		4		µs	FCCU1, FCCU2
$T_{FCCU_PULSE_DET}$	Minimum detectable pulse width	FCCU_PLS_FLT = 0		4		µs	FCCU1, FCCU2
$T_{FCCU_PULSE_FIL_0}$	FCCU input deglitch filter time	FCCU_PLS_FLT = 0		2		µs	FCCU1, FCCU2
$T_{FCCU_PULSE_FIL_1}$	FCCU input deglitch filter time	FCCU_PLS_FLT = 1		4		µs	FCCU1, FCCU2 FCCU1, FCCU2
$T_{FCCU_DELAY_00}$	Delay between FCCU fault detection and CB MOSFETs switch OFF	FCCU_DELAY = 00		0		ms	FCCU1, FCCU2
$T_{FCCU_DELAY_01}$	Delay between FCCU fault detection and CB MOSFETs switch OFF	FCCU_DELAY = 01		2		ms	FCCU1, FCCU2
$T_{FCCU_DELAY_10}$	Delay between FCCU fault detection and CB MOSFETs switch OFF	FCCU_DELAY = 10		4		ms	FCCU1, FCCU2
$T_{FCCU_DELAY_11}$	Delay between FCCU fault detection and CB MOSFETs switch OFF	FCCU_DELAY = 11		8		ms	FCCU1, FCCU2

4.12.5 MCU reset (RST1)

RST1 is a push-pull output that is set in order to reset the MCU.

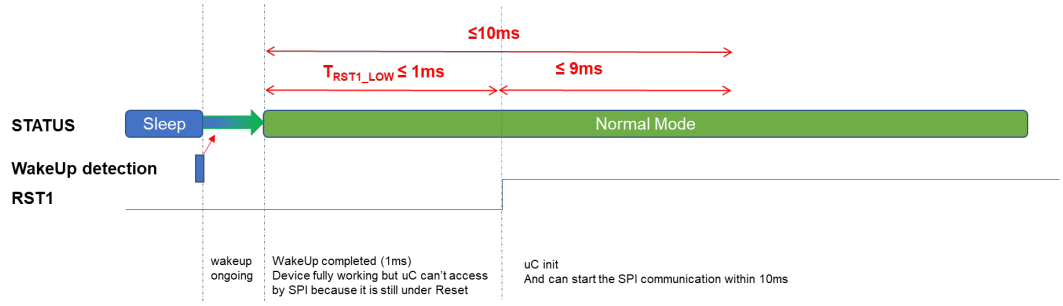
The pin is active low, and it is asserted in case of VCORE undervoltage and VCORE overvoltage diagnostics (refer to Section 4.3.5.1), WD1 and WD2 fail (refer to Section 4.16.1 and Section 4.16.2). It is used to reset certain registers in the register map - specifically, those registers listed under Reset Sources that include rst1_sync or rst1_sw_reset_sync.

Table 92. RST1 pin

Pin name	Active level	Clear	Type	NORMAL	STANDBY	SLEEP
RST1	LOW	After the T_{RST1_LOW} reset time de-assertion filter	Push-pull	Asserted in case of VCORE_UV, VCORE_DEEP_UV, VCORE_OV, VCORE_OT, Q&A watchdog and second watchdog fails	OFF	OFF

The RST1 pin is available in NORMAL MODE. In the following figure, the timing diagram for a power up sequence by wake detection in SLEEP MODE with the indication of T_{RST1_LOW} is illustrated.

Figure 41. Power up by wake detection in SLEEP MODE



4.12.5.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 93. RST1 electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{RST1_HIGH}	RST1 high voltage		V_{VIO} – 0.4			V	RST1
V_{RST1_LOW}	RST1 low voltage				0.4	V	RST1
T_{RST1_LOW}	Reset time de-assertion filter				1	ms	RST1

4.12.6 Software reset (SW_RST) – hardware reset (device reset: RST2)

RST2 is a digital input that can generate the reset of some blocks of the L9988, which is a hardware reset. The pin is active high.

The same reset is also possible by sending a SW_RST sequence via SPI, which is a software reset.

Table 94. Blocks reset by software reset and hardware reset

Blocks
PRN Watchdog
Q&A Watchdog
FCCU1, FCCU2 Digital IN pins

Blocks
Digital OUT fault pins (LATCH, FAULT, FSO…)
GPIOs Digital IN/OUT
Voltage Conversion Routine (Cells, GPIOs Analog IN, Internal nodes, Diagnostics)
Voltage ADC logics
Current Conversion Routine (CS, Coulomb Counter)
CS ADC logic
CC ADC logic
CC Accumulators
Short Circuit Detection
RTC and Cyclic Activation
Safety: Current (X-CHECK CS-CC)
Safety: Voltage (ADC Swapping, Plausibility check VBS vs. Sum of Cells, etc.)
Cyclic CRC trimming/Configuration Registers
Balancing and related Diagnostics

To generate a software reset by SPI, the following procedure shall be implemented. Once triggered, the software reset procedure will reset some R/W and CR SPI registers to their default values according to the register map table and the blocks listed in Table 90.

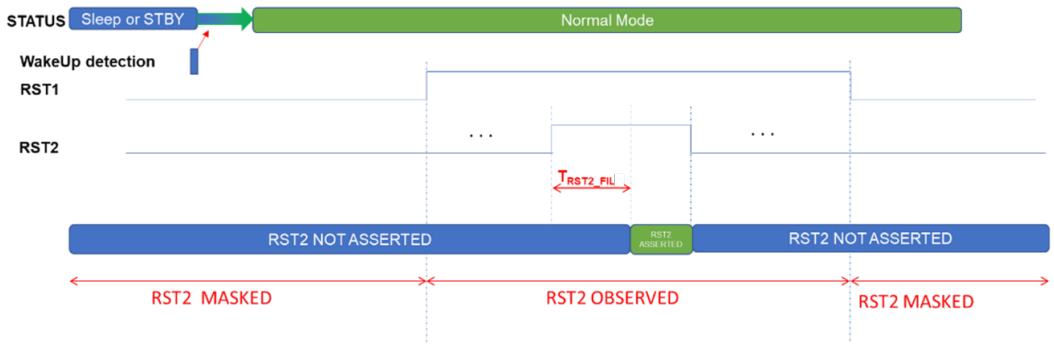
Procedure 5 – software reset SW_RST

1. MCU writes 0xE1 in the write-only field SPECIAL_KEY in the SPECIAL_REG register to enter partial reset mode
2. MCU writes 0x1E in the write-only field SPECIAL_KEY in the SPECIAL_REG register to confirm reset

Frames must be sent exactly in this sequence, otherwise registers will not be reset. The user SW can eventually trigger a re-download of the configuration from the Non-Volatile Memory (NVM).

To generate a hardware reset by the RST2 pin, the following sequence must be followed. RST2 is masked until RST1 is released. When RST1=1, the reset will be accepted only if the RST2 pulse lasts longer than T_{RST2_FIL}.

Figure 42. RST2 assertion in the power up sequence by wake detection in SLEEP or STANDY MODE



4.12.6.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 95. RST2 electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{RST2_HIGH}	RST2 high voltage		2			V	RST2
V_{RST2_HYS}	RST2 hysteresis voltage		0.1		0.5	V	RST2
T_{RST2_FIL}	RST2 filter time		5		10	µs	RST2
R_{RST2_PD}	RST2 pull-down resistor		0.4	1	1.6	MΩ	RST2

4.12.7 Data ready interrupt (INTC)

INTC is a push-pull output that is used to interrupt MCU activity at the end of voltage and current conversion routines if SOC by internal timer is enabled. The INTC pin generates a positive edge at the end of the voltage conversion routine and the current conversion routine, and it automatically generates a negative edge at the new SOC.

The INTC pin stays high for at least T_{INTC_PULSE} to inform the MCU that measurement data is available also in case the new SOC is generated during T_{INTC_PULSE}.

Table 96. INTC pin

Pin name	Active level	Clear	Type	NORMAL	STANDBY	SLEEP
INTC	HIGH	At new SOC command by internal timer	Push-pull	Asserted at the end of VCR and CCR if SOC by internal timer is enabled	OFF	OFF

4.12.7.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 97. INTC electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{INTC_HIGH}	INTC high voltage		V_{VIO} – 0.4			V	RST1
V_{INTC_LOW}	INTC low voltage				0.4	V	RST1
T_{INTC_PULSE}	INTC pulse time			10		µs	INTC

4.12.8 RTC wakeup state (RTCWPST)

RTCWPST is a push-pull output that is set to 1 when the RTC wake up procedure has concluded (refer to 4.13). The pin is available in NORMAL state, and it is active high.

Table 98. RTCWPST state pin

Pin name	Active level	Clear	Type	NORMAL	STANDBY	SLEEP
RTCWPST	HIGH	As soon as RTC WUP flag is properly cleared, internal RTC counter is reset	Push-pull	Asserted after RTC WUP procedure has concluded	OFF	OFF

4.12.8.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 99. RTCWPST electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$V_{RTCWPST_HIGH}$	RTCWPST high voltage		V_{VIO} – 0.4			V	RTCWPST
$V_{RTCWPST_LOW}$	RTCWPST low voltage				0.4	V	RTCWPST

4.12.9 Edge-triggered wakeup (WAKE)

WAKE is a digital input sensitive to positive edge only by default (after OFF state transition). It is intended to wake up the L9988 from low-power modes, forcing the transition from SLEEP to NORMAL state or from STANDBY to NORMAL state.

The wake up occurs when a toggle (according to the programmed edge) of the WAKE pin is detected, and it keeps the new level for a time longer than T_{WAKE_FIL}.

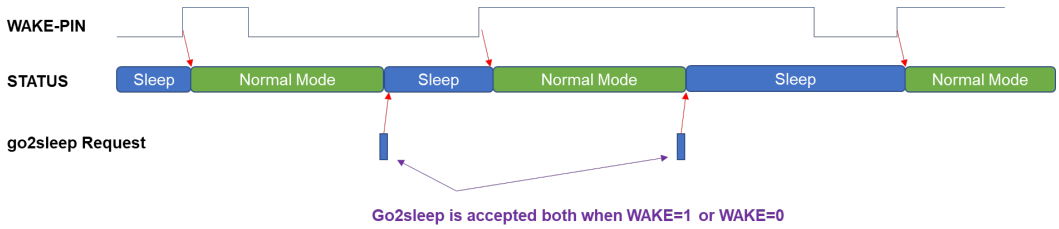
The status of the WAKE pin filtered is available via SPI by reading the bit WAKE_ECHO (in NORMAL MODE).

The WAKE_EDGE_CONFIG bit can be programmed in NORMAL MODE to select rising (“0”) or falling (“1”) detection.

Table 100. WAKE pin

Pin Name	Edge	Active level	Type	NORMAL	STANDBY	SLEEP
WAKE	Programmable: RISING (default), FALLING	-	Digital input	Ignored	Active, the IC moves to NORMAL MODE	Active, the IC moves to NORMAL MODE

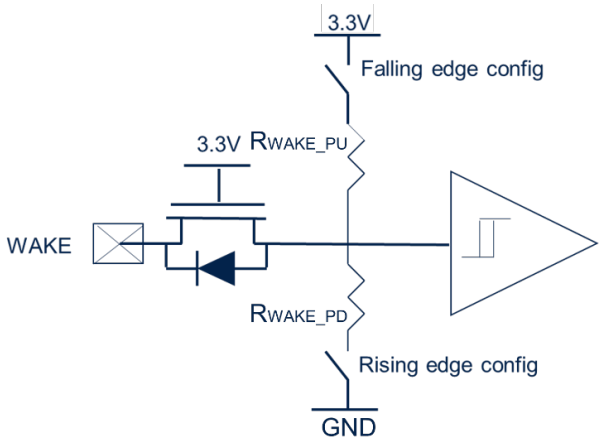
Figure 43. Wake detection by rising edge and GO2SLP request



In order to avoid a floating input in case of pin open, passive pull-up/down resistors are integrated:

- Pull-up in case of falling edge configuration. In this way there will be a current flowing in WAKE pin only when it is low.
- Pull-down in case of rising edge configuration. In this way there will be a current flowing in WAKE pin only when it is high.
- Current estimated in passive pull-up/down is 5µA.

Figure 44. **WAKE digital input structure**



4.12.9.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 101. **WAKE electrical parameters**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
T_{WAKE_FIL}	WAKE filter time		450		550	µs	WAKE
V_{WAKE_TH+}	WAKE rising edge threshold voltage		1.3	1.5	1.7	V	WAKE
V_{WAKE_TH-}	WAKE falling edge threshold voltage		1	1.1	1.25	V	WAKE
V_{WAKE_HYS}	WAKE hysteresis voltage		100		500	mV	WAKE
R_{WAKE_PU}	WAKE pull-up resistor		0.4	1	1.6	MΩ	WAKE
R_{WAKE_PD}	WAKE pull-down resistor		0.4	1	1.6	MΩ	WAKE

4.12.10 Level-triggered wakeup (IGN)

IGN is a high-voltage digital input sensitive to positive level. It is intended to wake up the L9988 from low-power modes and vice-versa, according to the ignition switch position.

A wakeup condition is triggered if a voltage higher than V_{IGN_HIGH} is applied to the IGN pin for an interval longer than T_{IGN_FIL}.

The status of the IGN pin filtered is available via SPI by reading the bit IGN_ECHO (in NORMAL MODE).

Similarly, the device moves to a low-power state if a voltage lower than V_{IGN_HIGH} - V_{IGN_HYS} is applied to the IGN pin for an interval longer than T_{IGN_FIL} and, after this, a GO2SLP or GO2STBY command is sent by SPI. Note that a GO2SLP or GO2STBY command is ignored if a voltage higher than V_{IGN_HIGH} is applied to the IGN pin.

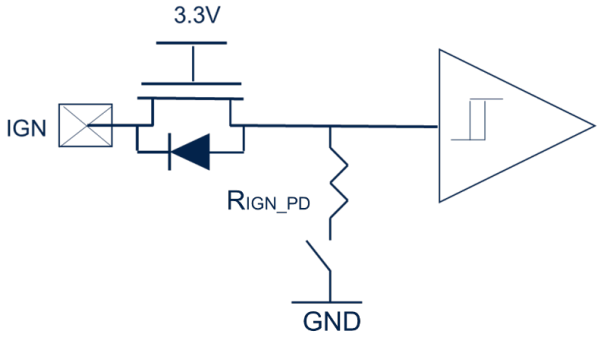
Once a state transition has been initiated, the IGN source will be masked until the transition is complete.

Table 102. **IGN pin**

Pin name	Edge	Active level	Type	NORMAL	STANDBY	SLEEP
IGN	-	HIGH	Digital input	Active. If LOW and GO2SLP cmd is sent via SPI, the IC moves to SLEEP MODE. If LOW and GO2STBY cmd is sent via SPI, the IC moves to STANDBY MODE.	Active. If HIGH, the IC moves to NORMAL MODE.	Active. If HIGH, the IC moves to NORMAL MODE.

In order to avoid floating input in case of pin open, a passive pull-down is integrated. In this way, there will be a current flowing in the IGN pin only when it is high. The current estimated in passive pull-down is 5 µA.

Figure 45. IGN digital input structure



4.12.10.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 103. IGN electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{IGN_HIGH}	IGN high voltage		2			V	IGN
V_{IGN_HYS}	IGN hysteresis voltage		0.1		0.5	V	IGN
T_{IGN_FIL}	IGN filter time		450		550	µs	IGN
R_{IGN_PD}	IGN pull-down resistor		0.4	1	1.6	MΩ	IGN

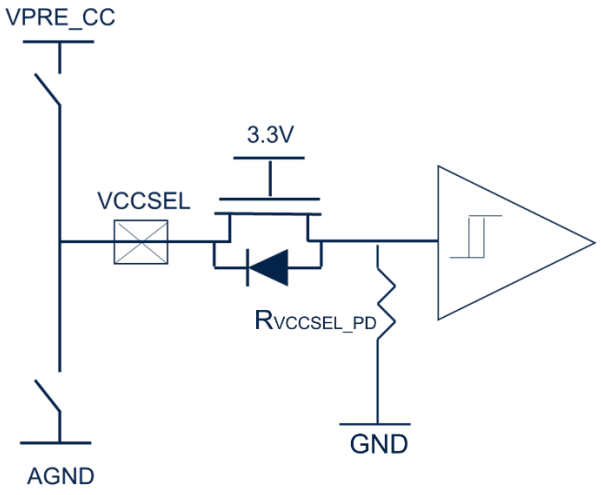
4.12.11 VCC selection (VCCSEL)

VCCSEL is a digital input used to configure the VCC regulated output voltage of LDO1.

In detail:

- if VCCSEL = 0, that is the pin is connected to AGND, V_{VCC} = 3.3V
- if VCCSEL = 1, that is the pin is connected to VPRE_CC pin, V_{VCC} = 5V

Figure 46. VCCSEL digital input structure and external connection



4.12.11.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 104. VCCSEL electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{VCCSEL_HIGH}	VCCSEL high voltage		2			V	VCCSEL
V_{VCCSEL_HYS}	VCCSEL hysteresis voltage		0.1		0.5	V	VCCSEL
R_{VCCSEL_PD}	VCCSEL internal pull-down resistor		0.4	1	1.6	MΩ	VCCSEL
T_{VCCSEL_FIL}	VCCSEL filter time			5		µs	VCCSEL

4.13 Internal RTC wakeup

The RTC wakeup procedure exploits the XTAL oscillator (with or without crystal) to generate the selectable time period $T_{CYCLE_STANDBY}$programmed via SPI using the **CYCLE_STANDBY** 4-bit field.

Procedure 6 – Internal RTC Wakeup

A counter will register the number $N_{CYCLE_STANDBY}$ of $T_{CYCLE_STANDBY}$ cycles that have occurred since entering the STANDBY state. Any time the NORMAL state is entered from STANDBY:

- The latest NCYCLE_STANDBY can be read by the MCU in the read-only 24-bit N_CYCLE_STANDBY_STATUS field, divided into N_CYCLE_STANDBY_STATUS_MSB (12-bit) and N_CYCLE_STANDBY_STATUS_LSB (12-bit) registers.

When $N_{CYCLE_STANDBY}$ reaches the maximum number (programmed via SPI using the N_CYCLE_STANDBY 24-bit field divided into N_CYCLE_STANDBY_MSB (12-bit) and N_CYCLE_STANDBY_LSB (12-bit), different from 0x00; in case **N_CYCLE_STANDBY** = 0x00, the internal RTC Wakeup is disabled), the MCU is woken up by entering NORMAL MODE state and:

- the pin RTCWPST is asserted.
- the SPI flag RTCWUP is set. This flag is cleared on read by the MCU
- when the flag is cleared, the $N_{CYCLE_STANDBY}$ is reset.

Note that N_CYCLE_STANDBY=0x00 means that internal RTC is disabled when the device enters STANDBY MODE state. In this case, the L9988 is in full STANDY MODE state, with no cyclic activation.

If the cyclic activation is needed, N_CYCLE_STANDBY=0x00 should be above 0, and depends on how long the device needs to stay in STANDBY MODE state.

4.13.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 105. Internal RTC wakeup electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$N_{CYCLE_STANDBY}$	Maximum number of $T_{CYCLE_STANDBY}$ cycles before device moves to NORMAL STATE; with 0x00 configuration, internal RTC wakeup is disabled $N_{CYCLE_STANDBY} = CODE_{N_CYCLE_STANDBY}$		1		$(2^{24}-1)$	-	-
$T_{CYCLE_STANDBY}$	Time period during which the voltage and current conversion routines are cyclically performed in STANDBY MODE (4 bit) $T_{CYCLE_STANDBY} = 1s * (CODE_{CYCLE_STANDBY} + 1)$		1		16	s	-

4.14 SPI interface

The IC integrates a SPI Target peripheral to be connected to the MCU.

4.14.1 Physical layer - SPI target

The SPI pins are:

- NCS: Chip select (digital input, weak pullup R_{IN_PU})
- SDI: Serial data input (digital input, weak pull-down R_{IN_PD})
- SDO: Serial data output (digital output). The output buffer is connected to **VIO.**
- SCL: Serial clock (digital input, weak pull-down R_{IN_PD})

Weak pull-down resistors on SDI and SCL pins and wake pull-up resistor on NCS pin are always enabled to address open failures.

Figure 47. SPI physical layer

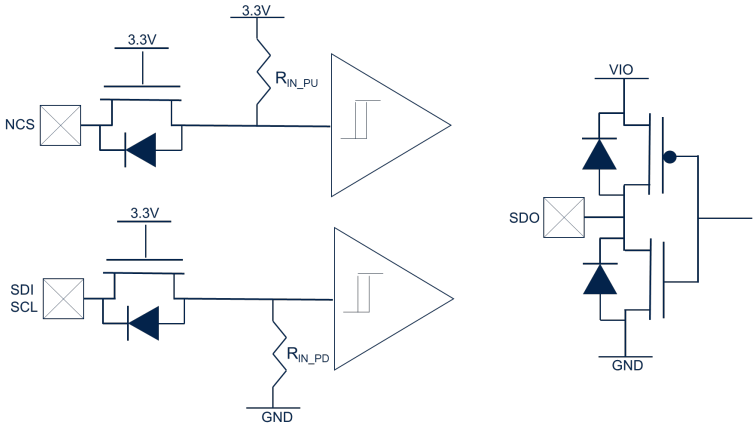
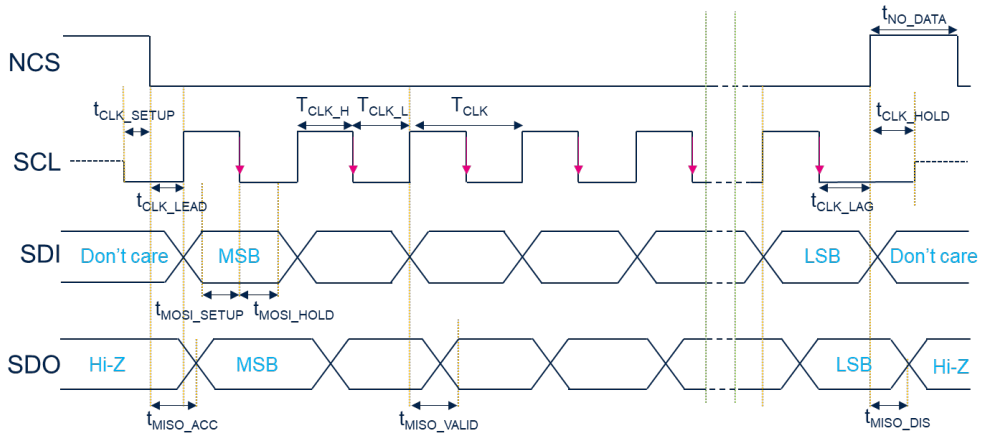


Table 106. SPI target quick look

Parameter	Description
Protocol	Out of frame
Single frame length (NBIT)	40 bit
Frame protection	6 bit CRC
Max. frequency	4 MHz
CPOL	0
CPHA	1

Figure 48. **SPI target timing diagram**



4.14.1.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 107. **SPI target electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
f_{CLK_SPI}	SCL clock frequency (50% duty cycle), $f_{CLK_SPI} = 1/T_{CLK}$	Application info			4	MHz	NCS, SDI, SDO, SCL
T_{CLK_L}	Time interval for SCL = LOW	Application info	120			ns	NCS, SDI, SDO, SCL
T_{CLK_H}	Time interval for SCL = HIGH	Application info	120			ns	NCS, SDI, SDO, SCL
t_{MISO_VALID}	Propagation delay (time passed after propagating SCL rising edge @ SDO active)	C_{LOAD} = 60pF			50	ns	NCS, SDI, SDO, SCL
t_{CLK_LEAD}	Time passed after NCS H/L edge @ first SCL edge	Application info	240			ns	NCS, SDI, SDO, SCL
t_{MOSI_SETUP}	SDI input setup time (time passed after SDI data valid @ sampling SCL falling edge)	Application info	90			ns	NCS, SDI, SDO, SCL
t_{MOSI_HOLD}	SDI input hold time (time passed after propagating SCL falling edge @ SDI data "not valid anymore")	Application info	90			ns	NCS, SDI, SDO, SCL
t_{CLK_SETUP}	Time passed after SCL = LOW before NCS H/L edge	f_{CLK_SPI} = 4 MHz	240			ns	NCS, SDI, SDO, SCL
t_{CLK_LAG}	Time passed after SCL = LOW before NCS L/H edge	f_{CLK_SPI} = 4 MHz	240			ns	NCS, SDI, SDO, SCL
t_{CLK_HOLD}	Time passed after NCS L/H edge with SCL = LOW before SCL = IDLE	f_{CLK_SPI} = 4 MHz	240			ns	NCS, SDI, SDO, SCL
$t_{NO_DATA_MAIN}$	Minimum time for NCS = HIGH when SPI address is in 0x00 - 0x44 range	f_{CLK_SPI} = 4 MHz	2			µs	NCS, SDI, SDO, SCL
$t_{NO_DATA_STBY}$	Minimum time for NCS = HIGH when SPI address is in 0x45 - 0x4A range	f_{CLK_SPI} = 4 MHz	8			µs	NCS, SDI, SDO, SCL
t_{MISO_DIS}	Time passed after NCS L/H edge to SDO = Hi-Z	C_{LOAD} = 60pF			240	µs	NCS, SDI, SDO, SCL
t_{MISO_ACC}	Time passed after NCS H/L edge to SDO active	C_{LOAD} = 60pF			240	µs	NCS, SDI, SDO, SCL

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
V_{NCS_HIGH}	NCS high voltage		2			V	NCS
V_{NCS_HYS}	NCS hysteresis voltage		0.1		0.5	V	NCS
V_{SDI_HIGH}	SDI high voltage		2			V	SDI
V_{SDI_HYS}	SDI hysteresis voltage		0.1		0.5	V	SDI
V_{SCL_HIGH}	SCL high voltage		2			V	SCL
V_{SCL_HYS}	SCL hysteresis voltage		0.1		0.5	V	SCL
R_{IN_PU}	Weak pull-up resistor to 3.3V		0.4	1	1.6	MΩ	NCS
R_{IN_PD}	Weak pull-down resistor		0.4	1	1.6	MΩ	SDI, SCL
V_{SDO_HIGH}	SDO high voltage	I_{SOURCE} = 2mA	V_{VIO}-0.4			V	SDO
V_{SDO_LOW}	SDO low voltage	I_{SINK} = 2mA			0.4	V	SDO

4.14.2 Protocol layer

This section defines the communication protocol layer. The protocol is 40 bits, out of frame.

4.14.2.1 Single read/write

The following table describes the protocol for managing single read/write commands.

All registers of the L9988 can be accessed, in NORMAL state, performing single read/write operations on the SPI target.

In case the received CRC is not correct, the frame will be discarded, the CRC error flag SPI_CRC_ERR will be asserted in the status register COMM_ERR_SPI and, at the next SPI access, an **SPI ERROR** frame will be issued. The **FSO1** and **FSO2** lines will be asserted.

In case a wrong clock cycle number is received before NCS de-assertion, the frame will be discarded, the SDO data will not be reliable, an error flag (SPI_SHORT_FRAME or SPI_LONG_FRAME) will be asserted in the register COMM_ERR_SPI and, at the next access, an **SPI ERROR** will be sent on the SDO. The **FSO1** and **FSO2** lines will be asserted. The SPI_LONG_FRAME error will not be set in case the received number of clock cycles is multiple of 40 (NBIT) to be compatible with BURST Read.

In case the MCU tries to address a non-existent register, the SPI_WRONG_ADD flag is asserted in the register COMM_ERR_SPI and an **SPI ERROR** frame will be sent at the next SPI access. The **FSO1** and **FSO2** lines will be asserted.

In case the MCU sends a frame with a wrong frame counter, the frame will be discarded, the SPI_FRM_CNT_ERR flag will be asserted in the register COMM_ERR_SPI and an **SPI ERROR** frame will be sent as a response to the next SPI access. The **FSO1** and **FSO2** lines will be asserted.

Table 108. Single read/write frame format

	39	38 37 36 35 34 33 32	31 30 29 28	27	26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5 4 3 2 1 0
MOSI	R/W	Address	RSVD	Frame counter	Reserved	DATA WRITE	CRC
MISO	SPIERR	Address feedback	IERR	Frame counter	Reserved	DATA READ	CRC

In the following table, all fields of the MISO/MOSI frame are described.

Table 109. Read/write frame fields

Field	Size [bit]	Description	Value
R/W	1	Used to distinguish between read/write operations	0 = Read 1 = Write
SPIERR	1	Used to signal an incorrect frame	0 = No Error 1 = Error in the previous frame
Address / Address feedback	7	Identifies the register address for the read/write operation. Used also for burst commands.	[0-127]
RSVD	4	Reserved for MOSI	0
IERR[3:0]	4	IERR[3]: Fault interrupt IERR[2]: Latch interrupt IERR[1]: Fail Safe Output 1 IERR[0]: Fail Safe Output 2	
Frame counter	1	Toggles at each frame	
Reserved	1	Reserved bit for MOSI and MISO	0
DATA WRITE	20	Specifies the register content to be written in write operations. Don't care in read operations	Read: X Write: [0 to 2^{20}-1]
DATA READ	20	Returns the register content in both read/write operations	[0 to 2^{20}-1]
CRC	6	Checksum sized for high coverage (hamming distance ≥ 3)	[0-63]

The **SPI ERROR** frame, issued on MISO after a wrong frame, is composed by SPIERR =1, address feedback corresponding to 0x7F and DATA READ storing the details of errors.

Table 110. SPI ERROR frame

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	SPIERR	Address feedback 0x7F						IERR				Frame counter	Reserved	0x00															SPI_SHORT_FRAME	SPI_LONG_FRAME	SPI_WRONG_ADD	SPI_FRM_CNT_ERR	SPI_CRC_ERR	CRC						

4.14.2.2 *Burst read*

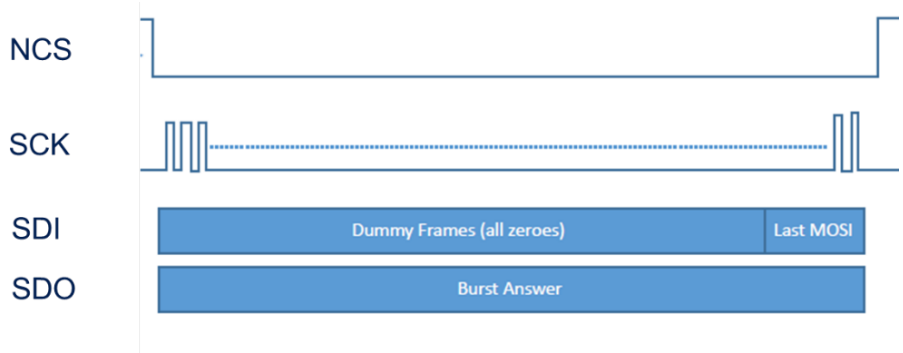
The SPI burst access can be used to reduce the time needed to readout long data series of consecutive addresses inside the range from 0x00 to 0x44.

This access is achieved by the MCU asserting the NCS and sending **N*NBIT** clock cycles on SCL, where N is the number of burst frames to be read from the L9988. Each NBIT MISO frame is a complete SPI frame as described in Table 102 and Table 103, starting with the first ADDRESS FEEDBACK requested in the previous frame. The successive frames will contain the ADDRESS FEEDBACK + 1 register and so forth.

First (N-1) * NBIT MOSI frames are dummy 0 frames, while the last NBIT frame is considered a single read/write access as described in Section 4.14.2.1. Since the protocol is out-of-frame, the feedback at this last MOSI frame will be sent at the next SPI access.

In case a wrong number of clock cycles is sent by the MCU, the last frame will be not reliable, and the pointed register will be lost. At the next access to the SPI target, an **SPI ERROR** frame will be sent, and an error flag (SPI_SHORT_FRAME or SPI_LONG_FRAME) will be asserted in the status register COMM_ERR_SPI.

Figure 49. **SPI burst read**



Note: In case there is an SPI error frame before a burst read command, then all the burst answers will contain info about the previously detected fault.

4.14.2.3 *CRC*

In case of single read/write access, the SPI frame is equipped with a 6-bit CRC code to guarantee information integrity. Corrupted frames received will be discarded, the SPI_CRC_ERR error flag will be set and, at the next SPI access, an **SPI ERROR** frame will be issued. The **FSO1** and **FSO2** lines will be asserted in case SPI_CRC_ERR is set.

Table 111. **SPI target CRC calculation information**

Parameter	Value
Length	6 bit
Polynomial	$x^6 + x^5 + x^2 + x + 1$
Seed	0x38

During burst communication, the CRC is generated for each single NBIT frame on MISO, while a single CRC is expected on the MOSI frame for the last NBIT frame.

4.14.2.4 *Frame counter*

In case of single read/write access, the frame counter bit toggles at each SPI frame, starting from 0, to allow frame loss detection on both the sender and receiver side.

The MCU must send a frame counter bit coherent with the expected frame counter of the device; otherwise the frame will be discarded, the SPI_FRM_CNT_ERR error flag will be set, and a **SPI ERROR** frame will be sent on the next SPI access. The **FSO1** and **FSO2** lines will be asserted in case SPI_FRM_CNT_ERR is set.

The frame counter bit is available on the MISO frame, to be checked at the MCU side with respect to the MCU internal frame counter.

During burst access, the frame counter is provided by the MCU for the last NBIT frame. For the MISO frame, the same internal frame counter is sent for each single NBIT frame, valid for the entire burst read access.

4.15 Configuration lock

To prevent inadvertent modification of Safety Relevant Registers (SRR) and Safety Latent Registers (SLR) (highlighted with this color code in the register map), such register map sectors are protected by a lock field.

By default, SRR/SLR registers are locked. To configure the device, the following procedure shall be implemented:

Procedure 7 - configuration lock/unlock

1. The MCU writes 0x55 in the write-only field SPECIAL_KEY in the SPECIAL_REG register to enter in partial unlock.
2. The MCU writes 0x33 in the write-only field SPECIAL_KEY in the SPECIAL_REG register to confirm the unlock.
3. The MCU changes any configuration register within $T_{CFG_TIMEOUT}$
4. The MCU re-applies the lock by writing 0xAA in the write-only field SPECIAL_KEY in the SPECIAL_REG register
   – If the $T_{CFG_TIMEOUT}$ expires, the lock is automatically re-applied.

Trying to write a protected register (SRR or SLR) without unlocking it will result in data being discarded.

*Note: Writing lock-protected registers only alters the current configuration loaded in the SPI registers. To save the configuration and guarantee a correct reload at each power up, the update must be pushed into the **Non Volatile Memory (NVM)** as described in the dedicated section.*

*Note: For temporary modifications to the IC configuration, which do not need to be pushed in the **Non Volatile Memory (NVM)**, it is recommended to disable the **Configuration Register Data Integrity Check (CONF_CRC)**.*

4.15.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 112. Configuration timeout

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	UNIT
$T_{CFG_TIMEOUT}$	Configuration lock timeout			2		s

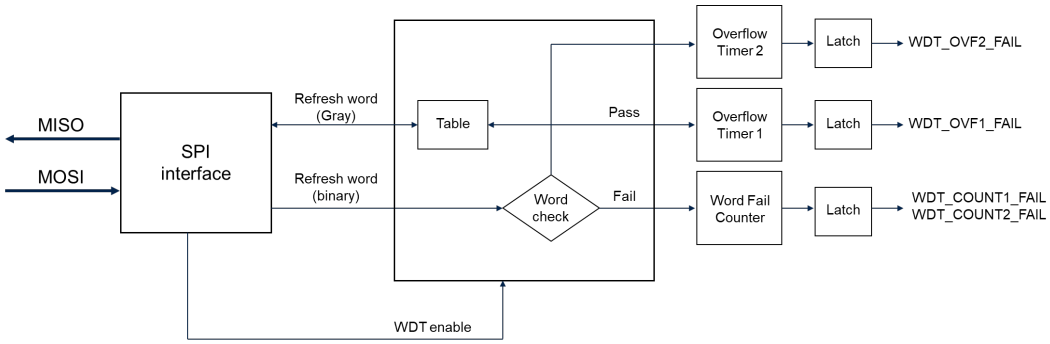
4.16 Watchdog and MCU monitor

The L9988 offers a 2-level watchdog control approach. The first control level is given by means of a **query & answer watchdog (WD1)**. The second control level monitors the PRN input pin to assert the proper frequency and is delivered by the MCU **(WD2-PRN)**.

4.16.1 Q&A watchdog (WD1)

The L9988 implements a Q&A watchdog via SPI to verify MCU activity and monitor its computational integrity.

Figure 50. Watchdog timer simplified block diagram



The Watchdog Timer (WDT, named WD1) is disabled by default, and the MCU must write the NVM bit WD1_AUTO_EN and perform an NVM upload to enable the WD1 feature.

The NVM bit WD1_AUTO_EN can be written by the MCU once the device programming operation is completed to enable the WD1 functions:

- If WD1_AUTO_EN = 0 (default), the WD1 is disabled
- If WD1_AUTO_EN = 1, the WD1 works according to the WDT_EN register.

With this bit, after the first power up of the device, the WD1 will not be enabled by default, so the MCU can be configured with no time limit. At the end of the programming phase, the MCU must set the WD1_AUTO_EN bit to “1” and run an NVM upload. Then, the WD1 will be enabled according to the WDT_EN register.

For safety reasons, in case of a CRC error during NVM download, the WD1_AUTO_EN bit will be set to “0” but WD1 will be enabled according to the WDT_EN register.

Once enabled, the first refresh command should be received by the SPI before the long window timeout t_{WDT_LONG} expires. All WDT configuration registers must be set during the long window. If the watchdog timer is waiting for a refresh pulse inside the long window, the WDT_LONG_WNDW_ACTIVE bit in WDT_STATUS register is set to 1, otherwise it is set to 0.

If the first refresh command is not received before the long window timeout, the error flag WDT_LONG_FAIL in WDT_STATUS register is set, the **FAULT** and **RST1** pins are asserted and the WD_RST_CNT error counter is incremented. The WD_RST_CNT value is readable by SPI through the WD_RST_CNT_STATUS field in WDT_STATUS_2 register.

The WD_RST_CNT has a maximum value, set in the WD_RST_CNT_MAX field in the WDT_CFG register (default value 31), above which the **WD_RESET_LATCH** is set at 1 and the device enters POWER DOWN state. The WD_RST_CNT is reset in SLEEP state. The WD_RESET_LATCH is reset in POWER DOWN state when **IGN** is **LOW** (in detail, when $V_{IGN} < V_{IGN_HIGH} - V_{IGN_HYS}$ for an interval longer than T_{IGN_FIL}) to reach SLEEP state.

During the long window timeout t_{WDT_LONG}, it is possible to disable the WDT by writing WDT_EN = 0.

Reprogramming of WD1 configuration is possible not only during the first long window, but also while WDT is disabled (WDT_EN = 0 in WDT_EN register). This is useful when the software of the MCU needs to be updated and the watchdog cannot be refreshed in the required times.

Table 113. Watchdog enable bit

WDT_EN	WD1_AUTO_EN	Description
0	0	Watchdog disabled

WDT_EN	WD1_AUTO_EN	Description
1	0	Watchdog disabled (default)
0	1	Watchdog disabled
1	1	Watchdog enabled

Once disabled, it is possible to re-enable the WDT by writing WDT_EN=1 and starting the refresh sequence with the long window timeout.

Once disabled, WDT_EN can be reset at its default if RST1 is asserted.

The activation status of WDT is also stored in the WDT_ON_STATUS bit of the SPI read-only register WDT_STATUS: if equal to 0, WDT is not active; if equal to 1, WDT is active.

As soon as the first expected refresh command is received, the overflow counter is started, thus defining the refresh window T_{WDT_OVF1} and T_{WDT_OVF2}, with accuracy WDT_OVF_ACC, whose length is defined by the WDT_OVF_CFG bit field of WDT_CFG register.

Table 114. Watchdog configuration table for WDT overflow counter

WDT_OVF_CFG	WDT_OVF LSB	T_{WDT_OVF1}typ	T_{WDT_OVF2} typ
00	0.256ms	11.3ms	22.5ms
01	0.512ms (default)	22.5ms (default)	45.0ms(default)
10	1.024ms	45.0ms	90.1ms
11	2.048ms	90.1ms	180.2 ms

The WDT overflow counter status can be accessed through the dedicated WDT_OVF_STATUS bit fields in the WDT_STATUS_2 read-only register. The WDT_OVF timer value in seconds can be retrieved by the following reconstruction formula:

$$T_{WDT_OVF_STATUS} = D_{WDT_OVF_STATUS} * \Delta_{WDT_OVF_LSB} \quad (8)$$

where DWDT_OVF_STATUS is the digital word stored in the WDT_OVF_STATUS bit field and ΔWDT_OVF_LSB is the correspondent counter LSB as defined by the WDT_OVF_CFG bit field.

Example

DWDT_OVF_STATUS = 110010 (binary) → 50 (decimal)

WDT_OVF_CFG = 10 → LSB = 1.024ms

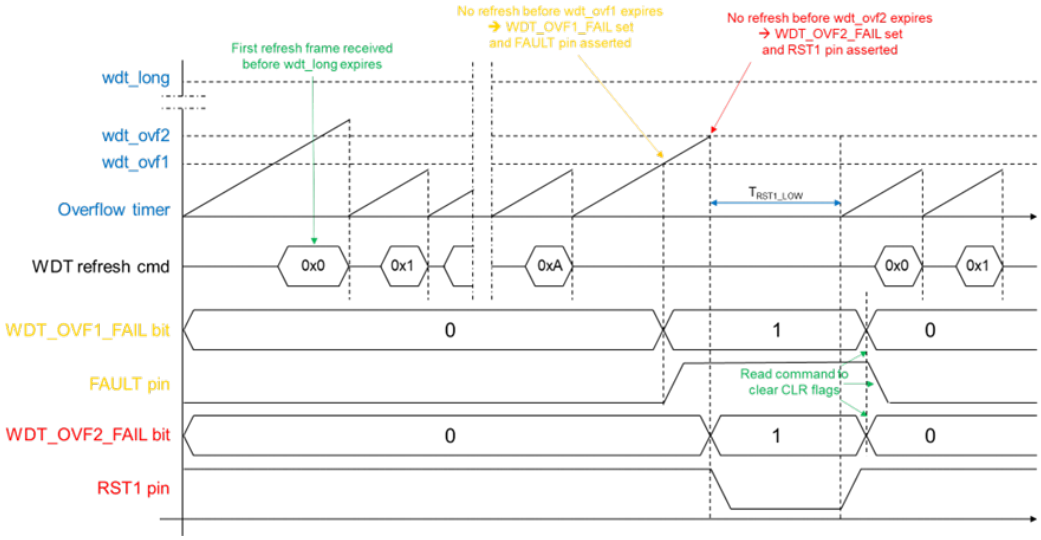
Watchdog overflow counter status: TWDT_OVF_STATUS = 50 * 1.024ms = 51.2ms

Within this window, the watchdog expects a refresh pulse to reset the overflow counter and restart a new window.

If the refresh is missed before the overflow counter of Timeout 1 T_{WDT_OVF1} has elapsed, the error flag WDT_OVF1_FAIL in WDT_STATUS register is set, and the **FAULT** pin is asserted.

If the refresh is missed also when the overflow counter of Timeout 2 T_{WDT_OVF2} has elapsed, the error flag WDT_OVF2_FAIL in the WDT_STATUS register is set, the **RST1** pin is managed to reset the MCU, the WD reset counter (WD_RST_CNT) is incremented, and the timer restarts waiting for a refresh command received by the SPI before the long window timeout t_{WDT_LONG} expires.

Figure 51. **WDT operation – overflow counter failure**



The auto-retry procedure is activated by managing the **RST1** pin. If WD_RST_CNT reaches WD_RST_CNT_MAX, the bit **WD_RESET_LATCH** is set, the **RST1** pin is asserted, and the device moves to POWER DOWN state.

The refresh of the overflow counter must be performed by the MCU through a dedicated SPI frame including the 4-bit watchdog refresh command WDT_BINARY_CODE in the WDT_CMD register.

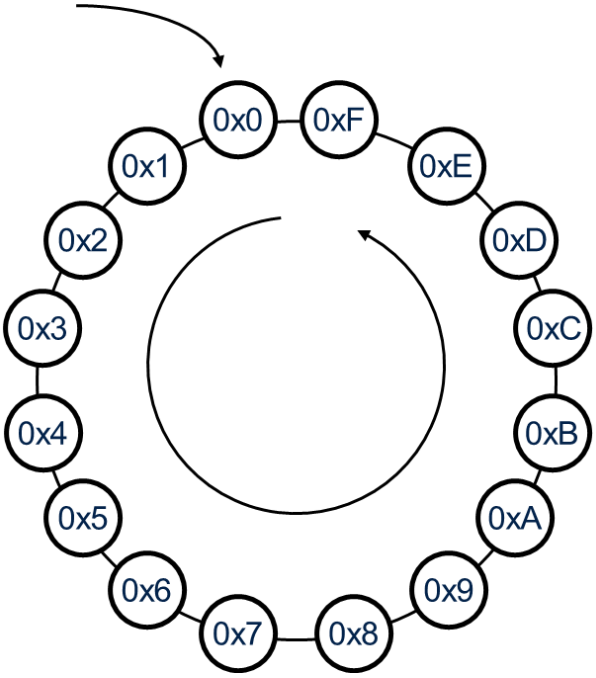
The watchdog circuitry compares the received watchdog refresh command with an internal Look-Up Table (LUT) and answers with a corresponding 4-bit gray code (WDT_GRAY_CODE in WDT_CMD register) in the next frame.

Table 115. **Watchdog Binary to Gray answer conversion**

Binary → Gray	Binary → Gray	Binary → Gray	Binary → Gray
0x0 (0000) → 0x0 (0000)	0x4 (0100) → 0x6 (0110)	0x8 (1000) → 0xC (1100)	0xC (1100) → 0xA (1010)
0x1 (0001) → 0x1 (0001)	0x5 (0101) → 0x7 (0111)	0x9 (1001) → 0xD (1101)	0xD (1101) → 0xB (1011)
0x2 (0010) → 0x3 (0011)	0x6 (0110) → 0x5 (0101)	0xA (1010) → 0xF (1111)	0xE (1110) → 0x9 (1001)
0x3 (0011) → 0x2 (0010)	0x7 (0111) → 0x4 (0100)	0xB (1011) → 0xE (1110)	0xF (1111) → 0x8 (1000)

The expected watchdog command order starts with number 0x0 (0b0000) and is incremented by 1 at each refresh window if the command is correctly interpreted and no failure is detected. Once command number 0xF (0b1111) is reached, the sequence restarts with number 0x0 (0b0000), as shown in the following figure. The expected watchdog command for the next frame is available in the WDT_EXP_BINARY_CODE field in the WDT_CMD register, to have a recovery mode in case of sequence mismatch.

Figure 52. **Watchdog command order sequence**



In case of a wrong WDT data command (command different from the expected sequence order), the watchdog word fail counter WDT_FAIL_COUNT is incremented by 1. With the next valid watchdog data command, the fail counter is decreased by 1.

If the WDT_FAIL_COUNT counter reaches the failure limit defined in WDT_COUNT_FAIL_1 according to the WDT_WRONG_CMD_CFG field in the WDT_CFG register, the watchdog fail flag WDT_DATA1_FAIL in the WDT_STATUS register is set and the **FAULT** pin is asserted.

If the WDT_FAIL_COUNT reaches the failure limit defined in WDT_COUNT_FAIL_2 according to the WDT_WRONG_CMD_CFG field in the WDT_CFG register, the watchdog fail flag WDT_DATA2_FAIL in the WDT_STATUS register is set, the **RST1** pin is asserted and the WD_RST_CNT is incremented.

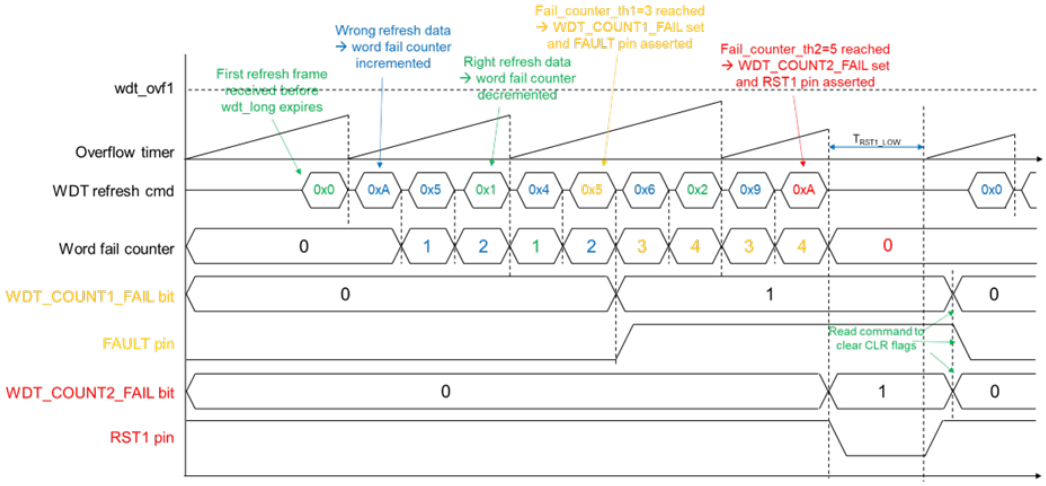
The failure counter limit can be programmed as shown in the following table.

Table 116. **Watchdog configuration table for WDT data fail counter**

WDT_WRONG_CMD_CFG	WDT_COUNT_FAIL_1	WDT_COUNT_FAIL_2
00 (default)	1 (default)	3 (default)
01	2	4
10	3	5
11	4	6

The information about the number of encountered WDT data failures is stored in the dedicated WDT_FAIL_COUNT_STATUS field of the WDT_STATUS_2 register.

Figure 53. **WDT operation – Word sequence failure**



4.16.1.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 117. **Q&A watchdog electrical parameters**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{WDT_LONG}	Initial long window			500		ms
WDT_OVF_ACC	T_{WDT_OVFx} accuracy		-10		+10	%

4.16.2 Second watchdog (WD2 - PRN)

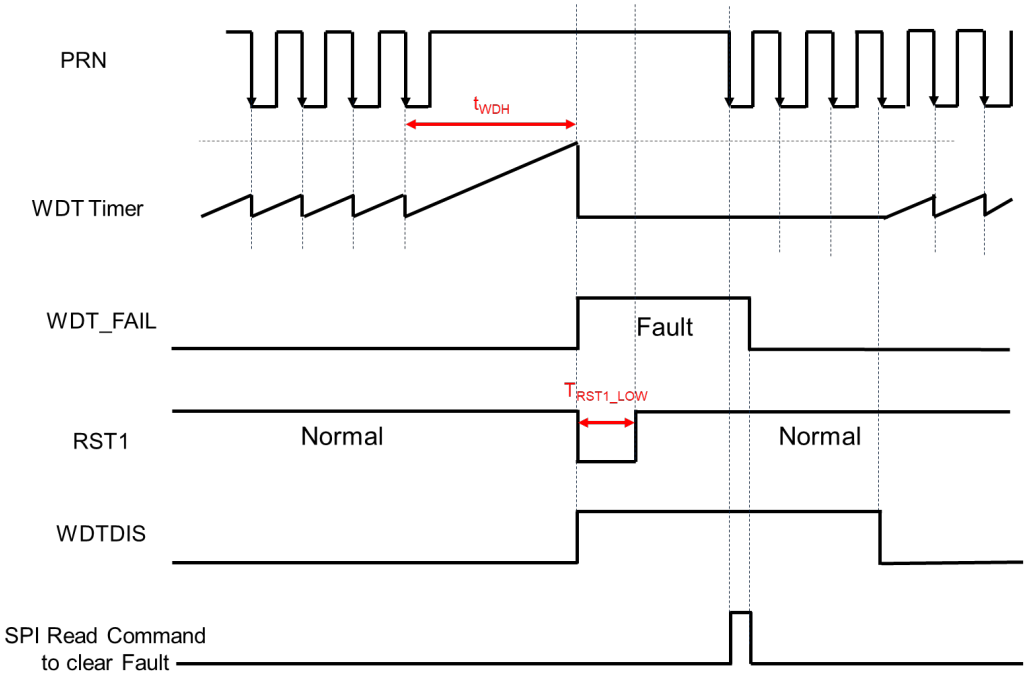
When the second watchdog is activated by the MCU with WDTDIS = 0, the MCU starts to refresh the watchdog service through the PRN pin.

The status of the WDTDIS pin filtered is available via SPI by reading the bit WDTDIS_ECHO (in NORMAL MODE).

The watchdog logic detects only the falling edge of the WDT signal coming on the PRN pin.

The status of the PRN pin filtered is available via SPI by reading the bit PRN_ECHO (in NORMAL MODE). A WDT fault is generated when the WDT signal stops for more than t_{WDH}.

Figure 54. **Second watchdog operation**



As a reaction to a WDT fault, the following events occur:

- **RST1** is asserted to reset the MCU and the WDT timer is reset
- WD_RST_CNT is incremented
- The error flag WDT_FAIL is set to be cleared by the MCU after RST1 release.
- The WDT timer restarts if WDTDIS is LOW

If WD_RST_CNT reaches WD_RST_CNT_MAX, the bit **WD_RESET_LATCH** is set, the **RST1** pin is asserted, and the device moves to POWER DOWN state. The WD_RESET_LATCH is reset in POWER DOWN state when IGN is LOW to reach SLEEP MODE. When the WDTDIS = 1, the WD2 is disabled. The WDTDIS implements a passive pull-down to ensure the voltage level does not interrupt the WDT control in case of open connection.

The watchdog is reset in case RST1 is asserted.

4.16.2.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 118. **Second watchdog electrical parameters**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
t_{WDH}	Window timeout for watchdog refresh			250		ms	PRN
V_{PRN_HIGH}	PRN high voltage		2			V	PRN
V_{PRN_HYS}	PRN hysteresis voltage		0.1		0.5	V	PRN
T_{PRN_FIL}	PRN filter time		1.5	2	2.5	µs	PRN
R_{PRN_PD}	PRN pull-down resistor		0.4	1	1.6	MΩ	PRN
V_{WDTDIS_HIGH}	WDTDIS high voltage		2			V	WDTDIS
V_{WDTDIS_HYS}	WDTDIS hysteresis voltage		0.1		0.5	V	WDTDIS
T_{WDTDIS_FIL}	WDTDIS filter time		1.5	2	2.5	µs	WDTDIS
R_{WDTDIS_PD}	WDTDIS pull-down resistor		0.4	1	1.6	MΩ	WDTDIS

4.16.3 RST1 LATCH timeout

The L9988 implements an internal timeout able to detect:

1. In NORMAL MODE, an unexpected RST1 assertion (e.g. persistent VCORE undervoltage) longer than $T_{RST1_LATCH_TIMEOUT}$
2. In STANDBY MODE, the missing end of the cyclic wakeup routine (triggered each $T_{CYCLE_STANDBY}$) in a time longer than $T_{RST1_LATCH_TIMEOUT}$

In these scenarios, the bit **WD_RESET_LATCH** is set, and the device moves to POWER DOWN state. If in STANDBY MODE, the device reaches this state by first moving to NORMAL MODE.

The WD_RESET_LATCH is reset when IGN is LOW to reach SLEEP MODE.

4.16.3.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 119. RST1 LATCH timeout electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$T_{RST1_LATCH_TIMEOUT}$	Internal timeout for WD_RESET_LATCH assertion		12.5	15	17.5	s	RST1

4.17 Non Volatile Memory (NVM)

The IC allows saving key configuration parameters in the internal NVM. Refer to the register map file attached. All registers marked with this color code throughout the document identify configuration registers stored in the NVM.

4.17.1 NVM read/write operations

NVM data is automatically downloaded into local registers every time the IC performs the transition SLEEP to NORMAL:

As the IC reaches NORMAL state, the following commands allow user interaction with the NVM:

- NVM_OP_CMD=0x3 triggers the NVM upload and download: this operation fetches the data previously written into configuration registers and writes it to the relative NVM sectors, then it automatically triggers a full NVM re-download in order to guarantee whole data consistency. The operation lasts T_{NVM_UPLOAD} and during this time interval the MCU will not be able to perform R/W operations (any command will be discarded)
- NVM_OP_CMD=0x5 triggers the NVM download, fetching the data from NVM sectors and writing it to the configuration registers. The operation lasts $T_{NVM_DOWNLOAD}$ and during this time interval the MCU will not be able to perform R/W operations (any command will be discarded)

During NVM upload/download operations, NVM_READY flag is reset to ‘0’, indicating that the NVM is busy. Once the task is complete, the NVM_READY is set high; as no NVM read/write operation is running, the NVM circuit is kept under reset.

In order to guarantee data retention, the NVM write operation number must not exceed $N_{NVM_WRITE_CYCLES}$; if this limit is exceeded, data retention is not guaranteed. By the way, the IC will continue to accept and perform every write operation, even if it is beyond the $N_{NVM_WRITE_CYCLES}$ count. Every time a write operation is performed, the IC automatically updates the NVM_UPLOAD_COUNT counter field, which is stored in the NVM as well. The counter value is user-accessible, reading the NVM_UPLOAD_COUNT bit (read-only). The counter value saturates at $N_{NVM_WRITE_CYCLES}$: if a new write operation is done above the $N_{NVM_WRITE_CYCLES}$ limit, the counter value is increased at $N_{NVM_WRITE_CYCLES}$+1 and will never be updated anymore.

4.17.2 NVM data integrity checks

NVM content can be categorized into two main groups: trimming data and configuration data (used to configure IC operation). All this data is organized into sectors, each of them individually protected by CRC. Trimming data and configuration data do not share the same sectors.

Every time the IC performs an NVM download operation (either automatic or user-driven), an integrity check against the NVM CRC (sector by sector) is performed as well. In case of check failure, the following actions are performed:

- The CRC check failing sector data is not downloaded into the local registers. This data is replaced by all zeros. It is possible to mask this replacement by setting the NVM_CRC_FAIL_MSK bit before a download. Hence, depending on the sector content, either function accuracy will not be guaranteed, or the IC expected configuration will not be applied.
- In case at least one of the trimming sectors has failed the CRC check, TRIM_NVM_CRC_FAIL latch is set (clear-upon-read). This bit is set to 0 if NVM_CRC_FAIL_MSK = 1 before a download
- In case at least one of the IC configurations sectors has failed the CRC check, CONF_NVM_CRC_FAIL latch is set (clear-upon-read). This bit is set to 0 if NVM_CRC_FAIL_MSK = 1 before a download
- No other action is taken, i.e., no interruption/inhibition of IC functionalities.

Every time the user triggers an NVM upload and download operation, the corresponding sector CRC is updated as well; this is done by the IC automatically.

Once an NVM upload command is issued, the NVM_VERIFY_ERR flag is asserted in case of upload procedure fails. The assertion of this flag will inhibit the automatic download of the NVM content. If the MCU issues a specific download NVM command, it will be executed despite the assertion of the NVM_VERIFY_ERR.

4.17.2.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 120. NVM electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
$N_{NVM_WRITE_CYCLES}$	Number of allowed NVM write cycles to guarantee data retention	Guaranteed by SCAN			30	cycles	-
$N_{NVM_SECTORS}$	Number of NVM sectors			17		sectors	-
$NVM_{CAPACITY}$	Capacity of NVM			4352		bit	-
T_{NVM_UPLOAD}	NVM user sector upload time duration	Guaranteed by SCAN			25	ms	-
$T_{NVM_DOWNLOAD}$	NVM full download time duration	Guaranteed by SCAN			2.5	ms	-
T_{CONFIG}	Time required to turn on the entire internal power supply and to download the first four sectors of NVM in SLEEP to NORMAL MODE transition			1024		µs	-
T_{NVM_TRIM}	NVM first sector download time duration in SLEEP to NORMAL MODE transition			128		µs	-

4.17.3 Configuration register data integrity check (CONF_CRC)

In order to guarantee the integrity over time of NVM downloaded key trimming and configuration data, both safety relevant and latent register content (highlighted with this color code in the register map) is automatically and cyclically checked against corruption in NORMAL MODE: this is possible because local register data is provided with a CRC signature, which can be checked periodically (with period T_{CONF_CRC}) when no operation is performed on the NVM, i.e. the NVM circuit is in reset state.

In case of check failure, the following actions are performed:

- In case trimming data has failed the CRC signature check, TRIM_CYC_CRC_FAIL latch is set (clear-upon-read)
- In case IC configuration data has failed the CRC signature check, CONF_CYC_CRC_FAIL latch is set (clear-upon-read)
- No other action is taken, i.e., no interruption/inhibition of IC functionalities.
- In case of permanent data corruption, failure latch set pulse occurs every T_{CONF_CRC}

The user can decide to completely disable this integrity check by setting CYC_CRC_DIS to 1; after the feature has been disabled, it is still possible to clear-upon-read both CYC_TRIM _CRC_FAIL and CYC_CFG_CRC_FAIL.

The local register CRC signature is managed in the following way:

- Every time NVM data is downloaded into local registers (either automatic or user-driven), a CRC signature is refreshed as well.
- Every time the user changes the local register data, the corresponding CRC signature is not automatically updated, thus a CRC check failure is expected at the next execution cycle; by the way, as the user triggers the NVM upload and refresh operation, after the NVM sector CRC has been automatically updated, the local register CRC signature is updated accordingly, and no further CRC check failure is expected. In order to mask the systematic CRC check failure explained just before, the user can use the CYC_CRC_DIS feature; however, the systematic failure scenario can be used as a fault-injection test.

A CRC check is also performed during cyclic activation in STANDBY MODE and in case of CRC error the device will move to NORMAL MODE and the FAULT pin is asserted.

4.17.3.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 121. Configuration integrity check characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	PIN
T_{CONF_CRC}	Configuration integrity check period				90	ms	-

4.17.4 NVM fault internal upload during POWER DOWN state

In case the POWER DOWN state is reached because of persistent watchdog fails (WD_RESET_LATCH = 1), the device will upload to the NVM a copy of all the information about faults related to MCU failure reported in the Fault flag column below.

Uploaded fault information will be downloaded during SLEEP to NORMAL transition and can be read by SPI accessing read-only flags with the “_PDN_NVM” suffix.

Table 122. List of uploaded fault

Fault type	Fault flag	NVM flag (SPI READ ONLY)
VBST Undervoltage	VBST_UV	VBST_UV_PDN_NVM
VBST Overvoltage	VBST_OV	VBST_OV_PDN_NVM
VBST Overcurrent	VBST_OVC	VBST_OVC_PDN_NVM
CP Undervoltage	VCP_UV	VCP_UV_PDN_NVM
CP Overvoltage	VCP_OV	VCP_OV_PDN_NVM
VPRE Overvoltage	VPRE_OV	VPRE_OV_PDN_NVM
VPRE Undervoltage	VPRE_UV	VPRE_UV_PDN_NVM
VPRE Overtemperature	VPRE_OT	VPRE_OT_PDN_NVM
VCORE Overvoltage	VCORE_OV	VCORE_OV_PDN_NVM
VCORE Undervoltage	VCORE_UV	VCORE_UV_PDN_NVM
VCORE Deep Undervoltage	VCORE_DEEP_UV	VCORE_DEEP_UV_PDN_NVM
VCORE Overtemperature	VCORE_OT	VCORE_OT_PDN_NVM
VCC Undervoltage	VCC_UV	VCC_UV_PDN_NVM
VCC Overvoltage	VCC_OV	VCC_OV_PDN_NVM
VCC Overtemperature	VCC_OT	VCC_OT_PDN_NVM
VCC CAN Undervoltage	VCC_CAN_UV	VCC_CAN_UV_PDN_NVM
VCC CAN Overvoltage	VCC_CAN_OV	VCC_CAN_OV_PDN_NVM
VCC CAN Overtemperature	VCC_CAN_OT	VCC_CAN_OT_PDN_NVM
VTREF Undervoltage	VTREF_UV	VTREF_UV_PDN_NVM

Fault type	Fault flag	NVM flag (SPI READ ONLY)
VTREF Overvoltage	VTREF_OV	VTREF_OV_PDN_NVM
VTREF Overtemperature	VTREF_OT	VTREF_OT_PDN_NVM
VSTBY Undervoltage	VSTBY_UV	VSTBY_UV_PDN_NVM
VSTBY Overvoltage	VSTBY_OV	VSTBY_OV_PDN_NVM
VSTBY Overtemperature	VSTBY_OT	VSTBY_OT_PDN_NVM
Internal Analog LDO OV	VANA_OV	VANA_OV_PDN_NVM
Internal Analog LDO UV	VANA_UV	VANA_UV_PDN_NVM
Internal Analog LDO OT	VANA_OT	VANA_OT_PDN_NVM
Number of NVM Upload performed	NVM_UPLOAD_COUNT	NVM_UPLOAD_COUNT_PDN_NVM
FSO1 Fail Safe Output 1	FSO1_ECHO	FSO1_ECHO_PDN_NVM
FSO0 Fail Safe Output 0	FSO2_ECHO	FSO2_ECHO_PDN_NVM
RTC Wakeup Fault	RTCWUP	RTCWUP_PDN_NVM
SPI Fault	COMM_ERR_SPI	COMM_ERR_SPI_PDN_NVM
Watchdog Fault	WD_RESET_LATCH	WD_RESET_LATCH_PDN_NVM
Watchdog Fault	WDT_OVF1_FAIL	WDT_OVF1_FAIL_PDN_NVM
Watchdog Fault	WDT_OVF2_FAIL	WDT_OVF2_FAIL_PDN_NVM
Watchdog Fault	WDT_COUNT_FAIL_1	WDT_COUNT_FAIL_1_PDN_NVM
Watchdog Fault	WDT_COUNT_FAIL_2	WDT_COUNT_FAIL_2_PDN_NVM
Watchdog Fault	WDT_FAIL	WDT_FAIL_PDN_NVM
FCCU Fault	FCCU_FAIL	FCCU_FAIL_PDN_NVM

4.18 Die temperature monitor (T_J)

The L9988 monitors the junction temperature with two ADCs and a sensor placed close to the ADC stage to feed the calibration algorithm.

The junction temperature measurements are stored in the TEMP_ADC0_DATA and the TEMP_ADC1_DATA registers and can be computed according to the following formula: Code*0.10887-89.988.

TEMP_ADC0_DATA= 0.10887* (12-bit TEMP_ADC0 register CODE converted in decimal value) -89.988, in which

12-bit TEMP_ADC0 register CODE = 0x44E = 1102

Therefore, TEMP_ADC0_DATA = 0.10887*(1102)-89.988 = 29.98°C

TEMP_ADC1_DATA= 0.10887* (12-bit TEMP_ADC1 register CODE converted in decimal value) -89.988, in which

12-bit TEMP_ADC1 register CODE = 0x441 = 1089

Therefore, TEMP_ADC1_DATA = 0.10887*(1089)-89.988 = 28.57°C

4.18.1 Diagnostics

Table 123. Die temperature monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Thermal Warning	• If T_J rises above $T_{J_WARN_TH}$ the TJ_WARN fault is acknowledged	• The TJ_WARN flag is set	• If T_J falls below $T_{J_WARN_TH}$ - $T_{J_WARN_HYS}$, the TJ_WARN flag can be cleared by MCU	• None	• Non maskable
Thermal Shutdown	• If T_J rises above $T_{J_SD_TH}$ the TJ_SD fault is acknowledged	• The TJ_SD flag is set • The IC moves to POWER DOWN state	• If T_J falls below $T_{J_SD_TH}$ - $T_{J_SD_HYS}$, the TJ_SD flag can be cleared by MCU	• None	• Non maskable

4.18.2 Temperature ADC cross-check

The two ADCs used for temperature calibration are continuously x-checking each other while in NORMAL and STANDBY MODE states (during CYCLIC ACTIVATION) to ensure calibration algorithm integrity. In case a mismatch is detected, the XCHECK_TEMP_FAIL latch is set.

To prevent latent failures affecting the detection, it is possible to perform a fault injection, by programming XCHECK_TEMP_FAULT_INJ = 1 and verifying that XCHECK_TEMP_FAIL is set. After that, the fault injection can be stopped programming XCHECK_TEMP_FAULT_INJ = 0 and verifying that XCHECK_TEMP_FAIL is clearable on read.

4.18.3 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: all supplies according to the operating range in Table 2; T_J according to the operating range in Table 5.

Table 124. Die temperature monitor electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{J_ERR}	Die Temperature Total Conversion Error		-10		10	°C
$T_{J_SD_TH}$	Thermal shutdown threshold		180	190	200	°C
$T_{J_SD_HYS}$	Thermal shutdown threshold hysteresis		5	6	7	°C
$T_{J_WARN_TH}$	Thermal warning threshold	Guaranteed by SCAN	150	165	180	°C
$T_{J_WARN_HYS}$	Thermal warning threshold hysteresis	Guaranteed by SCAN		10		°C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{XCHECK_TEMP_TH}$	Thermal x-check threshold			20		°C

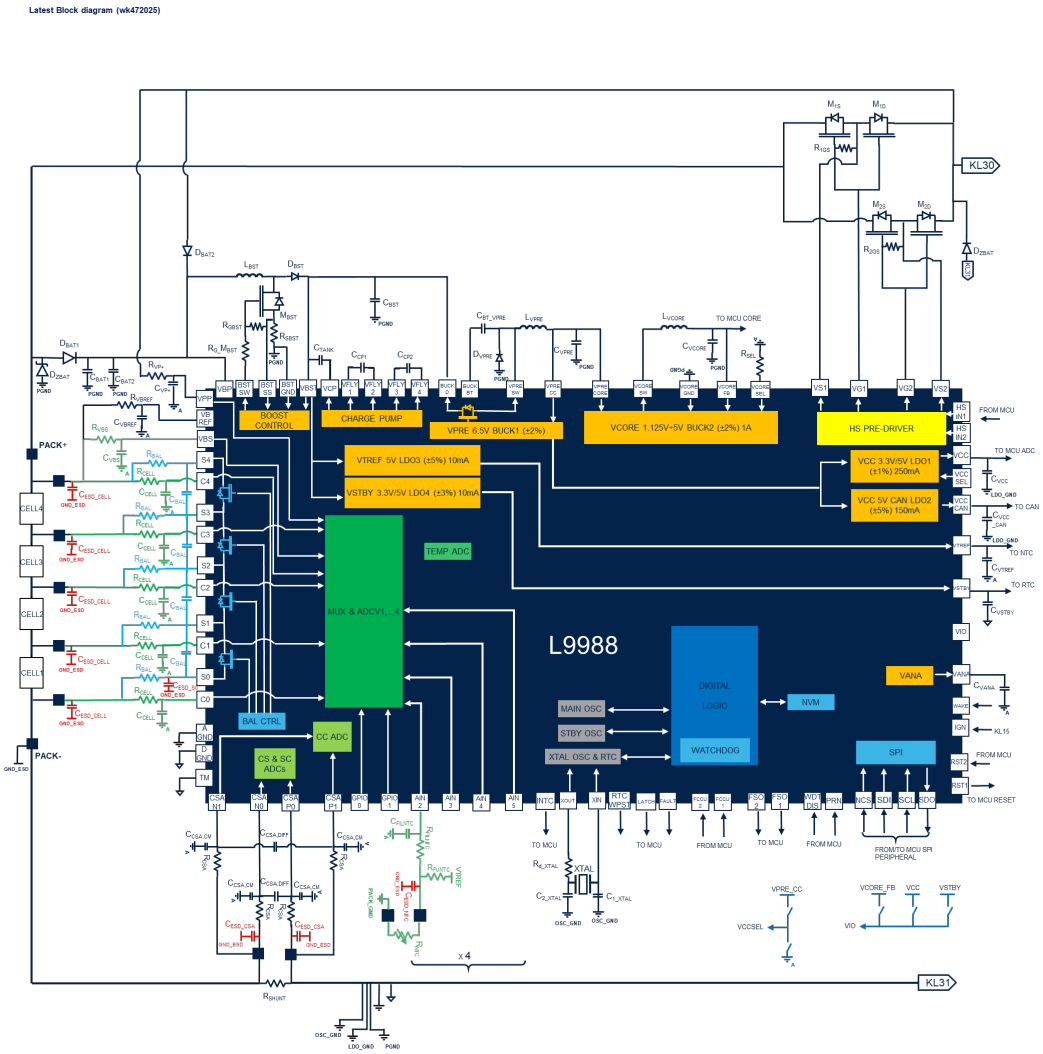
5 Device register map

L9988 register map is available in the STSW-L9988FW software package

6 Application information

Referring to the figure below, this section lists the layout recommendations and the components to be used in a typical application circuit.

Figure 55. Typical application scenario



6.1 Layout recommendations

6.1.1 PCB stackup

In order to achieve the best performance in terms of accuracy and EMC, an optimal PCB layer partitioning must be chosen. On a 4-layer board, the following stackup is recommended.

- **Top layer**: analog sensing lines
  - Battery sensing lines
  - Cell sensing lines
  - Current sensing lines
  - NTC sensing lines
- **2nd layer**: ground planes
  - AGND under sensing lines
  - DGND under digital lines
  - GND_ESD under the ESD capacitors in the battery connector region
  - PGND under the power supply circuit
  - OSC_GND under the XTAL oscillator circuit
  - LDO_GND under the LDO1(VCC) and LDO2 (VCC_CAN) circuits
- **3rd layer**: analog forcing lines and balancing lines
- **Bottom layer**: digital lines and regulators

6.1.2 Ground connections

In order to achieve the best performance in terms of accuracy and EMC, care must be taken while designing ground connections. The L9988 features 2 ground pins used as internal reference:

- **AGND**: is the reference plane for the analog circuitry and must be kept as “clean” as possible in order not to catch noise from the nearby switching components. It can be used as the 2nd layer of the PCB to shield voltage sense lines routed on the 1st layer.
- **DGND**: is the reference plane for the digital circuitry and it introduces noise on the PCB due to the logic switching activity. It must be separated from the AGND plane and can be routed over the 2nd PCB layer.

It is also recommended to implement the following 3 ground planes:

- **PGND**: is the reference plane for the power supply circuit and for the buck regulators.
- **OSC_GND**: is the reference for the external XTAL oscillator.
- **LDO_GND**: is the reference for the LDO1(VCC) and LDO2 (VCC_CAN) circuits.

All the planes/lines mentioned above should be joined on the same node (KL31) and then connected to PACK- through the RSHUNT resistor, thus measuring the system current.

6.1.3 Cell balancing and cell sensing lines

The sensing tracks of CELLs and NTCs must be kept away from the noisy paths. Concerning the cells, the sensing paths and the balancing ones shall be split as close as possible to the cell input connector.

6.1.4 Current sensing lines

Regarding the current sensing circuit, it is good practice to reduce the number of contacts and ways to a minimum to reduce possible thermal effects that lead to phase shifts between the CSAx inputs. Furthermore, it is necessary to provide parallel tracks on the same side of the product, as symmetrical and shielded as possible.

6.1.5 Regulators

The buck circuit must be placed as close as possible to the corresponding device pin in order to avoid loops generated by long traces and filter any ripple caused by current absorption peaks. The ground join must be positioned as close as possible to the device pins.

6.2 Power supply circuit

Table 125. Recommended power supply components

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
D_{ZBAT}	TVS for power supply line	-			Optional	Needs to be sized in order to avoid AMR violation, considering hot-plug spikes, ISO pulse, EFT and SURGE positive and negative pulses. Proposed STMicroelectronics LDP01-28AY and SM6F13AY
C_{BAT1}	Tank capacitor for power supply line	40µF (4 * 10µF)	50V	20%	Mandatory	
C_{BAT2}	Filtering capacitor for power supply line	100nF	50V	20%	Optional	Improves EMC emission/immunity performances at high frequency. Place as close as possible to IC pin.
D_{BAT1}	Reverse diode for power supply line	-			Optional	Maximum forward voltage = 0.5V Proposed STMicroelectronics STPS2L40UF or PMEG060V030EPDZ
D_{BAT2}	Reverse diode for power supply line	-			Optional	Maximum forward voltage = 0.5V Proposed STMicroelectronics STPS2L40UF or PMEG060V030EPDZ
R_{VBREF}	Filtering resistor for battery supply line for internal ADC reference	200Ω		1%	Mandatory	Sized to match the cutoff frequency of battery sensing lines The cutoff frequency is $f_C = \frac{1}{2\pi R_{VBREF} C_{VBREF}}$ Place as close as possible to device pin
C_{VBREF}	Filtering capacitor for battery supply line for internal ADC reference	47nF	50V	10%	Mandatory	Sized to obtain cutoff frequency in conjunction with R_{VBREF} Place as close as possible to device pin
C_{ESD_BAT}	ESD protection capacitor for power supply line	47nF	100V	20%	Optional	

6.3 Battery sensing circuit

Table 126. Recommended components for battery sensing circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
R_{VBS}	Filtering resistor for battery sensing line	200Ω		1%	Mandatory	Sized to match the cutoff frequency of cell sensing lines. The cutoff frequency is $f_C = \frac{1}{(2\pi R_{VBS} C_{VBS})}$
C_{VBS}	Filtering capacitor for battery sensing line	47nF	50V	10%	Mandatory	Sized to obtain cutoff frequency in conjunction with R_{VBS}
R_{VPP}	Filtering resistor for KL30 sensing input	200Ω		1%	Mandatory	Sized to match the cutoff frequency of battery sensing lines. The cutoff frequency is $f_C = \frac{1}{(2\pi R_{VP} C_{VP})}$
C_{VPP}	Filtering capacitor for KL30 sensing input	47nF	50V	10%	Mandatory	Sized to obtain cutoff frequency in conjunction with R_{VPP}
C_{ESD_VBS}	ESD protection capacitor for battery sensing line	47nF	50V	20%	Optional	

6.4 Boost pre-regulator (VBST) circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
$M_{BST}_Q_G$	External FET M_{BST} gate charge	16nC			Mandatory	Proposed Onsemi NVTFS5C466NL Proposed NXP BUK9M24-40E
$M_{BST}_C_{iss}$	External FET M_{BST} input capacitor	860pF			Mandatory	
$R_G_M_{BST}$	External FET M_{BST} gate serial resistor	10Ω			Mandatory	
R_{GBST}	External FET M_{BST} gate pull-down resistor	220KΩ			Mandatory	
R_{SBST}	External shunt resistor	100mΩ		10%	Mandatory	
C_{BST}	Output capacitance	18.8µF (4 * 4.7µF)	50V	20%	Mandatory	Output capacitor ESR 3mΩ Proposed Murata GCM31CR71E475KA55
L_{BST}	Boost inductor	2.2µH min 4.7µH typ 10µH MAX		-	Mandatory	Inductor DC resistance 20mΩ typ, 40mΩ MAX Proposed TDK B82464P4103M000
D_{BST}	VBST external diode	-			Mandatory	Maximum forward voltage = 0.5V Proposed NXP PMEG060V030EPDZ Proposed Onsemi NRVTSAF5100ET3G

6.5 Charge pump (VCP) circuit

Table 127. Recommended components for charge pump circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
C_{TANK}	External tank capacitor	680nF	50V	10%	Mandatory	Proposed AVX 08055C684K4Z2A
C_{CP1}	External flying capacitor	33nF	50V	30%	Mandatory	Proposed AVX 06035C333K4Z2A
C_{CP2}	External flying capacitor	33nF	50V	30%	Mandatory	Proposed AVX 06035C333K4Z2A

6.6 Buck1 pre-regulator (VPRE) circuit

Table 128. Recommended components for Buck1 pre-regulator circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
C_{VPRE}	VPRE external output capacitance (decoupling capacitors in parallel)	20µF (2 * 10µF)	25V	10%	Mandatory	Proposed TDK CGA4J1X7S1E106K125AC Proposed Murata GCM31CR71C106KA64K
L_{VPRE}	VPRE external output inductor	22µH		20%	Mandatory	Inductor DC resistance 26.3mΩ Proposed TDK SLF12575T-220M4R0-H (Proposed Coiltronics HCM1A0703V2-220-R) (Proposed TDK CLF7045NIT-220M-D)
C_{BT_VPRE}	VPRE external bootstrap capacitor	0.47µF	25V	20%	Mandatory	Proposed TDK CGA3E3X5R1E474K080AB Proposed Murata GCM188R71C474KA55
D_{VPRE}	VPRE external diode	-			Mandatory	Proposed Vishay SS36

6.7 Buck2 regulator 1.125V-5V (VCORE) circuit

Table 129. Recommended components for Buck2 VCORE regulator circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
R_{SEL}	VCORE external voltage selection resistor	0KΩ 10KΩ 20KΩ 30KΩ 39KΩ 51KΩ 68KΩ		1%	Mandatory	VCORE disabled V_{VCORE} = 1.125V V_{VCORE} =1.2V V_{VCORE} = 1.3V V_{VCORE} = 1.5V V_{VCORE} = 3.3V V_{VCORE} = 5V

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
L_{VCORE}	VCORE external coil	22µH		20%	Mandatory	Inductor DC resistance 135mΩ typ, 149mΩ MAX Proposed Coiltronics HCM1A0703V2-220-R (Proposed TDK CLF7045NIT-220M-D)
C_{VCORE}	VCORE external output capacitor	68µF= (22µF*3//2.2µF)		20%	Mandatory	Output capacitor ESR 1mΩ to 10mΩ Proposed Murata GRT21BR61C226ME13L Proposed Murata CGA3E1X5R1C225K080AC

6.8 3.3V/5V LDO1 (VCC) circuit

Table 130. Recommended components for LDO1 circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
C_{VCC}	External output capacitor	10µF		20%	Mandatory	Output capacitor ESR 5mΩ Proposed Murata GCM188D70J106ME36

6.9 5V LDO2 (VCC CAN) circuit

Table 131. Recommended components for LDO2 circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
C_{VCC_CAN}	External output capacitor	10µF		20%	Mandatory	Output capacitor ESR 5mΩ Proposed Murata GCM188D70J106ME36

6.10 5V thermistor bias LDO3 (VTREF) circuit

Table 132. Recommended components for LDO3 circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
C_{VTREF}	External output capacitance	2µF (2 * 1µF)		30%	Mandatory	Output capacitor ESR 15mΩ Proposed Kemet C1206C105K3RACAUTO

6.11 3.3V/5V standby LDO4 (VSTBY) circuit

Table 133. Recommended components for LDO4 circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
C_{VSTBY}	External output capacitor	4.7µF		10%	Mandatory	Output capacitor ESR 3mΩ Proposed Murata GCM31CR71E475KA55

6.12 Internal analog LDO (VANA) circuit

Table 134. Recommended components for internal analog LDO circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
C_{VANA}	External output capacitor	2.2µF		30%	Mandatory	Output capacitor ESR 1mΩ to 10mΩ Proposed Murata GRM188R61E225KA12D

6.13 Cell sensing circuit

Table 135. Recommended components for cell sensing circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
R_{CELL}	Filtering resistor for cell sensing line	200Ω		1%	Mandatory	Filters noise on cell sensing lines. The cutoff frequency is $f_C = \frac{1}{(2\pi R_{CELL} C_{CELL})}$ Sized to obtain 16.9KHz cutoff frequency on cell sensing lines in conjunction with C_{CELL}
C_{CELL}	Filtering capacitor for cell sensing line	47nF	50V	10%	Mandatory	Sized to obtain cutoff frequency in conjunction with R_{CELL}
C_{ESD_CELL}	ESD protection capacitor for cell sensing line	47nF	100V	20%	Optional	

6.14 Cell balancing circuit

Table 136. Recommended components for cell balancing circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
R_{BAL}	Balancing resistor for cell balancing line	22Ω	500mW	10%	Mandatory	Sized to obtain 110mA maximum balancing current when cell voltage is 5V
C_{BAL}	Filtering capacitor for cell balancing line	68nF	50V	10%	Mandatory	Filters noise on balancing sensing lines. The cutoff frequency is $f_C = \frac{1}{(4\pi R_{BAL} C_{BAL})}$ Sized to obtain 53KHz cutoff frequency on cell balancing lines in conjunction with R_{BAL}
C_{S0}	Filtering capacitor for S0 pin	47nF	50V	10%	Optional	Filters noise on balancing sensing lines. The cutoff frequency is $f_C = \frac{1}{(2\pi R_{BAL} C_{S0})}$

6.15 Current sensing circuit

Table 137. Recommended components for current sensing circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
R_{SHUNT}	CSA shunt resistor	100µΩ		1%	Mandatory	Proposed Vishay WSLP5931L1000FEA

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
R_{CSA}	CSA differential filtering resistor	47Ω	100mW	1%	Mandatory	Used to filter both differential and common-mode noise on the CSAN0/1 and CSAP0/1 inputs The differential filter cutoff frequency is $f_C = \frac{1}{4\pi R_{CSA}\left(C_{CSA_DIFF} + \frac{C_{CSA_CM}}{2}\right)}$ The common mode filter cutoff frequency is $f_C = \frac{1}{2\pi R_{CSA} C_{CSA_CM}}$ Sized to obtain 3KHz differential cutoff frequency in conjunction with $C_{CSA_DIFF}$and C_{CSA_CM}
C_{CSA_DIFF}	CSA differential filtering capacitor	560nF	16V	10%	Mandatory	Sized to obtain 3KHz differential cutoff frequency in conjunction with R_{CSA} and C_{CSA_CM}
C_{CSA_CM}	CSA common mode filtering capacitor	33nF	16V	10%	Mandatory	Sized to obtain 100KHz cutoff frequency in conjunction with R_{CSA}. Needed to pass BCI tests. Choose a capacitor with low impedance up to 400MHz
C_{ESD_CSA}	CSA ESD protection capacitor	100nF	50V	10%	Optional	Contributes also to filtering BCI. Choose a capacitor with low impedance up to 400MHz

6.16 Temperature sensing circuit

Table 138. Recommended components for temperature sensing circuit

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
R_{PUNTC}	NTC pull-up biasing resistor	10KΩ		10%	Mandatory	
R_{FILNTC}	NTC filtering resistor	3.3KΩ	250mW	10%	Mandatory	Filters noise on NTC lines and protects against short-to-battery The cutoff frequency is $f_C = \frac{1}{(2\pi R_{FILNTC} C_{FILNTC})}$ Power rating sized for withstanding short to maximum operating battery voltage
C_{FILNTC}	NTC filtering capacitor	10nF	50V	20%	Mandatory	Sized to obtain cutoff frequency in conjunction with R_{FILNTC} Voltage rating shall be sized considering short-to-battery failure
C_{ESD_NTC}	NTC ESD protection capacitor	6.8nF	50V	20%	Optional	Voltage rating shall be sized considering short-to-battery failure

6.17 GPIOs

Table 139. Recommended components for GPIO connection

Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
C_{GPIO_EXT}	GPIO external bypass capacitor	150pF			Mandatory	
$R_{GPIO_EXT_PU}$	GPIO external pull-up resistor for open-drain configurations	4.7KΩ		1%	Mandatory	

6.18 HS pre-drivers and CB MOSFETs

Table 140. Recommended components for CB MOSFETs connection

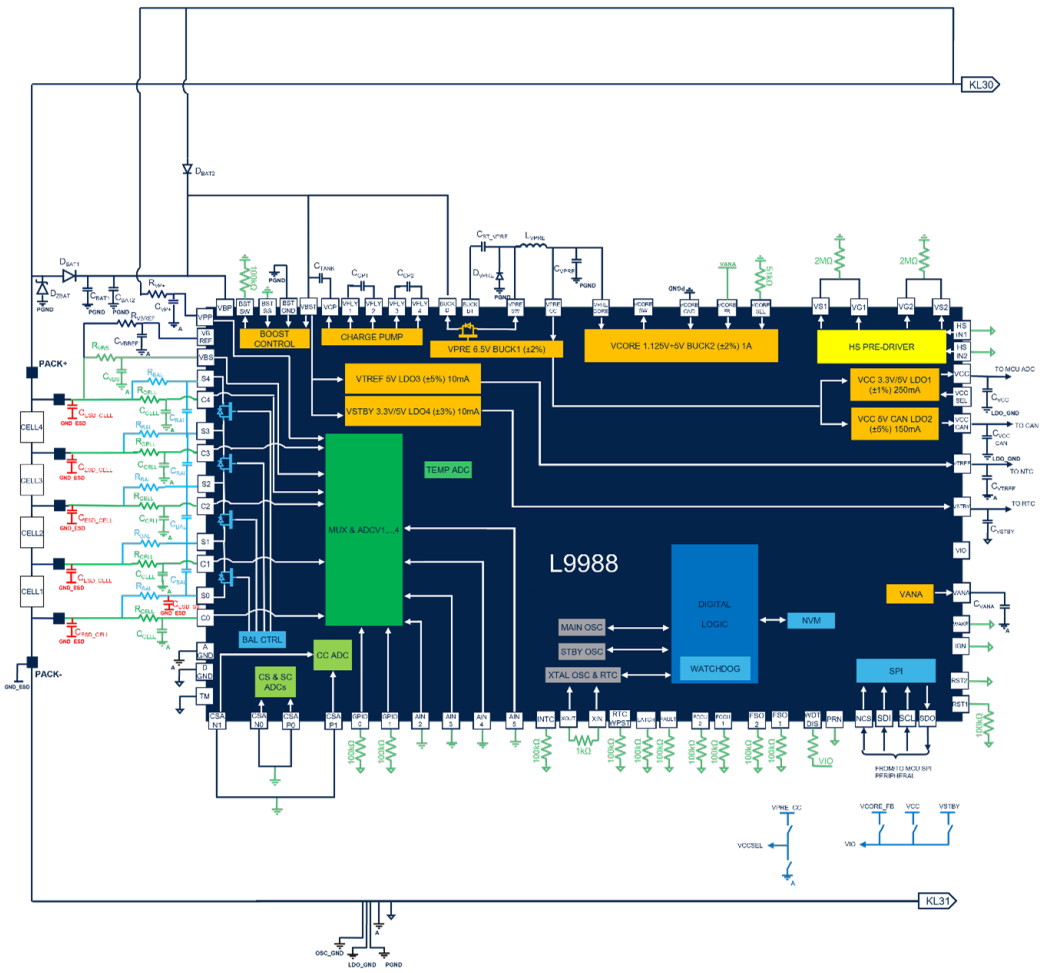
Symbol	Parameter	Value	Rating	Max tolerance	Required	Comments
R_{1GS}, R_{2GS}	External VGS pull-down resistance	1MΩ		20%	Optional	

Table 141. Recommended external MOSFETs

Part number	Maker	V_{DS_MAX} [V]	V_{GS_MAX} [V]	V_{GSth} [V]	I_D [A] 25°C	P_{TOT} [W] 25°C	R_{DSon} [mΩ] @V_{GS}=10V	Q_g [nC] @V_{GS}=10V	Required
TPWR7904PB	Toshiba	40	20	2 min, 3 MAX	150	170	0.79	85	Optional
JMSL040SAGQ	JieJie Microelectronics	40	20	1.2 min, 2.5 MAX	349	139	0.75	116	Optional
STL325N4LF8AG	ST Microelectronics	40	16	1.2 min, 2 MAX	373	188	0.75	95	Optional
NVMFS5C410NL	ON Semiconductor	40	20	2 MAX	330	167	0.82	143	Optional

6.19 Unused pin connections

Figure 56. Unused pin connections



Besides, for other functions, when not used, recommended pin configuration is according to the following Table 137.

Table 142. Typical unused pins connection

Unused pin #	Symbol	Pin functions	Pin type	Connection
1	CSAN1	Current sense ADC1 negative input terminal	Analog	Short to CSAP1 and then connect to GND
2	CSAP1	Current sense ADC1 positive input terminal	Analog	Short to CSAN1 and then connect to GND
3	CSAN0	Current sense ADC0 negative input terminal	Analog	Short to CSAP0 and then connect to GND
4	CSAP0	Current sense ADC0 positive input terminal	Analog	Short to CSAN0 and then connect to GND
23	AIN5	NTC sensing input	Analog	Short to GND
24	AIN4	NTC sensing input	Analog	Short to GND
25	AIN3	NTC sensing input	Analog	Short to GND
26	AIN2	NTC sensing input	Analog	Short to GND
27	GPIO0	General purpose I/O	Analog Digital in Digital out	Pull-down to GND by 100kΩ
28	GPIO1	General purpose I/O	Analog Digital in Digital out	Pull-down to GND by 100kΩ
29	VS1	MOS 1S-1D source	Analog	Short to VG1 and pull-down to GND by 2MΩ
30	VG1	MOS 1S-1D gate	Analog	Short to VS1 and pull-down to GND by 2MΩ
31	VG2	MOS 2S-2D gate	Analog	Short to VS2 and pull-down to GND by 2MΩ
32	VS2	MOS 2S-2D source	Analog	Short to VG2 and pull-down to GND by 2MΩ
38	VBST	Boost output voltage	Power	Short to VBP
39	BSTSW	Boost switching terminal	Analog	Pull-down to GND by 100kΩ
40	BSTSS	Boost sensing terminal	Analog	Short to GND
50	WAKE	Edge-triggered wakeup input	Digital in	Short to GND if using IGN
51	IGN	Level-triggered wakeup input (KL15)	Digital in	Short to GND if using WAKE
57	VCORESW	Buck2 VCORE switching node	Analog	Open
59	VCOREFB	Buck2 VCORE feedback voltage	Power	Short to VANA
60	VCORESEL	Buck2 VCORE output voltage selection pin	Analog	Connect 51kΩ
61	XOUT	Ext oscillator output	Analog	Short to XIN with 1kΩ
62	XIN	Ext oscillator input	Analog	Short to XOUT with 1kΩ
64	INTC	Interrupt pin	Digital out	Pull-down to GND by 100kΩ
65	RST1	Reset output. Reset MCU	Digital out	Pull-down to GND by 100kΩ
66	FSO1	Fail safe output (active high)	Digital out	Pull-down to GND by 100kΩ
67	FSO2	Fail safe output (active low)	Digital out	Pull-down to GND by 100kΩ
70	RTCWPST	RTC wakeup state	Digital out	Pull-down to GND by 100kΩ
71	LATCH	Latch interrupt output in case of short-circuit detection	Digital out	Pull-down to GND by 100kΩ
73	FAULT	Fault interrupt output in case OV/UV/OT etc. occur during voltage conversion routine, OVC/CC_WUP etc. occur during current conversion routine or other detection described in detail in Section 4.12.1	Digital out	Pull-down to GND by 100kΩ
74	PRN	Watchdog pin	Digital in	Short to GND

Unused pin #	Symbol	Pin functions	Pin type	Connection
75	HS_IN2	MOS 2S-2D command	Digital in	Short to GND
76	HS_IN1	MOS 1S-1D command	Digital in	Short to GND
77	RST2	Reset input. Reset device	Digital in	Short to GND
78	WDTDIS	Watchdogs disable	Digital in	Pull-up to VIO with 10kΩ
79	FCCU2	MCU lock-step error detection	Digital in	Short to GND and program FCCU_REACT = 0
80	FCCU1	MCU lock-step error detection	Digital in	Short to GND and program FCCU_REACT = 0

7 Packaging and marking

Figure 57. **Package TQFP80**

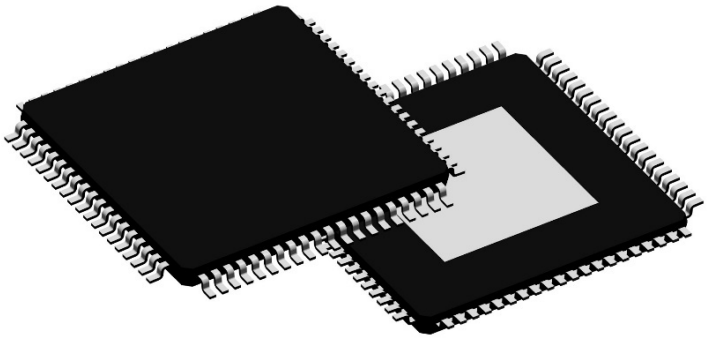


Table 143. **TQFP80 14x14 80L exposed pad down package dimensions (JEDEC ref. number MS-026-AEC-HD**

ST DATABOOK				
Symbol	**Min.**	**Nom.**	**Max.**	**Note**
Θ	0°	3.5°	7°	
Θ1	0°	-	-	
Θ2	10°	12°	14°	
Θ3	10°	12°	14°	
A	-	-	1.20	15
A1	0.05	-	0.15	12
A2	0.95	1.00	1.05	15
b	0.22	0.32	0.38	9,11
b1	0.22	0.30	0.33	11
c	0.09	-	0.20	11
c1	0.09	-	0.16	11
D		16.00 BSC		4
D1		14.00 BSC		2,5
D2		VARIATIONS		13
D3		VARIATIONS		14
e		0.65 BSC		
E		16.00 BSC		4
E1		14.00 BSC		2,5
E2		VARIATIONS		13
E3		VARIATIONS		14
L	0.45	0.60	0.75	
L1		1.00 REF		
N		80		16
R1	0.08	-	-	

ST DATABOOK				
Symbol	Min.	Nom.	Max.	Note
R2	0.08	-	0.20	
S	0.20	-	-	

TOLERANCE OF FORM AND POSITION		
Symbol	DATABOOK	Note
aaa	0.20	1,7,20
bbb	0.20	
ccc	0.10	
ddd	0.13	

VARIATIONS				
DATABOOK				
Symbol	Min.	Nom.	Max.	PAD OPT.
D2	-	-	8.27	8.0x8.0 (T1)
E2	-	-	8.27	
D3	6.78	-	-	
E3	6.78	-	-	

Figure 58. **TQFP80 bottom and top view**

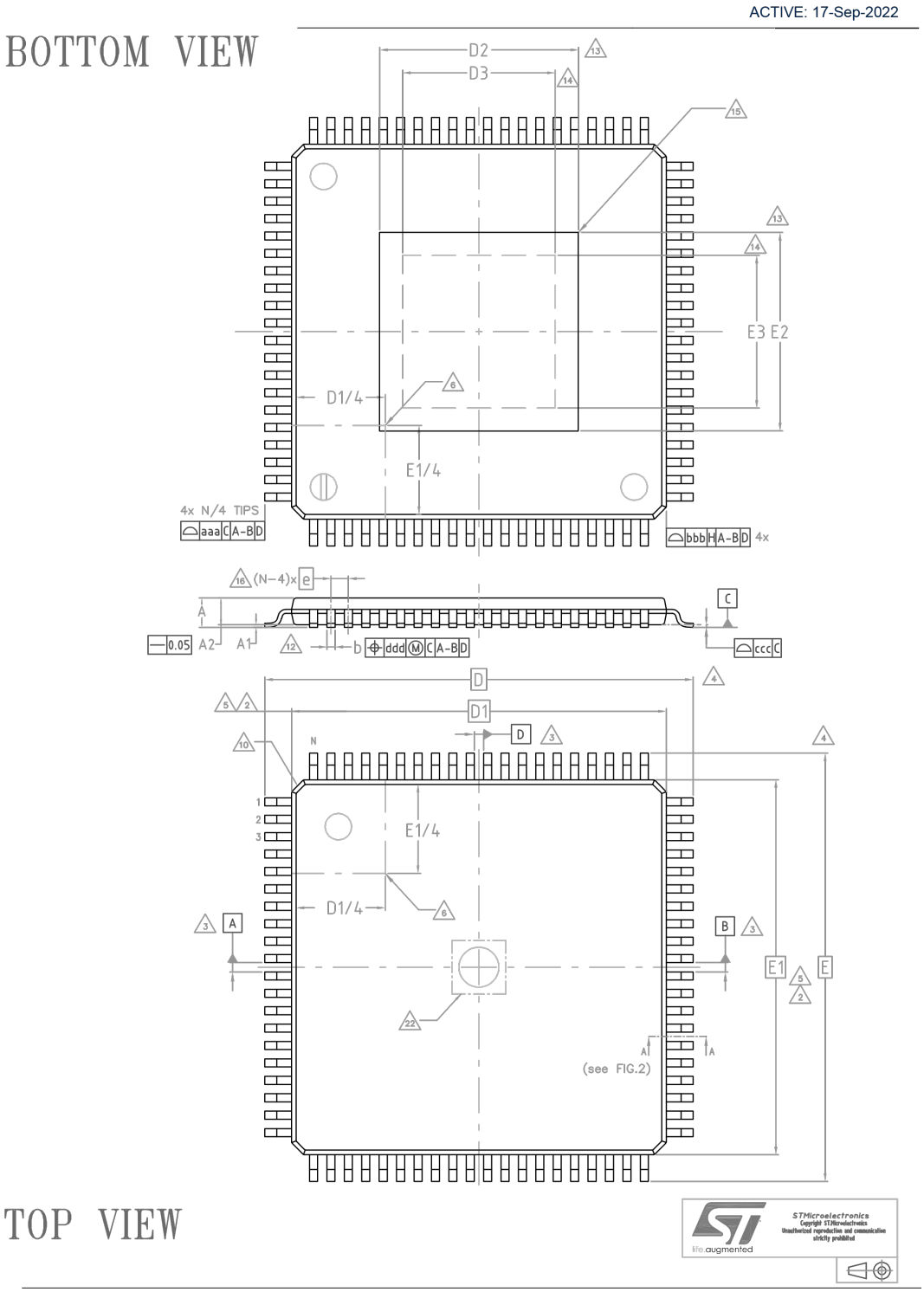


Figure 59. **TQFP80 section A-A and section B-B**

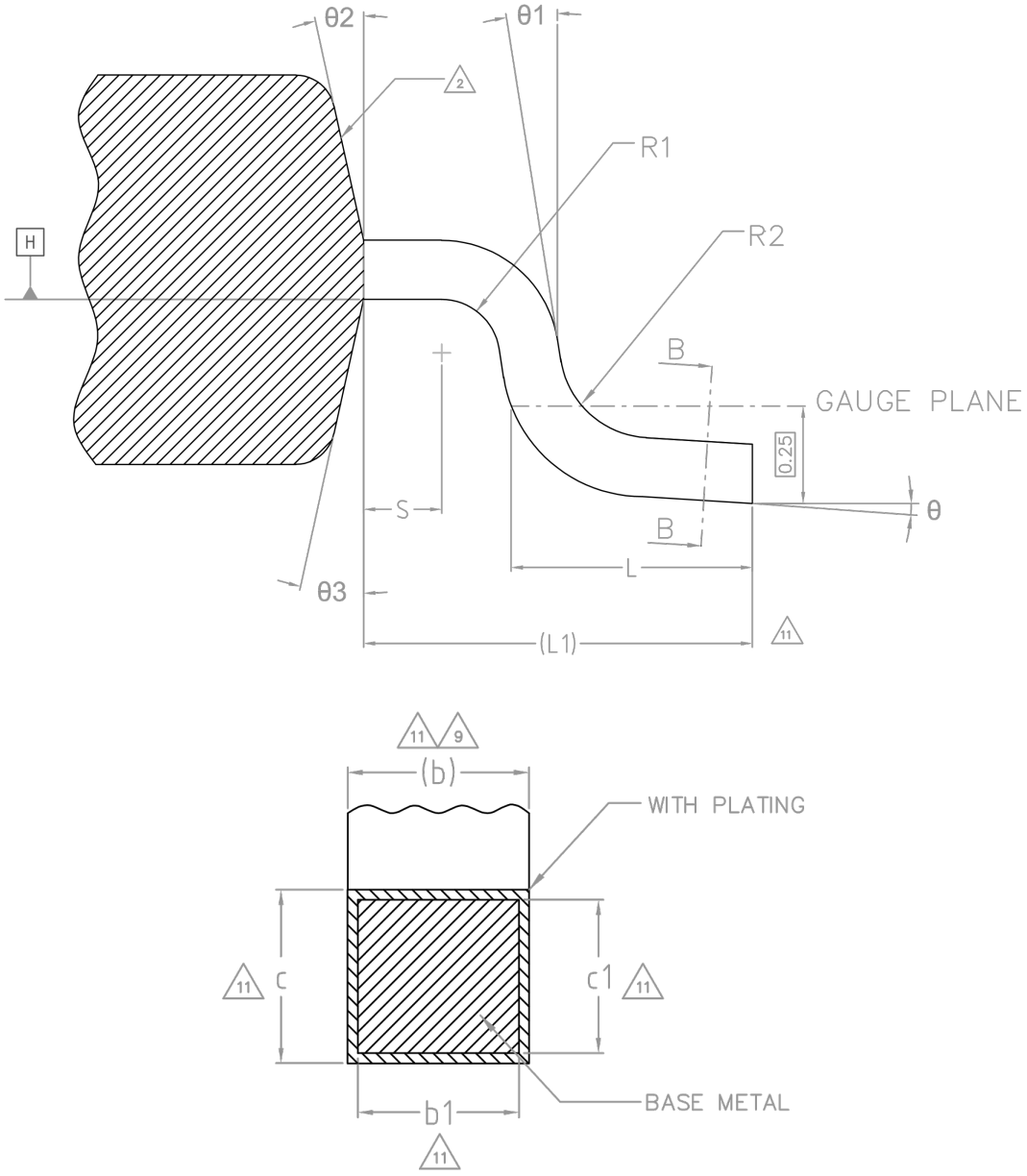
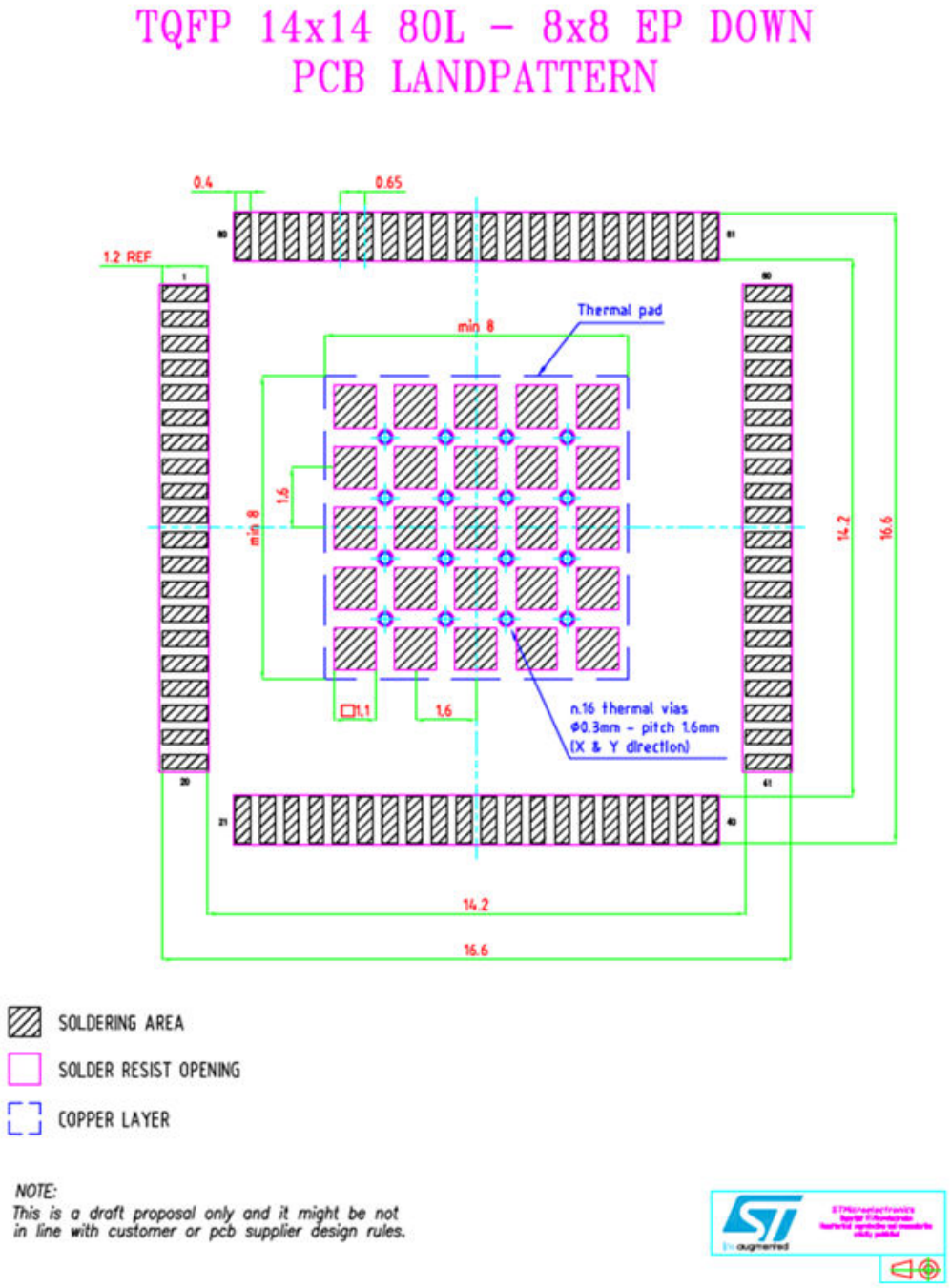


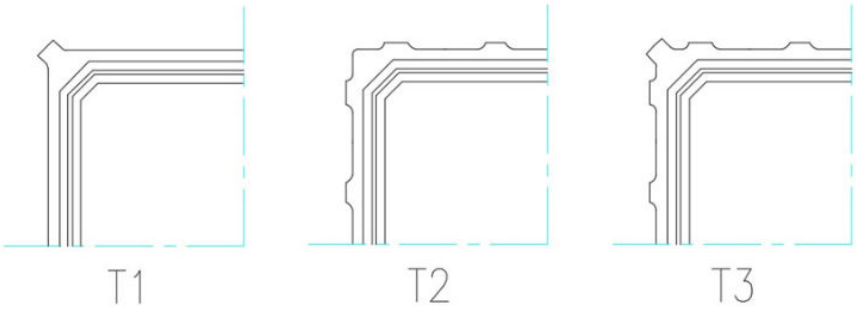
Figure 60. **PCB landpattern**



Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by up to 0.15 mm.
3. Datums A-B and D are to be determined at datum plane H.
4. To be determined at the seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "*0.25 mm*" per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of the pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards of the leads.

9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between a protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. The exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. The type of exposed pad is variable depending on leadframe pad design (T1, T2, T3), as shown in the figure below. The end user should verify D2 and E2 dimensions according to specific device application.



14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by the internal edge of the inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.
17. For tolerance of form and position see table.
18. Critical dimensions:
    a. Stand-off
    b. Overall width
    c. Lead coplanarity
19. Component cross reference: see DMS spec. 8404938, DM00886812.
20. For symbols, recommended values and tolerances see table below
21. POA FORMAT & CONTENT spec. reference number is CD10033601.
22. A notch may be present in this area (MAX 2.0mm square) if center top gate molding technology is applied. Resin gate residual not protruding out of package top surface.

Table 144. Tolerance definition

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by the basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	
ccc	The unilateral tolerance located above the seating plane wherein the bottom surfaces of all terminals must be located.	This tolerance is commonly known as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with the tolerance zone defined by “b”.

Parts marked as **ES** are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Appendix A Ordering codes

Table 145. **Device label**

Order code	Package	Packing
L9988	TQFP80	Tray
L9988-TR		Tape & Reel

Revision history

Table 146. **Document revision history**

Date	Version	Changes
03-Aug-2026	1	Initial release.

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