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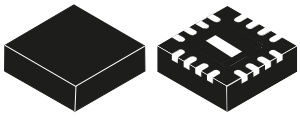
A6983I

Datasheet

Automotive 38 V, 10 W synchronous iso-buck converter for isolated applications



QFN16 (3 x 3 mm)

Maturity status link
A6983I

Features

- AEC-Q100 qualified
- Operating temperature range: -40 °C to +150 °C for T_j
- Designed for iso-buck topology
- 3.5 V to 38 V operating input voltage
- Load dump tolerant up to 40 V
- Primary output voltage regulation, no optocoupler required
- 4.5 A source/sink peak primary current capability
- Peak current mode architecture in forced PWM operation
- 390 ns blanking time
- 25 µA operating quiescent current
- 200 kHz to 1 MHz programmable switching frequency, stable with low ESR capacitor: min 2 µF
- Internal compensation network
- 2 µA shutdown current
- Internal soft-start
- Enable pin
- Overvoltage protection
- Output voltage sequencing
- Thermal protection
- Optional spread spectrum for improved EMC
- Power Good
- Synchronization to external clock
- QFN16 (3x3 mm) package

Applications

- Automotive isolated IGBT/SiC MOSFET gate drive supply
- OBC (on-board charger) for HEV/EV
- Electric traction systems

Description

The A6983I is a device specifically designed for isolated buck topology. The primary output voltage can be accurately adjusted, whereas the isolated secondary output is derived by using a given transformer ratio. No optocoupler is required. The primary sink capability up to -4.5 A (even during soft-start) allows a proper energy transfer to the secondary side, as well as enables a tracked soft-start of the secondary output. The control loop is based on a peak current mode architecture and the device operates in forced PWM. The 390 ns blanking time filters oscillations, generated by the transformer leakage inductance, makes the solution more robust.

Both the compact QFN-16 (3x3 mm) package and the internal compensation of the A6983I help minimizing the design complexity and size.

The switching frequency can be programmed in the 200 kHz to 1 MHz range with an optional spread spectrum for improved EMC.

The EN pin provides a enable/disable functionality. The typical shutdown current is 2 µA when disabled. As soon as the EN pin is pulled-up, the device is enabled and the internal 1.3 ms soft-start takes place. The A6983I features a Power Good open collector that monitors the FB voltage. Pulse by pulse current sensing on both power elements implements an effective constant current protection and thermal shutdown prevents thermal runaway.

1 Pin configuration

Figure 1. **Pin connection (top through view)**

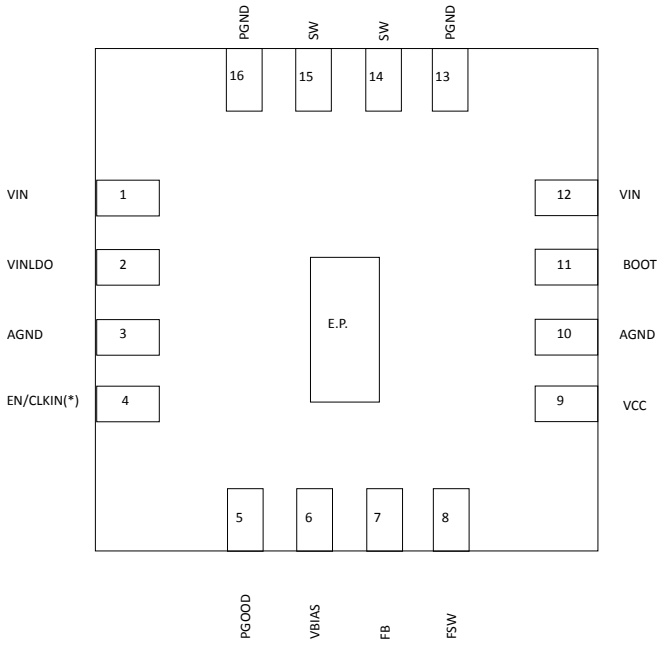


Table 1. **Pin description**

Pin n°	Symbol	Function
1	VIN	DC input voltage.
2	VINLDO	DC input voltage, connect to the supply rail with a simple RC filter.
3	AGND	Analog ground.
4	EN / CLKIN	Enable pin with internal voltage divider. Pull-down/up to disable/enable the device. This pin is also used to provide an external clock signal, which synchronizes the device.
5	PGOOD	The PGOOD open collector output is driven to low impedance when the output voltage is out of regulation and released once the output voltage becomes valid.
6	VBIAS	Typically connected to the regulated output voltage, an external voltage source can be used to supply part of the analog circuitry to reduce current consumption at light load. Connect to AGND if not used.
7	FB	Feedback input. The primary output voltage can be regulated by connecting an external resistor divider (upper resistor from VOUT to FB and lower resistor between FB and ground).
8	FSW	Connect an external resistor to program the oscillator frequency and enable optional dithering.
9	VCC	This pin supplies the embedded analog circuitry. Connect a ceramic capacitor (≥ 1 µF) to filter internal voltage reference.
10	AGND	Analog ground.
11	BOOT	Connect an external capacitor (100 nF typ.) between the BOOT and SW pins. The gate charge required to drive the internal nMOS refreshes during the low-side switch conduction time.
12	VIN	DC input voltage.
13	PGND	Power ground.
14	SW	Switching node.
15	SW	Switching node.

Pin n°	Symbol	Function
16	PGND	Power ground.
-	Exposed PAD	Exposed pad must be connected to AGND, PGND.

2 Typical application circuit

Figure 2. Basic application

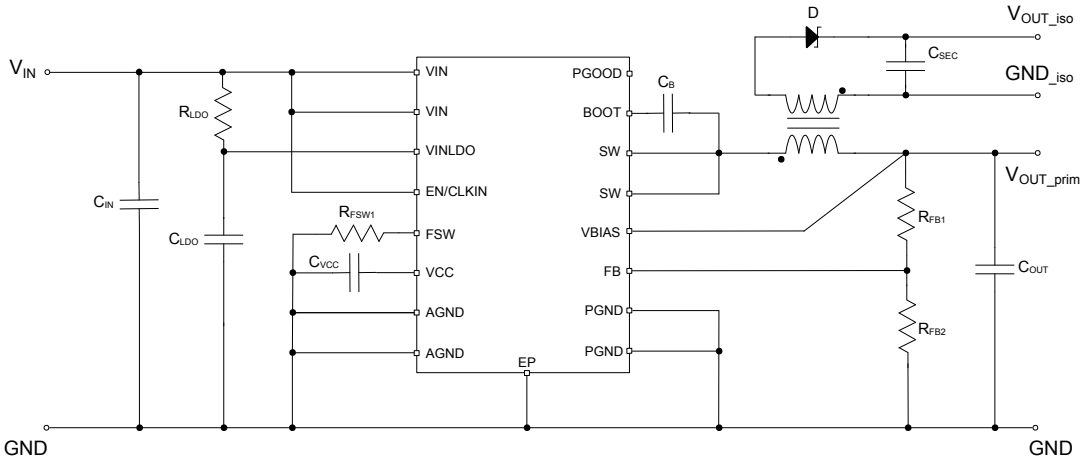


Table 2. Typical application component

Symbol	Value	Description
C_{IN}	10 µF	Input capacitor Two additional 1 µF capacitors, each one very close to pins 1 and 12 respectively, are strongly recommended.
R_{LDO}	0.1 kΩ	VINLDO filter resistor
C_{LDO}	1 µF	VINLDO filter capacitor
C_{VCC}	1 µF	VCC bypass capacitor
C_B	100 nF	Bootstrap capacitor
C_{OUT}	3 x 22 µF	Output capacitor
R_{FB1}	400 kΩ	VOUT divider upper resistor
R_{FB2}	82 kΩ	VOUT divider lower resistor
R_{FSW1}	0 Ω	Frequency setting resistor

3 Maximum ratings

3.1 Absolute maximum ratings

Stressing the device above the ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VIN	Maximum pin voltage	-0.3	42	V
AGND	Maximum pin voltage	0	0	V
PGND	Maximum pin voltage	-0.3	0.3	V
BOOT	Maximum pin voltage	SW -0.3	SW +4	V
VCC	Maximum pin voltage	-0.3	Min. (VIN +0.3 V; 4 V)	V
VOUT/FB	Maximum pin voltage	-0.3	8	V
FSW	Maximum pin voltage	-0.3	VCC +0.3	V
VBIAS	Maximum pin voltage	-0.3	VIN +0.3	V
EN	Maximum pin voltage	-0.3	VIN +0.3	V
PGOOD	Maximum pin voltage	-0.3	VIN +0.3	V
SW	Maximum pin voltage	-0.85	VIN +0.3	V
		-3.8 for 0.5 ns (1)		V
TJ	Operating temperature range	-40	150	°C
TSTG	Storage temperature range	-65	150	°C
TLEAD	Lead temperature (soldering 10 sec.)		260	°C
IHS, ILS	High-side/low-side RMS switch current		3	A

1. *Negative peak voltage during switching activities caused by parasitic layout elements.*

3.2 ESD protection

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM (corner pins)	500	V
		CDM	750	

3.3 Thermal characteristics

Table 5. Thermal data

Symbol	Parameter	Package	Value	Unit
R_{th_JA}	Thermal resistance junction ambient (device soldered on the STMicroelectronics® demonstration board, refer to Section 8.1)	QFN16	30	°C/W

4 Electrical characteristics

T_J = -40 to 150 °C, V_{IN} = 12 V unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		3.5		38	V
V_{INH}	V_{CC} rising threshold		2.3		3.3	V
V_{INL}	$V_{CC\ UVLO}$ falling threshold		2.15		3.15	V
I_{PK} (1)	Peak current limit	Duty cycle < 40%	4.1	4.6		A
		Duty cycle = 99% Closed loop operation	3.1	3.6		A
I_{VY}	Valley current limit		3.3	3.9	4.6	A
I_{VY_SINK} (1)	Reverse current limit	VOUT overvoltage	4	4.5	5	A
R_{DSON_HS}	High-side RDSON			0.130	0.26	Ω
R_{DSON_LS}	Low-side RDSON			0.085	0.18	Ω
T_{OFF_MIN}	Minimum off-time			200		ns
T_{ON_MIN}	Minimum on-time		330	390	450	ns
Enable						
V_{WAKE_UP}	Wake-up threshold	Rising			0.7	V
		Falling	0.2			V
V_{EN}	Enable threshold	Rising	1.08	1.2	1.32	V
		Falling		0.2		V
VCC regulator						
V_{CC}	LDO output voltage		3	3.3	3.6	V
Power consumption						
I_{SHTDWN}	Shutdown current from V_{IN}	VEN = GND		2	3	µA
I_{Q_VIN}	Quiescent current from V_{IN}	VBIAS = GND	1.6	2.3	3	mA
		VBIAS = 5 V	300	550	800	µA
I_{Q_VBIAS}	Quiescent current from VBIAS	VBIAS = 5 V	1.3	1.8	2.3	µA
Soft-start						
T_{SS}	Internal soft-start		1	1.3	1.6	ms
Error amplifier						
V_{FB}	Voltage feedback	T_J = 25 °C	0.845	0.85	0.855	V
		T_J = -40 °C ≤ T_J ≤ 150 °C	0.837	0.85	0.859	V
Overvoltage protection						
V_{OVP}	Overvoltage trip (VOVP/VREF)		115	120	125	%
V_{OVP_HYST}	Overvoltage hysteresis		1	2	6	%

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Synchronization						
f_{CLKIN}	Synchronization range		200		1000	kHz
V_{CLKIN_TH}	Amplitude of synchronization clock		2.3			V
V_{CLKIN_T} (2)	Synchronization pulse ON and OFF-time 2.3 ≤ V_{CLKIN_TH} ≤ 2.5 V	V_{CLKIN_TH} = 2.3 V	60			ns
	Synchronization pulse ON and OFF-time V_{CLKIN_TH} > 2.5 V		20			ns
Power Good						
V_{THR} (3)	PGOOD threshold	T_J = -40 °C ≤ T_J ≤ 150 °C	87	90	93	%
V_{THR_HYST}	PGOOD hysteresis (QFN version only)			3		
V_{PGOOD}	PGOOD open collector output	V_{IN} > V_{INH} and V_{FB} < V_{TH} 4 mA sinking load			0.4	V
		2 < V_{IN} < V_{INH} 4 mA sinking load			0.8	V
T_{SHDWN} (2)	Thermal shutdown temperature			165		°C
T_{HYS} (2)	Thermal shutdown hysteresis			30		°C

1. *Parameters tested in a static condition during the testing phase. The parameter value may change in the presence of a dynamic application condition.*
2. *Not tested in production.*
3. *Specifications in the -40 to +150 °C temperature range are assured by characterization and statistical correlation.*

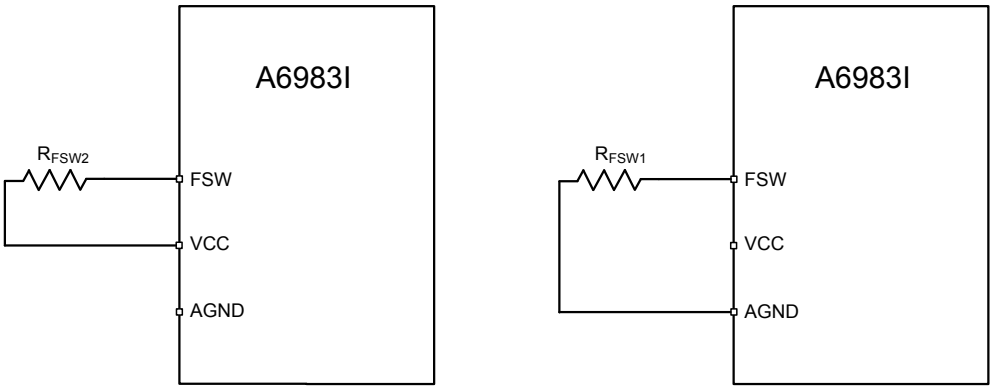
4.1 Frequency selection table

All the populations are tested at T_J = -40 to 150 °C, V_{IN} = 12 V unless otherwise specified.

Table 7. FSW selection for the QFN16 version

Symbol	Option	RVCC (kΩ)	RGND (KΩ)	Min.	Typ.	Max.	Unit
FSW	Dithering	1.8	N.C.		200		kHz
		0	N.C.		400		kHz
		3.3	N.C.		500		kHz
		5.6	N.C.		700		kHz
		10	N.C.		1000		kHz
	No dithering	N.C.	1.8		200		kHz
		N.C.	0	360	400	440	kHz
		N.C.	3.3		500		kHz
		N.C.	5.6	630	700	770	kHz
		N.C.	10	900	1000	1100	kHz

Figure 3. Frequency setting with dithering (left) and without dithering (right)



5 Datasheet parameters over the temperature range

100% of the population in the production flow is tested at three different ambient temperatures (-40 °C, +25 °C, and +150 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C to +150 °C). The device operation is guaranteed when the junction temperature is within the (-40 °C to +150 °C) temperature range. The designer can estimate the silicon temperature increase with respect to the ambient temperature by evaluating the internal power losses generated during the device's operation. However, the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the T_{SHTDWN} (+165 °C typ.) temperature.

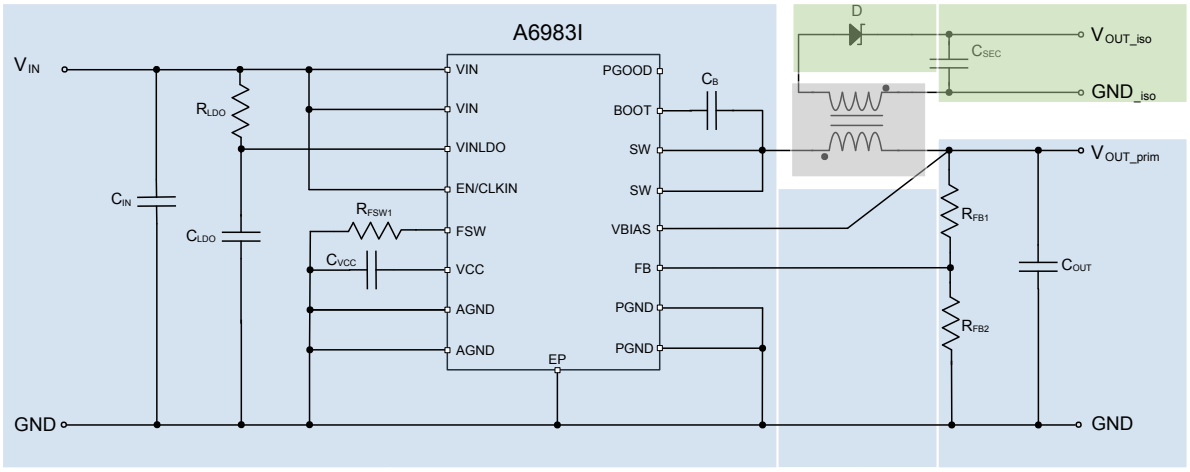
All the datasheet parameters can be guaranteed to a maximum junction temperature of +135 °C to avoid triggering the thermal shutdown protection during the testing phase because of self-heating.

6 Functional description

The iso-buck topology based on the A6983I consists of:

- The primary side: the regulation loop of the peak current mode architecture regulates the primary voltage (blue area in the picture below).
- A two-winding transformer (gray area in the picture below).
- The secondary side: which generates the isolated output voltage (green area in the picture below) given the selected transformer ratio.

Figure 4. Iso-buck general schematic



6.1 Primary side

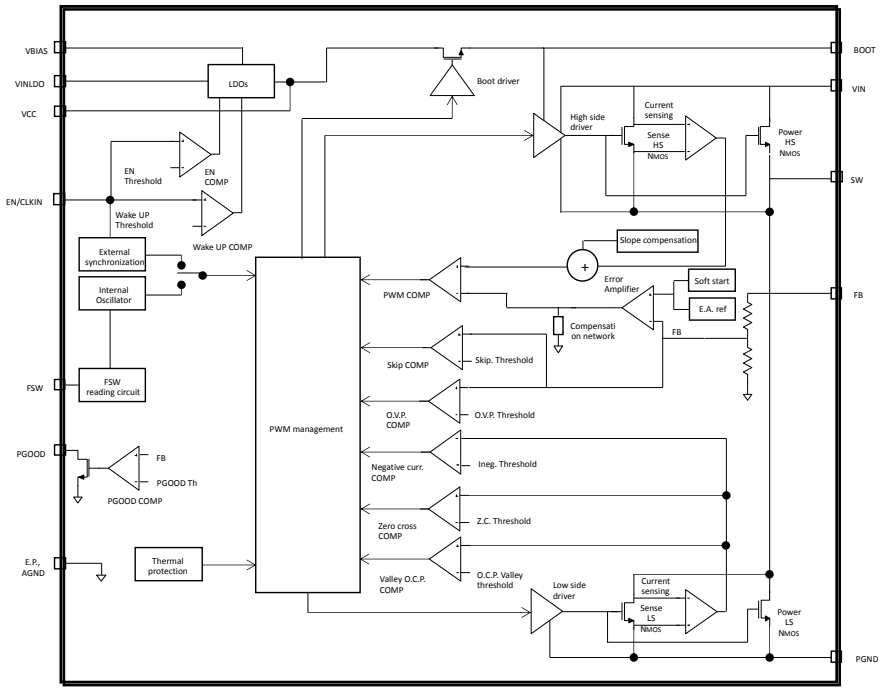
The A6983I device is based on a “peak current mode" architecture with constant frequency control. Therefore, the intersection between the error amplifier output and the sensed inductor current generates the PWM control signal to drive the power switch.

The device operates in forced PWM control, allowing negative currents to flow in the synchronous MOSFET, hence transferring energy to the secondary coil during the off-time.

The main internal blocks are shown in the block diagram in Figure 5:

- Embedded power elements.
- A fully integrated adjustable oscillator, which is able to set five different switching frequencies from 200 to 1 MHz.
- The ramp for the slope compensation, which avoids subharmonic instability.
- A transconductance error amplifier with an integrated compensation network.
- The high-side current sense amplifier to sense the inductor current.
- A “Pulse Width Modulator” (PWM) comparator and the driving circuitry of the embedded power elements.
- The soft-start block ramps up the reference voltage on an error amplifier, thus decreasing the inrush current at power-up. The EN pin inhibits the device when driven low.
- The EN/CLK pin section, which allows the synchronization of the device to an external clock generator.
- The pulse by pulse high-side/low-side switch current sensing to implement the constant current protection.
- A circuit to implement the thermal protection function.
- The OVP circuitry to discharge the output capacitor in case of an overvoltage event.
- The switchover capability of the internal regulator to supply a portion of the quiescent current when the VBIAS pin is connected to an external output voltage.
- Enable/disable dithering operation.

Figure 5. **Block diagram**



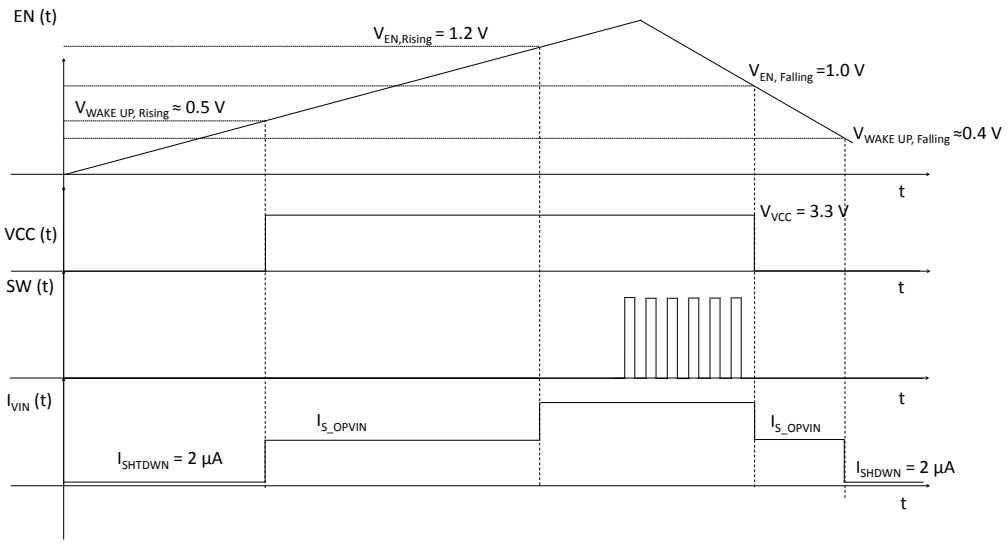
6.1.1 Enable

The EN pin is a digital input that turns the device on or off.

To maximize both the EN threshold accuracy and the current consumption, the device implements two different thresholds:

1. The wake-up threshold, V_{WAKE_UP} = 0.5 V (see Table 6)
2. The start-up threshold, V_{EN} = 1.2 V (see Table 6)

Figure 6. **Power up/down behavior**



When the voltage applied on the EN pin rises over $V_{WAKEUP, RISING}$, the device powers up the internal circuit thus increasing the current consumption.

As soon as the voltage rises over the $V_{EN, RISING}$, the device starts the switching activities as described in Section 6.1.2: Soft-start.

Once the voltage becomes lower than $V_{EN, FALLING}$, the device interrupts the switching activities.

As soon as the voltage becomes lower than $V_{WAKEUP.FALLING}$, the device powers down the internal circuit reducing the current consumption. The pin is V_{IN} compatible.

Refer to Table 6 for the reported thresholds.

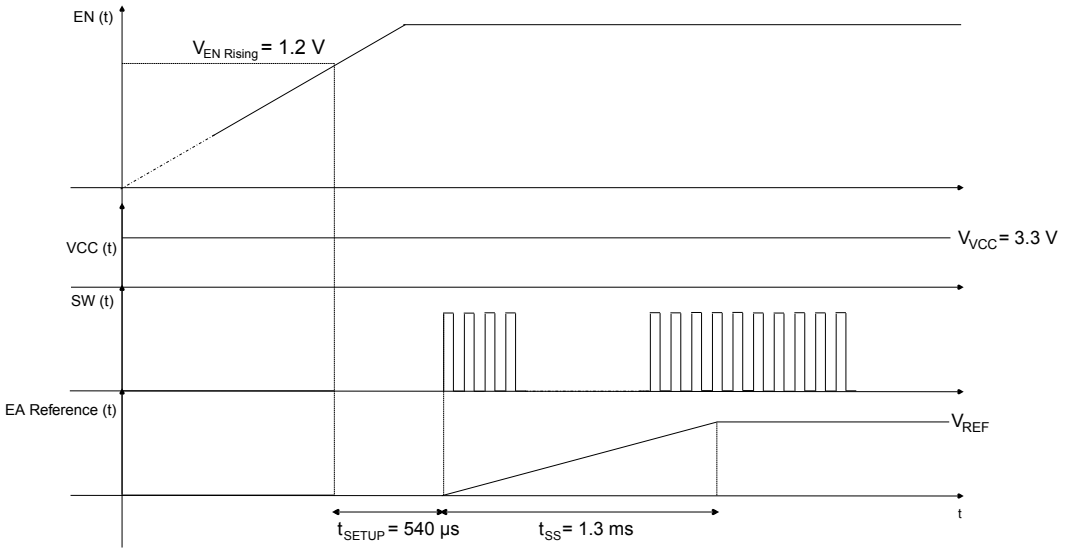
6.1.2 Soft-start

The soft-start (SS) limits the inrush current surge and makes the output voltage increase monotonically.

The device implements the soft-start phase, ramping the internal reference with very small steps. Once the SS ends, the error amplifier reference is switched to the internal value of 0.85 V which comes directly from the band gap cell.

The soft-start duration is fixed and has a typical value of 1.3 ms.

Figure 7. Soft-start procedure

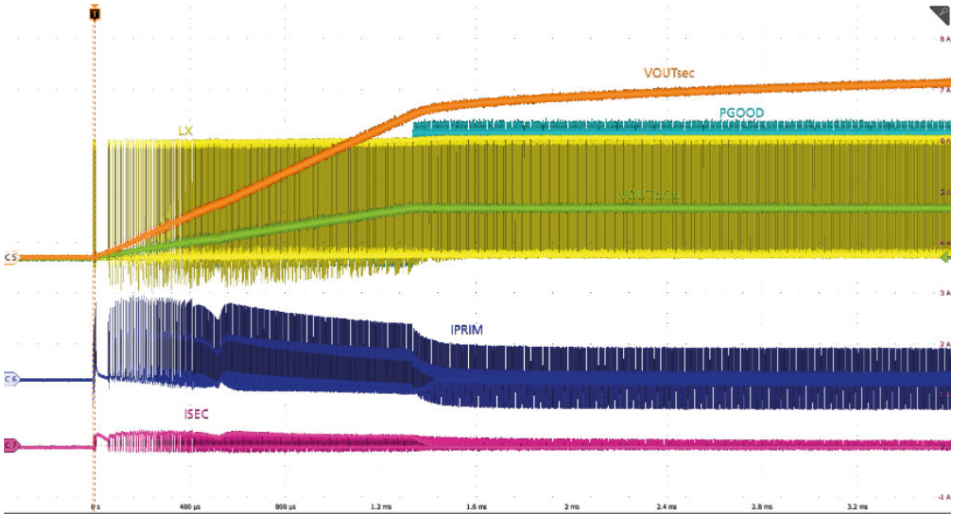


During normal operation, a new soft-start cycle takes place in case of a:

1. Thermal shutdown event
2. UVLO event
3. EN pin rising over the VEN threshold (refer to Table 6)

The device can invert the current even during a soft-start, hence enabling the energy transfer to the secondary winding. Therefore, the secondary isolated output voltage goes up simultaneously with the primary output voltage, thus implementing a tracked soft-start.

Figure 8. **Tracked soft-start on the secondary side**



6.1.3 Undervoltage lockout

The device implements the undervoltage lockout (UVLO) by continuously sensing the voltage on the V_{CC} pin. If the UVLO lasts more than 10 µs, the internal logic resets the device by turning off both the LS and HS.

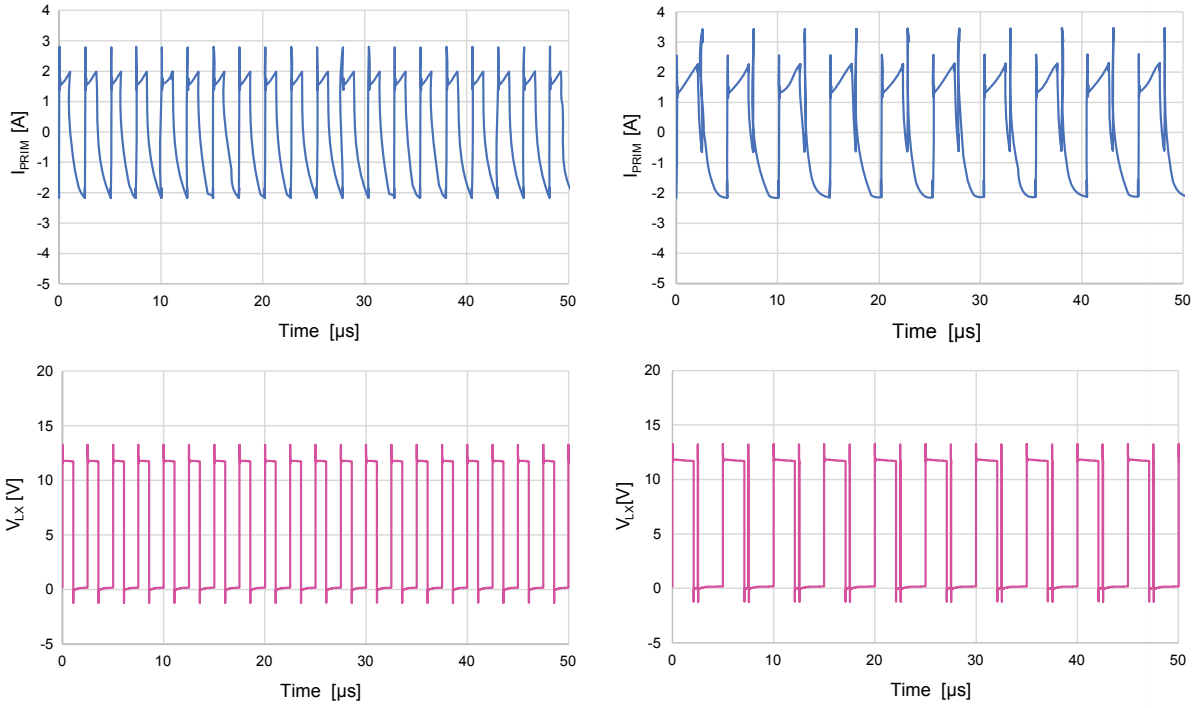
After the reset, if the EN pin is still high, the device repeats the soft-start procedure.

6.1.4 Minimum on-time

The current sense in the high-side MOSFET is not active (masked) for a certain time at the beginning of the ON-time (masking time, from which the parameter $T_{ON\ MIN}$ derives).

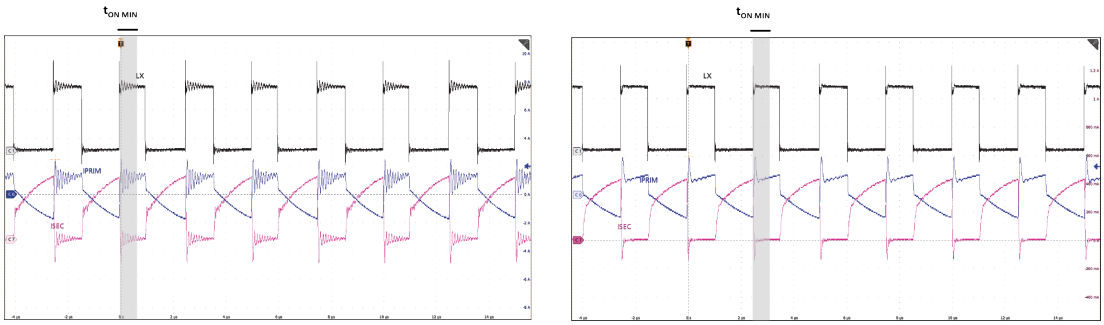
This current sense blanking time is implemented to prevent any primary side pulsed current at the high-side turn-on (resonating with transformer leakage inductance, parasitic capacitances, and reverse junction capacitance of the Schottky diode of the secondary side) from overcoming the EA programmed switch current for the conversion, which would make the conversion unstable (depicted in Figure 9). For the A6983I, the $T_{ON\ MIN}$ has a typical value of 400 ns.

Figure 9. Simulation with different masking times: insufficient (< 100 ns, left) and appropriate (400 ns, right)



Despite the masking time, an RC snubber (for example, across the Schottky diode of the secondary side) is normally recommended to damp oscillations. Figure 10 shows how the RC snubber helps in smothering the remaining oscillations.

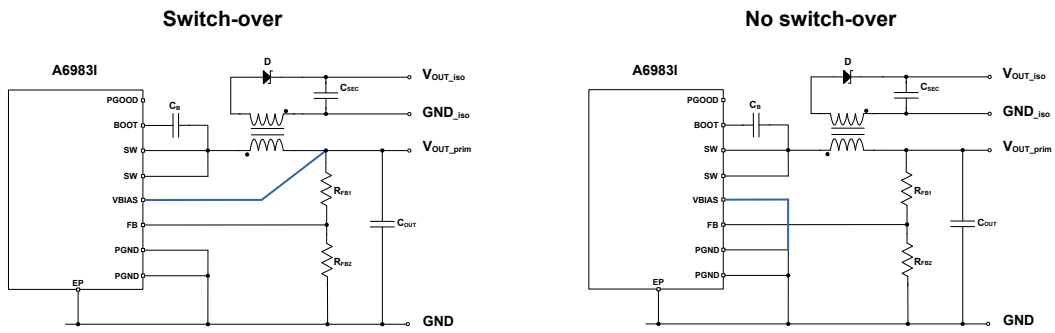
Figure 10. Remaining oscillations (left) and their filtering with RC snubber (right) V_{IN} = 12 V, N = 6, I_{OUTiso} = 200 mA



6.1.5 Switch-over feature

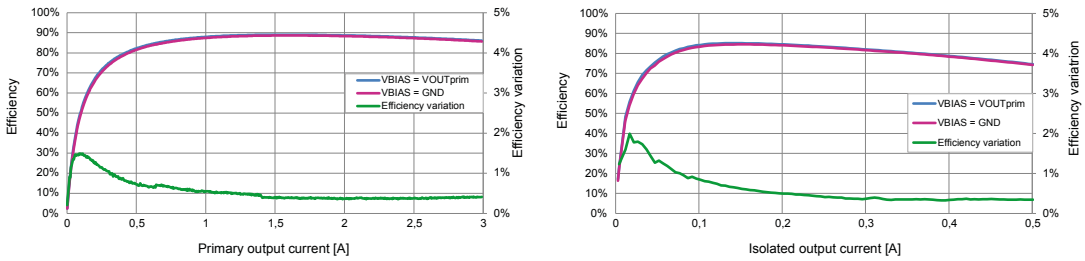
The switch-over (selectable by connecting the VBIAS pin as shown in Figure 11, left) helps improve efficiency, especially at lower currents.

Figure 11. Switch-over selection



The effects on the efficiency for both the primary output and the isolated secondary output are shown in Figure 12.

Figure 12. Effect of the switch-over on efficiency for the primary output (left) and the isolated secondary output (right)



6.1.6 Spread spectrum

The spread spectrum feature, helpful in improving EMC performance, is selectable by connecting the R_{FSW} resistor to the V_{CC} pin (refer to Table 6). The internal dithering circuit changes the switching frequency to a range of ±5%.

$$\Delta F_{SW} = 10\% \cdot F_{sw} \quad (1)$$

The device updates the frequency every clock period by fixed steps:

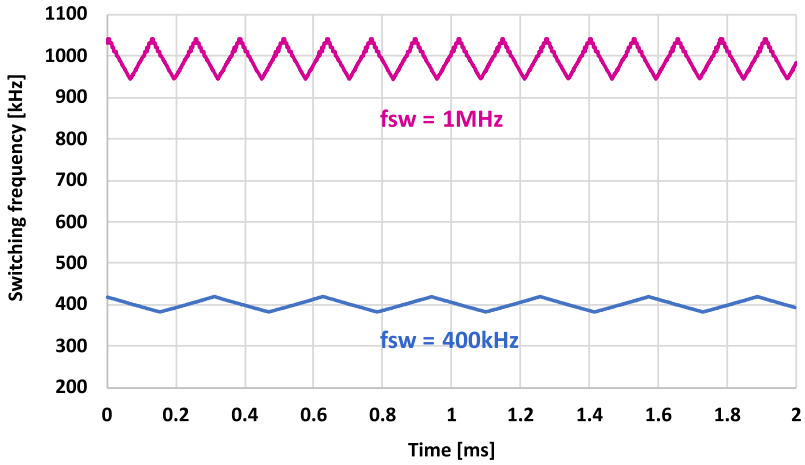
- Ramps-up in 63 steps from minimum to maximum FSW
- Ramps-down in 63 steps from maximum to minimum FSW

The modulation shape is almost triangular with a frequency of:

$$F_{Dithering} = \frac{F_{SW}}{126} \quad (2)$$

A visual explanation about how the switching frequency varies when the spread spectrum feature is used can be observed in Figure 13.

Figure 13. **Switching frequency trend with spread spectrum feature activated**



6.2 Transformer

The transformer is the key component for the iso-buck, ensuring the desired isolation as well as allowing the energy transfer to the secondary side, hence generating the secondary isolated output voltage.

More details about the transformer selection are provided in the dedicated section (see Section 11.2: Transformer selection).

6.3 Secondary side

The secondary side includes an LC filter (secondary winding of the transformer and secondary output capacitor) and the rectifying element (Schottky diode).

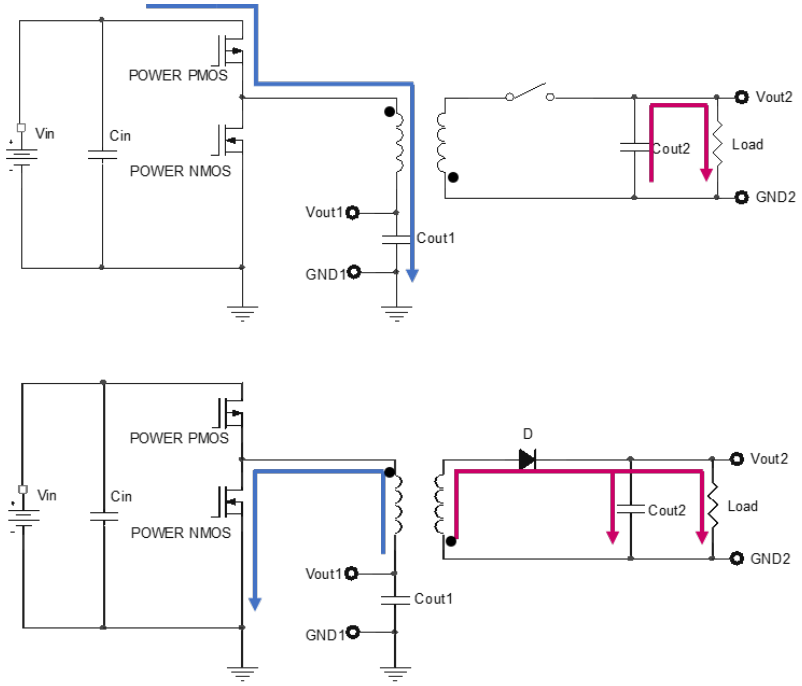
6.4 Iso-buck operation principle

The diagram below describes the operation principle of the iso-buck converter.

When the high-side MOSFET is turned on, the current flows through the primary winding of the transformer and charges the primary output capacitor. Considering the dot convention of the transformer, the voltage at the anode of the Schottky diode is negative, hence the diode is reverse biased and no current flows in the secondary winding. The load connected to the secondary output is supplied by C_{OUT2}.

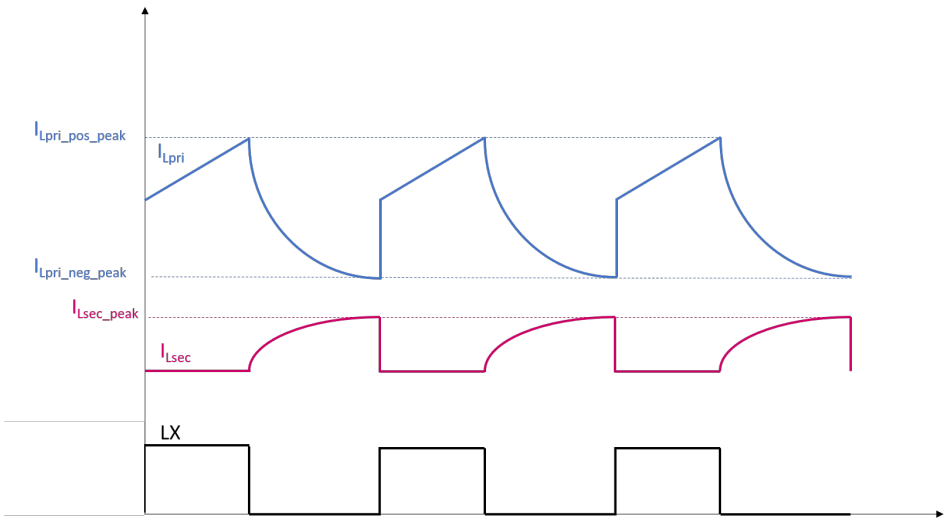
When the low-side MOSFET is turned on, the voltage applied at the transformer winding inverts its polarity. As a consequence, the Schottky diode is now forward biased and allows the current to flow from the secondary winding to C_{OUT} and the load. Under this condition the energy transfer from primary to secondary side occurs.

Figure 14. **Iso-buck basic operating principle**



The waveforms in Figure 15 reproduce the trend of the current in the two windings according to the switch node transitions.

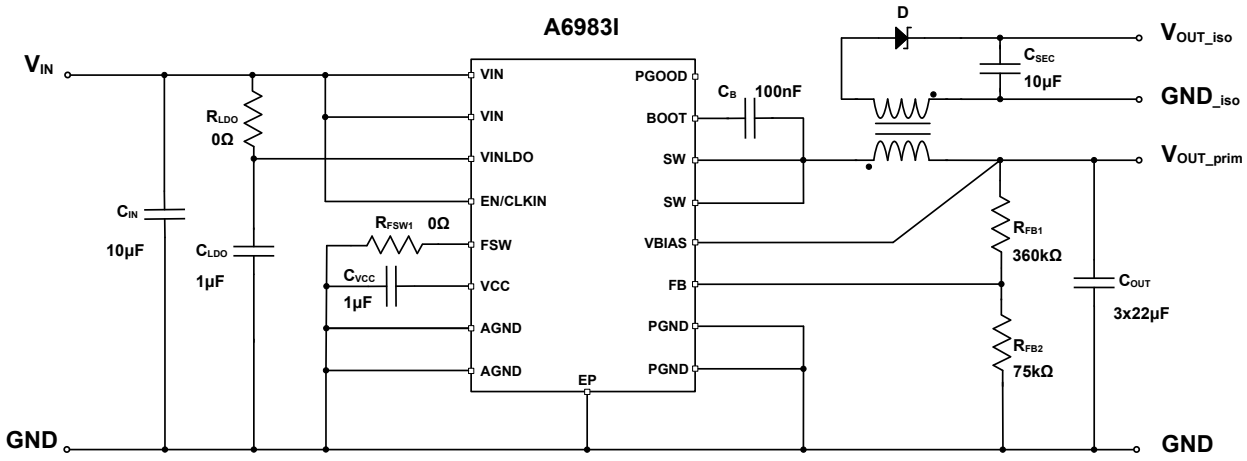
Figure 15. **Iso-buck primary and secondary current waveforms**



7 Iso-buck performance

All results shown in this section come from measurements performed using the reference schematic depicted in Figure 16.

Figure 16. Reference schematic for measurements of line and load regulation and efficiency

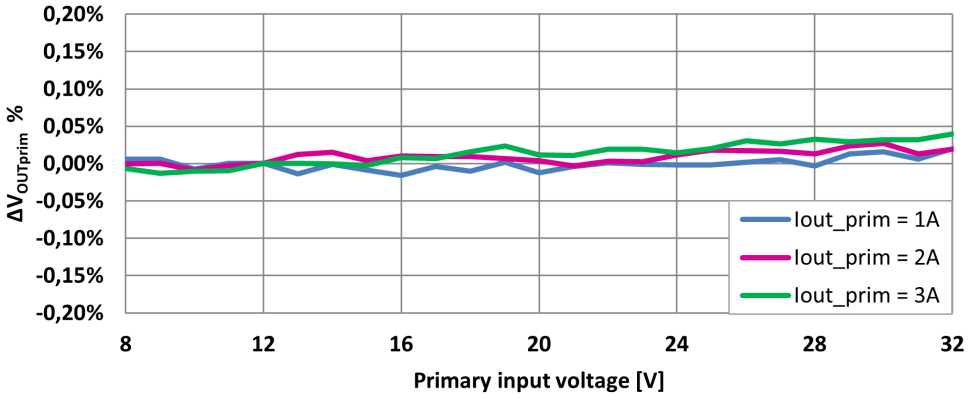


7.1 Output voltage line regulation

Primary output line regulation

The regulator features an enhanced primary line regulation due to the peak current mode architecture. Figure 17 shows the negligible output voltage variation (normalized to the value measured at V_{IN} = 12 V) over an input voltage range up to 32 V for A6983I with $V_{OUT\ prim}$ = 5 V, at three different output currents.

Figure 17. Primary output line regulation

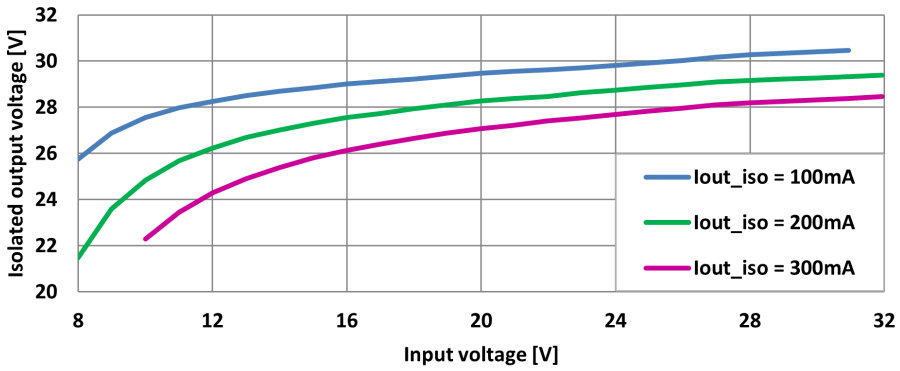


Secondary output line regulation

The secondary output line regulation is defined, similarly to the primary side, as the variation of the secondary output voltage due to the input voltage change at a specific current. The secondary output line regulation is mainly affected by the transformer and in particular by its leakage inductance.

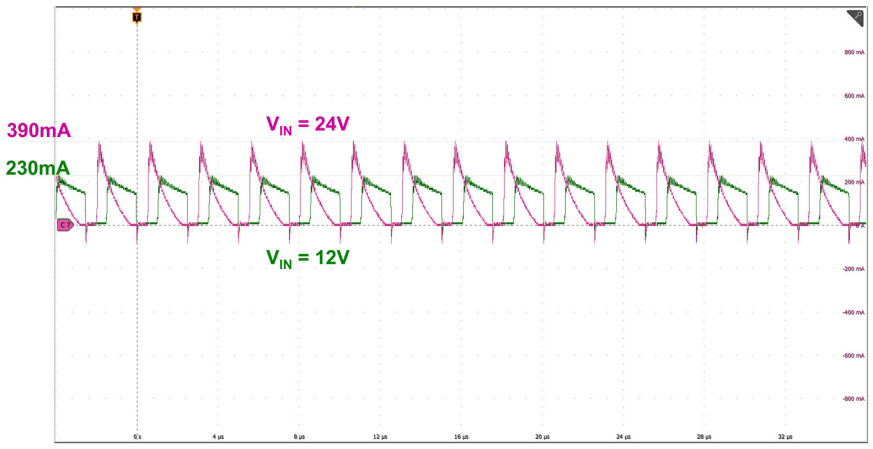
Keeping constant the leakage inductance (that is, using the same transformer), a higher input voltage causes the isolated output voltage to slightly increase, as shown in Figure 18.

Figure 18. Secondary output line regulation



The input voltage value influences the peak current in the secondary winding (see Figure 19), hence determining the amount of energy delivered to the secondary output and, in turn, the isolated output voltage value.

Figure 19. Secondary winding current at different input voltages

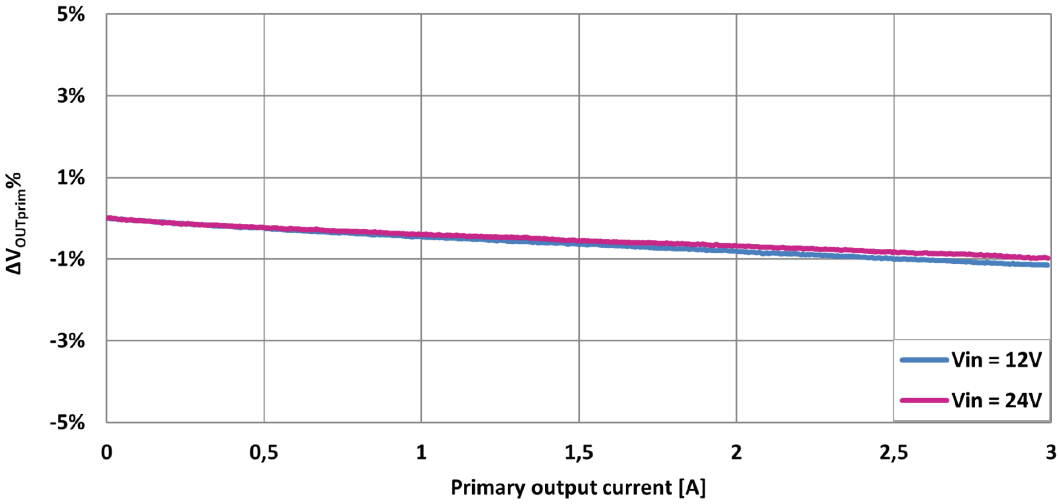


7.2 Output voltage load regulation

Primary output load regulation

Figure 20 shows negligible primary output voltage variation (normalized to the value measured at I_{OUT} = 0 A) over the entire output current range for the A6983I with $V_{OUTprim}$ = 5 V.

Figure 20. Load regulation of the primary not isolated output voltage

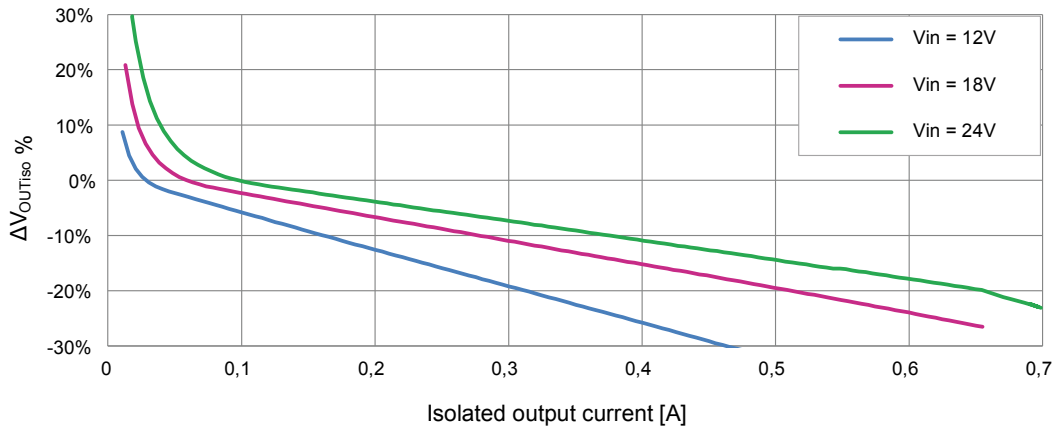


Secondary output load regulation

Since there is not a regulation loop involving the secondary output, its load regulation depends, to some extent, on the primary load regulation and is affected by the leakage inductance of the transformer (see Figure 22). The voltage drops across to the Schottky diode (diode forward voltage) and the DCR of the secondary coil, as indicated by the equation (1) (where only the last two contributions are considered). Minimizing all the mentioned parameters leads to a better load regulation.

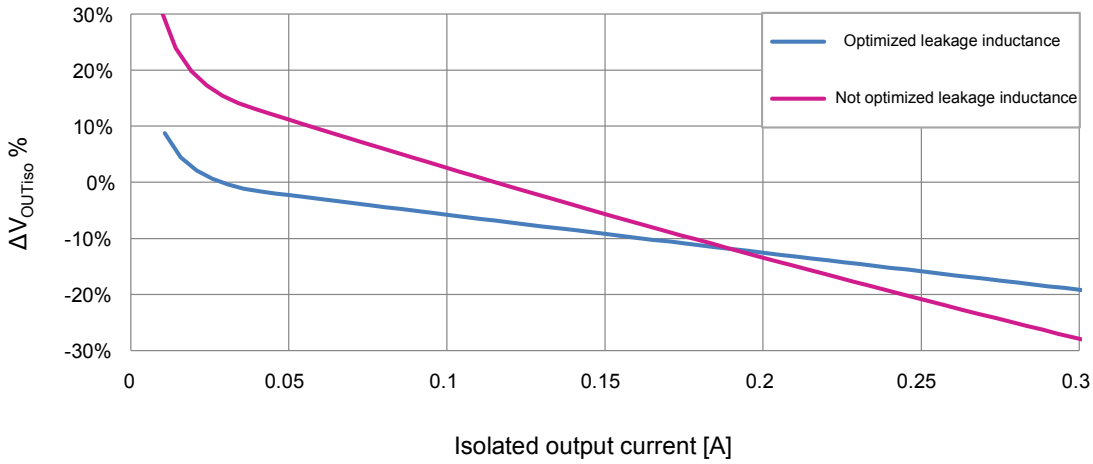
As shown in Section 7.1, the input voltage also plays a role in the isolated output regulation, as depicted by Figure 21.

Figure 21. Load regulation of secondary isolated output voltage



The dependency of the isolated output voltage on the leakage is demonstrated by Figure 22, in which the load regulations with two different transformers are compared. The optimized solution implements the same inductor of the demo board described in Section 12 (ZB1346-AE, whose leakage inductance is around 1% of the magnetizing inductance, as typically recommended). The not optimized solution consists of the use of a transformer with a higher leakage inductance (twice as much the other transformer).

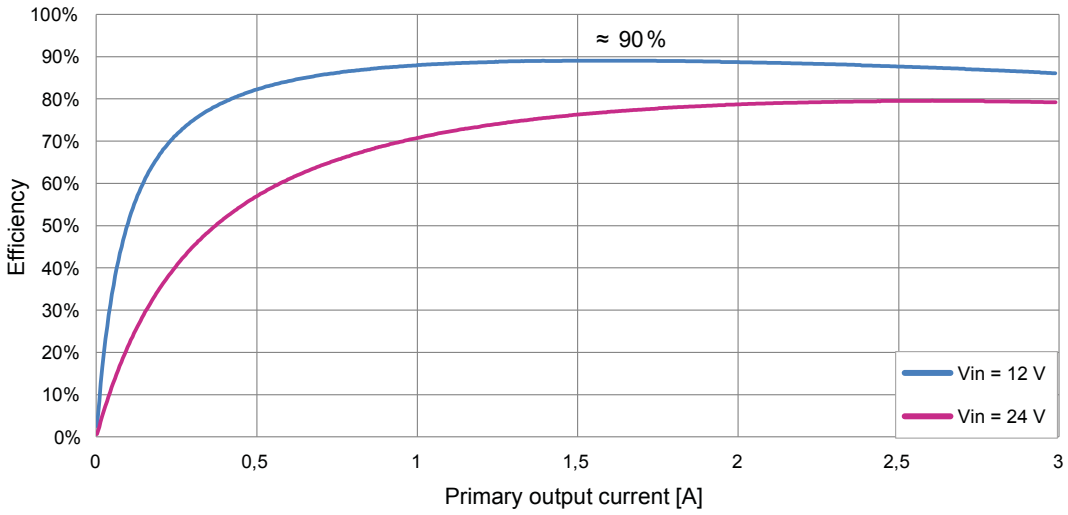
Figure 22. Effect of the transformer leakage inductance on the isolated output load regulation



7.3 Efficiency

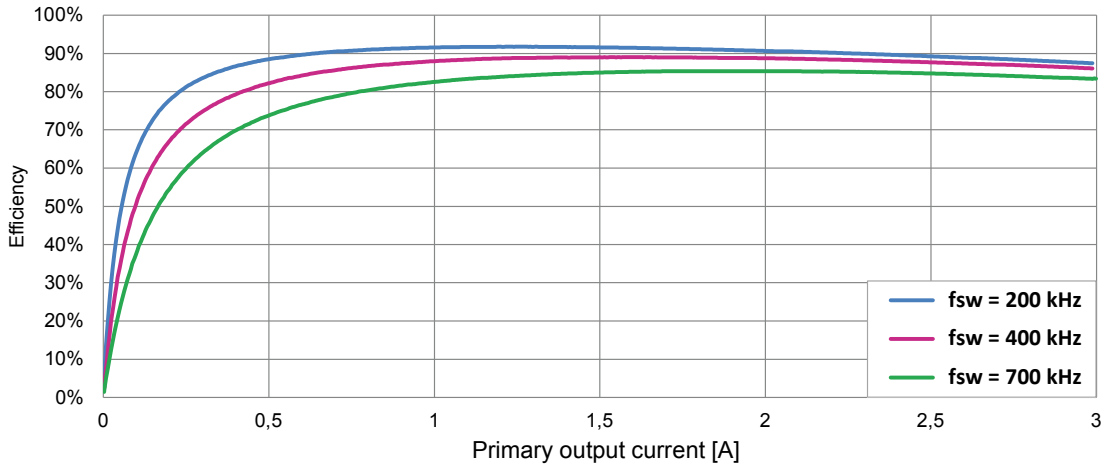
Figure 23 shows the efficiency referred to in the primary output, at two different input voltages, which achieves a peak value of almost 90%.

Figure 23. Primary output efficiency



Instead, Figure 24 compares the efficiency trends depending on the switching frequency, whose effect is dominant at lower currents.

Figure 24. **Primary output efficiency vs. switching frequency**



Secondary isolated output

Figure 25 shows the efficiency referred to in the secondary isolated output at different input voltages, whose effect on the efficiency is more evident at lower currents.

Figure 25. **Secondary isolated output efficiency at different input voltages**

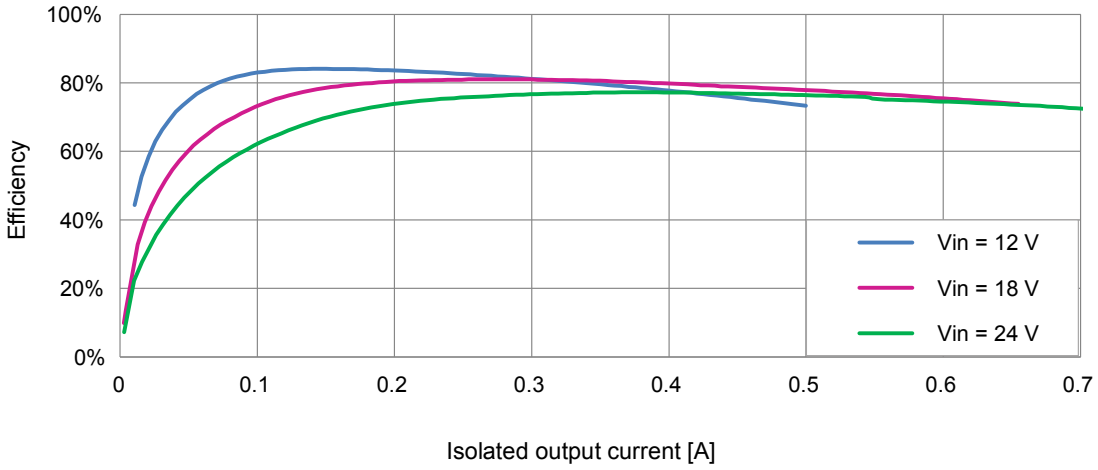
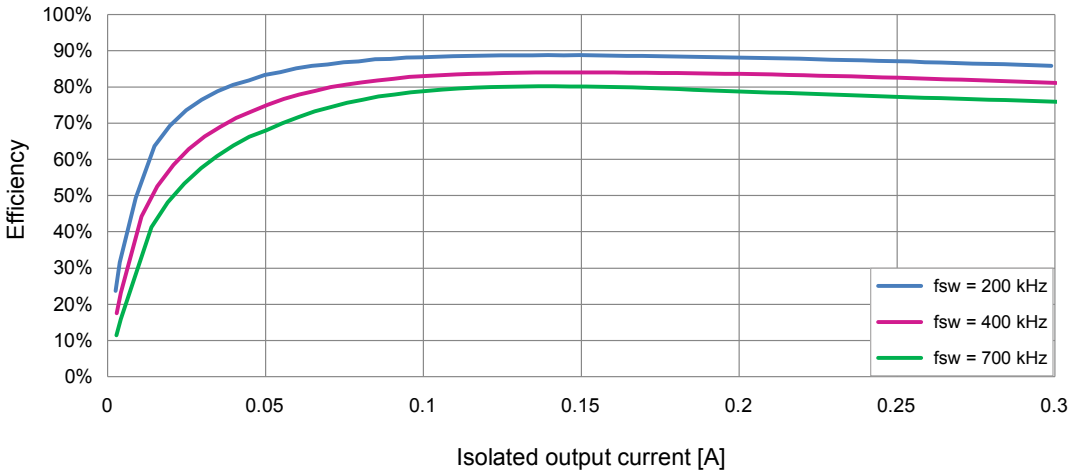


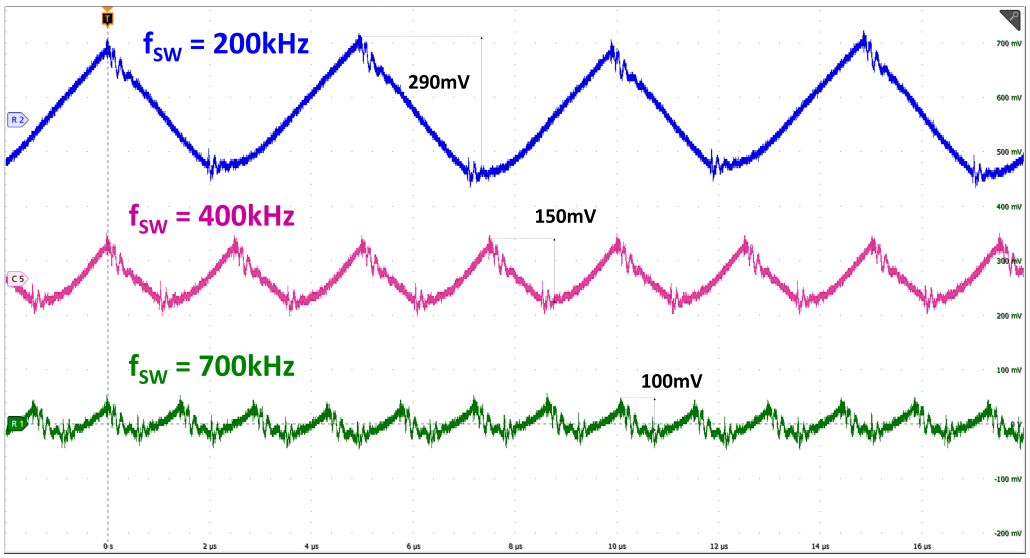
Figure 26 depicts the efficiency variation with the switching frequency. A lower switching frequency contributes to a better efficiency by improving the load regulation (higher isolated output voltage, i.e. higher power), in addition to the obvious lower switching losses.

Figure 26. **Secondary output efficiency vs. switching frequency**



Selecting a lower switching frequency impacts the transformer size and the ripple (see Figure 27) thus requiring a higher output capacitance to reduce it.

Figure 27. **Isolated output voltage ripple vs switching frequency (C_{OUTiso} = 10 µF)**



8 Device protections

8.1 Overvoltage protection

Overvoltage is a second level protection, and it should never be triggered in normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance determined by the compensation network should guarantee an output voltage regulation within the overvoltage threshold even during a worst-case scenario in terms of load transitions.

In the case of an overvoltage event (for the threshold, see the parameter V_{OVP} in Table 6), the device reacts by switching the LS MOSFET on (to discharge the primary output capacitance). This implies that a negative current flows through this MOSFET. This current is limited by the reverse current limit (see parameter I_{VY_SINK} in Table 6, typical value - 4.5 A) to protect the switch. Once this threshold is exceeded, the LS MOSFET is switched off and the current flows through the body diode of the HS MOSFET. At the next clock cycle, if the overvoltage condition persists, the device repeats this procedure.

8.2 Overcurrent protection

Primary side

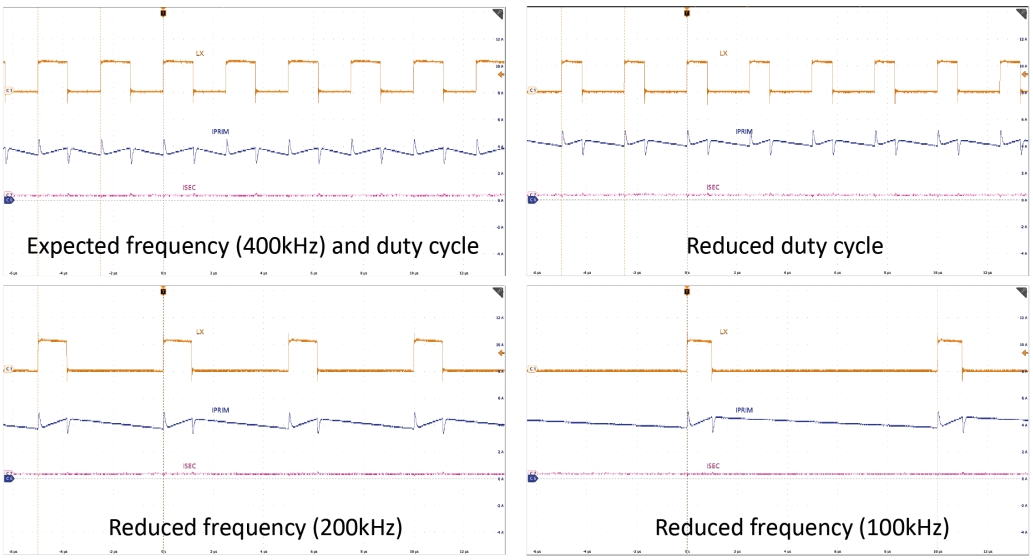
The current protection circuitry features a constant current protection, so the device limits the maximum peak current (refer to Table 6) in an overcurrent condition.

The A6983I device implements a pulse by pulse current sensing on both power elements (high-side and low-side switches) for effective current protection over the duty cycle range. The high-side current sensing is called “peak” and the low-side sensing is called “valley.”

The internal noise generated during the switching activity makes the current sensing circuitry ineffective for a minimum conduction time of the power element. This time is called “masking time” (see Section 6.1.4) because the information from the analog circuitry is masked by the logic to prevent an erroneous detection of the overcurrent event. Therefore, the peak current protection is disabled for a masking time after the high-side switch is turned on. The masking time for the valley sensing (T_{OFF_MIN}, see Table 6) is activated after the low-side switch is turned on. In other words, the peak current protection can be ineffective at extremely low duty cycles, and the valley current protection at extremely high duty cycles.

The A6983I device assures an effective overcurrent protection sensing the current flowing in both power elements. In case one of the two current sensing circuitry is ineffective because of the masking time, the device is protected by sensing the current on the opposite switch. Thus, the combination of the “peak” and “valley” current limits (I_{PK} and I_{VY} respectively) assure the effectiveness of the overcurrent protection even in extreme duty cycle conditions.

Figure 28. Effects of the peak and valley current protections on duty cycle and frequency



The current limit intervention might affect the duty cycle as well as the frequency. Reaching the peak current limit implies a duty cycle reduction (until the T_{ON_MIN} is reached). When the low-side switch is on, as long as the current is above the I_{VY}, any new clock cycle is ignored. The switching frequency is hence reduced. These effects of both duty cycle and switching frequency are summarized as 0.

A short circuit at the primary output is a particular case of overcurrent. Figure 29 shows the behavior of the device in case of a short circuit present before the soft-start.

Figure 29. Soft-start procedure with a short circuit at the primary output

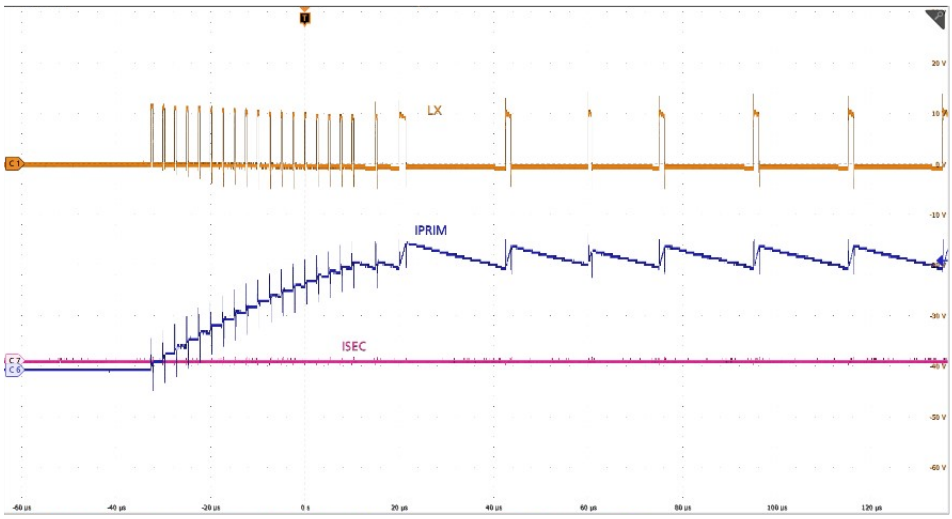
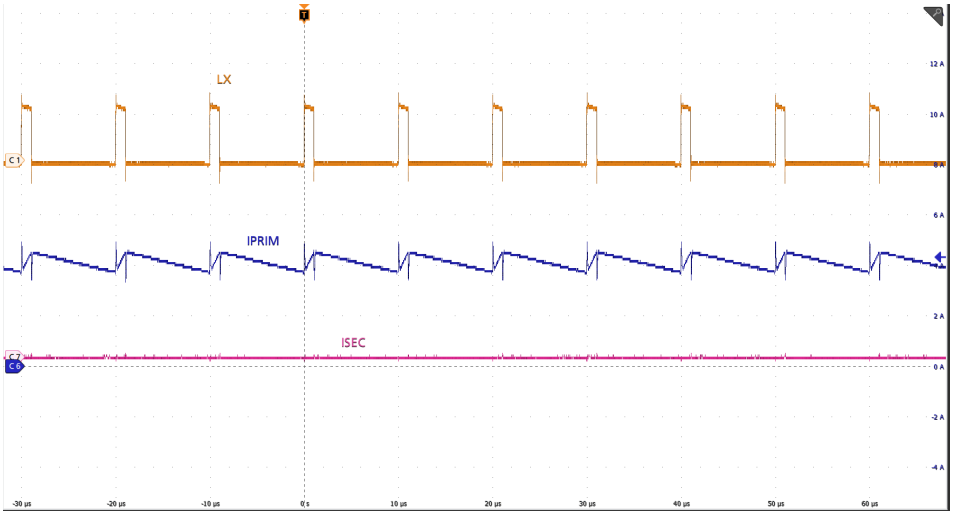


Figure 30 shows a persistent short circuit condition (frequency reduced from 400 kHz to 100 kHz).

Figure 30. Overcurrent procedure in case of persistent short circuit at the primary output



Secondary side

The increase of the secondary output current affects the current shape on the primary side. In particular, the peak currents in the high-side and low-side MOSFETs rise (in absolute value in the low-side, in other words, the current becomes more negative), in accordance with equations (1) and (2).

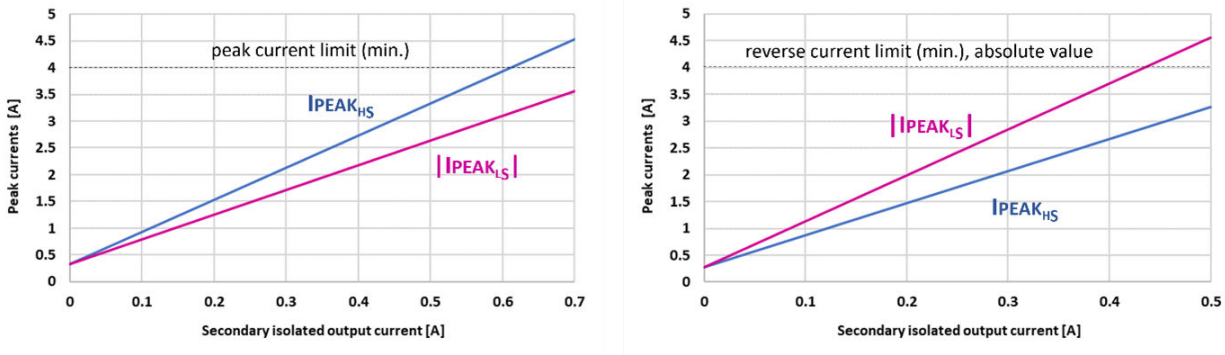
$$I_{PEAK_{HS}} = I_{OUT_pri} + N \cdot I_{OUT_sec} + \frac{\Delta I_L}{2} \quad (3)$$

$$I_{PEAK_{LS}} = -N \cdot I_{OUT_sec} \cdot \left(\frac{2D}{1-D}\right) - \frac{\Delta I_L}{2} + I_{OUT_prim} \quad (4)$$

Where I_{OUT_pri} and I_{OUT_sec} are respectively the primary and secondary output currents, N is the transformer turn ratio, D the duty cycle, and ΔI_L is the current ripple in the primary winding.

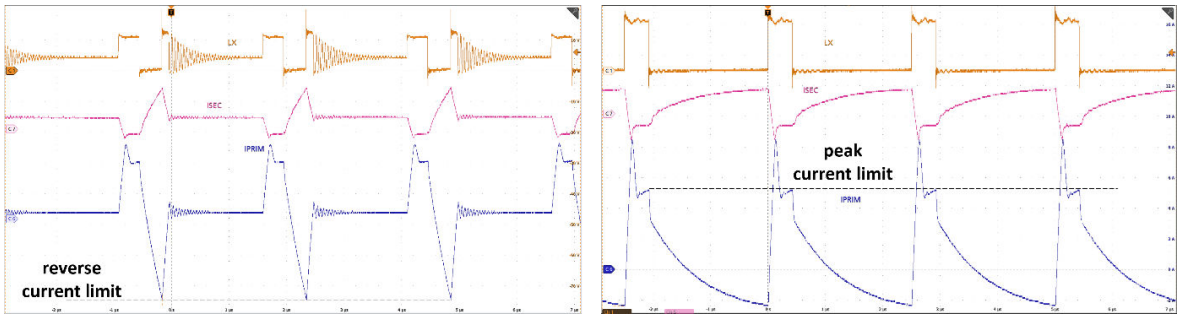
Figure 31 depicts how these peak currents vary depending on the secondary output current, under the specified conditions.

Figure 31. Peak currents in LS and HS MOSFET depending on the isolated output current



Depending on the application conditions (e.g. duty cycle and therefore the input voltage), the peak or the reverse current limit can be first exceeded and thus represents the limit of the secondary isolated output current (see Figure 32).

Figure 32. Left: V_{IN} = 12 V, I_{PRIM} first exceed I_{VY_SINK}. Right: V_{IN} = 18 V, I_{PRIM} first exceeds I_{PK}



The crossing of the peak current limit implies the procedure explained in Section 7.1.

If instead the reverse current limit is exceeded, the device manages this condition as described in Section 8.1 for the overvoltage protection.

Once the reverse current limit is crossed, the device turns the LS MOSFET off and the current flows in the body diode of the HS MOSFET until it reaches zero. Both HS and LS MOSFET remain off until the next clock cycle.

8.3 Thermal shutdown

The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold (T_{SHDWN}, refer to Table 6). The thermal sensing element is close to the power elements, assuring fast and accurate temperature detection. A hysteresis of approximately 30 °C prevents the device from turning ON and OFF too fast. After a thermal protection event expires, the A6983I restarts with a new soft-start.

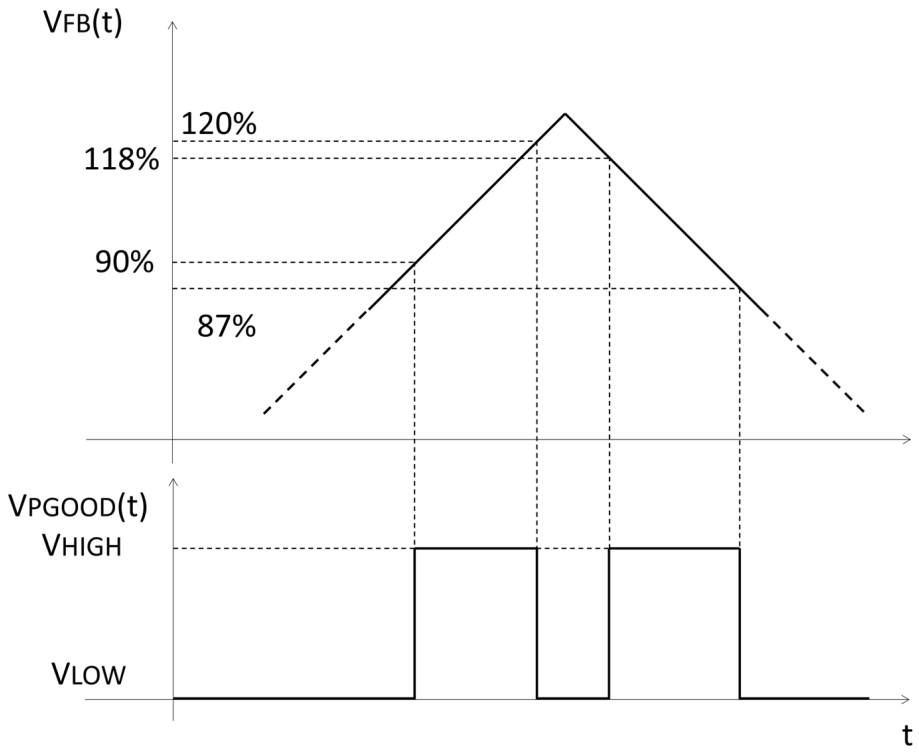
8.4 Power Good

The PGOOD pin indicates whether the output voltage is within its regulation level. The pin output is an open drain MOSFET. The PGOOD is pulled low when:

- The FB pin voltage is lower than 90% (typ.) of the nominal internal reference for more than 10 µs.
- The FB pin voltage is higher than 120% (typ.) of the nominal internal reference for more than 10 µs (see Section 7.1).
- During the soft-start procedure also with a precharged VOUT.
- If a thermal shutdown event occurs.
- If a UVLO event occurs.

The PGOOD pin is VIN compatible.

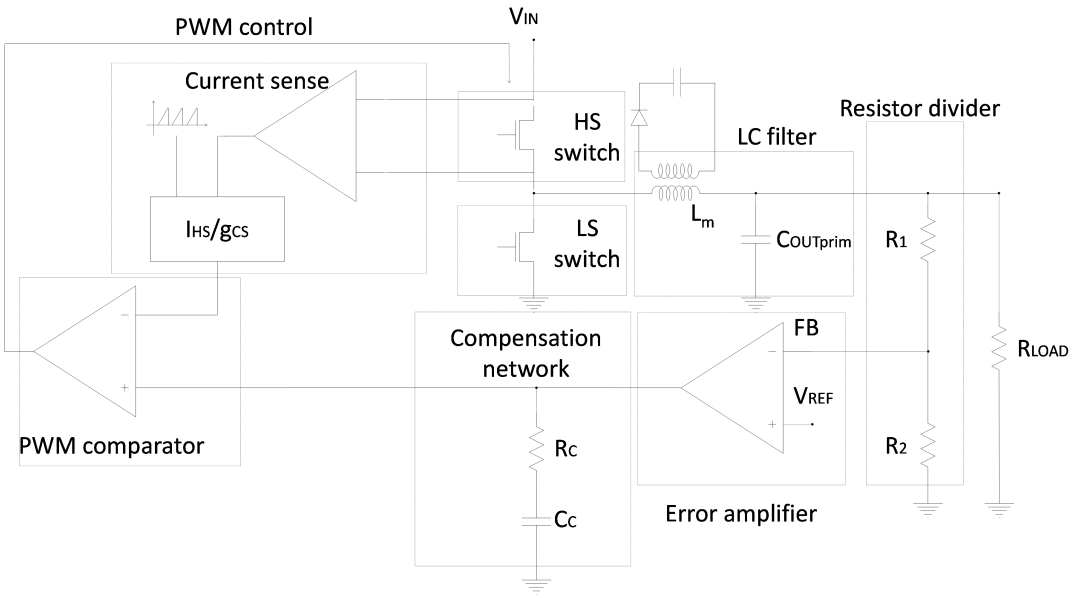
Figure 33. PGOOD thresholds



9 Closing the loop

The iso-buck, compared to a standard buck, includes the transformer in the place of the inductor and all the components connected to the secondary winding (at least the Schottky diode and the secondary output capacitor). Nevertheless, the regulation loop does not include the secondary side components. As a first approximation, the control loop of an iso-buck can be assimilated to the one of a standard buck. Therefore, the block diagram in the figure below can be still used (where the inductor symbol identifies the inductance of the primary winding) as well as all the equations and calculations in the next sections.

Figure 34. Block diagram of the loop



9.1 $G_{CO}(s)$ control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter is written as follows:

$$G_{CO}(s) = R_{LOAD} \cdot g_{CS} \cdot \frac{1}{1 + \frac{R_{LOAD} \cdot T_{SW}}{L} \cdot [m_C \cdot (1-D) - 0.5]} \cdot \frac{\left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)} \cdot F_H(s)$$

Where R_{LOAD} represents the load resistance, the g_{CS} equivalent sensing transconductance of the current sense circuitry, ω_P the single pole introduced by the power stage, and the ω_Z zero given by the ESR of the output capacitor. $F_H(s)$ considers the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}}$$

$$\omega_P = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1-D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}}$$

Where:

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = I_{SLOPE} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \end{cases}$$

Where I_{SLOPE} is equal to 1 A.

S_n represents the on-time slope of the sensed inductor current, S_e the on-time slope of the external ramp that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

The sampling effect contribution F_H (s) is:

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}}$$

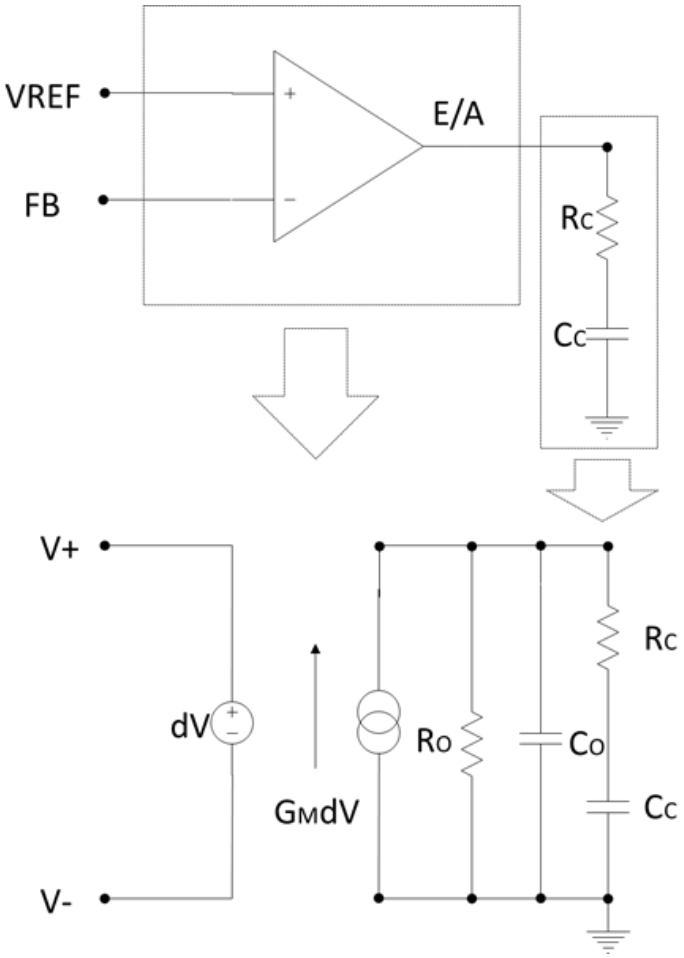
Where:

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]}$$

9.2 Error amplifier compensation network

The following figure shows the typical compensation network required to stabilize the system.

Figure 35. Transconductance embedded error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. The transfer function of the error amplifier and its compensation network is:

$$A_O(s) = \frac{A_{VO} \cdot (1 + s \cdot R_C \cdot C_C)}{s^2 \cdot R_O \cdot C_O \cdot R_C \cdot C_C + s \cdot (R_O \cdot C_C + R_O \cdot C_O + R_C \cdot C_C) + 1}$$

Where:

$$A_{VO} = G_m \cdot R_O$$

The poles of this transfer function are (if $C_C >> C_O$):

$$f_{PLF} = \frac{1}{2 \cdot \pi \cdot R_O \cdot C_C}$$

$$f_{PHF} = \frac{1}{2 \cdot \pi \cdot R_O \cdot C_O}$$

Whereas the zero is defined as:

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_C}$$

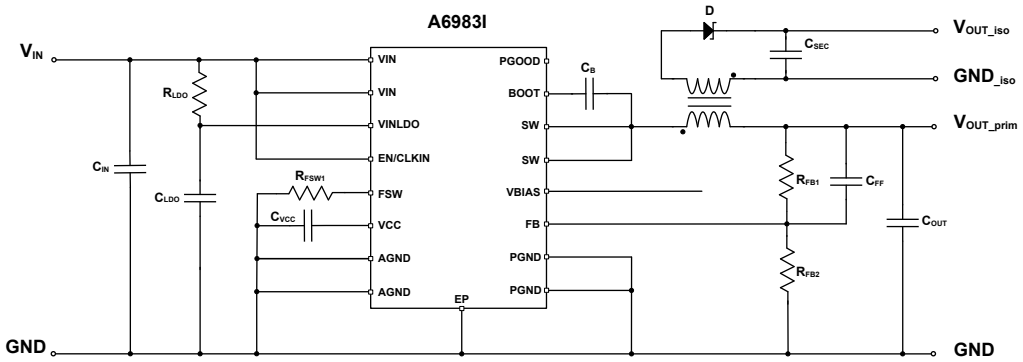
9.3 Voltage divider

The contribution of a simple voltage divider is:

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2}$$

A small signal capacitor in parallel to the upper resistor (only for the adjustable part number) of the voltage divider implements a leading network ($f_{ZERO} < f_{POLE}$), sometimes necessary to improve the system phase margin:

Figure 36. Contribution of the resistor divider



The Laplace transform of the leading network:

$$\boldsymbol{G_DIV}\left(\boldsymbol{s}\right) = \frac{\boldsymbol{R_2}}{\boldsymbol{R_1 + R_2}} \cdot \left(\left(1 + \boldsymbol{s} \cdot \boldsymbol{R}_1 \cdot \boldsymbol{C}_\boldsymbol{R}1\right)\right) / \left(\left(1 + \boldsymbol{s} \cdot \frac{\boldsymbol{R_1} \cdot \boldsymbol{R_2}}{\boldsymbol{R_1 + R_2}}\right) \cdot C_R1\right)$$

Where:

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_{R1}}$$

$$f_P = \frac{1}{2 \cdot \pi \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}}$$

$$f_Z < f_P$$

So, closing the loop, the loop gain is:

$$G(s) = G_{DIV}(s) \cdot G_{CO}(s) \cdot A_O(s)$$

10 Application notes

10.1 Output voltage adjustment

Primary output voltage

The error amplifier reference voltage is 0.85 V typical. The primary output voltage is adjusted accordingly to the equation below:

$$V_{OUT_prim} = 0.85 \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \quad (5)$$

Where R_{FB1} and R_{FB2} are the resistors used in the output divider (see Figure 37).

Figure 37. Primary output voltage regulation

A general recommendation is to keep the duty cycle below 50 to 60%. A higher duty cycle would limit off-time, limiting the time in which the energy transfer to the secondary side takes place.

Other restrictions in the duty cycle selection arise due to the minimum on-time (see Section 9.2), generally summarized by the following equation:

$$D \geq D_{MIN} = T_{ON\ MIN} \cdot f_{SW} \quad (6)$$

Secondary output voltage

In the iso-buck converter, the secondary output voltage is not included in the regulation loop. Nevertheless, a good regulation of the secondary output voltage is achieved by relying on the primary output voltage regulation, and the selection of a proper turn ratio of the transformer. Other influencing parameters are the voltage drops due to the secondary winding resistance and the Schottky diode, as well as the leakage inductance of the transformer. This is summarized by the following equation:

$$V_{OUT_sec} = N \cdot [V_{OUT_prim} + I_{OUT_{pri}} \cdot (R_{DS(on\ LS} + R_{wind_pri})] \cdot \frac{L_m}{L_m + L_{LEAK}} - R_{wind_sec} \cdot I_{OUT_sec} - V_{FD1} \quad (7)$$

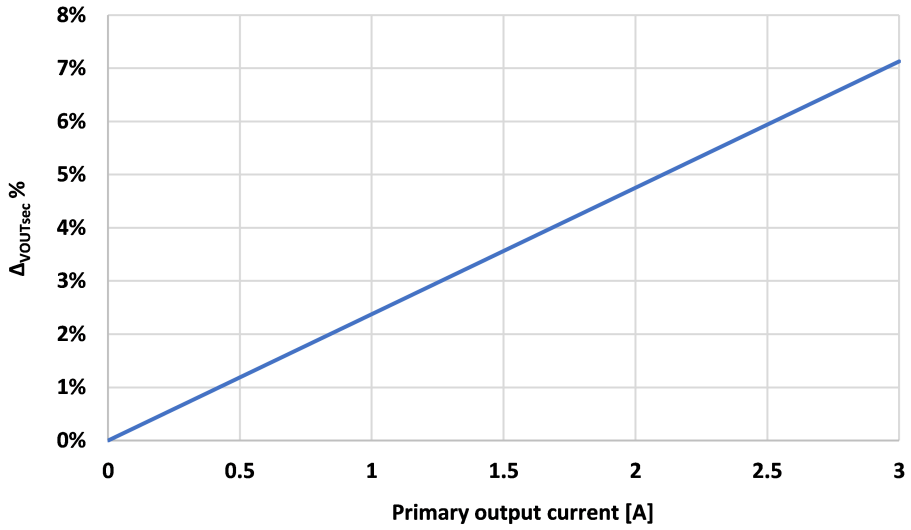
Where N is the turn ratio, R_{wind_prim} and R_{wind_sec} are the winding resistances of the primary and secondary sides respectively, V_{FD1} is the forward voltage of the Schottky diode, L_m is the magnetizing inductance of the transformer, and L_{LEAK} is the leakage inductance of the transformer.

If no current is drawn from the primary output, the equation (24) can be simplified as follows:

$$V_{OUT_sec} = N \cdot V_{OUT_{prim}} \cdot \frac{L_m}{L_m + L_{LEAK}} - R_{wind_sec} \cdot I_{OUT_sec} - V_{FD1} \quad (8)$$

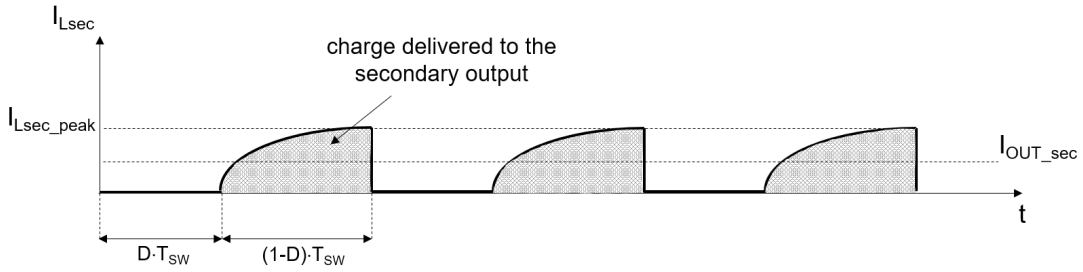
The equation (25) emphasizes how the selection of the transformer and, to some extent, the Schottky diode plays a crucial role in the accurate regulation of the secondary output voltage. The figure below shows instead the effect of the current drawn from the primary output on the isolated voltage, as described by the equation (25).

Figure 38. **Isolated voltage variation due to the primary output current**



Another factor affecting the secondary output voltage regulation is the leakage inductance of the transformer. As described later on, the leakage inductance determines the peak current that can be reached in the secondary winding. This peak current defines the maximum current from the secondary isolated output by limiting the amount of charge delivered to the output. When the current demand from the secondary isolated output exceeds the maximum deliverable charge limited by the peak current, the isolated output voltage drops.

Figure 39. **Secondary output current**



The effect of the leakage on the load regulation is shown in Figure 22 in Section 6.2.

Additionally, to some extent, the duty cycle can affect the secondary output voltage. Since the energy transfer from primary to secondary occurs only during the T_{OFF}, a too high duty cycle could reduce the achievable peak current, hence limiting the deliverable current to the secondary output. Under this condition, the secondary output could drop.

10.2 Switching frequency

A resistor connected to the FSW pin features the selection of the switching frequency (refer to Table 7). Connecting the resistor between the pins FSW and VCC, the internal dithering circuit is turned on (see Figure 3). The selection of the switching frequency must take into account the minimum on-time of the device ($T_{ON\ MIN}$, as indicated in Table 6), as described by the following equation:

$$f_{SW_max} \leq \frac{V_{OUT}}{T_{ON\ MIN} \cdot V_{IN} \cdot \eta} \quad (9)$$

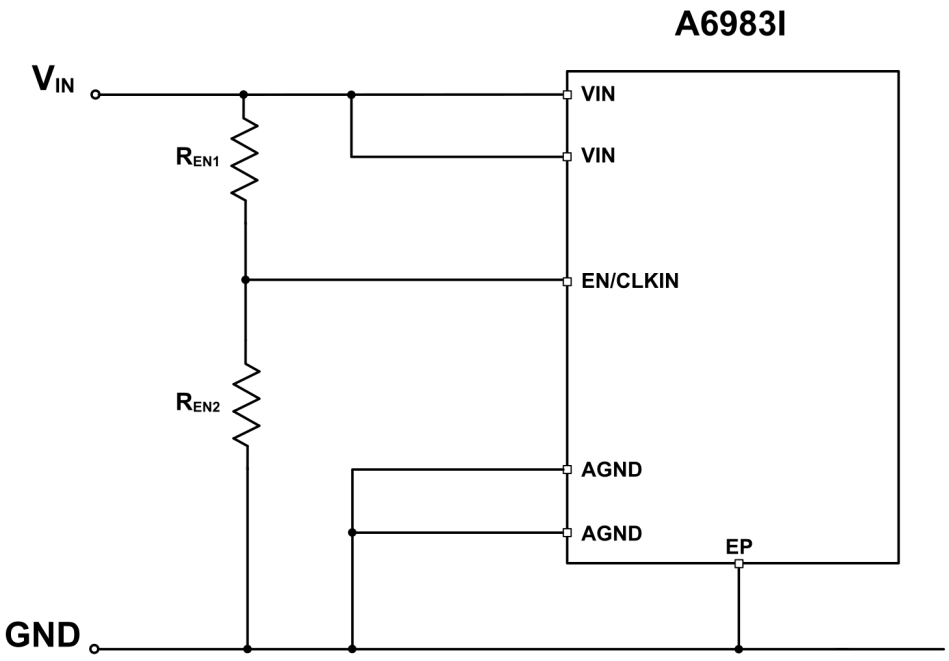
The switching frequency affects the selection of the primary inductance as well as the transformer construction. The efficiency also varies with the switching frequency (see Figure 24 and Figure 26).

10.3 Programmable power-up threshold

The enable rising threshold is equal to 1.2 V typical (refer to Table 6). The power-up threshold is adjusted according to the following equation:

$$V_{Power\ UP} = 1.2 \cdot \left(1 + \frac{R_{EN\ 1}}{R_{EN\ 2}}\right) \quad (10)$$

Figure 40. Programming the power-up threshold



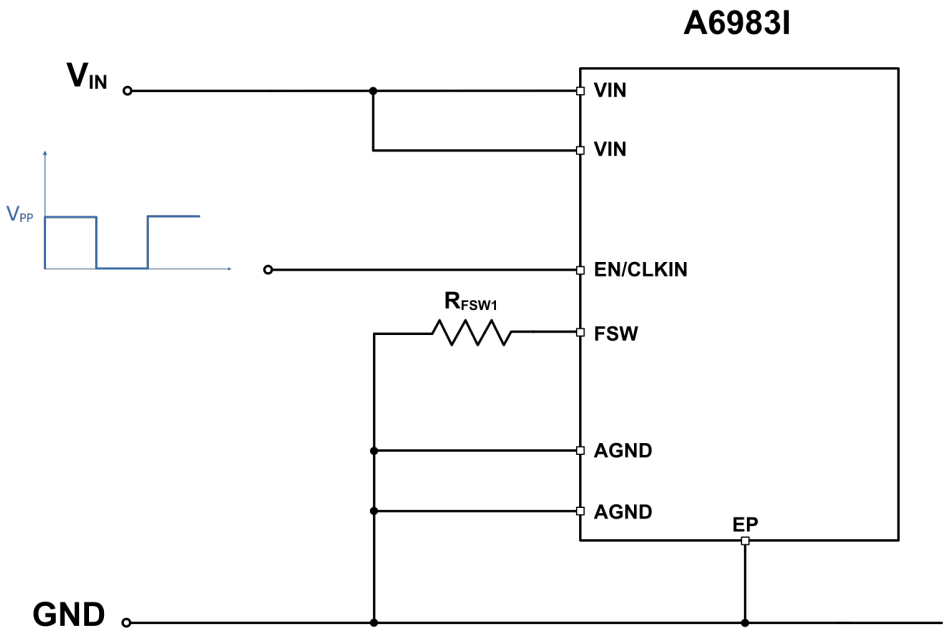
The enable falling threshold is equal to 1.0 V typical (refer to Table 6). The turn-off threshold is obtained according to the following equation:

$$V_{Power\ Down} = 1.0 \cdot \left(1 + \frac{R_{EN\ 1}}{R_{EN\ 2}}\right) \quad (11)$$

10.4 Output external synchronization

The device allows a direct connection between a clock source and the EN/CLKIN pin.

Figure 41. External synchronization (direct connection)



The device internally implements a low-pass filter connected to the EN/CLKIN pin that is able to acquire the average value of the applied signal.

The device turns on when the average of the signal applied is higher than V_{EN} rising (refer to Table 6). The device turns off when the average of the signal is lower than V_{EN} falling (refer to Table 6).

Considering, for example, a clock source with V_{PP} = 5.0 V, the minimum duty cycle to guarantee the power-up is given by:

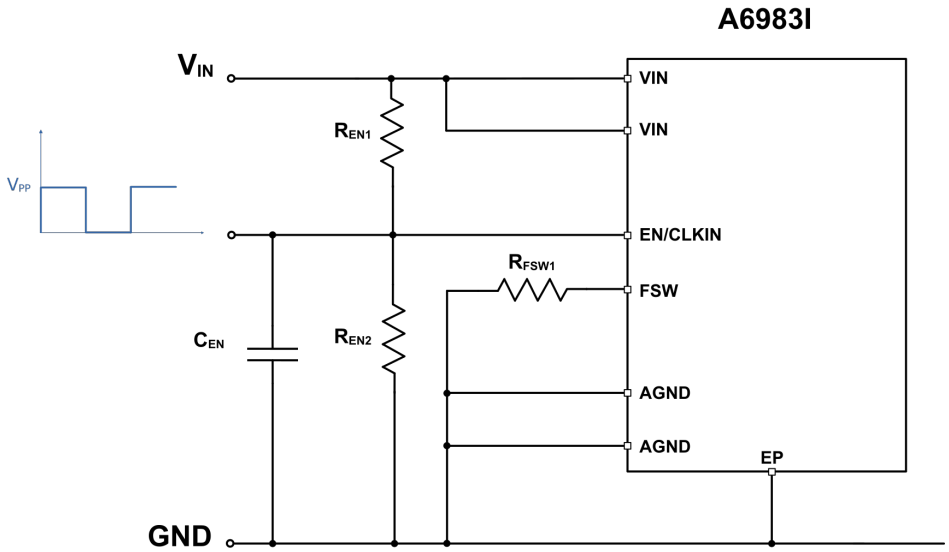
$$\mathrm{Duty}_{\mathrm{min}} = \frac{V_{\mathrm{EN,\,Rising}}}{V_{\mathrm{PP}}} = 0.24 \quad (12)$$

The maximum duty cycle to guarantee turn-off is given by:

$$\mathrm{Duty}_{\mathrm{MAX}} = \frac{V_{\mathrm{EN,\,Falling}}}{V_{\mathrm{PP}}} = 0.2 \quad (13)$$

The device also allows for an AC coupling.

Figure 42. **External synchronization (AC coupling)**



The AC coupling allows the device to keep the power-up and down thresholds defined by the partition connected to the EN/CLKIN pin and described in Section 9.3.

The following table resumes the minimum pulse duration for the external signal and maximum duty cycle that allows the synchronization by keeping the selected power-up and down thresholds.

V_{PP} [V]	TON, MIN, EXT $_{Clock}$ [ns]	DMAX, EXT$_{Clock}$ [%]
2.3	60	45
3.3	20	30
5	20	20

The minimum amplitude for the external clock signal is, for both the configurations, equal to 2.3 V.

The network given by C_{EN} and R_{ENL} sets a high-pass filter. Considering a resistor in the order of 220 kΩ, a capacitor equal to 1 nF is the correct choice.

11 Design of the external components

11.1 Input capacitor selection

The input capacitor, just like in a standard buck, should limit the input voltage ripple. Key parameters of the input capacitor are, together with its value, the maximum operating voltage and the RMS current capability.

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity, a pulsed current flows into the input capacitor and so its RMS current capability must be selected accordingly with the application conditions. Internal losses of the input filter depend on the ESR value, so usually low ESR capacitors (like multilayer ceramic capacitors) have higher RMS current capability. On the other hand, given the RMS current value, a lower ESR input filter has lower losses and so it contributes to a higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

$$I_{RMS}=\left(I_{OUT_pri}+\frac{I_{OUT_sec}}{N}\right)\cdot\sqrt{\left(1-\frac{D}{\eta}\right)\cdot\frac{D}{\eta}} \quad (14)$$

In the ideal case of efficiency η = 1, the RMS current reaches its maximum value when D = 0.5.

In general, the maximum and minimum duty cycles can be calculated as:

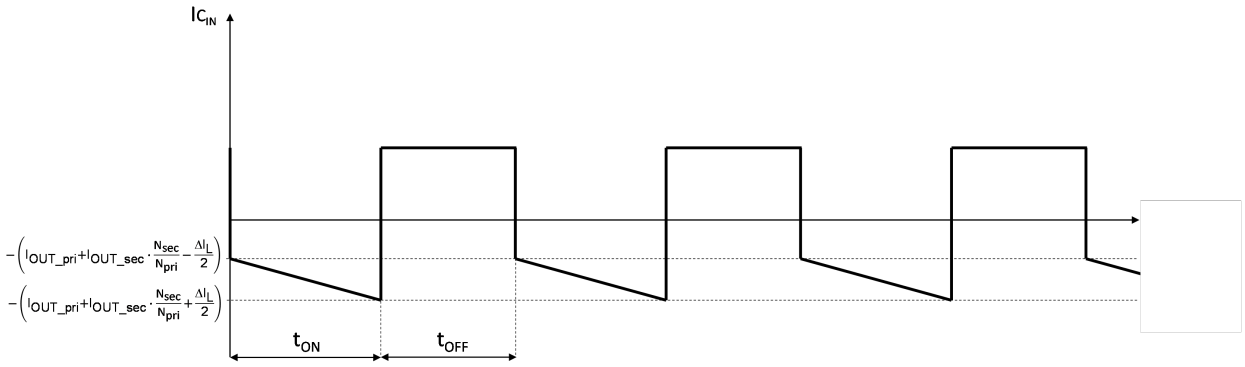
$$D_{MAX}=\frac{V_{OUT_pri}+\Delta V_{LS}}{V_{INmin}+\Delta V_{LS}-\Delta V_{HS}} \quad (15)$$

$$D_{MIN}=\frac{V_{OUT_pri}+\Delta V_{LS}}{V_{INmax}+\Delta V_{LS}-\Delta V_{HS}} \quad (16)$$

Where ΔV_{HS} and ΔV_{LS} are the voltage drops across the high-side and low-side MOSFETs respectively.

The AC component of the input current (see Figure 43) flows in the input capacitor, generating the input voltage ripple.

Figure 43. Input capacitor AC current



The peak to peak voltage across the input capacitor can be calculated as follows:

$$V_{PP}=\left(\frac{I_{OUT_pri}+I_{OUT_sec}\cdot\frac{N_{sec}}{N_{pri}}}{C_{IN}\cdot f_{SW}}\right)\cdot\frac{D}{\eta}\cdot\left(1-\frac{D}{\eta}\right)+ESR\cdot\left(I_{OUT_pri}+I_{OUT_sec}+\frac{\Delta I_L}{2}\right) \quad (17)$$

In the case of a negligible ESR (for example, in the case of MLCC capacitors) the equation (6) can be simplified. The value of the input capacitor can be calculated as follows:

$$C_{IN}=\frac{I_{OUT_pri}+I_{OUT_sec}\cdot\frac{N_{sec}}{N_{pri}}}{V_{PP}\cdot f_{SW}}\cdot\frac{D}{\eta}\cdot\left(1-\frac{D}{\eta}\right) \quad (18)$$

Considering the ideal case of η = 1, the equation above reaches its maximum value when D = 0.5. Therefore, the minimum input capacitance value can be defined as follows:

$$C_{IN} \geq C_{INmin} = \frac{I_{OUT_pri} + I_{OUT_sec} \cdot \frac{N_{sec}}{N_{pri}}}{4 \cdot V_{PP} \cdot f_{SW}} \quad (19)$$

Typically, C_{IN} is dimensioned to keep the maximum peak to peak voltage across the input filter in the order of 5% V_{INMAX}.

To minimize the spike on the V_{IN} pins (1 and 12) caused by the stray inductance and the pulsed input current, it is strongly recommended to add, for each one, a filter capacitor. A 1 µF capacitor with a 0603 footprint is a good choice.

11.2 Transformer selection

The transformer has two essential tasks:

- Providing isolation between the primary and secondary sides in accordance with the application requirements.
- Generating the necessary secondary output voltage from the regulated primary voltage with the most suitable turn ratio.

The transformer selection implies defining the following parameters:

- Isolation voltage
- Turn ratio
- Primary inductance
- Peak and RMS currents
- Windings resistance
- Leakage inductance
- Parasitic capacitances

Isolation voltage

Isolation of the transformer in terms of voltage capability (1.5 kV, 4 kV, and so on) and type (functional basic, reinforced, etc.) is mainly driven by the application. Both parameters normally affect the size of the transformer as well as other electrical characteristics (e.g. winding resistance, leakage inductance, etc.).

Turn ratio

Naming N_{pri} and N_{sec} the number of turns of the primary and secondary windings respectively, the turn ratio is so defined:

$$N = \frac{N_{sec}}{N_{prim}} \quad (20)$$

Considering equation (11), the turn ratio must be defined so that the voltage at the secondary output is the desired one over the whole secondary output current range:

$$N \geq \frac{V_{OUT_sec} + R_{wind_sec} \cdot I_{OUT_sec} + V_{FD1}}{V_{OUT_pri} + I_{OUT_{pri}} \cdot \left(R_{DS(on)LS} + R_{wind_pri}\right)} \quad (21)$$

If no current is drawn from the primary output, the turn ratio should be only chosen to compensate for the drops due to the secondary winding resistance and the Schottky diode.

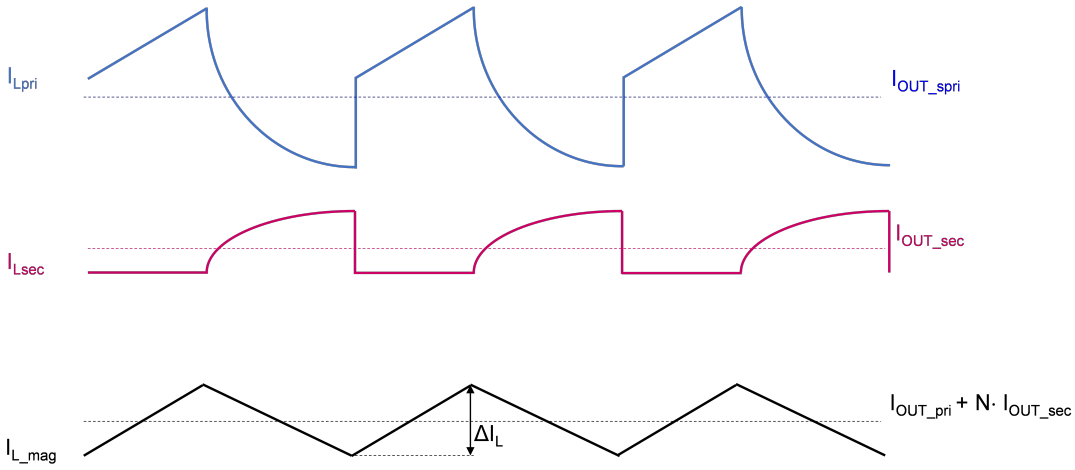
The effect of the leakage inductance on the secondary output voltage regulation (not included in the equation above) should be taken into account, too. Figure 17 clearly shows how the secondary output voltage can drift due to the leakage inductance.

Primary inductance

The choice of the primary inductance does not differ much from a standard buck. The magnetizing current (see Figure 44), which combines the two winding currents, has the same shape as the buck inductor current and can be defined as:

$$I_{L_mag} = I_{pri} + N \cdot I_{sec} \quad (22)$$

Figure 44. Primary winding current (blue), secondary winding current (magenta), and magnetizing current (black)



Therefore, setting the current ripple ΔI_L, the inductance is defined as:

$$L_{pri} = \frac{(V_{IN} - V_{OUT_prim}) \cdot V_{OUT_prim}}{V_{IN} \cdot f_{SW} \cdot \Delta I_L} \quad (23)$$

For example, assuming I_{OUT_prim} = 500 mA, I_{OUT_sec} = 100 mA, N = 6, the current ripple can be set around 30% of the total current I_{OUT_pri} + N < I_{OUT_sec} = 1.1 A, therefore 330 mA. If V_{IN} = 12 V, V_{OUT_prmi} = 5 V and f_{SW} = 400 kHz, the inductor value should be 22 µH.

Peak and RMS current

As any inductor, the peak and RMS current for each winding must be calculated to define the saturation and the RMS current that the transformer should fulfill.

For the primary winding, the equations below are valid:

$$I_{pri_pos_peak} = I_{OUT_pri} + \frac{I_{OUT_sec}}{N} + \frac{\Delta I_{pri}}{2} \quad (24)$$

$$I_{pri_RMS} = \left(I_{OUT_pri} + \frac{I_{OUT_sec}}{N}\right) \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta I_{pri} \cdot N}{N \cdot I_{OUT_pri} + I_{OUT_sec}}\right)} \quad (25)$$

For the secondary winding, the peak current can change depending on the leakage inductance. In the picture below, the secondary winding current waveforms with different leakage inductances are simulated. It is evident how the peak current can significantly vary. Considering the target leakage inductance value for an iso-buck (recommended up to 1% of the primary inductance), the waveform can be approximated with a sawtooth shape and the peak and the RMS current can be hence estimated as:

$$I_{sec_pos_peak} = \frac{2 \cdot I_{OUT_sec}}{1 - D} \quad (26)$$

$$I_{sec_RMS} = I_{sec_pos_peak} \cdot \sqrt{\frac{1 - D}{3}} \quad (27)$$

Equation (16) gives an indication about the peak value. Nevertheless, the waveform can significantly change with the leakage. Therefore, the measured peak value can differ from the one provided by this equation.

A duty cycle higher than 50 to 60% significantly increases the peak current in the secondary winding, hence affecting the negative peak current on the primary side.

Winding resistance

Winding resistances should be minimized as much as possible since they affect the secondary output load regulations.

They also contribute to power losses, hence affecting the efficiency of the total solution.

Leakage inductance

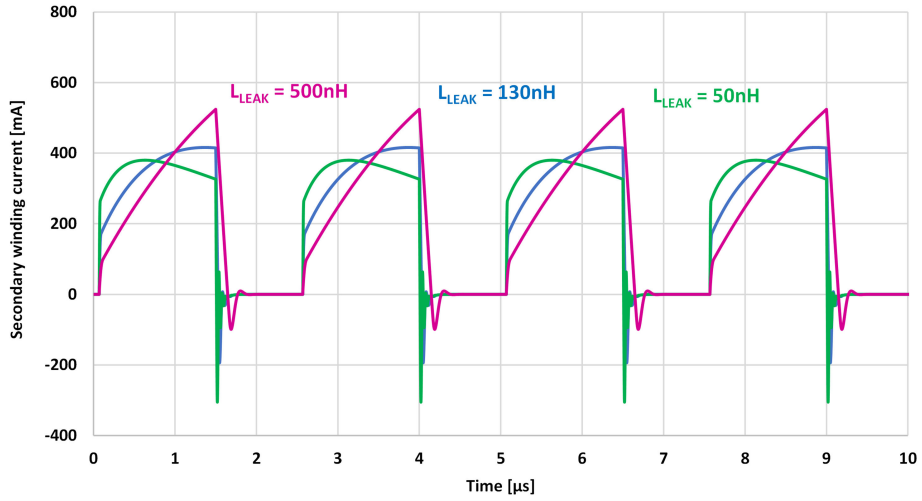
The leakage inductance of a transformer can be defined as an undesired inductive component due to the imperfect magnetic linking of the two windings. Leakage inductance is inherent to the transformer construction and can be only reduced, but not eliminated.

As shown in Figure 45, the leakage inductance affects the shape of the secondary winding current. In general, a very low leakage inductance implies that the current in the secondary winding can quickly ramp-up allowing the charge of the secondary output capacitor and supporting the load current demand.

A high leakage inductance slows down the secondary winding current rise, limiting the charge delivery to the output. Comparing solutions with different values of transformer leakage inductance shows that higher leakage inductance transformers are characterized by poorer load regulation performances (as already depicted in Figure 22).

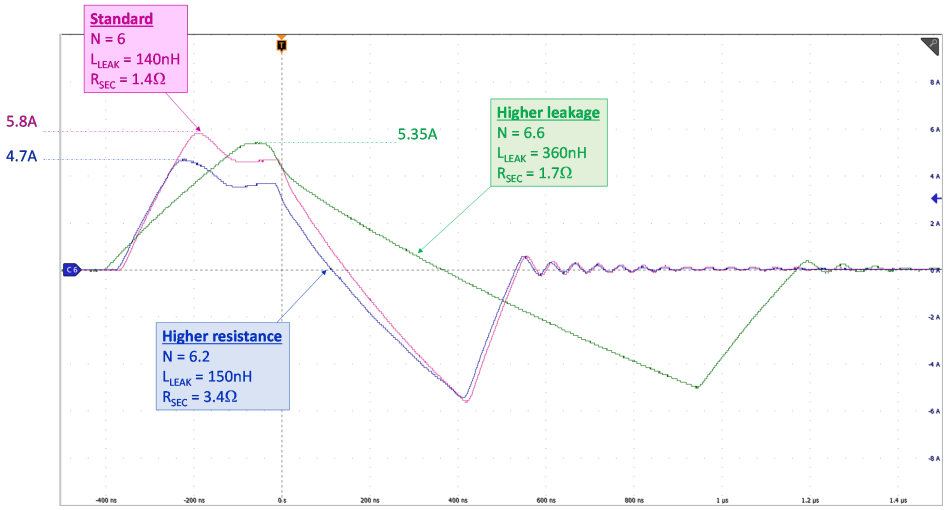
On the other hand, the leakage inductance determines the slope of the rising edge of current in the primary winding (the lower is the leakage, the steeper the slope) and the peak value it could reach. Therefore, under certain conditions (e.g. short circuit on the secondary side) this peak can be significantly high.

Figure 45. Impact of the leakage inductance on the secondary winding peak current



A higher value of the leakage can help in these cases, however, jeopardizing the load regulation performances. A similar effect can also be achieved by increasing the resistance of the secondary winding, keeping the optimized value of the inductance. In both cases it is also possible to adjust the N value to improve the load regulation (see Figure 46). Both higher leakage and higher secondary winding resistance have a slight negative impact on the efficiency.

Figure 46. Primary winding current peak reduction with higher leakage or higher secondary winding resistance

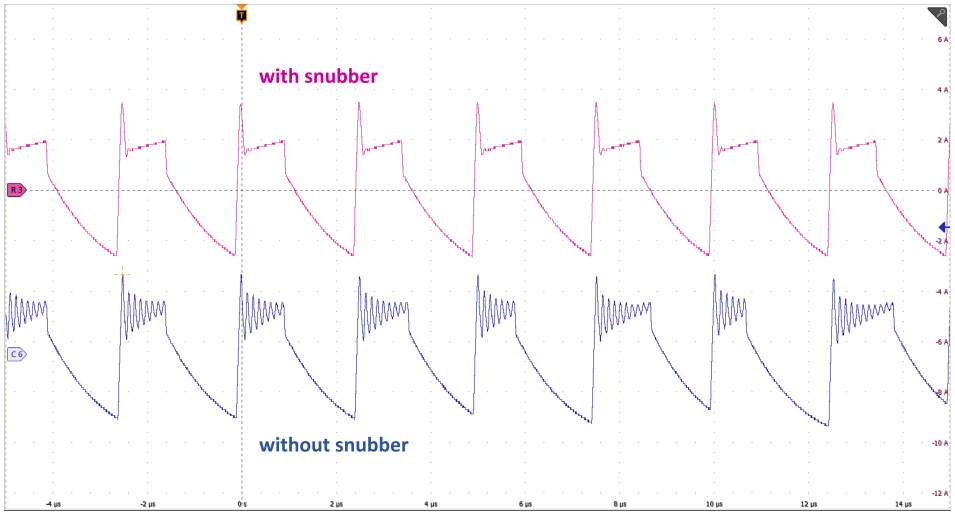


Another effect of the leakage inductance is the ringing observed when the transition from the off-phase to on-phase occurs. These oscillations are due to the LC circuit represented by the leakage inductance and the total parasitic capacitance observed by the primary winding. This capacitance consists of several contributions:

- Primary winding capacitance
- Secondary winding capacitance, reflected on the primary side
- Reverse capacitance of the Schottky diode, reflected on the primary side

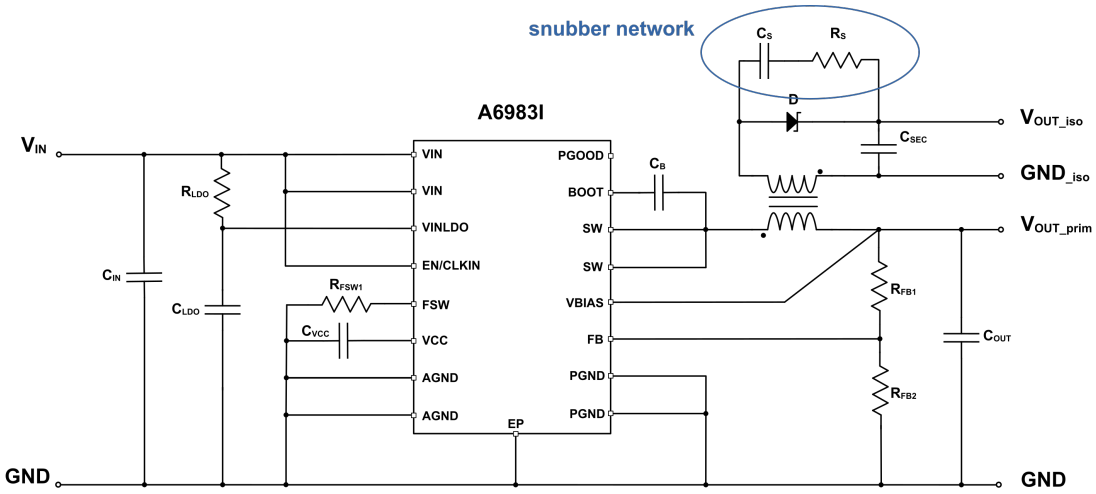
The ringing at the primary side could affect the regulation loop and falsely trigger the internal comparator, turning off the high-side MOSFET although it should be kept on. This might result in an undesired jitter at the switch node.

Figure 47. Filtering effect of the snubber network



A proper masking time ($T_{ON\ MIN}$) filters these oscillations, which can otherwise affect the loop on the primary side. Nevertheless, a RC snubber circuit (depicted in Figure 48) to dump this ringing is always recommended.

Figure 48. RC snubber network

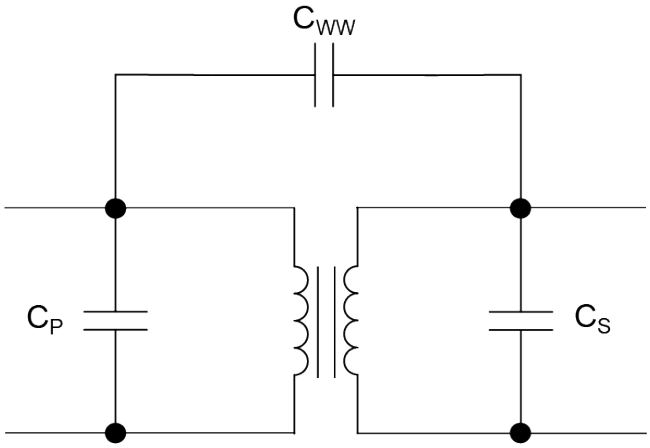


Capacitance

The parasitic capacitance of a real transformer mainly consists of the following contributions:

- Capacitance across each winding (C_P and C_S, in the picture below) due to the capacitive coupling between the coil and the core. As already mentioned, the winding capacitances are involved in the ringing observed during the transition from the off to on phase of the primary side.
- Interwinding capacitance (C_{WW}), that is the capacitance between windings. The interwinding capacitance should be reduced to limit disturbance on the primary side due to possible steep voltage transitions present in the load connected to the secondary output.

Figure 49. Transformer parasitic capacitances



11.3 Schottky diode

In the selection of the Schottky diode, the following parameters should be considered:

- Maximum forward current, mainly defined by the secondary output current demand (see equation (25));
- Forward voltage drop, which affects the secondary output voltage regulation;
- Maximum peak reverse voltage. During the on phase of the primary side, when in the secondary side no current flows, the diode is reverse biased and must withstand this voltage; and

$$V_{D1_rev} = N \cdot \left(V_{INmax} - V_{OUT_pri}\right) + V_{OUT_sec} \quad (28)$$

- Junction capacitance, which should be as low as possible in order to reduce the ringing described in the previous section.

11.4 Output capacitor selection

Primary output capacitor

As in a standard buck converter, the primary output capacitor is involved in:

- Determining the output voltage ripple
- Supporting load transient
- The loop stability, by setting one pole and one zero in the transfer function

Considering the output voltage ripple requirement, the primary output capacitance should be selected according to the following equation:

$$C_{OUT_pri} = \frac{\Delta I_{pri}}{8 \cdot f_{SW} \cdot \left(\Delta V_{OUT_pri} - ESR \cdot \Delta I_{pri}\right)} \quad (29)$$

Normally, an MLCC capacitor is the best choice for the output capacitor, therefore the ESR contribution is negligible and the equation can be simplified.

Secondary output capacitor

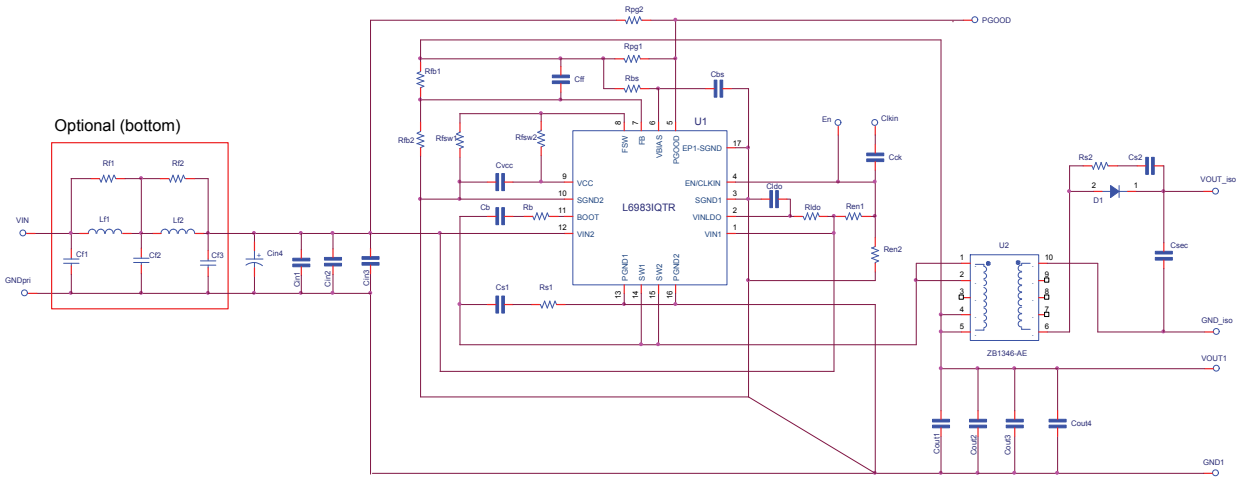
The secondary output capacitor supplies the secondary output load current during the tON (when diode D1 is reverse biased) and its value defines the secondary output voltage ripple (ΔV_{OUT}):

$$C_{OUT_sec} = \frac{I_{OUT_sec} \cdot D}{\Delta V_{OUT_sec} \cdot f_{SW}} \quad (30)$$

12 Application board

The application board (STEVAL-L6983IV1) schematic is shown in Figure 50:

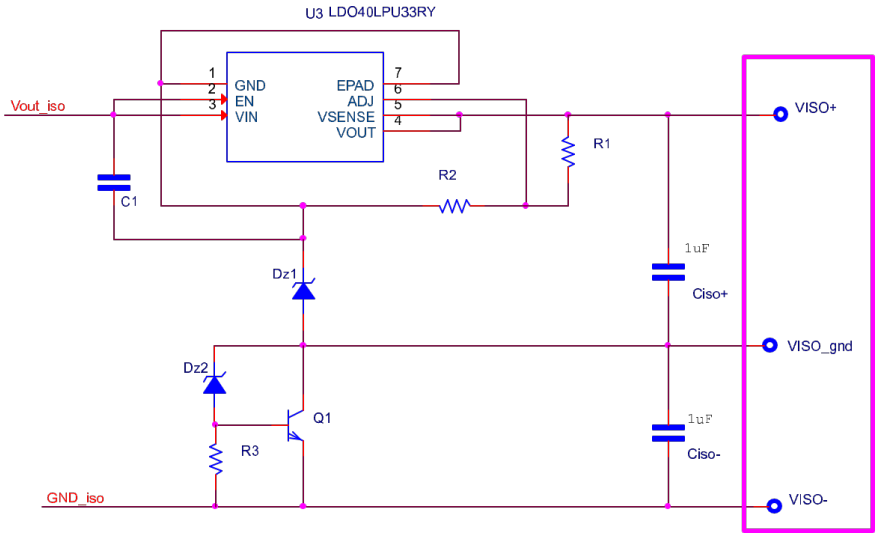
Figure 50. Schematic of the application board (unregulated isolated output)



The additional input filter (in the dotted box in Figure 50, on the bottom side of the board) limits the conducted emission on the power supply. In the case that the filter is not necessary or should be by-passed for any test, two 0 Ω resistors should be placed at Rf1 and Rf2.

The isolated output supplied by the board is unregulated. Nevertheless, a post regulation circuit (see the schematic in Figure 51) is provided on the bottom side (components not mounted). The values and the components indicated in the BOM Table 8 are assumed for a dual voltage 18 V/-5 V.

Figure 51. Proposed circuitry for post regulation (not mounted, bottom side) for dual voltage (18 V/-5 V)



If a different dual isolated voltage is necessary (e.g. 15 V/-6 V), the replacement of two components is enough to adapt the board: the Zener diode D_{Z2} (with a diode providing the most suitable Zener voltage) and the resistor divider (one of the two resistors) R_1 - R_2, in accordance with the equation:

$$V_{ISO+} = 1.2V \cdot \frac{R_1+R_2}{R_2} + V_{DZ1} \quad (31)$$

Table 8. **BOM list**

Reference	Part number	Description	Value	Manufacturer
U1	L6983IQTR			ST
U2	ZB1346-AE	Transformer	N = 6, 2 kV isolation	Coilcraft
Rs1		0805 SMD resistor	Not mounted	
Rs2		0805 SMD resistor	300 Ω	
Rb		0603 SMD resistor	0 Ω	
Ren1		0603 SMD resistor	100 kΩ	
Ren2		0603 SMD resistor	Not mounted	
Rfb1		0603 SMD resistor	360 kΩ	
Rfb2		0603 SMD resistor	75 kΩ	
Rfsw1		0603 SMD resistor	0 Ω	
Rfsw2		0603 SMD resistor	Not mounted	
Rpg1		0603 SMD resistor	Not mounted	
Rpg2		0603 SMD resistor	Not mounted	
Rbs		0603 SMD resistor	0 Ω	
Rldo		0603 SMD resistor	100 Ω	
Cldo		0603 MLCC	1 µF, 50 V	
Cff		0603 MLCC	Not mounted	
Cbs		0603 MLCC	100 nF, 50 V	
Cs1		0603 MLCC	Not mounted	
Cs2		0603 MLCC	180 pF, 50 V	
Cin1		1206 MLCC	10 µF, 50 V	
Cin2, Cin3		0805 MLCC	1 µF, 50 V	
Cin4		SMD Electrolytic capacitor, 10x10mm	100 µF, 50 V	Panasonic
Cout, Cout2, Cout3		1206 MLCC	22 µF, 50 V	
Cout4		0603 MLCC	Not mounted	
Csec		1206 MLCC	22 µF, 50 V	
Cck		0603 MLCC	Not mounted	
Cbs		0603 MLCC	Not mounted	
D1	STPS1170AY	Schottky diode	V_{RRM} = 170 V, I_F = 1 A	ST
EMI input filter				
Rf1		0603/0805 SMD resistor		
Rf2		0603/0805 SMD resistor		
Cf1, Cf2, Cf3		1206 MLCC, 4.7 µF, 50 V		
Lf1	MPZ2012S221A	220 Ω Ferrite bead, 100 MHz		
Lf2	XAL4030-682ME	6.8 µH coil		Coilcraft
Post regulation circuitry (option 18 V/-5 V)				
U3		LDO	Not mounted (DFN6)	ST
R1		0603 SMD resistor	Not mounted (910 Ω)	
R2		0603 SMD resistor	Not mounted (220 Ω)	

Reference	Part number	Description	Value	Manufacturer
R3		0603 SMD resistor	Not mounted (330 Ω)	
C1		0603 MLCC	Not mounted (1 µF, 35 V)	
Ciso+, Ciso-		0805 MLCC	Not mounted (1 µF, 50 V)	
Dz1		Zener diode	Not mounted (Vz1 = 12 V)	
Dz2		4.7 V Zener diode	Not mounted (Vz1 = 4.7 V)	
Q1	2STR1215	NPN power transitor	Not mounted	ST

Note: The STEVAL_L6983IV1 embeds the L6983I. The STEVAL_L6983I is however suitable for the A6983I. If the A6983I is be tested, simply replace the L6983I with A6983I.

13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

13.1 QFN16 (3x3 mm) package information

Figure 52. QFN16 (3x3 mm) package outline

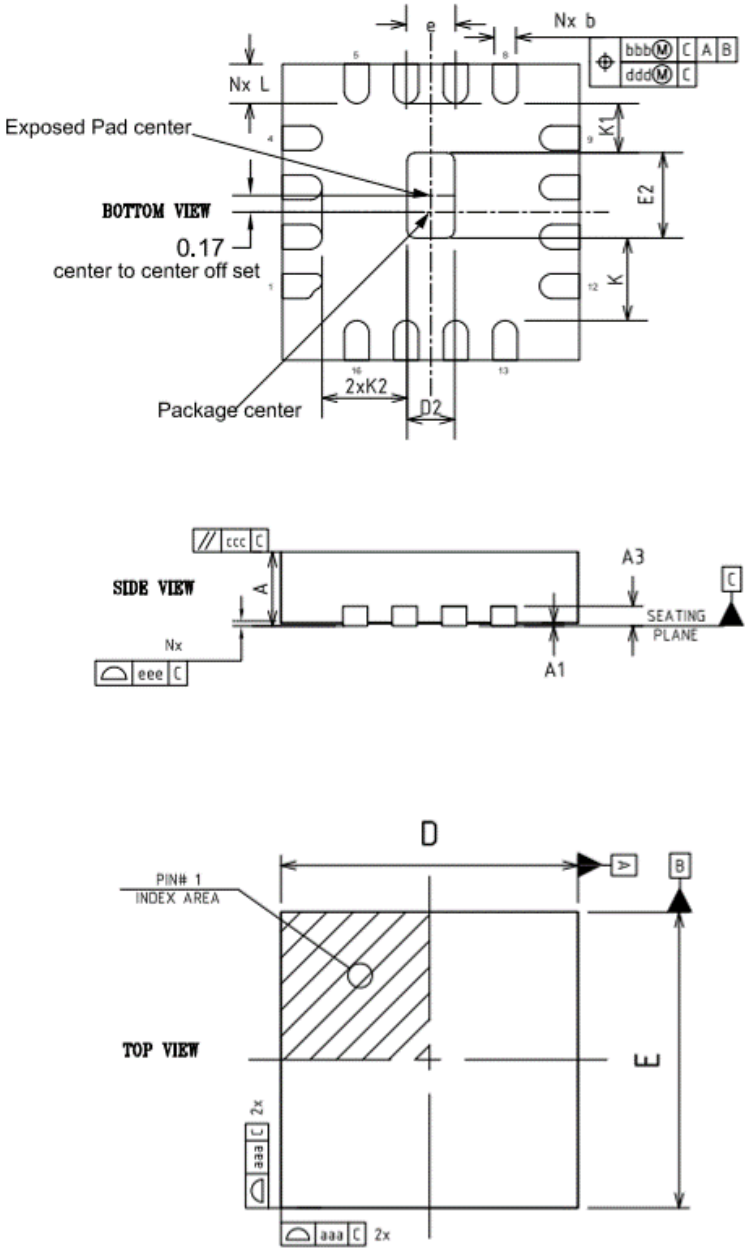


Figure 53. **QFN16 (3x3 mm) package outline. Detail A**

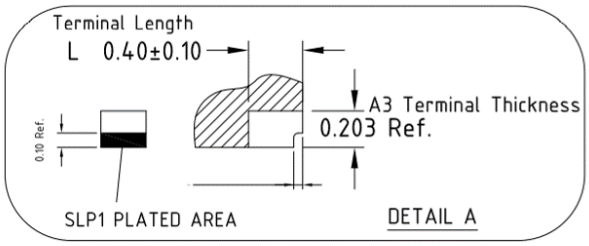
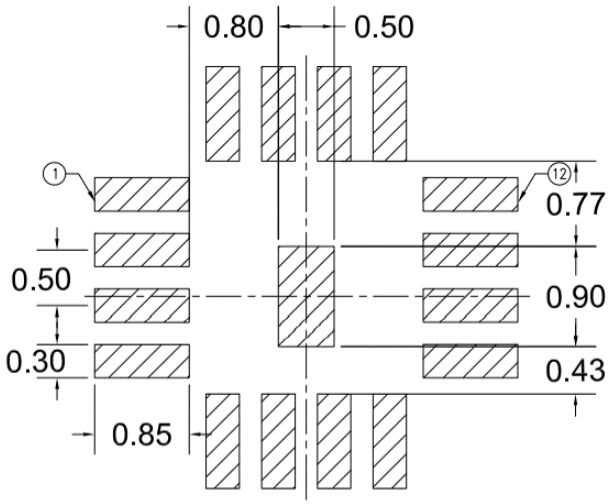


Table 9. **QFN16 (3x3 mm) mechanical data**

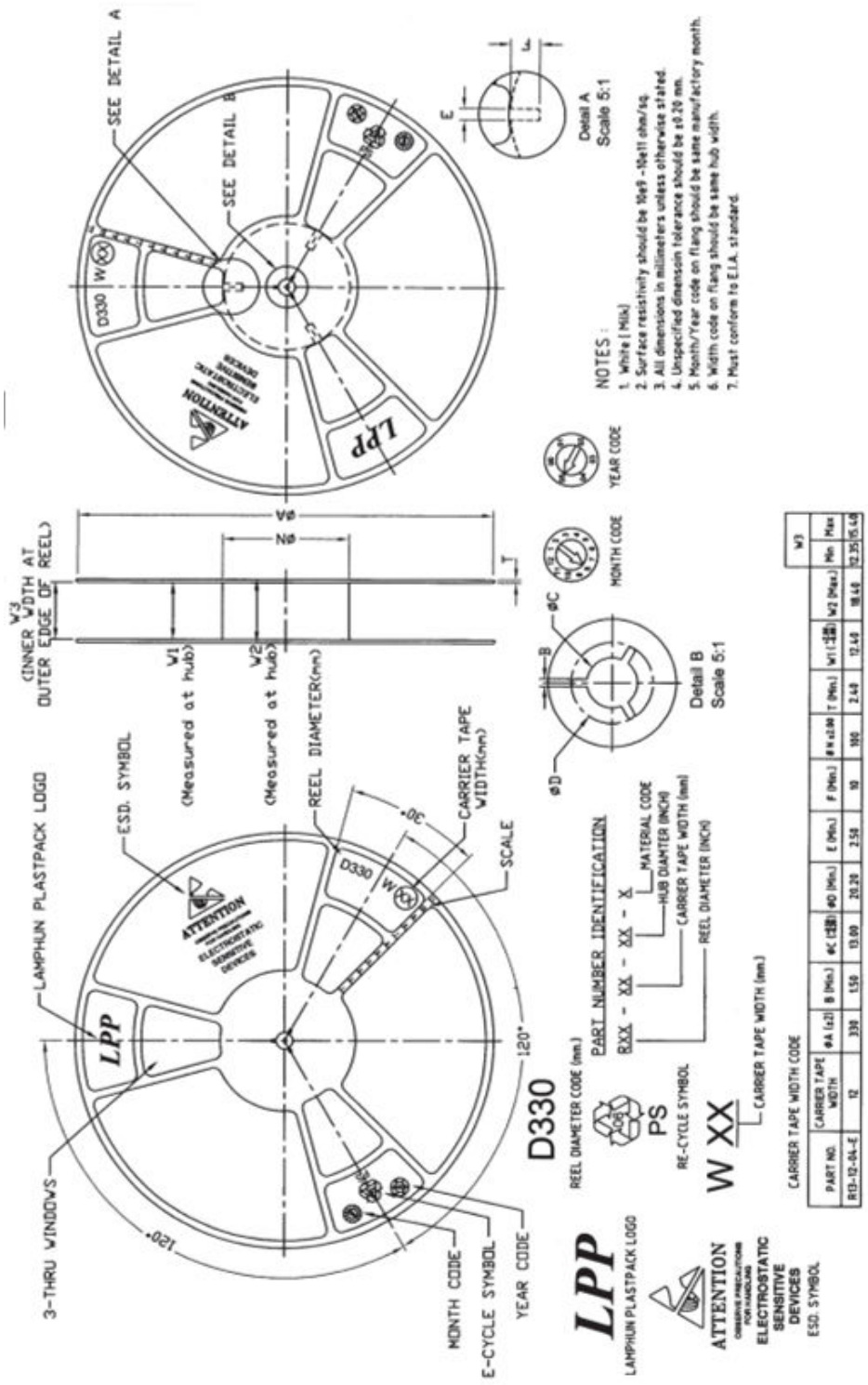
Symbol	mm		
	Min.	Typ.	Max.
A	0.7	0.75	0.8
A1	0		0.05
A2	0,5	0.55	0.6
A3		0,203REEF	
b	0.2	0.25	0.3
L	0.3	0.4	0.5
e		0,50BSC	
D	2.95	3	3.05
E	2.95	3	3.05
D1	0.43	0.48	0.53
E1	0.81	0.86	0.91

Figure 54. **QFN16 (3x3 mm) recommended footprint**



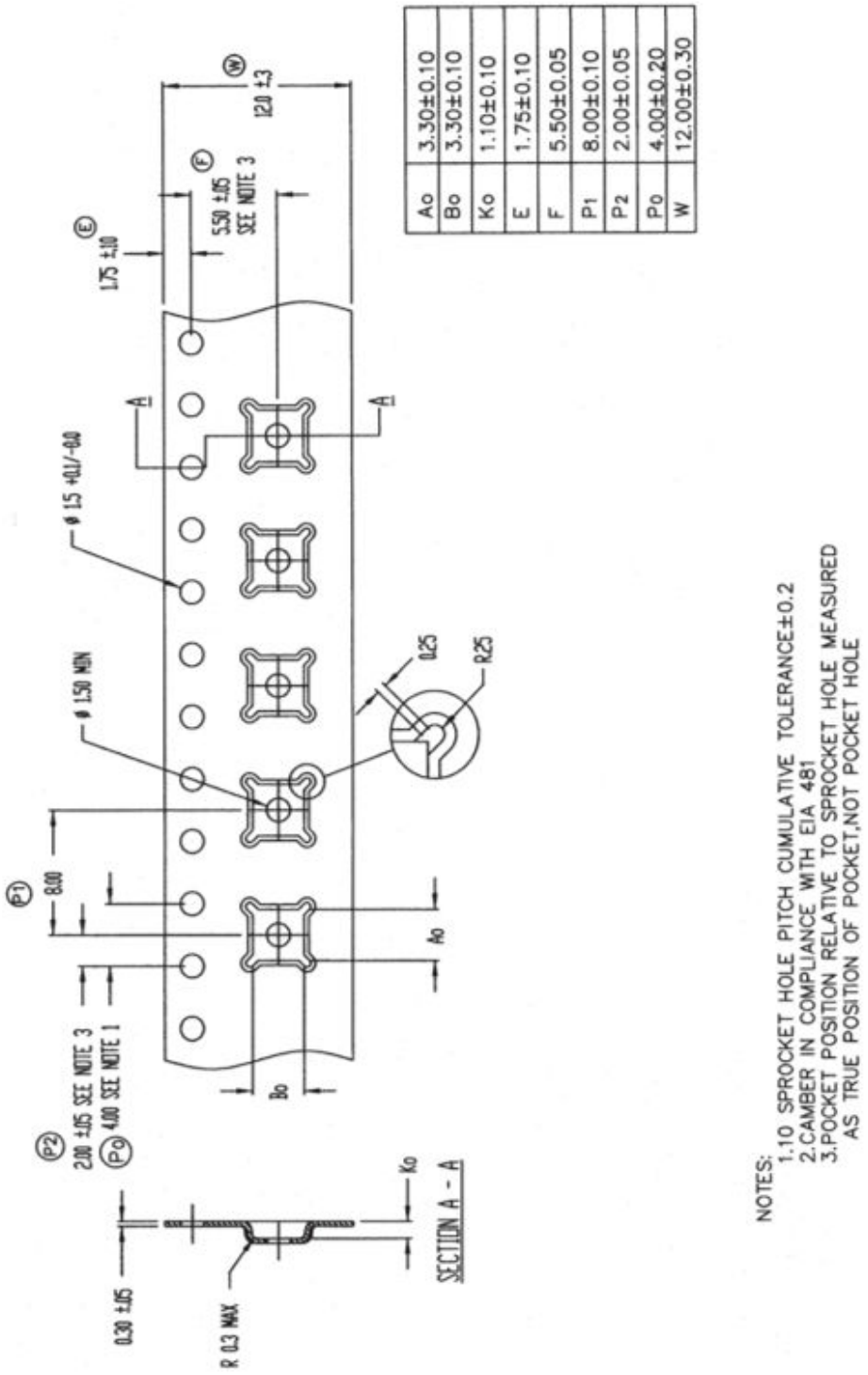
13.2 QFN16 (3x3 mm) packing information

Figure 55. Carrier tape for QFN 3x3 mm



PART NO.	CARRIER TAPE WIDTH	øA (±2)	B (Min.)	øC (±2)	øD (Min.)	E (Min.)	F (Min.)	øH (±0.08)	T (Max.)	W1 (±1)	W2 (Max.)	W3 Min	W3 Max
R13-12-04-E	12	330	1.50	13.00	20.20	2.50	10	1.60	2.40	12.40	18.40	12.35	15.40

Figure 56. **QFN16 (3x3 mm) plastic reel 13"**



14 Ordering information

Table 10. **Order codes**

Part numbers	Package	Packaging
A6983IQTR	QFN16	Tape and reel

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
19-Dec-2023	1	Initial release.

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