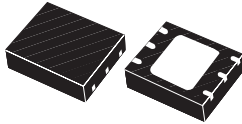


400 mA low-dropout LDO



DFN6 (2 x 2)
Wettable Flanks

Maternity status link

[LDQ44](#)

Features

- AEC-Q100 grade 1 qualified
- Operating temperature range: $-40\text{ }^{\circ}\text{C} < T_J < 150\text{ }^{\circ}\text{C}$
- Input voltage from 3.3 to 40 V
- Dropout voltage (1 V typ. at 400 mA load)
- Low ground current (2 μA typ. at no load)
- ADJ from 1.2 V to 12 V
- Output voltage tolerance: $\pm 2\%$ over temperature, 0.5% at 25 $^{\circ}\text{C}$
- 400 mA guaranteed output current
- Power good
- Logic-controlled electronic shutdown
- Internal current limit
- Short-circuit protection
- Thermal shutdown
- Output active discharge function
- Package options:
 - DFN6 (2x2) WF for automotive grade
 - DFN6 (2x2) for industrial grade

Applications

- EV powertrain
- Always-on battery connected application
- Infotainment and instrument cluster
- ADAS

Description

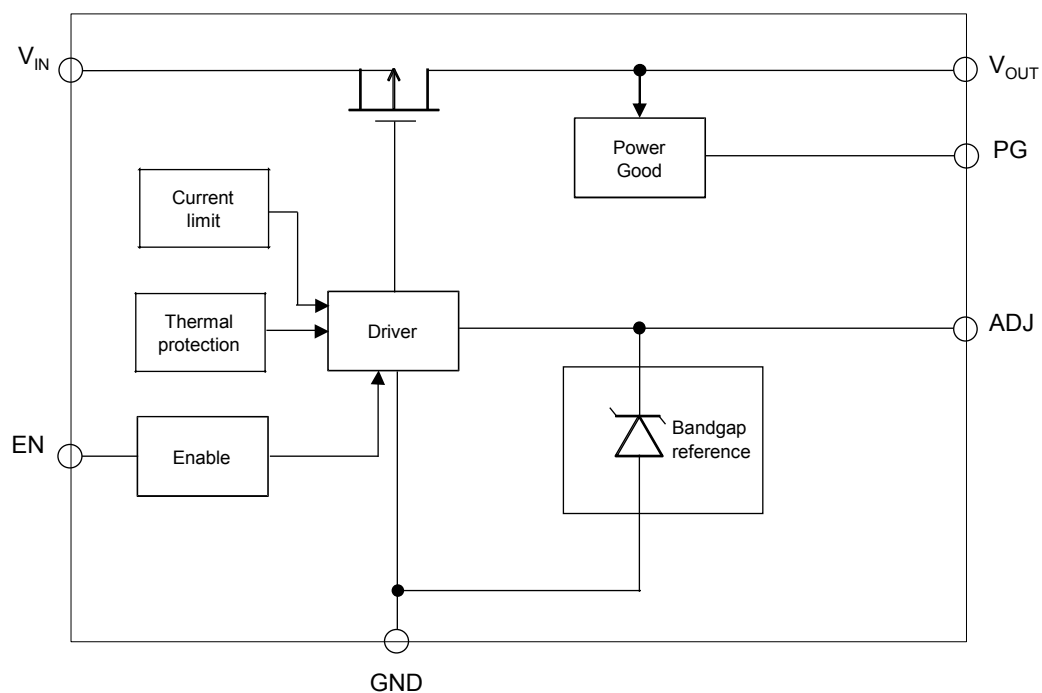
The **LDQ44** is a high accuracy voltage regulator, which provides 400 mA of current. It is available in a DFN 2x2 6L package, to maximize space saving.

The device is stabilized with a small ceramic capacitor on the output. The low drop, low quiescent current, and short-circuit protection make the **LDQ44** suitable for low power battery-operated applications.

An enable logic control function puts the **LDQ44** in shutdown mode allowing a total current consumption lower than 0.3 μA . Thermal protection is also included.

1 Diagrams

Figure 1. Block diagram adjustable version



2 Pin configuration

Figure 2. Pin connection (top view)

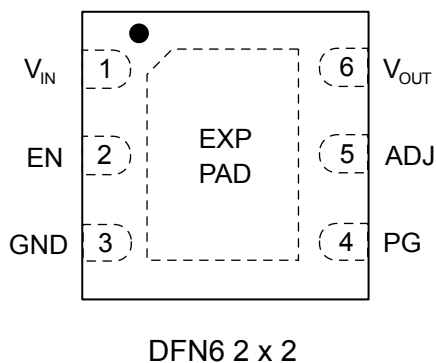


Table 1. Pin description

DFN6 2 x 2	Symbol	Description
1	V_{IN}	Input voltage
2	EN	Enable pin logic input: set V_{EN} = high to turn on the device V_{EN} = low to turn off the device Don't leave this pin floating
3	GND	Ground
4	PG	Power GOODood
5	ADJ	ADJ: adjust pin on the adjustable version. Connect to resistor divider to set the output voltage
6	V_{OUT}	Output voltage
Exp PAD	Exposed pad	Connect to GND

3 Typical application circuit

Figure 3. Typical application for adjustable version

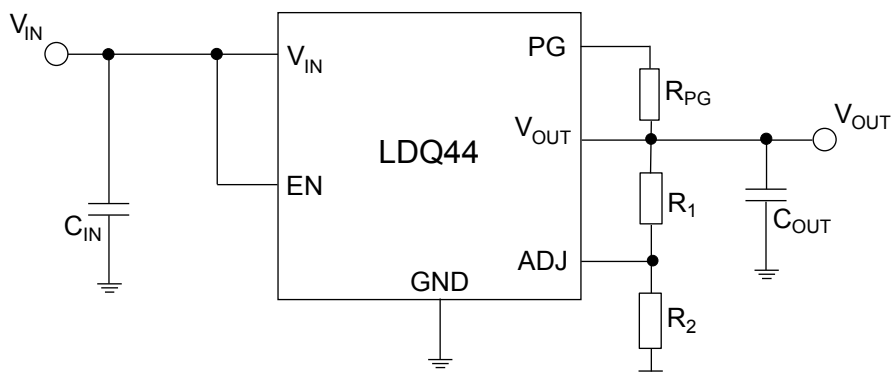


Table 2. Typical application components

Symbol	Value	Description	Note
C_{IN}	1 μ F	Input capacitor	Ceramic type
C_{OUT}	From 1 to 200 μ F	Output capacitor	Ceramic type
ESR	From 5 m Ω to 10 Ω		
R_1		Output voltage side resistor	2 M Ω max
R_2		Ground side resistor	2 M Ω max

Note: Including component derating.

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	-0.3 to 42	V
V_{OUT}	Output voltage ADJ version	-0.3 to 13	V
V_{ADJ}	Adjustable voltage	-0.3 to 3	V<
V_{EN}	Enable input voltage	-0.3 to V_{IN}	V
V_{PG}		13	V
I_{OUT}	Output current ⁽¹⁾	Internally limited (see I_{SC} on Table 6)	A
T_{STG}	Storage temperature range	-40 to 150	°C
T_{JOP}	Operating junction temperature range	-40 to 150	°C

1. FR4 board with using 1 sq-in pad, 1 oz Cu.

Note: Stressing the device above the rating listed in Table 3 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Thermal data

Symbol	Parameter	DFN6 (2x2)	Unit
R_{thJA}	Thermal resistance junction-ambient ⁽¹⁾	62	°C/W

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM on corner pins of DFN WF	750	V
		CDM inner pins of DFN WF	500	V
		CDM industrial packages	500	V

5 Electrical characteristics

Table 6. Electrical characteristics $V_{IN} = V_{OUT(NOM)} + 0.8\text{ V}$ or 3.3 V (whichever is greater); $I_{OUT} = 1\text{ mA}$; $C_{IN} = 4.7\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$; $V_{EN} = V_{IN}$; typical values are at $T_J = 25\text{ }^\circ\text{C}$; min/max values are at $-40\text{ }^\circ\text{C} \leq T_J \leq 150\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		$V_{OUT} + V_{DROP}$		40	V
$V_{IN(UVLO)}$	Undervoltage lockout	Rising edge		2.55	2.65	V
		Hysteresis		0.2		
V_{REF}	Reference voltage for adjustable devices	$T_J = 25\text{ }^\circ\text{C}$;		1.2		V
V_{OUT}	Output voltage accuracy	All versions, $T_J = 25\text{ }^\circ\text{C}$	-0.5		+0.5	%
		$V_{OUT(NOM)} + 1\text{ V} \leq V_{IN} \leq 18\text{ V}$;				
		Adjustable version $I_{OUT} = 1\text{ mA}$ to 400 mA ; $-40\text{ }^\circ\text{C} \leq T_J \leq 125\text{ }^\circ\text{C}$	-2.0		2.0	
ΔV_{OUT-IN}	V_{IN} static regulation	$V_{OUT(NOM)} + 1\text{ V} \leq V_{IN} \leq 18\text{ V}$		0.01	0.05	% / V
$\Delta V_{OUT-LOAD}$	Static load regulation	$I_{OUT} = 1\text{ mA}$ to 400 mA		3.2	4.8	mV
V_{DROP}	Dropout voltage	$I_{OUT} = 400\text{ mA}$;		1000	1900	mV
I_{LIM}	Output current limit	$V_{OUT} = 90\% V_{OUT(NOM)}$	450	680	1000	mA
I_{SC}	Short circuit protection	$V_{OUT} = 0.4\text{ V}$	150	275	450	mA
I_{ADJ}	ADJ pin operating current			0.1	0.5	μA
I_Q	Quiescent current during regulation	V_{IN} from 2.5 to 40 V no load		2	5	μA
		10 mA		15		
		100 mA		90		
		400 mA		300	1500	
I_{Q_OFF}	Standby current	$V_{IN} = 14\text{ V}$		0.3	1	μA
V_{EN}	Enable input logic low	V_{IN} up to 40 V			1.6	V
	Enable input logic high	V_{IN} up to 40 V	2.0			
I_{EN}	Enable pin input current	V_{EN} from 2 V to 40 V		0.01	0.1	μA
V_{PG_OK}	Power good output threshold, rising ⁽¹⁾		93		98	% V_{OUT}
V_{PG_NOK}	Power good output threshold, falling ⁽¹⁾		86		95	
	Power good hysteresis		30	70		mV
V_{PG_L}	Power good output voltage low	$I_{SINK_MAX} = 6\text{ mA}$, open drain output			0.4	V
T_{ON}	Turn on time	From assertion of V_{EN} to $V_{OUT} = 98\% V_{OUT(NOM)}$; $V_{OUT(NOM)} \cdot V_{OUT(NOM)} = 1.0\text{ V}$		500		μs
SVR_i	V_{IN} supply voltage rejection (adj version)	$V_{IN} = V_{OUT(NOM)} + 0.8\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2\text{ V}$; freq = 1 kHz $I_{OUT} = 10\text{ mA}$; $V_{OUT(NOM)} = 2.5\text{ V}$		60		dB
e_{N-ADJ}	Output noise voltage (adj version)	$V_{IN} = V_{OUT(NOM)} + 1\text{ V}$; $V_{OUT(NOM)} = 1.2\text{ V}$;		50		μV_{RMS}

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		10 Hz to 100 kHz, $I_{OUT} = 1\text{ mA}$				
R_{ON}	Output voltage discharge MOSFET			150		Ω
T_{SHDN}	Thermal shutdown			170		$^{\circ}\text{C}$
	Hysteresis			20		

1. The power good threshold is calculated as the percentage of the measured V_{OUT} .

6 Application information

6.1 V_{IN} pin voltage requirements

The LDQ44 is a low-dropout linear voltage regulator equipped with a low-RDS-(on) P-channel MOSFET used as a pass-element. The device's internal circuits are able to start with an input voltage as low as 3.3 V.

6.2 Output voltage

The LDQ44 is available in adjustable output voltage version. The latter option is usually chosen when the output voltage has to be set to non-standard values. In the adjustable version, the output voltage can be set from 1.2 V up to 12 V, by connecting a resistor divider between the ADJ pin and the output.

6.3 Output discharge function

The LDQ44 embeds an open drain that allows the output capacitor to discharge, with about 75 Ohm when the enable pin goes to zero.

6.4 Short circuit and current limitation

The LDQ44 is protected against short circuits on the output. The load current is limited to the maximum value of I_{LIM} when V_{OUT} is equal to 90% of its nominal value. When the output voltage drops below 0.4 V, the output current is limited to the short-circuit value.

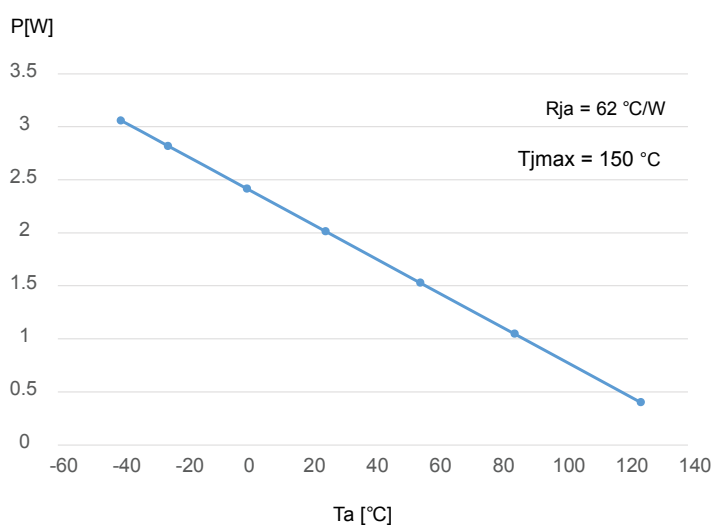
6.5 Thermal protection

Thermal protection acts when the junction temperature reaches 170 °C typical. At this point, the output of the IC shuts down. As soon as the junction temperature falls below the thermal hysteresis value, the device starts working again.

To calculate the maximum power that the device can dissipate, keeping the junction temperature below the maximum operating value, the following formula is used:

$$P_{DMAX} = (150 - T_{AMB}) / R_{thJA} \quad (1)$$

Figure 4. Derating curve



6.6 Input and output capacitors

The LDQ44 requires external capacitors to assure the regulator control loop stability.

Any good quality ceramic capacitor can be used, however, the X5R and the X7R are suggested since they guarantee a very stable combination of capacitance and ESR overtemperature.

It is recommended that the input/output capacitors are located as close as possible to the relative pins.

The LDQ44 requires a V_{IN} capacitor with a minimum value of 1 μ F minimum.

The control loop is designed to be stable with any good quality output ceramic capacitor (such as X5R/X7R types) with a minimum value of 1.0 μ F and equivalent series resistance in the [5 m Ω – 10 Ω] range. It is important to highlight that the output capacitor must maintain its capacitance and ESR in the stable region over the full operating temperature and load and input voltage ranges, to assure stability. Therefore, capacitance and ESR variations must be taken into account in the design phase to ensure the device works in the expected stability region.

6.7 Power good output

The LDQ44 features a power good open-drain output. The pin is high-Z when the output voltage is within the valid range or when the device is disabled (EN = LOW). The pin is pulled low when the output voltage is below the minimum PG threshold (see V_{PG_OK} V_{PG_NOK} parameters).

7 Typical performance characteristics

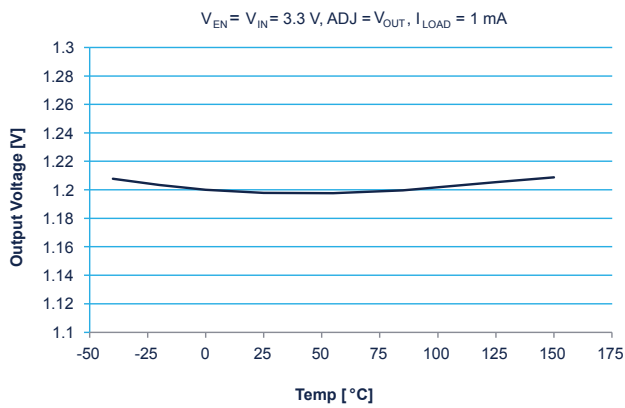
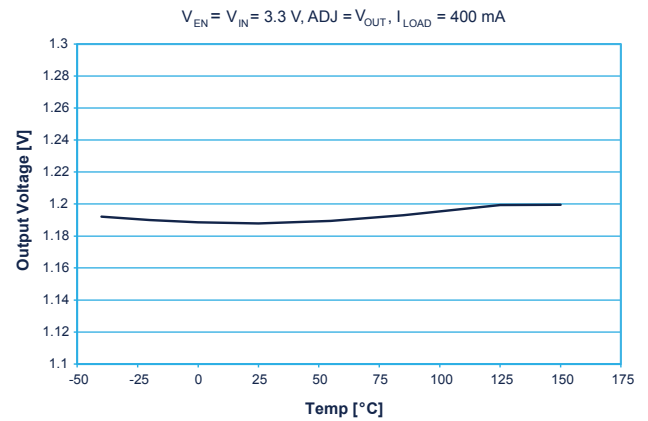
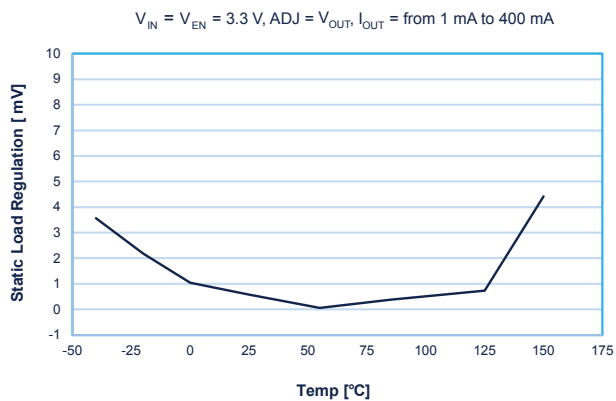
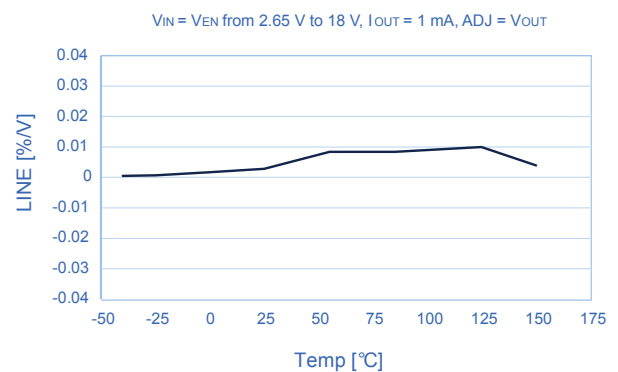
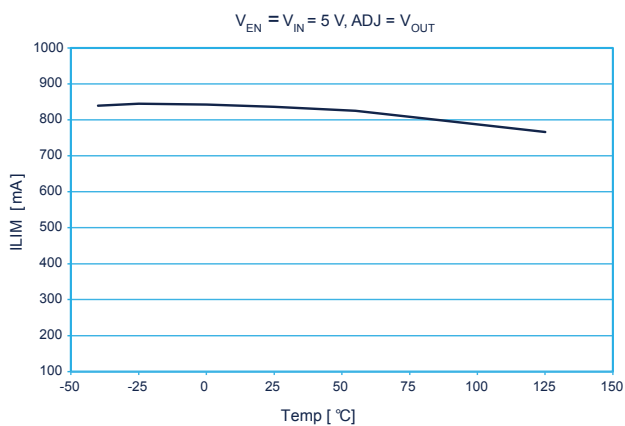
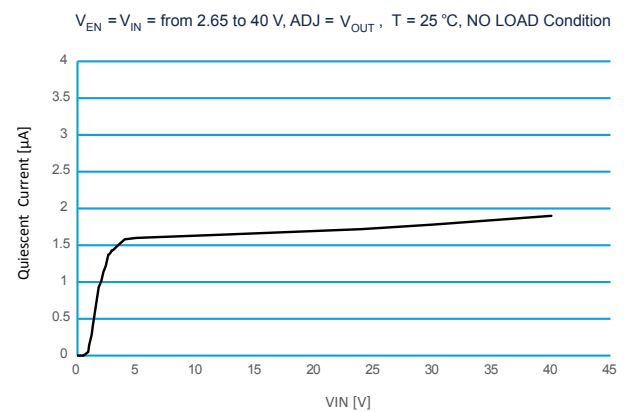
 $C_{IN} = 4.7 \mu F$; $C_{OUT} = 10 \mu F$
Figure 5. Output voltage vs. temperature

Figure 6. Output voltage vs. temperature

Figure 7. Static load vs. temperature

Figure 8. Line regulation

Figure 9. Output current limit vs. temperature

Figure 10. Quiescent current vs. V_{IN}


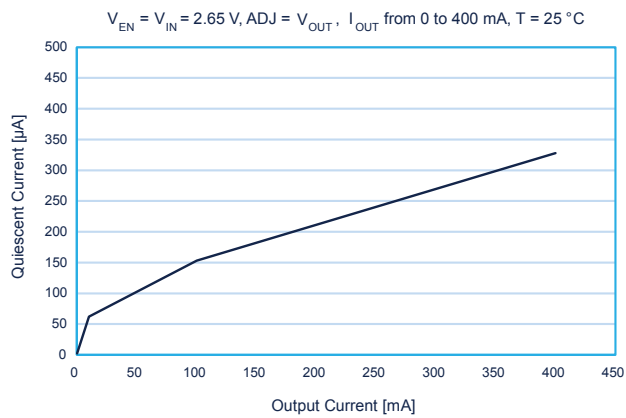
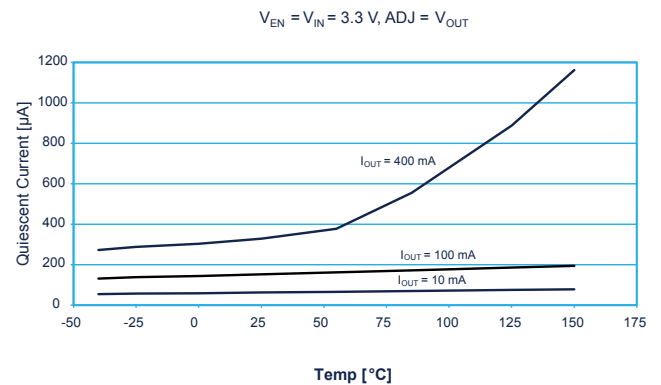
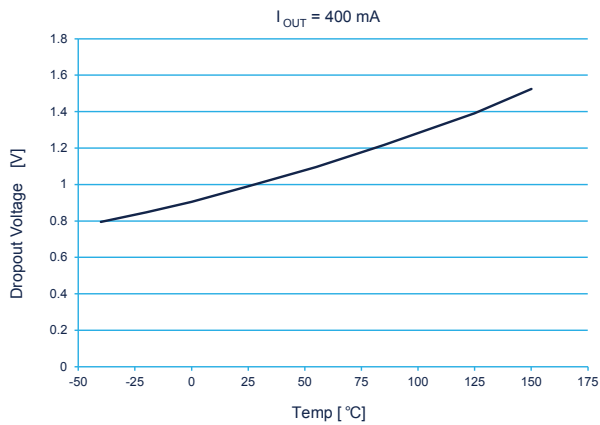
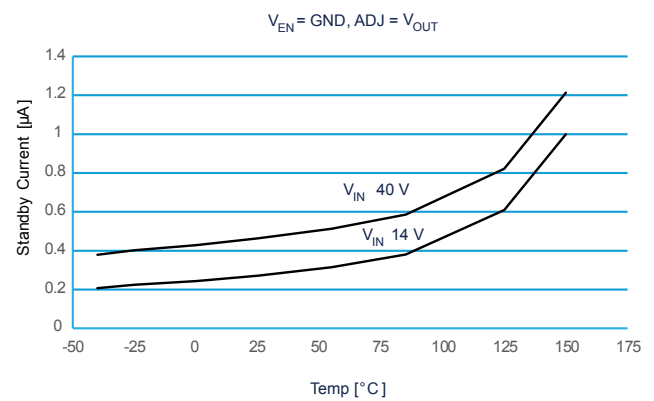
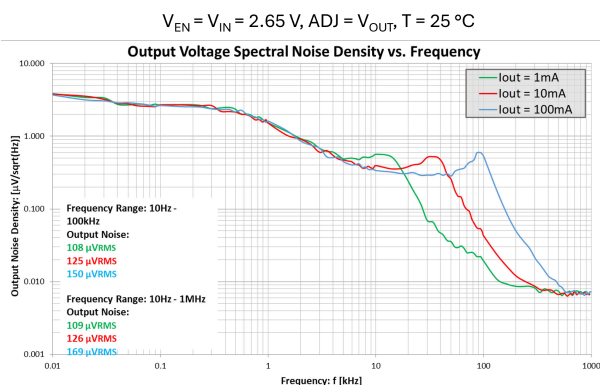
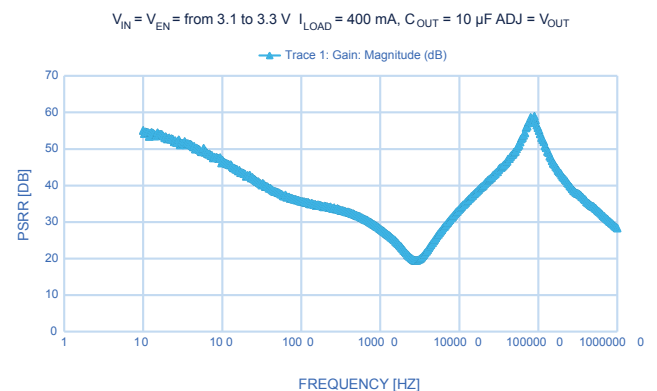
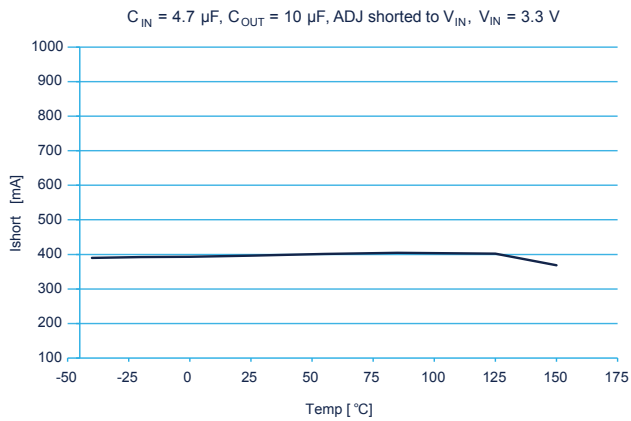
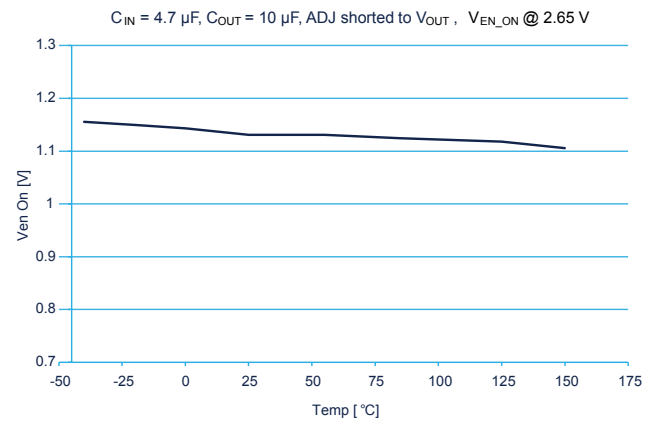
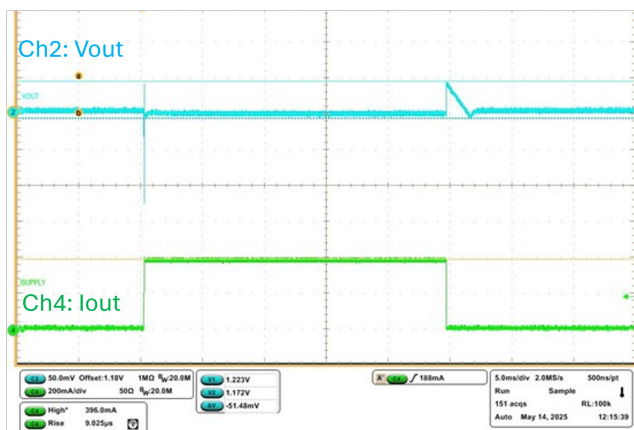
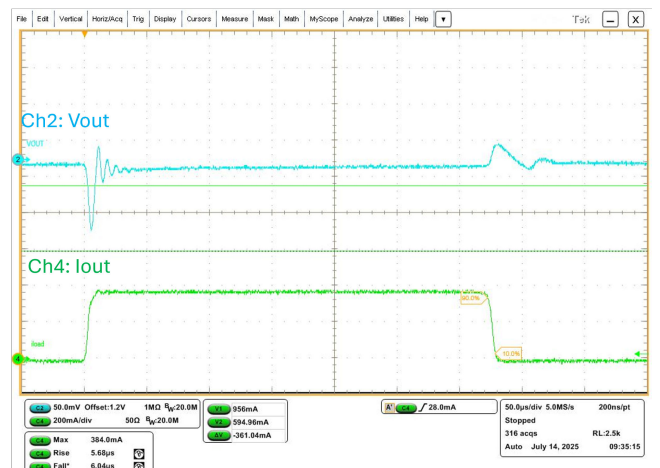
Figure 11. Quiescent current vs. output current

Figure 12. Quiescent current vs. temperature

Figure 13. Dropout voltage vs. temperature

Figure 14. Standby current vs. input voltage

Figure 15. Output noise voltage

Figure 16. PSRR tests


Figure 17. Short-circuit current vs. temperature

Figure 18. Enable threshold vs. temperature

Figure 19. Load regulation transient

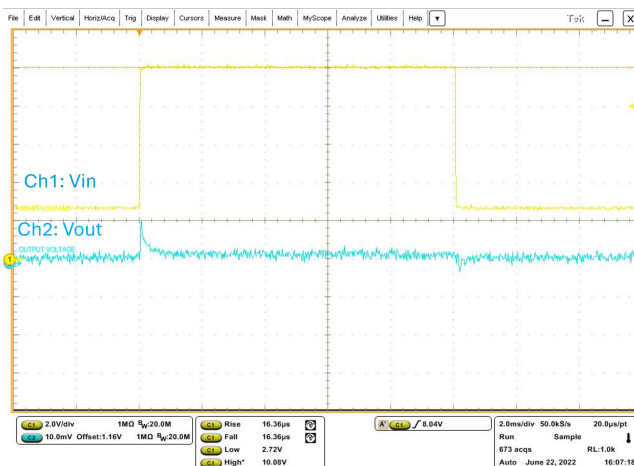
$V_{IN} = V_{EN} = 3.3 V$, ADJ = V_{OUT} , 100 μA to 400 mA, $t_r = t_f = 5 \mu s$


Figure 20. Load transient

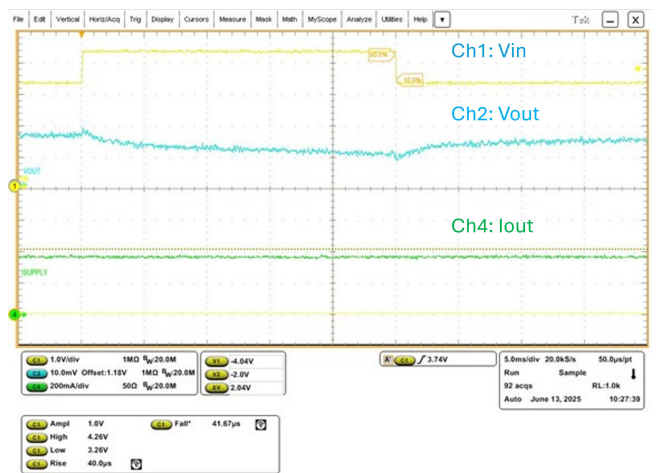
$V_{IN} = V_{EN} = 3.3 V$, ADJ = V_{OUT} , 1 mA to 400 mA, $t_r = t_f = 5 \mu s$


Figure 21. Line transient

$V_{IN} = V_{EN} = 2.65 V$ to 10 V, $t_r = t_f = 1 \mu s$, ADJ = V_{OUT} , $I_{OUT} = 1 mA$


Figure 22. Line transient

$V_{IN} = V_{EN} = 3.3 V$ to 4.3 V, $t_r = t_f = 1 \mu s$, ADJ = V_{OUT} , $I_{OUT} = 400 mA$



8 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 DFN6 (2 x 2) package information

Figure 23. DFN6 (2 x 2) package outline

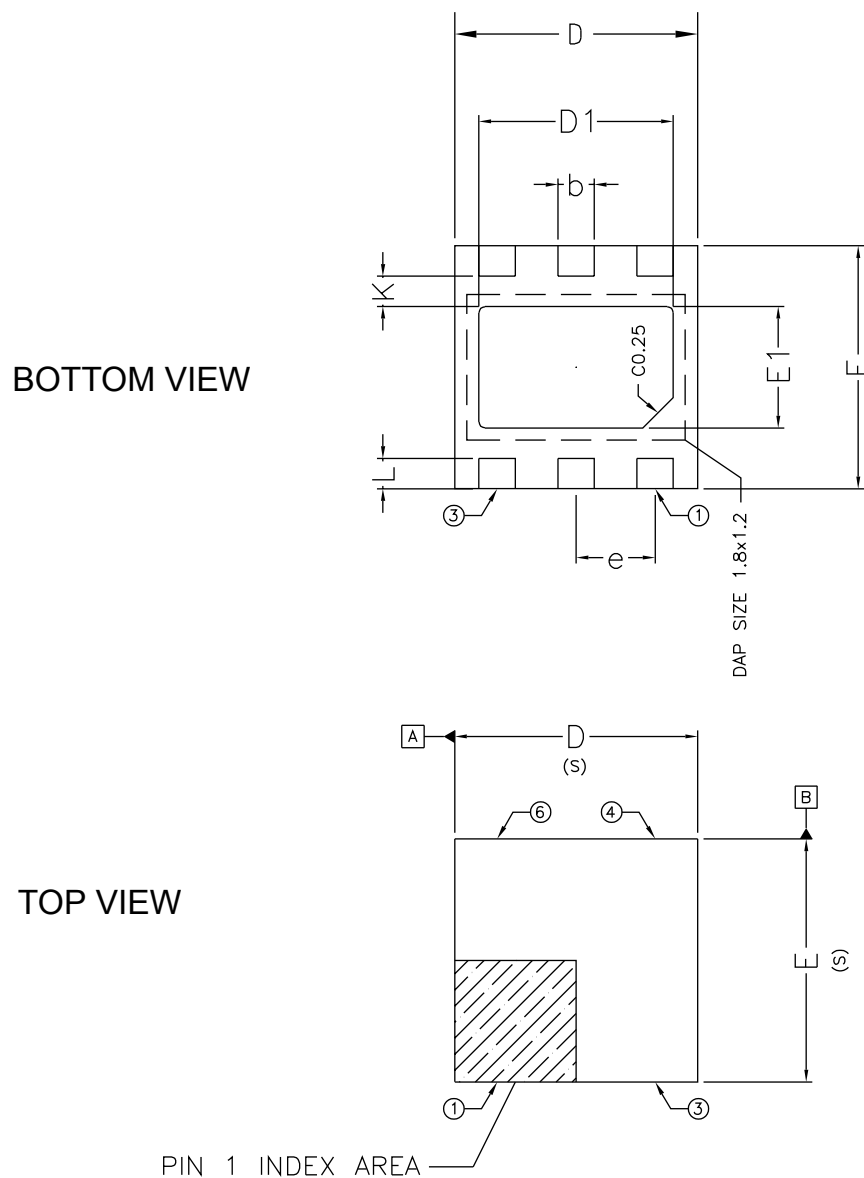
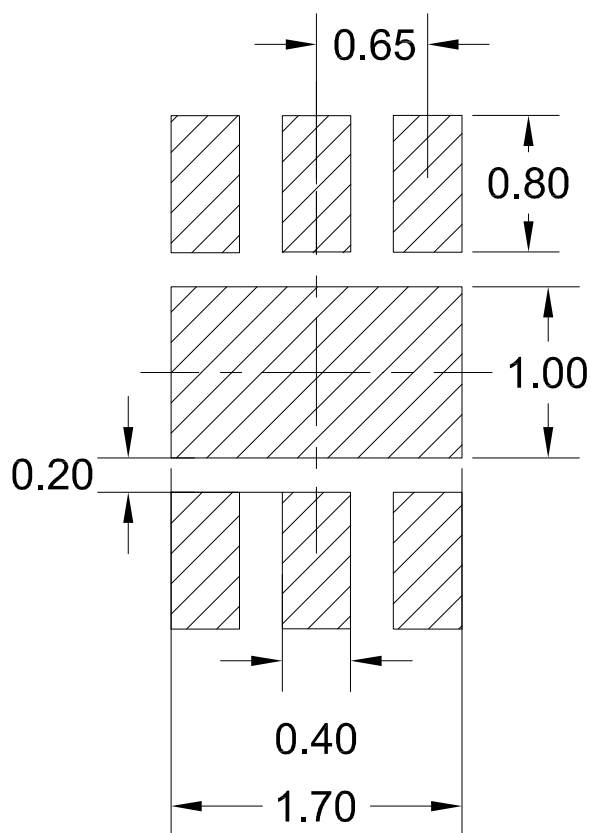


Table 7. DFN6 (2 x 2) mechanical data

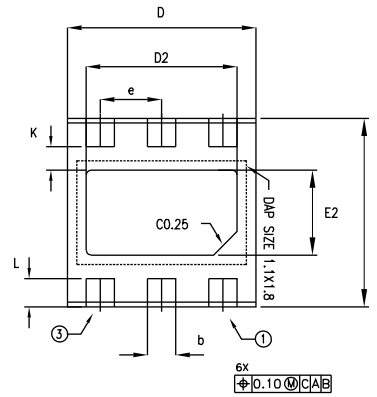
Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00		0.05
A3	0.200 REF		
b	0.25	0.30	0.35
D	1.95	2.00	2.05
D1	1.50	1.60	1.70
e	0.65 BSC		
e2	0.25 REF		
E	1.95	2.00	2.05
E1	0.90	1.00	1.10
K		0.25	
L	0.15	0.25	0.35

Figure 24. DFN6 (2 x 2) recommended footprint


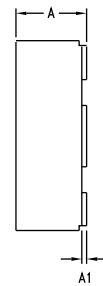
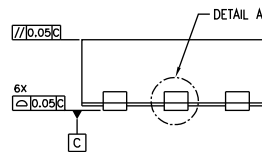
8.2 DFN6 (2 x 2) wettable flanks package information

Figure 25. DFN6 (2 x 2) wettable flanks package outline

BOTTOM VIEW



SIDE VIEW



TOP VIEW

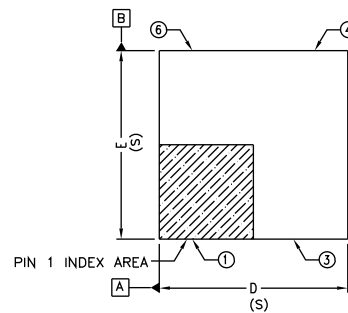
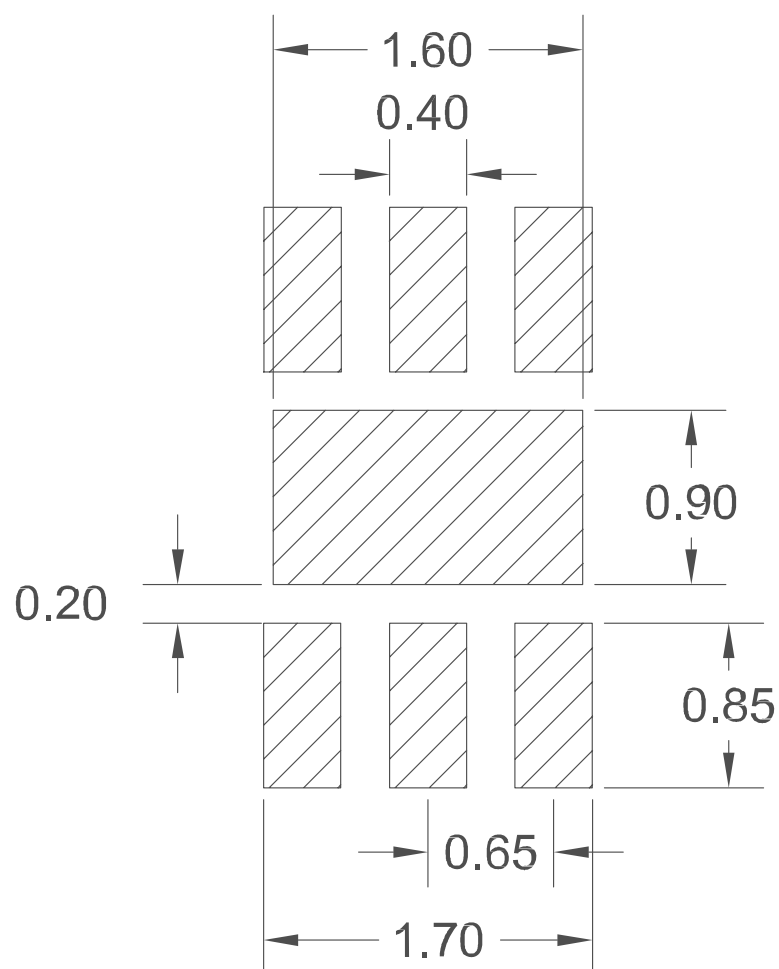


Table 8. DFN6 (2 x 2) wettable flanks mechanical data

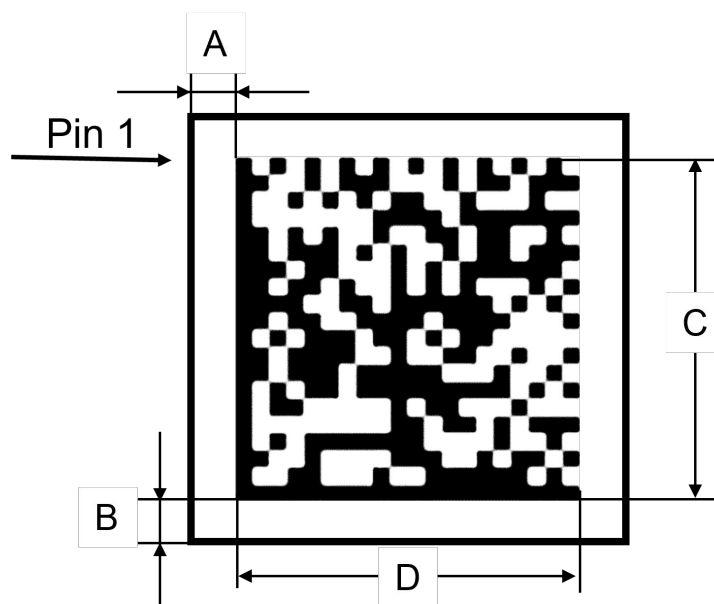
Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00		0.05
b	0.25	0.30	0.35
D	1.95	2.00	2.05
D2	1.50	1.60	1.70
e	0.65 BSC		
E	1.95	2.00	2.05
E2	0.80	0.90	1.00
L	0.20	0.30	0.40
K	0.25 BSC		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.10		

Figure 26. DFN6 (2 x 2) wettable flanks recommended footprint



8.3 DFN6 WF 2D marking information

Figure 27. DFN6 WF 2D marking



Spec	UTL
A	0.2 mm
B	0.2 mm
C	1.6x1.6 (+/-0.125) mm.
D	1.6x1.6 (+/-0.125) mm.

Figure 28. DFN6 (2x2 mm) tape outline

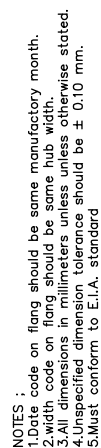


Figure 29. DFN6 (2x2 mm) reel outline

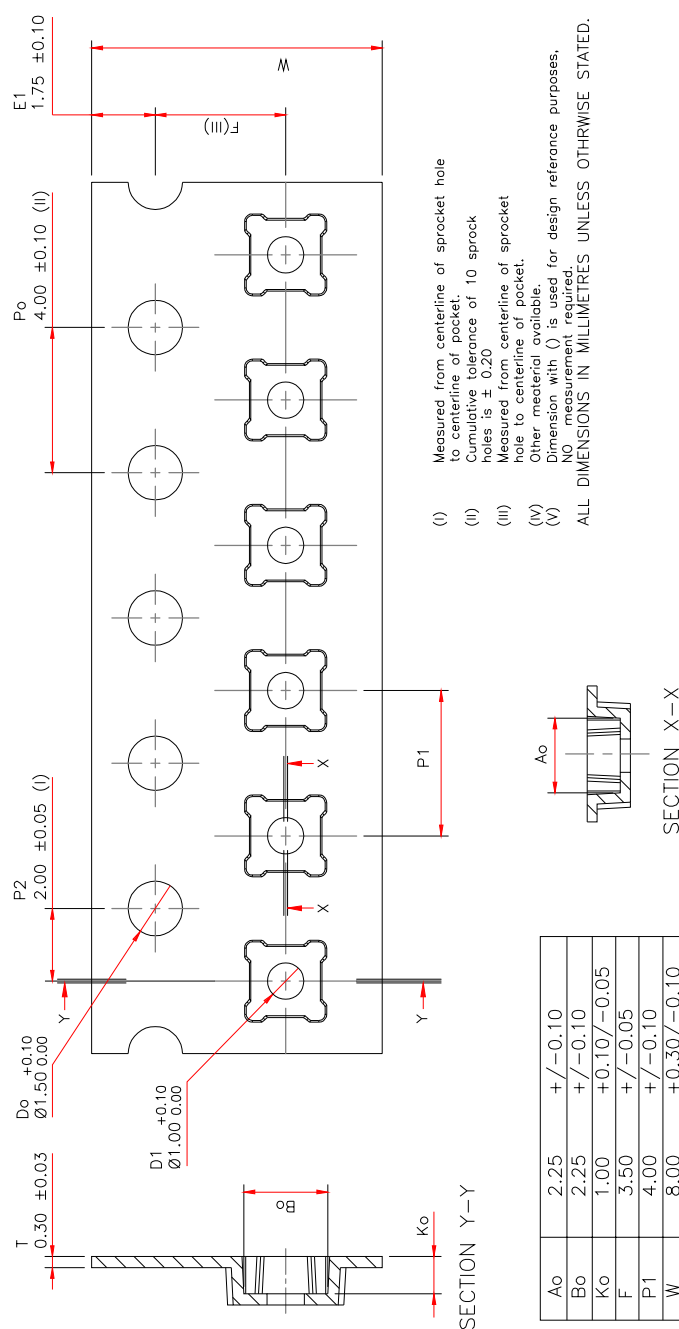


Figure 30. Pin 1 orientation

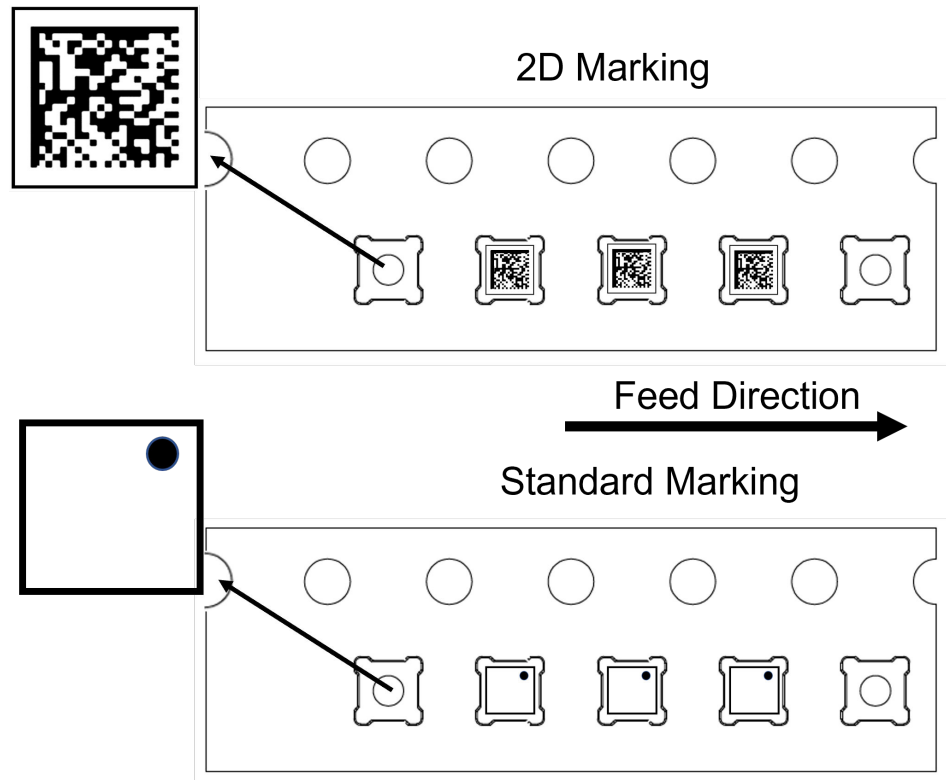
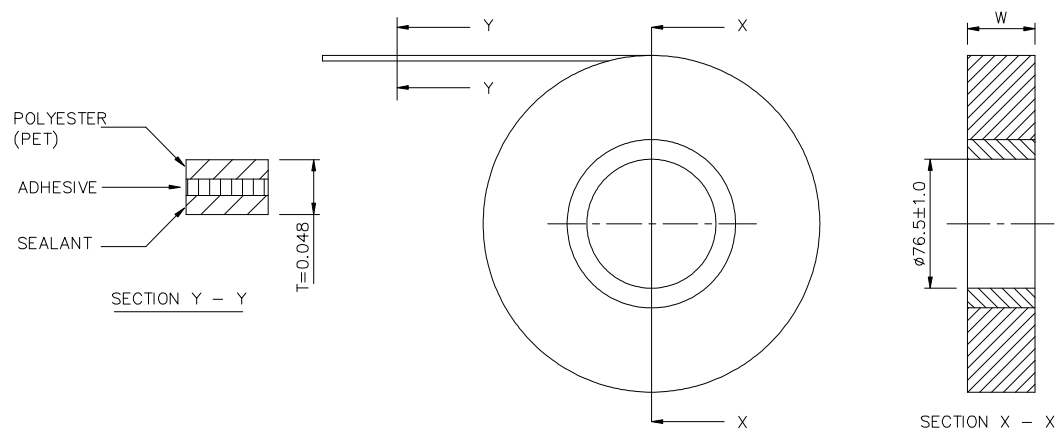


Figure 31. DFN6 (2x2 mm) cover tape outline



COVER TAPE WIDTH* (W ±0.1)	CARRIER TAPE WIDTH
5.3, 5.4, 5.5	8
9.2, 9.3, 9.5	12
13.3, 13.5	16
21.0, 21.3	24
25.5	32
37.5	44
49.5	56
81.5	88

NOTES

- 1 THICKNESS : 0.041 – 0.055
- 2 STANDARD LENGTH : 300m or 500m
- 3 TENSILE STRENGTH : >5.0kg/mm sq.
- 4 ELONGATION : >75%
- 5 SURFACE RESISTANCE: 1E+4 TO 9.9E+10 ohms.
SURFACE RESISTIVITY: 1E+5 TO 9.9E+11 ohms/sq.
- 6 PEEL STRENGTH CONFORMS TO EIA SPEC: 20 TO 80g
- 7 RECOMMENDED SHELF LIFE : 2 YEARS
FROM MANUFACTURING DATE
- 8 LUMINOUS TRANSMITTANCE : 87.8%
- 9 HAZE : 28%
- *10 OTHER COVER TAPE WIDTH REFER TO W14.08–04.

9 Ordering information

Table 9. Order code

Order code	Package	V _{OUT}	Marking
LDQ44PURY	DFN6 2x2 wettable flanks	ADJ	see 2D code
LDQ44PUR	DFN6 2x2	ADJ	AD

Revision history

Table 10. Document revision history

Date	Revision	Changes
04-Jun-2026	1	Initial release.

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