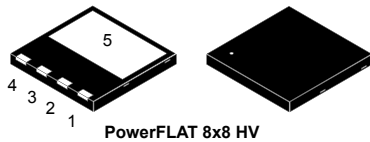
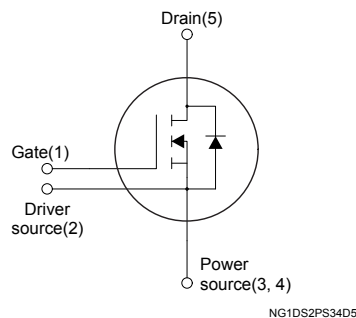


N-channel 650 V, 38 mΩ typ., 55 A, MDmesh DM9 Power MOSFET in a PowerFLAT 8x8 HV package



Product status link

[ST8L65N050DM9](#)

Product summary

Order code	ST8L65N050DM9
Marking	65N050DM9
Package	PowerFLAT 8x8 HV
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
ST8L65N050DM9	650 V	50 mΩ	55 A

- Fast-recovery body diode
- Very low FOM (R_{DS(on)}•Q_g)
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Excellent switching performance thanks to the extra driving source pin

Applications

- LLC resonant converter
- Power supplies and converters

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh DM9 technology, suitable for medium/high voltage MOSFETs featuring very low R_{DS(on)} per area coupled with a fast-recovery diode. The silicon-based DM9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The fast-recovery diode featuring very low recovery charge (Q_{rr}), time (t_{rr}) and R_{DS(on)} makes this fast-switching super-junction Power MOSFET tailored for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	55	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	35	
$I_{DM}^{(2)}$	Drain current (pulsed)	225	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	167	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	120	V/ns
$di/dt^{(3)}$	Peak diode recovery current slope	900	A/ μs
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Referred to TO-247 long leads package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 27.5\text{ A}$, $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
4. $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.75	$^\circ\text{C/W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	45	$^\circ\text{C/W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	7	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 100\text{ V}$)	787	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			5	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			200	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.5	4.0	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 27.5\text{ A}$		38	50	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$, $V_{GS} = 0\text{ V}$	-	4584	-	pF
C_{oss}	Output capacitance		-	80	-	pF
$C_{oss\text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	977	-	pF
R_g	Intrinsic gate resistance	$f = 250\text{ kHz}$, open drain	-	1	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 27.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 14. Test circuit for gate charge behavior)	-	107	-	nC
Q_{gs}	Gate-source charge		-	26	-	nC
Q_{gd}	Gate-drain charge		-	41	-	nC

1. $C_{oss\text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 27.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	25	-	ns
t_r	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	80	-	ns
t_f	Fall time		-	3.5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-	-	55	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-	-	225	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 55\text{ A}$	-	-	1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 55\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 150\text{ V}$ (see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	157	-	ns
Q_{rr}	Reverse recovery charge		-	1.4	-	μC
I_{RRM}	Reverse recovery current		-	11	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 55\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 150\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	315	-	ns
Q_{rr}	Reverse recovery charge		-	3	-	μC
I_{RRM}	Reverse recovery current		-	19	-	A

1. Referred to TO-247 long leads package.
2. Pulse width is limited by safe operating area.
3. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

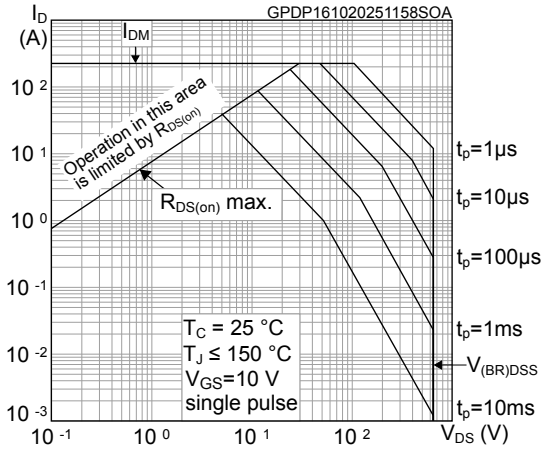
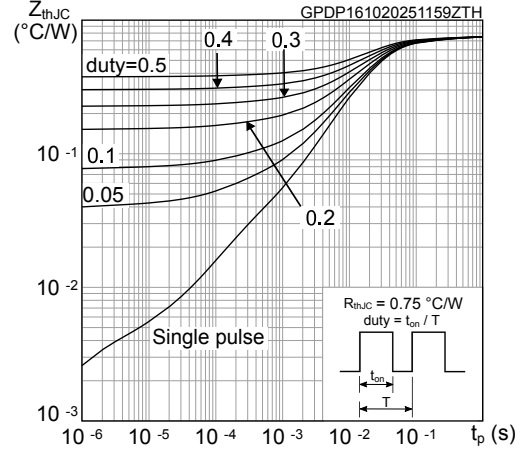
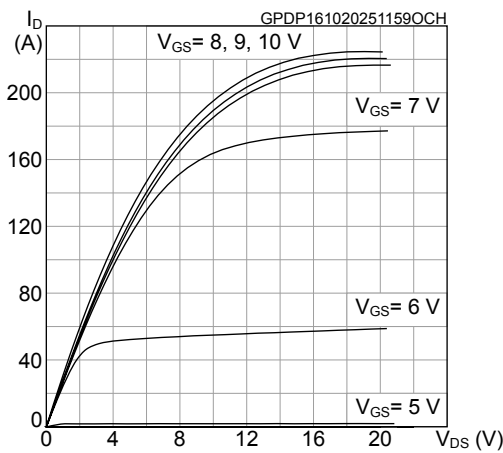
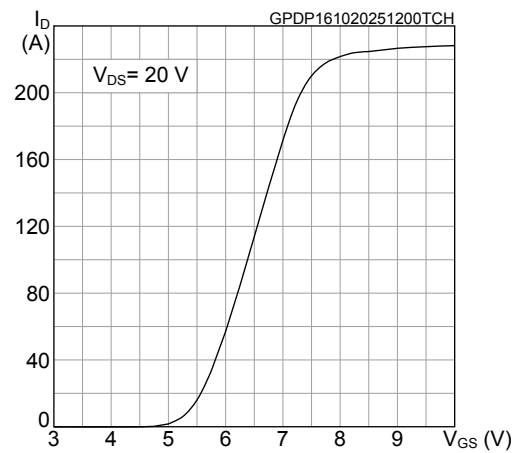
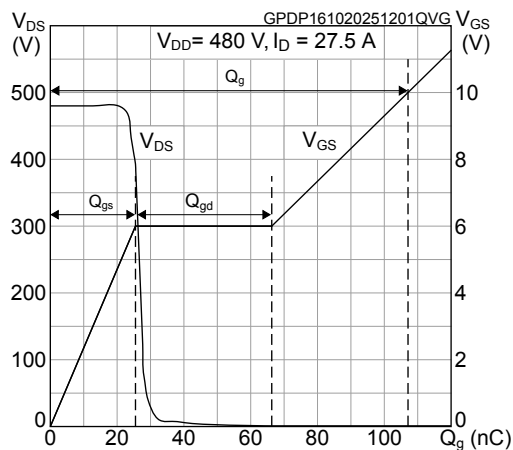
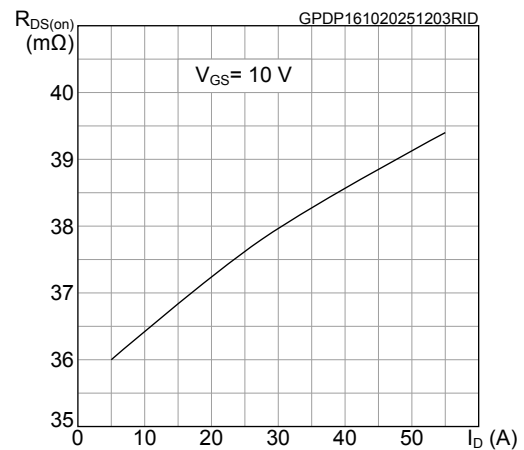
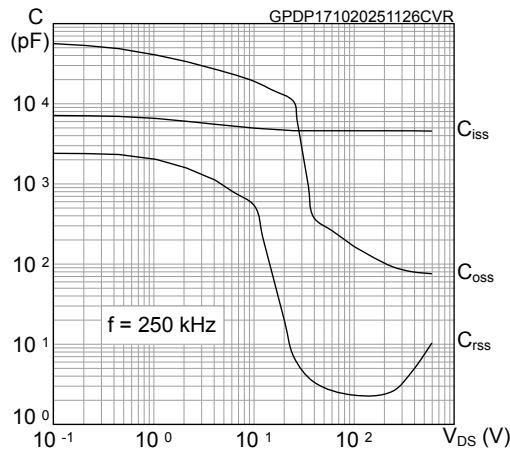
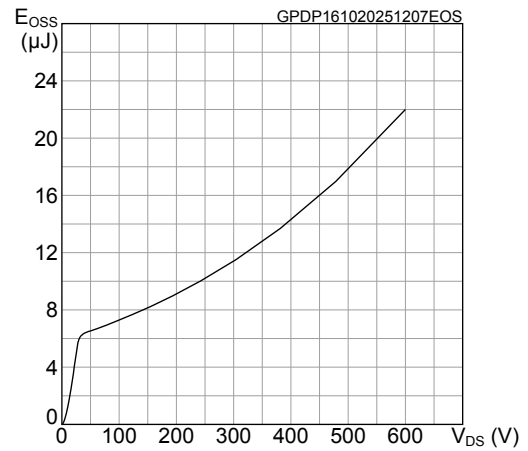
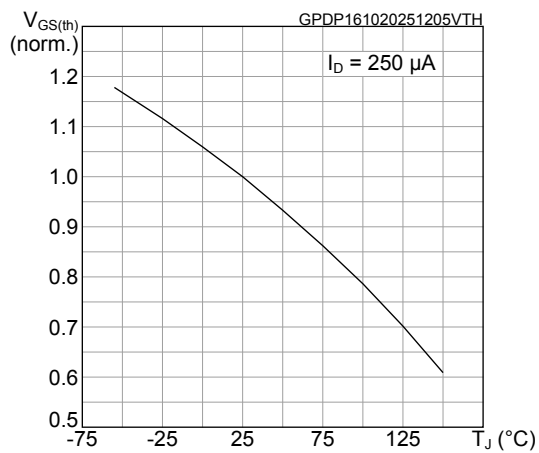
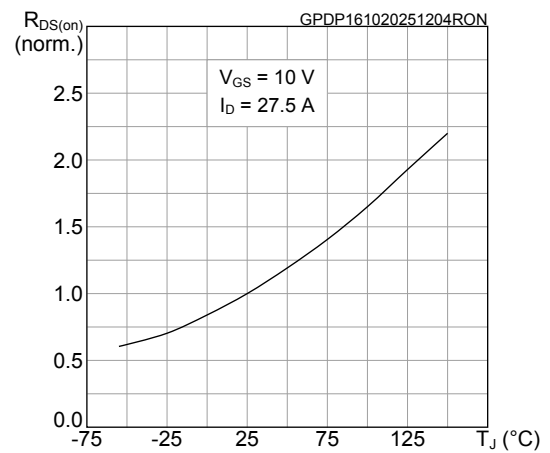
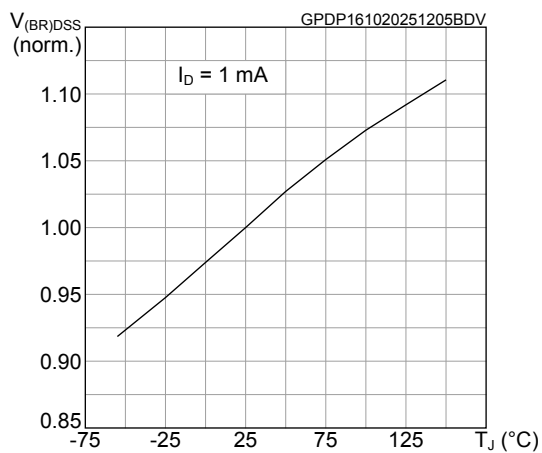
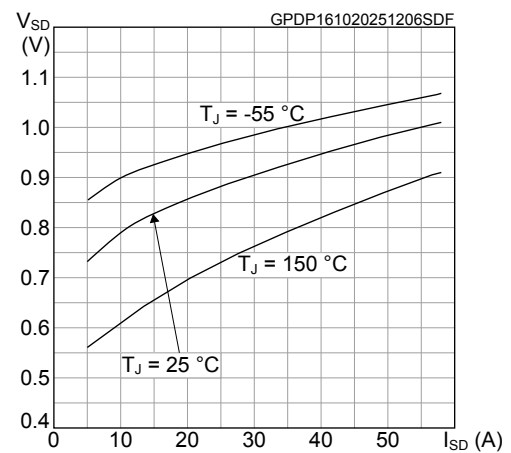
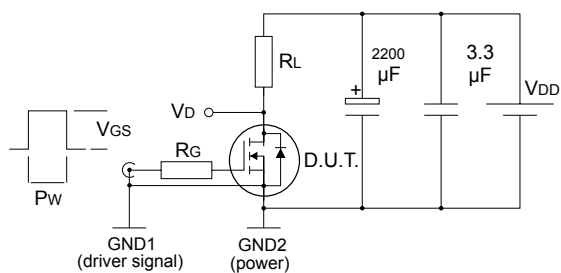
Figure 1. Safe operating area

Figure 2. Maximum transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical drain-source on-resistance


Figure 7. Typical capacitance characteristics

Figure 8. Typical output capacitance stored energy

Figure 9. Normalized gate threshold vs temperature

Figure 10. Normalized on-resistance vs temperature

Figure 11. Normalized breakdown voltage vs temperature

Figure 12. Typical reverse diode forward characteristics


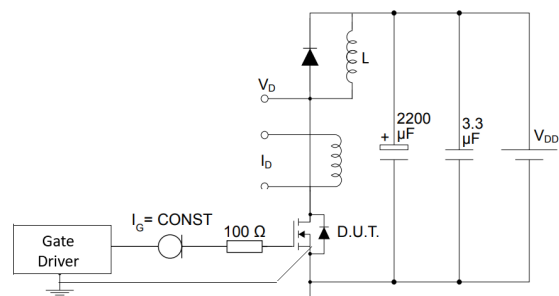
3 Test circuits

Figure 13. Test circuit for resistive load switching times



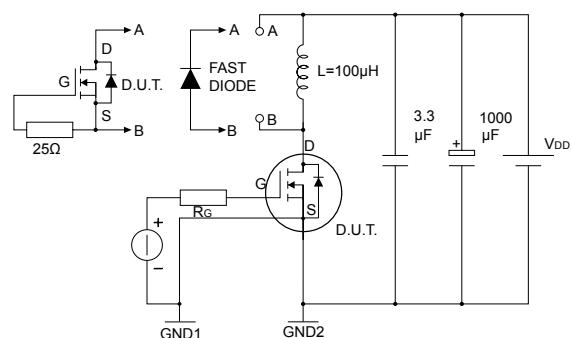
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Figure 14. Test circuit for gate charge behavior



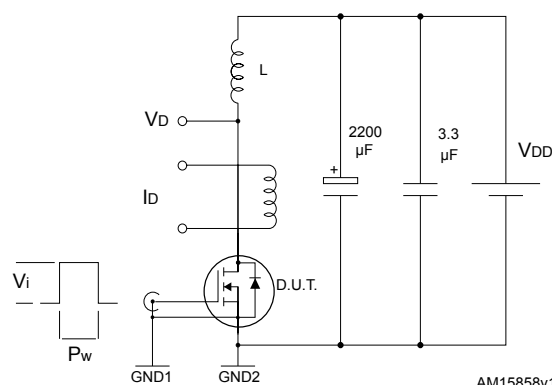
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Figure 15. Test circuit for inductive load switching and diode recovery times



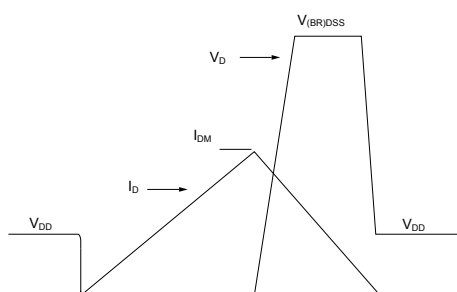
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Figure 16. Unclamped inductive load test circuit



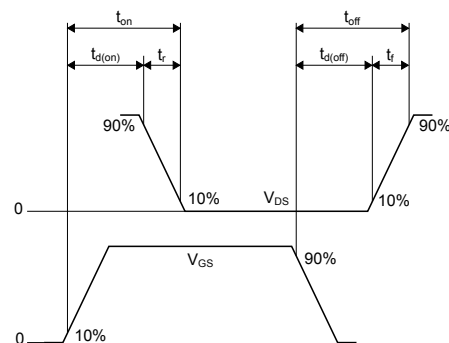
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



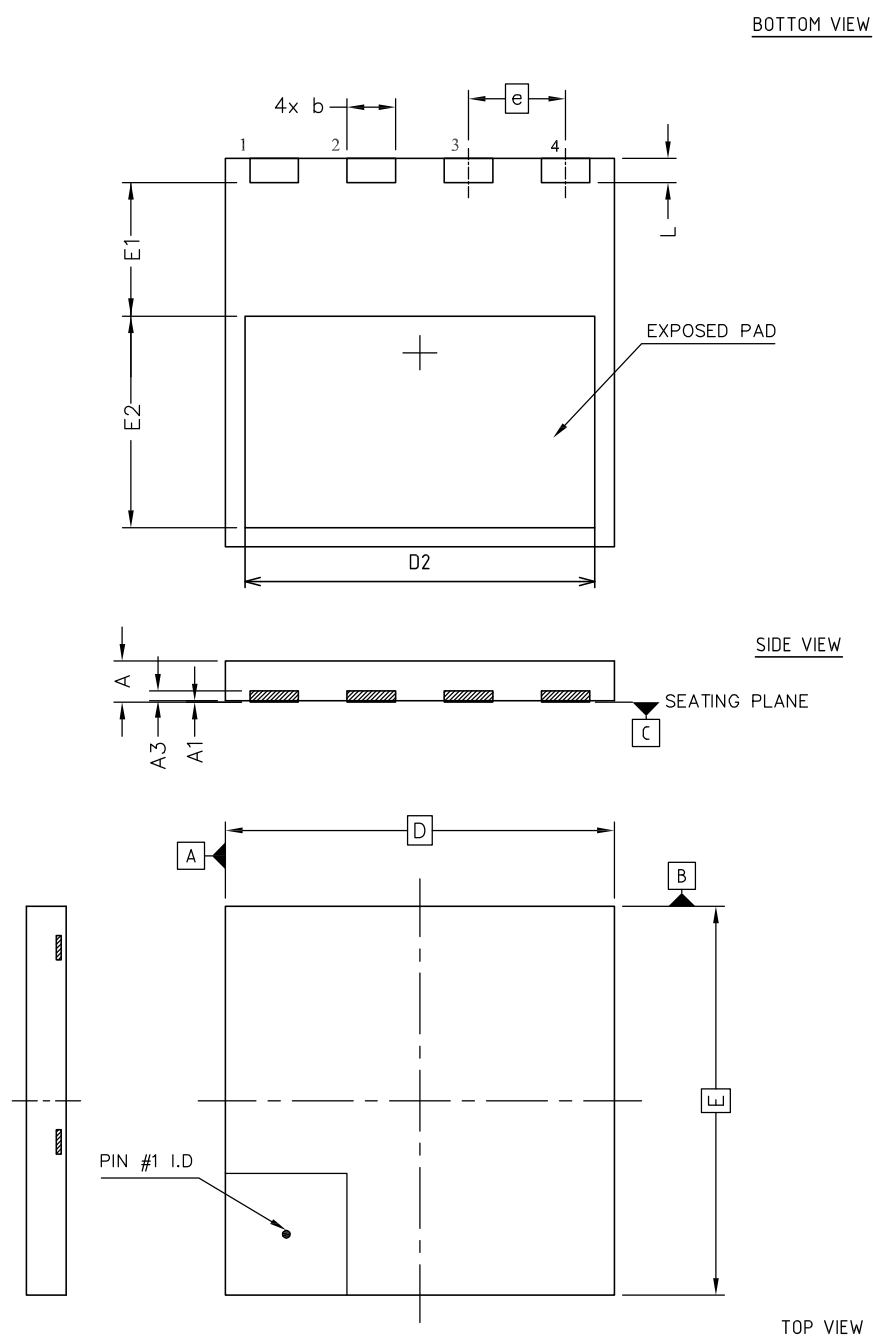
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 8x8 HV type A package information

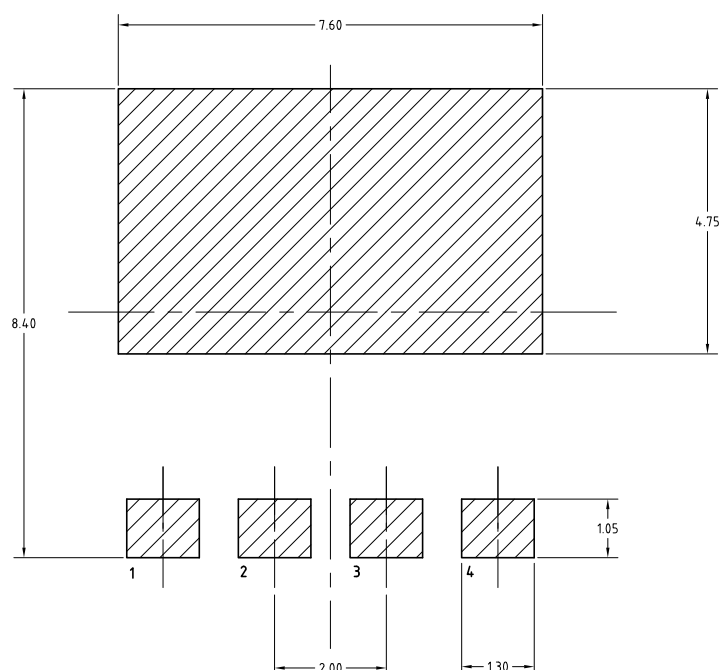
Figure 19. PowerFLAT 8x8 HV type A package outline



8222871_Rev_4

Table 8. PowerFLAT 8x8 HV type A mechanical data

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e	2.00 BSC		
L	0.40	0.50	0.60

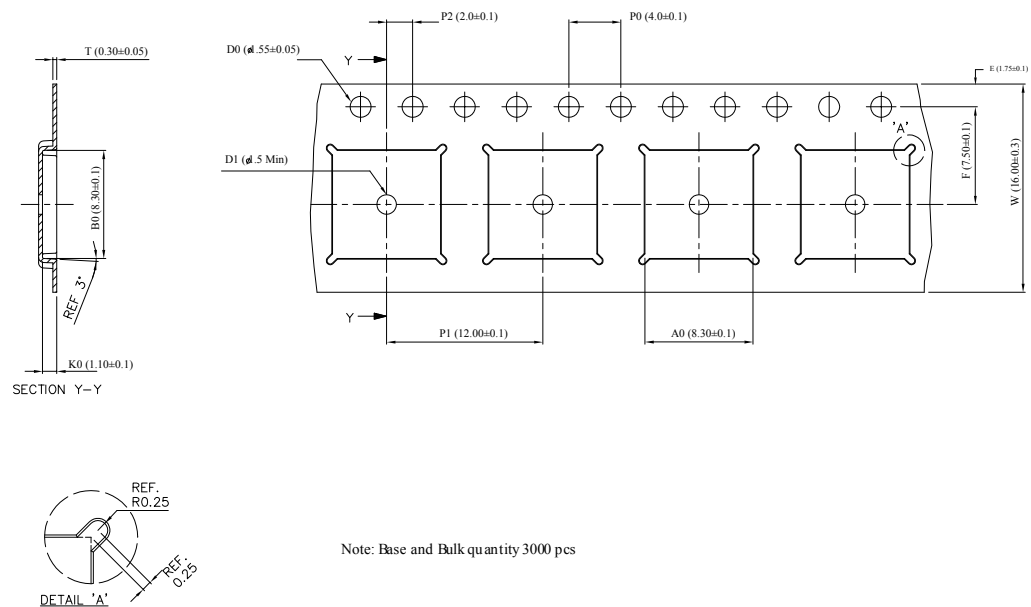
Figure 20. PowerFLAT 8x8 HV footprint


8222871_REV_4_footprint

Note: All dimensions are in millimeters.

4.2 PowerFLAT 8x8 HV packing information

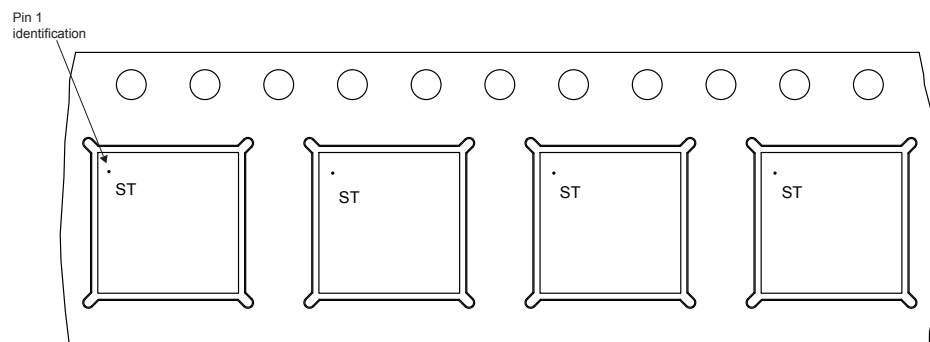
Figure 21. PowerFLAT 8x8 HV tape



8229819_Tape_revA

Note: All dimensions are in millimeters.

Figure 22. PowerFLAT 8x8 HV package orientation in carrier tape



The technical drawing consists of two main views: a top view (left) and a side view (right).

Top View (Left):

- A circular part with three radial slots.
- Dimensions include: $\#21.2 \pm .03$, $R4.6$, $\phi 17$, $\phi 19$, 10.0 , and $4.0W \times 10.0D$ CUT SLOT (3 PLCS).
- A central hole is dimensioned as $\phi 17$.
- A small feature at the bottom is dimensioned as 2.0 .

Side View (Right):

- A cross-sectional view of the circular part.
- Dimensions include: $R57.7$, $R113$, $R50$, $R119$, $6.5 \pm .18$, 120° , 120° , 60° , 16 , 36 , and $6.5 \pm .18$.
- A note "SEE DETAIL C" points to a specific feature.
- A logo for "DETAIL C" is shown below the view.

Bottom View (Far Left):

- A detailed cross-section of a component.
- Dimensions include: $16.4 \pm .02$, $2.4 \pm .04$, 0.6 , $\phi 100 \pm .08$, 2.0 , and $\phi 330.0 \pm .08$.

Note: All dimensions are in millimeters.

Revision history

Table 9. Document revision history

Date	Revision	Changes
20-Oct-2025	1	First release.

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