



Description

The ENP2N7002VR has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

General Features

- $V_{DS} = 60V$ $I_D = 300mA$
 $R_{DS(ON)}(Typ.) = 2\Omega$ @ $V_{GS} = 10V$
 $R_{DS(ON)}(Typ.) = 2.5\Omega$ @ $V_{GS} = 4.5V$
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
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- Lead, Halogen and Antimony Free, RoHS Compliant "Green"
- ESD Protected Up To 2kV

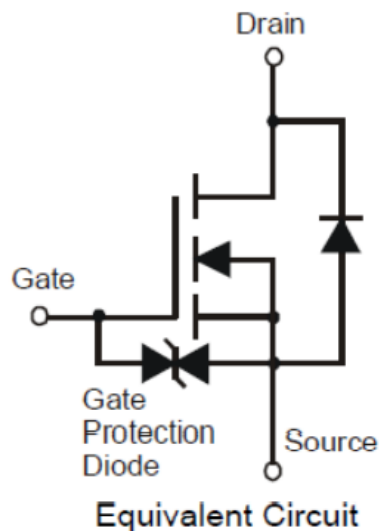
Application

- Motor control
- Power Management Functions
- Backlighting

Package

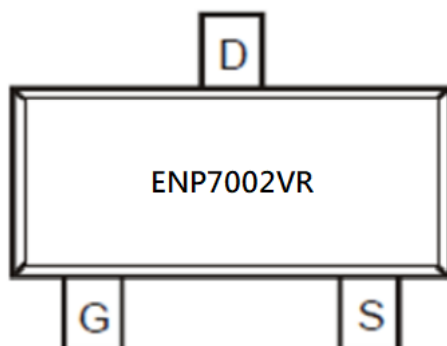
- SOT-23

Schematic diagram



Marking and pin assignment

SOT-23
(TopView)



Ordering Information

ENP2N7002VR XX R

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B1=SOT-23

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter		symbol	limit	unit
Drain-source voltage		V_{DS}	60	V
Gate-source voltage		V_{GS}	±20	V
Continuous Drain Current	TC=25 °C	I_D	380	mA
	TC=70 °C		300	
Pulsed Drain Current		I_{DP}	1.2	A
Maximum power dissipation	TC=25 °C	P_D	540	mW
Operating junction Temperature range		T_j	-55—150	°C

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
		$T_J=85^\circ C$	-	-	30	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 1	μA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.45	2.1	V
Drain-source on-state resistance ¹	$R_{DS(on)}$	$V_{GS}=10V, I_D=380mA$	-	1.7	2	Ω
		$V_{GS}=4.5V, I_D=300mA$	-	2.6	3	
On Status Drain Current	$I_{D(on)}$	$V_{DS}=5V, V_{GS}=10V$	380	-	-	mA
Diode Characteristics						
Diode Forward Voltage ¹	V_{SD}	$I_{SD}=300mA, V_{GS}=0V$	-	0.9	1.1	V
Diode Continuous Forward Current	I_S		-	-	380	mA
Dynamic Characteristics²						
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}=0V, f=1MHz$	-	133	-	m Ω
Input capacitance	C_{ISS}	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$	-	30	-	pF
Output capacitance	C_{OSS}		-	4.2	-	
Reverse transfer capacitance	C_{RSS}		-	2.9	-	
Turn-on delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=30V,$ $R_L=25\Omega, I_D=200mA$	-	3.9	-	ns
Turn-on Rise time	t_r		-	3.4	-	
Turn-off delay time	$t_{D(off)}$		-	15.7	-	
Turn-off Fall time	t_f		-	9.9	-	
Total gate charge	Q_g	$V_{GS}=10V, I_D=200mA$ $V_{DS}=10V$	-	0.3	-	nC
Gate-source charge	Q_{gs}		-	0.2	-	
Gate-drain charge	Q_{gd}		-	0.08	-	

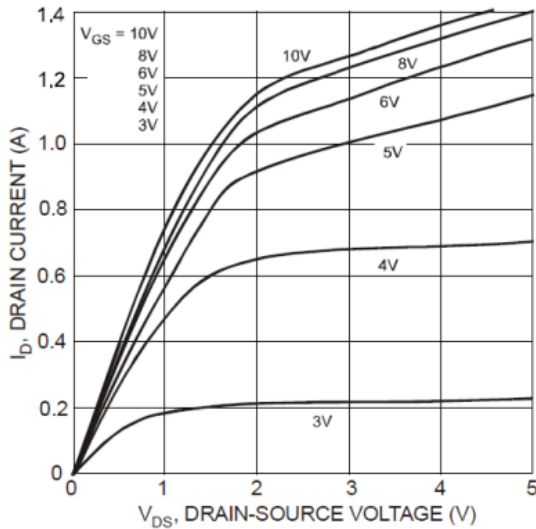
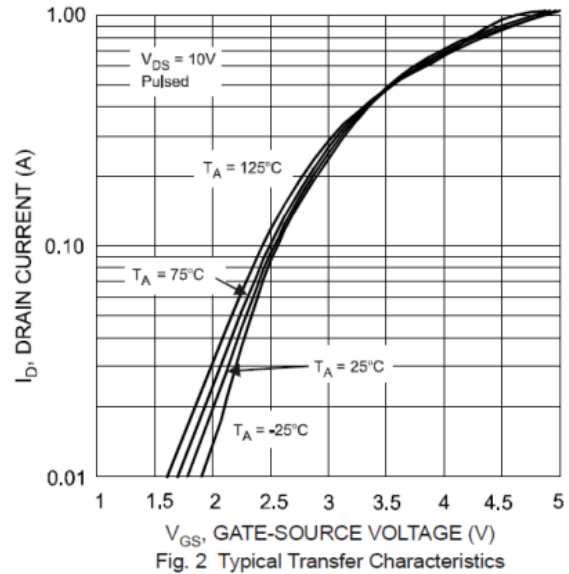
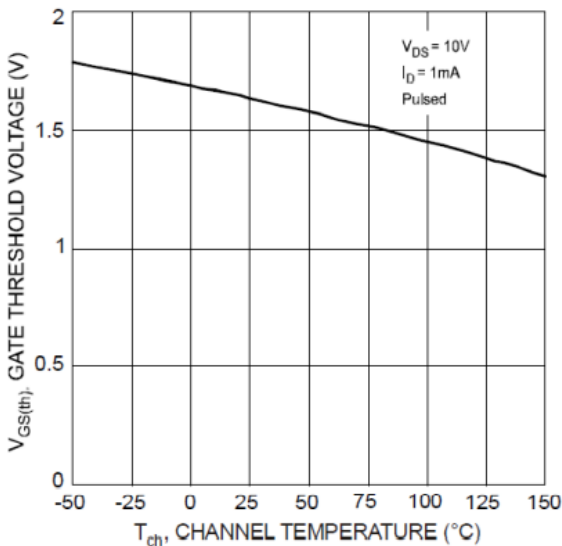
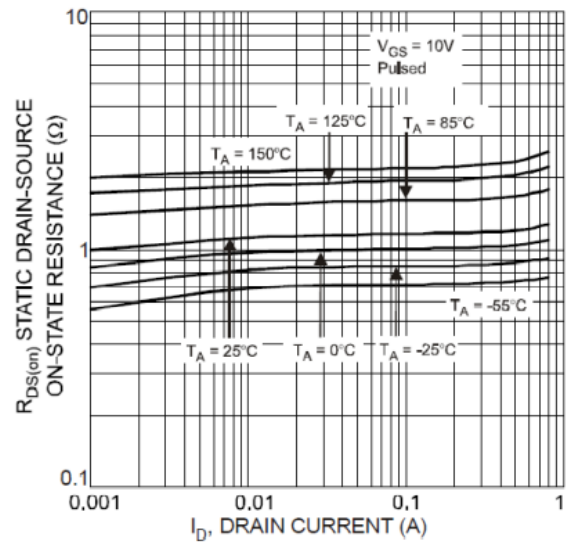
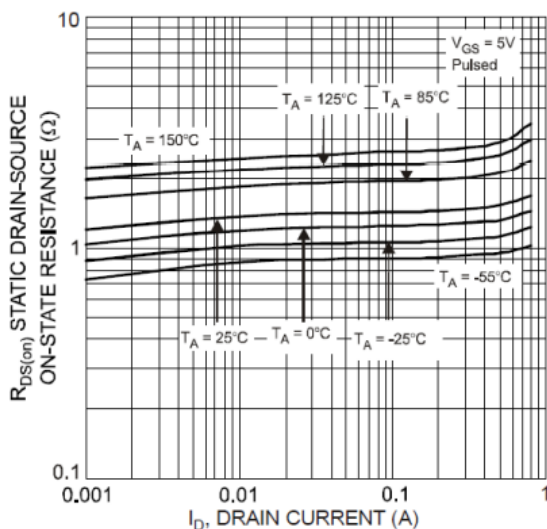
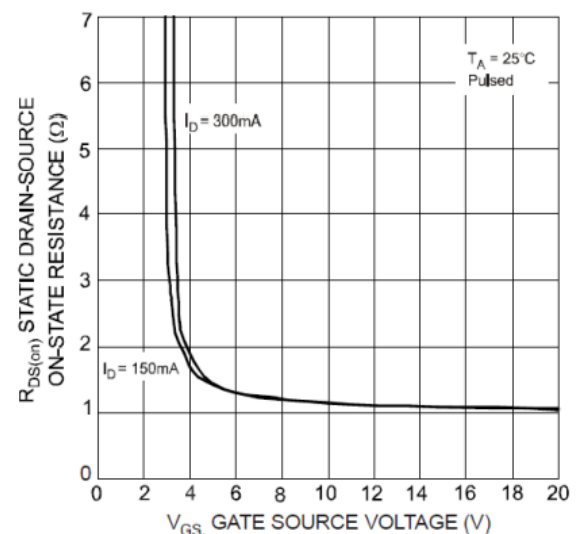
Note: 1: Pulse test; pulse width $\cong 300ns$, duty cycle $\cong 2\%$.

2: Guaranteed by design, not subject to production testing.

Thermal Characteristics

Parameter	Symbol	Typical	Unit
Thermal Resistance-Junction to Case	$R_{\theta jc}$	1.7	$^\circ C/W$
Thermal Resistance junction-to ambient	$R_{\theta ja}$	62.5	

Typical Performance Characteristics



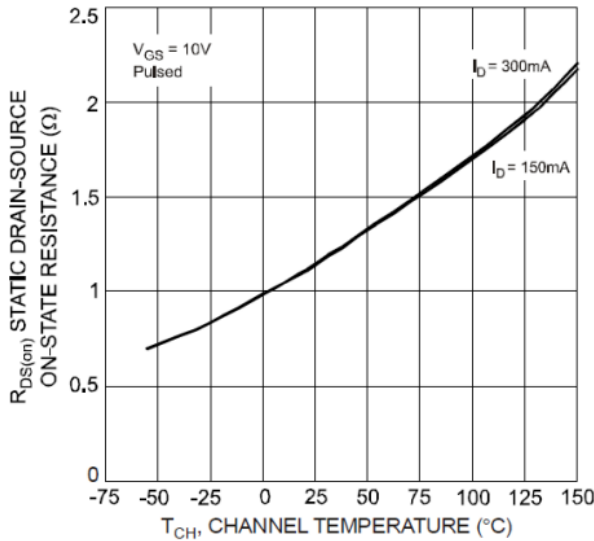


Fig. 7 Static Drain-Source On-State Resistance vs. Channel Temperature

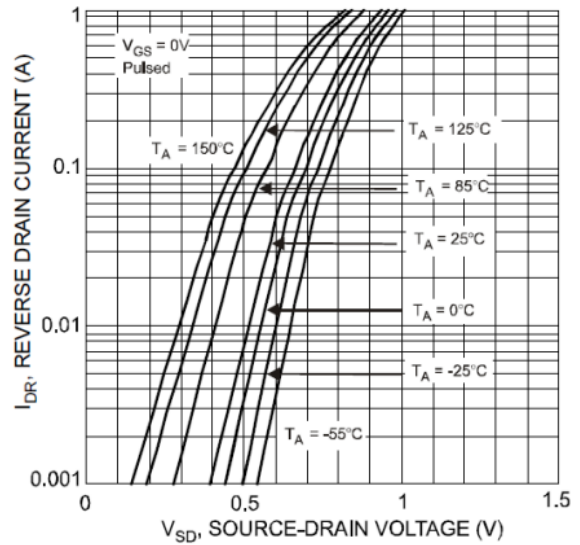


Fig. 8 Reverse Drain Current vs. Source-Drain Voltage

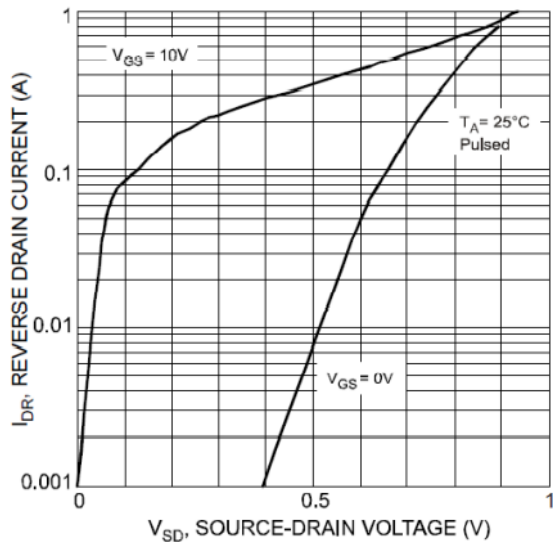


Fig. 9 Reverse Drain Current vs. Source-Drain Voltage

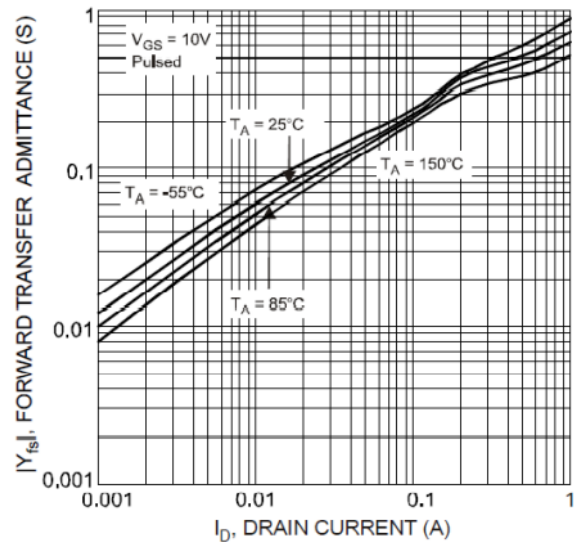


Fig. 10 Forward Transfer Admittance vs. Drain Current

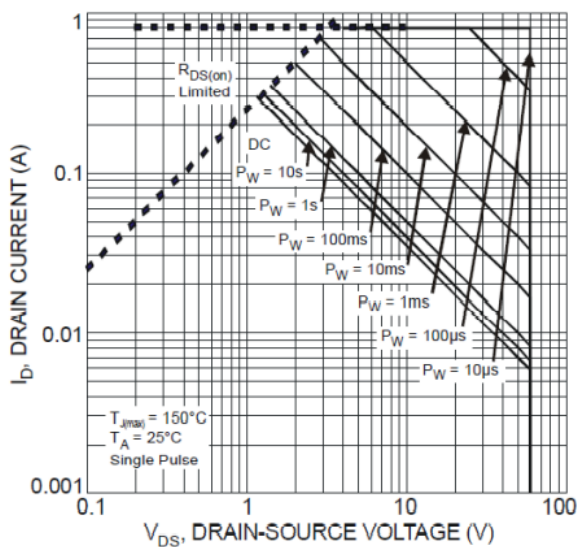


Fig. 11 Safe Operation Area

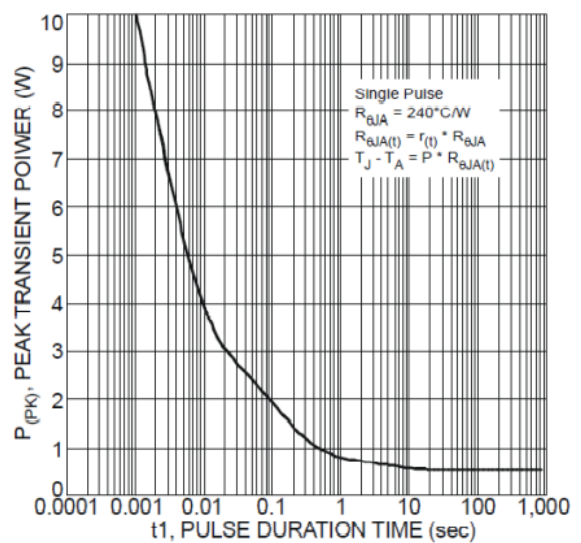
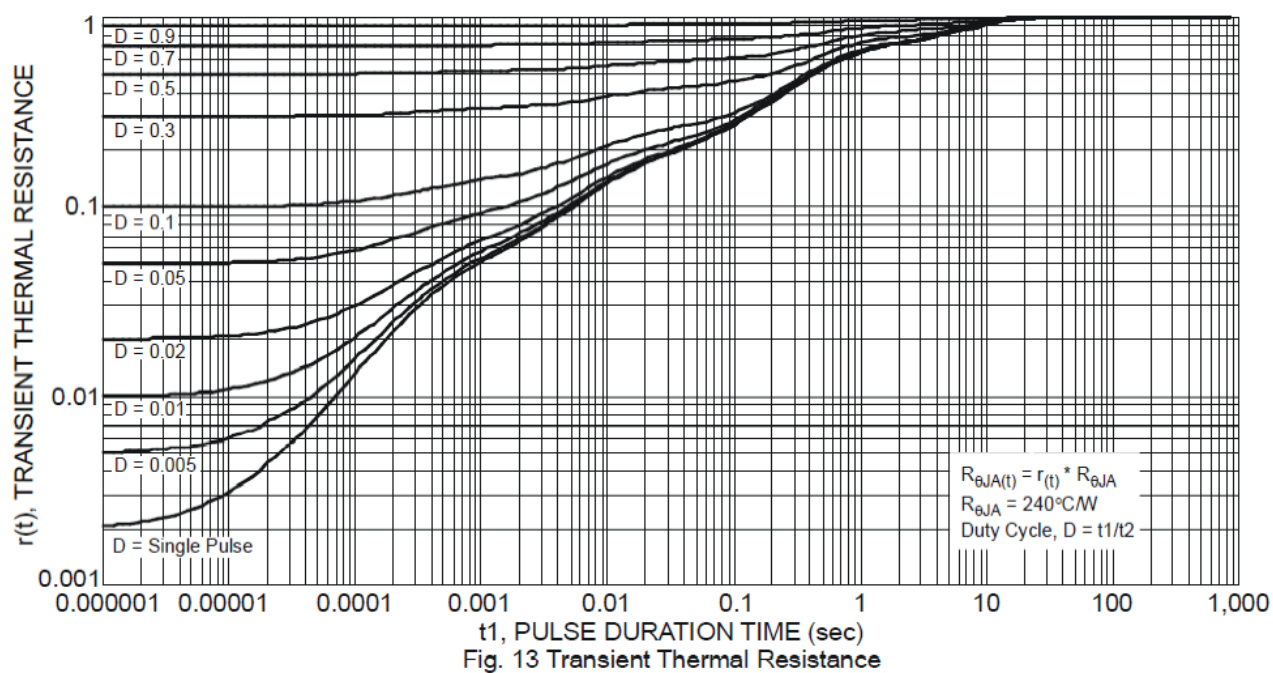
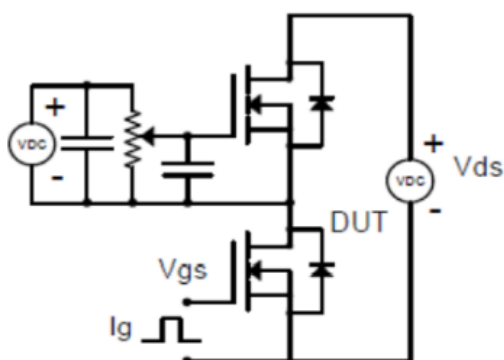
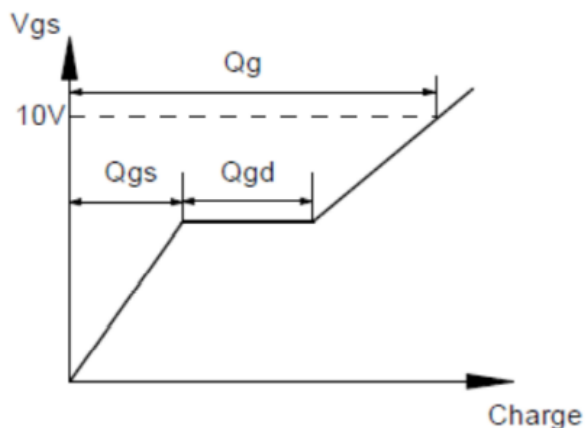


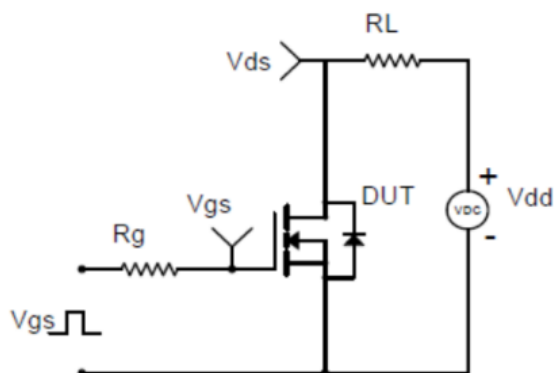
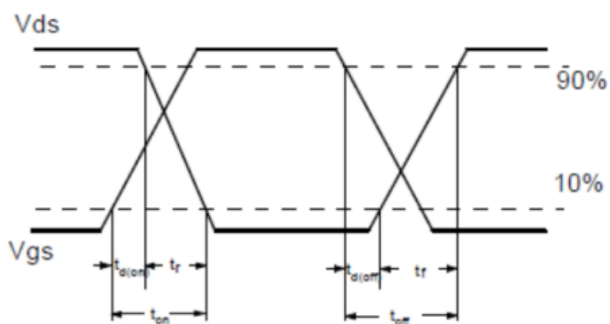
Fig. 12 Single Pulse Maximum Power Dissipation



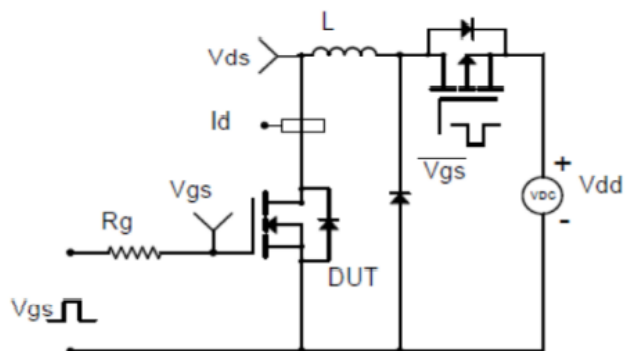
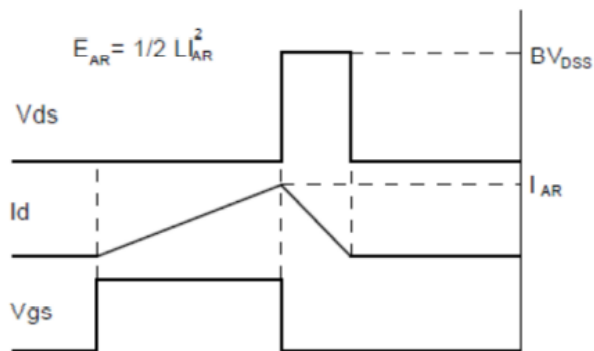
Gate Charge Test Circuit & Waveform



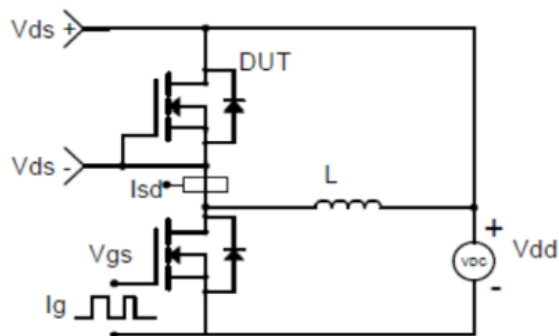
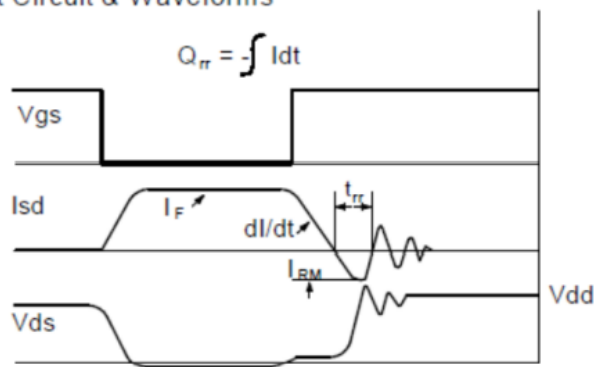
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

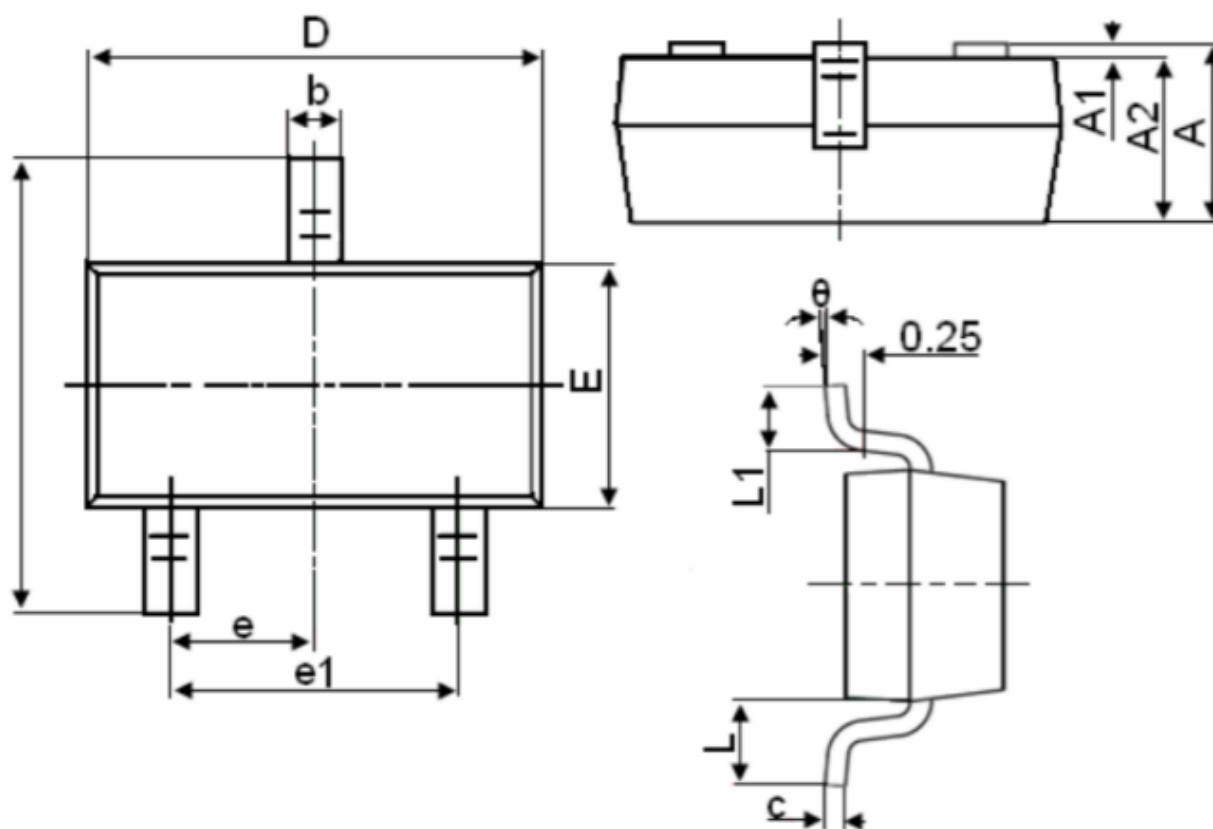


Diode Recovery Test Circuit & Waveforms



Package Information

- SOT-23



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°