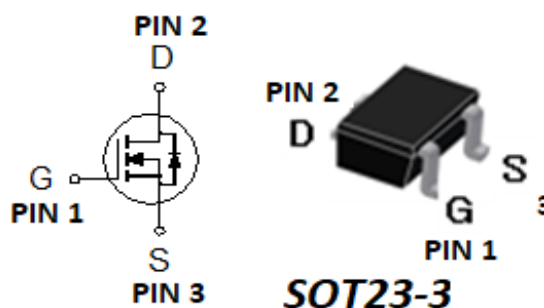


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

• Product Summary:

	N-CH
BV_{DSS}	60V
$R_{DS(on)} (MAX.) @ V_{GS}=10V$	75mΩ
$R_{DS(on)} (MAX.) @ V_{GS}=4.5V$	83mΩ
$I_D @ T_C=25^{\circ}C$	10A
$I_D @ T_A=25^{\circ}C$	2.8A

• Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant

AEC-Q101 Qualified

• ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	10	A
	$T_C = 100^{\circ}C$		7	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	2.8	
	$T_A = 70^{\circ}C$		2	
Pulsed Drain Current ¹		I_{DM}	11	
Avalanche Current		I_{AS}	8	mJ
Avalanche Energy	$L = 1mH$	EAS	32	
Repetitive Avalanche Energy ²	$L = 0.5mH$	EAR	16	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	17.6	W
	$T_C = 100^{\circ}C$		8.8	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	1.3	W
	$T_A = 70^{\circ}C$		0.9	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 175	$^{\circ}C$

• 100% UIS testing in condition of $V_D=40V$, $L=1mH$, $V_G=10V$, $I_L=5A$, Rated $V_{DS}=60V$ N-CH

• THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	UNIT
Junction-to-Lead		$R_{\theta JC}$	8.5	$^{\circ}C/W$
Junction-to-Ambient ³	$t \leq 10s$	$R_{\theta JA}$	77	
	Steady-State	$R_{\theta JA}$	114	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $< 1\%$

³The value of $R_{\theta JA}$ is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}C$.

⁴Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	60			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.9	1.5	2.0	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±16V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V			1	μA
		V _{DS} =60V, V _{GS} =0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	10			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 5A		63	75	mΩ
		V _{GS} = 4.5V, I _D = 3A		69	83	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 5A		15		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 30V, f = 1MHz		544		pF
Output Capacitance ⁵	C _{oss}			39		
Reverse Transfer Capacitance ⁵	C _{rss}			32		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.3		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 30V, V _{GS} = 10V, I _D = 5A		16		nC
	Q _g (V _{GS} =4.5V)			8		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			3		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 30V, V _{GS} = 10V, I _D = 5A , R _g = 6Ω		5		nS
Rise Time ^{1,2,5}	t _r			7		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			24		
Fall Time ^{1,2,5}	t _f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				10	A
Pulsed Current ³	I _{SM}				11	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		16		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			2.2		A
Reverse Recovery Charge ⁵	Q _{rr}			12		nC

¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

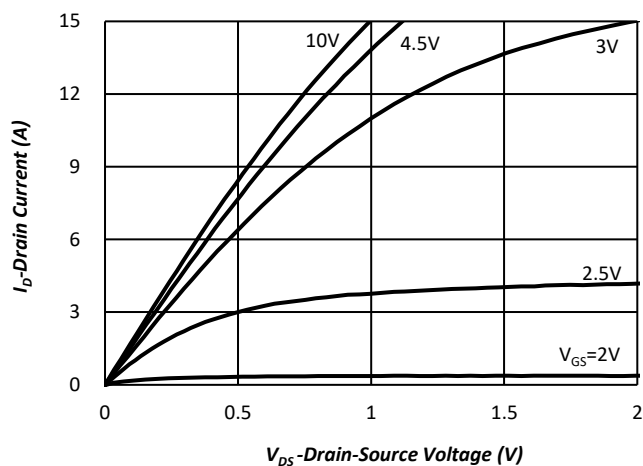
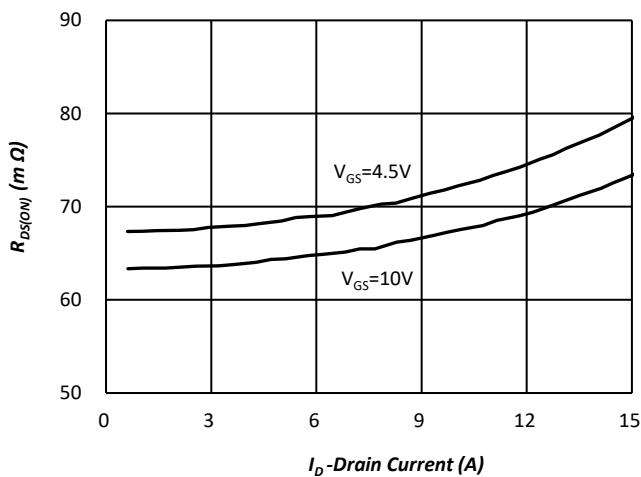
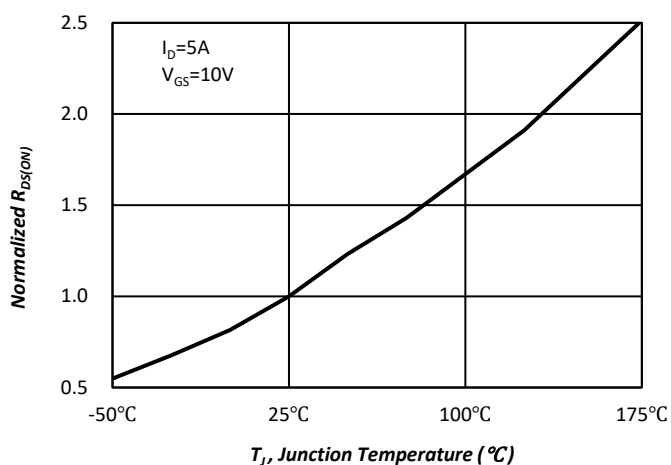
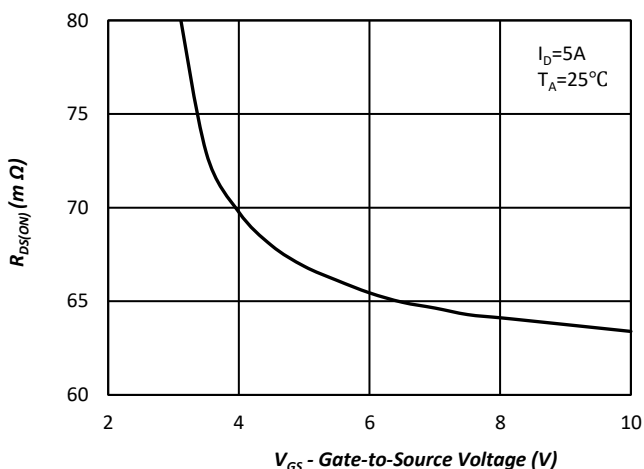
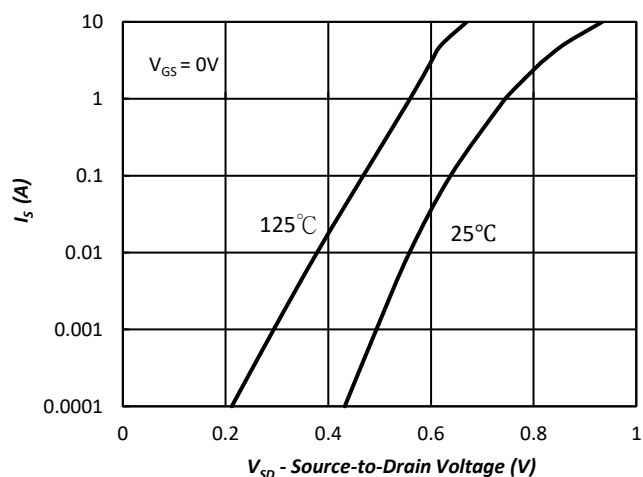
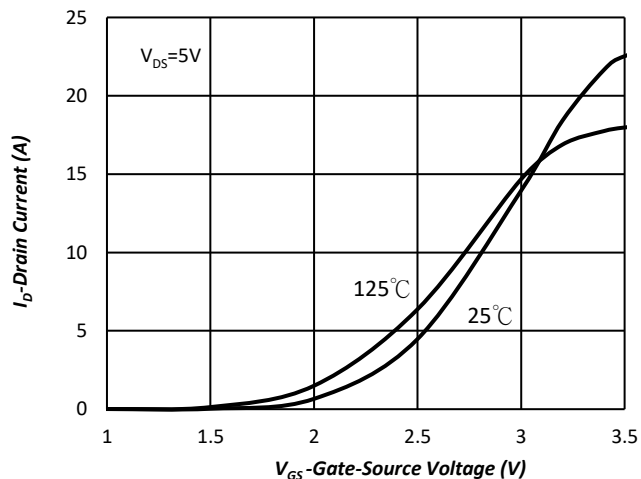
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

•TYPICAL CHARACTERISTICS



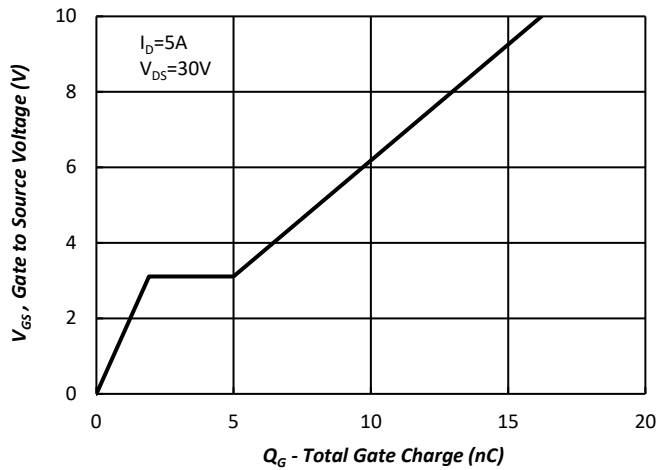


Fig.7 Gate Charge Characteristics

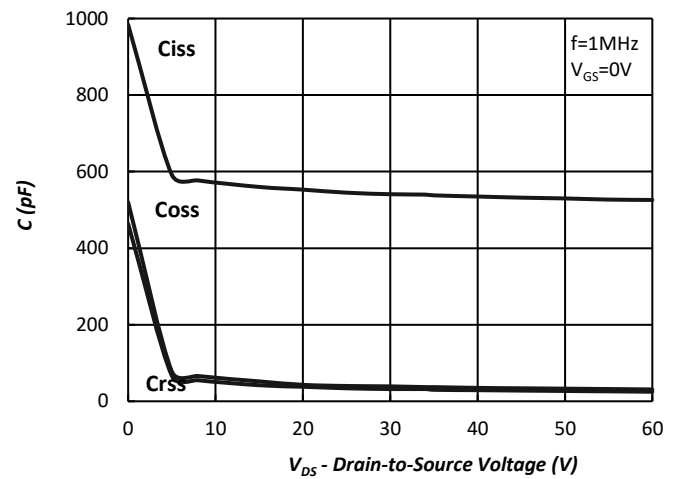


Fig.8 Typical Capacitance Characteristics

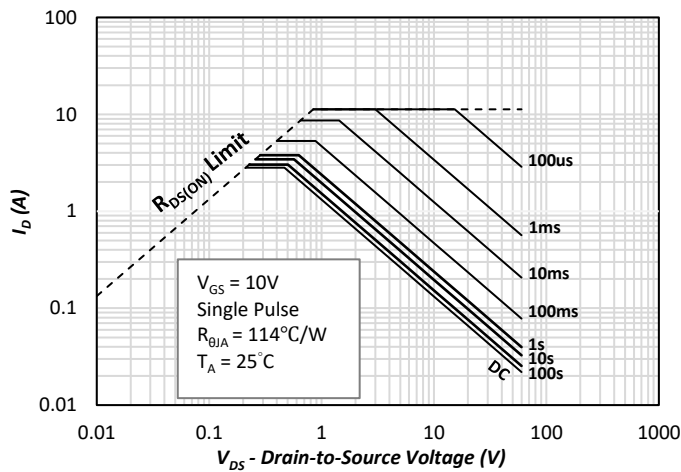


Fig.9. Maximum Safe Operating Area

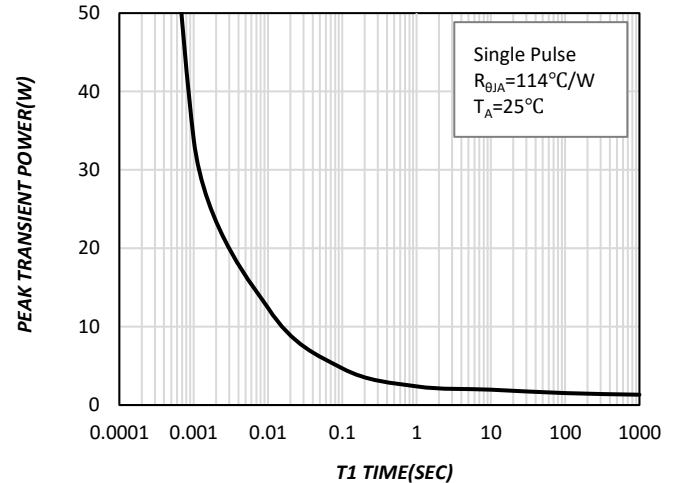


Fig.10. Single Pulse Maximum Power Dissipation

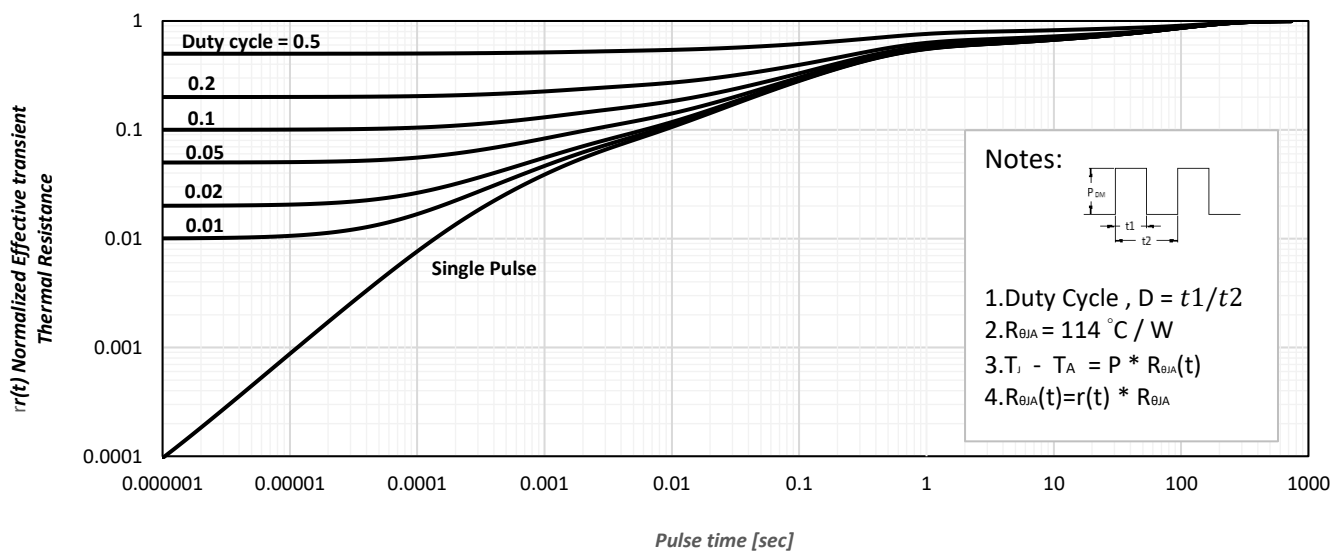


Fig.11. Effective Transient Thermal Impedance

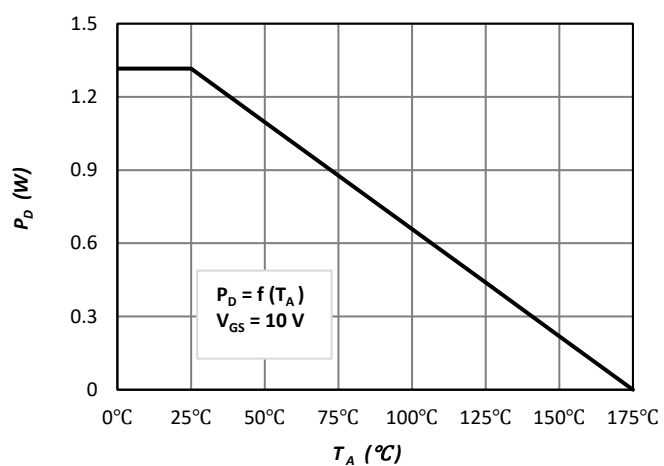


Fig.12 Power dissipation

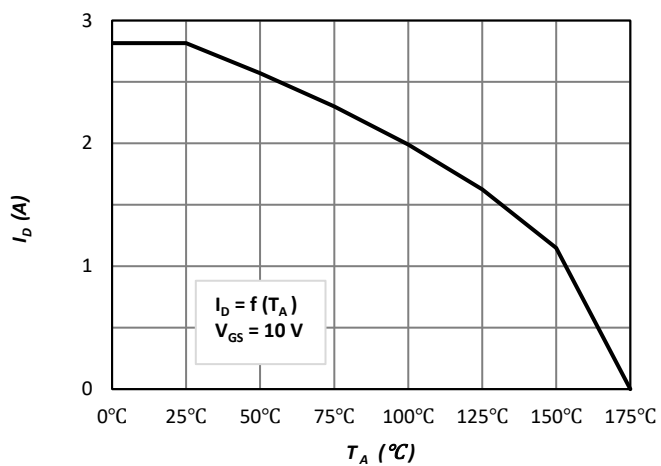
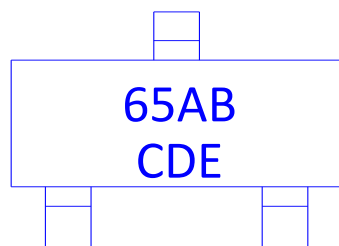


Fig.13 Drain current

Ordering & Marking Information:

Device Name: EMVB70N06JS for SOT23-3



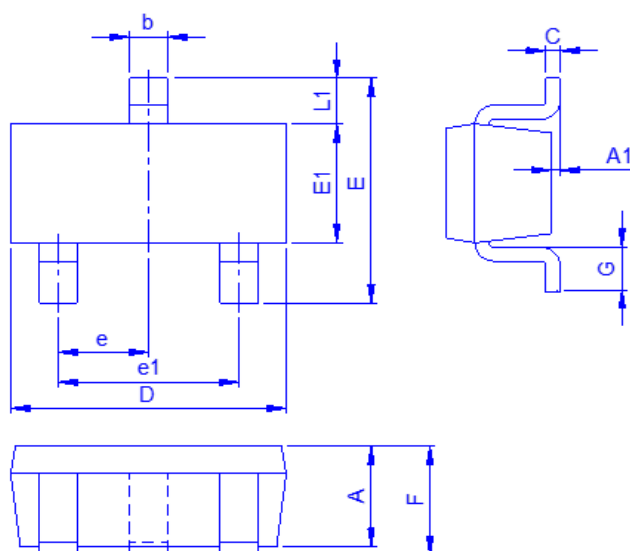
65 for EMVB70N06JS

A: Year(A:2008 B:2009 C:2010....)

B: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

CDE: Serial No.

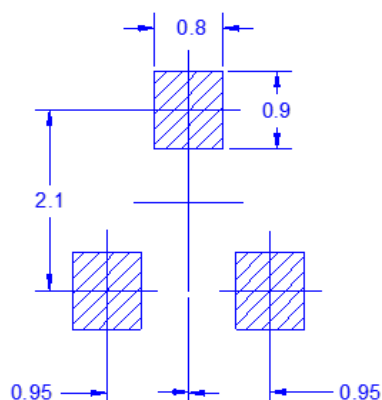
Outline Drawing



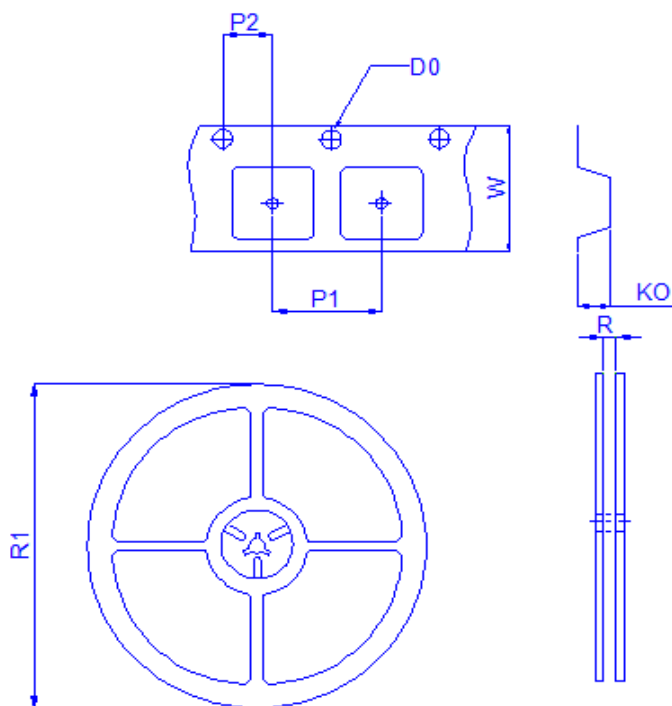
Dimension in mm

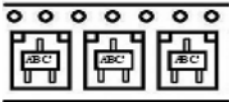
Dimension	A	A1	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.88	-	0.3	0.13	2.8	2.25	1.2	0.9	1.8	0.89	0.3	
Typ.	0.95	-	0.4	0.17	2.9	2.5	1.3	0.95	1.9		0.45	0.55
Max.	1.1	0.1	0.5	0.2	3	2.64	1.4	1	2	1.15	0.6	

Footprint



◆ Tape&Reel Information:3000pcs/Reel



Package	SOT23-3
Reel	7"
Device orientation	<p>FEED DIRECTION</p> 

Dimension in mm

Dimension	Carrier tape					Reel	
	D0	K0	P1	P2	W	R	R1
Typ.	1.53	1.45	4	2	8	8.5	178
±	0.2	0.5	0.2	0.2	0.5	REF	REF