# GD25LQ64H

# DATASHEET

# 1 FEATURES

◆ 64M-bit Serial NOR Flash Memory
- 8M-Byte
- 256 Bytes per programmable page

◆ Standard, Dual, Quad SPI, QPI, DTR
- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#, RESET#
- Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#, RESET#
- Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3, RESET#
- QPI: SCLK, CS#, IO0, IO1, IO2, IO3, RESET#
- SPI DTR (Double Transfer Rate) Read

◆ High Speed Clock Frequency
- 133MHz for fast read
- Dual I/O Data transfer up to 266Mbits/s
- Quad I/O Data transfer up to 532Mbits/s
- QPI Mode Data transfer up to 532Mbits/s
- DTR Dual I/O Data transfer up to 416Mbits/s
- DTR Quad I/O Data transfer up to 832Mbits/s

◆ Software Write Protection
- Write protect all/portion of memory via software
- Enable/Disable protection with WP# Pin
- Top/Bottom Block protection

◆ Endurance and Data Retention
- Minimum 100,000 Program/Erase Cycles
- 20-year data retention typical

◆ Allows XiP (eXecute In Place) Operation
- High speed Read reduce overall XiP instruction fetch time
- Continuous Read with Wrap further reduce data latency to fill up SoC cache

◆ Fast Program/Erase Speed
- Page Program time: 0.18ms typical
- Sector Erase time: 40ms typical
- Block Erase time: 0.1s/0.16s typical
- Chip Erase time: 10s typical

◆ Flexible Architecture
- Uniform Sector of 4K-Byte
- Uniform Block of 32/64K-Byte

◆ Low Power Consumption
- 10μA typical standby current
- 1μA typical deep power down current

◆ Advanced Security Features
- 128-bit Unique ID for each device
- Serial Flash Discoverable parameters (SFDP) register
- 3x1024-Byte Security Registers With OTP Locks

◆ Single Power Supply Voltage
- Full voltage range: 1.65-2.0V

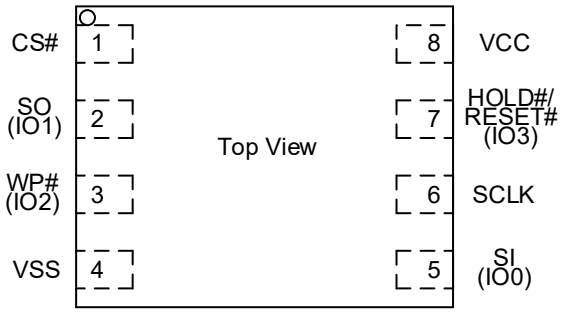
◆ Package Information
- USON8 (3x4mm)
- USON8 (4x4mm)
- SOP8 150mil
- WSON8 (6x5mm)
- SOP8 208mil

# 2 GENERAL DESCRIPTIONS

The GD25LQ64H (64M-bit) Serial NOR Flash supports the standard Serial Peripheral Interface (SPI), the Dual and DTR Dual SPI, and the Quad and DTR Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), I/O3 (HOLD#/ RESET#). The Dual I/O data is transferred with speed of 266Mbit/s, The Quad I/O data is transferred with speed of 532Mbit/s. The DTR Dual I/O data is transferred with speed of 416Mbits/s, and the DTR Quad I/O data is transferred with speed of 832Mbits/s.

## CONNECTION DIAGRAM AND PIN DESCRIPTION

**Figure 1 Connection Diagram for USON8/WSON8 package**




8 - LEAD USON/WSON

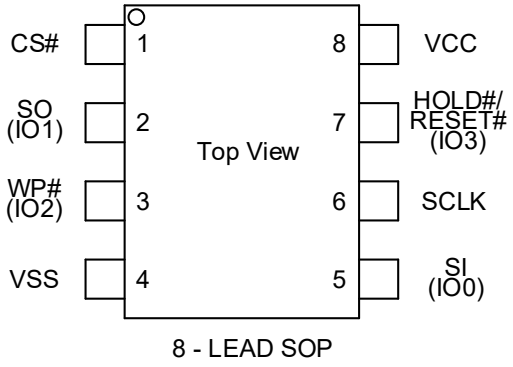
**Table 1. Pin Description for USON8/WSON8 Package**

| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | CS# | I | Chip Select Input |
| 2 | SO (IO1) | I/O | Data Output (Data Input Output 1) |
| 3 | WP# (IO2) | I/O | Write Protect Input (Data Input Output 2) |
| 4 | VSS | | Ground |
| 5 | SI (IO0) | I/O | Data Input (Data Input Output 0) |
| 6 | SCLK | I | Serial Clock Input |
| 7 | HOLD#/RESET# (IO3) | I/O | Hold or Reset Input (Data Input Output 3) |
| 8 | VCC | | Power Supply |

Note:

1. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.
2. WP# functions are only available for Standard/Dual/DTR Dual SPI.

**Figure 2 Connection Diagram for SOP8 package**




8 - LEAD SOP

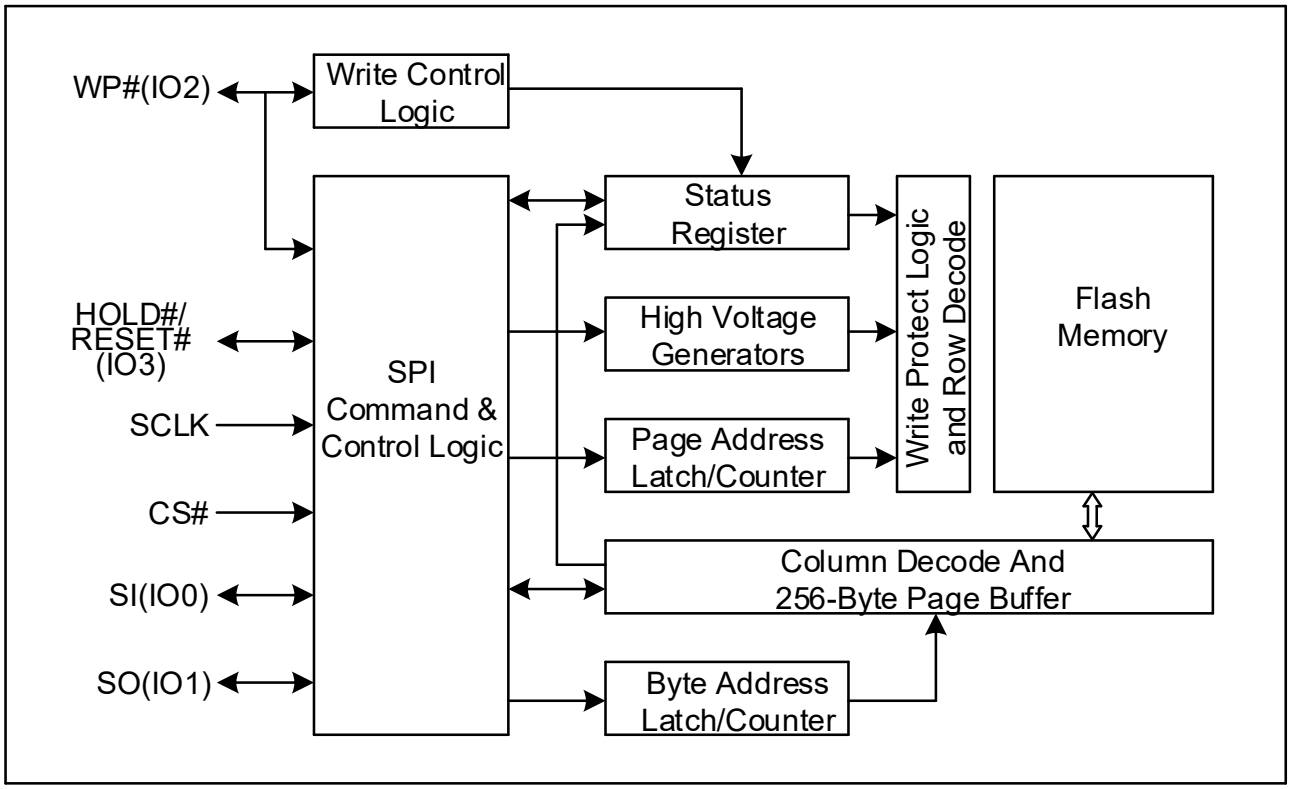
**Table 2. Pin Description for SOP8 Package**

| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | CS# | I | Chip Select Input |
| 2 | SO (IO1) | I/O | Data Output (Data Input Output 1) |
| 3 | WP# (IO2) | I/O | Write Protect Input (Data Input Output 2) |
| 4 | VSS | | Ground |
| 5 | SI (IO0) | I/O | Data Input (Data Input Output 0) |
| 6 | SCLK | I | Serial Clock Input |
| 7 | HOLD#/RESET# (IO3) | I/O | Hold or Reset Input (Data Input Output 3) |
| 8 | VCC | | Power Supply |

Note:

1. CS# must be driven high if chip is not selected. Please don’t leave CS# floating any time after power is on.
2. WP# functions are only available for Standard/Dual/DTR Dual SPI.

## BLOCK DIAGRAM



# 3 MEMORY ORGANIZATION

### GD25LQ64H

| Each device has | Each block has | Each sector has | Each page has | |
|---|---|---|---|---|
| 8M | 64/32K | 4K | 256 | Bytes |
| 32K | 256/128 | 16 | - | pages |
| 2K | 16/8 | - | - | sectors |
| 128/256 | - | - | - | blocks |

### UNIFORM BLOCK SECTOR ARCHITECTURE

**GD25LQ64H 64K Bytes Block Sector Architecture**

| Block | Sector | Address range | |
|---|---|---|---|
| 127 | 2047 | 7FF000H | 7FFFFFH |
| | ..... | ..... | ..... |
| | 2032 | 7F0000H | 7F0FFFH |
| 126 | 2031 | 7EF000H | 7EFFFFH |
| | ..... | ..... | ..... |
| | 2016 | 7E0000H | 7E0FFFH |
| ..... | ..... | ..... | ..... |
| | ..... | ..... | ..... |
| | ..... | ..... | ..... |
| ..... | ..... | ..... | ..... |
| | ..... | ..... | ..... |
| | ..... | ..... | ..... |
| 2 | 47 | 02F000H | 02FFFFH |
| | ..... | ..... | ..... |
| | 32 | 020000H | 020FFFH |
| 1 | 31 | 01F000H | 01FFFFH |
| | ..... | ..... | ..... |
| | 16 | 010000H | 010FFFH |
| 0 | 15 | 00F000H | 00FFFFH |
| | ..... | ..... | ..... |
| | 0 | 000000H | 000FFFH |

# 4 DEVICE OPERATIONS

## 4.1 SPI Mode

**Standard SPI**

The GD25LQ64H features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

**Dual SPI**

The GD25LQ64H supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3Bh and BBh) commands. These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI commands, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

**Quad SPI**

The GD25LQ64H supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad I/O Fast Read” (6Bh, EBh) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI commands, the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and the WP# and HOLD# pins become bidirectional I/O pins: IO2 and IO3. The Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register set to 1.

**DTR Dual SPI**

The GD25LQ64H supports DTR Dual SPI operation when using the “DTR Dual I/O Fast Read” (BDh) command. This command allows data to be transferred to or from the device at four times the rate of the standard SPI, and data output will be latched on both rising and falling edges of the serial clock. When using the DTR Dual SPI command, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

**DTR Quad SPI**

The GD25LQ64H supports DTR Quad SPI operation when using the “DTR Quad I/O Fast Read” (EDh) command. This command allows data to be transferred to or from the device at eight times the rate of the standard SPI, and data output will be latched on both rising and falling edges of the serial clock. When using the DTR Quad SPI command, the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and the WP# and HOLD# pins become bidirectional I/O pins: IO2 and IO3. For GD25LQ64H, the Quad Enable (QE) bit of status Register must be set to 1 before sending the “DTR Quad I/O Fast Read” command

## 4.2 QPI Mode

The GD25LQ64H supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enable the QPI (38h)” command. The QPI mode utilizes all four IO pins to input the command code. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. “Enable the QPI (38h)” and “Disable the QPI (FFh)” commands are used to switch between these two modes. Upon power-up and Hardware Reset and JEDEC RESET or after Software Reset using “Enable Reset (66h) and Reset (99h)” command, the default state of the device is Standard/Dual/Quad SPI mode. The QPI commands require the non-volatile Quad Enable bit (QE) in Status Register set to 1.

## 4.3 HOLD Function

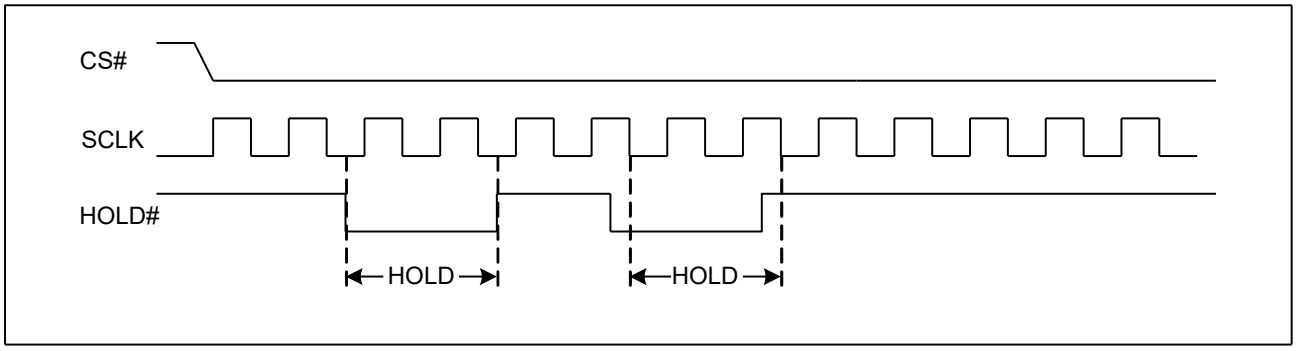
The HOLD/RST bit is used to determine whether HOLD or RESET function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0, the HOLD#/RESET# pin acts as HOLD# pin. The HOLD function is available when QE=0. If QE=1, The HOLD function is disabled, and the HOLD#/RESET# pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, except the operation of write status register, programming, or erasing in progress.

The operation of HOLD needs CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low. If SCLK is not low, HOLD operation will not start until SCLK is low. The HOLD condition ends on rising edge of HOLD# signal with SCLK being low. If SCLK is not low, HOLD operation will not end until SCLK is low.

The SO is high impedance, both SI and SCLK don't care during the HOLD operation. If CS# is driven high during HOLD operation, it will reset the internal logic of the device. To re-start communication with the chip, the HOLD# must be at high and then CS# must be at low.

**Figure 3 HOLD Condition**



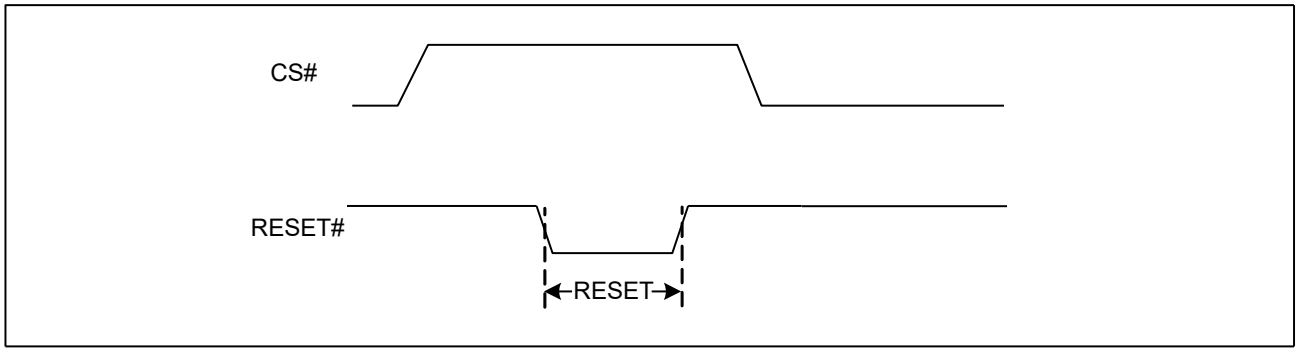

## 4.4 RESET Function

The HOLD/RST bit is used to determine whether HOLD or RESET function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=1, the HOLD#/RESET# pin acts as RESET# pin. The hardware RESET function is available when QE=0. If QE=1, The RESET function is disabled, and the HOLD#/RESET# pin acts as dedicated data I/O pin. For 16-pin and 24-ball packages, a dedicated RESET# is used to do the hardware RESET and it is independent of QE bit setting. The RESET# pin goes low for a minimum period of tRLRH (1μs) will reset the flash. After reset cycle, the flash is at the following states:

-Standby mode

-All the volatile bits will return to the default status as power on.

**Figure 4. RESET Condition**

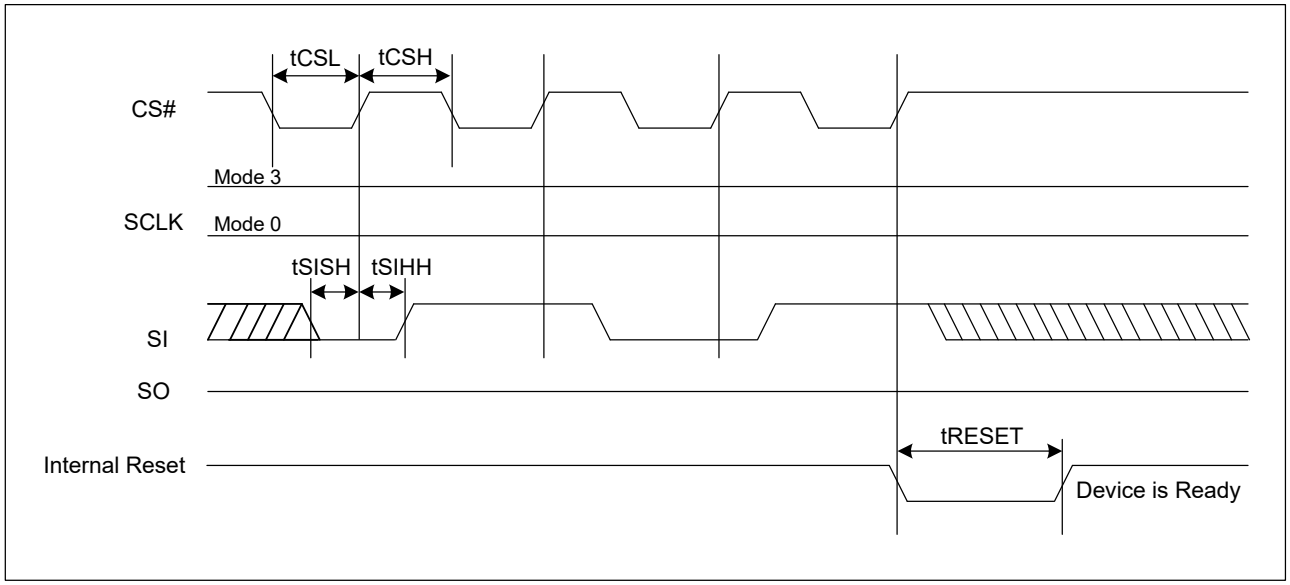


JEDEC RESET is JEDEC-JESD252.01 compliance, which specifies a signaling protocol to perform a hardware reset by using only the CS#, SCLK, and the SI pin without a dedicated hardware RESET# pin.

The procedure of initiating the reset request is: CS# goes low → SCLK remains stable in either a high or low state → SI pin goes low by the host, simultaneously with CS# going low → CS# goes high.

As soon as the fourth CS# is driven high, the device will take approximately $t_{RESET}$ = 100ms to reset. Please note that SI is low on the first CS# pulse, high on the second CS# pulse, low on the third CS# pulse, high on the fourth CS# pulse. This provides a 5h pattern to differentiate it from random noise.

**Figure 5. JEDEC RESET Signaling Protocol**



# 5 DATA PROTECTION

The GD25LQ64H provide the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  -Power-Up / Hardware Reset / Software Reset (66h+99h) / JEDEC RESET
  -Write Disable (WRDI)
  -Write Status Register (WRSR)
  -Page Program (PP)
  -Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
  -Erase Security Registers (44h) / Program Security Registers (42h)
- Software Protection Mode: The Block Protect bits (BP4-BP0) define the section of the memory array that can be read but not changed.
- Hardware Protection Mode: WP# goes low to protect the Block Protect bits (BP4-BP0) and the SRP bits (SRP1 and SRP0).
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command and Software Reset (66h+99h).

**Table 3. GD25LQ64H Protected area size (CMP=0)**

| Status Register Content | | | | | Memory Content | | | |
|---|---|---|---|---|---|---|---|---|
| BP4 | BP3 | BP2 | BP1 | BP0 | Blocks | Addresses | Density | Portion |
| X | X | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 126 to 127 | 7E0000H-7FFFFFH | 128KB | Upper 1/64 |
| 0 | 0 | 0 | 1 | 0 | 124 to 127 | 7C0000H-7FFFFFH | 256KB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 1 | 120 to 127 | 780000H-7FFFFFH | 512KB | Upper 1/16 |
| 0 | 0 | 1 | 0 | 0 | 112 to 127 | 700000H-7FFFFFH | 1MB | Upper 1/8 |
| 0 | 0 | 1 | 0 | 1 | 96 to 127 | 600000H-7FFFFFH | 2MB | Upper 1/4 |
| 0 | 0 | 1 | 1 | 0 | 64 to 127 | 400000H-7FFFFFH | 4MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 to 1 | 000000H-01FFFFH | 128KB | Lower 1/64 |
| 0 | 1 | 0 | 1 | 0 | 0 to 3 | 000000H-03FFFFH | 256KB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 1 | 0 to 7 | 000000H-07FFFFH | 512KB | Lower 1/16 |
| 0 | 1 | 1 | 0 | 0 | 0 to 15 | 000000H-0FFFFFH | 1MB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 1 | 0 to 31 | 000000H-1FFFFFH | 2MB | Lower 1/4 |
| 0 | 1 | 1 | 1 | 0 | 0 to 63 | 000000H-3FFFFFH | 4MB | Lower 1/2 |
| X | X | 1 | 1 | 1 | 0 to 127 | 000000H-7FFFFFH | 8MB | ALL |
| 1 | 0 | 0 | 0 | 1 | 127 | 7FF000H-7FFFFFH | 4KB | Top Block |
| 1 | 0 | 0 | 1 | 0 | 127 | 7FE000H-7FFFFFH | 8KB | Top Block |
| 1 | 0 | 0 | 1 | 1 | 127 | 7FC000H-7FFFFFH | 16KB | Top Block |
| 1 | 0 | 1 | 0 | X | 127 | 7F8000H-7FFFFFH | 32KB | Top Block |
| 1 | 0 | 1 | 1 | 0 | 127 | 7F8000H-7FFFFFH | 32KB | Top Block |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000H-000FFFH | 4KB | Bottom Block |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000H-001FFFH | 8KB | Bottom Block |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 1 | 0 | 000000H-003FFFH | 16KB | Bottom Block |
| 1 | 1 | 1 | 0 | X | 0 | 000000H-007FFFH | 32KB | Bottom Block |
| 1 | 1 | 1 | 1 | 0 | 0 | 000000H-007FFFH | 32KB | Bottom Block |

**Table 4. GD25LQ64H Protected area size (CMP=1)**

| Status Register Content | | | | | Memory Content | | | |
|---|---|---|---|---|---|---|---|---|
| **BP4** | **BP3** | **BP2** | **BP1** | **BP0** | **Blocks** | **Addresses** | **Density** | **Portion** |
| X | X | 0 | 0 | 0 | ALL | 000000H-7FFFFFH | ALL | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 to 125 | 000000H-7DFFFFH | 8064KB | Lower 63/64 |
| 0 | 0 | 0 | 1 | 0 | 0 to 123 | 000000H-7BFFFFH | 7936KB | Lower 31/32 |
| 0 | 0 | 0 | 1 | 1 | 0 to 119 | 000000H-77FFFFH | 7680KB | Lower 15/16 |
| 0 | 0 | 1 | 0 | 0 | 0 to 111 | 000000H-6FFFFFH | 7MB | Lower 7/8 |
| 0 | 0 | 1 | 0 | 1 | 0 to 95 | 000000H-5FFFFFH | 6MB | Lower 3/4 |
| 0 | 0 | 1 | 1 | 0 | 0 to 63 | 000000H-3FFFFFH | 4MB | Lower 1/2 |
| 0 | 1 | 0 | 0 | 1 | 2 to 127 | 020000H-7FFFFFH | 8064KB | Upper 63/64 |
| 0 | 1 | 0 | 1 | 0 | 4 to 127 | 040000H-7FFFFFH | 7936KB | Upper 31/32 |
| 0 | 1 | 0 | 1 | 1 | 8 to 127 | 080000H-7FFFFFH | 7680KB | Upper 15/16 |
| 0 | 1 | 1 | 0 | 0 | 16 to 127 | 100000H-7FFFFFH | 7MB | Upper 7/8 |
| 0 | 1 | 1 | 0 | 1 | 32 to 127 | 200000H-7FFFFFH | 6MB | Upper 3/4 |
| 0 | 1 | 1 | 1 | 0 | 64 to 127 | 400000H-7FFFFFH | 4MB | Upper 1/2 |
| X | X | 1 | 1 | 1 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 0 to 127 | 000000H-7FEFFFH | 8188KB | L-2047/2048 |
| 1 | 0 | 0 | 1 | 0 | 0 to 127 | 000000H-7FDFFFH | 8184KB | L-1023/1024 |
| 1 | 0 | 0 | 1 | 1 | 0 to 127 | 000000H-7FBFFFH | 8176KB | L-511/512 |
| 1 | 0 | 1 | 0 | X | 0 to 127 | 000000H-7F7FFFH | 8160KB | L-255/256 |
| 1 | 0 | 1 | 1 | 0 | 0 to 127 | 000000H-7F7FFFH | 8160KB | L-255/256 |
| 1 | 1 | 0 | 0 | 1 | 0 to 127 | 001000H-7FFFFFH | 8188KB | U-2047/2048 |
| 1 | 1 | 0 | 1 | 0 | 0 to 127 | 002000H-7FFFFFH | 8184KB | U-1023/1024 |
| 1 | 1 | 0 | 1 | 1 | 0 to 127 | 004000H-7FFFFFH | 8176KB | U-511/512 |
| 1 | 1 | 1 | 0 | X | 0 to 127 | 008000H-7FFFFFH | 8160KB | U-255/256 |
| 1 | 1 | 1 | 1 | 0 | 0 to 127 | 008000H-7FFFFFH | 8160KB | U-255/256 |

# 6 STATUS REGISTER

**Table 5. Status Register-SR No.1**

| No. | Name | Description | Note |
|---|---|---|---|
| S7 | SRP0 | Status Register Protection Bit | Non-volatile writable |
| S6 | BP4 | Block Protect Bit | Non-volatile writable |
| S5 | BP3 | Block Protect Bit | Non-volatile writable |
| S4 | BP2 | Block Protect Bit | Non-volatile writable |
| S3 | BP1 | Block Protect Bit | Non-volatile writable |
| S2 | BP0 | Block Protect Bit | Non-volatile writable |
| S1 | WEL | Write Enable Latch | Volatile, read only |
| S0 | WIP | Erase/Write In Progress | Volatile, read only |

**Table 6. Status Register-SR No.2**

| No. | Name | Description | Note |
|---|---|---|---|
| S15 | SUS1 | Erase Suspend Bit | Volatile, read only |
| S14 | CMP | Complement Protect Bit | Non-volatile writable |
| S13 | LB3 | Security Register Lock Bit | Non-volatile writable (OTP) |
| S12 | LB2 | Security Register Lock Bit | Non-volatile writable (OTP) |
| S11 | LB1 | Security Register Lock Bit | Non-volatile writable (OTP) |
| S10 | SUS2 | Program Suspend Bit | Volatile, read only |
| S9 | QE | Quad Enable Bit | Non-volatile writable |
| S8 | SRP1 | Status Register Protection Bit | Non-volatile writable |

**Table 7. Status Register-SR No.3**

| No. | Name | Description | Note |
|---|---|---|---|
| S23 | HOLD/RST | HOLD# or RESET# Function | Non-volatile writable |
| S22 | DRV1 | Output Driver Strength Bit | Non-volatile writable |
| S21 | DRV0 | Output Driver Strength Bit | Non-volatile writable |
| S20 | DLP | Data Learning Pattern Enable bit | Non-volatile writable |
| S19 | EE | Erase Error Bit | Volatile, read only |
| S18 | PE | Program Error Bit | Volatile, read only |
| S17 | DC1 | Dummy Configuration Bit | Non-volatile writable |
| S16 | DC0 | Dummy Configuration Bit | Non-volatile writable |

The status and control bits of the Status Register are as follows:

**WIP bit**

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

**WEL bit**

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

**BP4, BP3, BP2, BP1, BP0 bits**

The Block Protect (BP4, BP3, BP2, BP1 and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1 and BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1 and BP0) bits are 1 and CMP=1.

**SRP1, SRP0 bits**

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

| SRP1 | SRP0 | #WP | Status Register | Description |
|---|---|---|---|---|
| 0 | 0 | X | Software Protected | The Status Register can be written to after a Write Enable command, WEL=1.(Default) |
| 0 | 1 | 0 | Hardware Protected | WP#=0, the Status Register locked and cannot be written to. |
| 0 | 1 | 1 | Hardware Unprotected | WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1. |
| 1 | X | X | Power Supply Lock-Down(1) | Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle, Hardware Reset, Software Reset (66h+99h), JEDEC RESET. |
| 1 | X | X | One Time Program(2) | Status Register is permanently protected and cannot be written to. **(Enabled by adding prefix command AAh, 55h)** |

Note:

1. When SRP1 =1, a Power-down, Power-up cycle, Hardware Reset, Software Reset (66h+99h), JEDEC RESET will change SRP1 =0 state.
2. Please contact GigaDevice for details regarding the special instruction sequence.

**QE bit**

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD#/RESET# pin are enabled. When the QE bit is set to 1, the IO2 pin is enabled for Quad SPI and DTR Quad SPI, the WP# pin is still available for Standard/Dual/DTR Dual SPI. When the QE pin is set to 1, the Quad IO3 pins is enable, the HOLD#/RESET# pin is not available. (It is best to set the QE bit to 0 to avoid short issues if the WP# or HOLD# pin is tied directly to the power supply or ground.)

**LB3, LB2, LB1 bits**

The LB3, LB2 and LB1 bits are non-volatile One Time Program (OTP) bits in Status Register (S13, S12 and S11) that provide the write protect control and status to the Security Registers. The default state of LB3, LB2 and LB1 bits are 0, the security registers are unlocked. The LB3, LB2 and LB1 bits can be set to 1 individually using the Write Register instruction. The LB3, LB2 and LB1 bits are One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

**CMP bit**

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction with the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

**SUS1, SUS2 bits**

The SUS1 and SUS2 bits are read only bits in the status register (S15 and S10) that are set to 1 after executing an Erase/Program Suspend (75h) command (The Erase Suspend will set the SUS1 bit to 1, and the Program Suspend will set the SUS2 bit to 1). The SUS1 and SUS2 bits are cleared to 0 by Erase/Program Resume (7Ah) command, Hardware Reset, Software reset (66h+99h) command, JEDEC RESET, as well as a power-down, power-up cycle.

**DC1, DC0 bits**

The Dummy Configuration (DC) bits are non-volatile, which select the number of dummy cycles between the end of address and the start of read data output. Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional dummy cycles as the SCLK frequency increases.

The following dummy cycle tables provide different dummy cycle settings that are configured.

| Command | DC1, DC0 | Numbers of Dummy Cycles | Freq.(MHz) |
|---|---|---|---|
| 0Bh, 3Bh, 6Bh | 00 (default) | 8 | 133 |
| | 01 | 8 | 133 |
| | 10 | 8 | 133 |
| | 11 | 8 | 133 |
| BBh | 00 (default) | 4 | 133 |
| | 01 | 4 | 133 |
| | 10 | 4 | 133 |
| | 11 | 4 | 133 |
| EBh | 00 (default) | 6 | 120 |
| | 01 | 6 | 120 |
| | 10 | 8 | 133 |
| | 11 | 10 | 133 |
| BDh<br>EDh | 00 (default) | 10 | 104 |
| | 01 | 8 | 80 |
| | 10 | 10 | 104 |
| | 11 | 10 | 104 |

**PE bit**

The Program Error (PE) bit is a read-only bit that indicates a program failure. It will also be set when the user attempts to program a protected array sector or access the locked OTP space. PE is cleared to "0" after program operation resumes or by Clear Flag Status Register command (30h).

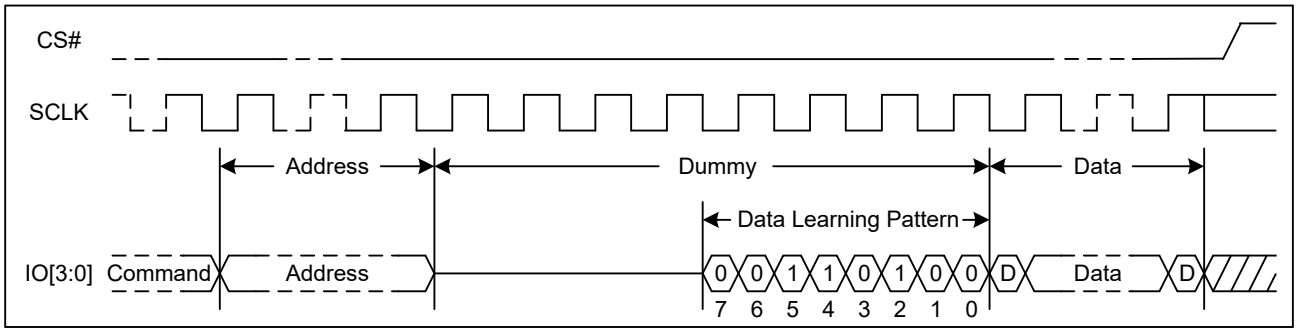
**EE bit**

The Erase Error (EE) bit is a read-only bit that indicates an erase failure. It will also be set when the user attempts to erase a protected array sector or access the locked OTP space. EE is cleared to "0" after erase operation resumes or by Clear Flag Status Register command (30h).

**DLP bit**

For “DTR Dual I/O Fast Read (BDh)”, “DTR Quad I/O Fast Read (EDh)”, and “DTR Burst Read with Wrap (0Eh)” commands, a pre-defined “Data Learning Pattern” can be used by the flash memory controller to determine the flash data output timing on 4 I/O pins. When DLP=1, during the last 4 dummy clocks just prior to the data output, the flash will output “00110100” Data Learning Pattern sequence on each of the 4 I/O pins. During this period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP=0 will disable the Data Learning Pattern output.

**Figure 6. Data Learning Pattern Sequence Diagram (DTR, Dummy Clock ≥ 8)**




Note: 8 dummy cycle example

**DRV1, DRV0 bits**

The DRV1 and DRV0 bits are used to determine the output driver strength for the Read operations.

**Table 8. Driver Strength for Read Operations**

| DRV1, DRV0 | Driver Strength |
|---|---|
| 00 | 25ohm (100%) |
| 01 | 35ohm (75% default) |
| 10 | 50ohm (50%) |
| 11 | 65ohm (25%) |

**HOLD/RST bit**

The HOLD/RST bit is used to determine whether HOLD# or RESET# function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0 (Default), the pin acts as HOLD#, When the HOLD/RST=1, the pin acts as RESET#. However, the HOLD# or RESET# function are only available when QE=0, If QE=1, The HOLD# and RESET# functions are disabled, the pin acts as dedicated data I/O pin.

# 7 COMMAND DESCRIPTIONS

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, with most significant bit first on SI, and each bit is latched on the rising edges of SCLK.

Every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then CS# must be driven high to return to deselected status.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

**Table 9. Commands (Standard/Dual/Quad SPI, QPI)**

| Command Name | Code | SPI | | QPI | | Addr. Bytes | Data Bytes |
|---|---|---|---|---|---|---|---|
| | | Command-Addr.-Data | Dummy Clock Cycles | Command-Addr.-Data | Dummy Clock Cycles | | |
| Write Enable | 06h | 1-0-0 | 0 | 4-0-0 | 0 | 0 | 0 |
| Write Disable | 04h | 1-0-0 | 0 | 4-0-0 | 0 | 0 | 0 |
| Read Status Register-1 | 05h | 1-0-(1) | 0 | 4-0-(4) | 0 | 0 | 1 |
| Read Status Register-2 | 35h | 1-0-(1) | 0 | 4-0-(4) | 0 | 0 | 1 |
| Read Status Register-3 | 15h | 1-0-(1) | 0 | 4-0-(4) | 0 | 0 | 1 |
| Write Status Register-1&2 | 01h | 1-0-1 | 0 | 4-0-4 | 0 | 0 | 1~2 |
| Write Status Register-2 | 31h | 1-0-1 | 0 | 4-0-4 | 0 | 0 | 1 |
| Write Status Register-3 | 11h | 1-0-1 | 0 | 4-0-4 | 0 | 0 | 1 |
| Volatile SR write Enable | 50h | 1-0-0 | 0 | 4-0-0 | 0 | 0 | 0 |
| Clear SR Flags | 30h | 1-0-0 | 0 | 4-0-0 | 0 | 0 | 0 |
| Read Data | 03h | 1-1-(1) | 0 | - | - | 3 | 1 to ∞ |
| Fast Read | 0Bh | 1-1-(1) | 8 | 4-4-(4) | 4(1) | 3 | 1 to ∞ |
| Dual Output Fast Read | 3Bh | 1-1-(2) | 8 | - | - | 3 | 1 to ∞ |
| Dual I/O Fast Read | BBh | 1-2-(2) | 4(2) | - | - | 3 | 1 to ∞ |
| DTR Dual I/O Fast Read | BDh | 1-2d-(2d) | 10(2)(3) | - | - | 3 | 1 to ∞ |
| Quad Output Fast Read | 6Bh | 1-1-(4) | 8 | - | - | 3 | 1 to ∞ |
| Quad I/O Fast Read | EBh | 1-4-(4) | 6(2)(3) | 4-4-(4) | 4(1) | 3 | 1 to ∞ |
| DTR Quad I/O Fast Read | EDh | 1-4d-(4d) | 10(2)(3) | 4-4d-(4d) | 10(1) | 3 | 1 to ∞ |
| Burst Read with Wrap | 0Ch | - | - | 4-4-(4) | 4(1) | 3 | 1 to ∞ |
| DTR Burst Read with Wrap | 0Eh | - | - | 4-4d-(4d) | 10(1) | 3 | 1 to ∞ |
| Set Burst with Wrap | 77h | 1-0-4 | 6 | - | - | 0 | 1 |
| Set Read Parameters | C0h | - | - | 4-0-(4) | 0 | 0 | 1 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Page Program | 02h | 1-1-1 | 0 | 4-4-4 | 0 | 3 | 1 to ∞ |
| Quad Page Program | 32h | 1-1-4 | 0 | - | - | 3 | 1 to ∞ |
| Sector Erase | 20h | 1-1-0 | 0 | 4-4-0 | 0 | 3 | 0 |
| Block Erase (32K) | 52h | 1-1-0 | 0 | 4-4-0 | 0 | 3 | 0 |
| Block Erase (64K) | D8h | 1-1-0 | 0 | 4-4-0 | 0 | 3 | 0 |
| Chip Erase | C7/60h | 1-0-0 | 0 | 4-0-0 | 0 | 0 | 0 |
| Read Manufacturer/ Device ID | 90h | 1-1-(1) | 0 | 4-4-(4) | 0 | 3 | 2 |
| Read Identification | 9Fh | 1-0-(1) | 0 | 4-0-(4) | 0 | 0 | 3 |
| Read Unique ID | 4Bh | 1-1-(1) | 8 | - | - | 3 | 1 to ∞ |
| Erase Security Registers | 44h | 1-1-0 | 0 | - | - | 3 | 0 |
| Program Security Registers | 42h | 1-1-1 | 0 | - | - | 3 | 1 to ∞ |
| Read Security Registers | 48h | 1-1-(1) | 8 | - | - | 3 | 1 to ∞ |
| Enable Reset | 66h | 1-0-0 | 0 | 4-0-0 | 0 | 0 | 0 |
| Reset | 99h | 1-0-0 | 0 | 4-0-0 | 0 | 0 | 0 |
| Program/Erase Suspend | 75h | 1-0-0 | 0 | 4-0-0 | 0 | 0 | 0 |
| Program/Erase Resume | 7Ah | 1-0-0 | 0 | 4-0-0 | 0 | 0 | 0 |
| Deep Power-Down | B9h | 1-0-0 | 0 | 4-0-0 | 0 | 0 | 0 |
| Release From Deep Power-Down | ABh | 1-0-0 | 0 | 4-0-0 | 0 | 0 | 0 |
| Release From Deep Power-Down and Read Device ID | ABh | 1-0-(1) | 24 | 4-0-(4) | 6 | 0 | 1 |
| Enable QPI | 38h | 1-0-0 | 0 | - | - | 0 | 0 |
| Disable QPI | FFh | - | - | 4-0-0 | 0 | 0 | 0 |
| Read Serial Flash Discoverable Parameter | 5Ah | 1-1-(1) | 8 | - | - | 3 | 1 to ∞ |

Note:

1. The dummy cycle number in the table is default value, and can be set by the "Set Read Parameters (C0h)" Command.
2. The dummy cycle includes the Mode bits. Please refer to the command sequence diagram for details.
3. The dummy cycle number in the table is default value, and can be set by the DC bits in Status Register-3.

## TABLE OF ID DEFINITIONS

### GD25LQ64H

| Operation Code | MID7-MID0 | ID15-ID8 | ID7-ID0 |
|---|---|---|---|
| 9Fh | C8 | 60 | 17 |
| 90h | C8 | | 16 |
| ABh | | | 16 |

## 7.1 Write Enable (WREN) (06h)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR) and Erase/Program Security Registers command.

The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

**Figure 7. Write Enable Sequence Diagram (SPI)**

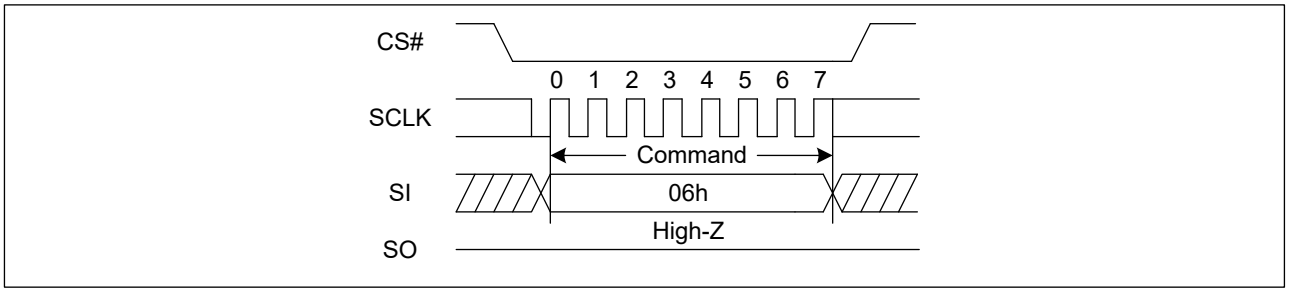
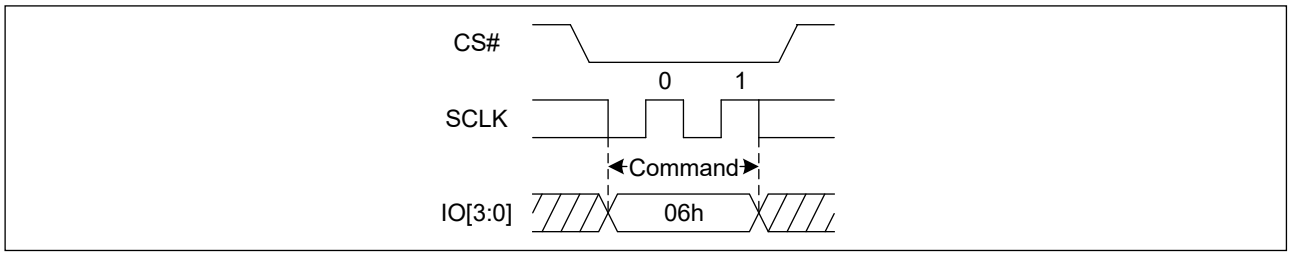



**Figure 8. Write Enable Sequence Diagram (QPI)**




## 7.2 Write Disable (WRDI) (04h)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit may be set to 0 by issuing the Write Disable (WRDI) command to disable Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), that require WEL be set to 1 for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit =1.

The WEL bit is reset by following condition: Write Disable command (WRDI), Power-up, and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Sector Erase, Block Erase and Chip Erase commands.

The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high.

**Figure 9. Write Disable Sequence Diagram (SPI)**

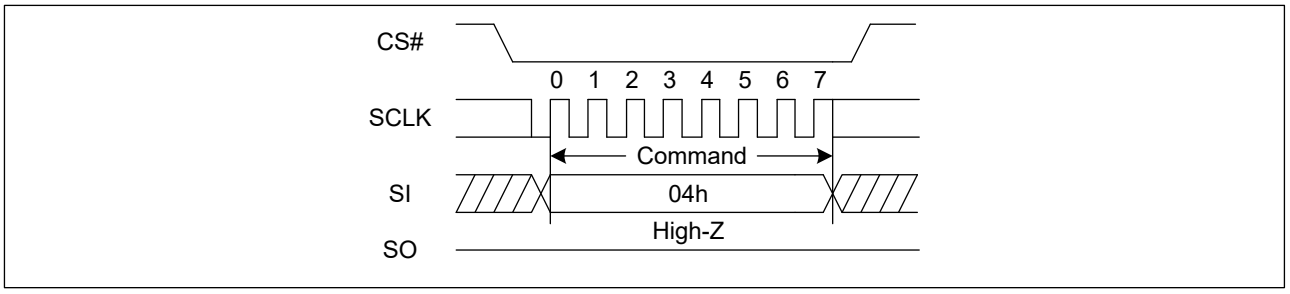
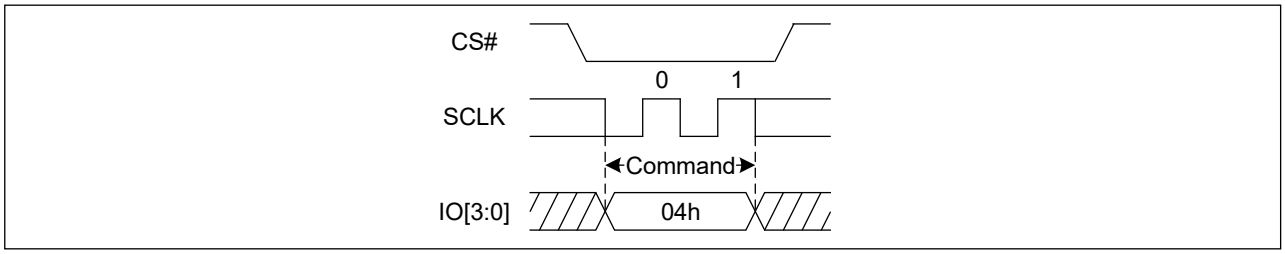


**Figure 10. Write Disable Sequence Diagram (QPI)**




## 7.3 Read Status Register (RDSR) (05h/35h/15h)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code of "05h" / "35h" / "15h", the SO will output Status Register bits S7~S0 / S15-S8 / S23-S16.

**Figure 11. Read Status Register Sequence Diagram (SPI)**

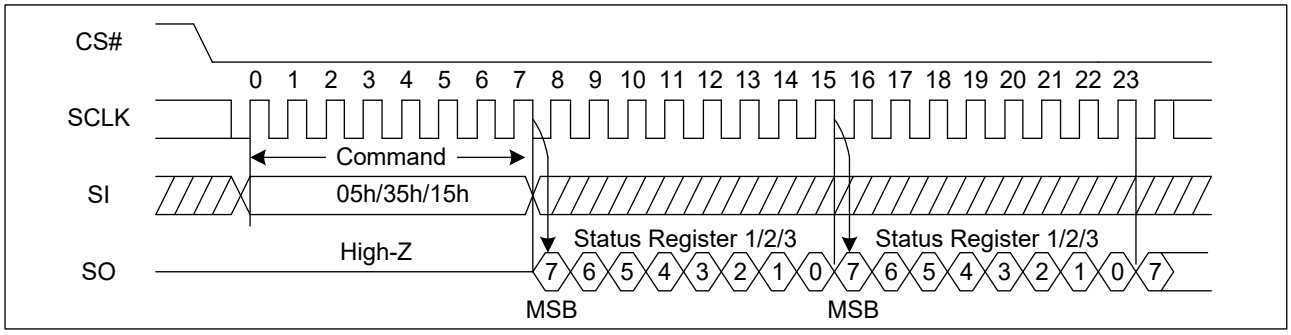
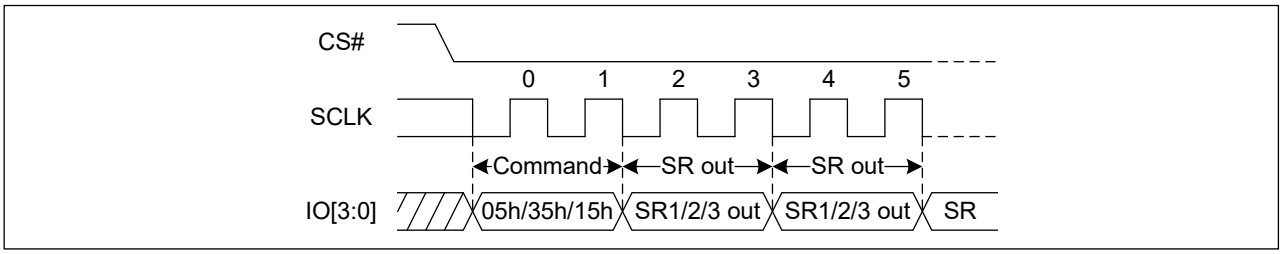



**Figure 12. Read Status Register Sequence Diagram (QPI)**




## 7.4 Write Status Register (WRSR) (01h/31h/11h)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S15, S10, S1 and S0 of the Status Register. For Command code of "01h", the Status Register-1&2 (S15~S0) would be written. CS# must be driven high after the eighth or sixteenth bit of the data byte has been latched in. Otherwise, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the Write Status Register-1&2(01h) instruction will only program the Status Register-1, the QE and CMP bits in Status Register-2 will be cleared to 0 in SPI mode, while only the CMP bit will be cleared to 0 in QPI mode. For Command code of "31h/11h", the Status Register bits S15~S8 / S23~S16 would be written. CS# must be driven high after the eighth bit of the data byte has been latched in. Otherwise, the Write Status Register (WRSR)

command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is $t_W$) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1 and BP0) bits, to define the size of the area that is to be treated as read-only.

The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

**Figure 13. Write Status Register-1&2 Sequence Diagram (SPI)**

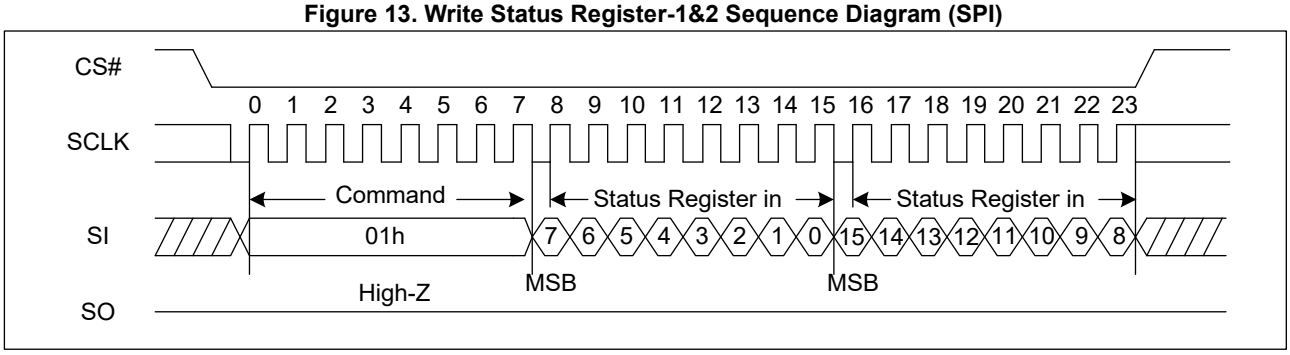



**Figure 14. Write Status Register-1&2 Sequence Diagram (QPI)**

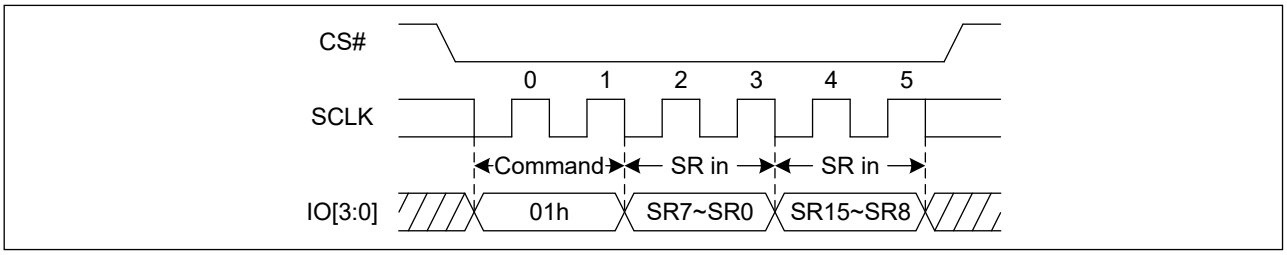



**Figure 15. Write Status Register Sequence Diagram (SPI)**

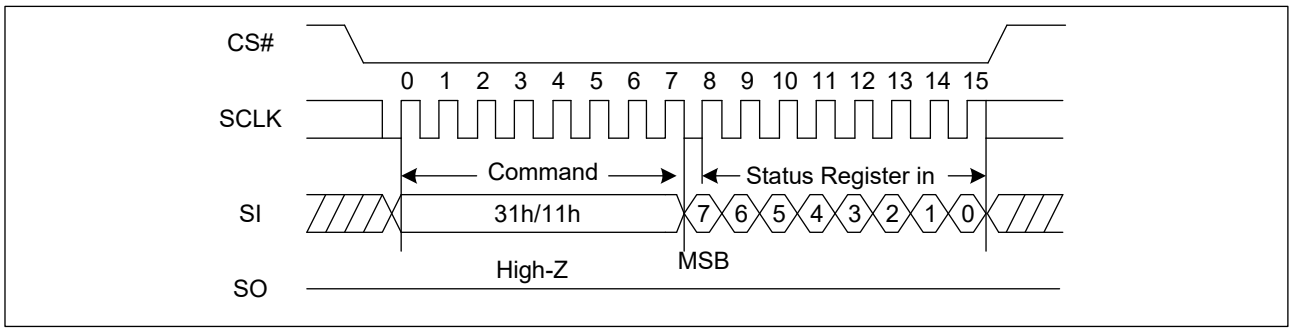
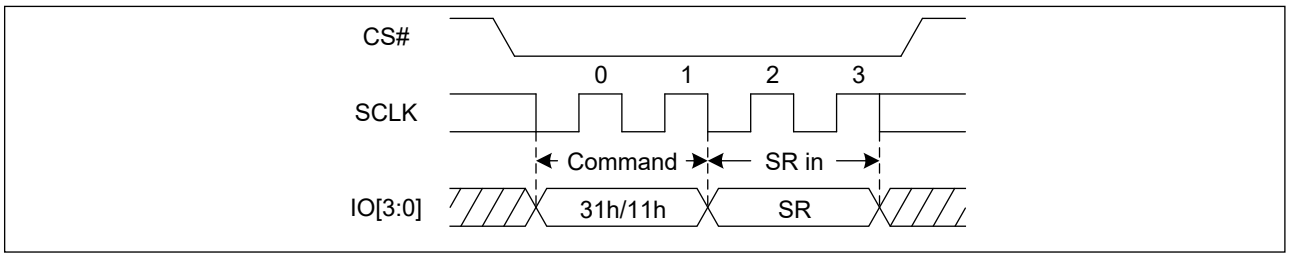


**Figure 16. Write Status Register Sequence Diagram (QPI)**




## 7.5 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

**Figure 17. Write Enable for Volatile Status Register Sequence Diagram (SPI)**

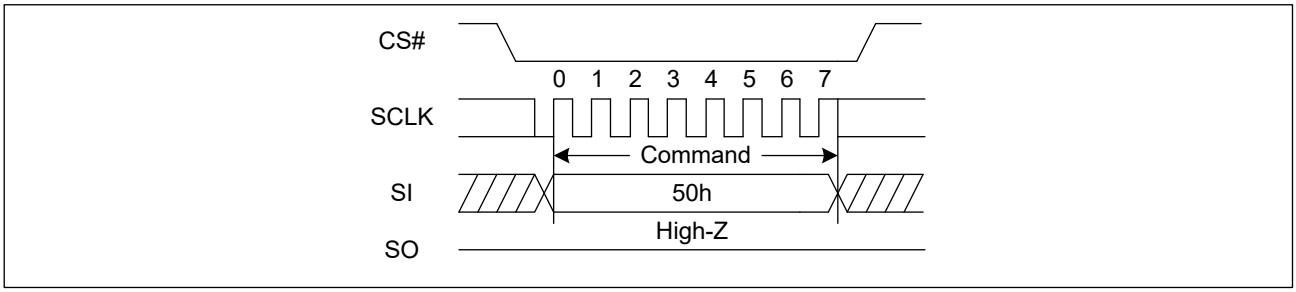
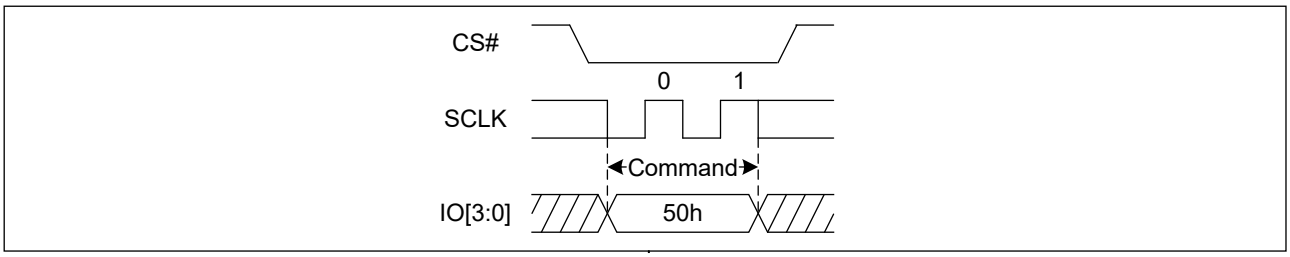



**Figure 18. Write Enable for Volatile Status Register Sequence Diagram (QPI)**




## 7.6 Clear SR Flags (30h)

The Clear Status Register Flags command resets bit S19 (Erase Error Bit) and S18 (Program Error Bit) in status register. It is not necessary to set the WEL bit before the Clear Status Register command is executed. The Clear SR command will not be accepted when the device remains busy with WIP set to 1. The WEL bit will be unchanged after this command is executed.

**Figure 19. Clear Status Register Flags Sequence Diagram**

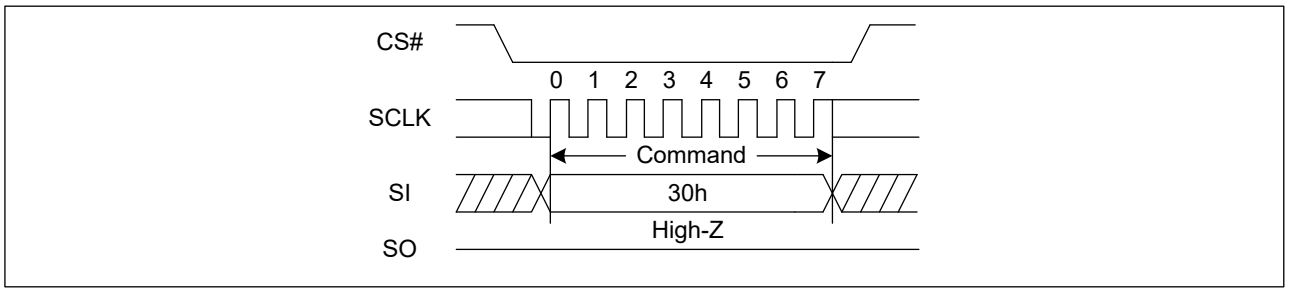
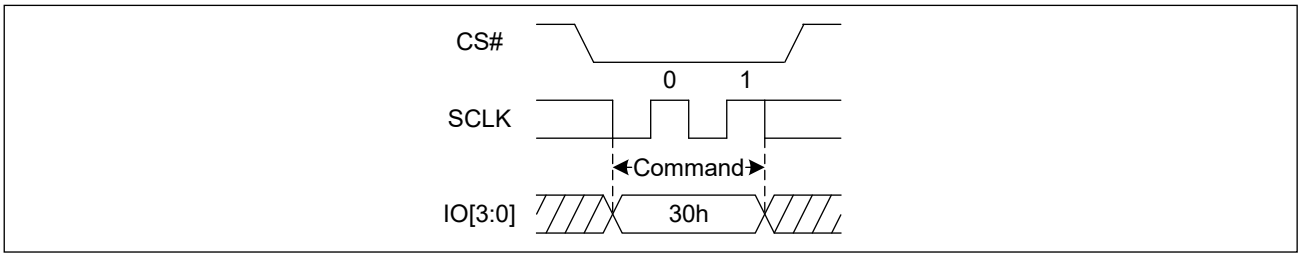


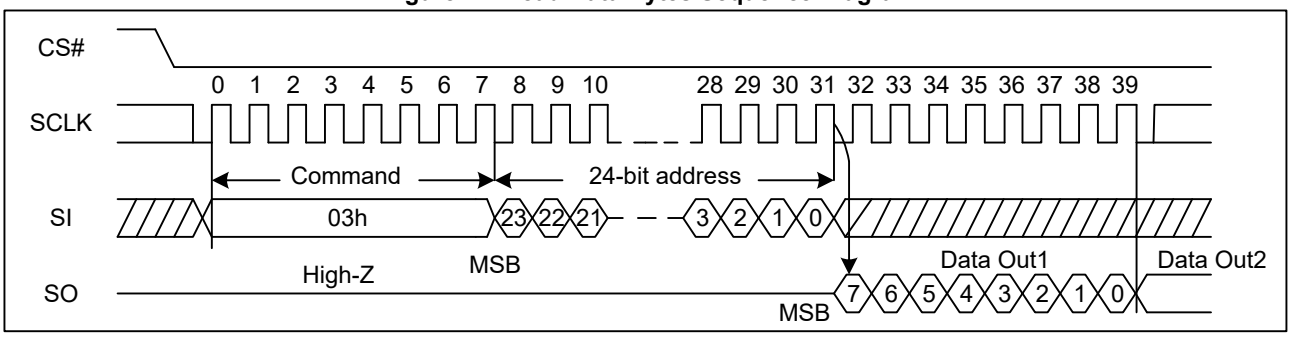

**Figure 20. Clear Status Register Flags Sequence Diagram (QPI)**




## 7.7 Read Data Bytes (READ) (03h)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency $f_R$, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 21. Read Data Bytes Sequence Diagram**




## 7.8 Read Data Bytes at Higher Speed (Fast Read) (0Bh)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency $f_C$, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

The Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" command to accommodate a wide range application with different needs for either maximum

Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P5,P4 setting, the number of dummy clocks can be configured.

**Figure 22. Read Data Bytes at Higher Speed Sequence Diagram (SPI)**

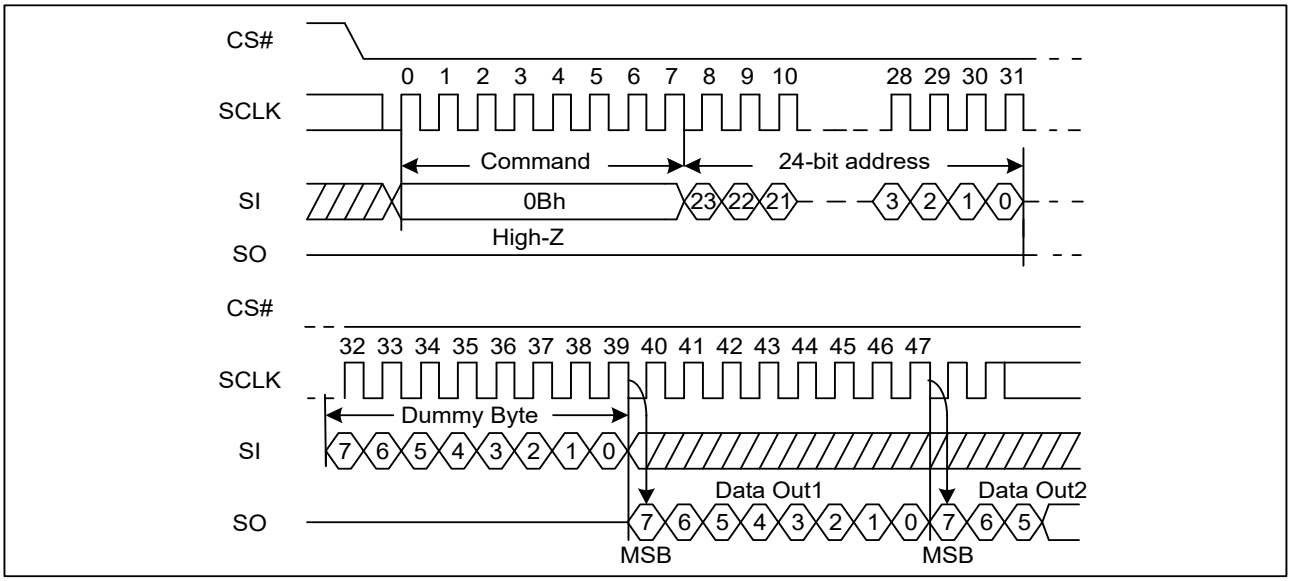
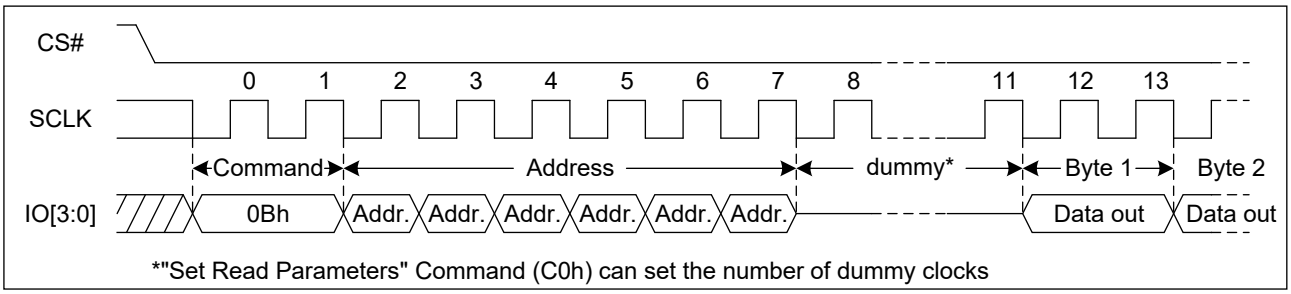



**Figure 23. Read Data Bytes at Higher Speed Sequence Diagram (QPI)**

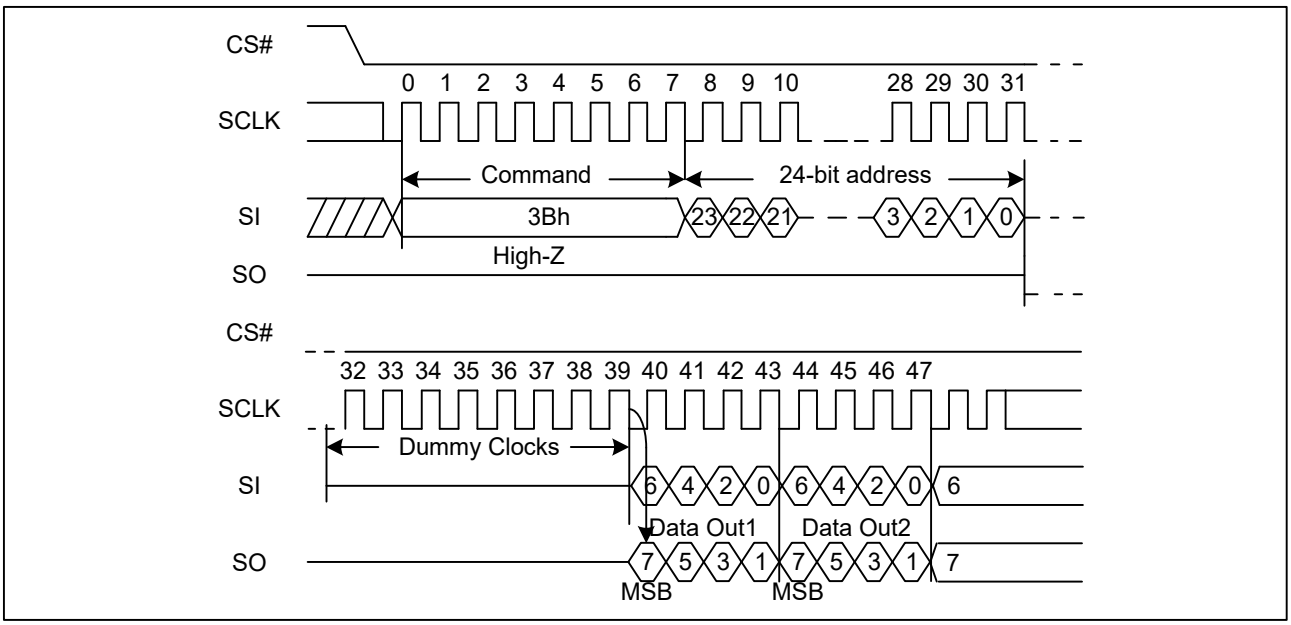



## 7.9 Dual Output Fast Read (3Bh)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

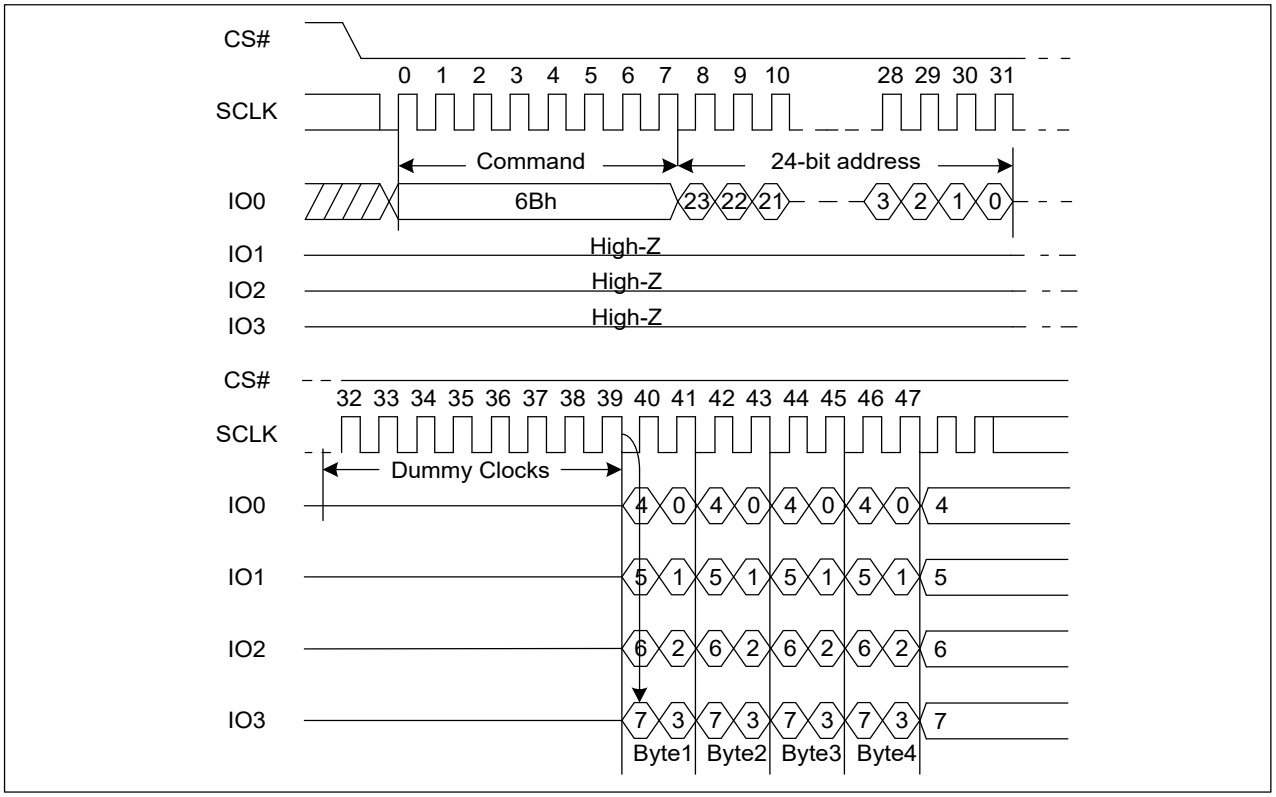
**Figure 24. Dual Output Fast Read Sequence Diagram**




## 7.10 Quad Output Fast Read (6Bh)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad Output Fast Read command.

**Figure 25. Quad Output Fast Read Sequence Diagram**



## 7.11 Dual I/O Fast Read (BBh)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-A0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

### Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBh command code. If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be also used to reset (M7-0) before issuing normal command.

**Figure 26. Dual I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0))**

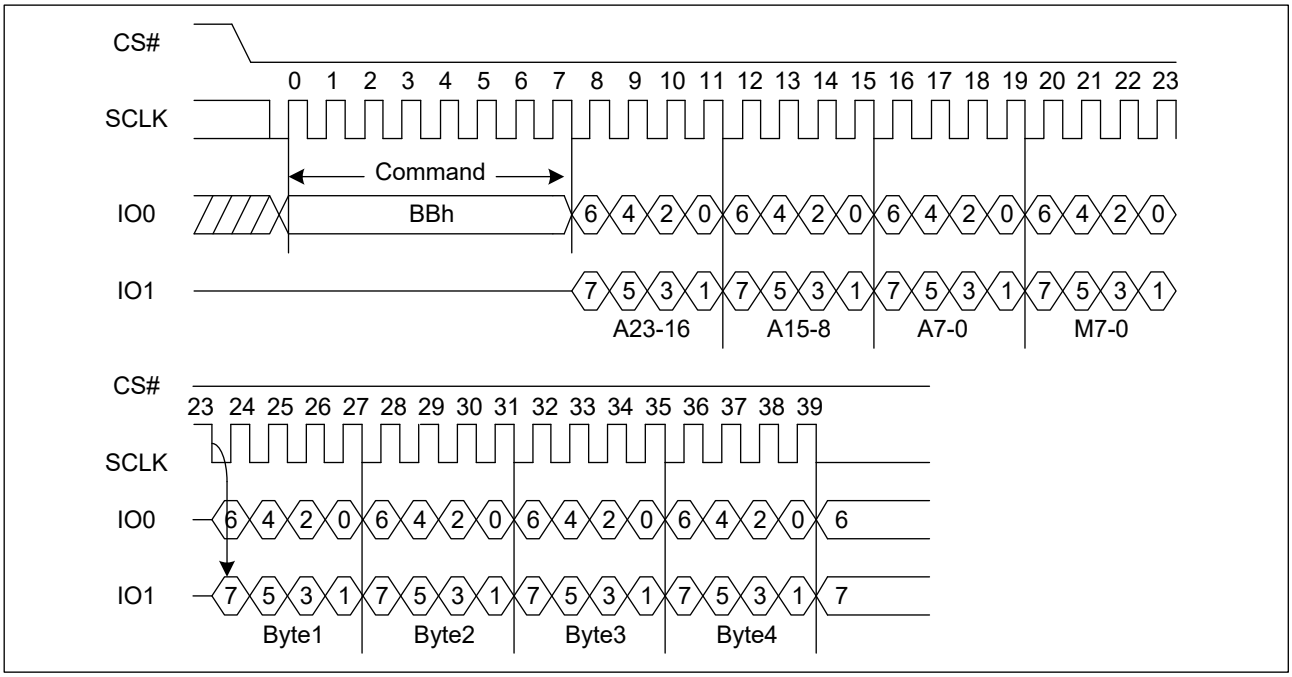
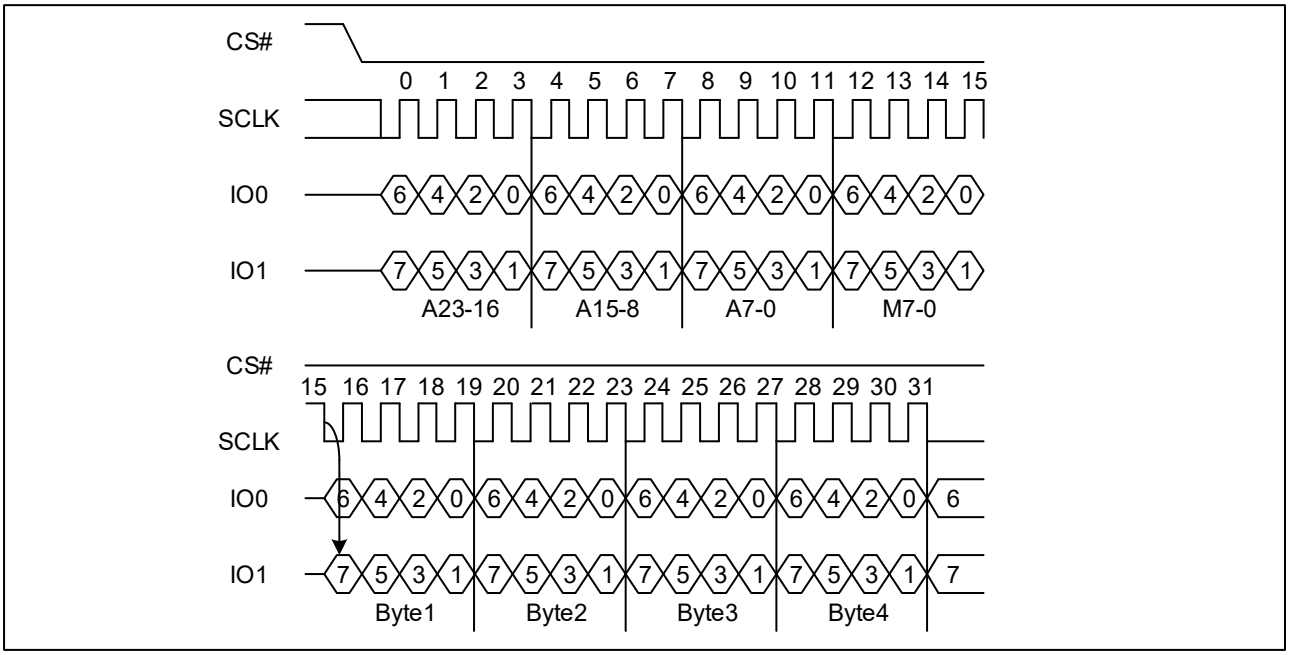


Figure 27. Dual I/O Fast Read Sequence Diagram ((M5-4) = (1, 0))




## 7.12 Quad I/O Fast Read (EBh)

The Quad I/O Fast Read command is similar to the Quad Output Fast Read command but with the capability to input the 3-byte address (A23-A0) and a “Continuous Read Mode” byte and 4-dummy clock (4-bit per clock) by IO0, IO1, IO2, IO3, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

The Quad I/O Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P5~P4 setting, the number of dummy clocks can be configured. To reach the maximum frequency, the device must be set in QPI mode with most dummy clocks. In QPI mode, the “Continuous Read Mode” bits M7-M0 are also considered as dummy clocks. “Continuous Read Mode” feature is also available in QPI mode for Quad I/O Fast Read command. “Wrap Around” feature is not available in QPI mode for Quad I/O Fast Read command. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) command must be used.

### Quad I/O Fast Read with “Continuous Read Mode”

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBh command code. If the “Continuous Read Mode” bits (M5-4) do not equal to (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be also used to reset (M7-0) before issuing normal command.

**Figure 28. Quad I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0), SPI)**

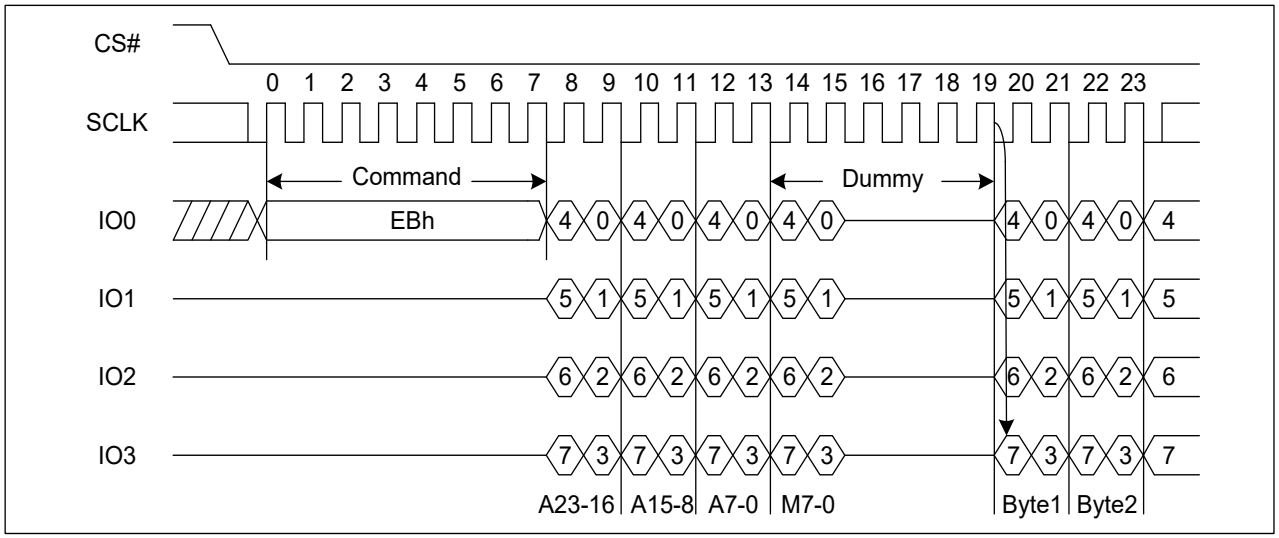



**Figure 29. Quad I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0), QPI)**

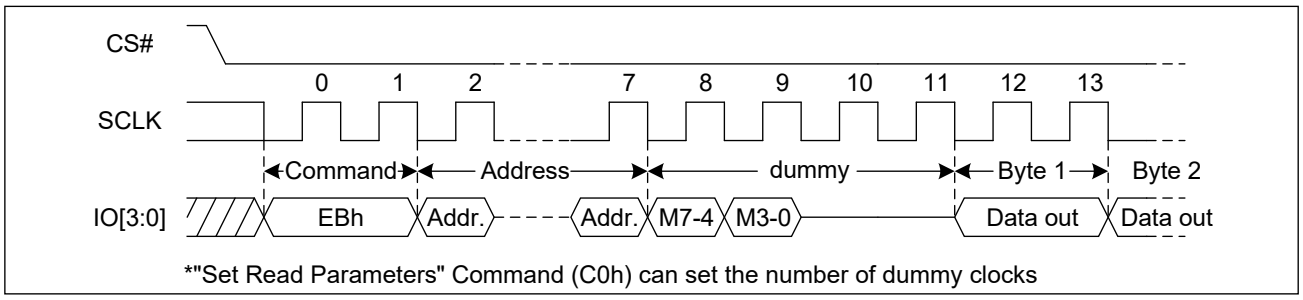
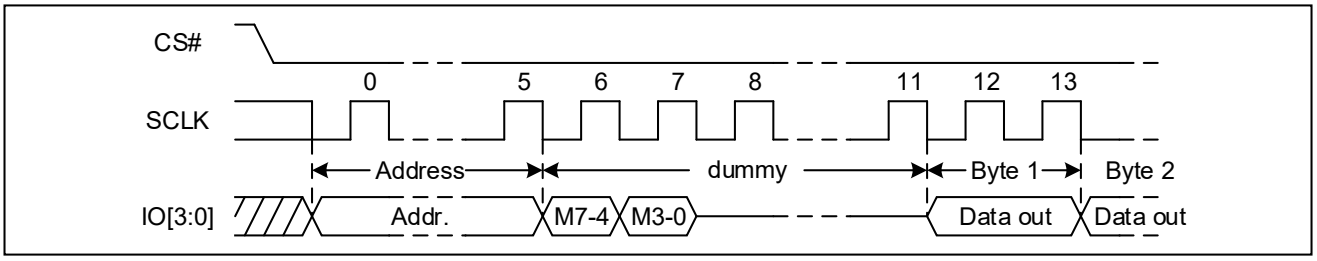



**Figure 30. Quad I/O Fast Read Sequence Diagram ((M5-4) = (1, 0))**




Note: Dummy is set by DC1/DC0 in SPI mode, dummy is set by "Set Read Parameters" command (C0h) in QPI mode.

## Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77h) commands prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap"

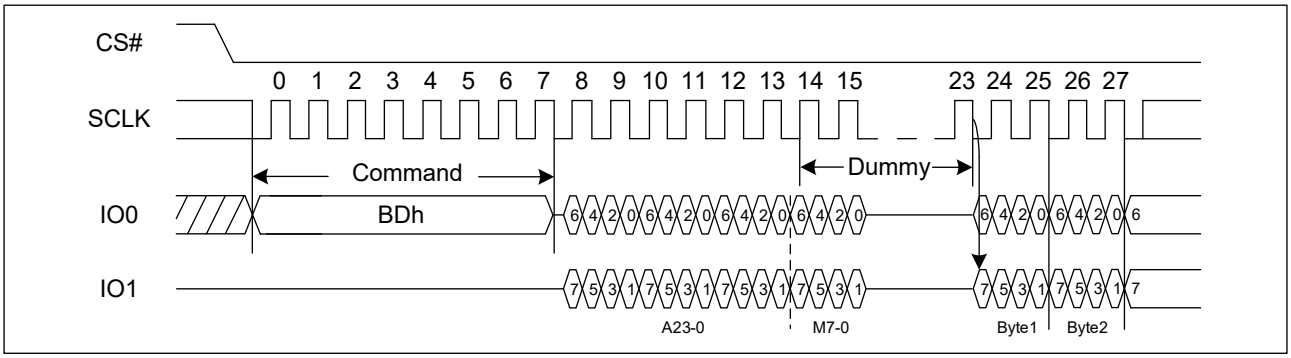
command allows three “Wrap Bits” W6-W4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-W5 is used to specify the length of the wrap around section within a page.

## 7.13 DTR Dual I/O Fast Read (BDh)

The DTR Dual I/O Fast Read instruction enables Double Transfer Rate throughput on dual I/O of Serial Flash in read mode. The address (interleave on 2 I/O pins, IO0 and IO1) is latched on both rising and falling edge of SCLK, and data (interleave on 2 I/O pins, IO0 and IO1) shift out on both rising and falling edge of SCLK. The 4-bit address can be latched-in at one clock, and 4-bit data can be read out at one clock, which means two bits at rising edge of clock, the other two bits at falling edge of clock. The first address Byte can be at any location. The address is automatically increased to the next higher address after each Byte data is shifted out, so the whole memory can be read out at a single DTR Dual I/O Fast Read command. The address counter rolls over to 0 when the highest address has been reached.

While Program/Erase/Write Status Register cycle is in progress, DTR Dual I/O Fast Read command is rejected without any impact on the Program/Erase/Write Status Register current cycle.

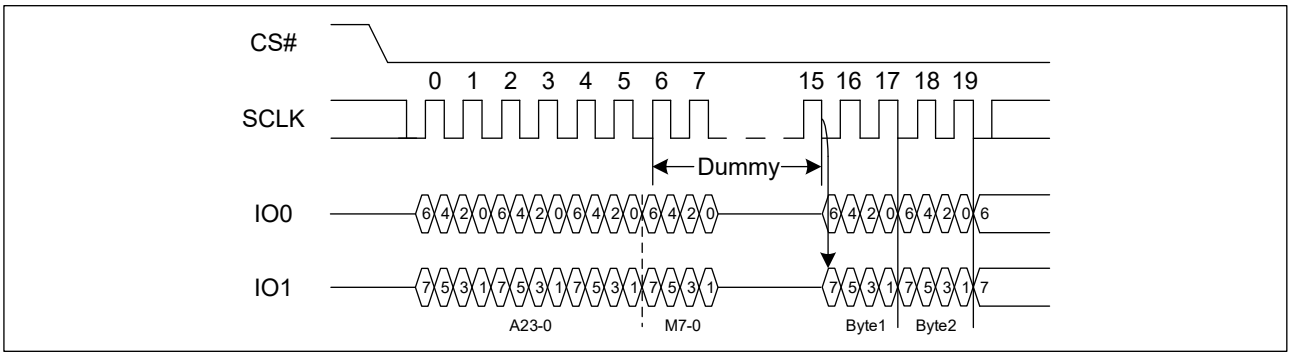
**Figure 31. DTR Dual I/O Fast Read Sequence Diagram (M5-4 ≠ (1, 0))**




### DTR Dual I/O Fast Read with “Continuous Read Mode”

The DTR Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-4) after the input 3-Byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next DTR Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BDh command code. If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be also used to reset (M7-0) before issuing normal command.

**Figure 32. DTR Dual I/O Fast Read Sequence Diagram (M5-4 = (1, 0))**




## 7.14 DTR Quad I/O Fast Read (EDh)

The DTR Quad I/O Fast Read instruction enables Double Transfer Rate throughput on quad I/O of Serial Flash in read

mode. A Quad Enable (QE) bit of status Register must be set to 1 before sending the DTR Quad I/O Fast Read instruction. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DTR Quad I/O Fast Read command. The address counter rolls over to 0 when the highest address has been reached. Once writing DTR Quad I/O Fast Read command, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

While Program/Erase/Write Status Register cycle is in progress, DTR Quad I/O Fast Read command is rejected without any impact on the Program/Erase/Write Status Register current cycle.

### DTR Quad I/O Fast Read with "Continuous Read Mode"

The DTR Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input address. If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next DTR Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EDh command code. If the "Continuous Read Mode" bits (M5-4) do not equal to (1, 0), the next command requires the first EDh command code, thus returning to normal operation. The only way to quit the DTR Quad I/O Continuous Read Mode" is to set the "Continuous Read Mode" bits (M5-4) not equal to (1, 0).

**Figure 33. DTR Quad I/O Fast Read Sequence Diagram (SPI, M5-4≠ (1, 0))**

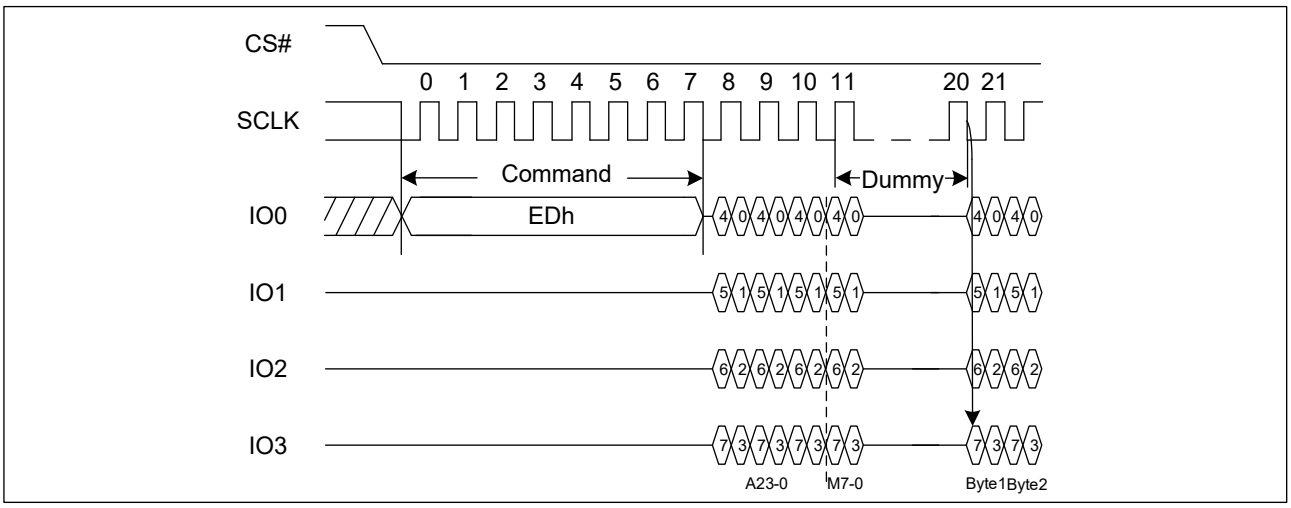



**Figure 34. DTR Quad I/O Fast Read Sequence Diagram (QPI, M5-4≠ (1, 0))**

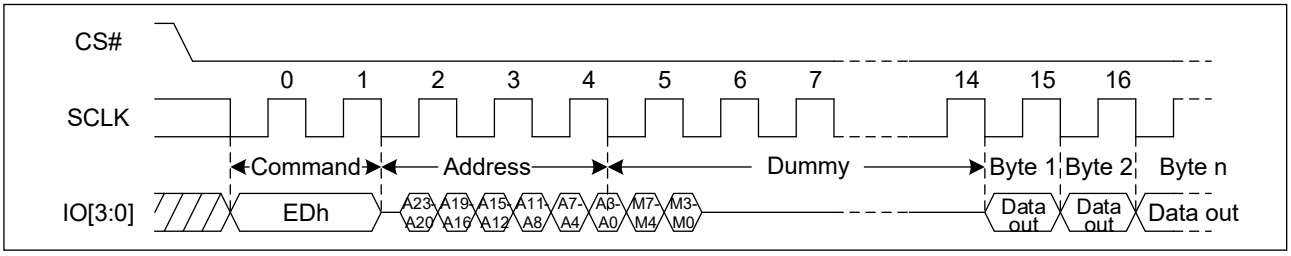
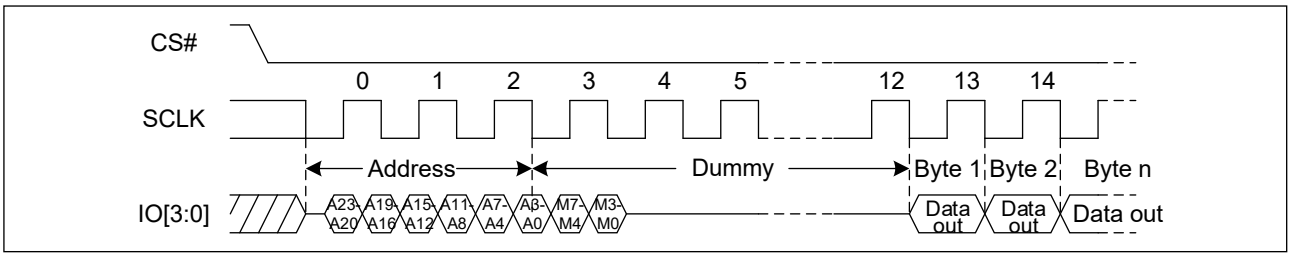


**Figure 35. DTR Quad I/O Fast Read Sequence Diagram (M5-4 = (1, 0))**




### DTR Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

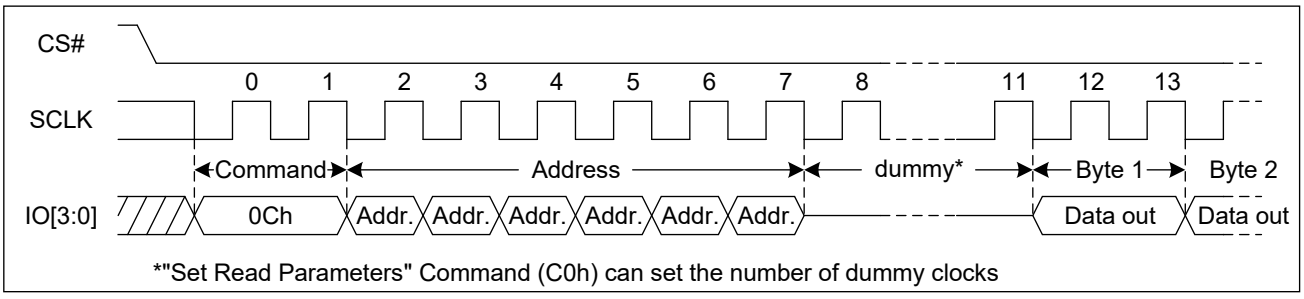
The DTR Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77h) commands prior to EDh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EDh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

## 7.15 Burst Read with Wrap (0Ch)

The "Burst Read with Wrap (0Ch)" command provides an alternative way to perform the read operation with "Wrap Around" in QPI mode. This command is similar to the "Fast Read (0Bh)" command in QPI mode, except the addressing of the read operation will "Wrap Around" to the beginning boundary of the "Wrap Around" once the ending boundary is reached. The "Wrap Length" and the number of dummy clocks can be configured by the "Set Read Parameters (C0h)" command.

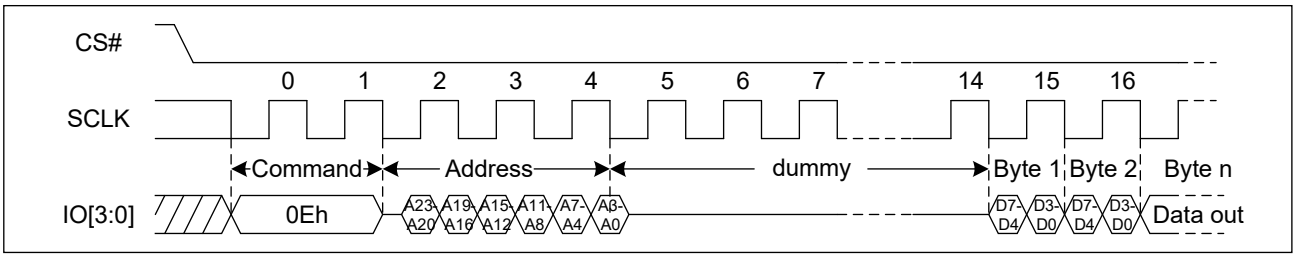
**Figure 36. Burst Read with Wrap Sequence Diagram**




## 7.16 DTR Burst Read with Wrap (0Eh)

The "DTR Burst Read with Wrap (0Eh)" instruction provides an alternative way to perform the read operation with "Wrap Around" in QPI mode. The instruction is similar to the "Fast Read (0Bh)" instruction in QPI mode, except the addressing of the read operation will "Wrap Around" to the beginning boundary of the "Wrap Around" once the ending boundary is reached. The "Wrap Length" can be configured by the "Set Read Parameters (C0h)" command.

**Figure 37. DTR Burst Read with Wrap Sequence Diagram**




## 7.17 Set Burst with Wrap (77h)

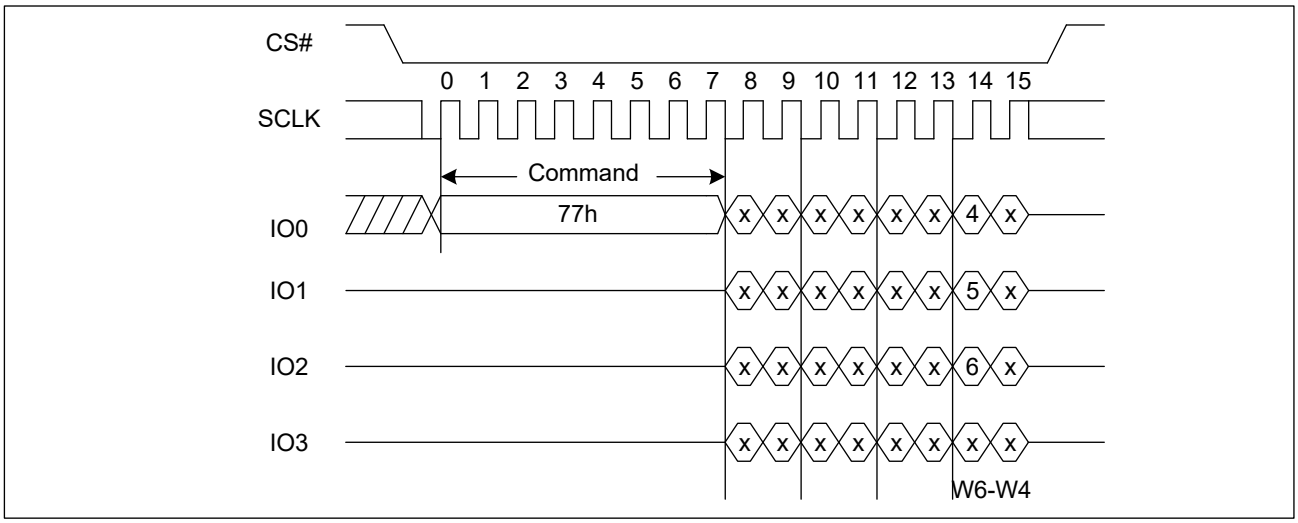
The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read" and "DTR Quad I/O Fast Read" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits "Wrap bits" → CS# goes high.

| W6,W5 | W4=0 | | W4=1 (default) | |
|---|---|---|---|---|
| | Wrap Around | Wrap Length | Wrap Around | Wrap Length |
| 0, 0 | Yes | 8-byte | No | N/A |
| 0, 1 | Yes | 16-byte | No | N/A |
| 1, 0 | Yes | 32-byte | No | N/A |
| 1, 1 | Yes | 64-byte | No | N/A |

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read" and "DTR Quad I/O Fast Read" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

**Figure 38. Set Burst with Wrap Sequence Diagram**




## 7.18 Set Read Parameters (C0h)

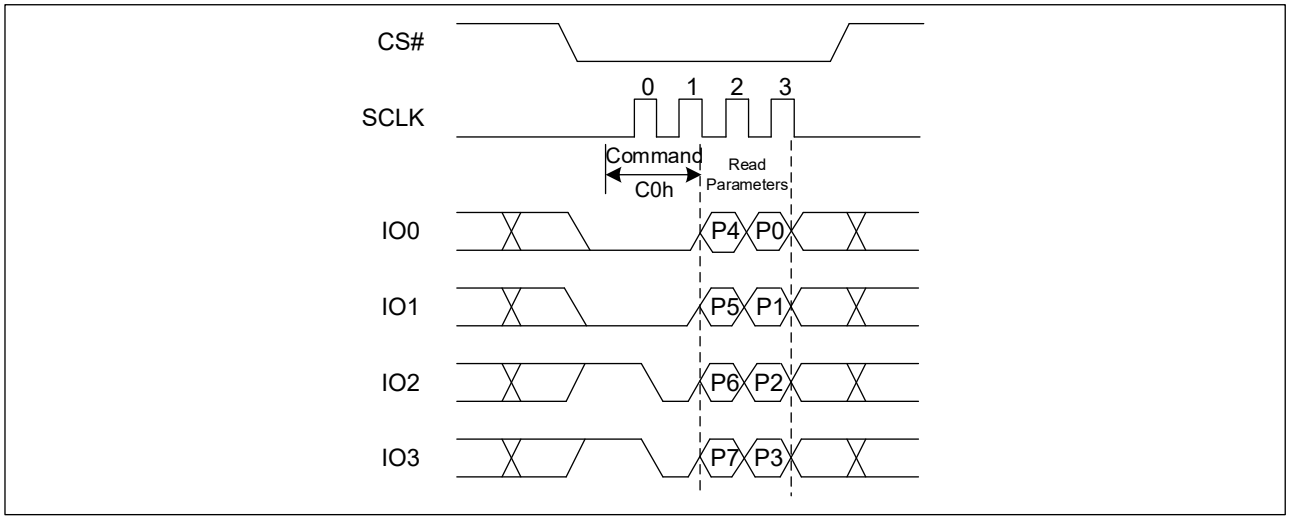
In QPI mode the "Set Read Parameters (C0h)" command can be used to configure the number of dummy clocks for "Fast Read (0Bh)", "Quad I/O Fast Read (EBh)", "DTR Quad I/O Fast Read (EDh)", "Burst Read with Wrap (0Ch)" and "DTR Burst Read with Wrap (0Eh)" command, and to configure the number of bytes of "Wrap Length" for the "Burst Read with Wrap (0Ch)" and "DTR Burst Read with Wrap (0Eh)" command. The "Wrap Length" is set by W5-6 bit in the "Set Burst with Wrap

(77h)" command. This wrap setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

| P5-P4 | STR FAST READ | | DTR FAST READ | | P1-P0 | Wrap Length |
|---|---|---|---|---|---|---|
| | Dummy Clocks | Maximum Read Freq. | Dummy Clocks | Maximum Read Freq. | | |
| 0 0 (default) | 4 | 80MHz | 10 | 104MHz | 0 0 (default) | 8-Byte |
| 0 1 | 4 | 80MHz | 10 | 104MHz | 0 1 | 16-Byte |
| 1 0 | 6 | 104MHz | 10 | 104MHz | 1 0 | 32-Byte |
| 1 1 | 8 | 133MHz | 10 | 104MHz | 1 1 | 64-Byte |

Note: Default from power up or reset

**Figure 39. Set Read Parameters command Sequence Diagram**




## 7.19 Page Program (PP) (02h)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is $t_{PP}$) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1 and BP0) is not executed and WEL will clear to "0".

**Figure 40. Page Program Sequence Diagram (SPI)**

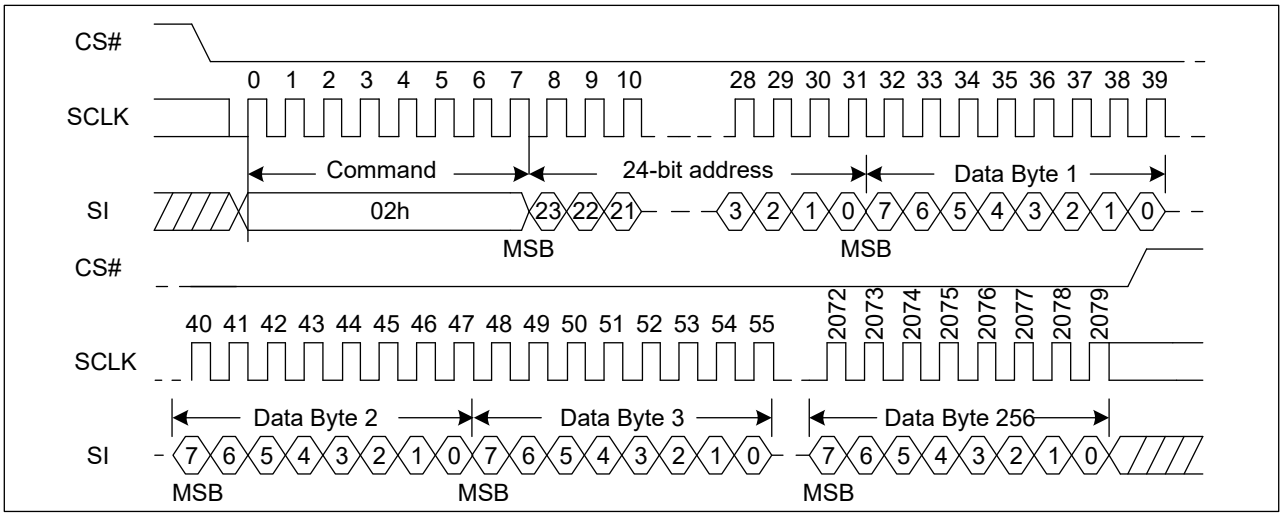
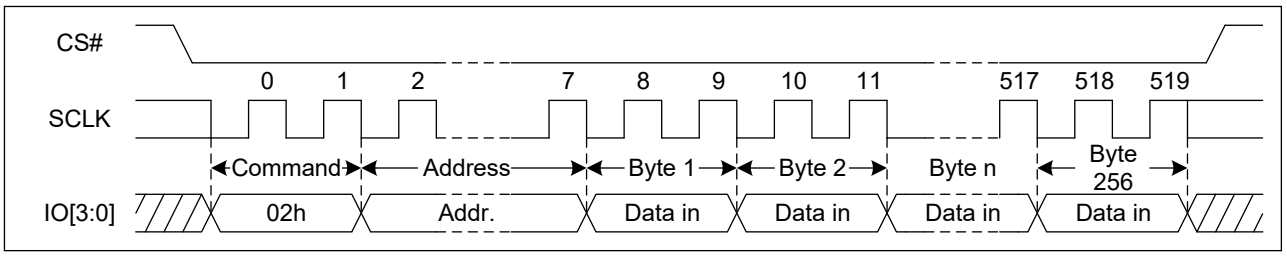



**Figure 41. Page Program Sequence Diagram (QPI)**




## 7.20 Quad Page Program (32h)

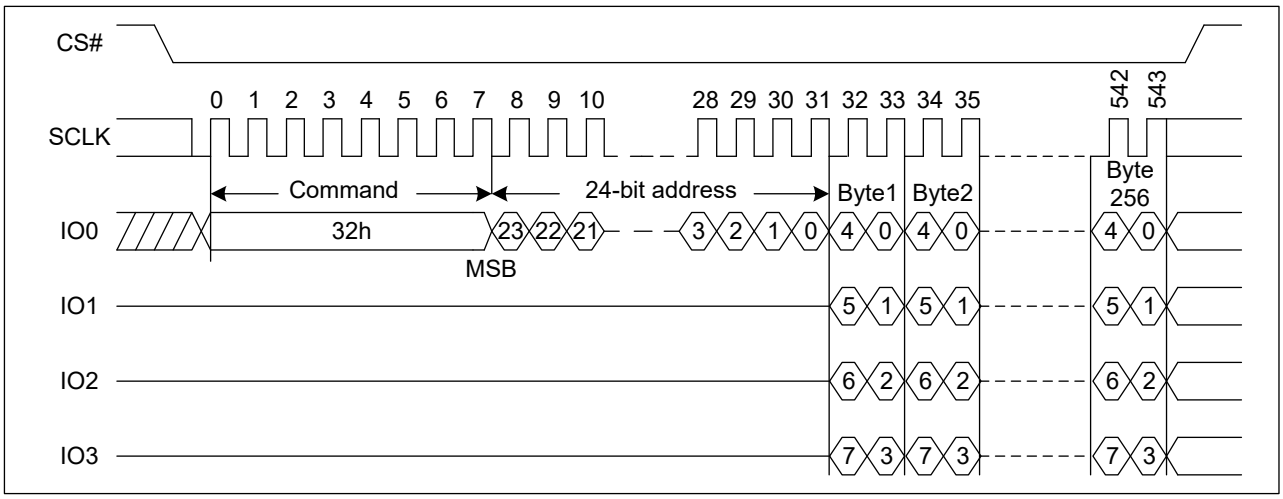
The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32h), three address bytes and at least one data byte on IO pins.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is $t_{PP}$) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1 and BP0) is not executed and WEL will clear to “0”.

**Figure 42. Quad Page Program Sequence Diagram**




## 7.21 Sector Erase (SE) (20h)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is $t_{SE}$) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1 and BP0) bit is not executed and WEL will clear to “0”.

**Figure 43. Sector Erase Sequence Diagram (SPI)**

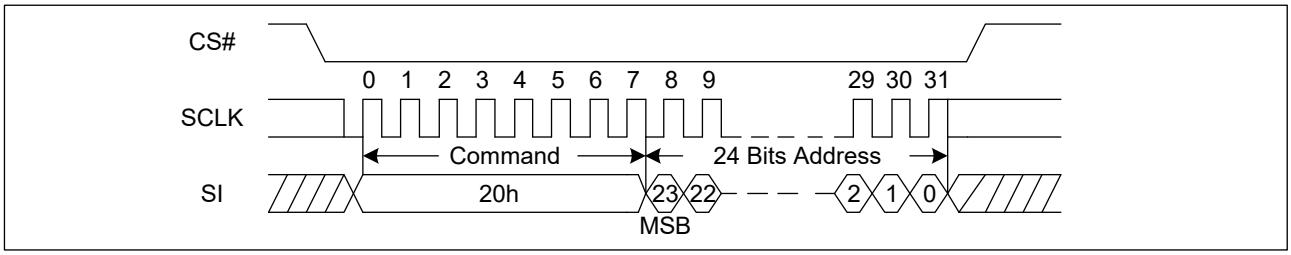
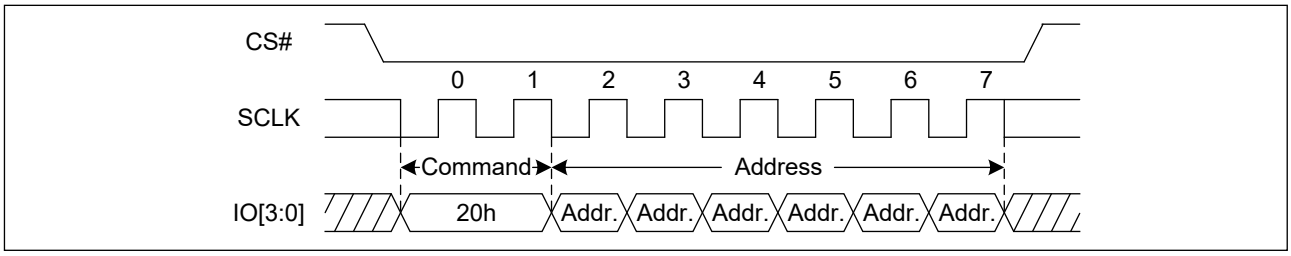



**Figure 44. Sector Erase Sequence Diagram (QPI)**



## 7.22 32KB Block Erase (BE32) (52h)

The 32KB Block Erase command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is $t_{BE1}$) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1 and BP0) bits is not executed and WEL will clear to "0".

**Figure 45. 32KB Block Erase Sequence Diagram (SPI)**

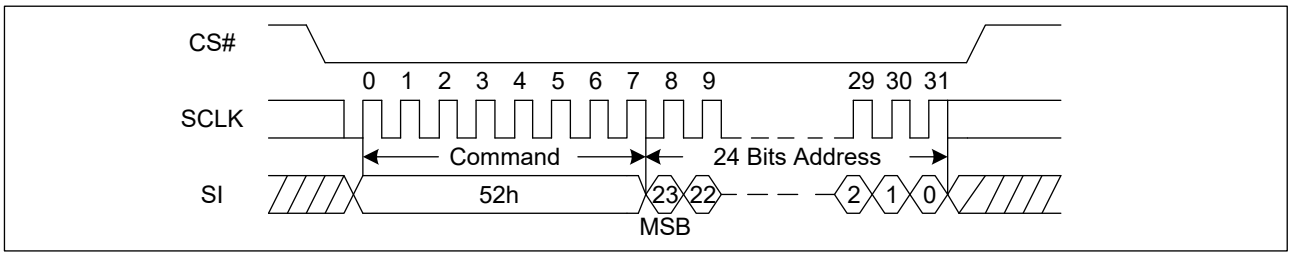
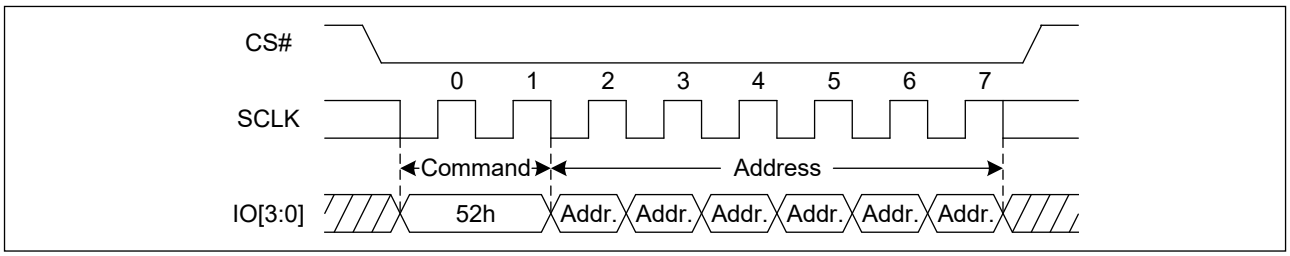



**Figure 46. 32KB Block Erase Sequence Diagram (QPI)**




## 7.23 64KB Block Erase (BE64) (D8h)

The 64KB Block Erase command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is $t_{BE2}$) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1 and BP0) bits is not executed and WEL will clear to "0".

**Figure 47. 64KB Block Erase Sequence Diagram (SPI)**

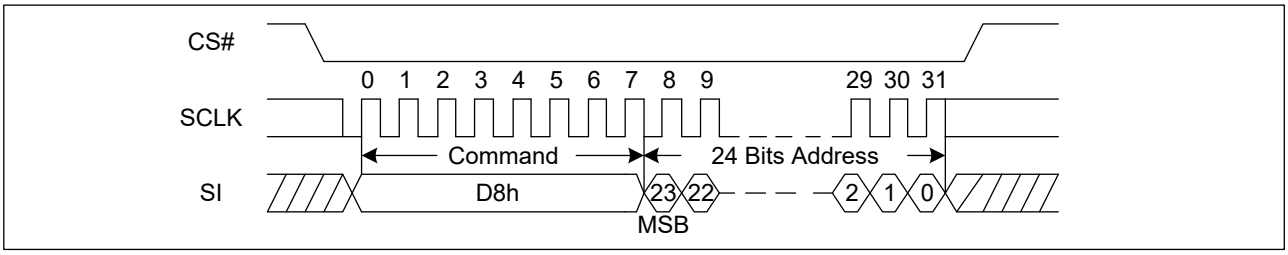
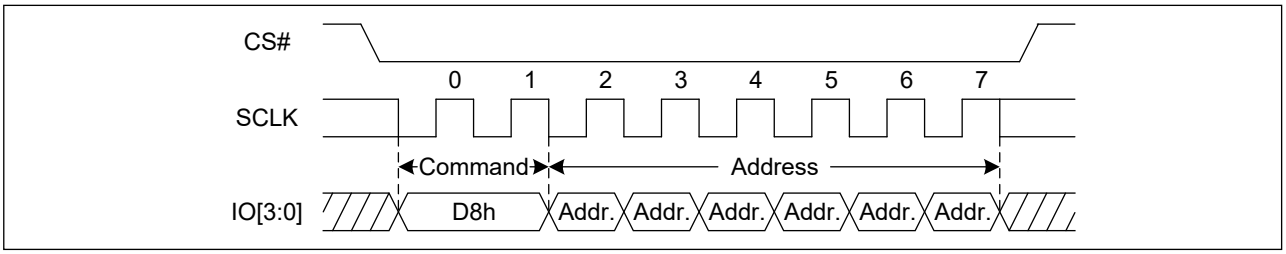



**Figure 48. 64KB Block Erase Sequence Diagram (QPI)**




## 7.24 Chip Erase (CE) (60h/C7h)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is $t_{CE}$) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1 and BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1 and BP0) bits are 1 and CMP=1. The Chip Erase (CE) command is ignored if one or more sectors are protected and WEL will clear to “0”.

**Figure 49. Chip Erase Sequence Diagram (SPI)**

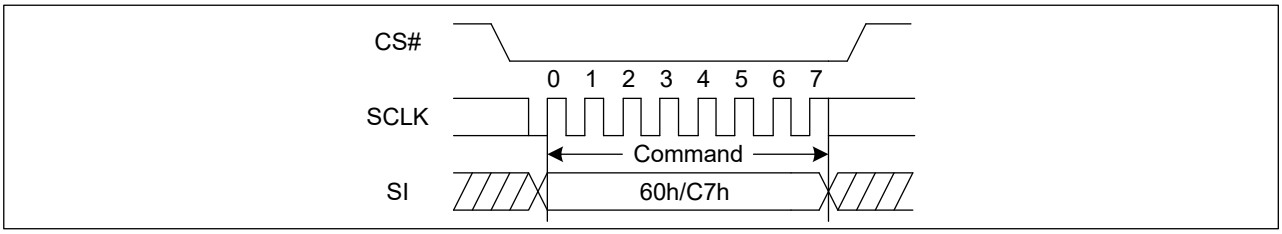
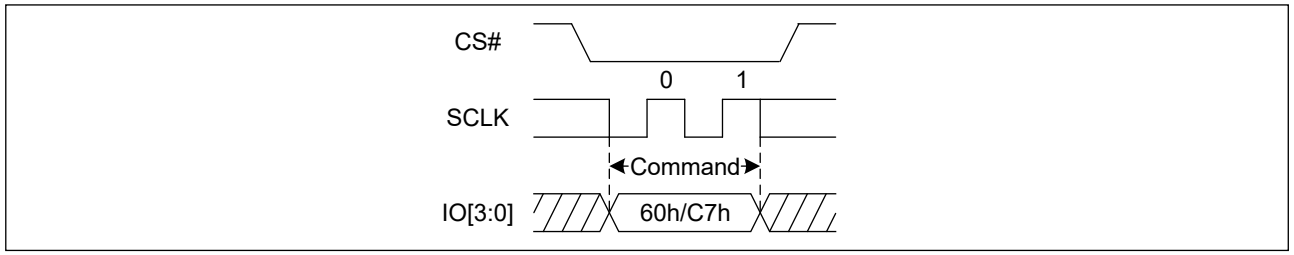


**Figure 50. Chip Erase Sequence Diagram (QPI)**




## 7.25 Read Manufacture ID/ Device ID (REMS) (90h)

The Read Manufacturer/Device ID command is a read Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90h” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first.

**Figure 51. Read Manufacture ID/ Device ID Sequence Diagram (SPI)**

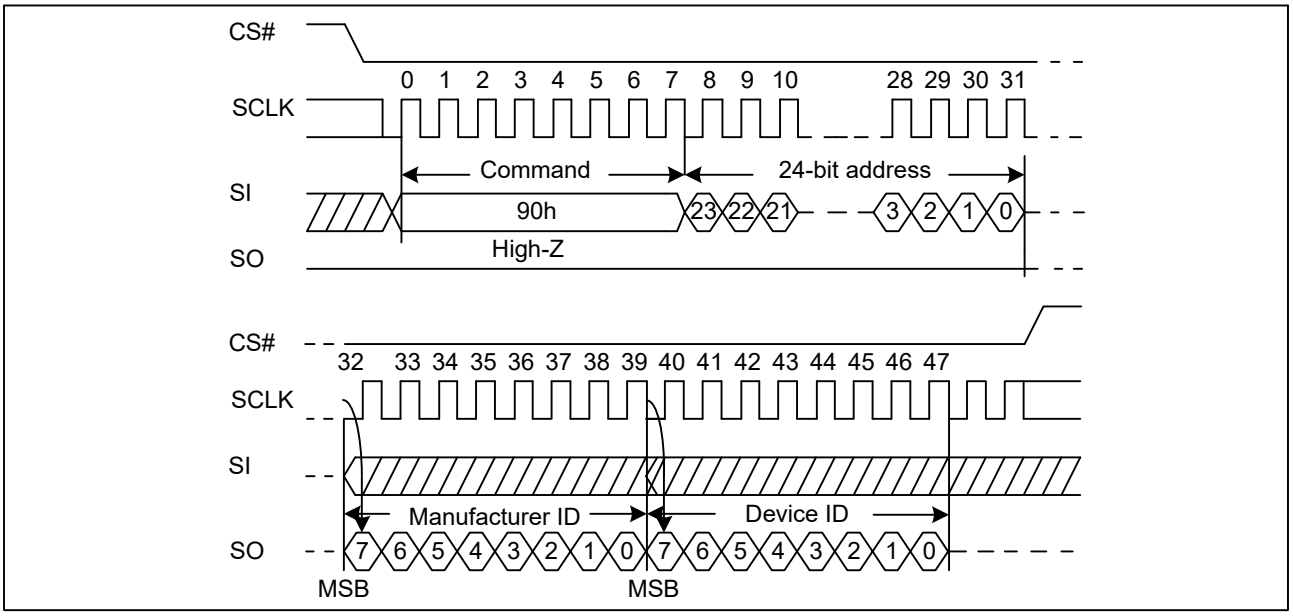
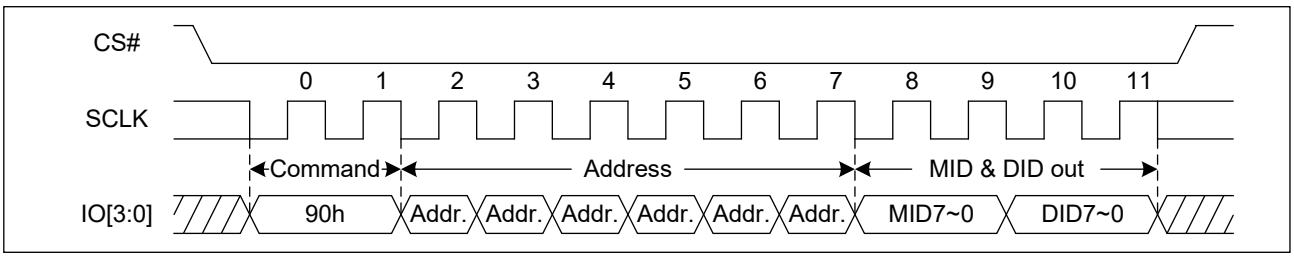



**Figure 52. Read Manufacture ID/ Device ID Sequence Diagram (QPI)**




## 7.26 Read Identification (RDID) (9Fh)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress, is not

decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The Read Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

**Figure 53. Read Identification ID Sequence Diagram (SPI)**

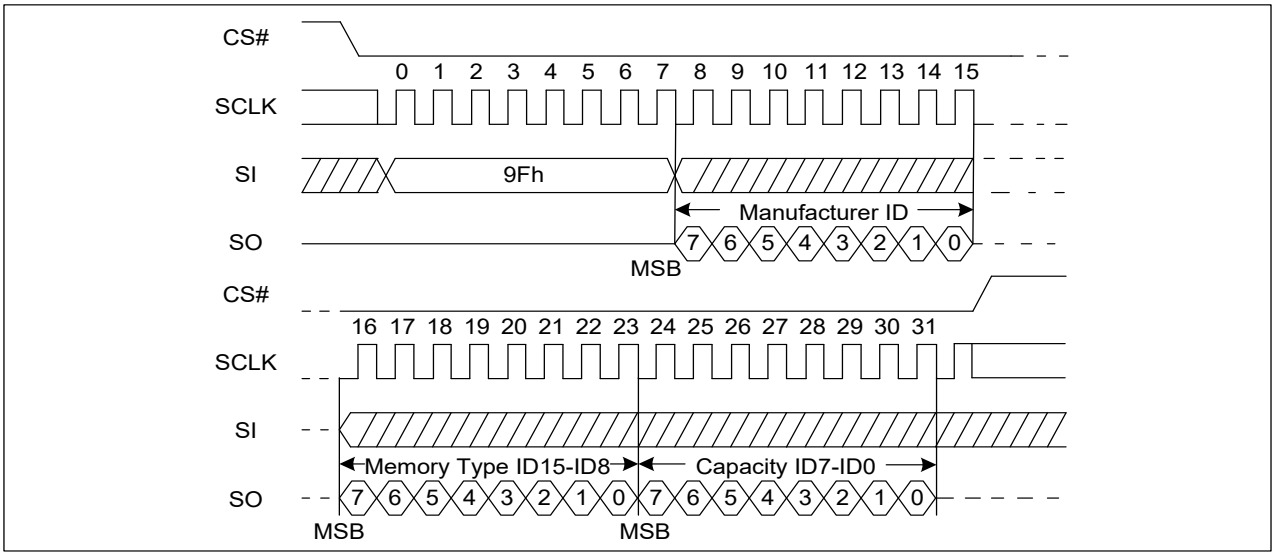
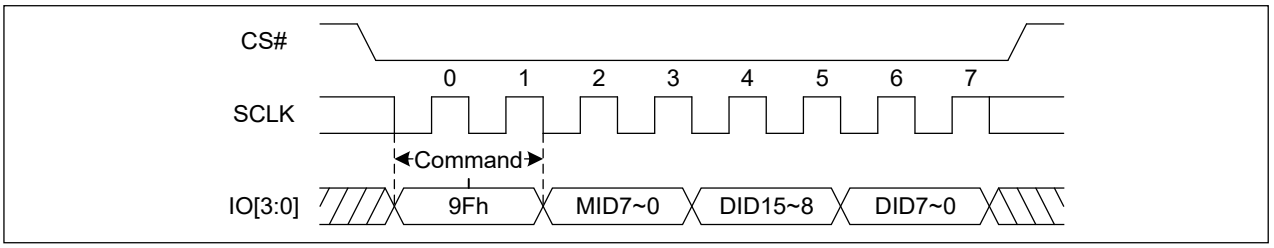



**Figure 54. Read Identification ID Sequence Diagram (QPI)**

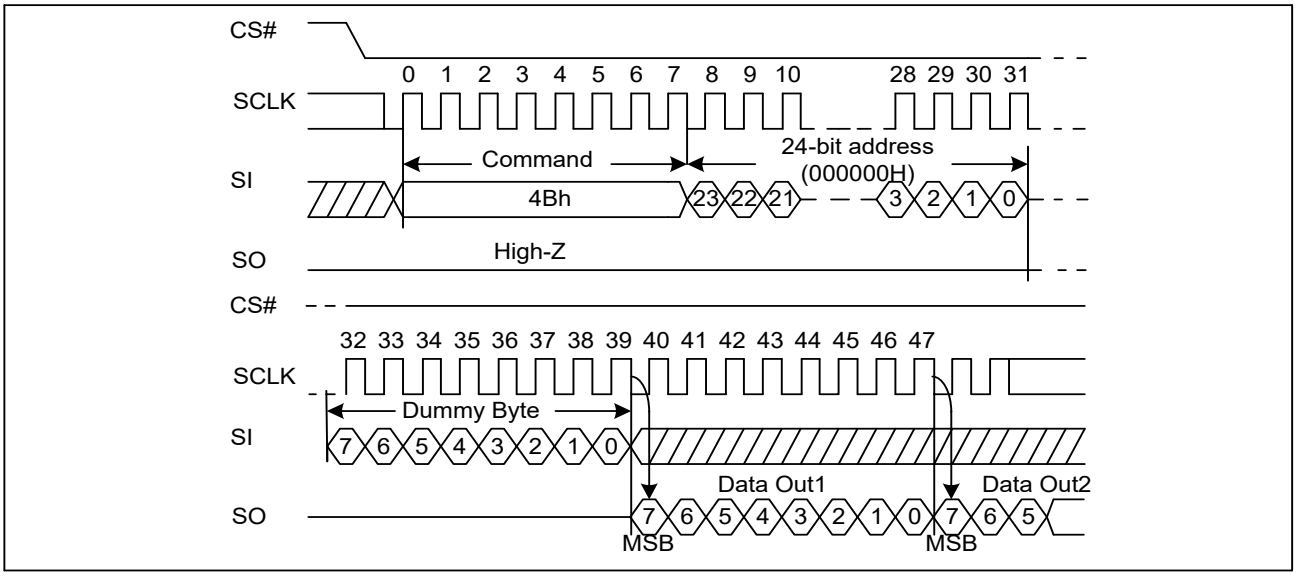



## 7.27 Read Unique ID (4Bh)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command → 3-Byte Address (000000H) →Dummy Byte→128bit Unique ID Out →CS# goes high.

**Figure 55. Read Unique ID Sequence Diagram**




## 7.28 Erase Security Registers (44h)

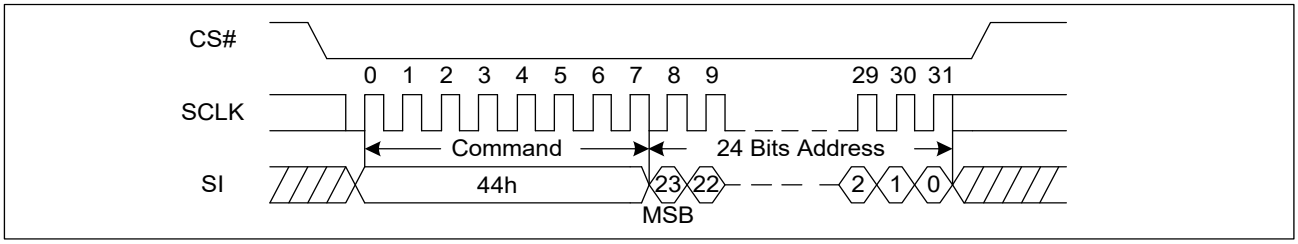
The GD25LQ64H provides 3x1024-Byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → 3-byte address on SI → CS# goes high. The command sequence is shown below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is $t_{SE}$) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB1, LB2, LB3) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored and WEL will clear to "0".

| Address | A23-16 | A15-12 | A11-10 | A9-0 |
|---|---|---|---|---|
| **Security Register 1** | 00H | 0001b | 00b | Don't care |
| **Security Register 2** | 00H | 0010b | 00b | Don't care |
| **Security Register 3** | 00H | 0011b | 00b | Don't care |

**Figure 56. Erase Security Registers command Sequence Diagram**



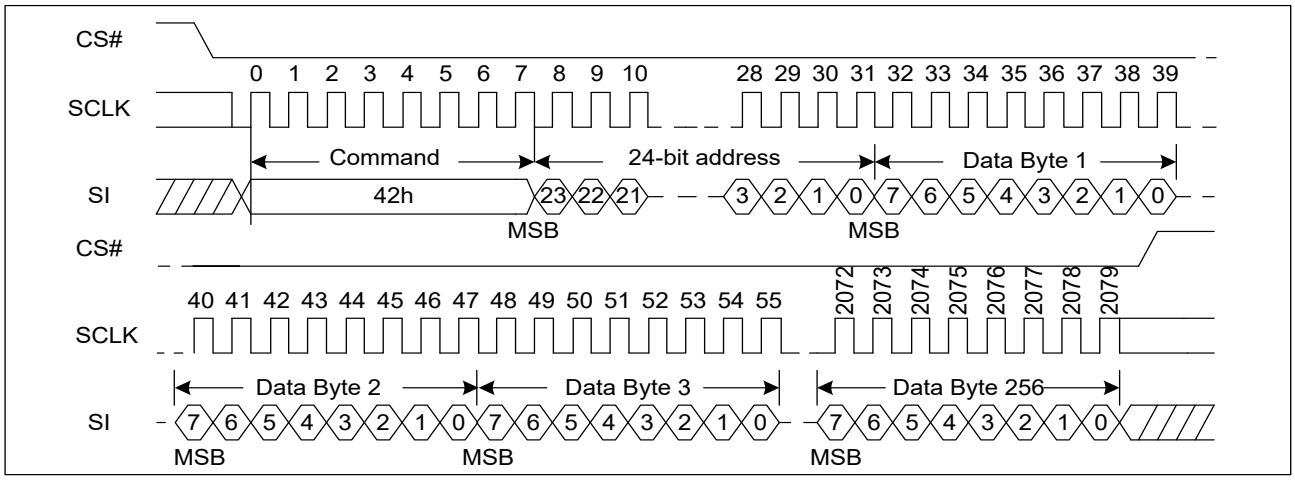
## 7.29 Program Security Registers (42h)

The Program Security Registers command is similar to the Page Program command. Each security register contains four pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42h), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is $t_{PP}$) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB1, LB2, LB3) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored and WEL will clear to “0”.

| Address | A23-16 | A15-12 | A11-10 | A9-0 |
|---|---|---|---|---|
| **Security Register 1** | 00H | 0001b | 00b | Byte Address |
| **Security Register 2** | 00H | 0010b | 00b | Byte Address |
| **Security Register 3** | 00H | 0011b | 00b | Byte Address |

**Figure 57. Program Security Registers command Sequence Diagram**

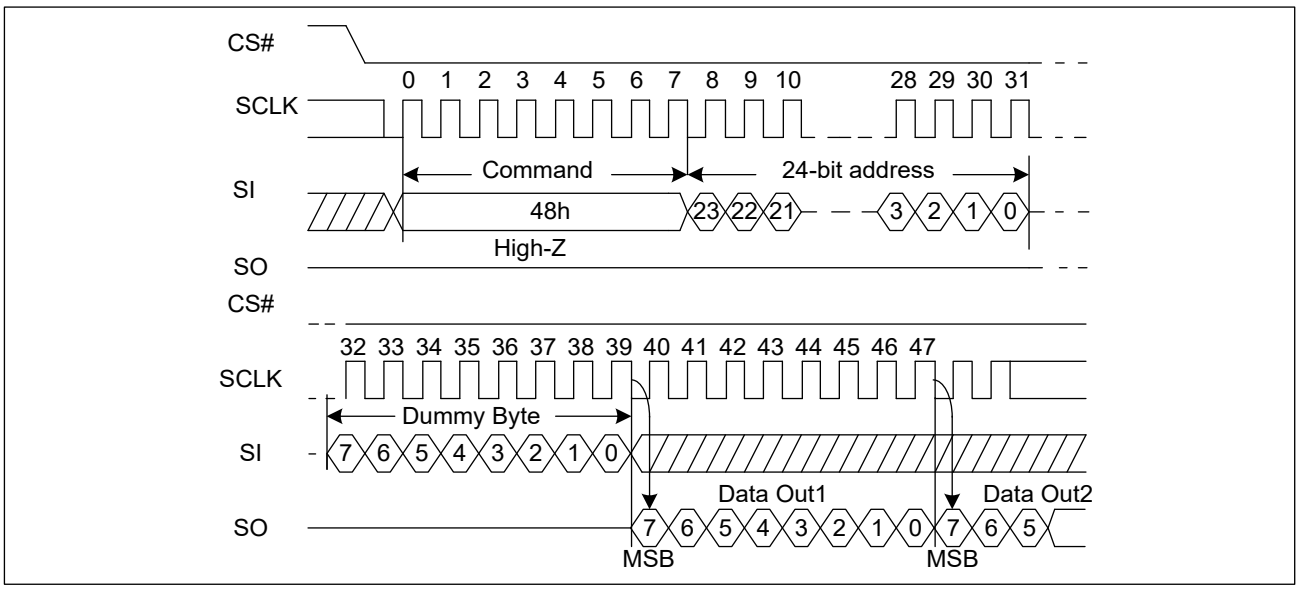



## 7.30 Read Security Registers (48h)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency $f_C$, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

| Address | A23-16 | A15-12 | A11-10 | A9-0 |
|---|---|---|---|---|
| **Security Register 1** | 00H | 0001b | 00b | Byte Address |
| **Security Register 2** | 00H | 0010b | 00b | Byte Address |
| **Security Register 3** | 00H | 0011b | 00b | Byte Address |

**Figure 58. Read Security Registers command Sequence Diagram**




## 7.31 Enable Reset (66h) and Reset (99h)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Deep Power Down Mode, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The “Enable Reset (66h)” and the “Reset (99h)” commands can be issued in either SPI or QPI mode. The “Enable Reset (66h)” and “Reset (99h)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately $t_{RST}$/$t_{RST_E}$ to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the WIP bit and the SUS1/SUS2 bit in Status Register before issuing the Reset command sequence.

**Figure 59. Enable Reset and Reset command Sequence Diagram (SPI)**

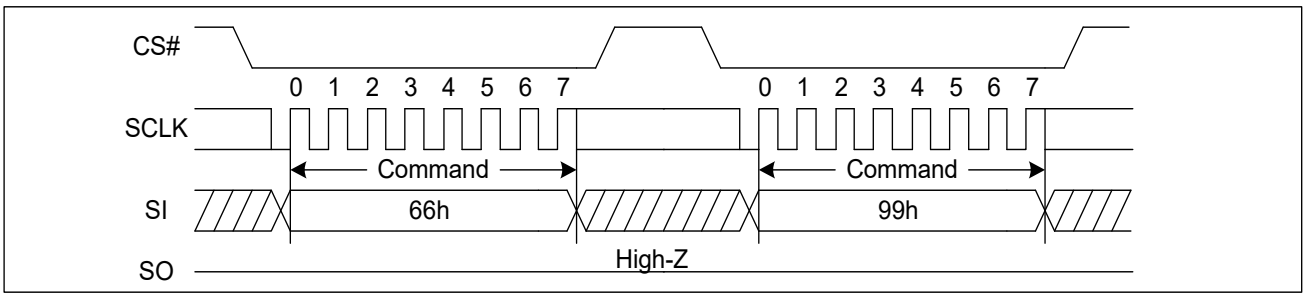
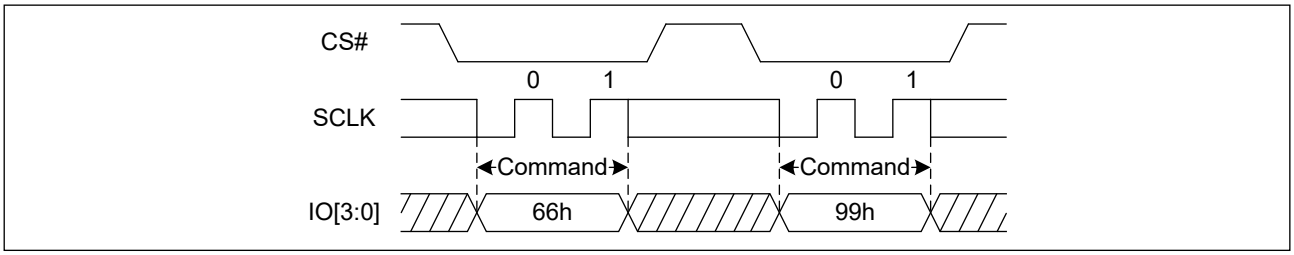


**Figure 60. Enable Reset and Reset command Sequence Diagram (QPI)**




Note: Enable Reset (66h) and Reset (99h) commands cannot reset the device when the device is in DTR Quad I/O Continuous Read Mode. The only way to quit the DTR Quad I/O Continuous Read Mode is to set the "Continuous Read Mode" bits (M5-4) not equal to (1,0).

## 7.32 Program/Erase Suspend (PES) (75h)

The Program/Erase Suspend command "75h", allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01h, 31h, 11h) and Erase/Program Security Registers command (44h, 42h) and Erase commands (20h, 52h, D8h, C7h, 60h) and Page Program command (02h, 32h) are not allowed during Program suspend. The Write Status Register command (01h, 31h, 11h) and Erase Security Registers command (44h) and Erase commands (20h, 52h, D8h, C7h, 60h) are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of "tsus" (See AC Characteristics) is required to suspend the program/erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS1/SUS2 bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS1/SUS2 bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within "tsus" and the SUS1/SUS2 bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state.

**Figure 61. Program/Erase Suspend Sequence Diagram (SPI)**

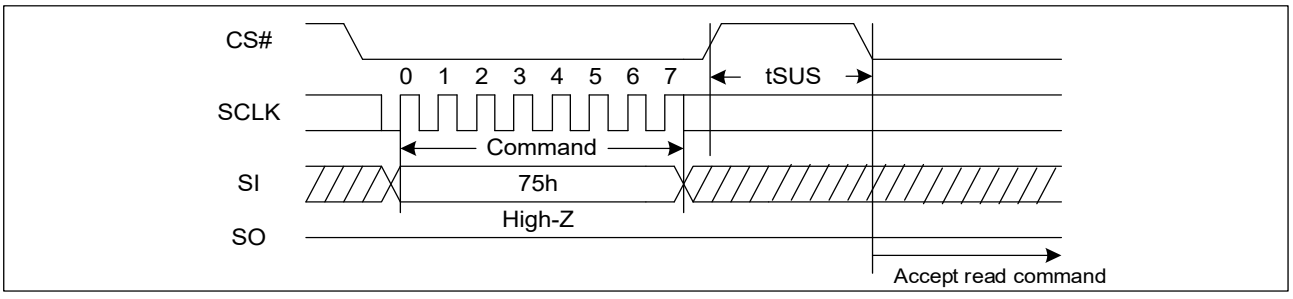
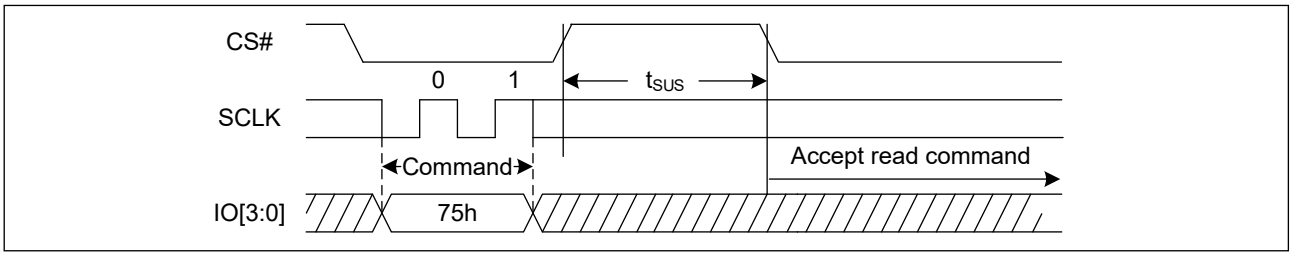



**Figure 62. Program/Erase Suspend Sequence Diagram (QPI)**



## 7.33 Program/Erase Resume (PER) (7Ah)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase command will be accepted by the device only if the SUS1/SUS2 bit equal to 1 and the WIP bit equal to 0. After issued the SUS1/SUS2 bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active.

**Figure 63. Program/Erase Resume Sequence Diagram (SPI)**

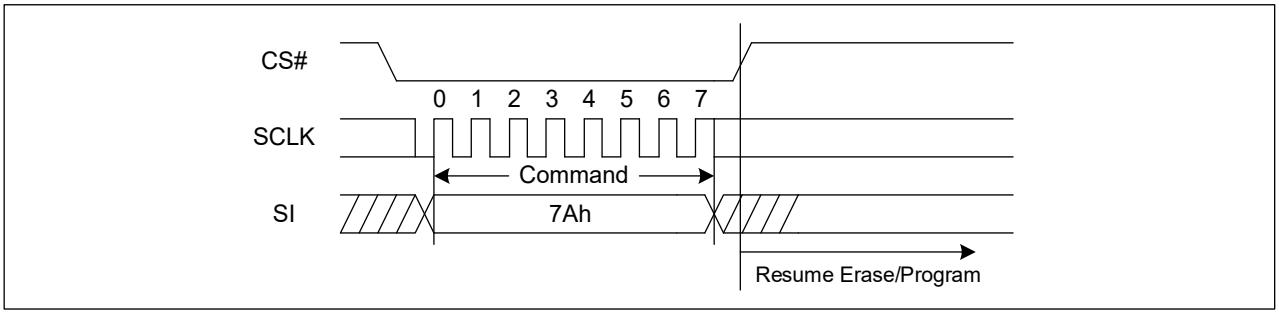
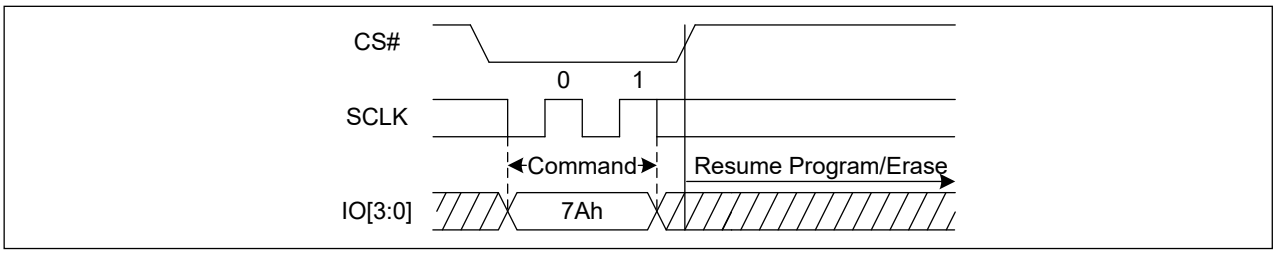



**Figure 64. Program/Erase Resume Sequence Diagram (QPI)**




## 7.34 Deep Power-Down (DP) (B9h)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command or software reset command. The Release from Deep Power-Down and Read Device ID (RDI) command releases the device from Deep Power-Down mode, also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always in the Standby Mode after Power-Up.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of $t_{DP}$ before the supply current is reduced to $I_{CC2}$ and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 65. Deep Power-Down Sequence Diagram (SPI)**

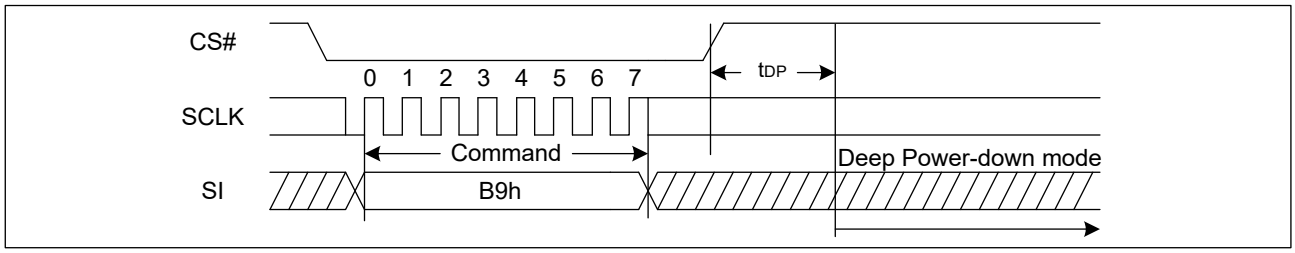
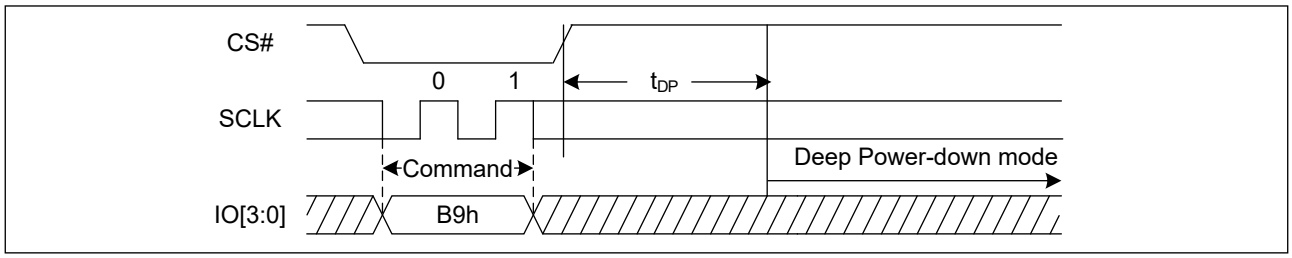



**Figure 66. Deep Power-Down Sequence Diagram (QPI)**




## 7.35 Release from Deep Power-Down and Read Device ID (RDI) (ABh)

The Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code "ABh" and driving CS# high. Release from Power-Down will take the time duration of $t_{RES1}$ (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the $t_{RES1}$ time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABh" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, except that after CS# is driven high it must remain high for a time duration of $t_{RES2}$ (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the command is ignored and will not have any effects on the current cycle.

**Figure 67. Release Power-Down Sequence Diagram (SPI)**

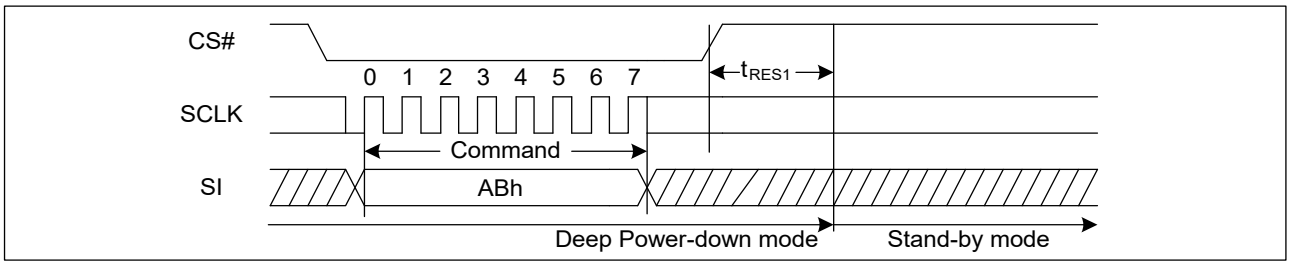


**Figure 68. Release Power-Down Sequence Diagram (QPI)**

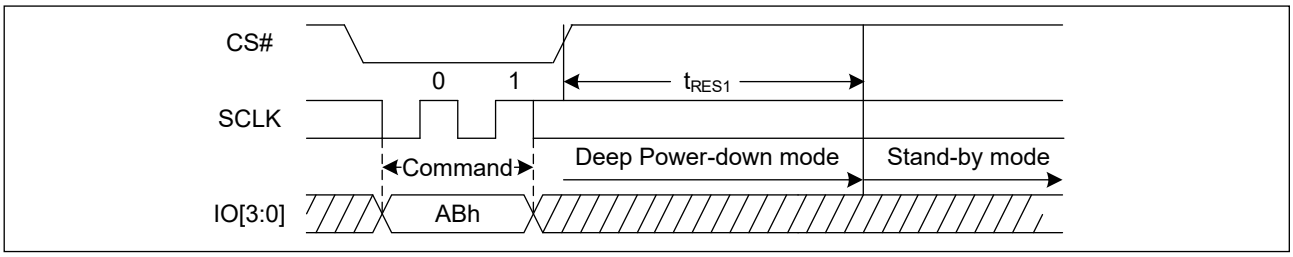



**Figure 69. Release Power-Down/Read Device ID Sequence Diagram (SPI)**

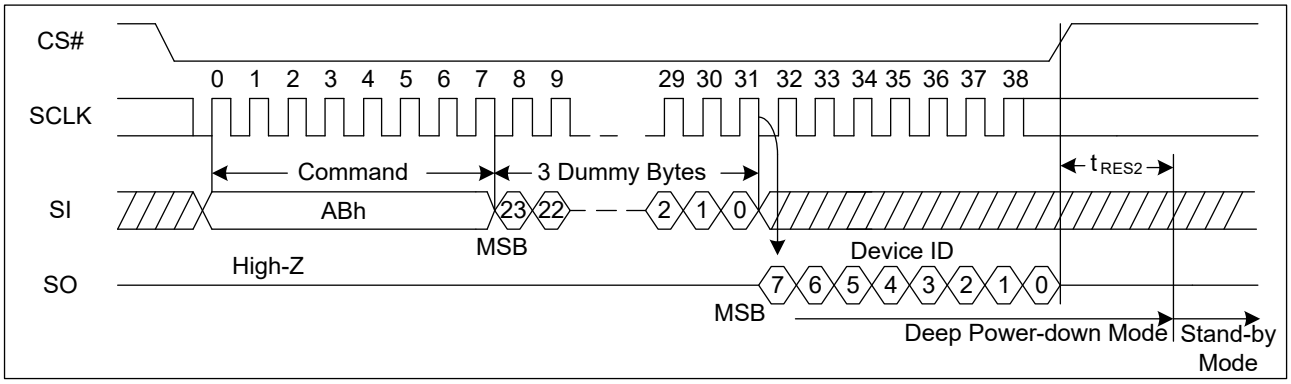
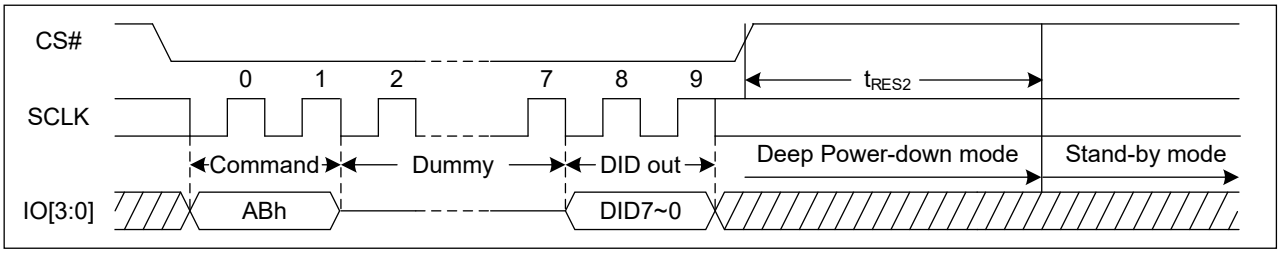


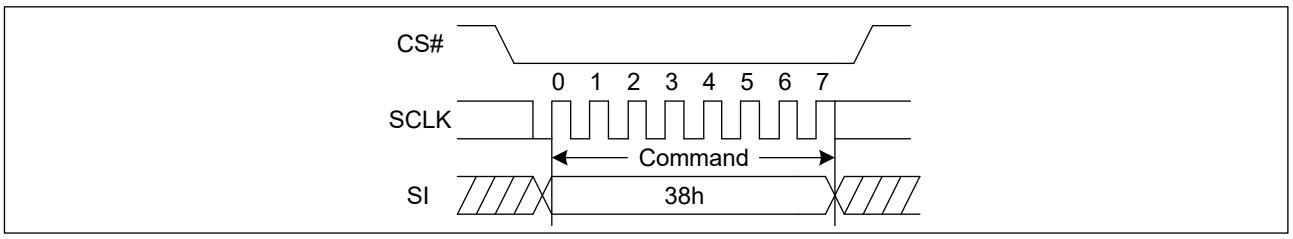

**Figure 70. Release Power-Down/Read Device ID Sequence Diagram (QPI)**




## 7.36 Enable QPI (38h)

The GD25LQ64H supports both Standard/Dual/Quad SPI and QPI mode. The “Enable QPI (38h)” command can switch the device from SPI mode to QPI mode. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register must be set to 1 first, and “Enable QPI (38h)” command must be issued. If the QE bit is 0, the “Enable QPI (38h)” command will be ignored and the device will remain in SPI mode. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

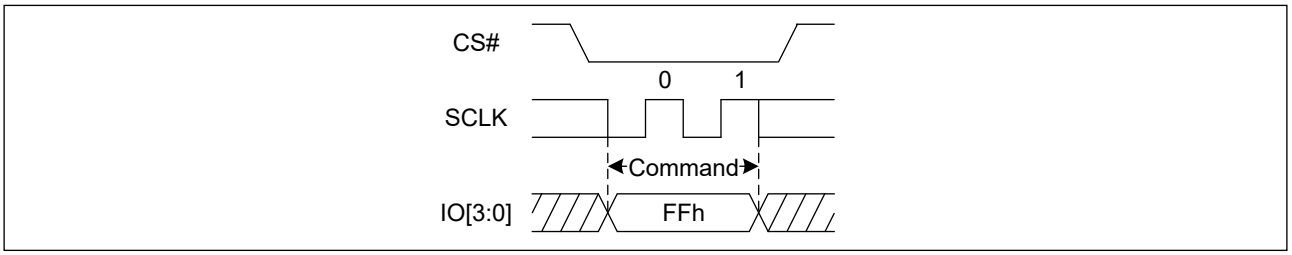
**Figure 71. Enable QPI mode command Sequence Diagram**



## 7.37 Disable QPI (FFh)

To exit the QPI mode and return to Standard/Dual/Quad SPI mode, the “Disable QPI (FFh)” command must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

**Figure 72. Disable QPI mode command Sequence Diagram**




## 7.38 Read Serial Flash Discoverable Parameter (5Ah)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216C.

**Figure 73. Read Serial Flash Discoverable Parameter command Sequence Diagram**

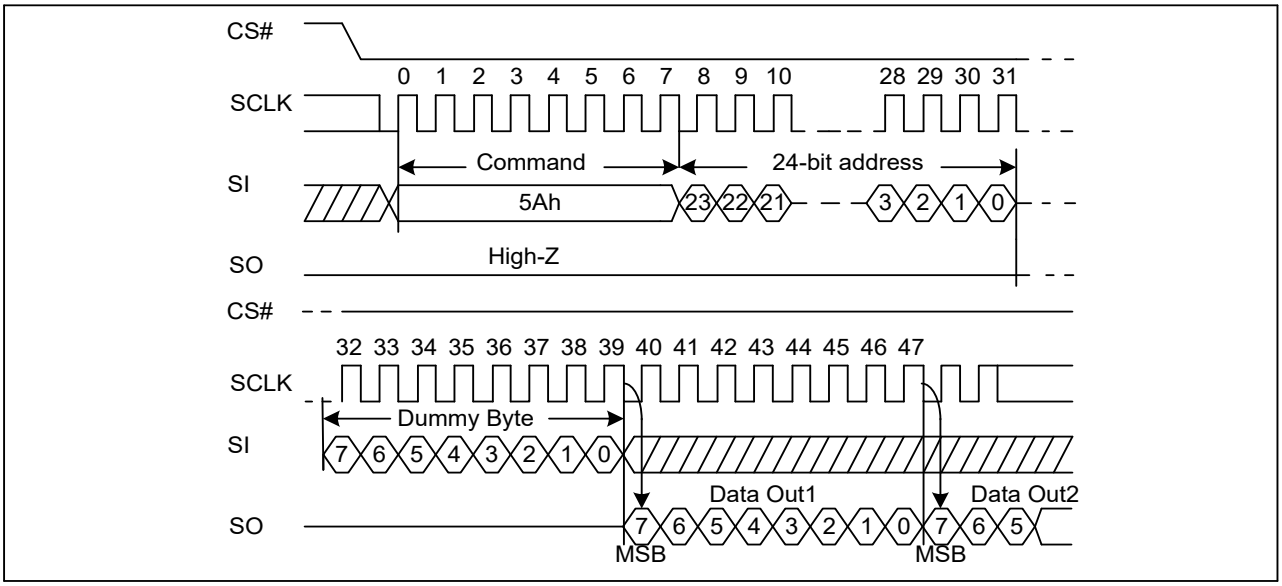



**Table 10. Signature and Parameter Identification Data Values (Please contact GigaDevice for Details)**

# 8 ELECTRICAL CHARACTERISTICS

## 8.1 Power-On Timing

**Figure 74. Power-On Timing Sequence Diagram**

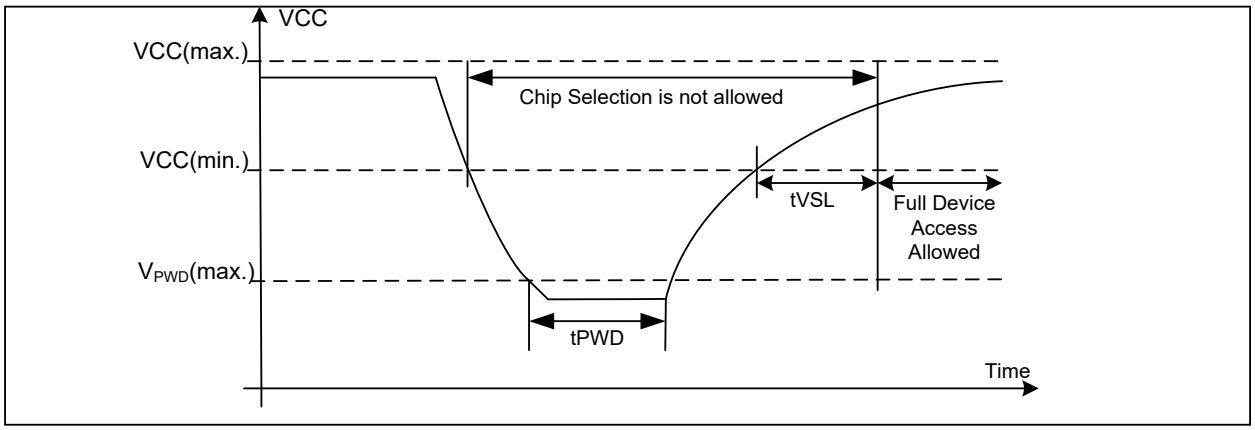



**Table 11. Power-Up Timing and Write Inhibit Threshold**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tVSL | VCC (min.) to device operation | 0.7 | | ms |
| VWI | Write Inhibit Voltage | | 1.5 | V |
| VPWD | VCC voltage needed to below VPWD for ensuring initialization will occur | | 0.5 | V |
| tPWD | The minimum duration for ensuring initialization will occur | 300 | | μs |

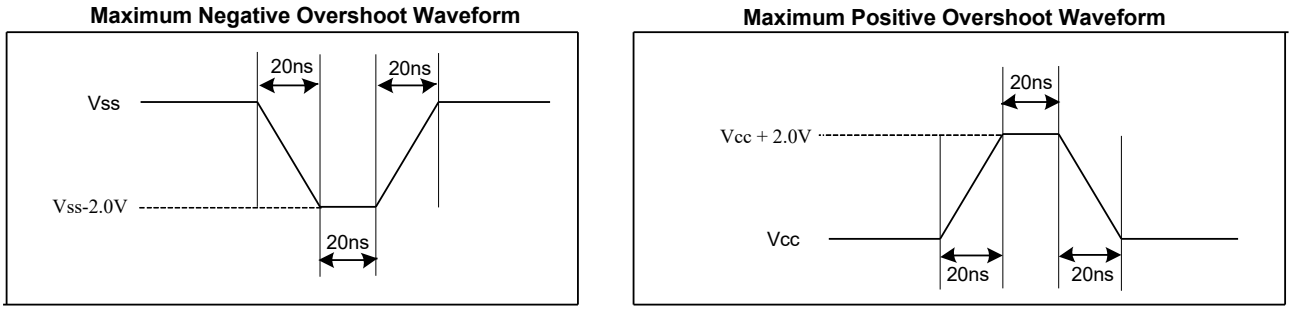
## 8.2 Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each Byte contains FFH). The Status Register contains 00H, except that DRV0 bit (S21) is set to 1.

## 8.3 Absolute Maximum Ratings

| Parameter | Value | Unit |
|---|---|---|
| Ambient Operating Temperature ($T_A$) | -40 to 85<br>-40 to 105<br>-40 to 125 | ℃ |
| Storage Temperature | -65 to 150 | ℃ |
| Transient Input/Output Voltage (note: overshoot) | -2.0 to VCC+2.0 | V |
| Applied Input/Output Voltage | -0.6 to VCC+0.4 | V |
| VCC | -0.6 to 2.5 | V |

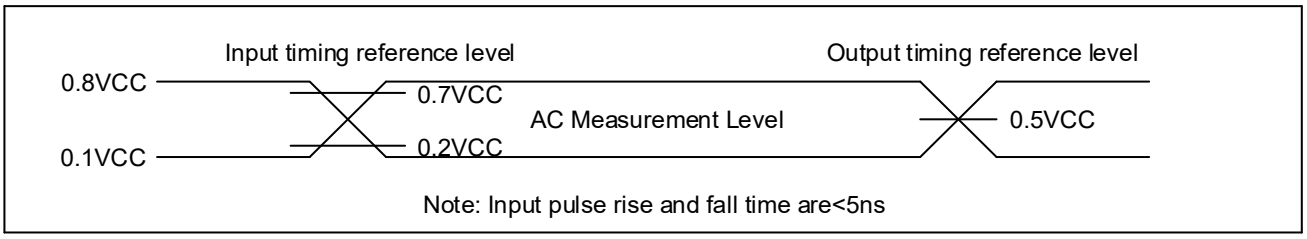
**Figure 75. Input Test Waveform and Measurement Level**




## 8.4 Capacitance Measurement Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | | | 6 | pF | VIN=0V |
| COUT | Output Capacitance | | | 8 | pF | VOUT=0V |
| $C_L$ | Load Capacitance | | 30 | | pF | |
| | Input Rise And Fall time | | | 5 | ns | |
| | Input Pulse Voltage | | 0.1VCC to 0.8VCC | | V | |
| | Input Timing Reference Voltage | | 0.3VCC to 0.7VCC | | V | |
| | Output Timing Reference Voltage | | 0.5VCC | | V | |

**Figure 76. Absolute Maximum Ratings Diagram**



## 8.5 DC Characteristics

($T_A$ = -40℃~85℃, VCC=1.65~2.0V)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | | | | ±2 | μA |
| $I_{LO}$ | Output Leakage Current | | | | ±2 | μA |
| $I_{CC1}$ | Standby Current | CS#=VCC,<br>VIN=VCC or VSS | | 10 | 28 | μA |
| $I_{CC2}$ | Deep Power-Down Current | CS#=VCC,<br>VIN=VCC or VSS | | 1 | 10 | μA |
| $I_{CC3}$ | Operating Current (Read) | CLK=0.1VCC / 0.9VCC at 133MHz,<br>Q=Open(*1,*2,*4 I/O) | | 10 | 14 | mA |
| | | CLK=0.1VCC / 0.9VCC at 80MHz,<br>Q=Open(*1,*2,*4 I/O) | | 7 | 10 | mA |
| | | CLK=0.1VCC / 0.9VCC at DTR 104MHz,<br>Q=Open(*4 I/O) | | 9 | 12 | mA |
| $I_{CC4}$ | Operating Current (PP) | CS#=VCC | | 12 | 20 | mA |
| $I_{CC5}$ | Operating Current (WRSR) | CS#=VCC | | 12 | 20 | mA |
| $I_{CC6}$ | Operating Current (SE) | CS#=VCC | | 12 | 20 | mA |
| $I_{CC7}$ | Operating Current (BE) | CS#=VCC | | 12 | 20 | mA |
| $I_{CC8}$ | Operating Current (CE) | CS#=VCC | | 12 | 20 | mA |
| $V_{IL}$ | Input Low Voltage | | -0.5 | | 0.2VCC | V |
| $V_{IH}$ | Input High Voltage | | 0.7VCC | | VCC+0.4 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 100μA | | | 0.2 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -100μA | VCC-0.2 | | | V |

Note:

1. Typical value at $T_A$ = 25℃, VCC = 1.8V; Maximum value at $T_A$ = 85℃, VCC = 2.0V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

($T_A$ = -40℃~105℃, VCC=1.65~2.0V)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | | | | ±2 | μA |
| $I_{LO}$ | Output Leakage Current | | | | ±2 | μA |
| $I_{CC1}$ | Standby Current | CS#=VCC,<br>VIN=VCC or VSS | | 10 | 50 | μA |
| $I_{CC2}$ | Deep Power-Down Current | CS#=VCC,<br>VIN=VCC or VSS | | 1 | 25 | μA |
| $I_{CC3}$ | Operating Current (Read) | CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(*1,*2,*4 I/O) | | 10 | 14 | mA |
| | | CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O) | | 7 | 10 | mA |
| | | CLK=0.1VCC / 0.9VCC at DTR 104MHz, Q=Open(*4 I/O) | | 9 | 12 | mA |
| $I_{CC4}$ | Operating Current (PP) | CS#=VCC | | 12 | 23 | mA |
| $I_{CC5}$ | Operating Current (WRSR) | CS#=VCC | | 12 | 23 | mA |
| $I_{CC6}$ | Operating Current (SE) | CS#=VCC | | 12 | 23 | mA |
| $I_{CC7}$ | Operating Current (BE) | CS#=VCC | | 12 | 23 | mA |
| $I_{CC8}$ | Operating Current (CE) | CS#=VCC | | 12 | 23 | mA |
| $V_{IL}$ | Input Low Voltage | | -0.5 | | 0.2VCC | V |
| $V_{IH}$ | Input High Voltage | | 0.7VCC | | VCC+0.4 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 100μA | | | 0.2 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -100μA | VCC-0.2 | | | V |

Note:

1. Typical value at $T_A$ = 25℃, VCC = 1.8V; Maximum value at $T_A$ = 105℃, VCC = 2.0V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

($T_A$ = -40℃~125℃, VCC=1.65~2.0V)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | | | | ±2 | μA |
| $I_{LO}$ | Output Leakage Current | | | | ±2 | μA |
| $I_{CC1}$ | Standby Current | CS#=VCC,<br>VIN=VCC or VSS | | 10 | 100 | μA |
| $I_{CC2}$ | Deep Power-Down Current | CS#=VCC,<br>VIN=VCC or VSS | | 1 | 50 | μA |
| $I_{CC3}$ | Operating Current (Read) | CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(*1,*2,*4 I/O) | | 10 | 14 | mA |
| | | CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O) | | 7 | 10 | mA |
| | | CLK=0.1VCC / 0.9VCC at DTR 104MHz, Q=Open(*4 I/O) | | 9 | 12 | mA |
| $I_{CC4}$ | Operating Current (PP) | CS#=VCC | | 12 | 23 | mA |
| $I_{CC5}$ | Operating Current (WRSR) | CS#=VCC | | 12 | 23 | mA |
| $I_{CC6}$ | Operating Current (SE) | CS#=VCC | | 12 | 23 | mA |
| $I_{CC7}$ | Operating Current (BE) | CS#=VCC | | 12 | 23 | mA |
| $I_{CC8}$ | Operating Current (CE) | CS#=VCC | | 12 | 23 | mA |
| $V_{IL}$ | Input Low Voltage | | -0.5 | | 0.2VCC | V |
| $V_{IH}$ | Input High Voltage | | 0.7VCC | | VCC+0.4 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 100μA | | | 0.2 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -100μA | VCC-0.2 | | | V |

Note:

1. Typical value at $T_A$ = 25℃, VCC = 1.8V; Maximum value at $T_A$ = 125℃, VCC = 2.0V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

## 8.6 AC Characteristics

($T_A$ = -40℃~85℃, VCC=1.65~2.0V)

| Symbol | Parameter | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|
| $f_{C1}$ | Serial Clock Frequency For: all commands except Read (03h), DTR Dual I/O Fast Read (BDh), DTR Quad I/O Fast Read (EDh) and DTR Burst Read with Wrap (0Eh) | | | 133 | MHz |
| $f_{C2}$ | Serial Clock Frequency For: BDh, EDh, 0Eh | | | 104 | MHz |
| $f_R$ | Serial Clock Frequency For: 03h | | | 90 | MHz |
| $t_{CLH}$ | Serial Clock High Time | 45% (1/$Fc_{MAX}$) | | | ns |
| $t_{CLL}$ | Serial Clock Low Time | 45% (1/$Fc_{MAX}$) | | | ns |
| $t_{CLCH}$ | Serial Clock Rise Time (Slew Rate) | 0.1 | | | V/ns |
| $t_{CHCL}$ | Serial Clock Fall Time (Slew Rate) | 0.1 | | | V/ns |
| $t_{SLCH}$ | CS# Active Setup Time | 3 | | | ns |
| $t_{CHSH}$ $t_{CLSH}$ | CS# Active Hold Time | 3 | | | ns |
| $t_{SHCH}$ | CS# Not Active Setup Time | 3 | | | ns |
| $t_{CHSL}$ | CS# Not Active Hold Time | 3 | | | ns |
| $t_{SHSL}$ | CS# High Time (Read/Write) | 20 | | | ns |
| $t_{SHQZ}$ | Output Disable Time | | | 6 | ns |
| $t_{CLQX}$ $t_{CHQX}$ | Output Hold Time | 1.2 | | | ns |
| $t_{DVCH}$ $t_{DVCL}$ | Data In Setup Time | 2 | | | ns |
| $t_{CHDX}$ $t_{CLDX}$ | Data In Hold Time | 2 | | | ns |
| $t_{HLCH}$ | HOLD# Low Setup Time (Relative To Clock) | 5 | | | ns |
| $t_{HHCH}$ | HOLD# High Setup Time (Relative To Clock) | 5 | | | ns |
| $t_{CHHH}$ | HOLD# Low Hold Time (Relative To Clock) | 5 | | | ns |
| $t_{CHHL}$ | HOLD# High Hold Time (Relative To Clock) | 5 | | | ns |
| $t_{HLQZ}$ | HOLD# Low To High-Z Output | | | 6 | ns |
| $t_{HHQX}$ | HOLD# High To Low-Z Output | | | 6 | ns |
| $t_{CLQV}$ | Clock Low To Output Valid (CL = 30pF) | | | 7 | ns |
| $t_{CHQV}$ | Clock Low To Output Valid (CL = 15pF) | | | 6 | ns |
| $t_{WHSL}$ | Write Protect Setup Time Before CS# Low | 20 | | | ns |
| $t_{SHWL}$ | Write Protect Hold Time After CS# High | 100 | | | ns |
| $t_{DP}$ | CS# High To Deep Power-Down Mode | | | 3 | μs |
| $t_{RES1}$ | CS# High To Standby Mode Without Electronic Signature Read | | | 20 | μs |

| | | | | | |
|---|---|---|---|---|---|
| $t_{RES2}$ | CS# High To Standby Mode With Electronic Signature Read | | | 20 | μs |
| $t_{SUS}$ | CS# High To Next Command After Suspend | | | 20 | μs |
| $t_{RS}$(3) | Latency Between Resume And Next Suspend | 100 | | | μs |
| $t_{RST}$ | CS# High To Next Command After Reset (Except From Erase) | | | 30 | μs |
| $t_{RST_E}$ | CS# High To Next Command After Reset (From Erase) | | | 12 | ms |
| $t_{CSL}$ | CS# Low Time | 500 | | | ns |
| $t_{CSH}$ | CS# High Time | 500 | | | ns |
| $t_{SISH}$ | SI# In Setup Time (Relative To CS#) | 5 | | | ns |
| $t_{SIHH}$ | SI# In Hold Time (Relative To CS#) | 5 | | | ns |
| $t_{RESET}$ | Internal Reset Time for JEDEC Reset Signaling | | | 100 | ms |
| $t_W$ | Write Status Register Cycle Time | | 2 | 25 | ms |
| $t_{BP}$ | Byte Program Time | | 30 | 120 | μs |
| $t_{PP}$ | Page Programming Time | | 0.18(4) | 1.5 | ms |
| $t_{SE}$ | Sector Erase Time | | 40(4) | 300 | ms |
| $t_{BE1}$ | Block Erase Time (32K Bytes) | | 0.1(4) | 0.8 | s |
| $t_{BE2}$ | Block Erase Time (64K Bytes) | | 0.16(4) | 1.2 | s |
| $t_{CE}$ | Chip Erase Time (GD25LQ64H) | | 10(4) | 40 | s |

Note:

1. Typical value at $T_A$ = 25℃; Maximum value at $T_A$ = 85℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Minimum timing must be observed before issuing the next suspend command, and a period equal to or longer than the minimum timing is required in order for the program or erase operation to make progress, but the operation time may exceed the maximum value.
4. Please contact GigaDevice for details regarding the faster page program / erase.

($T_A$ = -40℃~105℃, VCC=1.65~2.0V)

| Symbol | Parameter | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|
| $f_{C1}$ | Serial Clock Frequency For: all commands except Read (03h), DTR Dual I/O Fast Read (BDh), DTR Quad I/O Fast Read (EDh) and DTR Burst Read with Wrap (0Eh) | | | 133 | MHz |
| $f_{C2}$ | Serial Clock Frequency For: BDh, EDh, 0Eh | | | 104 | MHz |
| $f_R$ | Serial Clock Frequency For: 03h | | | 90 | MHz |
| $t_{CLH}$ | Serial Clock High Time | 45% (1/$Fc_{MAX}$) | | | ns |
| $t_{CLL}$ | Serial Clock Low Time | 45% (1/$Fc_{MAX}$) | | | ns |
| $t_{CLCH}$ | Serial Clock Rise Time (Slew Rate) | 0.1 | | | V/ns |
| $t_{CHCL}$ | Serial Clock Fall Time (Slew Rate) | 0.1 | | | V/ns |
| $t_{SLCH}$ | CS# Active Setup Time | 3 | | | ns |
| $t_{CHSH}$ $t_{CLSH}$ | CS# Active Hold Time | 3 | | | ns |
| $t_{SHCH}$ | CS# Not Active Setup Time | 3 | | | ns |
| $t_{CHSL}$ | CS# Not Active Hold Time | 3 | | | ns |
| $t_{SHSL}$ | CS# High Time (Read/Write) | 20 | | | ns |
| $t_{SHQZ}$ | Output Disable Time | | | 6 | ns |
| $t_{CLQX}$ $t_{CHQX}$ | Output Hold Time | 1.2 | | | ns |
| $t_{DVCH}$ $t_{DVCL}$ | Data In Setup Time | 2 | | | ns |
| $t_{CHDX}$ $t_{CLDX}$ | Data In Hold Time | 2 | | | ns |
| $t_{HLCH}$ | HOLD# Low Setup Time (Relative To Clock) | 5 | | | ns |
| $t_{HHCH}$ | HOLD# High Setup Time (Relative To Clock) | 5 | | | ns |
| $t_{CHHH}$ | HOLD# Low Hold Time (Relative To Clock) | 5 | | | ns |
| $t_{CHHL}$ | HOLD# High Hold Time (Relative To Clock) | 5 | | | ns |
| $t_{HLQZ}$ | HOLD# Low To High-Z Output | | | 6 | ns |
| $t_{HHQX}$ | HOLD# High To Low-Z Output | | | 6 | ns |
| $t_{CLQV}$ | Clock Low To Output Valid (CL = 30pF) | | | 7 | ns |
| $t_{CHQV}$ | Clock Low To Output Valid (CL = 15pF) | | | 6 | ns |
| $t_{WHSL}$ | Write Protect Setup Time Before CS# Low | 20 | | | ns |
| $t_{SHWL}$ | Write Protect Hold Time After CS# High | 100 | | | ns |
| $t_{DP}$ | CS# High To Deep Power-Down Mode | | | 3 | μs |
| $t_{RES1}$ | CS# High To Standby Mode Without Electronic Signature Read | | | 20 | μs |
| $t_{RES2}$ | CS# High To Standby Mode With Electronic Signature Read | | | 20 | μs |

| | | | | | |
|---|---|---|---|---|---|
| $t_{SUS}$ | CS# High To Next Command After Suspend | | | 20 | μs |
| $t_{RS}$(3) | Latency Between Resume And Next Suspend | 100 | | | μs |
| $t_{RST}$ | CS# High To Next Command After Reset (Except From Erase) | | | 30 | μs |
| $t_{RST_E}$ | CS# High To Next Command After Reset (From Erase) | | | 12 | ms |
| $t_{CSL}$ | CS# Low Time | 500 | | | ns |
| $t_{CSH}$ | CS# High Time | 500 | | | ns |
| $t_{SISH}$ | SI# In Setup Time (Relative To CS#) | 5 | | | ns |
| $t_{SIHH}$ | SI# In Hold Time (Relative To CS#) | 5 | | | ns |
| $t_{RESET}$ | Internal Reset Time for JEDEC Reset Signaling | | | 100 | ms |
| $t_W$ | Write Status Register Cycle Time | | 2 | 25 | ms |
| $t_{BP}$ | Byte Program Time | | 30 | 120 | μs |
| $t_{PP}$ | Page Programming Time | | 0.18(4) | 3 | ms |
| $t_{SE}$ | Sector Erase Time | | 40(4) | 400 | ms |
| $t_{BE1}$ | Block Erase Time (32K Bytes) | | 0.1(4) | 1 | s |
| $t_{BE2}$ | Block Erase Time (64K Bytes) | | 0.16(4) | 2.4 | s |
| $t_{CE}$ | Chip Erase Time (GD25LQ64H) | | 10(4) | 60 | s |

Note:

1. Typical value at $T_A$ = 25℃; Maximum value at $T_A$ = 105℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Minimum timing must be observed before issuing the next suspend command, and a period equal to or longer than the minimum timing is required in order for the program or erase operation to make progress, but the operation time may exceed the maximum value.
4. Please contact GigaDevice for details regarding the faster page program / erase.

($T_A$ = -40℃~125℃, VCC=1.65~2.0V)

| Symbol | Parameter | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|
| $f_{C1}$ | Serial Clock Frequency For: all commands except Read (03h), DTR Dual I/O Fast Read (BDh), DTR Quad I/O Fast Read (EDh) and DTR Burst Read with Wrap (0Eh) | | | 133 | MHz |
| $f_{C2}$ | Serial Clock Frequency For: BDh, EDh, 0Eh | | | 104 | MHz |
| $f_R$ | Serial Clock Frequency For: 03h | | | 90 | MHz |
| $t_{CLH}$ | Serial Clock High Time | 45% (1/$Fc_{MAX}$) | | | ns |
| $t_{CLL}$ | Serial Clock Low Time | 45% (1/$Fc_{MAX}$) | | | ns |
| $t_{CLCH}$ | Serial Clock Rise Time (Slew Rate) | 0.1 | | | V/ns |
| $t_{CHCL}$ | Serial Clock Fall Time (Slew Rate) | 0.1 | | | V/ns |
| $t_{SLCH}$ | CS# Active Setup Time | 3 | | | ns |
| $t_{CHSH}$ $t_{CLSH}$ | CS# Active Hold Time | 3 | | | ns |
| $t_{SHCH}$ | CS# Not Active Setup Time | 3 | | | ns |
| $t_{CHSL}$ | CS# Not Active Hold Time | 3 | | | ns |
| $t_{SHSL}$ | CS# High Time (Read/Write) | 20 | | | ns |
| $t_{SHQZ}$ | Output Disable Time | | | 6 | ns |
| $t_{CLQX}$ $t_{CHQX}$ | Output Hold Time | 1.2 | | | ns |
| $t_{DVCH}$ $t_{DVCL}$ | Data In Setup Time | 2 | | | ns |
| $t_{CHDX}$ $t_{CLDX}$ | Data In Hold Time | 2 | | | ns |
| $t_{HLCH}$ | HOLD# Low Setup Time (Relative To Clock) | 5 | | | ns |
| $t_{HHCH}$ | HOLD# High Setup Time (Relative To Clock) | 5 | | | ns |
| $t_{CHHH}$ | HOLD# Low Hold Time (Relative To Clock) | 5 | | | ns |
| $t_{CHHL}$ | HOLD# High Hold Time (Relative To Clock) | 5 | | | ns |
| $t_{HLQZ}$ | HOLD# Low To High-Z Output | | | 6 | ns |
| $t_{HHQX}$ | HOLD# High To Low-Z Output | | | 6 | ns |
| $t_{CLQV}$ | Clock Low To Output Valid (CL = 30pF) | | | 7 | ns |
| $t_{CHQV}$ | Clock Low To Output Valid (CL = 15pF) | | | 6 | ns |
| $t_{WHSL}$ | Write Protect Setup Time Before CS# Low | 20 | | | ns |
| $t_{SHWL}$ | Write Protect Hold Time After CS# High | 100 | | | ns |
| $t_{DP}$ | CS# High To Deep Power-Down Mode | | | 3 | μs |
| $t_{RES1}$ | CS# High To Standby Mode Without Electronic Signature Read | | | 20 | μs |
| $t_{RES2}$ | CS# High To Standby Mode With Electronic Signature Read | | | 20 | μs |

| | | | | | |
|---|---|---|---|---|---|
| $t_{SUS}$ | CS# High To Next Command After Suspend | | | 20 | μs |
| $t_{RS}$(3) | Latency Between Resume And Next Suspend | 100 | | | μs |
| $t_{RST}$ | CS# High To Next Command After Reset (Except From Erase) | | | 30 | μs |
| $t_{RST_E}$ | CS# High To Next Command After Reset (From Erase) | | | 12 | ms |
| $t_{CSL}$ | CS# Low Time | 500 | | | ns |
| $t_{CSH}$ | CS# High Time | 500 | | | ns |
| $t_{SISH}$ | SI# In Setup Time (Relative To CS#) | 5 | | | ns |
| $t_{SIHH}$ | SI# In Hold Time (Relative To CS#) | 5 | | | ns |
| $t_{RESET}$ | Internal Reset Time for JEDEC Reset Signaling | | | 100 | ms |
| $t_W$ | Write Status Register Cycle Time | | 2 | 25 | ms |
| $t_{BP}$ | Byte Program Time | | 30 | 140 | μs |
| $t_{PP}$ | Page Programming Time | | 0.18(4) | 3 | ms |
| $t_{SE}$ | Sector Erase Time | | 40(4) | 500 | ms |
| $t_{BE1}$ | Block Erase Time (32K Bytes) | | 0.1(4) | 1.2 | s |
| $t_{BE2}$ | Block Erase Time (64K Bytes) | | 0.16(4) | 3 | s |
| $t_{CE}$ | Chip Erase Time (GD25LQ64H) | | 10(4) | 90 | s |

Note:

1. Typical value at $T_A$ = 25℃; Maximum value at $T_A$ = 125℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Minimum timing must be observed before issuing the next suspend command, and a period equal to or longer than the minimum timing is required in order for the program or erase operation to make progress, but the operation time may exceed the maximum value.
4. Please contact GigaDevice for details regarding the faster page program / erase.

**Figure 77. Serial Input Timing (STR)**

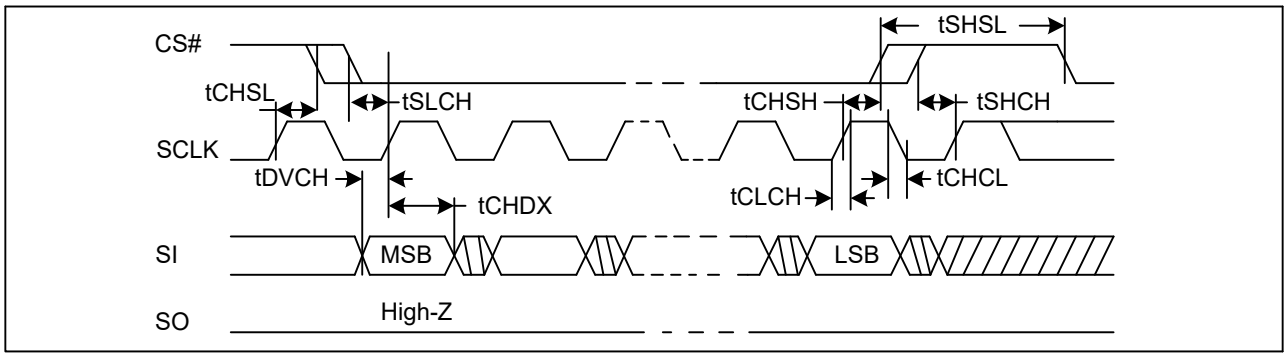


**Figure 78. Serial Output Timing (STR)**

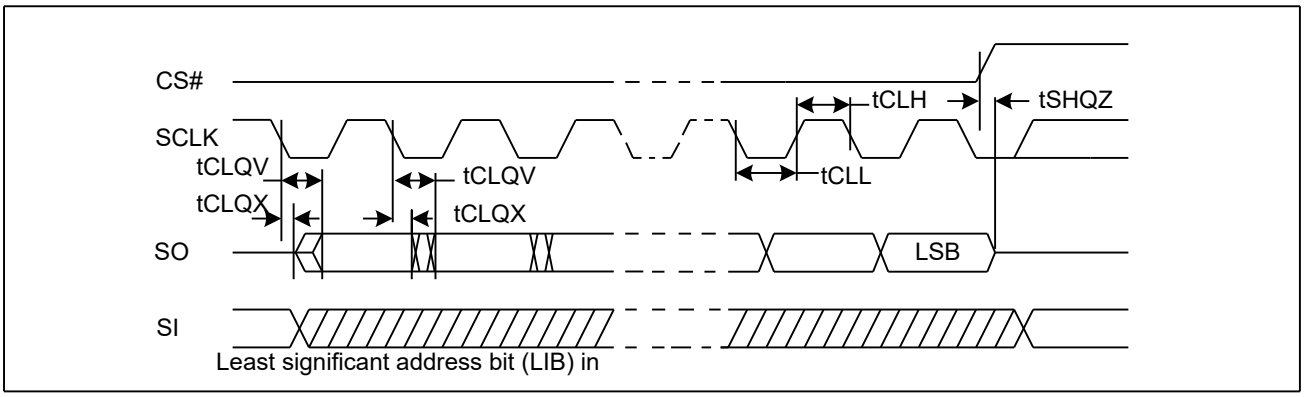



**Figure 79. Serial Input Timing (DTR)**

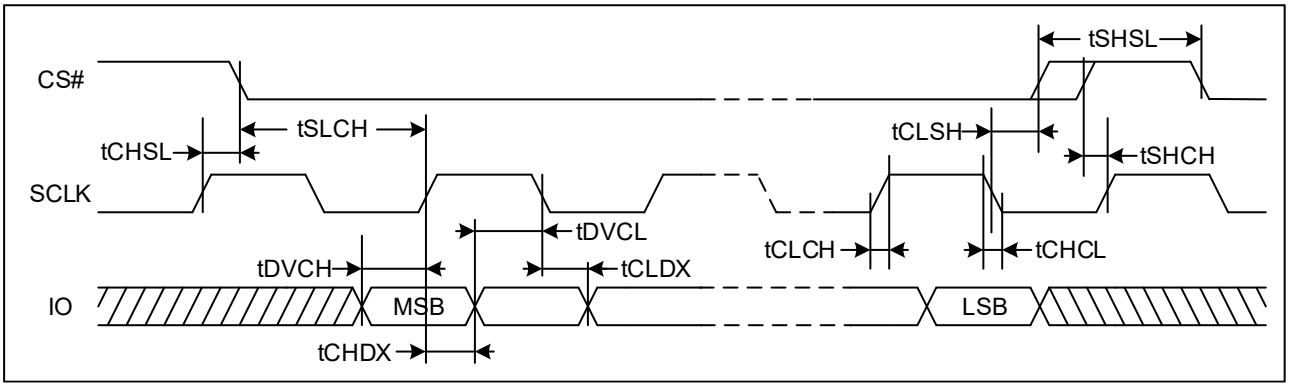



**Figure 80. Serial Output Timing (DTR)**

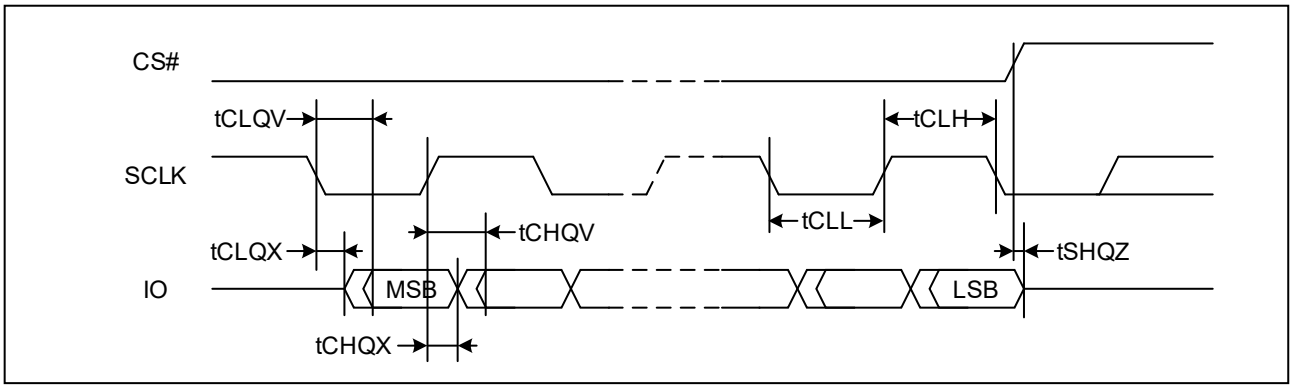



**Figure 81. Resume to Suspend Timing Diagram**

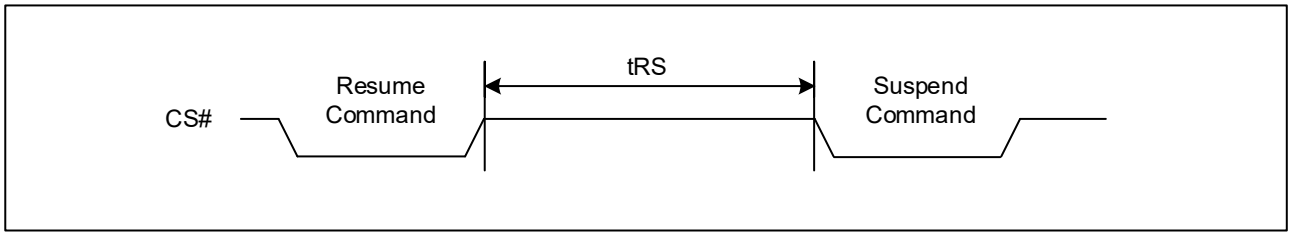


**Figure 82. HOLD# Timing**

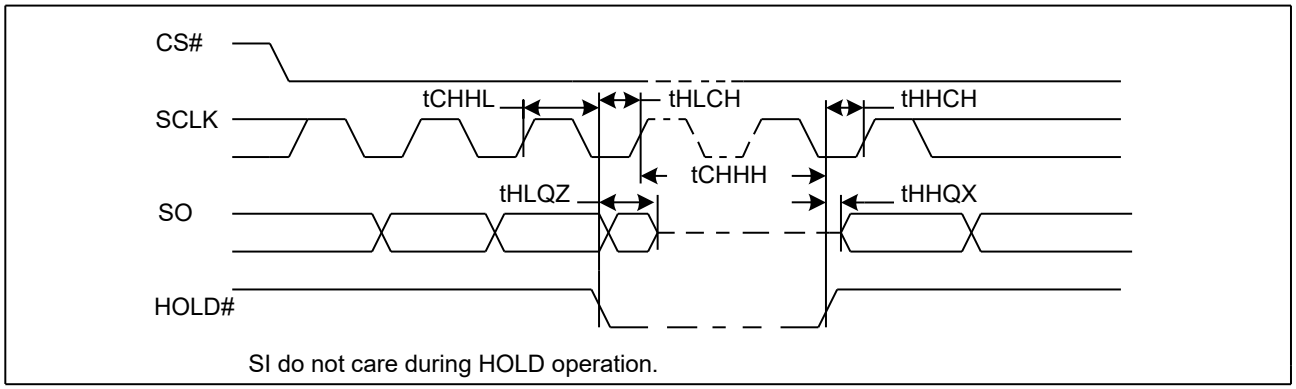



**Figure 83. WP# Timing**

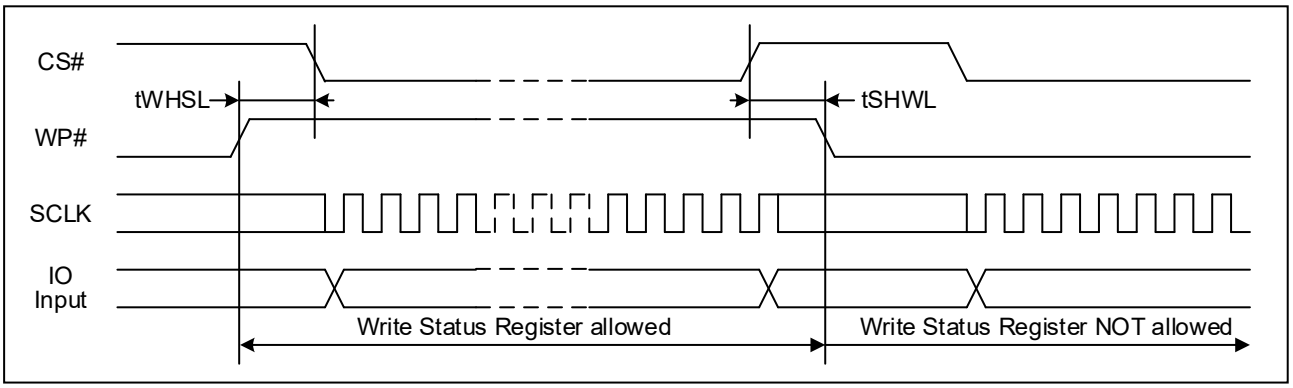



**Figure 84. RESET# Timing**

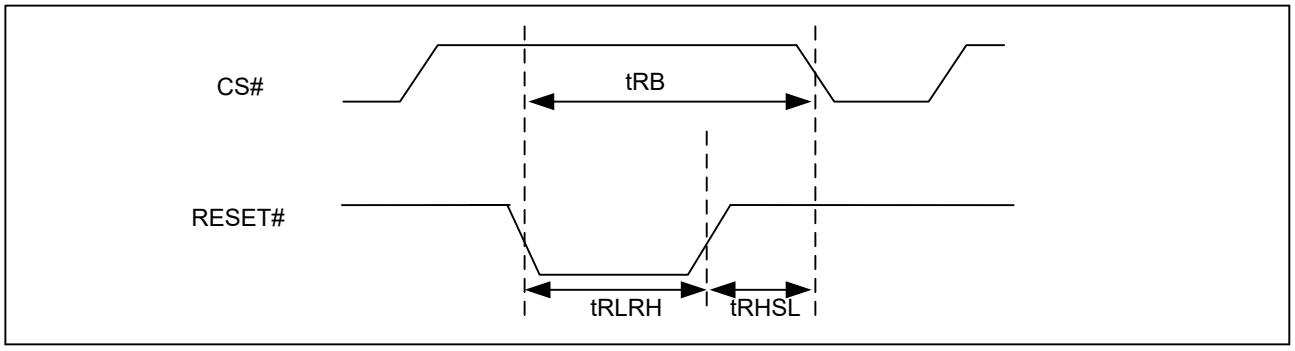


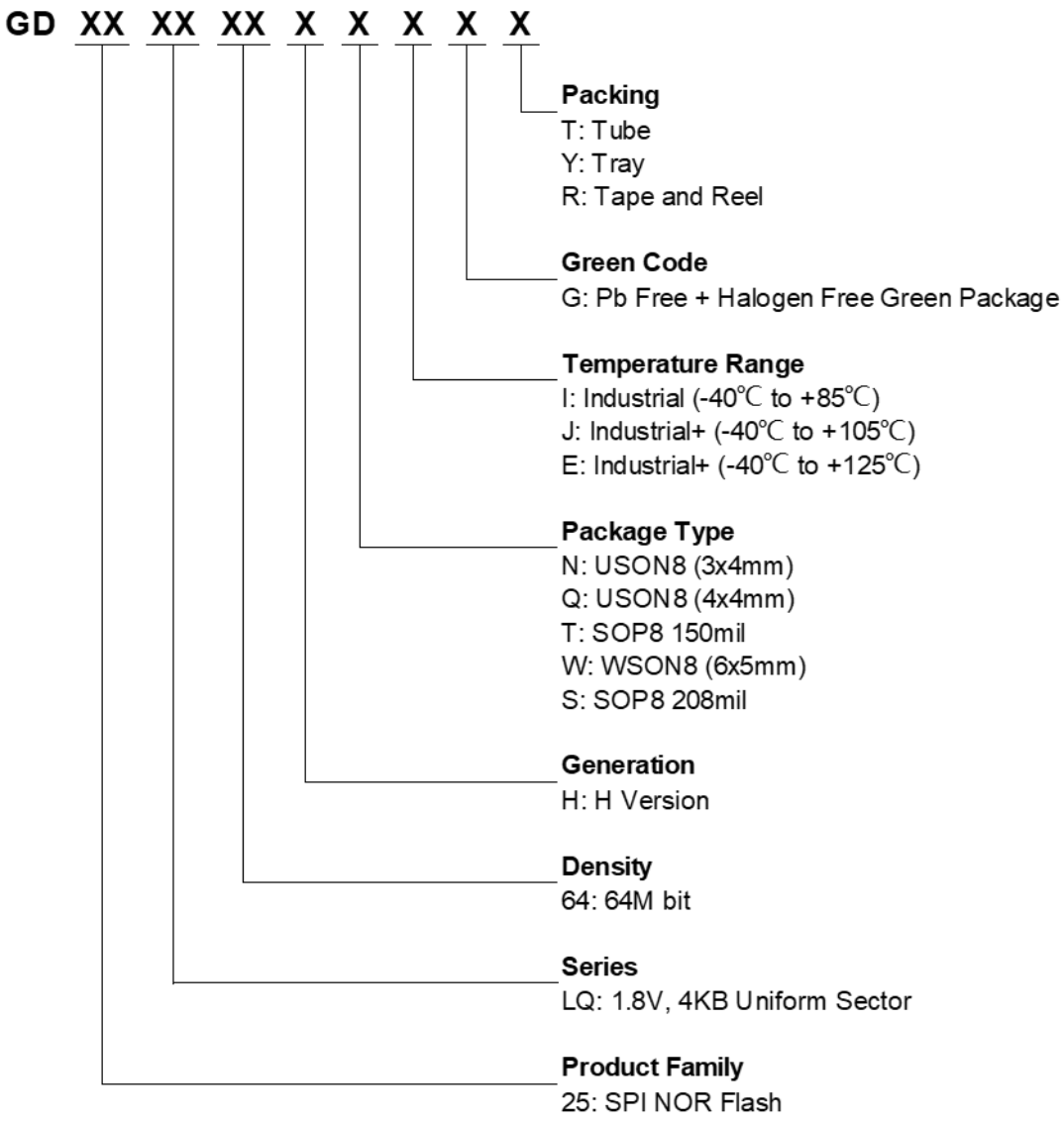

**Table 12. Reset Timing**

| Symbol | Parameter | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|
| tRLRH | Reset Pulse Width | 1 | | | μs |
| tRHSL | Reset Hold time before next Operation | 50 | | | ns |
| tRB | Reset Recovery Time | | | 12 | ms |

Note:

1. The device need tRB (max) at most to get ready for all commands after RESET# low.

# 9 ORDERING INFORMATION



## 9.1 Valid Part Numbers

**Please contact GigaDevice regional sales for the latest product selection and available form factors.**

**Temperature Range I: Industrial (-40℃ to +85℃)**

| Product Number | Density | Package Type | Packing Options |
|---|---|---|---|
| **GD25LQ64HNIG** | 64Mbit | USON8 (3x4mm) | R |
| GD25LQ64HQIG | 64Mbit | USON8 (4x4mm) | R |
| GD25LQ64HTIG | 64Mbit | SOP8 150mil | T/Y/R |
| **GD25LQ64HWIG** | 64Mbit | WSON8 (6x5mm) | Y/R |
| **GD25LQ64HSIG** | 64Mbit | SOP8 208mil | T/Y/R |

**Temperature Range J: Industrial+ (-40℃ to +105℃)**

| Product Number | Density | Package Type | Packing Options |
|---|---|---|---|
| GD25LQ64HNJG | 64Mbit | USON8 (3x4mm) | R |
| GD25LQ64HQJG | 64Mbit | USON8 (4x4mm) | R |
| GD25LQ64HTJG | 64Mbit | SOP8 150mil | T/Y/R |
| GD25LQ64HWJG | 64Mbit | WSON8 (6x5mm) | Y/R |
| GD25LQ64HSJG | 64Mbit | SOP8 208mil | T/Y/R |

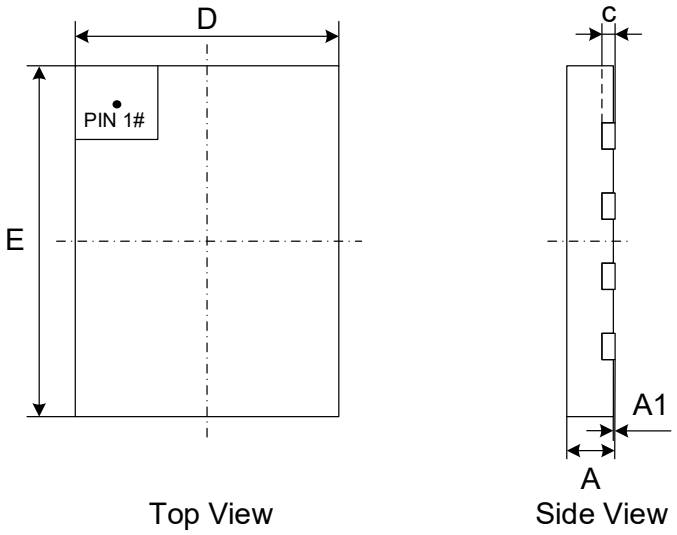
**Temperature Range E: Industrial+ (-40℃ to +125℃)**

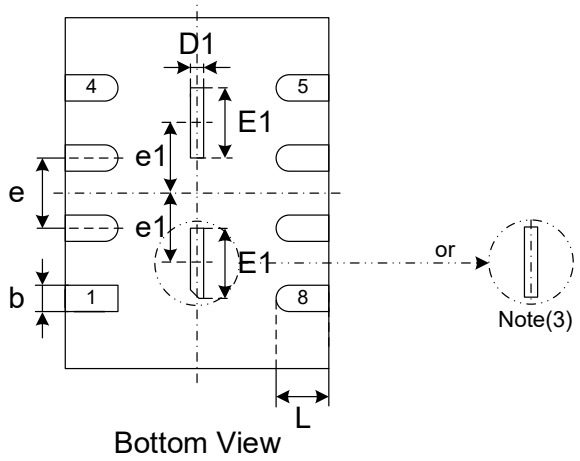
| Product Number | Density | Package Type | Packing Options |
|---|---|---|---|
| GD25LQ64HSEG | 64Mbit | SOP8 208mil | T/Y/R |

Note:
Bolded part numbers are the preferred general-purpose options for broad design-in.

# 10 PACKAGE INFORMATION

## 10.1 Package USON8 (3x4mm)



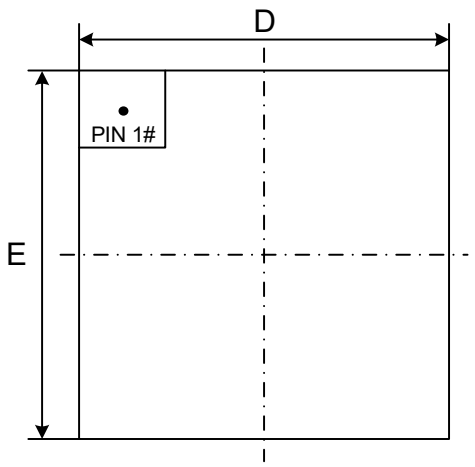

**Dimensions**

| Symbol / Unit | | A | A1 | c | b | D | D1 | E | E1 | e | e1 | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min | 0.50 | 0.00 | 0.10 | 0.25 | 2.90 | 0.10 | 3.90 | 0.70 | 0.80 BSC | 0.80 BSC | 0.50 |
| | Nom | 0.55 | 0.02 | 0.15 | 0.30 | 3.00 | 0.20 | 4.00 | 0.80 | | | 0.60 |
| | Max | 0.60 | 0.05 | 0.20 | 0.35 | 3.10 | 0.30 | 4.10 | 0.90 | | | 0.70 |

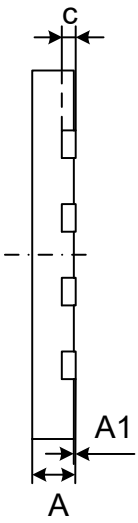
Note:

1. The exposed metal pad area on the bottom of the package is not connected to any internal signal. It is OK to connect it to the system ground (GND) or leave it floating.
2. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
3. The lead shape may be of little difference according to different package factories. These lead shapes are compatible with each other.

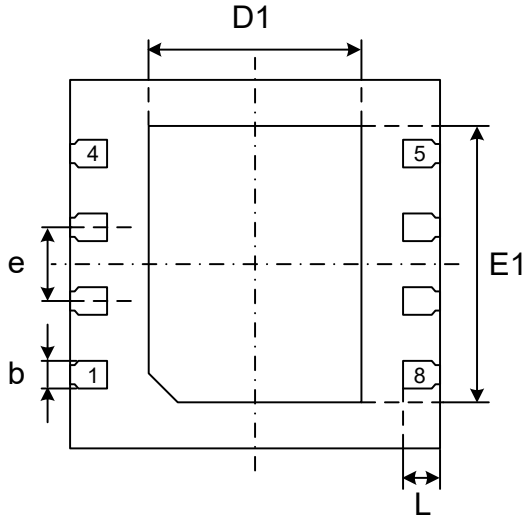
## 10.2 Package USON8 (4x4mm)




Top View




Side View




Bottom View

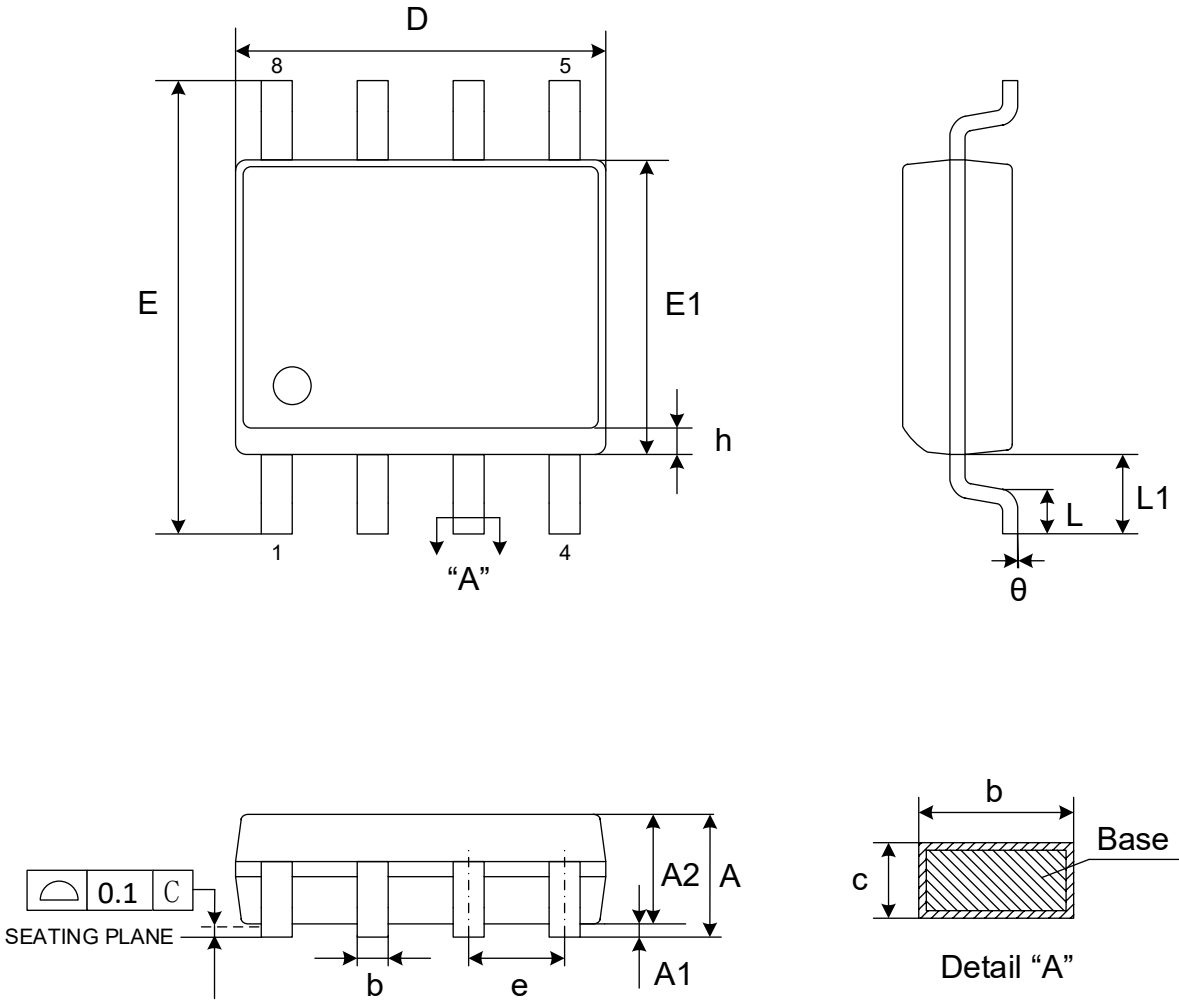
**Dimensions**

| Symbol / Unit | | A | A1 | c | b | D | D1 | E | E1 | e | L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min | 0.40 | 0.00 | 0.10 | 0.25 | 3.90 | 2.20 | 3.90 | 2.90 | 0.80 | 0.35 |
| | Nom | 0.45 | 0.02 | 0.15 | 0.30 | 4.00 | 2.30 | 4.00 | 3.00 | | 0.40 |
| | Max | 0.50 | 0.05 | 0.20 | 0.35 | 4.10 | 2.40 | 4.10 | 3.10 | | 0.45 |

Note:

1. The exposed metal pad area on the bottom of the package is not connected to any internal signal. It is OK to connect it to the system ground (GND) or leave it floating.
2. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
3. The lead shape may be of little difference according to different package factories. These lead shapes are compatible with each other

## 10.3 Package SOP8 150MIL



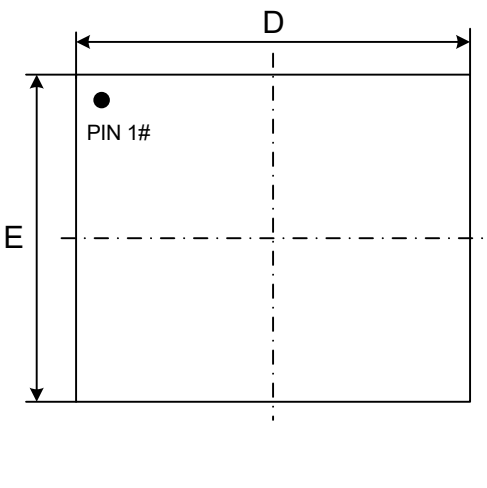

**Dimensions**

| Symbol / Unit | | A | A1 | A2 | b | c | D | E | E1 | e | L | L1 | h | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min | - | 0.10 | 1.25 | 0.31 | 0.10 | 4.80 | 5.80 | 3.80 | 1.27 | 0.40 | 1.04 | 0.25 | 0° |
| | Nom | - | 0.15 | 1.45 | 0.41 | 0.20 | 4.90 | 6.00 | 3.90 | | - | | - | - |
| | Max | 1.75 | 0.25 | 1.55 | 0.51 | 0.25 | 5.00 | 6.20 | 4.00 | | 0.90 | | 0.50 | 8° |

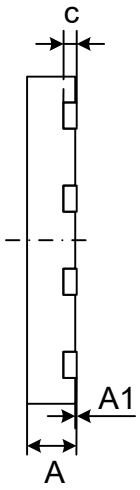
Note:

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per end.
2. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per end.

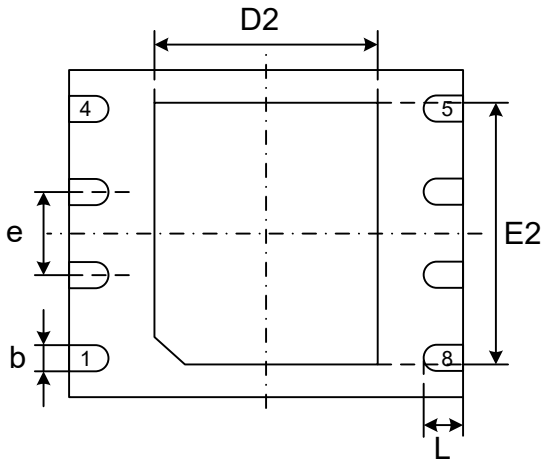
## 10.4 Package WSON8 (6x5mm)




Top View




Side View




Bottom View

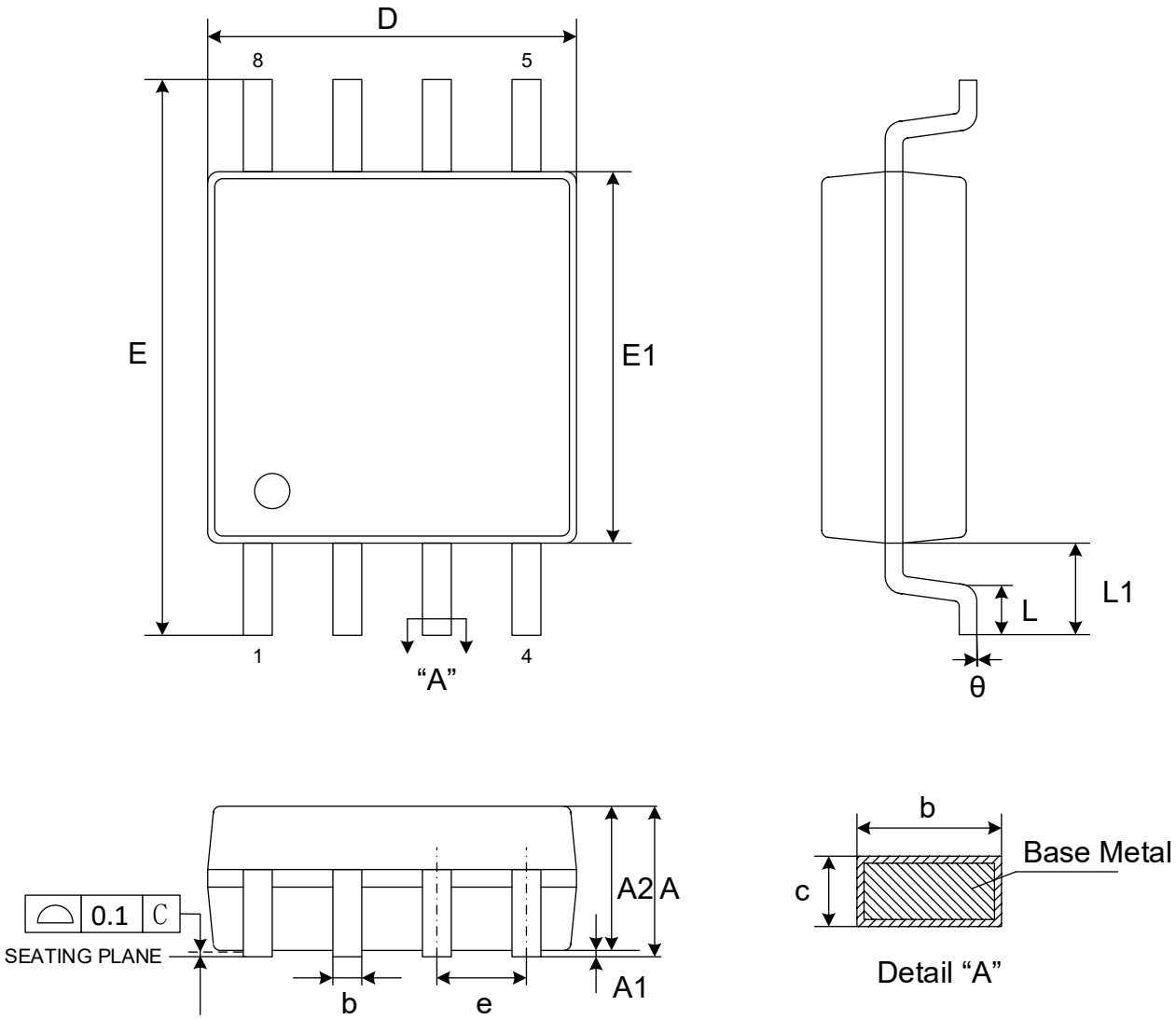
**Dimensions**

| Symbol / Unit | | A | A1 | c | b | D | D2 | E | E2 | e | L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min | 0.70 | 0.00 | 0.180 | 0.35 | 5.90 | 3.30 | 4.90 | 3.90 | 1.27 | 0.50 |
| | Nom | 0.75 | 0.02 | 0.203 | 0.40 | 6.00 | 3.40 | 5.00 | 4.00 | | 0.60 |
| | Max | 0.80 | 0.05 | 0.250 | 0.50 | 6.10 | 3.50 | 5.10 | 4.10 | | 0.75 |

Note:

1. The exposed metal pad area on the bottom of the package is not connected to any internal signal. It is OK to connect it to the system ground (GND) or leave it floating.
2. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
3. The lead shape may be of little difference according to different package lead frames. These lead shapes are compatible with each other.

## 10.5 Package SOP8 208MIL




**Dimensions**

| Symbol / Unit | | A | A1 | A2 | b | c | D | E | E1 | e | L | L1 | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min | - | 0.05 | 1.70 | 0.31 | 0.15 | 5.13 | 7.70 | 5.18 | 1.27 | 0.50 | 1.31 | 0° |
| | Nom | - | 0.15 | 1.80 | 0.41 | 0.20 | 5.23 | 7.90 | 5.28 | | - | | - |
| | Max | 2.16 | 0.25 | 1.90 | 0.51 | 0.25 | 5.33 | 8.10 | 5.38 | | 0.85 | | 8° |

Note:

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per end.
2. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per end.

# 11 REVISION HISTORY

| Version No | Description | Page | Date |
|---|---|---|---|
| 1.0 | Initial release | All | 2026-3-4 |

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