

HCPL-2530, HCPL-2531, HCPL-4534 HCPL-0530, HCPL-0531, HCPL-0534 Dual-Channel High-Speed Optocouplers

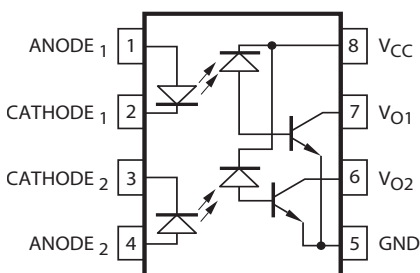
Description

These dual-channel optocouplers contain a pair of light-emitting diodes and integrated photodetectors with electrical insulation between the input and the output. A separate connection for the photodiode bias and the output transistor collectors increases the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

These dual-channel optocouplers are available in an 8-pin DIP and in an industry-standard SO-8 package. The following is a cross reference table listing the 8-pin DIP part number and the electrically equivalent SO-8 part number.

8-Pin DIP	SO-8 Package
HCPL-2530	HCPL-0530
HCPL-2531	HCPL-0531
HCPL-4534	HCPL-0534

Functional Diagram



TRUTH TABLE
(POSITIVE LOGIC)

LED	V _O
ON	LOW
OFF	HIGH

A 0.1-μF bypass capacitor between pins 5 and 8 is recommended.

Features

- 15-kV/μs minimum common mode transient immunity at V_{CM} = 1500V (HCPL-4534/0534)
- TTL compatible
- Available in 8-pin DIP, SO-8, and 8-pin DIP gull-wing surface-mount (Option 020) packages
- High-density packaging
- 3-MHz bandwidth
- Open collector outputs
- Safety approval:
 - UL recognized – 3750 V_{RMS} for 1 minute (5000 V_{RMS} for 1 minute for Option 020) per UL1577
 - CSA Approved
 - IEC/EN/DIN EN 60747-5-5
 - V_{IORM} = 630 V_{peak} for HCPL-2530/2531/4534 Option 060
 - V_{IORM} = 567 V_{peak} for HCPL-0530/0531/0534 Option 060
- Single-channel version available (HCPL-4502/HCPL-4503/HCPL-0452/HCPL-0453)
- MIL-PRF-38534 hermetic version available (HCPL-55xx, HCPL-65xx, 4N55)

Applications

- Line receivers – High common mode transient immunity (>1000 V/μs) and low input-output capacitance (0.6 pF)
- High-speed logic ground isolation – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL
- Replace pulse transformers – Save board space and weight
- Analog signal ground isolation – Integrated photon detector provides improved linearity over phototransistor type
- Polarity sensing
- Isolated analog amplifier – Dual-channel packaging enhances thermal tracking

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage and degradation that might be induced by electrostatic discharge (ESD). The components featured in this data sheet are not recommended to be used in military or aerospace applications or environments.

The SO-8 does not require through holes in a PCB. This package occupies approximately one-third the footprint area of the standard dual-inline package. The lead profile is designed to be compatible with standard surface-mount processes.

The HCPL-2530/0530 is for use in TTL/CMOS, TTL/LSTTL, or wide-bandwidth analog applications. The current transfer ratio (CTR) for the HCPL-2530/0530 is 7% minimum at $I_F = 16$ mA.

The HCPL-2531/0531 is designed for high-speed TTL/TTL applications. A standard 16-mA TTL sink current through the input LED provides enough output current for one TTL load and a 5.6-k Ω pull-up resistor. The CTR of the HCPL-2531/0531 is 19% minimum at $I_F = 16$ mA.

The HCPL-4534/0534 is an HCPL-2531/0531 with an increased common mode transient immunity of 15,000 V/ μ s minimum at $V_{CM} = 1500$ V guaranteed.

Selection Guide

Minimum CMR		Current Transfer Ratio (%)	8-Pin DIP (300 Mil)		Small-Outline SO-8		Wide Body (400 Mil)	Hermetic
dV/dt (V/ μ s)	V _{CM} (V)		Dual-Channel Package	Single-Channel Package ^a	Dual-Channel Package	Single-Channel Package ^a	Single-Channel Package ^a	Single- and Dual-Channel Packages ^a
1,000	10	7	HCPL-2530	6N135	HCPL-0530	HCPL-0500	HCNW135	—
		19	HCPL-2531	6N136 HCPL-4502	HCPL-0531	HCPL-0501 HCPL-0452	HCNW136 HCNW4502	—
15,000	1500	19	HCPL-4534	HCPL-4503	HCPL-0534	HCPL-0453	HCNW4503	—
1,000	10	9	—	—	—	—	—	HCPL-55XX HCPL-65XX 4N55

a. Technical data for these products is in separate Broadcom publications.

Ordering Information

The HCPL-2530, HCPL-2531, HCPL-4534, HCPL-0530, HCPL-0531, and HCPL-0534 are UL recognized with 3750 V_{RMS} for 1 minute per UL1577, and they are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 V _{RMS} / 1-Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant	Not RoHS Compliant							
HCPL-2530 HCPL-2531 HCPL-4534	-000E	No option	300 mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	#520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-360E	#360		X	X			X	50 per tube
	-560E	#560		X	X	X		X	1000 per reel
HCPL-0530 HCPL-0531 HCPL-0534	-000E	No option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel

To form an order entry, choose a part number from the Part Number column and combine it with the desired option from the Option column.

Example 1:

Use HCPL-2530-560E to order the product with a 300-mil DIP gull-wing surface-mount package in tape and reel packaging with IEC/EN/DIN EN 60747-5-5 safety approval and RoHS compliance.

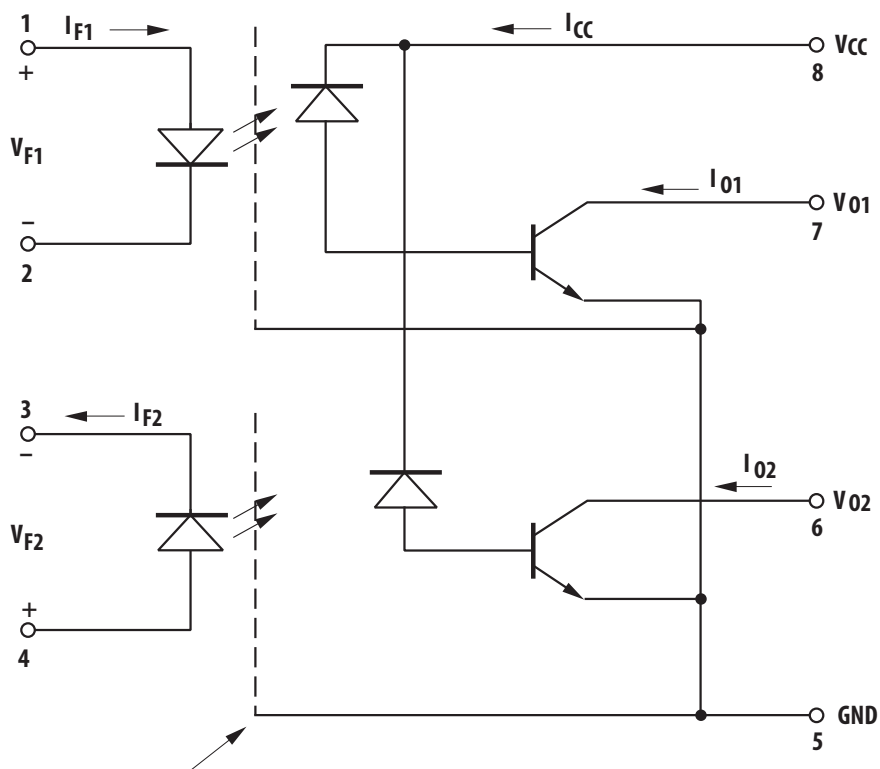
Example 2:

Use HCPL-2530 to order the product with a 300-mil DIP package in tube packaging and with no RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

NOTE: The notation '#XXX' is used for existing products, whereas products that launched since July 15, 2001 with the RoHS-compliant option use '-XXxE'.

Schematic



HCPL-4534/0534 SHIELD

USE OF A 0.1- μ F BYPASS CAPACITOR CONNECTED
 BETWEEN PINS 5 AND 8 IS RECOMMENDED.

Figure 1: 8-Pin DIP Package (HCPL-2530/2531/4534)

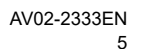
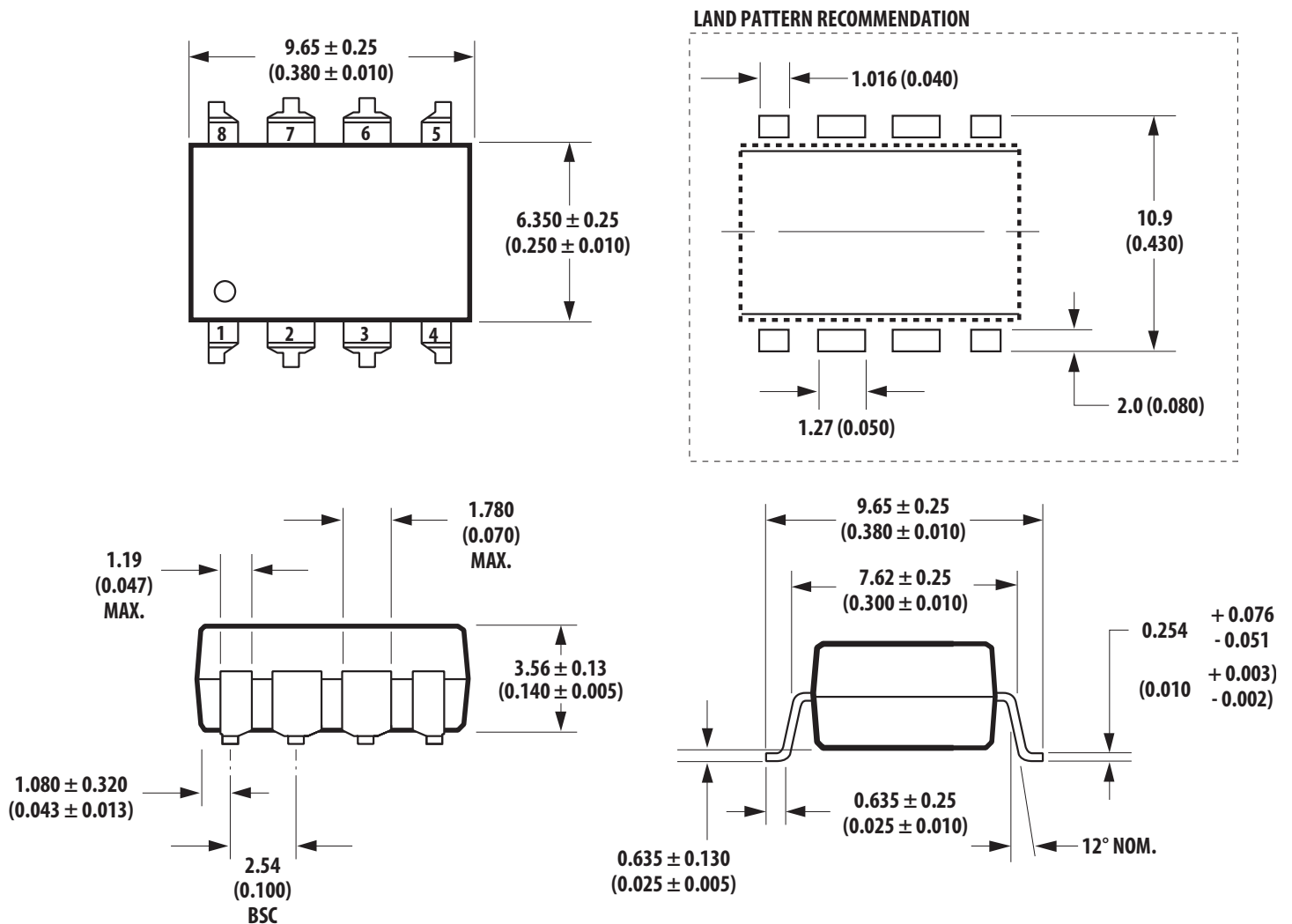


Figure 2: 8-Pin DIP Package with Gull-Wing Surface-Mount Option 300 (HCPL-2530/2531/4534)

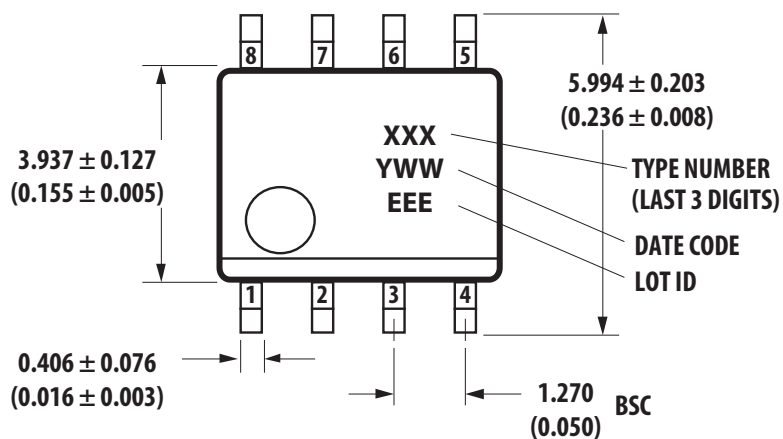


DIMENSIONS IN MILLIMETERS (INCHES).

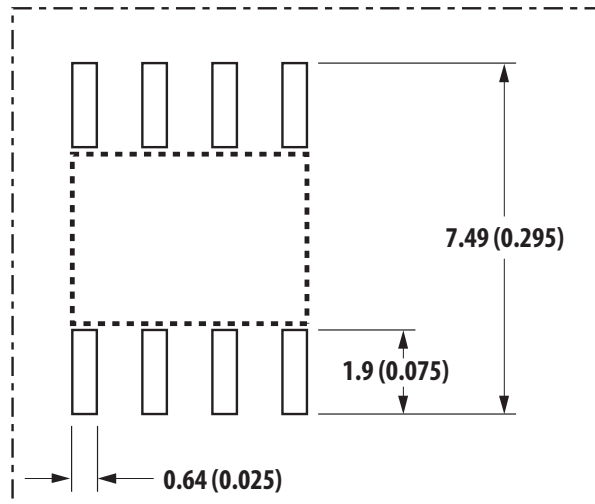
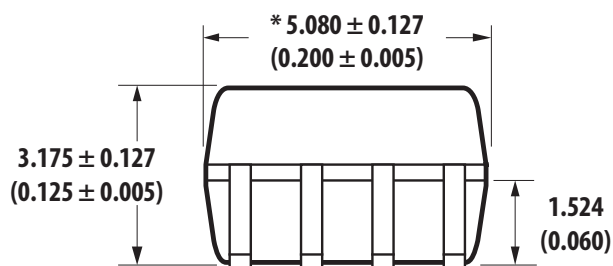
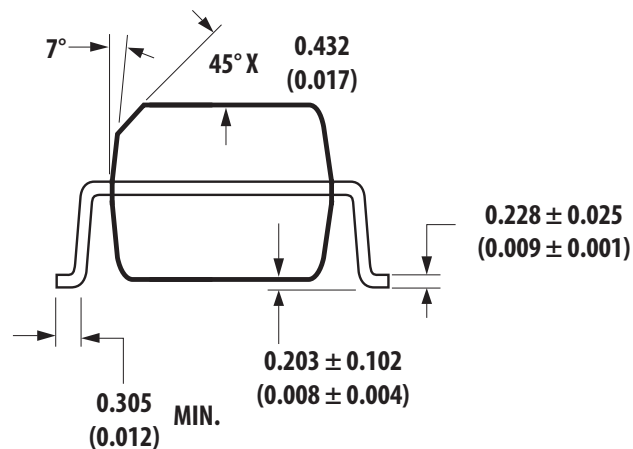
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Figure 3: Small Outline SO-8 Package (HCPL-0530/0531/0534)



LAND PATTERN RECOMMENDATION



* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
 5.207 ± 0.254 mm (0.205 ± 0.010 in)

DIMENSIONS IN MILLIMETERS (INCHES).
 LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Regulatory Information

The devices contained in this data sheet have been approved by the following organizations.

UL	Recognized under UL 1577, Component Recognition Program, File E55361.
CSA	Approved under CSA Component Acceptance Notice #5, File CA 88324.
IEC/EN/DIN	IEC/EN/DIN EN 60747-5-5 Approved under (Option 060 only).

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through the air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along the body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and the photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)	—	N/A	N/A	mm	Measured from input terminals to output terminals, along the internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/VDE 0303 Part 1.
Isolation Group	—	IIIa	IIIa	—	Material Group (DIN VDE 0110, 1/89, Table 1).

The Option 300 surface-mount classification is Class A in accordance with CECC 00802.

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060)

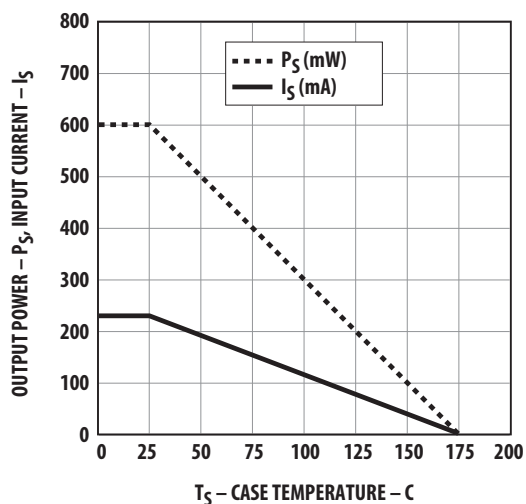
Description	Symbol	Characteristic HCPL-		
		2530/2531/4534	0530/0531/0534	Unit
Installation classification per DIN VDE 0110, Table 1 For rated mains voltage $\leq 150 V_{RMS}$ For rated mains voltage $\leq 300 V_{RMS}$ For rated mains voltage $\leq 600 V_{RMS}$	—	I – IV I – IV I – IV	I – IV I – IV I – III	—
Climatic Classification	—	0/70/21	0/70/21	—
Pollution Degree (DIN VDE 0110/39)	—	2	2	—
Maximum Working Insulation Voltage	V_{IORM}	630	567	V_{peak}
Input to Output Test Voltage, Method b ^a $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test $t_m = 1$ second, Partial discharge < 5 pC	V_{PR}	1181	1063	V_{peak}
Input to Output Test Voltage, Method a ^a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test $t_m = 10$ seconds, Partial discharge < 5 pC	V_{PR}	1008	907	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60$ seconds)	V_{IOTM}	8000	6000	V_{peak}
Safety-Limiting Values – Max. Values Allowed in the Event of a Failure.				
Case Temperature	T_S	175	150	$^{\circ}C$
Input Current ^b	I_S , INPUT	230	230	mA
Output Power ^b	P_S , OUTPUT	600	600	mW
Insulation Resistance at T_S , $V_{IO} = 500V$	R_S	$>10^9$	$>10^9$	Ω

a. Refer to the optocoupler section of the *Isolation and Control Components Designer's Catalog*, under the "Product Safety Regulations" section, IEC/EN/DIN EN 60747-5-5, for a detailed description of the Method a and Method b partial discharge test profiles.

b. See Figure 4 for the dependence of P_S and I_S on the ambient temperature.

NOTE: Isolation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in application.

Figure 4: Output Power/Input Current vs Case Temperature



Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units
Storage Temperature	T _S	—	–55	125	°C
Operating Temperature	T _A	—	–55	100	°C
Average Forward Input Current (Each Channel)	I _{F(AVG)}	—	—	25	mA
Peak Forward Input Current (Each Channel) (50% duty cycle, 1 ms pulse width)	I _{F(PEAK)}	—	—	50	mA
Peak Transient Input Current (Each Channel) (≤ 1 μs Pulse Width, 300 pps)	I _{F(TRANS)}	—	—	1	A
Reverse LED Input Voltage (Each Channel)	V _R	—	—	5	V
Input Power Dissipation (Each Channel)	P _{IN}	—	—	45	mW
Average Output Current (Each Channel)	I _{O(AVG)}	—	—	8	mA
Peak Output Current	I _{O(PEAK)}	—	—	16	mA
Supply Voltage (Pins 8–5)	V _{CC}	—	–0.5	30	V
Output Voltage (Pins 7–5, 6–5)	V _O	—	–0.5	20	V
Output Power Dissipation (Each Channel) ^a	P _O	—	—	35	mW
Lead Solder Temperature (Through-Hole Parts Only) 1.6 mm Below Seating Plane, 10 seconds	T _{LS}	8-Pin DIP	—	260	°C

a. Derate linearly above 90°C free-air temperature at a rate of 3.0 mW/°C for the SO-8 package.

Electrical Specifications (DC)

Over the recommended temperature ($T_A = 0^\circ\text{C}$ to 70°C) unless otherwise specified.¹

Parameter	Symbol	Device	Min.	Typ. ^a	Max.	Units	Test Conditions		Fig.	Note	
Current Transfer Ratio	CTR	HCPL-2530/0530	7	18	50	%	T _A = 25°C		I _F = 16 mA, V _{CC} = 4.5 V V _O = 0.5 V	5, 6, 8	b, c
			5								
		HCPL-2531/0531 HCPL-4534/0534	19	24	50	%	T _A = 25°C				
			15								
Logic Low Output Voltage	V _{OL}	HCPL-2530/0530	—	0.1	0.5	V	T _A = 25°C I _O = 1.1 mA		I _F = 16 mA V _{CC} = 4.5 V	5	b
					0.5		I _O = 0.8 mA				
		HCPL-2531/0531 HCPL-4534/0534	—	0.1	0.5	V	T _A = 25°C I _O = 3.0 mA				
					0.5		I _O = 2.4 mA				
Logic High Output Current	I _{OH}	—	—	0.003	0.5	μA	T _A = 25°C V _{CC} = V _O = 5.5 V I _F = 0 mA		I _F = 0 mA	10	b
					50		T _A = 25°C V _{CC} = V _O = 15 V I _F = 0 mA				
Logic Low Supply Current	I _{CCL}	—	—	100	400	μA	I _F = 16 mA V _O = Open V _{CC} = 15 V		—	—	—
Logic High Supply Current	I _{CCH}	—	—	0.05	4	μA	I _F = 0 mA V _O = Open V _{CC} = 15 V		—	—	—
Input Forward Voltage	V _F	—	—	1.5	1.7	V	T _A = 25°C		I _F = 16 mA	7	b
				—	1.8						
Input Reverse Breakdown Voltage	BV _R	—	5	—	—	V	I _R = 10 μA		—	—	b
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	—	—	−1.6	—	mV/°C	I _F = 16 mA		—	—	—
Input Capacitance	C _{IN}	—	—	60	—	pF	f = 1 MHz, V _F = 0 V		5	—	—

a. All typicals at $T_A = 25^\circ\text{C}$.

b. Each channel.

c. The current transfer ratio is defined as the ratio of the output collector current, I_O , to the forward LED input current, I_F , times 100%.

1. Use of a 0.1- μF bypass capacitor connected between pins 5 and 8 is recommended.

Switching Specifications (AC)

Over the recommended temperature ($T_A = 0^\circ\text{C}$ to 70°C), $V_{CC} = 5\text{V}$, $I_F = 16\text{ mA}$ unless otherwise specified.

Parameter	Symbol	Device HCPL-	Min.	Typ. ^a	Max.	Units	Test Conditions		Fig.	Note	
Propagation Delay Time to Logic Low at Output	t _{PHL}	2530/0530	—	0.2	1.5	μs	T _A = 25°C	R _L = 4.1 kΩ	9, 13, 15	b, c	
					2.0						
		2531/0531/ 4534/0534	—	0.2	0.8		T _A = 25°C	R _L = 1.9 kΩ			
					1.0						
Propagation Delay Time to Logic High at Output	t _{PLH}	2530/0530	—	1.3	1.5	μs	T _A = 25°C	R _L = 4.1 kΩ	9, 13, 15	b, c	
					2.0						
		2531/0531/ 4534/0534	—	0.6	0.8		T _A = 25°C	R _L = 1.9 kΩ			
					1.0						
Common Mode Transient Immunity at Logic High Level Output	CM _H	2530/0530	1	10	—	kV/μs	R _L = 4.1 kΩ	I _F = 0 mA T _A = 25°C V _{CM} = 10 V _{p-p}	14	b, c, d	
		2531/0531	1	10	—		R _L = 1.9 kΩ				
		4534/0534	15	30	—		R _L = 1.9 kΩ				
Common Mode Transient Immunity at Logic Low Level Output	CM _L	2530/0530	1	10	—	kV/μs	R _L = 4.1 kΩ	I _F = 0 mA T _A = 25°C V _{CM} = 10 V _{p-p}	14	b, c, d	
		2531/0531	1	10	—		R _L = 1.9 kΩ				
		4534/0534	15	30	—		R _L = 1.9 kΩ				
Bandwidth	BW	—	—	3	—	MHz	R _L = 100 kΩ		11, 12	—	

a. All typicals at $T_A = 25^\circ\text{C}$.

b. The 1.9-k Ω load represents one TTL unit load of 1.6 mA and the 5.6-k Ω pull-up resistor.

c. The 4.1-k Ω load represents one LSTTL unit load of 0.36 mA and the 6.1-k Ω pull-up resistor.

d. Common mode transient immunity in a logic high level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM} , to ensure that the output will remain in a logic high state (that is, $V_O > 2.0\text{V}$). Common mode transient immunity in a logic low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM} , to ensure that the output will remain in a logic low state (that is, $V_O < 0.8\text{V}$).

Package Characteristics

Parameter	Symbol	Device	Min.	Typ. ^a	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage ^b	V _{ISO}	HCPL-2530/2531/4534 Option 020	3750 5000	— —	— —	V _{RMS}	RH < 50% t = 1 minute	c, d c, e
Resistance (Input-Output)	R _{I-O}	—	—	10 ¹²	—	Ω	RH ≤ 45% V _{I-O} = 500 Vdc t = 5 seconds	c
Capacitance (Input-Output)	C _{I-O}	—	—	0.6	—	pF	f = 1 MHz T _A = 25°C	f
Input-Input Insulation Leakage Current	I _{I-I}	—	—	0.005	—	μA	RH ≤ 45% t = 5 seconds V _{I-I} = 500 Vdc	g
Resistance (Input-Input)	R _{I-I}	—	—	10 ¹¹	—	Ω	—	g
Capacitance (Input-Input)	C _{I-I}	HCPL-2530/2531/4534 HCPL-0530/0531/0534	— —	0.03 0.25	— —	pF	f = 1 MHz	g

- a. All typicals at T_A = 25°C.
- b. The input-output momentary withstand voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable), your equipment level safety specification, or Broadcom Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."
- c. The device is considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
- d. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥4500 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA).
- e. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥6000 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA).
- f. Measured between the LED anode and the cathode shorted together and pins 5 through 8 shorted together.
- g. Measured between pins 1 and 2 shorted together and pins 3 and 4 shorted together.

Figure 5: DC and Pulsed Transfer Characteristics

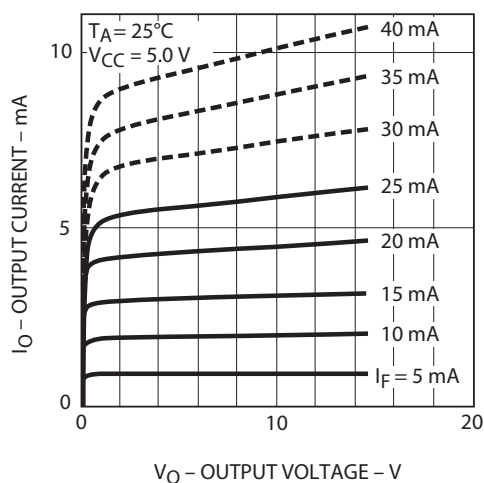


Figure 6: Current Transfer Ratio vs. Input Current

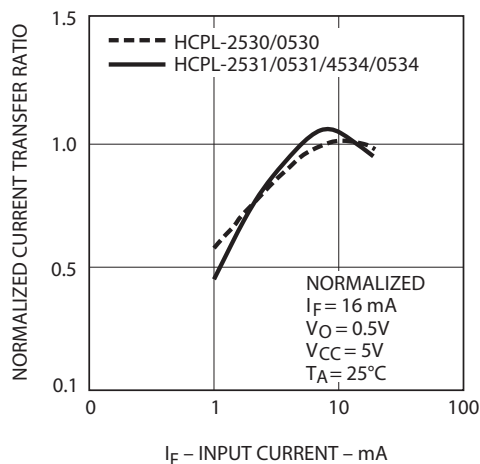


Figure 7: Input Current vs. Forward Voltage

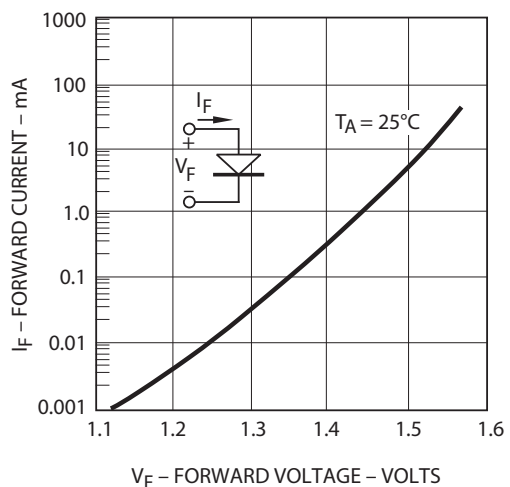


Figure 8: Current Transfer Ratio vs. Temperature

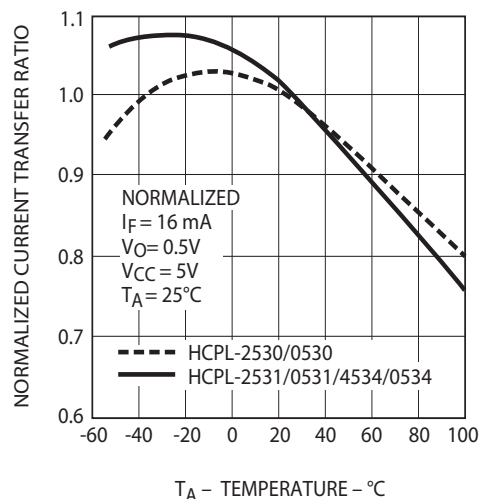


Figure 9: Propagation Delay vs. Temperature

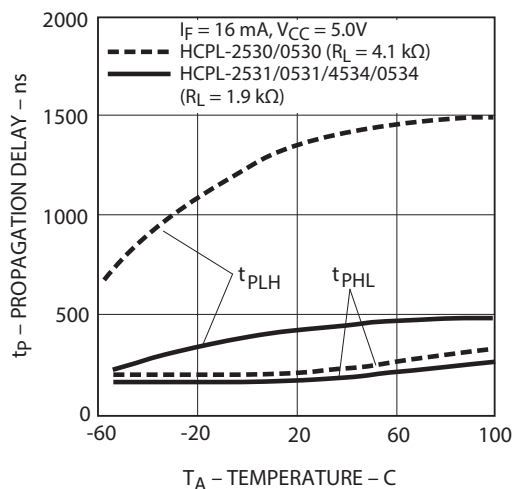


Figure 10: Logic High Output Current vs. Temperature

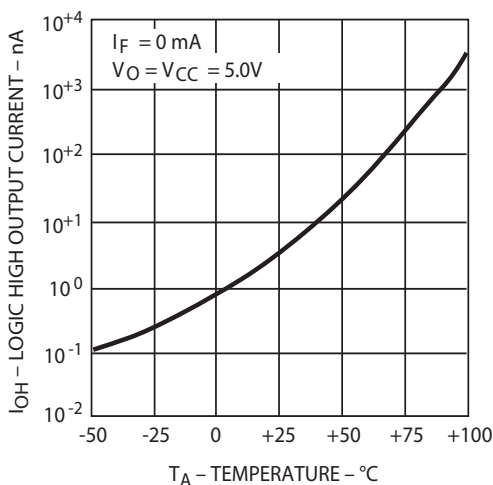


Figure 11: Small-Signal Current Transfer Ratio vs. Quiescent Input Current

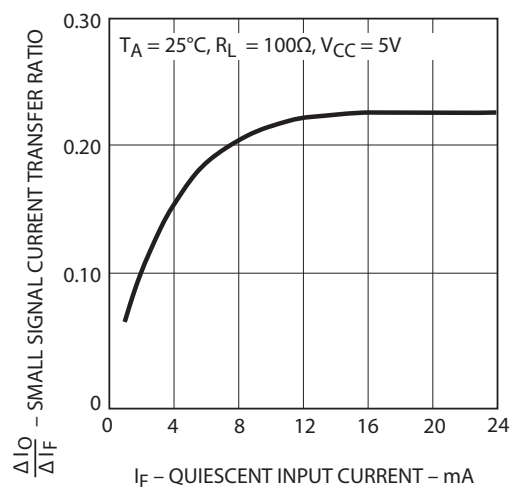


Figure 12: Frequency Response

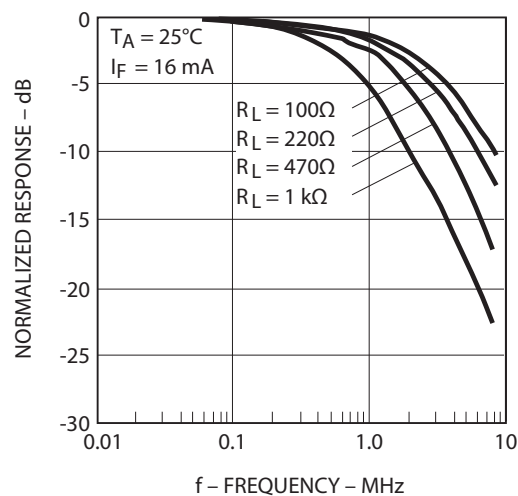
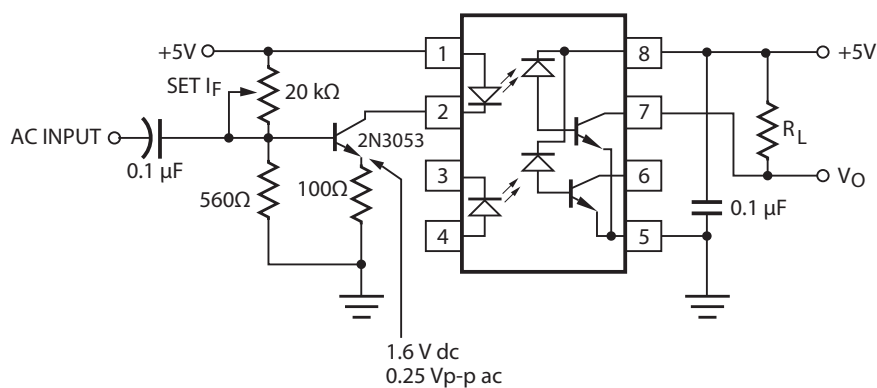
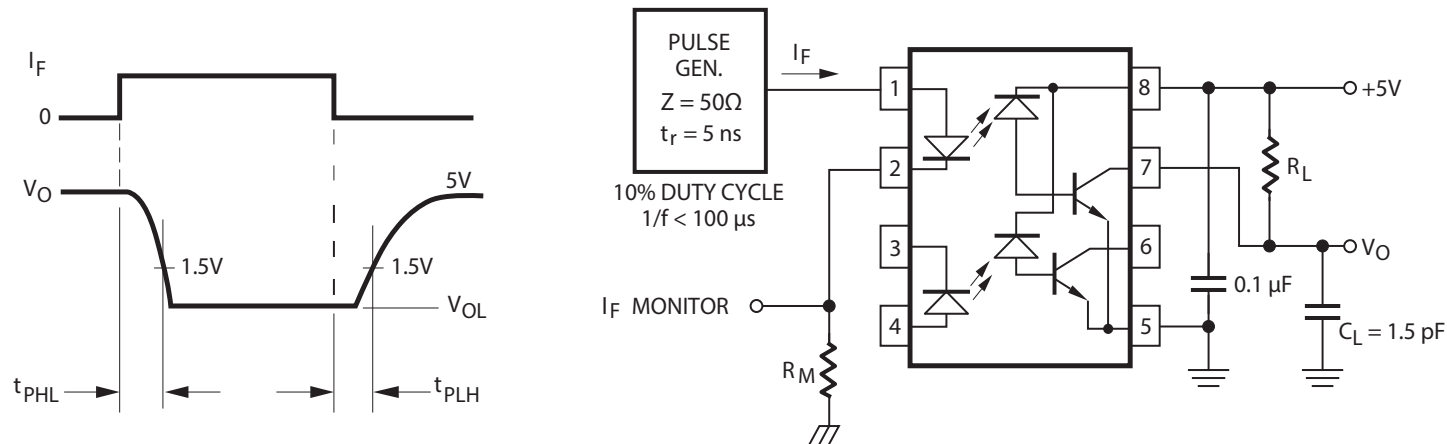


Figure 13: Switching Test Circuit



The figure consists of two parts. The top part is a schematic diagram of a 74VHC04 inverter circuit. The inverter is represented by a central block with pins 1, 2, 3, 4, 5, 6, 7, and 8. Pin 1 is connected to a variable input voltage V_{FF} through a switch that can be moved between positions A and B. Pin 2 is connected to a +5V supply. Pin 3 is connected to a +5V supply through a resistor R_L . Pin 4 is connected to a +5V supply. Pin 5 is connected to a +5V supply through a 0.1 μ F capacitor. Pin 6 is connected to a +5V supply. Pin 7 is connected to a +5V supply. Pin 8 is connected to a +5V supply. The output of the inverter is taken from pin 6, labeled V_O . A pulse generator is connected to the input of the inverter (pin 1) and the output (pin 6). The pulse generator is labeled V_{CM} and $PULSE GEN.$. The bottom part of the figure shows two timing diagrams. The first diagram is for the switch at position A, where $I_F = 0$ mA. It shows the output voltage V_O as a function of time. The input voltage V_{CM} is shown as a square wave. The output voltage V_O is shown as a square wave with a rise time t_r and a fall time t_f . The output voltage V_O is labeled V_{OL} when the input is high. The second diagram is for the switch at position B, where $I_F = 16$ mA. It shows the output voltage V_O as a function of time. The input voltage V_{CM} is shown as a square wave. The output voltage V_O is shown as a square wave with a rise time t_r and a fall time t_f . The output voltage V_O is labeled V_{OL} when the input is high.

The graph shows the propagation delay (t_p) in microseconds versus the load resistance (R_L) in kilohms for a 74123 monostable multivibrator. The supply voltage is $V_{CC} = 5.0V$ and the temperature is $T_A = 25^\circ C$. Two curves are plotted for different output current levels: $I_F = 10\text{ mA}$ (dashed line) and $I_F = 16\text{ mA}$ (solid line). The rising edge delay (t_{PLH}) increases with R_L , while the falling edge delay (t_{PHL}) decreases slightly with R_L .

R_L (k Ω)	t_{PLH} (μs) at $I_F = 10\text{ mA}$	t_{PLH} (μs) at $I_F = 16\text{ mA}$	t_{PHL} (μs) at $I_F = 10\text{ mA}$	t_{PHL} (μs) at $I_F = 16\text{ mA}$
1	-	0.10	0.32	0.24
2	0.10	0.60	0.28	0.20
3	0.70	1.00	0.25	0.18
4	1.00	1.30	0.23	0.17
5	1.20	1.50	0.22	0.16
6	1.35	1.65	0.22	0.16
7	1.50	1.80	0.22	0.16
8	1.65	1.95	0.22	0.16
9	1.80	2.10	0.22	0.16
10	2.00	2.30	0.22	0.16

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