

Multimode SCSI 15 Line Terminator

FEATURES

- Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination
- Meets SCSI-1, SCSI-2, Ultra2 (SPI-2 LVD SCSI), Ultra3, Ultra160 (SPI-3) and Ultra320 (SPI-4) Standards
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Thermal packaging for low junction temperature and better MTBF.

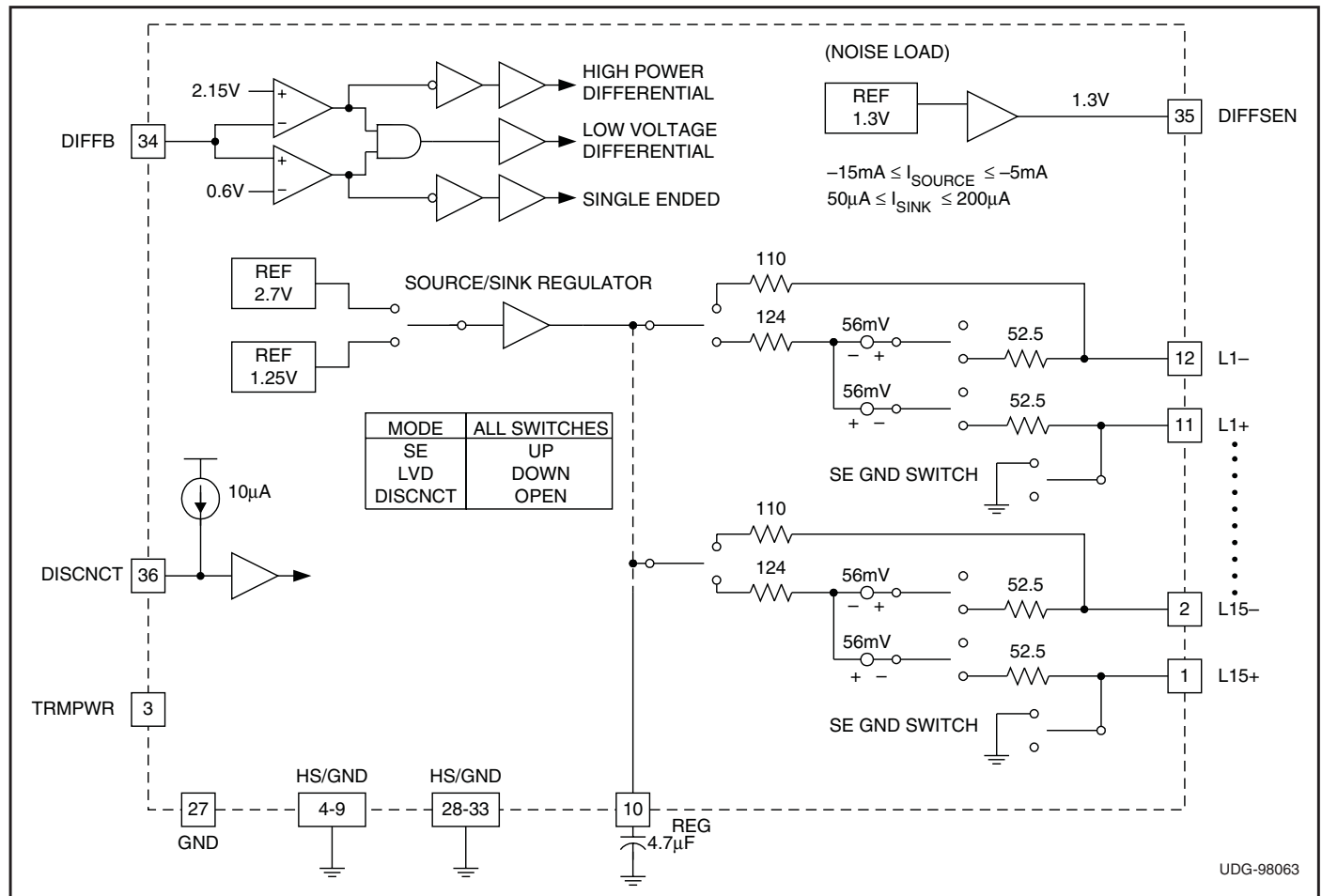
DESCRIPTION

The UCC5638 Multimode SCSI Terminator provides a smooth transition into the LVD SCSI Parallel Interface (SPI-2, SPI-3, SPI-4). It automatically senses the bus, via DIFFB, and switches the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5638 can not be used on a HVD, EIA485, differential SCSI bus. If the UCC5638 detects a HVD SCSI device, it switches to a high impedance state.

The Multimode terminator contains all functions required to terminate and auto detect and switch modes for SPI-2, SPI-3 and SPI-4 bus architectures. Single Ended and Differential impedances and currents are trimmed for maximum effectiveness. Fail Safe biasing is provided to insure signal integrity. Device/Bus type detection circuitry is integrated into the terminator to provide automatic switching of termination between single ended and LVD SCSI and a high impedance for HVD SCSI. The multimode function provides all the performance analog functions necessary to implement SPI-2 termination in a single monolithic device.

The UCC5638 is offered in a 48 pin LQFP package for a temperature range of 0°C to 70°C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

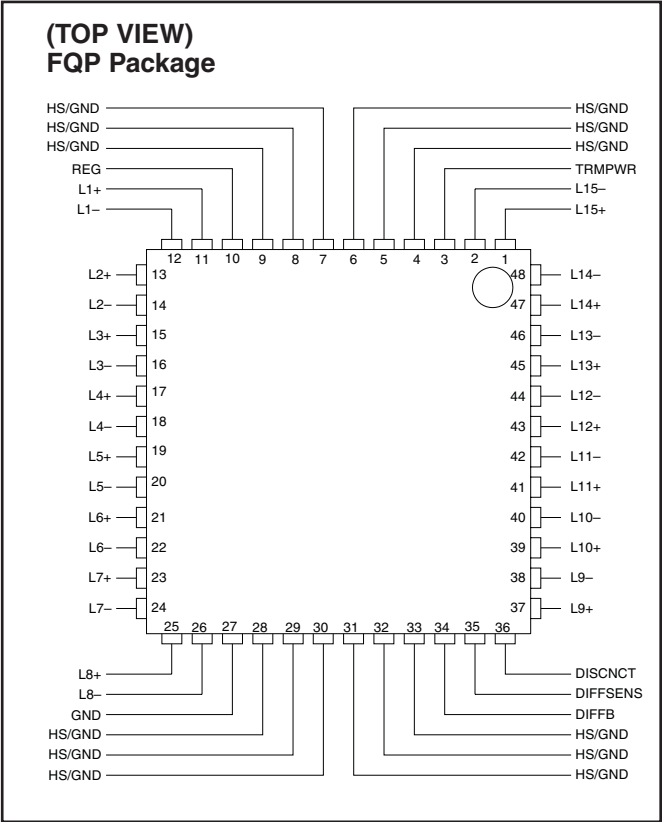
TRMPWR Voltage	+6V
Signal Line Voltage	0V to 5V
Package Dissipation	2W
Storage Temperature	–65°C to +150°C
Junction Temperature	–55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Recommended Operating Conditions	2.7V to 5.25V

Currents are positive into negative out of the specified terminal.
Note: Consult Packaging Section of Databook for thermal limitations and considerations of package.

RECOMMENDED OPERATING CONDITIONS

TRMPWR Voltage	2.7V to 5.25V
Temperature Ranges	0°C to +70°C

CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0^\circ\text{C}$ to 70°C , TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	LVD SCSI Mode		20	25	mA
	SE SCSI Mode		1.6	10	mA
	Disabled Terminator		250	400	μA
Regulator Section					
1.25V Regulator	LVD SCSI Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	$V_{\text{REG}} = 0\text{V}$	–375	–700	–1000	mA
1.25V Regulator Sink Current	$V_{\text{REG}} = 3.3\text{V}$	170	300	700	mA
1.3V Regulator	Diff Sense	1.2	1.3	1.4	V
1.3V Regulator Source Current	$V_{\text{REG}} = 0\text{V}$	–15		–5	mA
1.3V Regulator Sink Current	$V_{\text{REG}} = 3.3\text{V}$	50		200	μA
2.7V Regulator	SE SCSI Mode	2.5	2.7	3.0	V
2.7V Regulator Source Current	$V_{\text{REG}} = 0\text{V}$	–375	–700	–1000	mA
2.7V Regulator Sink Current	$V_{\text{REG}} = 3.3\text{V}$	170	300	700	mA
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedance	(Note 2)	110	150	165	Ω
Differential Bias Voltage		100		125	mV
Common Mode Bias		1.15	1.25	1.35	V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0^\circ\text{C}$ to 70°C , $\text{TRMPWR} = 3.3\text{V}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Single Ended Termination Section					
Impedance	$Z = (V_{LX} - 0.2\text{V}) / I_{LX}$, (Note 3)	102.3	110	117.7	Ω
Termination Current	Signal Level 0.2V, All Lines Low	-21	-24	-25.4	mA
	Signal Level 0.5V	-18		-22.4	mA
Output Leakage				400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SE Impedance	$I = 10\text{mA}$		20	60	Ω
Disconnect and Diff Buffer Input Section					
DISCNCT Threshold		0.8		2.0	V
DISCNCT Input Current			10	30	μA
Diff Buffer Single Ended to LVD Threshold		0.5		0.7	V
Diff Buffer LVD to HPD Threshold		1.9		2.4	V
DIFFB Input Current		-10		10	μA

Note 1: Ensured by design. Not 100% tested in production.

Note 2: Line+ (positive) tied to Line- (negative); $\frac{1.2\text{V}}{[I_{(VCM\text{ max})} - I_{(VCM\text{ min})}]}$

Note 3: V_{LX} = Output voltage for each terminator minus output pin (L1- through L15-) with each pin unloaded.
 I_{LX} = Output current for each terminator minus output pin (L1- through L15-) with the minus output pin forced to 0.2V.

PIN DESCRIPTIONS

DIFFB: Diff sense filter pin should be connected at a $4.7\mu\text{F}$ capacitor.

DIFFSENS: The SCSI bus Diff Sense line to detect what types of devices are connected to the SCSI bus.

DISCNCT: Disconnect pin shuts down the terminator when it is not at the end of the bus. The disconnect pin low enables the terminator.

Note: In Disconnect Mode, the comparator set powers down for low idle current.

LINE n -: Signal line active line for single ended or negative line in differential applications for the SCSI bus.

LINE n +: Ground line for single ended or positive line for differential applications for the SCSI bus.

REG: Regulator bypass pin, must be connected to a $4.7\mu\text{F}$ capacitor.

TRMPWR: V_{IN} 2.7V to 5.25V supply, bypass near the terminator with a $4.7\mu\text{F}$ capacitor to ground.

APPLICATION INFORMATION

The UCC5638 is a Multi-mode active terminator with selectable single ended (SE) and low voltage differential (LVD) SCSI termination integrated into a monolithic component. Mode selection is accomplished with the "diff sense" signal.

The diff sense signal is a three level signal, which is driven at each end of the bus by one active terminator. An LVD SCSI or multi-mode terminator drives the diff sense line to 1.3 V. If diff sense is at 1.3 V, then bus is in LVD SCSI mode. If a single ended SCSI device is plugged into the bus, the diff sense line is shorted to ground. With diff sense shorted to ground, the terminator changes to single ended mode to accommodate the SE device. If an HVD SCSI device is plugged in to the bus, the diff sense line is pulled high and the terminator shuts down.

The diff sense line is driven and monitored by the terminator through a 100ms to 300ms noise filter at the DIFFB input pin. A set of comparators, that allow for ground shifts, determine the bus status as follows. Any diff sense signal below 0.5V indicates single ended, between 0.7V and 1.9V is LVD SCSI and above 2.2V is HVD SCSI.

In the single ended mode, a multi-mode terminator has a 110 Ω terminating resistor connected to a 2.7V termination voltage regulator. The 2.7V regulator is used on all Unitorde terminators designed for 3.3V systems. This requires the terminator to operate in specification down to 2.7V TRMPWR voltage to allow for the 3.3V supply tolerance, an unidirectional fusing device and cable drop. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed so it will not effect the capacitive balance of the bus when the device is in LVD SCSI or disconnect mode. The device requirements call for 0.5pF balance on the lines of a differential pair. The terminator capacitance has to be a small part of the capacitance imbalance.

Layout is very critical for Ultra2, Ultra3, Ultra160 and Ultra320 systems. Multi-layer boards need to adhere to the 120 Ω impedance standard, including connector and feed-through. This is normally done on the outer layers

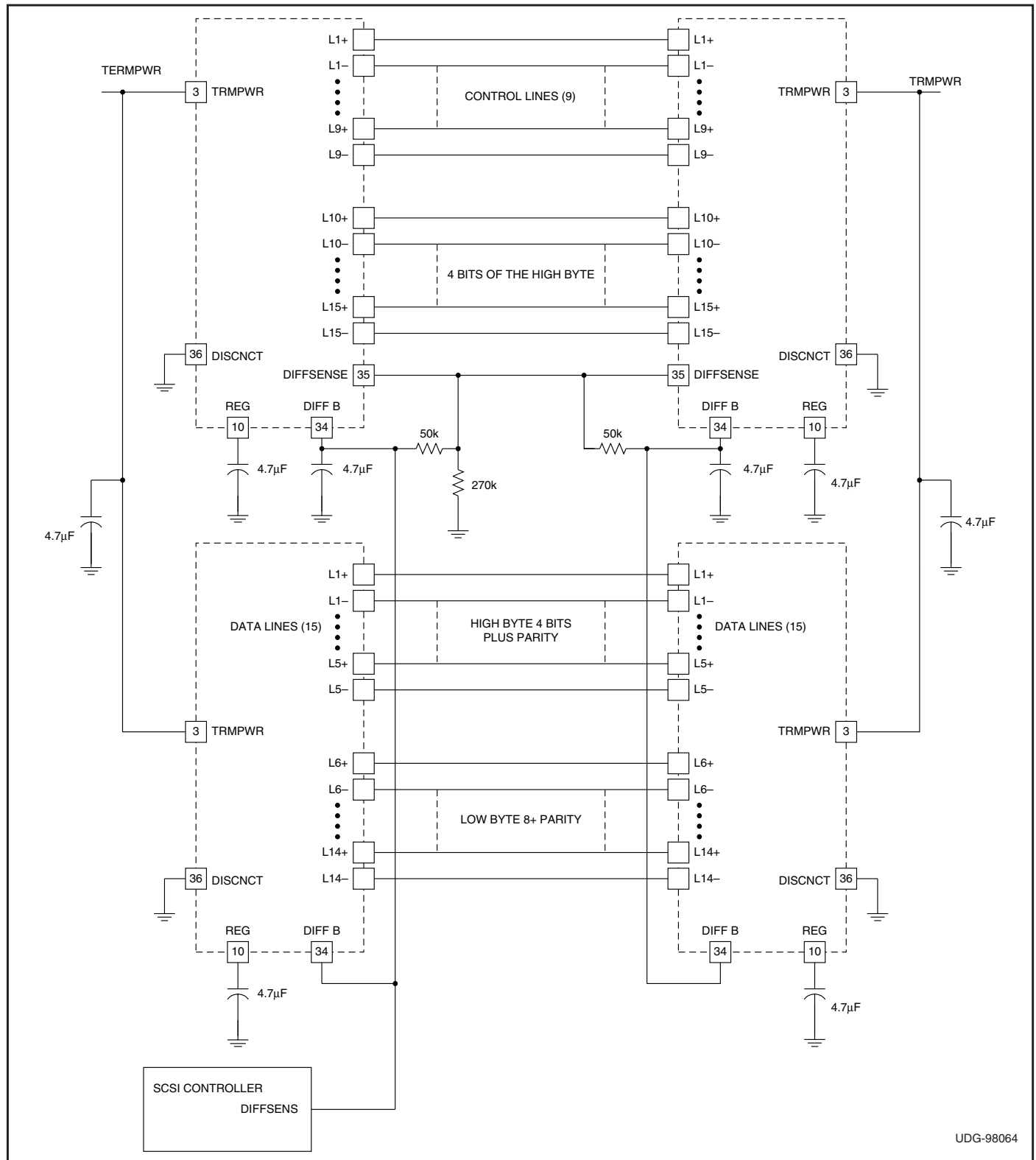
with 4 mil etch and 4 mil spacing between the runs within a pair, and a minimum of 8 mil spacing to the next pair. This spacing between the pairs reduces potential crosstalk. Beware of feed-throughs and each through hole connection adds a lot of capacitance. Standard power and ground plane spacing yields about 1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes can reduce the capacitance and opening up the power and ground planes under the connector can reduce the capacitance for through hole connector applications. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50 Ω rather than 120 Ω differential systems.

Capacitance balance is critical for Ultra2 and Ultra3/Ultra160. The balance capacitance standard is 0.5pF per line with the balance between pairs of 2pF. The components are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. Layout balance is critical, feed-throughs and etch length must be balanced, preferably no feed-throughs would be used. Capacitance for devices should be measured in the typical application, material and components above and below the circuit board effect the capacitance.

Multi-mode terminators need to consider power dissipation; the UCC5638 is offered in a power package with heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. These pins need to be connected to etch area or a feed-through per pin connecting to the ground plane layer on a multi-layer board.

In 3.3V TRMPWR systems, the UCC3912 should be used to replace the fuse and diode. This reduces the voltage drop, allowing for cable drop to the far end terminator. 3.3V battery systems normally have a 10% tolerance. The UCC3912 is 150mV drop under LVD SCSI loads, allowing 150mV drop in the cable system. All Unitorde LVD SCSI and multi-mode terminators are designed for 3.3V systems, operating down to 2.7V.

TYPICAL APPLICATION



Note: A 220k resistor is added to ground to insure the transceivers will come up in single-ended mode when no terminator is enabled. The controller DIFF SENSE ties to the DIFF B pin on the terminators, only one RC network should be on a device.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC5638FQPTR	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	UCC5638 FQP
UCC5638FQPTR.A	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	UCC5638 FQP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

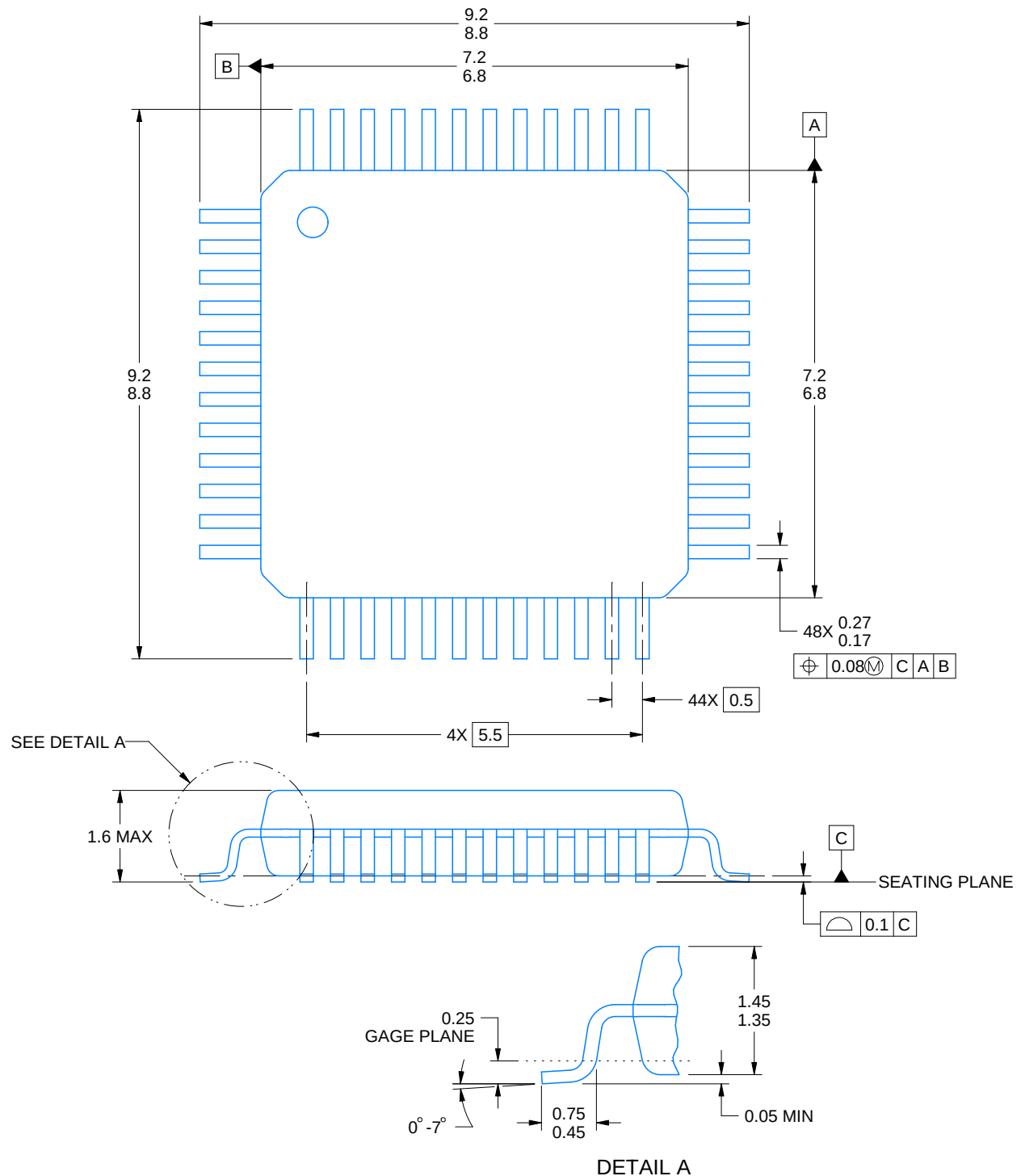
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PT0048A

PACKAGE OUTLINE

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



4215159/B 11/2023

NOTES:

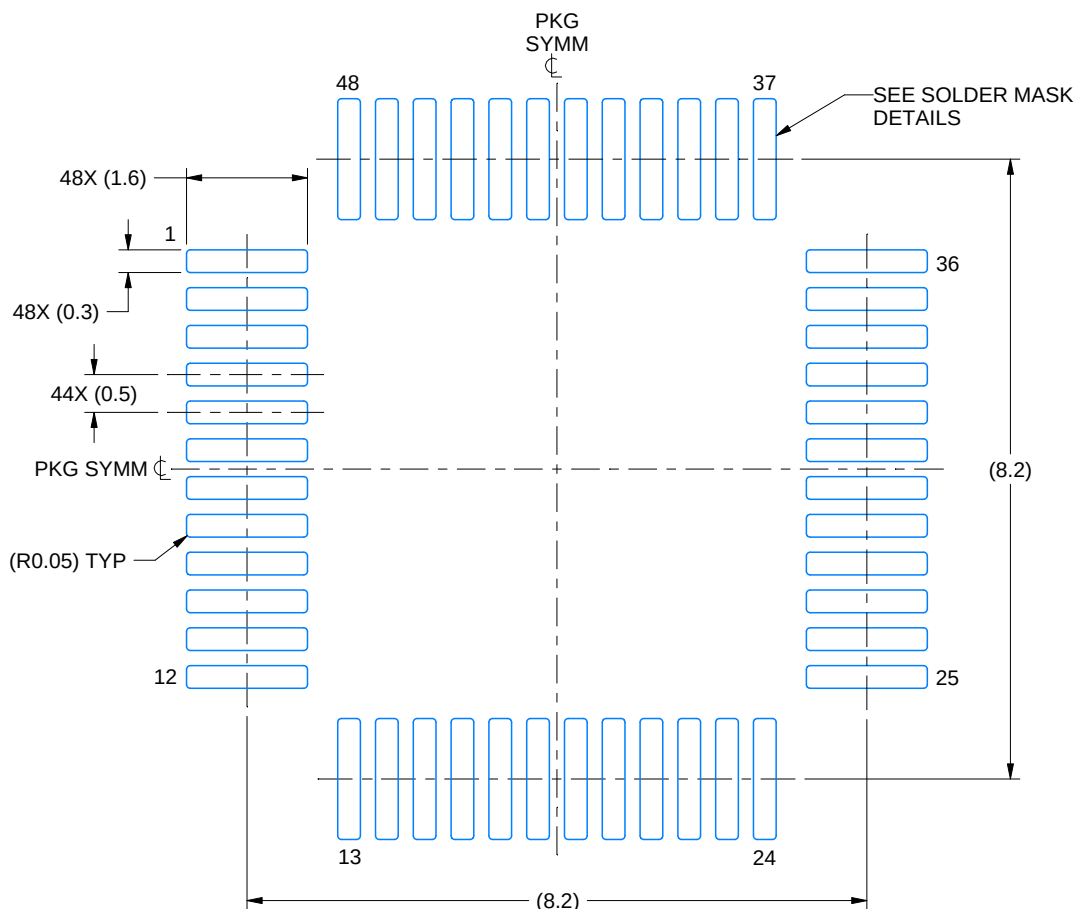
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads connected to the die pads.

EXAMPLE BOARD LAYOUT

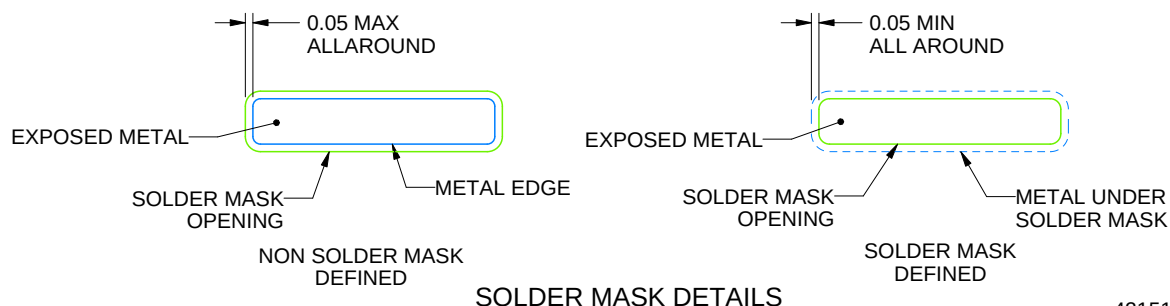
PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



SOLDER MASK DETAILS

4215159/B 11/2023

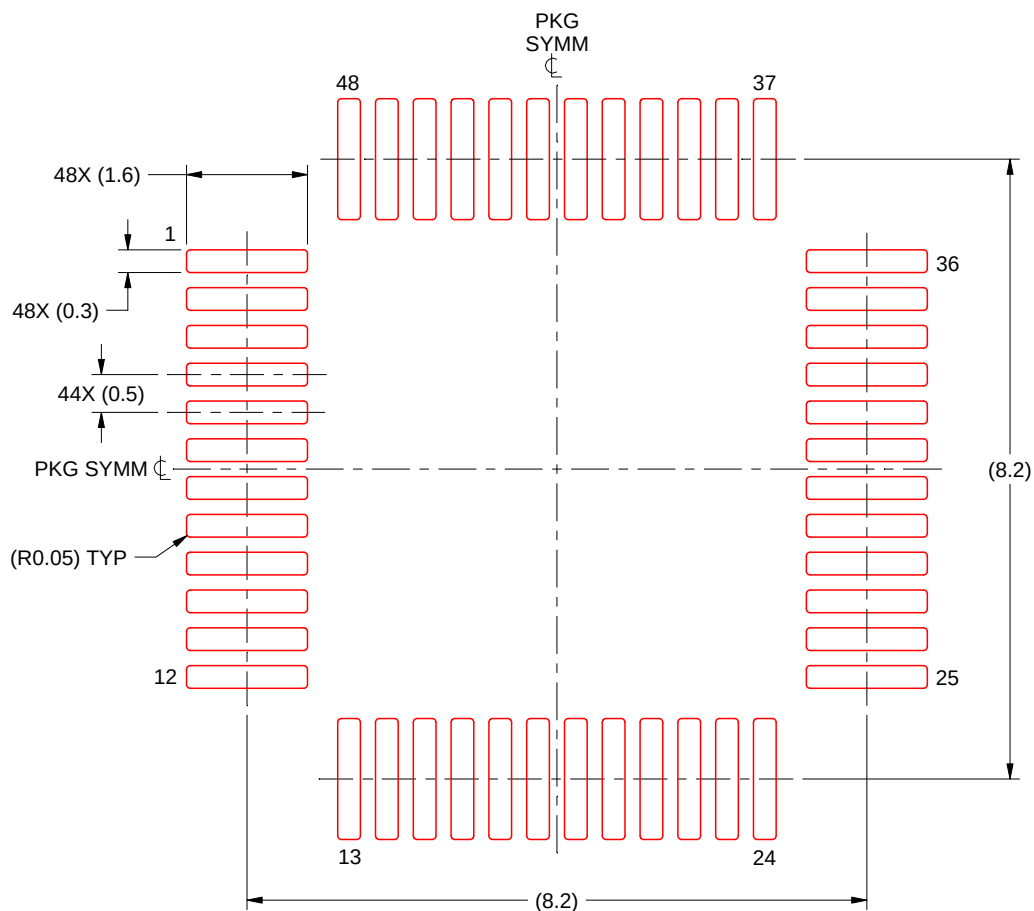
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025