BURR-BROWN®

ADC72

16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

FEATURES

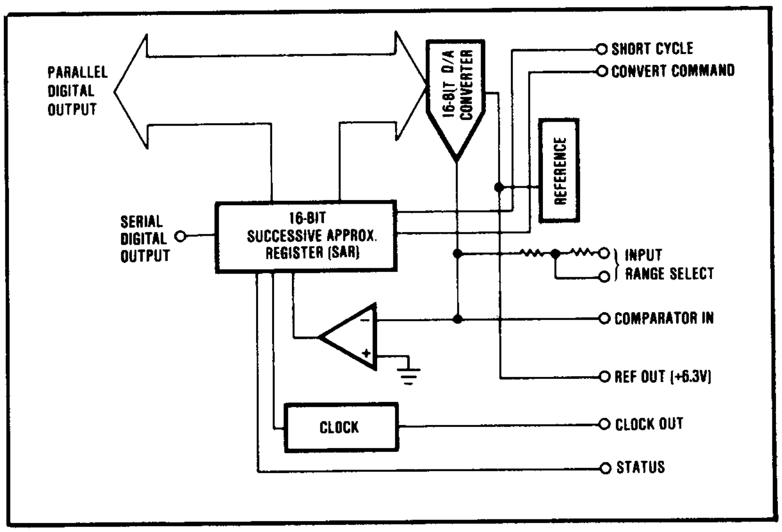
- 16-BIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- COMPACT DESIGN
  32-Pin Hermetic Metal Package
- FAST CONVERSION SPEED
  50μs Maximum
- LOW COST

DESCRIPTION

The ADC72 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. It uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a compact 32-pin metal dual-in-line package. The converter is complete with internal reference, clock, comparator, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Data is available in parallel and serial form with corresponding clock and status output. All digital input and outputs are DTL/TTL compatible.

Power supply voltages are ±15VDC and +5VDC.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-432B

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated power supplies unless otherwise noted.

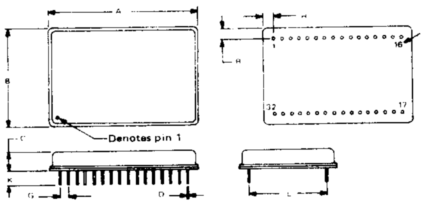
MODEL	ADC72JM, KM			ADC72AM, BM			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
INPUT							
ANALOG							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL(1)							
Convert Command	Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading			1			1	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(2)		±0.1	±0.2		±0.1	±0.2	%
Offset Gain(2)							
Unipolar		±0.05	±0.1		±0.05	±0.1	% of FSR(3)
Bipolar		±0.1	±0.2		±0.1	±0.2	% of FSR
Linearity Error KM, BM			±0.003			±0.003	% of FSR
JM, AM			±0.006			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		±0.003			±0.003		% of FSR/%ΔVs
+5VDC		±0.001			±0.001		% of FSR/%ΔVs
CONVERSION TIME(4) (14 Bits)			50			50	μs
WARM-UP TIME	10			10			min
DRIFT							
Gain		±10	±20		±7	±15	ppm/°C
Offset							
Unipolar		±2	±4			±2	ppm of FSR/°C
Bipolar		±8	±10		±5	±10	ppm of FSR/°C
Linearity		±2	±3			±2	ppm of FSR/°C
No Missing Codes Temp Range							
JM, AM (13 bits)	0		+50	0		+50	°C
KM, BM (14 bits)	+10		+40	+10		+40	°C
OUTPUT							
DIGITAL DATA							
All codes complementary							
Parallel							
Output Codes(5)							
Unipolar	CSB						
Bipolar	COB, CTC(6)						
Output Drive	2						TTL Loads
Status	Logic "1" during conversion						
Status Output Drive			2			2	TTL Loads
Internal Clock							
Clock Output Drive			2			2	TTL Loads
Frequency		280			280		kHz
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Max External Current with No Degradation of Specs			±200			±200	μA
Temp Coefficient			±10			±5	ppm/°C
POWER SUPPLY REQUIREMENTS							
Power Consumption		550			550		mW
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Rated Voltage, Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain +15VDC		+15			+15		mA
Supply Drain -15VDC		−18			−18		mA
Supply Drain +5VDC		+10			+10		mA
TEMPERATURE RANGE							
Specification	0		+70	-25		+85	°C
Operating (derated specs)	-25		+85	-55		+85	°C
Storage	-55		+125	-55		+125	°C

NOTES:

1. DTL/TTL compatible, i.e., Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V, max. Logic "1" = 2.4V, min
2. Adjustable to zero
3. FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR
4. Conversion time may be shortened with "Short Cycle" set for lower resolution, see "Additional Connections Required" section.
5. See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.
6. CTC coding obtained by inverting MSB. Pin 1

MECHANICAL

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.720	1.780	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

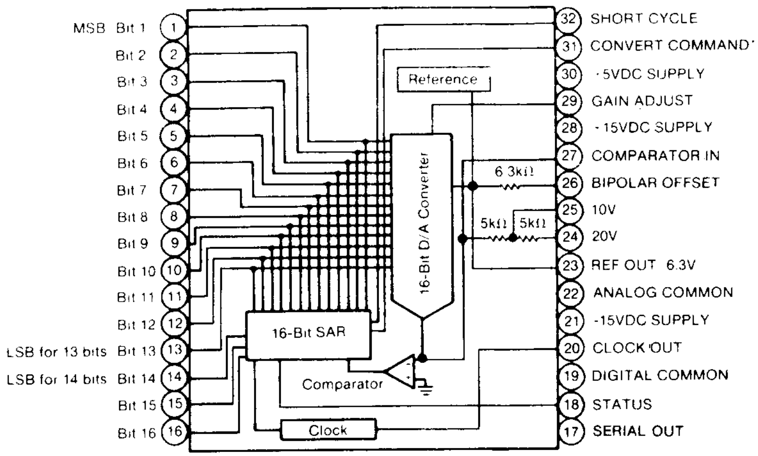


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

CASE: Nickel-plated kovar
MATING CONNECTOR: 2302MC
WEIGHT: 13 grams (0.46 oz.)
Contrasting glass seal or square corner denotes pin 1.

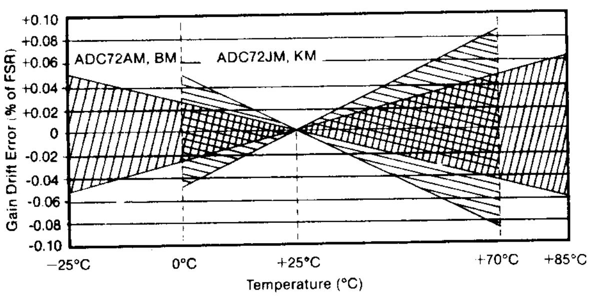
CONNECTION DIAGRAM



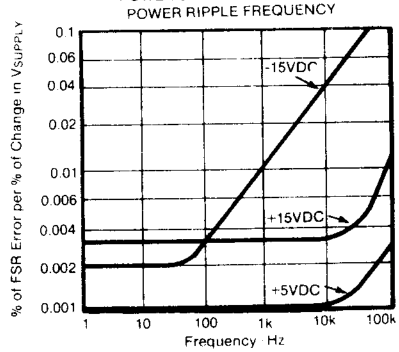
*If an external clock is used, connect the clock to pin 31 CONVERT COMMAND

TYPICAL PERFORMANCE CURVES

GAIN DRIFT ERROR (% OF FSR)
VS TEMPERATURE



POWER SUPPLY REJECTION VS
POWER RIPPLE FREQUENCY



DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2 LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC72 is also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperature range when short-cycled for 14-bit operation.

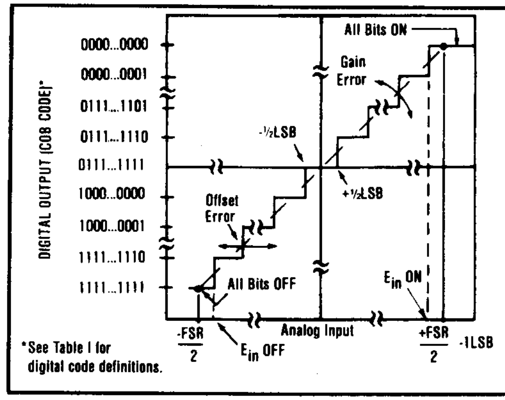


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 2a and 2b are timing diagrams showing the relationship of serial data to clock and valid data to status.

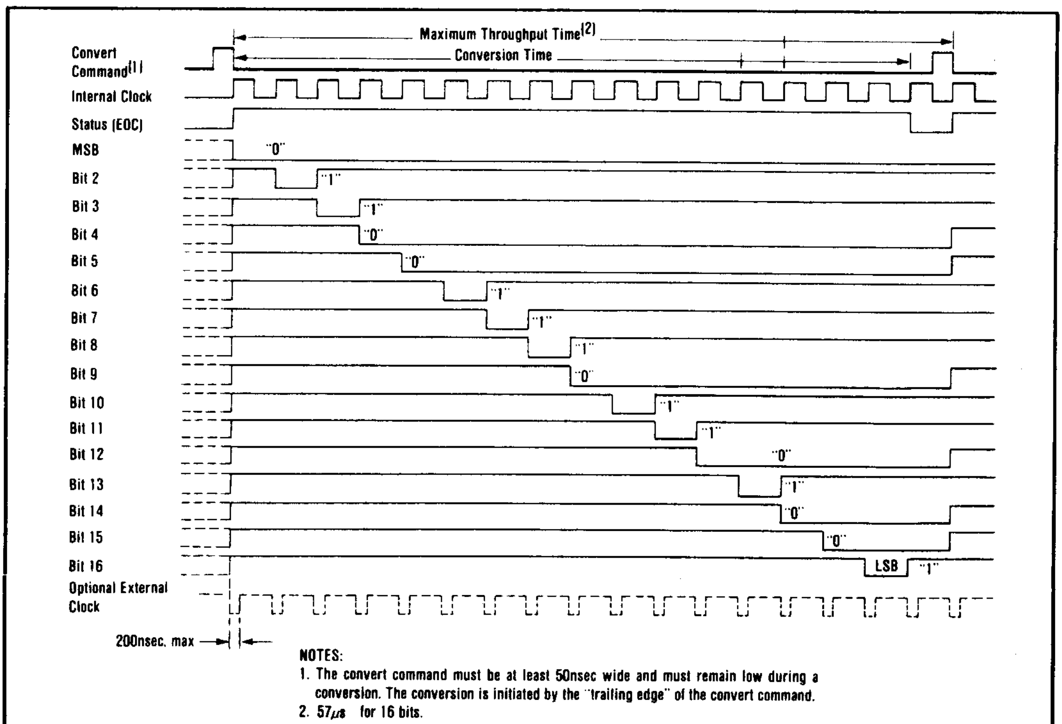


FIGURE 2. ADC72 Timing Diagram.

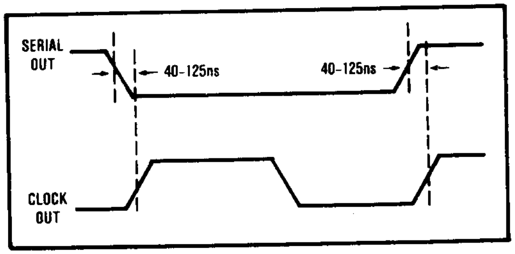


FIGURE 2a. Timing Relationship of Serial Data to Clock.

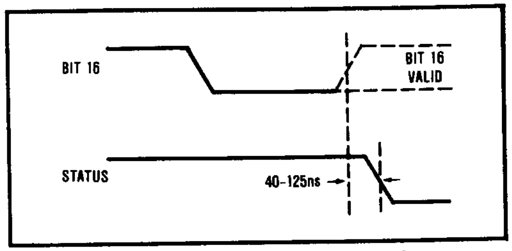


FIGURE 2b. Timing Relationship of Valid Data to Status.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Two binary codes are available on the ADC72 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (Pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 3 shows the connections for 14-bit resolution, parallel data output, with ±10V output.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line: CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagrams of Figures 2 and 2a. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

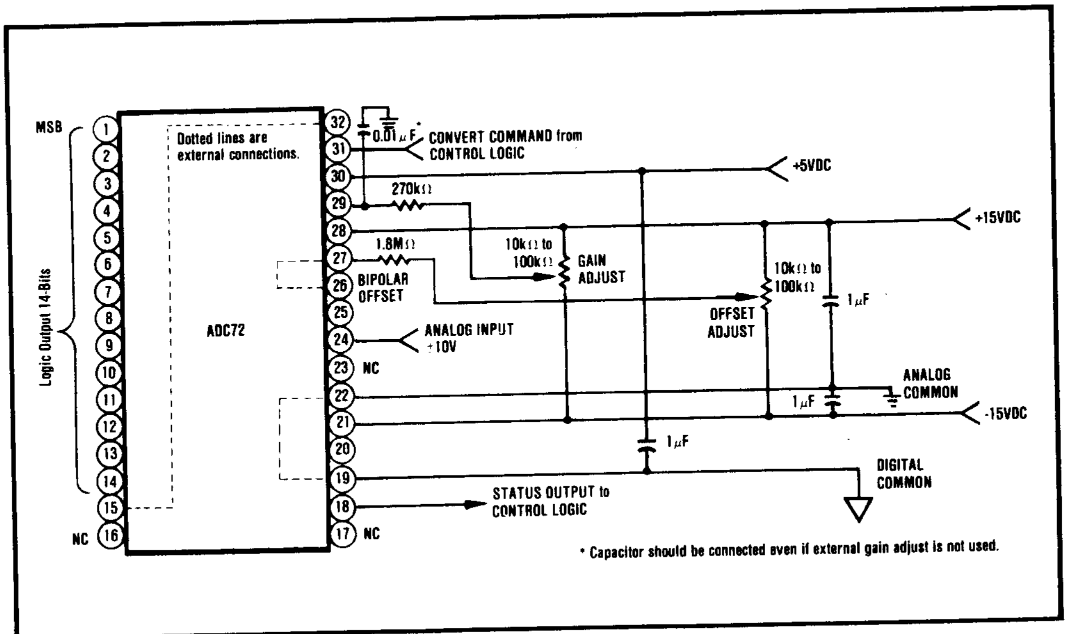


FIGURE 3. ADC72 Connections For: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary BIN Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]	CSB[3]
One Least Significant Bit LSB	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	n = 14	1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values MSB LSB							
000...000[4]	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

[1] COB = Complementary Offset Binary
[2] CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB = Pin 1
[3] CSB = Complementary Straight Binary
[4] Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC72 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC72 power supply sensitivity is specified for ±0.003% of FSR/%ΔV_S for ±15V supplies and ±0.001% of FSR/%ΔV_S for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 4.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC72 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF non-polarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (Pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum capacitors as shown in Figure 4 to obtain noise free operation. These capacitors should be located close to the ADC.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 5 for circuit details.

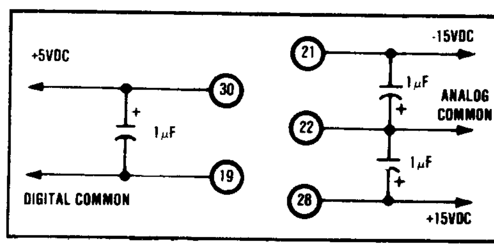


FIGURE 4. Recommended Power Supply Decoupling.

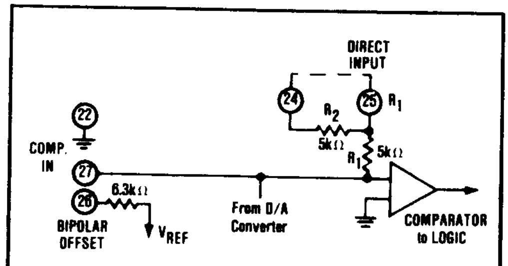


FIGURE 5. ADC72 Input Scaling Circuit.

TABLE II. ADC72 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB Pin 1

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and Pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 6. **Sweep the input through the end point transition voltage that should cause an output transition to all bits Off (E_{IN}^{OFF}).**

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

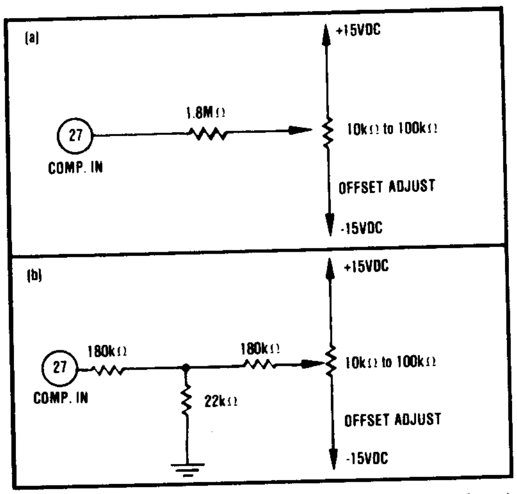


FIGURE 6. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

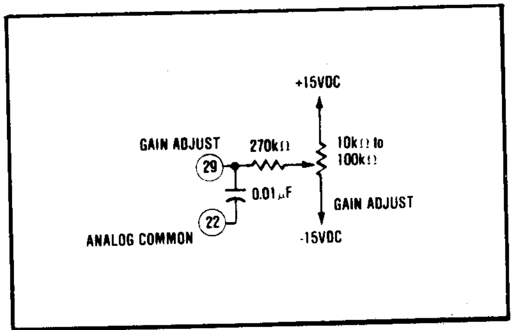


FIGURE 7. Connecting Optional Gain Adjust with a 0.2% Range of Adjustment.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

ADDITIONAL CONNECTIONS REQUIRED

The ADC72 may be operated at faster speeds for resolutions less than 14 or 13 bits, depending on the model selected, by connecting the Short-Cycle Input, pin 32, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

TABLE III. Short-Cycle Connections and Specifications for 12- to 14-Bit Resolutions.

Resolution (Bits)	16	14	13	12
Connect Pin 32 to	Open	Pin 15	Pin 14	Pin 13
Maximum Conversion Speed (μsec)(1)	57	50	46.5	43
Maximum Nonlinearity at 25°C (% of FSR)	0.003(2)	0.003(2)	0.006	0.006

NOTES:
1. Max. conversion time to maintain specified nonlinearity error.
2. BM and KM models only.

OUTPUT DRIVE

Normally all ADC72 logic outputs will drive 2 standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

HEAT DISSIPATION

The ADC72 dissipates approximately 550mW (typical) and the packages have a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above 70°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 8 for θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16 square inch (min.) area, this technique will allow operation to 85°C.

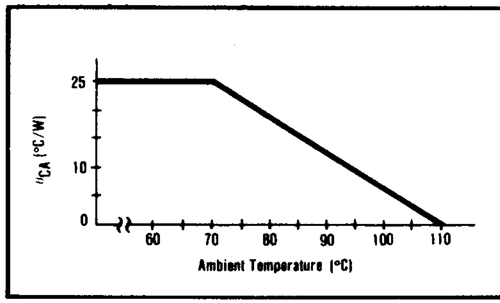


FIGURE 8. θ_{CA} Requirement Above 70°C.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	NONLINEARITY
ADC72JM	0°C to +70°C	±0.006% FSR
ADC72KM	0°C to +70°C	±0.003% FSR
ADC72AM	-25°C to +85°C	±0.006% FSR
ADC72BM	-25°C to +85°C	±0.003% FSR