

# 24-BIT, 192-kHz SAMPLING, ADVANCED SEGMENT, AUDIO STEREO DIGITAL-TO-ANALOG CONVERTER

## FEATURES

- **Supports Both DSD and PCM Formats**
- **24-Bit Resolution**
- **Analog Performance:**
  - **Dynamic Range: 113 dB**
  - **THD+N: 0.001%**
  - **Full-Scale Output: 2.1 V rms (at Postamplifier)**
- **Differential Voltage Output: 3.2 V p-p**
- **8× Oversampling Digital Filter:**
  - **Stop-Band Attenuation: –82 dB**
  - **Pass-Band Ripple: ±0.002 dB**
- **Sampling Frequency: 10 kHz to 200 kHz**
- **System Clock: 128, 192, 256, 384, 512, or 768 $f_S$ With Autodetect**
- **Accepts 16-, 20-, and 24-Bit Audio Data**
- **PCM Data Formats: Standard, $I^2S$, and Left-Justified**
- **DSD Format Interface Available**
- **Optional Interface to External Digital Filter or DSP Available**
- **$I^2C$-Compatible Serial Port**
- **User-Programmable Mode Controls:**
  - **Digital Attenuation: 0 dB to –120 dB, 0.5 dB/Step**
  - **Digital De-Emphasis**
  - **Digital Filter Rolloff: Sharp or Slow**
  - **Soft Mute**
  - **Zero Flags for Each Output in PCM and DSD Formats**
- **Dual Supply Operation:**
  - **5-V Analog, 3.3-V Digital**
- **5-V Tolerant Digital Inputs**
- **Small 28-Lead SSOP Package, Lead-Free Product**

## APPLICATIONS

- **A/V Receivers**
- **SACD Players**
- **DVD Players**
- **HDTV Receivers**
- **Car Audio Systems**
- **Digital Multitrack Recorders**
- **Other Applications Requiring 24-Bit Audio**

## DESCRIPTION

The DSD1793 is a monolithic CMOS integrated circuit that includes stereo digital-to-analog converters and support circuitry in a small 28-lead SSOP package. The data converters use TI’s advanced-segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The DSD1793 provides balanced voltage outputs, allowing the user to optimize analog performance externally. The DSD1793 accepts the PCM and DSD audio data formats, providing easy interfacing to audio DSP and decoder chips. The DSD1793 also accepts interfaces to external digital filter devices (DF1704, DF1706, PMD200). Sampling rates up to 200 kHz are supported. A full set of user-programmable functions is accessible through an $I^2C$-compatible serial control port.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE CODE | OPERATION TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| DSD1793DB | 28-lead SSOP | 28DB | −25°C to 85°C | DSD1793 | DSD1793DB | Tube |
| | | | | | DSD1793DBR | Tape and reel |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | DSD1791 |
|---|---|---|
| Supply voltage | $V_{CC}F$, $V_{CC}L$, $V_{CC}C$, $V_{CC}R$ | −0.3 V to 6.5 V |
| | $V_{DD}$ | −0.3 V to 4 V |
| Supply voltage differences: $V_{CC}F$, $V_{CC}L$, $V_{CC}C$, $V_{CC}R$ | | ±0.1 V |
| Ground voltage differences: AGNDF, AGNDL, AGNDC, AGNDR, DGND | | ±0.1 V |
| Digital input voltage | PLRCK, PDATA, PBCK, DSDL, DSDR, DBCK, ADR0, ADR1, SCK, SCL, SDA | –0.3 V to 6.5 V |
| | ZEROL, ZEROR | –0.3 V to ($V_{DD}$ + 0.3 V) < 4 V |
| Analog input voltage | | –0.3 V to ($V_{CC}$ + 0.3 V) < 6.5 V |
| Input current (any pins except supplies) | | ±10 mA |
| Ambient temperature under bias | | –40°C to 125°C |
| Storage temperature | | –55°C to 150°C |
| Junction temperature | | 150°C |
| Lead temperature (soldering) | | 260°C, 5 s |
| Package temperature (IR reflow, peak) | | 260°C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

all specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $V_{DD}$ = 3.3 V, $f_S$ = 44.1 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted

| | PARAMETER | DSD1793DB MIN | DSD1793DB TYP | DSD1793DB MAX | UNIT |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 24 | | Bits |
| **DATA FORMAT (PCM Mode)** | | | | | |
| | Audio data interface format | | Standard, I2S, left justified | | |
| | Audio data bit length | | 16-, 20-, 24-bit selectable | | |
| | Audio data format | | MSB first, 2s complement | | |
| $f_S$ | Sampling frequency | 10 | | 200 | kHz |
| | System clock frequency | | 128, 192, 256, 384, 512, 768 $f_S$ | | |
| **DATA FORMAT (DSD Mode)** | | | | | |
| | Audio data interface format | | DSD (direct stream digital) | | |
| | Audio data bit length | | 1 Bit | | |
| $f_S$ | Sampling frequency | | 2.8224 | | MHz |
| | System clock frequency | 2.8224 | | 11.2896 | MHz |

## ELECTRICAL CHARACTERISTICS (Continued)

all specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $V_{DD}$ = 3.3 V, $f_S$ = 44.1 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | DSD1793DB MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL INPUT/OUTPUT** | | | | | | |
| | Logic family | | | TTL compatible | | |
| $V_{IH}$ | Input logic level | | 2 | | | VDC |
| $V_{IL}$ | Input logic level | | | | 0.8 | VDC |
| $I_{IH}$ | Input logic current | $V_{IN} = V_{DD}$ | | | 10 | µA |
| $I_{IL}$ | Input logic current | $V_{IN}$ = 0 V | | | –10 | µA |
| $V_{OH}$ | Output logic level | $I_{OH}$ = −2 mA | 2.4 | | | VDC |
| $V_{OL}$ | Output logic level | $I_{OL}$ = 2 mA | | | 0.4 | VDC |
| **DYNAMIC PERFORMANCE (PCM MODE)** (1) | | | | | | |
| | THD+N at $V_{OUT}$ = 0 dB | $f_S$ = 44.1 kHz | | 0.001% | 0.002% | |
| | | $f_S$ = 96 kHz | | 0.0015% | | |
| | | $f_S$ = 192 kHz | | 0.003% | | |
| | Dynamic range | EIAJ, A-weighted, $f_S$ = 44.1 kHz | 110 | 113 | | dB |
| | | EIAJ, A-weighted, $f_S$ = 96 kHz | | 113 | | |
| | | EIAJ, A-weighted, $f_S$ = 192 kHz | | 113 | | |
| | Signal-to-noise ratio | EIAJ, A-weighted, $f_S$ = 44.1 kHz | 110 | 113 | | dB |
| | | EIAJ, A-weighted, $f_S$ = 96 kHz | | 113 | | |
| | | EIAJ, A-weighted, $f_S$ = 192 kHz | | 113 | | |
| | Channel separation | $f_S$ = 44.1 kHz | 106 | 110 | | dB |
| | | $f_S$ = 96 kHz | | 110 | | |
| | | $f_S$ = 192 kHz | | 109 | | |
| | Level linearity error | $V_{OUT}$ = –120 dB | | ±1 | | dB |
| **DYNAMIC PERFORMANCE (DSD MODE)** (1) (2) | | | | | | |
| | THD+N at $V_{OUT}$ = 0 dB | 2.1 V rms | | 0.001% | | |
| | Dynamic range | –60 dB, EIAJ, A-weighted | | 113 | | dB |
| | Signal-to-noise ratio | EIAJ, A-weighted | | 113 | | dB |
| **ANALOG OUTPUT** | | | | | | |
| | Gain error | | –8 | ±3 | 8 | % of FSR |
| | Gain mismatch, channel-to-channel | | –3 | ±0.5 | 3 | % of FSR |
| | Bipolar zero error | At BPZ | –2 | ±0.5 | 2 | % of FSR |
| | Differential output voltage (3) | Full scale (0 dB) | | 3.2 | | V p-p |
| | Bipolar zero voltage (3) | At BPZ | | 1.4 | | V |
| | Load impedance (3) | $R_1 = R_2$ | 1.7 | | | kΩ |

(1) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 32. Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode. For all sampling-frequency operations, measurement bandwidth is limited with a 20-kHz AES17 filter.

(2) Analog performance in the DSD mode is specified as the DSD modulation index of 100%. This is equivalent to PCM mode performance at 44.1 kHz and 64 $f_S$.

(3) These parameters are defined at the DSD1793 output pins. Load impedances, $R_1$ and $R_2$, are input resistors of the postamplifier. They are defined as dc-coupled loads.

## ELECTRICAL CHARACTERISTICS (Continued)

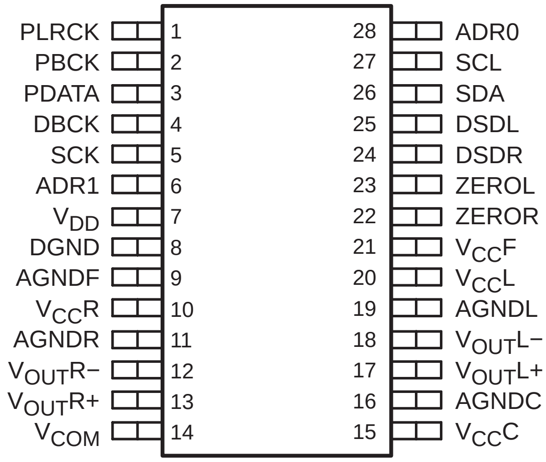
all specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $V_{DD}$ = 3.3 V, $f_S$ = 44.1 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | DSD1793DB MIN | DSD1793DB TYP | DSD1793DB MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL FILTER PERFORMANCE** | | | | | | |
| | De-emphasis error | | | | ±0.1 | dB |
| **FILTER CHARACTERISTICS-1: SHARP ROLLOFF** | | | | | | |
| | Pass band | ±0.002 dB | | | 0.454 $f_S$ | |
| | | –3 dB | | | 0.49 $f_S$ | |
| | Stop band | | 0.546 $f_S$ | | | |
| | Pass-band ripple | | | | ±0.002 | dB |
| | Stop-band attenuation | Stop band = 0.546 $f_S$ | –75 | | | dB |
| | | Stop band = 0.567 $f_S$ | –82 | | | |
| | Delay time | | | 29/$f_S$ | | s |
| **FILTER CHARACTERISTICS-2: SLOW ROLLOFF** | | | | | | |
| | Pass band | ±0.04 dB | | | 0.274 $f_S$ | |
| | | –3 dB | | | 0.454 $f_S$ | |
| | Stop band | | 0.732 $f_S$ | | | |
| | Pass-band ripple | | | | ±0.002 | dB |
| | Stop-band attenuation | Stop band = 0.732 $f_S$ | –82 | | | dB |
| | Delay time | | | 29/$f_S$ | | s |
| **POWER SUPPLY REQUIREMENTS** | | | | | | |
| $V_{DD}$ | Voltage range | | 3 | 3.3 | 3.6 | VDC |
| $V_{CC}$ | | | 4.5 | 5 | 5.5 | VDC |
| $I_{DD}$ | Supply current (1) | $f_S$ = 44.1 kHz | | 6.5 | 8 | mA |
| | | $f_S$ = 96 kHz | | 13.5 | | |
| | | $f_S$ = 192 kHz | | 28 | | |
| $I_{CC}$ | | $f_S$ = 44.1 kHz | | 14 | 16 | mA |
| | | $f_S$ = 96 kHz | | 15 | | |
| | | $f_S$ = 192 kHz | | 16 | | |
| | Power dissipation (1) | $f_S$ = 44.1 kHz | | 90 | 110 | mW |
| | | $f_S$ = 96 kHz | | 120 | | |
| | | $f_S$ = 192 kHz | | 170 | | |
| **TEMPERATURE RANGE** | | | | | | |
| | Operation temperature | | –25 | | 85 | °C |
| $\theta_{JA}$ | Thermal resistance | 28-pin SSOP | | 100 | | °C/W |

(1) Input is BPZ data.

## PIN ASSIGNMENTS

**DSD1793**
**(TOP VIEW)**

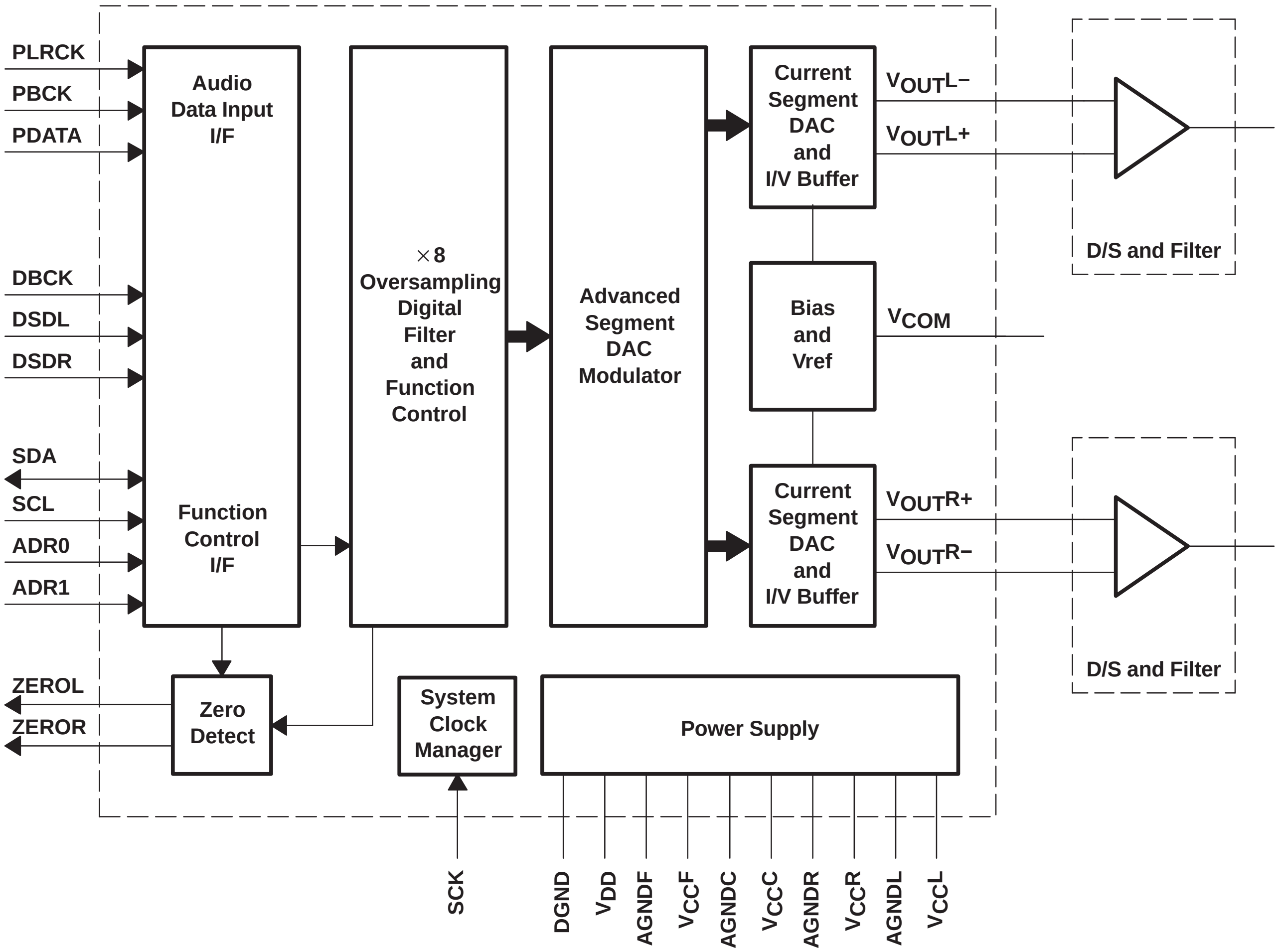


## Terminal Functions

| TERMINAL NAME | TERMINAL PIN | I/O | DESCRIPTIONS |
|---|---|---|---|
| ADR0 | 28 | I | $I^2C$ address 0 (1) |
| ADR1 | 6 | I | $I^2C$ address 1 (1) |
| AGNDC | 16 | – | Analog ground (internal bias and current DAC) |
| AGNDF | 9 | – | Analog ground (DACFF) |
| AGNDL | 19 | – | Analog ground (L-channel I/V) |
| AGNDR | 11 | – | Analog ground (R-channel I/V) |
| DBCK | 4 | I | Bit clock input for DSD mode (1) |
| DGND | 8 | – | Digital ground |
| DSDL | 25 | I | L-channel audio data input for DSD mode (1) |
| DSDR | 24 | I | R-channel audio data input for DSD mode (1) |
| PBCK | 2 | I | Bit clock input for PCM mode (1) |
| PDATA | 3 | I | Serial audio data input for PCM mode (1) |
| PLRCK | 1 | I | Left and right clock ($f_S$) input for PCM mode (1) |
| SCK | 5 | I | System clock input (1) |
| SCL | 27 | I | $I^2C$ clock (1) |
| SDA | 26 | I/O | $I^2C$ data (2) |
| $V_{CC}C$ | 15 | – | Analog power supply (internal bias and current DAC), 5 V |
| $V_{CC}F$ | 21 | – | Analog power supply (DACFF), 5 V |
| $V_{CC}L$ | 20 | – | Analog power supply (L-channel I/V), 5 V |
| $V_{CC}R$ | 10 | – | Analog power supply (R-channel I/V), 5 V |
| $V_{COM}$ | 14 | – | Internal bias decoupling pin |
| $V_{DD}$ | 7 | – | Digital power supply, 3.3 V |
| $V_{OUT}L+$ | 17 | O | L-channel analog voltage output + |
| $V_{OUT}L–$ | 18 | O | L-channel analog voltage output – |
| $V_{OUT}R+$ | 13 | O | R-channel analog voltage output + |
| $V_{OUT}R–$ | 12 | O | R-channel analog voltage output – |
| ZEROL | 23 | O | Zero flag for L-channel |
| ZEROR | 22 | O | Zero flag for R-channel |

(1) Schmitt-trigger input, 5-V tolerant
(2) Schmitt-trigger input and output. 5-V tolerant input, and open-drain, 3-state output

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL PERFORMANCE CURVES

## DIGITAL FILTER

### Digital Filter Response

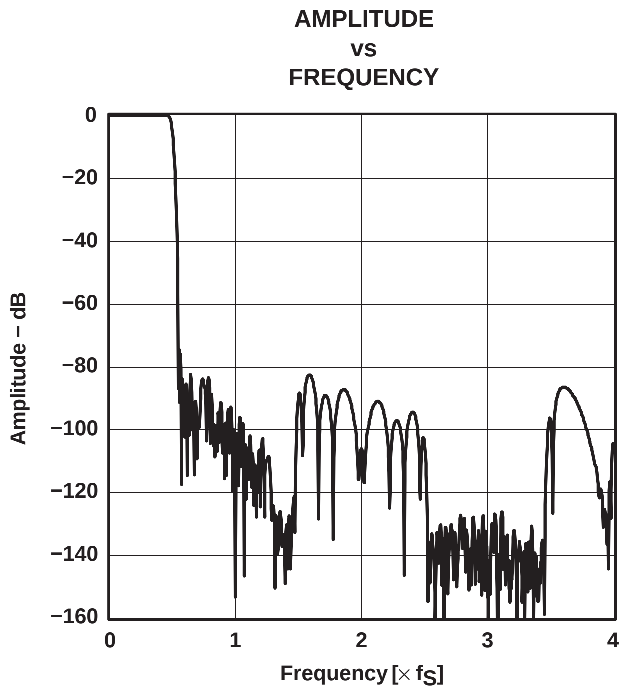



Figure 1. Frequency Response, Sharp Rolloff

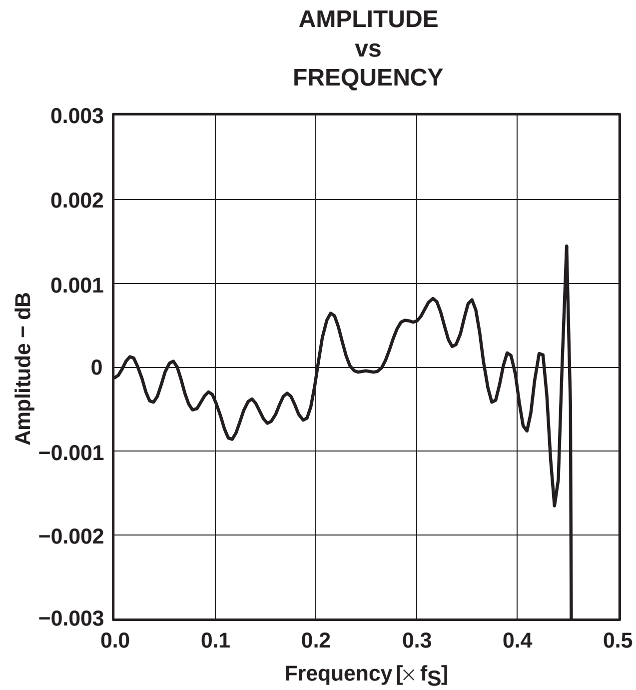



Figure 2. Pass-Band Ripple, Sharp Rolloff

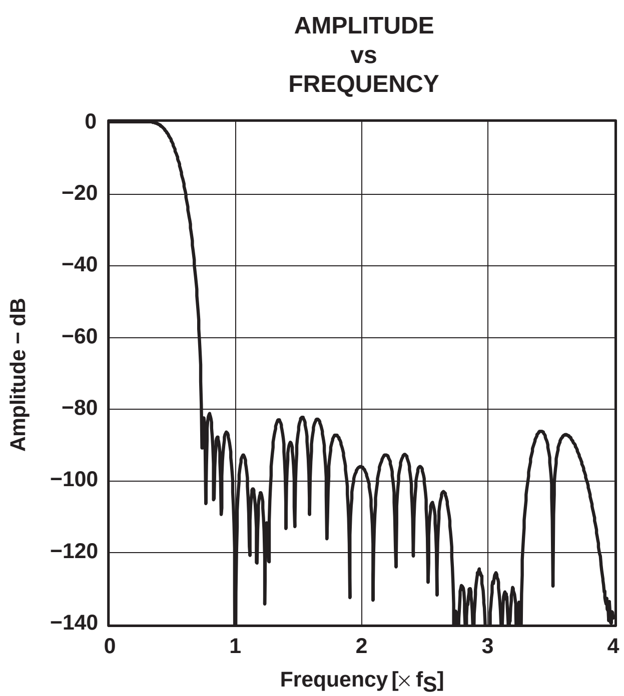



Figure 3. Frequency Response, Slow Rolloff

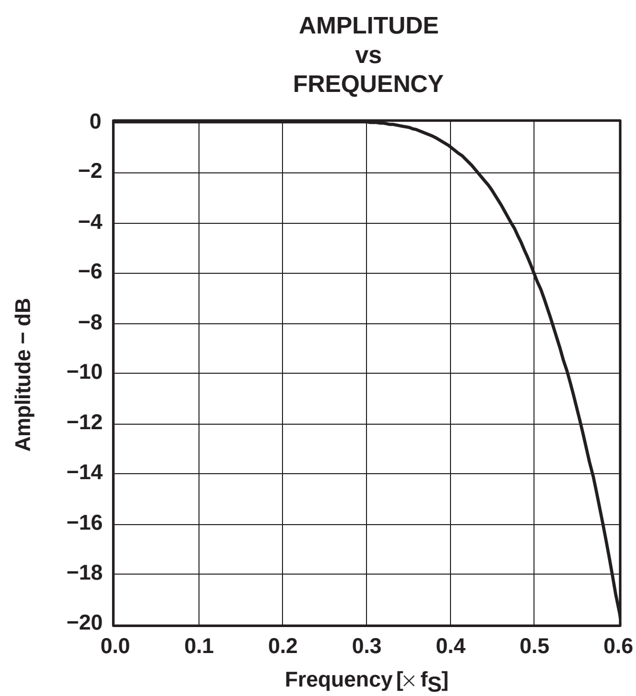



Figure 4. Transition Characteristics, Slow Rolloff

## De-Emphasis Filter

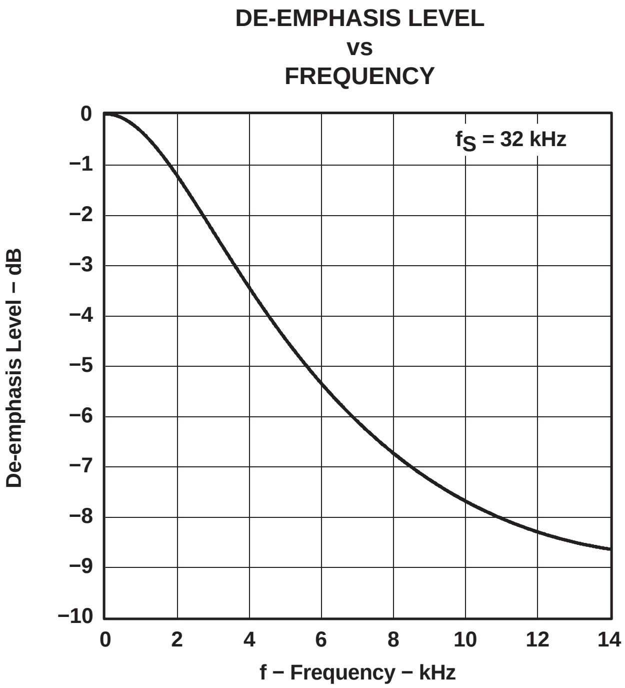



Figure 5

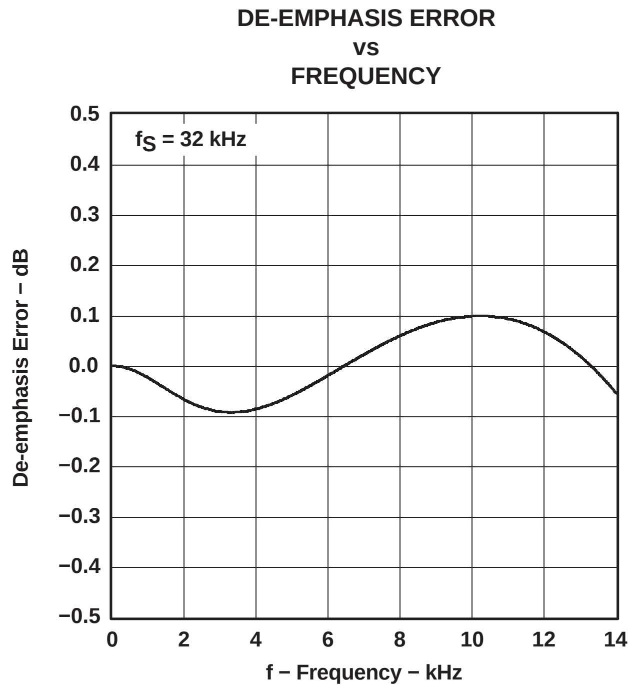



Figure 6

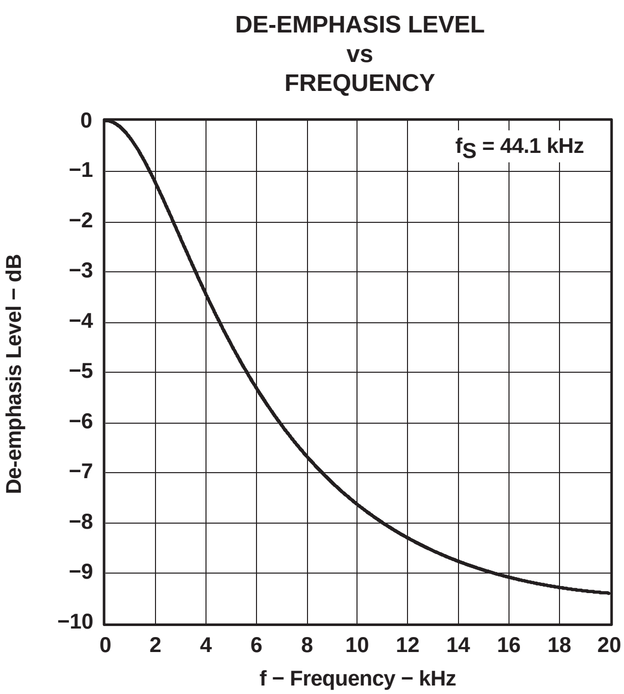



Figure 7

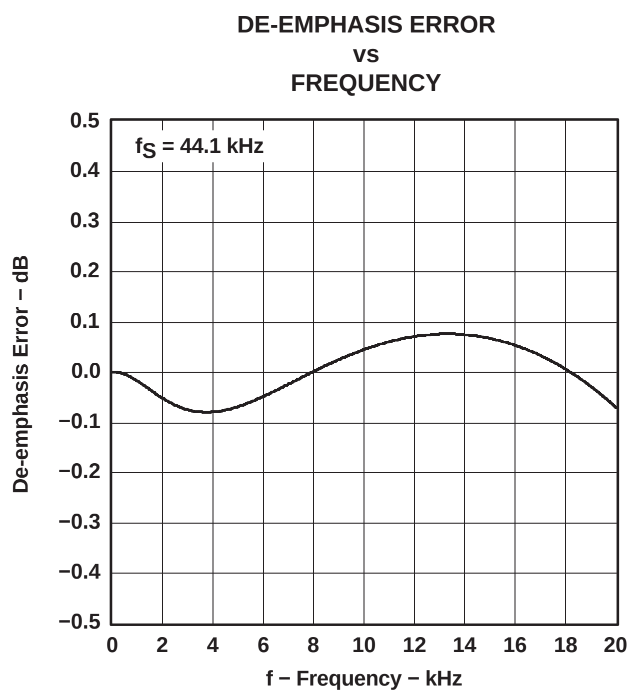



Figure 8

## De-Emphasis Filter (Continued)

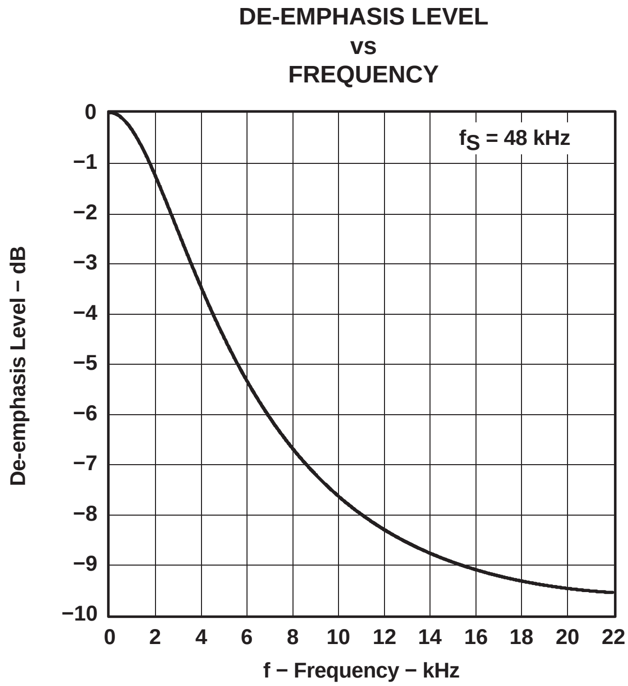



Figure 9

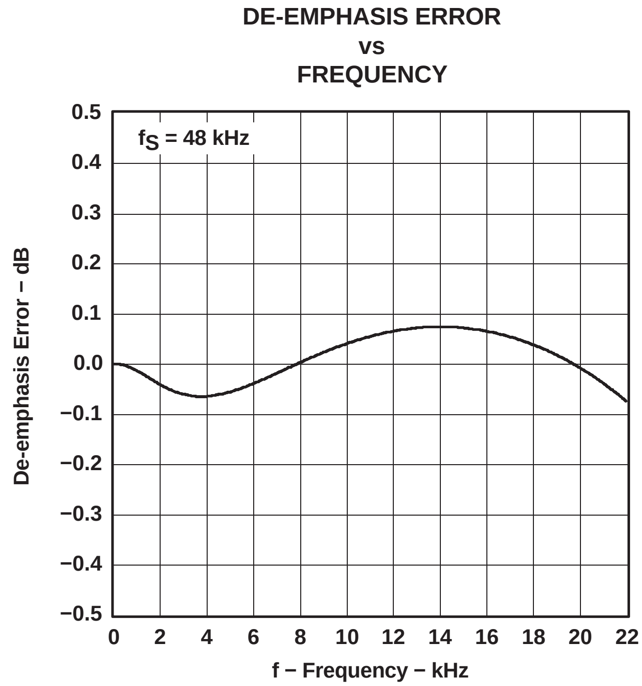



Figure 10

## ANALOG DYNAMIC PERFORMANCE

### Supply Voltage Characteristics

TOTAL HARMONIC DISTORTION + NOISE
vs
SUPPLY VOLTAGE

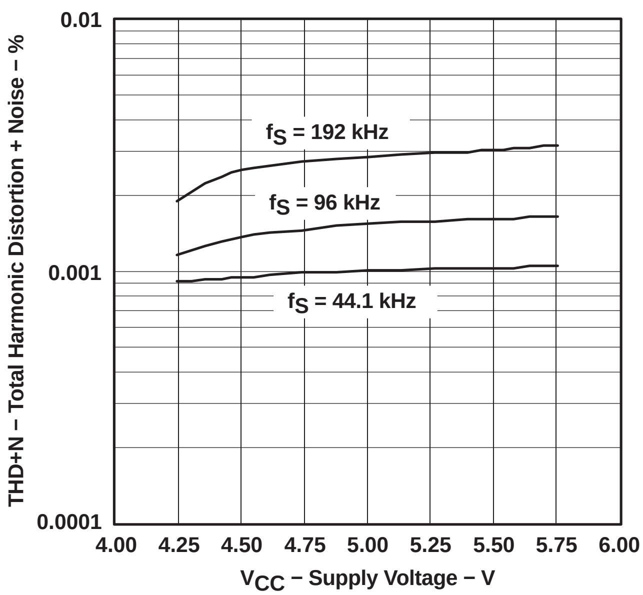



Figure 11

DYNAMIC RANGE
vs
SUPPLY VOLTAGE

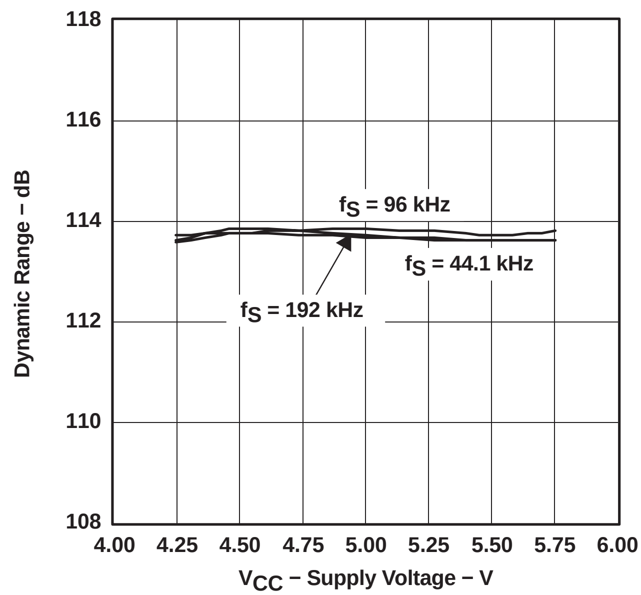



Figure 12

SIGNAL-to-NOISE RATIO
vs
SUPPLY VOLTAGE

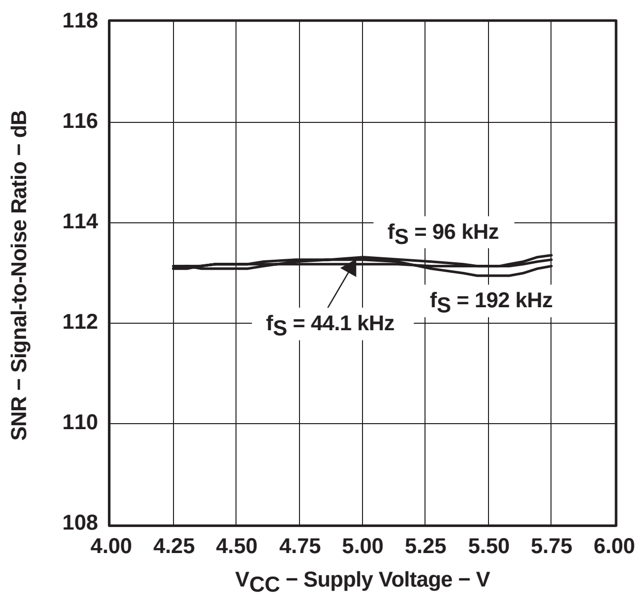



Figure 13

CHANNEL SEPARATION
vs
SUPPLY VOLTAGE

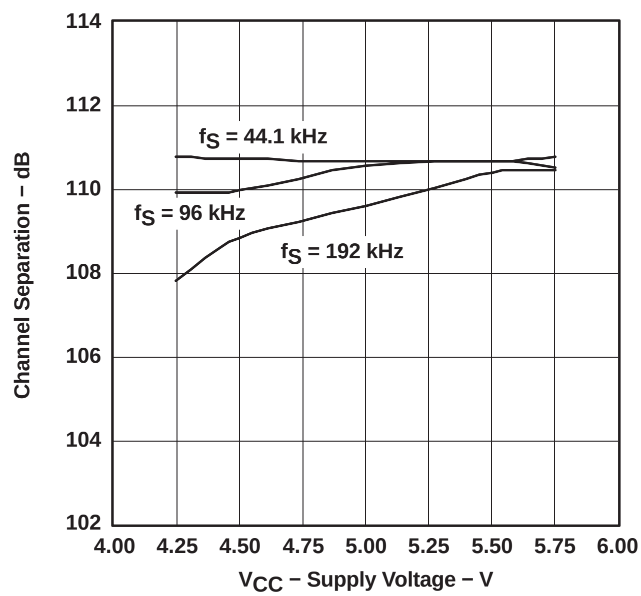



Figure 14

NOTE: PCM mode, $T_A$ = 25°C, $V_{DD}$ = 3.3 V.

## Temperature Characteristics

TOTAL HARMONIC DISTORTION + NOISE
vs
FREE-AIR TEMPERATURE

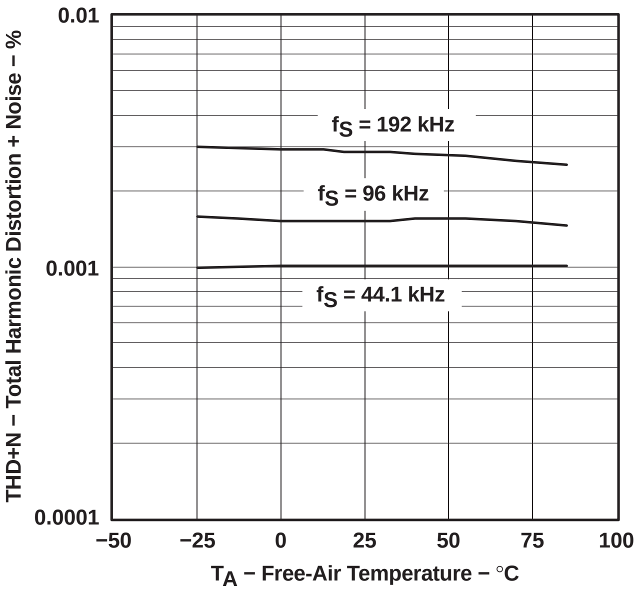



**Figure 15**

DYNAMIC RANGE
vs
FREE-AIR TEMPERATURE

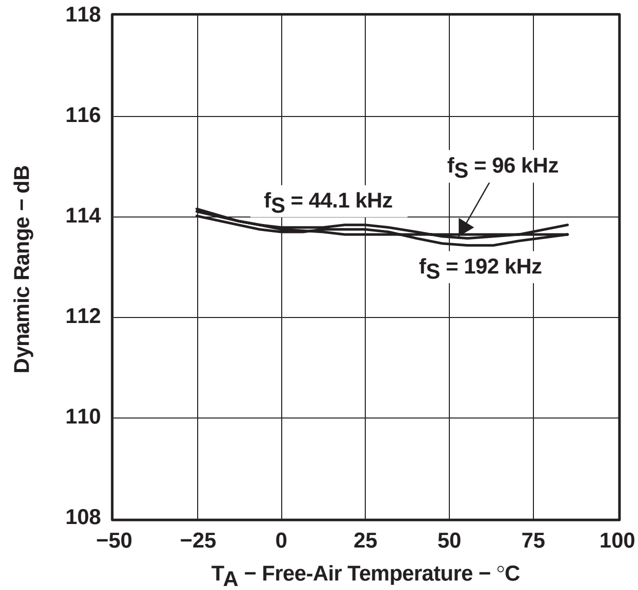



**Figure 16**

SIGNAL-to-NOISE RATIO
vs
FREE-AIR TEMPERATURE

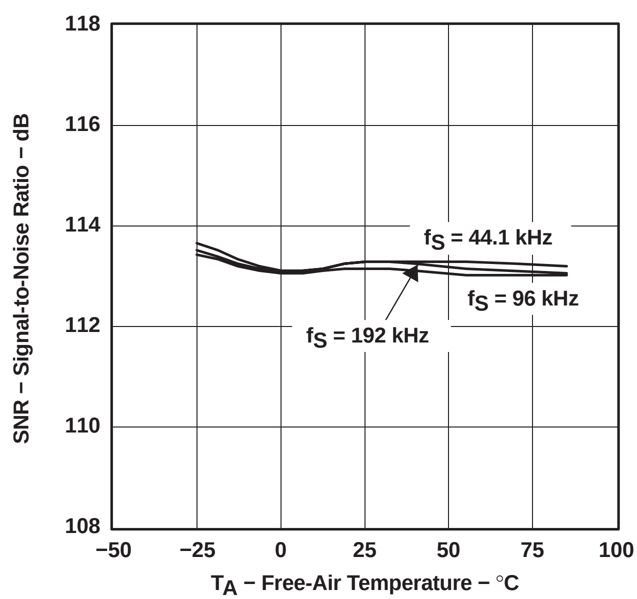



**Figure 17**

CHANNEL SEPARATION
vs
FREE-AIR TEMPERATURE

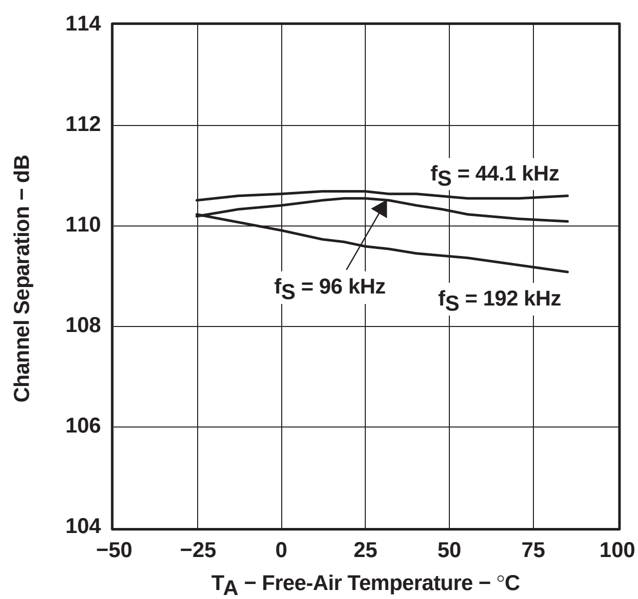



**Figure 18**

NOTE: PCM mode, $V_{DD}$ = 3.3 V, $V_{CC}$ = 5 V.

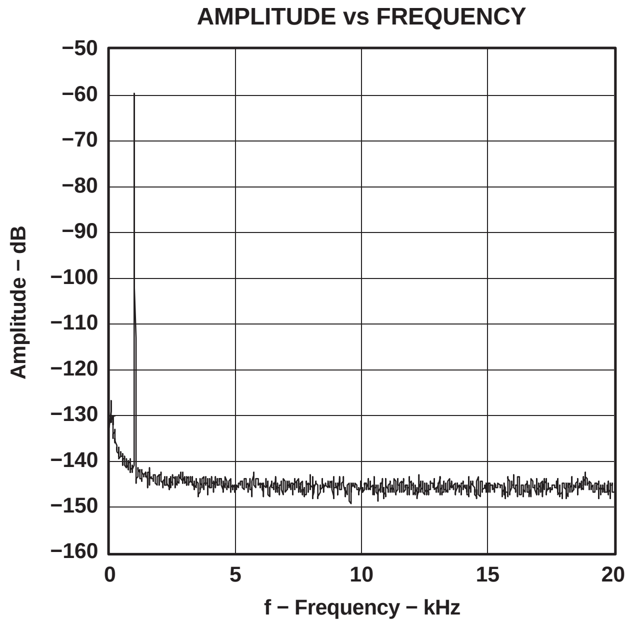



**Figure 19. −60-dB Output Spectrum, BW = 20 kHz**

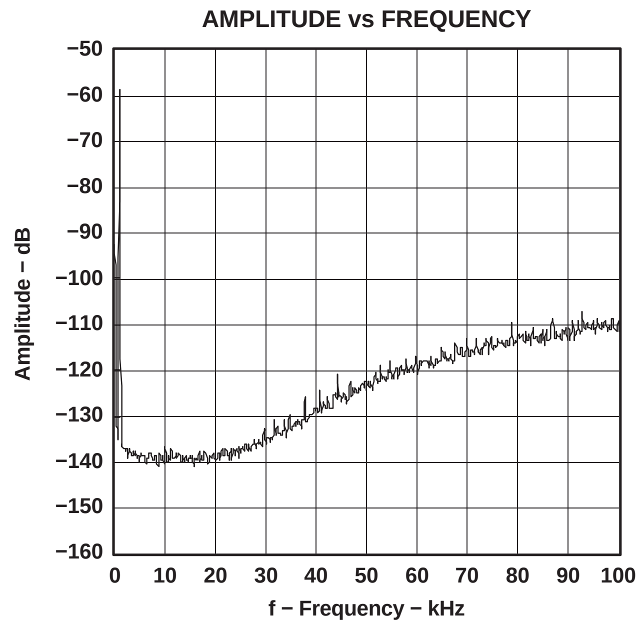



**Figure 20. −60-dB Output Spectrum, BW = 100 kHz**

NOTE: PCM mode, $f_S$ = 44.1 kHz, 32768 points, 8 average, $T_A$ = 25°C, $V_{DD}$ = 3.3 V, $V_{CC}$ = 5 V.

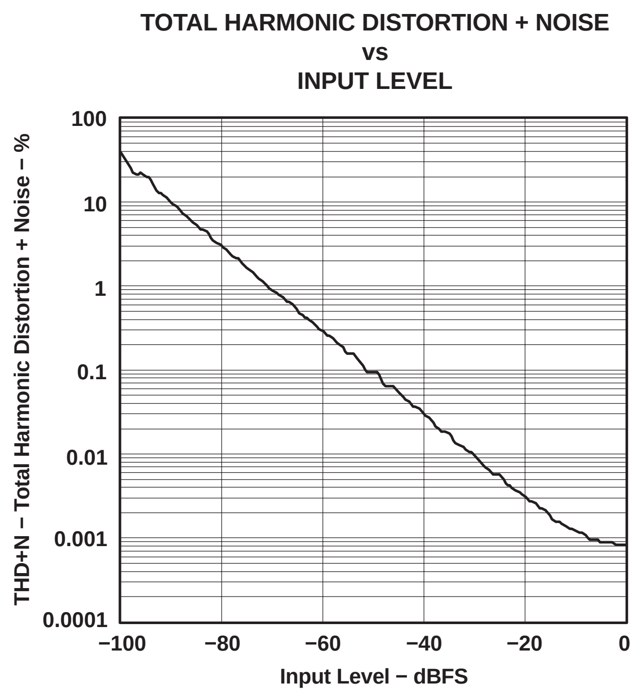



**Figure 21. THD+N vs Input Level, PCM Mode**

NOTE: PCM mode, $f_S$ = 44.1 kHz, $T_A$ = 25°C, $V_{DD}$ = 3.3 V, $V_{CC}$ = 5 V.

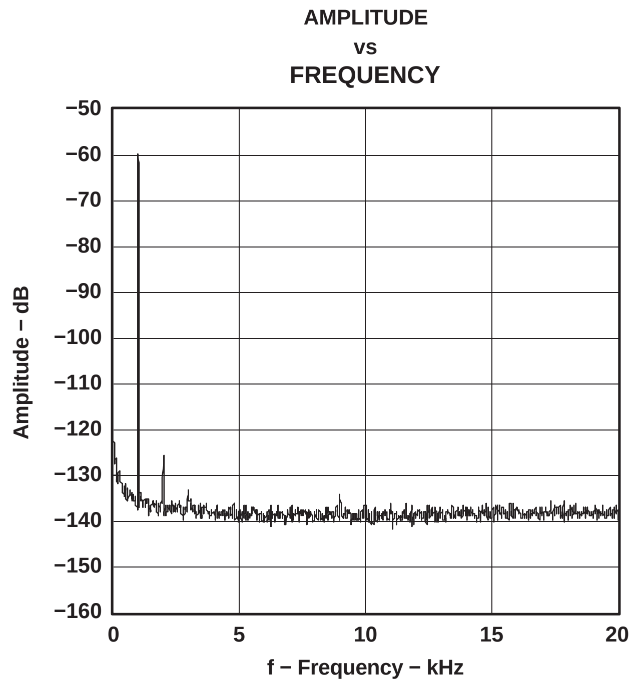



Figure 22. −60-dB Output Spectrum, DSD Mode

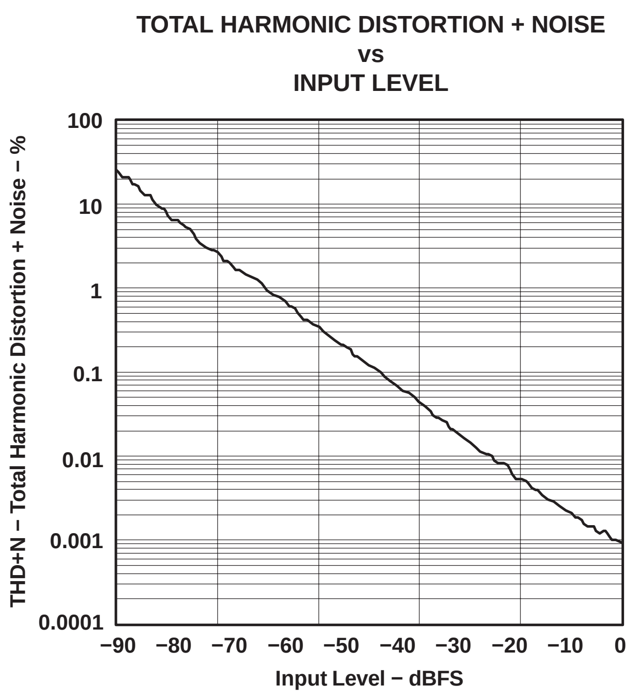



Figure 23. THD+N vs Input Level, DSD Mode

NOTE: DSD mode (FIR-2), $T_A$ = 25°C, $V_{DD}$ = 3.3 V, $V_{CC}$ = 5 V.

# SYSTEM CLOCK AND RESET FUNCTIONS

## System Clock Input

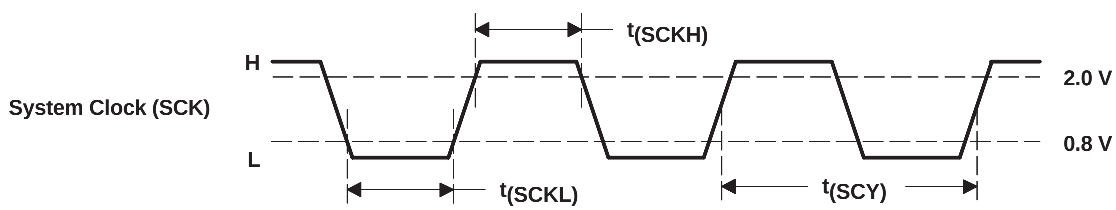
The DSD1793 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 5). The DSD1793 has a system clock detection circuit that automatically senses which frequency the system clock is operating. Table 1 shows examples of system clock frequencies for common audio sampling rates. If the oversampling rate of the delta-sigma modulator is selected as 128 $f_S$, the system clock frequency is over 256 $f_S$.

Figure 24 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. One of the Texas Instruments PLL1700 family of multiclock generators is an excellent choice for providing the DSD1793 system clock.

**Table 1. System Clock Rates for Common Audio Sampling Frequencies**

| SAMPLING FREQUENCY | SYSTEM CLOCK FREQUENCY ($F_{SCK}$) (MHZ) | | | | | |
|---|---|---|---|---|---|---|
| | 128 $f_S$ | 192 $f_S$ | 256 $f_S$ | 384 $f_S$ | 512 $f_S$ | 768 $f_S$ |
| 32 kHz | 4.096 (1) | 6.144 (1) | 8.192 | 12.288 | 16.384 | 24.576 |
| 44.1 kHz | 5.6488 (1) | 8.4672 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 48 kHz | 6.144 (1) | 9.216 | 12.288 | 18.432 | 24.576 | 36.864 |
| 96 kHz | 12.288 | 18.432 | 24.576 | 36.864 | 49.152 (1) | 73.728 (1) |
| 192 kHz | 24.576 | 36.864 | 49.152 (1) | 73.728 (1) | (2) | (2) |

(1) This system clock rate is not supported in $I^2C$ fast mode.
(2) This system clock rate is not supported for the given sampling frequency.




| PARAMETERS | | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{(SCY)}$ | System clock pulse cycle time | 13 | | ns |
| $t_{(SCKH)}$ | System clock pulse duration, HIGH | 5 | | ns |
| $t_{(SCKL)}$ | System clock pulse duration, LOW | 5 | | ns |

**Figure 24. System Clock Input Timing**

## Power-On Reset Function

The DSD1793 includes a power-on reset function. Figure 25 shows the operation of this function. With $V_{DD}$ > 2 V, the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time $V_{DD}$ > 2 V. After the initialization period, the DSD1793 is set to its default reset state, as described in the *MODE CONTROL REGISTERS* section of this data sheet.

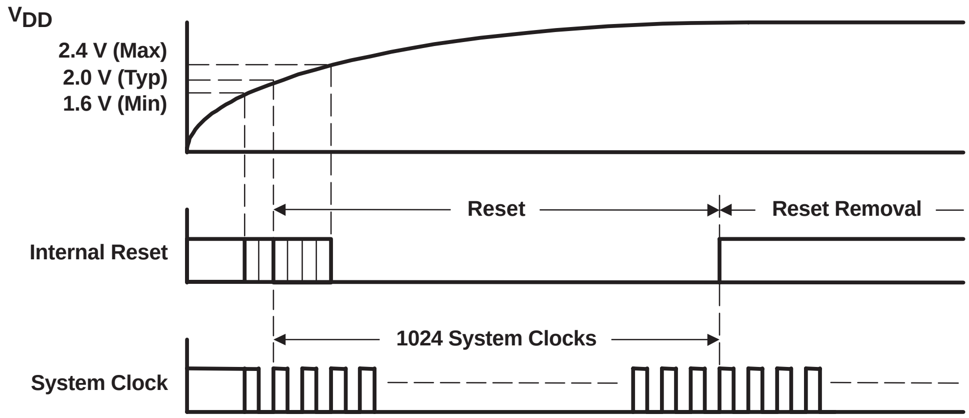



**Figure 25. Power-On Reset Timing**

# AUDIO DATA INTERFACE

## Audio Serial Interface

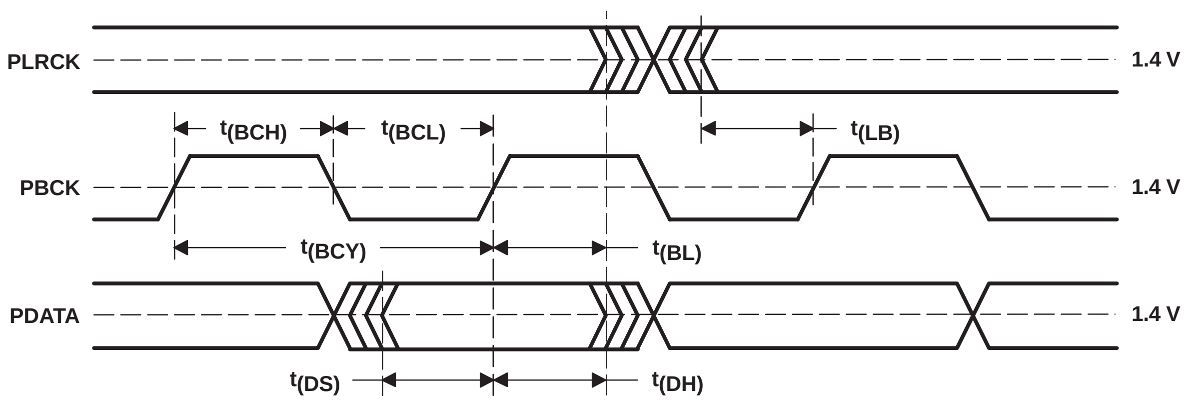
The audio interface port is a 3-wire serial port. It includes PLRCK (pin 1), PBCK (pin 2), and PDATA (pin 3). PBCK is the serial audio bit clock, and it is used to clock the serial data present on PDATA into the serial shift register of the audio interface. Serial data is clocked into the DSD1793 on the rising edge of PBCK. PLRCK is the serial audio left/right word clock.

The DSD1793 requires the synchronization of PLRCK and the system clock, but does not need a specific phase relation between PLRCK and the system clock.

If the relationship between PLRCK and the system clock changes more than ±6 PBCK, internal operation is initialized within $1/f_S$ and analog outputs are forced to the bipolar zero level until resynchronization between PLRCK and the system clock is completed.

## PCM Audio Data Formats and Timing

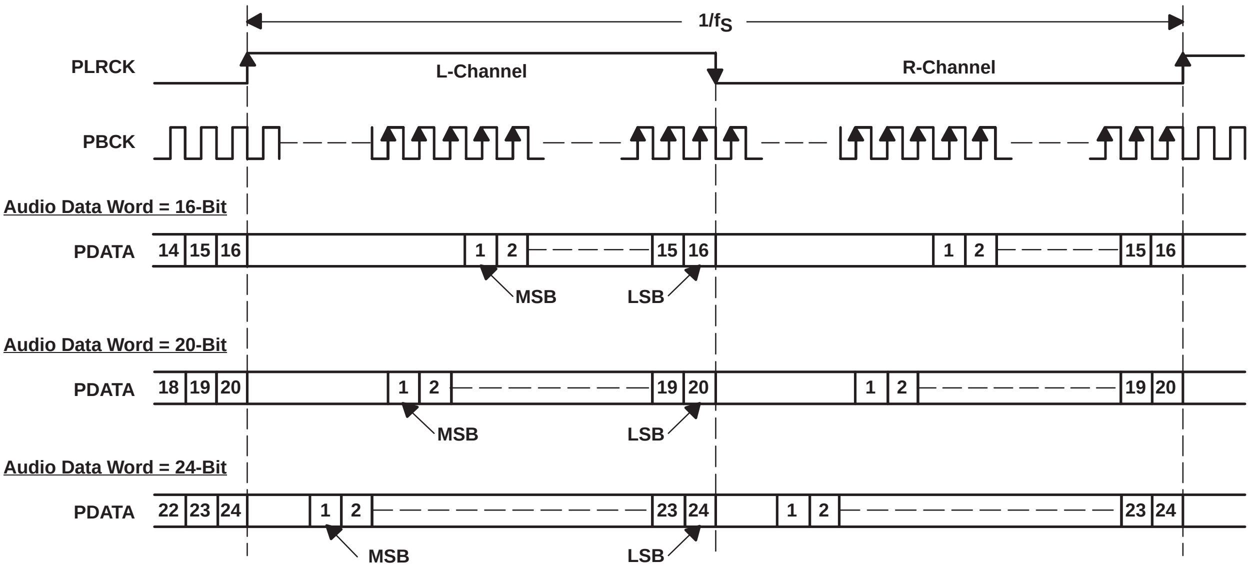
The DSD1793 supports industry-standard audio data formats, including standard right-justified, $I^2S$, and left-justified. The data formats are shown in Figure 27. Data formats are selected using the format bits, FMT[2:0], in control register 18. The default data format is 24-bit $I^2S$. All formats require binary 2s complement, MSB-first audio data. Figure 26 shows a detailed timing diagram for the serial audio interface.



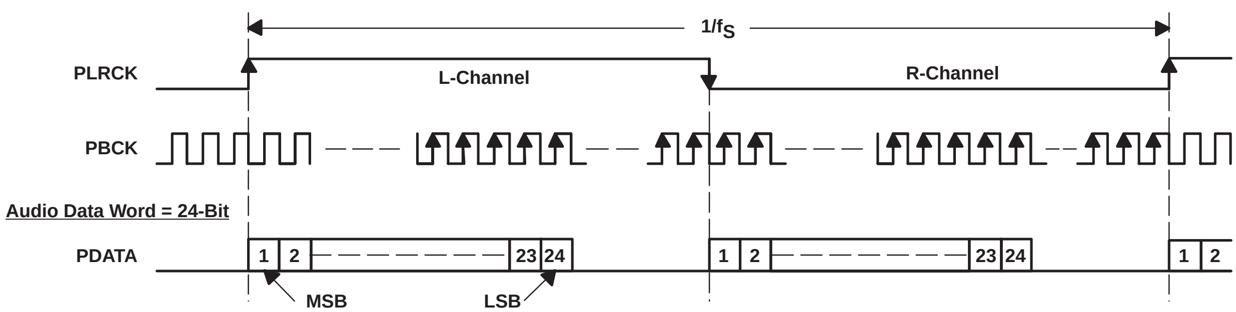

| PARAMETERS | | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{(BCY)}$ | PBCK pulse cycle time | 70 | | ns |
| $t_{(BCL)}$ | PBCK pulse duration, LOW | 30 | | ns |
| $t_{(BCH)}$ | PBCK pulse duration, HIGH | 30 | | ns |
| $t_{(BL)}$ | PBCK rising edge to PLRCK edge | 10 | | ns |
| $t_{(LB)}$ | PLRCK edge to PBCK rising edge | 10 | | ns |
| $t_{(DS)}$ | PDATA setup time | 10 | | ns |
| $t_{(DH)}$ | PDATA hold time | 10 | | ns |
| — | PLRCK clock data | 50% ± 2 bit clocks | | |

**Figure 26. Timing of Audio Interface**

### (1) Standard Data Format (Right Justified) ; L-Channel = HIGH, R-Channel = LOW




### (2) Left Justified Data Format; L-Channel = HIGH, R-Channel = LOW




### (3) I2S Data Format; L-Channel = LOW, R-Channel = HIGH

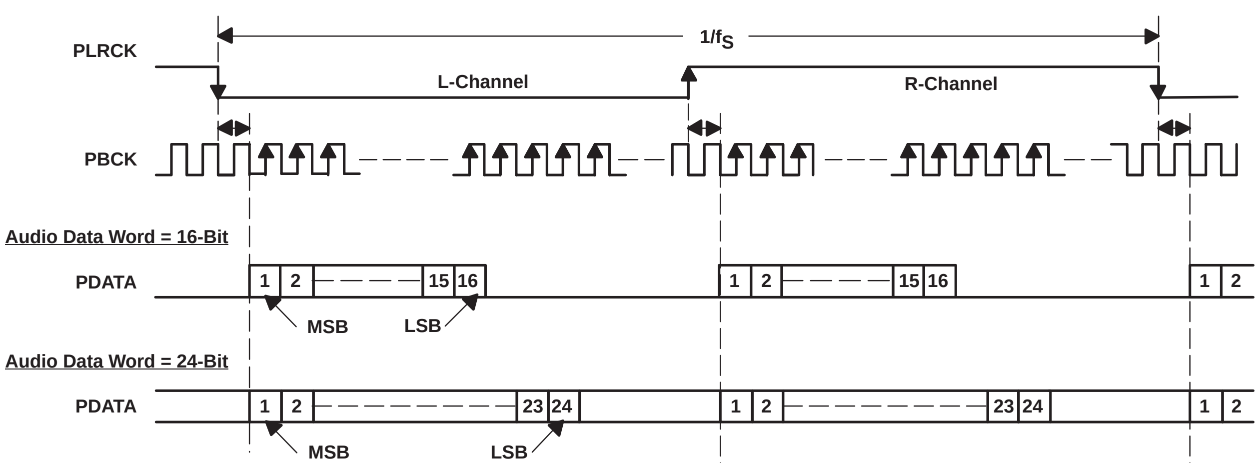



**Figure 27. Audio Data Input Formats**

## External Digital Filter Interface and Timing

The DSD1793 supports an external digital filter interface with a 3- or 4-wire synchronous serial port, which allows the use of an external digital filter. External filters include the Texas Instruments DF1704 and DF1706, the Pacific Microsonics PMD200, or a programmable digital signal processor.

In the external DF mode, PLRCK (pin 1), PBCK (pin 2) and PDATA (pin 3) are defined as WDCK, the word clock; BCK, the bit clock; and DATA, the monaural data, respectively. The external digital filter interface is selected by using the DFTH bit of control register 20, which functions to bypass the internal digital filter of the DSD1793.

When the DFMS bit of control register 19 is set, the DSD1793 can process stereo data. In this case, DSDL (pin 25) and DSDR (pin 24) are defined as L-channel data and R-channel data input, respectively.

Detailed information for the external digital filter interface mode is provided in the *APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE* section of this data sheet.

## Direct Stream Digital (DSD) Format Interface and Timing

The DSD1793 supports the DSD format interface operation, which includes out-of-band noise filtering using an internal analog FIR filter. The DSD format interface consists of a 3-wire synchronous serial port, which includes DBCK (pin 4), DSDL (pin 25), and DSDR (pin 24). DBCK is the serial bit clock. DSDL and DSDR are L-channel and R-channel DSD data input, respectively. They are clocked into the DSD1793 on the rising edge of DBCK. PLRCK (pin 1) and PBCK (pin 2) must be connected to GND in the DSD mode. The DSD format (DSD mode) interface is activated by setting the DSD bit of control register 20.

Detailed information for the DSD mode is provided in the *APPLICATION FOR DSD FORMAT (DSD MODE) INTERFACE* section of this data sheet.

# FUNCTIONAL DESCRIPTIONS

## Zero Detect

The DSD1793 has a zero-detect function. When the DSD1793 detects the zero conditions as shown in Table 2, the DSD1793 sets ZEROL (pin 23) and ZEROR (pin 22) to HIGH.

**Table 2. Zero Conditions**

| MODE | | DETECTING CONDITION AND TIME |
|---|---|---|
| PCM | | DATA is continuously LOW for 1024 LRCKs. |
| External DF mode | | DATA is continuously LOW for 8 × 1024 WDCKs. |
| DSD | DZ0 | There are an equal number of 1s and 0s in every 8 bits of DSD input data for 23 ms. |
| | DZ1 | The input data is 1001 0110 continuously for 23 ms. |

## Serial Control Interface (I²C)

The DSD1793 supports the I²C serial bus and the data transmission protocol for standard and fast mode as a slave device. This protocol is explained in I²C specification 2.0.

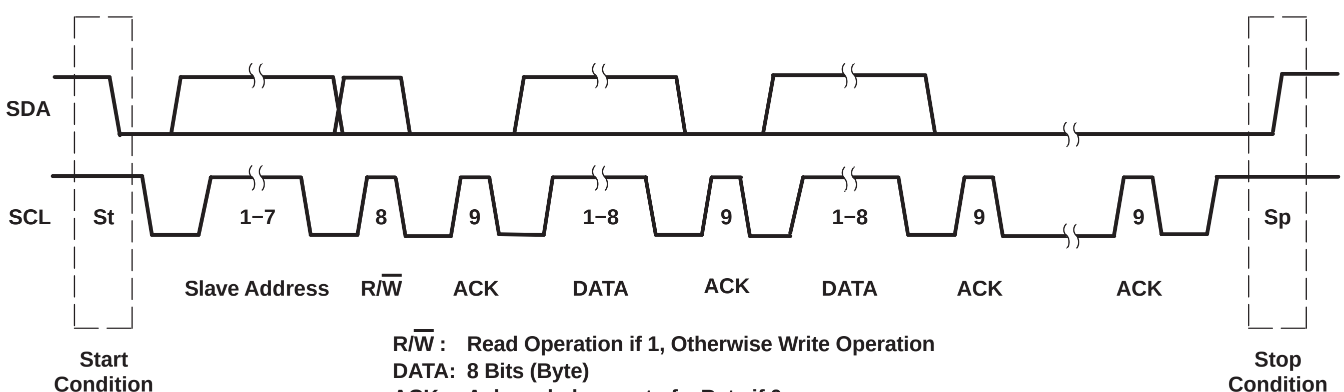
## Slave Address

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | ADR1 | ADR0 | $R/\overline{W}$ |

The DSD1793 has 7 bits for its own slave address. The first five bits (MSBs) of the slave address are factory preset to 10011. The next two bits of the address byte are the device select bits, which can be user-defined by the ADR1 and ADR0 terminals. A maximum of four DSD1793s can be connected on the same bus at one time. Each DSD1793 responds when it receives its own slave address.

## Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The DSD1793 supports only slave receivers and slave transmitters.




$R/\overline{W}$: Read Operation if 1, Otherwise Write Operation
DATA: 8 Bits (Byte)
ACK: Acknowledgement of a Byte if 0
NACK: Not Acknowledgement if 1

Write operation

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Transmitter | *M* | *M* | *M* | *S* | *M* | *S* | *M* | *S* | … | *S* | *M* |
| Data Type | St | Slave address | $\overline{W}$ | ACK | DATA | ACK | DATA | ACK | … | ACK | Sp |

Read operation

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Transmitter | *M* | *M* | *M* | *S* | *S* | *M* | *S* | *M* | … | *M* | *M* |
| Data Type | St | Slave address | R | ACK | DATA | ACK | DATA | ACK | … | NACK | Sp |

NOTE: M: Master device; S: Slave device; St: Start condition
Sp: Stop condition; $\overline{W}$: Write; R: Read

**Figure 28. Basic I²C Framework**

## Write Register

A master can write to any DSD1793 registers using single or multiple accesses. The master sends a DSD1793 slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When the data are received properly, the index register is incremented automatically by 1. When the index register reaches 0x7F, the next value is 0x0. When undefined registers are accessed, the DSD1793 does not send an acknowledgement. Figure 29 is a diagram of the write operation.

| Transmitter | *M* | *M* | *M* | *S* | *M* | *S* | *M* | *S* | *M* | *S* | … | *S* | *M* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Data Type | St | Slave address | $\overline{W}$ | ACK | Register address | ACK | Write data 1 | ACK | Write data 2 | ACK | … | ACK | Sp |

*M*: Master device  *S*: Slave device  St: Start condition
ACK: Acknowledge  Sp: Stop condition  $\overline{W}$: Write

**Figure 29. Write Operation**

## Read Register

A master can read the DSD1793 register. The value of the register address is stored in an indirect index register in advance. The master sends a DSD1793 slave address with a read bit after storing the register address. Then the DSD1793 transfers the data which the index register points to. When the data are transferred during a multiple access, the index register is incremented by 1 automatically. (When first going into read mode immediately following a write, the index register is not incremented. The master can read the register that was previously written.) When the index register reaches 0x7F, the next value is 0x0. The DSD1793 outputs some data when the index register is 0x10 to 0x1F, even if it is not defined in Table 4. Figure 30 is a diagram of the read operation.

| Transmitter | *M* | *M* | *M* | *S* | *M* | *S* | *M* | *M* | *M* | *S* | *S* | *M* | … | *M* | *M* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Data Type | St | Slave address | $\overline{W}$ | ACK | Register address | ACK | Sr | Slave address | R | ACK | Data | ACK | … | NACK | Sp |

*M*: Master device  *S*: Slave device  St: Start condition  Sr: Repeated start condition
ACK: Acknowledge  Sp: Stop condition  NACK: Not Acknowledge  $\overline{W}$: Write  R: Read

NOTE: The slave address after the repeat start condition must be the same as the previous slave address.

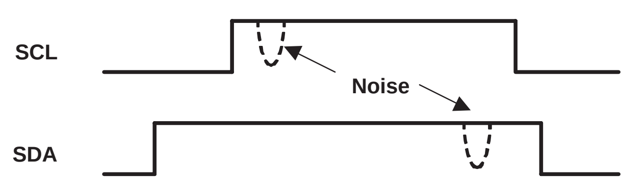
**Figure 30. Read Operation**

## Noise Suppression

The DSD1793 incorporates noise suppression using the system clock (SCK). However, there must be no more than two noise spikes in 600 ns. The noise suppression works for SCK frequencies between 8 MHz and 40 MHz in fast mode. However, it works incorrectly in the particular following conditions.

### Case 1:

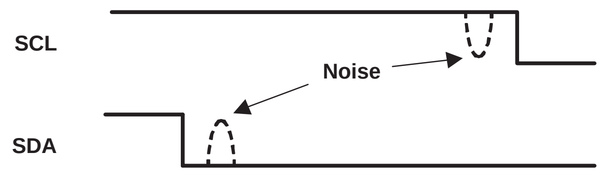
1. $t_{(SCK)}$ > 120 ns ($t_{(SCK)}$: period of SCK)
2. $t_{(HI)} + t_{(D-HD)} < t_{(SCK)} \times 5$
3. Spike noise exists on the first half of the SCL HIGH pulse.
4. Spike noise exists on the SDA HIGH pulse just before SDA goes LOW.




When these conditions occur at the same time, the data is recognized as LOW.

**Case 2:**

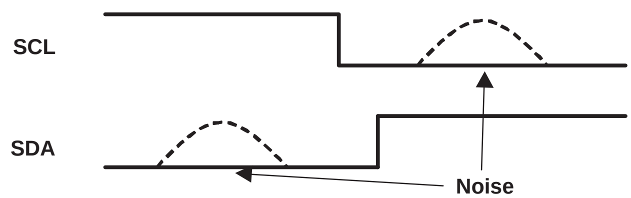
1. $t_{(SCK)}$ > 120 ns
2. $t_{(S-HD)}$ or $t_{(RS-HD)} < t_{(SCK)} \times 5$
3. Spike noise exists on both SCL and SDA during the hold time.




When these conditions occur at the same time, the DSD1793 fails to detect a start condition.

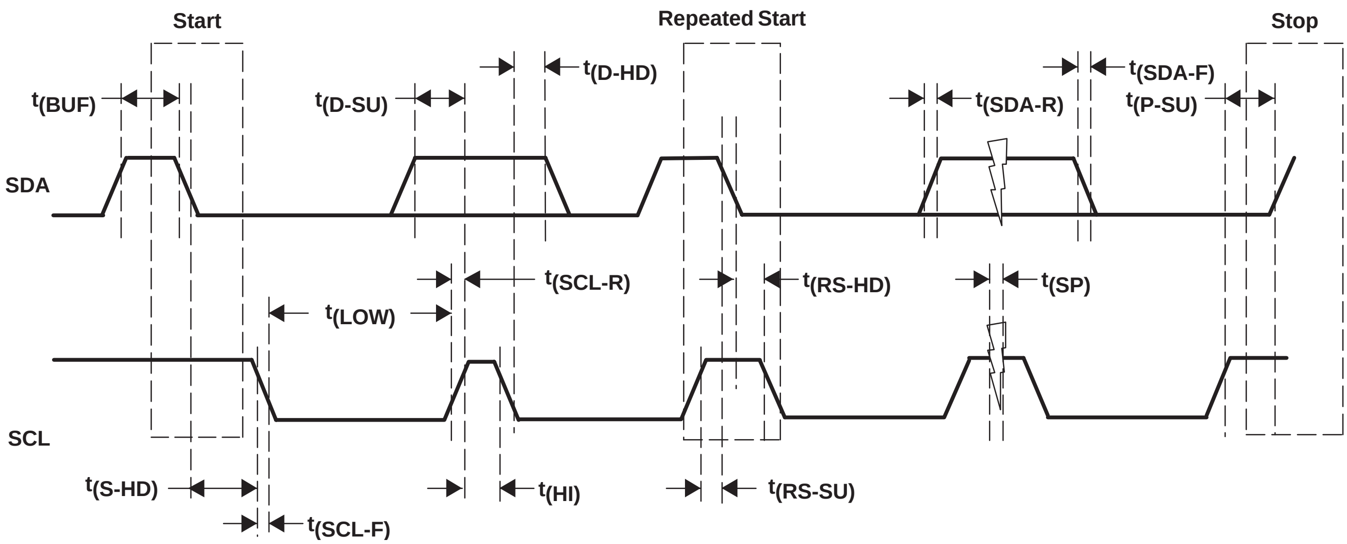
**Case 3:**

1. $t_{(SCK)}$ < 50 ns
2. $t_{(SP)} > t_{(SCK)}$
3. Spike noise exists on SCL just after SCL goes LOW.
4. Spike noise exists on SDA just before SCL goes LOW.




When these conditions occur at the same time, the DSD1793 erroneously detects a start or stop condition.

## TIMING DIAGRAM




## TIMING CHARACTERISTICS

| PARAMETER | | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{(SCL)}$ | SCL clock frequency | Standard | | 100 | kHz |
| | | Fast | | 400 | |
| $t_{(BUF)}$ | Bus free time between stop and start conditions | Standard | 4.7 | | µs |
| | | Fast | 1.3 | | |
| $t_{(LOW)}$ | Low period of the SCL clock | Standard | 4.7 | | µs |
| | | Fast | 1.3 | | |
| $t_{(HI)}$ | High period of the SCL clock | Standard | 4 | | µs |
| | | Fast | 600 | | ns |
| $t_{(RS-SU)}$ | Setup time for (repeated) start condition | Standard | 4.7 | | µs |
| | | Fast | 600 | | ns |
| $t_{(S-HD)}$<br>$t_{(RS-HD)}$ | Hold time for (repeated) start condition | Standard | 4 | | µs |
| | | Fast | 600 | | ns |
| $t_{(D-SU)}$ | Data setup time | Standard | 250 | | ns |
| | | Fast | 100 | | |
| $t_{(D-HD)}$ | Data hold time | Standard | 0 | 900 | ns |
| | | Fast | 0 | 900 | |
| $t_{(SCL-R)}$ | Rise time of SCL signal | Standard | $20 + 0.1\ C_B$ | 1000 | ns |
| | | Fast | $20 + 0.1\ C_B$ | 300 | |
| $t_{(SCL-R1)}$ | Rise time of SCL signal after a repeated start condition and after an acknowledge bit | Standard | $20 + 0.1\ C_B$ | 1000 | ns |
| | | Fast | $20 + 0.1\ C_B$ | 300 | |
| $t_{(SCL-F)}$ | Fall time of SCL signal | Standard | $20 + 0.1\ C_B$ | 1000 | ns |
| | | Fast | $20 + 0.1\ C_B$ | 300 | |
| $t_{(SDA-R)}$ | Rise time of SDA signal | Standard | $20 + 0.1\ C_B$ | 1000 | ns |
| | | Fast | $20 + 0.1\ C_B$ | 300 | |
| $t_{(SDA-F)}$ | Fall time of SDA signal | Standard | $20 + 0.1\ C_B$ | 1000 | ns |
| | | Fast | $20 + 0.1\ C_B$ | 300 | |
| $t_{(P-SU)}$ | Setup time for stop condition | Standard | 4 | | µs |
| | | Fast | 600 | | ns |
| $C_{(B)}$ | Capacitive load for SDA and SCL line | | | 400 | pF |
| $t_{(SP)}$ | Pulse duration of suppressed spike | Fast | | 50 | ns |
| $V_{NH}$ | Noise margin at high level for each connected device (including hysteresis) | | $0.2\ V_{DD}$ | | V |

# MODE CONTROL REGISTERS

## User-Programmable Mode Controls

The DSD1793 includes a number of user-programmable functions which are accessed via mode control registers. The registers are programmed using the serial control interface, which was previously discussed in this data sheet. Table 3 lists the available mode-control functions, along with their default reset conditions and associated register index.

**Table 3. User-Programmable Function Controls**

| FUNCTION | DEFAULT | REGISTER | BIT | PCM | DSD | DF BYPASS |
|---|---|---|---|---|---|---|
| Digital attenuation control<br>0 dB to –120 dB and mute, 0.5 dB step | 0 dB | Register 16<br>Register 17 | ATL[7:0] (for L-ch)<br>ATR[7:0] (for R-ch) | yes | | |
| Attenuation load control—Disabled, enabled | Attenuation disabled | Register 18 | ATLD | yes | | |
| Input audio data format selection<br>16-, 20-, 24-bit standard (right-justified) format<br>24-bit MSB-first left-justified format<br>16-/24-bit $I^2S$ format | 24-bit $I^2S$ format | Register 18 | FMT[2:0] | yes | | yes |
| Sampling rate selection for de-emphasis<br>Disabled,44.1 kHz, 48 kHz, 32 kHz | De-emphasis disabled | Register 18 | DMF[1:0] | yes | yes(1) | |
| De-emphasis control—Disabled, enabled | De-emphasis disabled | Register 18 | DME | yes | | |
| Soft mute control—Mute disabled, enabled | Mute disabled | Register 18 | MUTE | yes | | |
| Output phase reversal—Normal, reverse | Normal | Register 19 | REV | yes | yes | yes |
| Attenuation speed selection<br>$\times 1\ f_S$, $\times(1/2)f_S$, $\times(1/4)f_S$, $\times(1/8)f_S$ | $\times 1\ f_S$ | Register 19 | ATS[1:0] | yes | | |
| DAC operation control—Enabled, disabled | DAC operation enabled | Register 19 | OPE | yes | yes | yes |
| Stereo DF bypass mode select<br>Monaural, stereo | Monaural | Register 19 | DFMS | | | yes |
| Digital filter rolloff selection<br>Sharp rolloff, slow rolloff | Sharp rolloff | Register 19 | FLT | yes | | |
| Infinite zero mute control<br>Disabled, enabled | Disabled | Register 19 | INZD | yes | | yes |
| System reset control<br>Reset operation , normal operation | Normal operation | Register 20 | SRST | yes | yes | yes |
| DSD interface mode control<br>DSD enabled, disabled | Disabled | Register 20 | DSD | yes | yes | |
| Digital-filter bypass control<br>DF enabled, DF bypass | DF enabled | Register 20 | DFTH | yes | | yes |
| Monaural mode selection<br>Stereo, monaural | Stereo | Register 20 | MONO | yes | yes | yes |
| Channel selection for monaural mode data<br>L-channel, R-channel | L-channel | Register 20 | CHSL | yes | yes | yes |
| Delta-sigma oversampling rate selection<br>$\times 64\ f_S$, $\times 128\ f_S$, $\times 32\ f_S$ | $\times 64\ f_S$ | Register 20 | OS[1:0] | yes | yes(2) | yes |
| PCM zero output enable | Enabled | Register 21 | PCMZ | yes | | yes |
| DSD zero output enable | Disabled | Register 21 | DZ[1:0] | | yes | |
| Function Available Only For Read | | | | | | |
| Zero detection flag<br>Not zero, zero detected | Not zero = 0<br>Zero detected = 1 | Register 22 | ZFGL (for L-ch)<br>ZFGR (for R-ch) | yes | yes | yes |

(1) When in DSD mode, DMF[1:0] is defined as DSD filter (analog FIR) performance selection.
(2) When in DSD mode, OS[1:0] is defined as DSD filter (analog FIR) operation rate selection.

## Register Map

The mode control register map is shown in Table 4. Registers 16–21 include an $R/\overline{W}$ bit, which determines whether a register read ($R/\overline{W}$ = 1) or write ($R/\overline{W}$ = 0) operation is performed. Register 22 is read-only.

**Table 4. Mode Control Register Map**

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register 16 | $R/\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | ATL7 | ATL6 | ATL5 | ATL4 | ATL3 | ATL2 | ATL1 | ATL0 |
| Register 17 | $R/\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 0 | 1 | ATR7 | ATR6 | ATR5 | ATR4 | ATR3 | ATR2 | ATR1 | ATR0 |
| Register 18 | $R/\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 1 | 0 | ATLD | FMT2 | FMT1 | FMT0 | DMF1 | DMF0 | DME | MUTE |
| Register 19 | $R/\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 1 | 1 | REV | ATS1 | ATS0 | OPE | RSV | DFMS | FLT | INZD |
| Register 20 | $R/\overline{W}$ | 0 | 0 | 1 | 0 | 1 | 0 | 0 | RSV | SRST | DSD | DFTH | MONO | CHSL | OS1 | OS0 |
| Register 21 | $R/\overline{W}$ | 0 | 0 | 1 | 0 | 1 | 0 | 1 | RSV | RSV | RSV | RSV | RSV | DZ1 | DZ0 | PCMZ |
| Register 22 | R | 0 | 0 | 1 | 0 | 1 | 1 | 0 | RSV | RSV | RSV | RSV | RSV | RSV | ZFGR | ZFGL |

## Register Definitions

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register 16 | $R/\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | ATL7 | ATL6 | ATL5 | ATL4 | ATL3 | ATL2 | ATL1 | ATL0 |
| Register 17 | $R/\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 0 | 1 | ATR7 | ATR6 | ATR5 | ATR4 | ATR3 | ATR2 | ATR1 | ATR0 |

### $R/\overline{W}$: Read/Write Mode Select

When $R/\overline{W}$ = 0, a write operation is performed.

When $R/\overline{W}$ = 1, a read operation is performed.

Default value: 0

### ATx[7:0]: Digital Attenuation Level Setting

These bits are available for read and write.

Default value: 1111 1111b

Each DAC output has a digital attenuator associated with it. The attenuator can be set from 0 dB to –120 dB, in 0.5-dB steps. Alternatively, the attenuator can be set to infinite attenuation (or mute).

The attenuation data for each channel can be set individually. However, the data load control (the ATLD bit of control register 18) is common to both attenuators. ATLD must be set to 1 in order to change an attenuator setting. The attenuation level can be set using the following formula:

$$\text{Attenuation level (dB)} = 0.5\text{ dB} \bullet (\text{ATx[7:0]}_{DEC} - 255)$$

where $\text{ATx[7:0]}_{DEC}$ = 0 through 255

For $\text{ATx[7:0]}_{DEC}$ = 0 through 14, the attenuator is set to infinite attenuation. The following table shows attenuation levels for various settings:

| ATx[7:0] | Decimal Value | Attenuation Level Setting |
|---|---|---|
| 1111 1111b | 255 | 0 dB, no attenuation (default) |
| 1111 1110b | 254 | –0.5 dB |
| 1111 1101b | 253 | –1.0 dB |
| ⋮ | ⋮ | ⋮ |
| 0001 0000b | 16 | –119.5 dB |
| 0000 1111b | 15 | –120.0 dB |
| 0000 1110b | 14 | Mute |
| ⋮ | ⋮ | ⋮ |
| 0000 0000b | 0 | Mute |

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register 18 | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 1 | 0 | ATLD | FMT2 | FMT1 | FMT0 | DMF1 | DMF0 | DME | MUTE |

**R/$\overline{W}$: Read/Write Mode Select**

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

**ATLD: Attenuation Load Control**

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| ATLD = 0 | Attenuation control disabled (default) |
| ATLD = 1 | Attenuation control enabled |

The ATLD bit enables loading of the attenuation data contained in registers 16 and 17. When ATLD = 0, the attenuation settings remain at the previously programmed levels, ignoring new data loaded from registers 16 and 17. When ATLD = 1, attenuation data written to registers 16 and 17 is loaded normally.

**FMT[2:0]: Audio Interface Data Format**

These bits are available for read and write.

Default value: 101

| FMT[2:0] | Audio Data Format Selection |
|---|---|
| 000 | 16-bit standard format, right-justified data |
| 001 | 20-bit standard format, right-justified data |
| 010 | 24-bit standard format, right-justified data |
| 011 | 24-bit MSB-first, left-justified format data |
| 100 | 16-bit $I^2S$-format data |
| 101 | 24-bit $I^2S$-format data (default) |
| 110 | Reserved |
| 111 | Reserved |

The FMT[2:0] bits select the data format for the serial audio interface.

For the external digital filter interface mode (DFTH mode), this register is operated as shown in the *APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE* section of this data sheet.

**DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function**

These bits are available for read and write.

Default value: 00

| DMF[1:0] | De-Emphasis Sampling Frequency Selection |
|---|---|
| 00 | Disabled (default) |
| 01 | 48 kHz |
| 10 | 44.1 kHz |
| 11 | 32 kHz |

The DMF[1:0] bits select the sampling frequency used by the digital de-emphasis function when it is enabled by setting the DME bit. The de-emphasis curves are shown in the *TYPICAL PERFORMANCE CURVES* section of this data sheet.

For the DSD mode, analog FIR filter performance can be selected using this register. A register map and filter response plots are shown in the *APPLICATION FOR DSD FORMAT (DSD MODE) INTERFACE* section of this data sheet.

### DME: Digital De-Emphasis Control

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| DME = 0 | De-emphasis disabled (default) |
| DME = 1 | De-emphasis enabled |

The DME bit enables or disables the de-emphasis function for both channels.

### MUTE: Soft Mute Control

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| MUTE = 0 | MUTE disabled (default) |
| MUTE = 1 | MUTE enabled |

The MUTE bit enables or disables the soft mute function for both channels.

Soft mute is operated as a 256-step attenuator. The speed for each step to –∞ dB (mute) is determined by the attenuation rate selected in the ATS register.

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register 19 | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 1 | 1 | REV | ATS1 | ATS0 | OPE | RSV | DFMS | FLT | INZD |

### R/$\overline{W}$: Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

### REV: Output Phase Reversal

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| REV = 0 | Normal output (default) |
| REV = 1 | Inverted output |

The REV bit inverts the output phase for both channels.

### ATS[1:0]: Attenuation Rate Select

These bits are available for read and write.

Default value: 00

| ATS[1:0] | Attenuation Rate Selection |
|---|---|
| 00 | Every PLRCK (default) |
| 01 | PLRCK/2 |
| 10 | PLRCK/4 |
| 11 | PLRCK/8 |

The ATS[1:0] bits select the rate at which the attenuator is decremented/incremented during level transitions.

### OPE: DAC Operation Control

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| OPE = 0 | DAC operation enabled (default) |
| OPE = 1 | DAC operation disabled |

The OPE bit enables or disables the analog output for both channels. Disabling the analog outputs forces them to the bipolar zero level (BPZ) even if digital audio data is present on the input.

### DFMS: Stereo DF Bypass Mode Select

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| DFMS = 0 | Monaural (default) |
| DFMS = 1 | Stereo input enabled |

The DFMS bit enables stereo operation in the DF bypass mode. In the DF bypass mode, when DFMS is set to 0, the pin for the input data is PDATA (pin 3) only, therefore the DSD1793 operates as a monaural DAC. When DFMS is set to 1, the DSD1793 can operate as a stereo DAC with inputs of L-channel and R-channel data on DSDL (pin 25) and DSDR (pin 24), respectively.

### FLT: Digital Filter Rolloff Control

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| FLT = 0 | Sharp rolloff (default) |
| FLT = 1 | Slow rolloff |

The FLT bit selects the digital filter rolloff characteristic. The filter responses for these selections are shown in the *TYPICAL PERFORMANCE CURVES* section of this data sheet.

### INZD: Infinite Zero Detect Mute Control

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| INZD = 0 | Infinite zero detect mute disabled (default) |
| INZD = 1 | Infinite zero detect mute enabled |

The INZD bit enables or disables the zero detect mute function. Setting INZD to 1 forces muted analog outputs to hold a bipolar zero level when the DSD1793 detects zero condition in both channels. The infinite zero detect mute function is not available in the DSD mode.

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register 20 | R/$\overline{\text{W}}$ | 0 | 0 | 1 | 0 | 1 | 0 | 0 | RSV | SRST | DSD | DFTH | MONO | CHSL | OS1 | OS0 |

### R/$\overline{\text{W}}$: Read/Write Mode Select

When R/$\overline{\text{W}}$ = 0, a write operation is performed.

When R/$\overline{\text{W}}$ = 1, a read operation is performed.

Default value: 0

**SRST: System Reset Control**

This bit is available for write only.

Default value: 0

| | |
|---|---|
| SRST = 0 | Normal operation (default) |
| SRST = 1 | System reset operation (generate one reset pulse) |

The SRST bit resets the DSD1793 to the initial system condition.

**DSD: DSD Interface Mode Control**

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| DSD = 0 | DSD interface mode disabled (default) |
| DSD = 1 | DSD interface mode enabled |

The DSD bit enables or disables the DSD interface mode.

**DFTH: Digital Filter Bypass (or Through Mode) Control**

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| DFTH = 0 | Digital filter enabled (default) |
| DFTH = 1 | Digital filter bypassed for the external digital filter |

The DFTH bit enables or disables the external digital filter interface mode.

**MONO: Monaural Mode Selection**

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| MONO = 0 | Stereo mode (default) |
| MONO = 1 | Monaural mode |

The MONO function changes the operation mode from the normal stereo mode to the monaural mode. When the monaural mode is selected, both DACs operate in a balanced mode for one channel of audio input data. Channel selection is available for L-channel or R-channel data, determined by the CHSL bit as described immediately following.

**CHSL: Channel Selection for Monaural Mode**

This bit is available for read and write.

Default value: 0

| | |
|---|---|
| CHSL = 0 | L-channel selected (default) |
| CHSL = 1 | R-channel selected |

This bit is available when MONO = 1.

The CHSL bit selects L-channel or R-channel data to be used in monaural mode.

### OS[1:0]: Delta-Sigma Oversampling Rate Selection

These bits are available for read and write.

Default value: 00

| OS[1:0] | Operation Speed Select |
|---|---|
| 00 | 64 times $f_S$ (default) |
| 01 | 32 times $f_S$ |
| 10 | 128 times $f_S$ |
| 11 | Reserved |

The OS bits change the oversampling rate of delta-sigma modulation. Use of this function enables the designer to stabilize the conditions at the post low-pass filter for different sampling rates. As an application example, programming to set 128 times in 44.1-kHz operation, 64 times in 96-kHz operation, and 32 times in 192-kHz operation allows the use of only a single type (cutoff frequency) of post low-pass filter. The 128 $f_S$ oversampling rate is not available at sampling rates above 100 kHz. If the 128 $f_S$ oversampling rate is selected, a system clock of more than 256 $f_S$ is required.

In DSD mode, these bits select the speed of the bit clock for DSD data coming into the analog FIR filter.

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register 21 | $R/\overline{W}$ | 0 | 0 | 1 | 0 | 1 | 0 | 1 | RSV | RSV | RSV | RSV | RSV | DZ1 | DZ0 | PCMZ |

### $R/\overline{W}$: Read/Write Mode Select

When $R/\overline{W}$ = 0, a write operation is performed.

When $R/\overline{W}$ = 1, a read operation is performed.

Default value: 0

### DZ[1:0]: DSD Zero Output Enable

These bits are available for read and write.

Default value: 00

| DZ[1:0] | Zero Output Enable |
|---|---|
| 00 | Disabled (default) |
| 01 | Even pattern detect |
| 1x | $96_H$ pattern detect |

The DZ bits enable or disable the output zero flags, and select the zero pattern in the DSD mode.

### PCMZ: PCM Zero Output Enable

This bit is available for read and write.

Default value: 1

| | |
|---|---|
| PCMZ = 0 | PCM zero output disabled |
| PCMZ = 1 | PCM zero output enabled (default) |

The PCMZ bit enables or disables the output zero flags in the PCM mode and the external DF mode.

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register 22 | R | 0 | 0 | 1 | 0 | 1 | 1 | 0 | RSV | RSV | RSV | RSV | RSV | RSV | ZFGR | ZFGL |

### R: Read Mode Select

Value is always 1, specifying the readback mode.

### ZFGx: Zero-Detection Flag

Where x = L or R, corresponding to the DAC output channel. These bits are available only for readback.

Default value: 00

| | |
|---|---|
| ZFGx = 0 | Not zero |
| ZFGx = 1 | Zero detected |

These bits show zero conditions. Their status is the same as that of the zero flags on ZEROL (pin 23) and ZEROR (pin 22). See *Zero Detect* in the *FUNCTIONAL DESCRIPTIONS* section of this data sheet.

## TYPICAL CONNECTION DIAGRAM

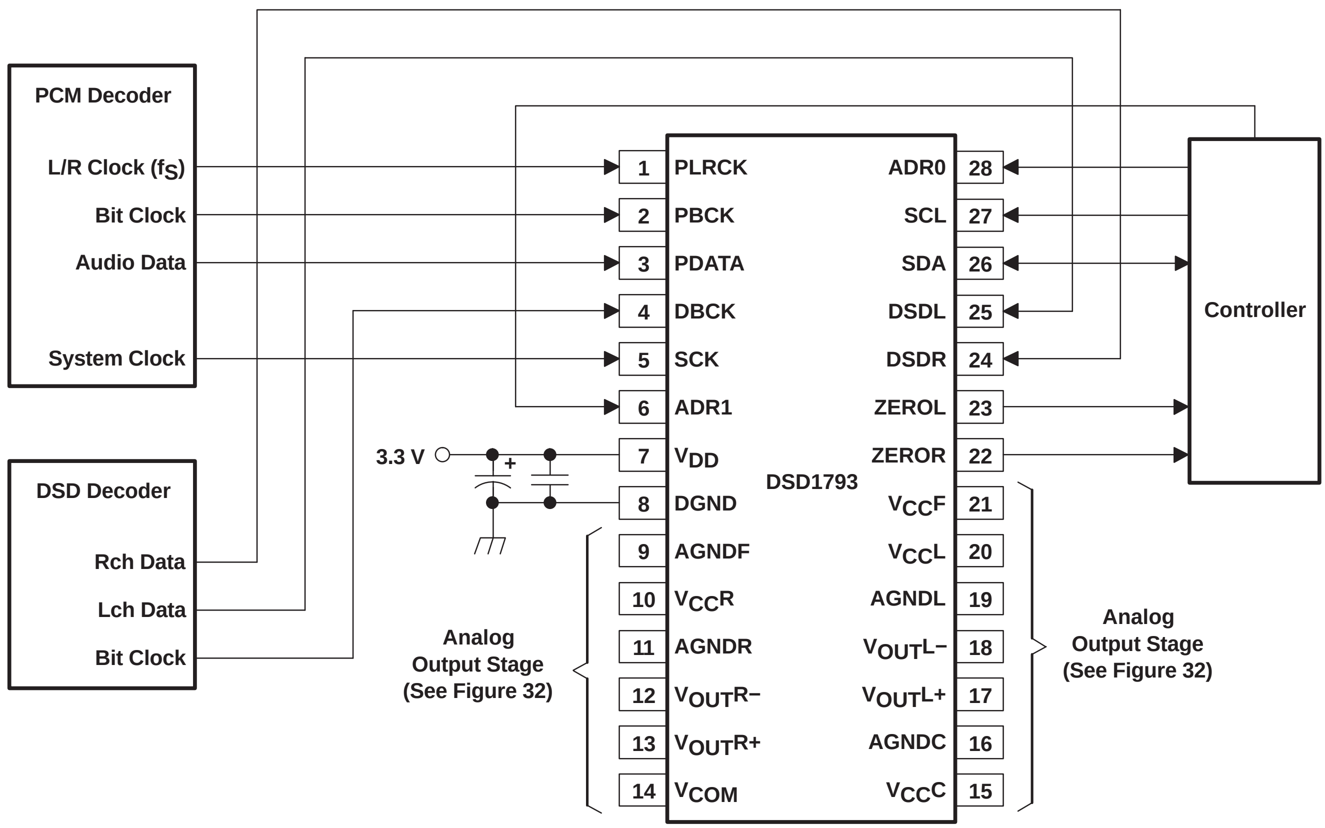
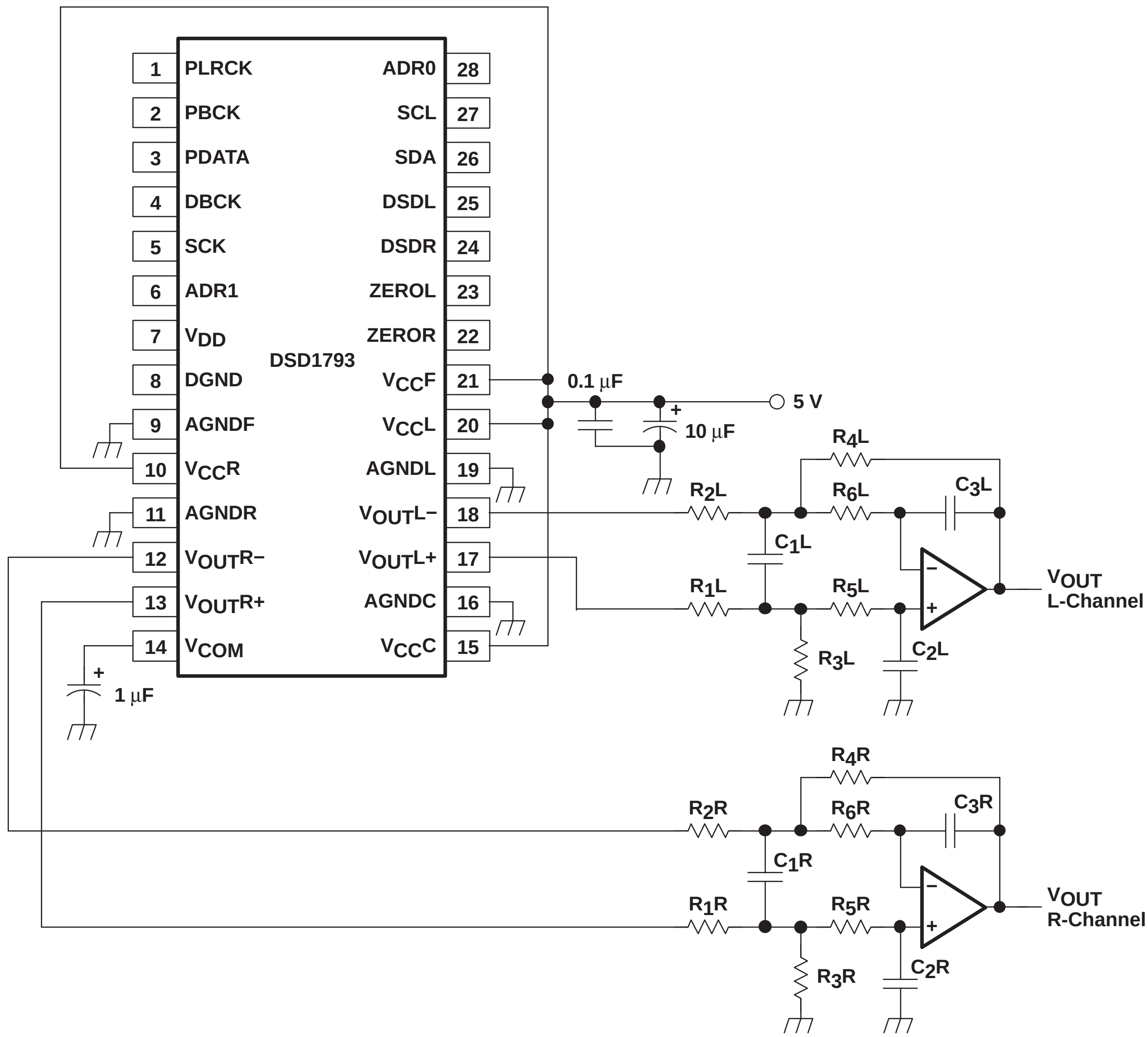



**Figure 31. Typical Application Circuit**

## APPLICATION INFORMATION

## ANALOG OUTPUTS




NOTE: Example R and C values for $f_C$ = 77 kHz – $R_1$, $R_2$: 1.8 kΩ, $R_3$,$R_4$: 3.3 kΩ, $R_5$,$R_6$: 680 Ω, $C_1$: 1800 pF, $C_2$, $C_3$: 560 pF.

**Figure 32. Typical Application for Analog Output Stage**

### Analog Output Level and LPF

The signal level of the DAC differential-voltage output {($V_{OUT}$L+)–($V_{OUT}$L–), ($V_{OUT}$R+)–($V_{OUT}$R–)} is 3.2 V p-p at 0 dB (full scale). The voltage output of the LPF is given by following equation:

$V_{OUT}$ = 3.2 V p-p × ($R_f$/$R_i$)

Here, $R_f$ is the feedback resistor in the LPF, and $R_3$ = $R_4$ in a typical application circuit. $R_i$ is the input resistor in the LPF, and $R_1$ = $R_2$ in a typical application circuit.

### Op Amp for LPF

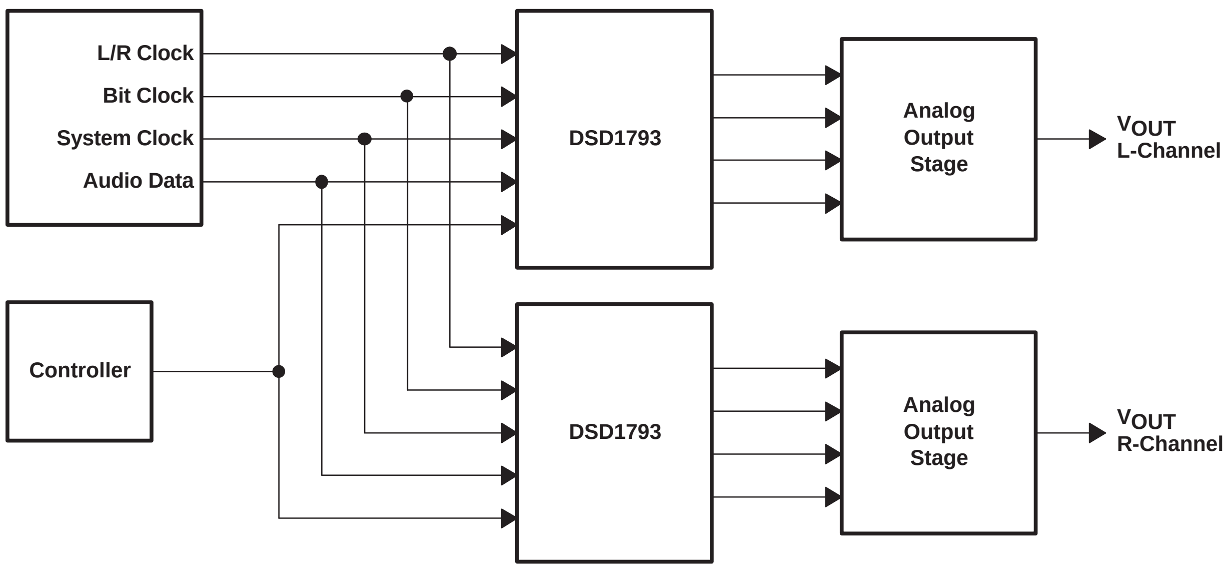
An OPA2134 or 5532 type op amp is recommended for the LPF circuit to obtain the specified audio performance. Dynamic performance such as gain bandwidth, settling time, and slew rate of the op amp largely determines the audio dynamic performance of the LPF section. The input noise specification of the op amp should be considered to obtain a 113-dB S/N ratio.

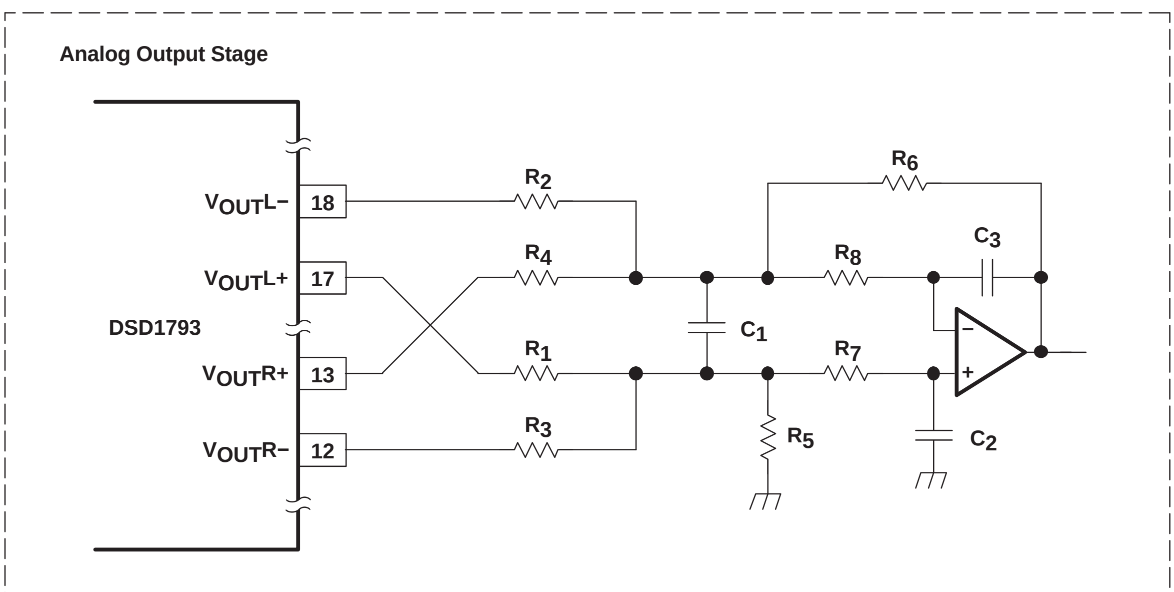
### Analog Gain of Balanced Amplifier

The DAC voltage outputs are followed by balanced amplifier stages, which sum the differential signals for each channel, creating a single-ended voltage output. In addition, the balanced amplifiers provide a third-order low-pass filter function, which band limits the audio output signal. The cutoff frequency and gain are determined by external R and C component values. In this case, the cutoff frequency is 77 kHz with a gain of 1.83. The output voltage for each channel is 5.9 V p-p, or 2.1 V rms.

### Application for Monaural-Mode Operation

A single-channel signal from the stereo audio data input is output from both $V_{OUT}$L and $V_{OUT}$R as a differential output. The channel to be output is selected by setting the CHSL bit in register 20. The advantage of monaural operation is to provide over 115 dB of dynamic range for high-end audio applications.




NOTE: Example R and C values for $f_C$ = 77 kHz, R1–R4: 3.6 kΩ, R5, R6: 3.3 kΩ, R7, R8: 680 Ω, C1: 1800 pF, C2, C3: 560 pF.

**Figure 33. Connection Diagram for Monaural Mode Interface**

## APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE

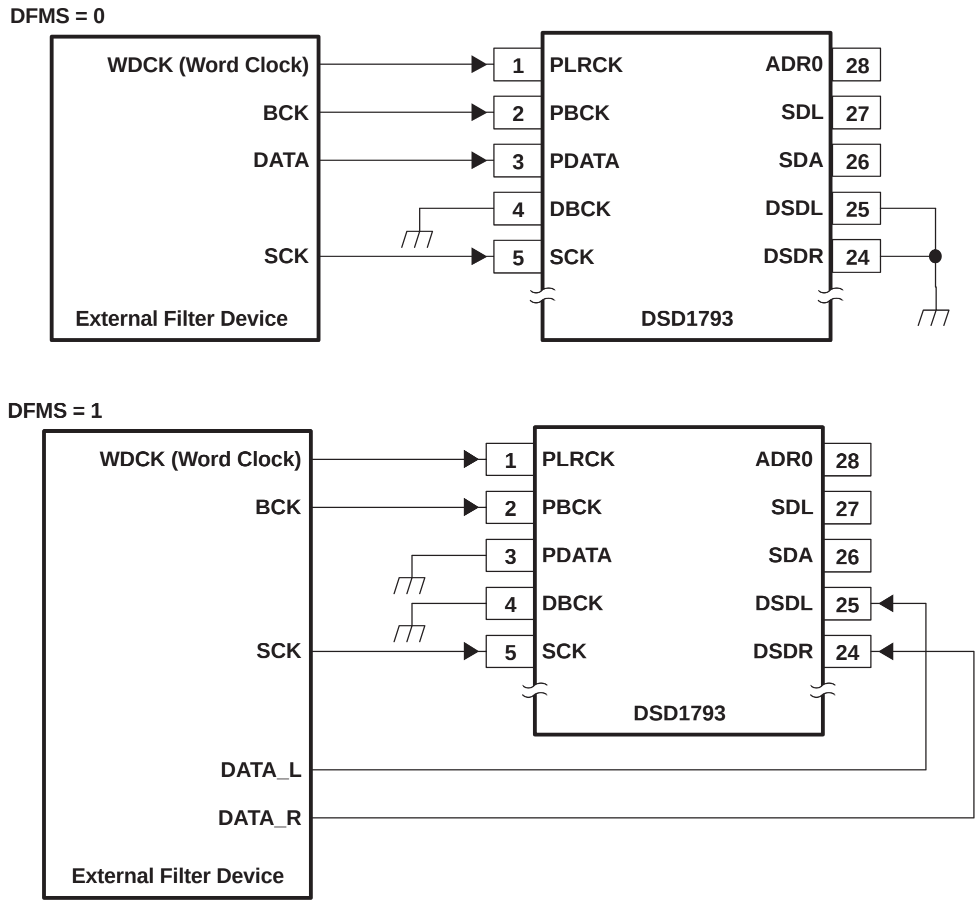



**Figure 34. Connection Diagram for External DIgital Filter (Internal DF Bypass Mode) Application**

### Application for Interfacing With an External Digital Filter

For some applications, it may be desirable to use an external digital filter to perform the interpolation function, as it can provide improved stop-band attenuation when compared to the internal digital filter of the DSD1793.

The DSD1793 supports several external digital filters, including:

- Texas Instruments DF1704 and DF1706
- Pacific Microsonics PMD200 HDCD filter/decoder IC
- Programmable digital signal processors

The external digital filter application mode is accessed by programming the following bit in the corresponding control register:

- DFTH = 1 (register 20)

The pins used to provide the serial interface for the external digital filter are shown in the connection diagram of Figure 34. The word clock (WDCK) signal must be operated at 8× or 4× the desired sampling frequency, $f_S$.

### Pin Assignments When Using the External Digital Filter Interface

- PLRCK (pin 1): WDCK as word clock input
- PBCK (pin 2): BCK as bit clock for audio data
- PDATA (pin 3): DATA as monaural audio data input when the DFMS bit is not set to 1
- DSDL (pin 25): DATAL as L-channel audio data input when the DFMS bit is set to 1
- DSDR (pin 24): DATAR as R-channel audio data input when the DFMS bit is set to 1

### Audio Format

The DSD1793 in the external digital filter interface mode supports right-justified audio formats including 16-bit, 20-bit, and 24-bit audio data, as shown in Figure 35. The audio format is selected by the FMT[2:0] bits of control register 18.

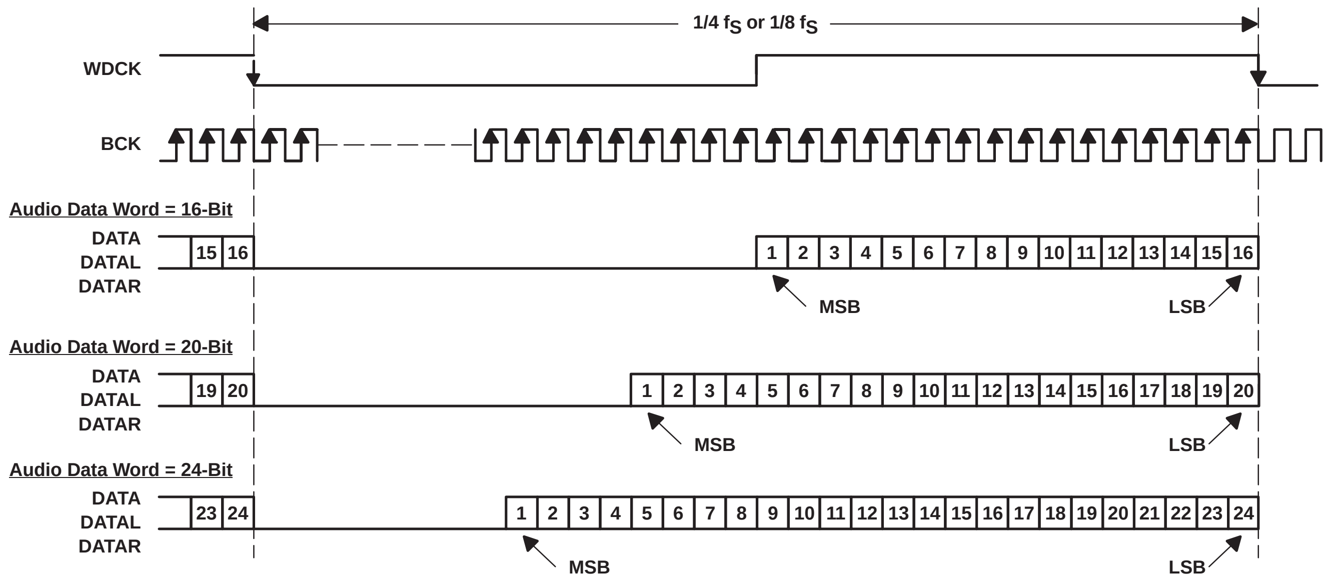
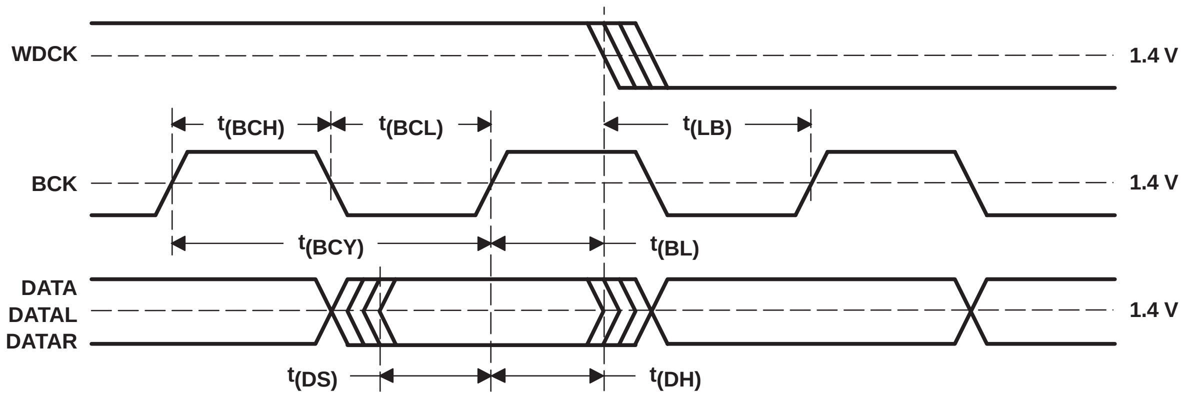



**Figure 35. Audio Data Input Format for External Digital Filter (Internal DF Bypass Mode) Application**

### System Clock (SCK) and Interface Timing

The DSD1793 in an application using an external digital filter requires the synchronization of WDCK and the system clock. The system clock is phase-free with respect to WDCK. Interface timing among WDCK, BCK, DATA, DATAL, and DATAR is shown in Figure 36.




| PARAMETER | | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{(BCY)}$ | BCK pulse cycle time | 20 | | ns |
| $t_{(BCL)}$ | BCK pulse duration, LOW | 7 | | ns |
| $t_{(BCH)}$ | BCK pulse duration, HIGH | 7 | | ns |
| $t_{(BL)}$ | BCK rising edge to WDCK falling edge | 5 | | ns |
| $t_{(LB)}$ | WDCK falling edge to BCK rising edge | 5 | | ns |
| $t_{(DS)}$ | DATA, DATAL, DATAR setup time | 5 | | ns |
| $t_{(DH)}$ | DATA, DATAL, DATAR hold time | 5 | | ns |

**Figure 36. Audio Interface Timing for External Digital Filter (Internal DF Bypass Mode) Application**

### Functions Available in the External Digital Filter Mode

The external digital filter mode allows access to the majority of the DSD1793 mode control functions.

The following table shows the register mapping available when the external digital filter mode is selected, along with descriptions of functions which are modified when using this mode selection.

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Register 16** | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | − | − | − | − | − | − | − | − |
| **Register 17** | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 0 | 1 | − | − | − | − | − | − | − | − |
| **Register 18** | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 1 | 0 | − | FMT2 | FMT1 | FMT0 | − | − | − | − |
| **Register 19** | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 1 | 1 | REV | − | − | OPE | − | DFMS | − | INZD |
| **Register 20** | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 1 | 0 | 0 | − | SRST | 0 | 1 | MONO | CHSL | OS1 | OS0 |
| **Register 21** | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 1 | 0 | 1 | − | − | − | − | − | − | − | PCMZ |
| **Register 22** | R | 0 | 0 | 1 | 0 | 1 | 1 | 0 | − | − | − | − | − | − | ZFGR | ZFGL |

NOTE: −: Function is disabled. No operation even if data bit is set

### FMT[2:0]: Audio Data Format Selection

Default value: 000

| FMT[2:0] | Audio Data Format Select |
|---|---|
| 000 | 16-bit right-justified format (default) |
| 001 | 20-bit right-justified format |
| 010 | 24-bit right-justified format |
| Other | N/A |

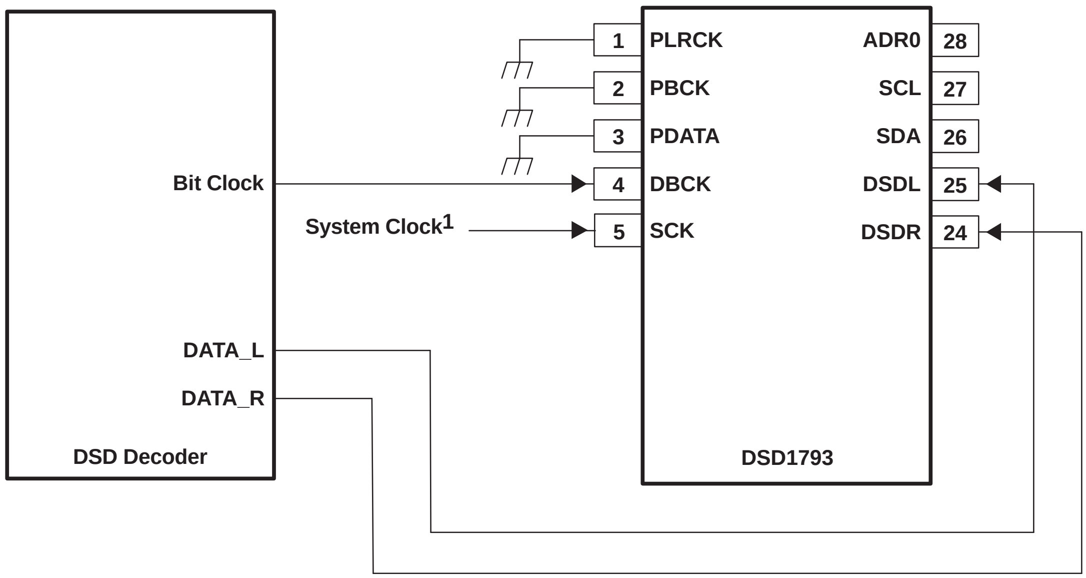
### OS[1:0]: Delta-Sigma Modulator Oversampling Rate Selection

Default value: 00

| OS[1:0] | Operation Speed Select |
|---|---|
| 00 | 8 times WDCK (default) |
| 01 | 4 times WDCK |
| 10 | 16 times WDCK |
| 11 | Reserved |

The effective oversampling rate is determined by the oversampling performed by both the external digital filter and the delta-sigma modulator. For example, if the external digital filter is 8× oversampling, and the user selects OS[1:0] = 00, then the delta-sigma modulator oversamples by 8×, resulting in an effective oversampling rate of 64×. The 16× WDCK oversampling rate is not available above a 100-kHz sampling rate. If the oversampling rate selected is 16× WDCK, the system clock frequency must be over 256 $f_S$.

## APPLICATION FOR DSD FORMAT (DSD MODE) INTERFACE




(1) The system clock is necessary for the initialization sequence and the I2C interface operation.

**Figure 37. Connection Diagram in DSD Mode**

### Feature

This mode is used for interfacing directly to a DSD decoder, which is found in Super Audio CD™ (SACD) applications.

The DSD mode is accessed by programming the following bit in the corresponding control register:

- DSD = 1 (register 20)

The DSD mode provides a low-pass filtering function. The filtering is provided using an analog FIR filter structure. Four FIR responses are available, and are selected via DMF[1:0] of control register 18.

### Pin Assignment When Using the DSD Format Interface

- DSDL (pin 25): L-channel DSD data input
- DSDR (pin 24): R-channel DSD data input
- DBCK (pin 4): Bit clock (BCK) for DSD data

Super Audio CD is a trademark of Sony Kabushiki Kaisha TA Sony Corporation, Japan.

### Requirements for Bit Clock and System Clock

The bit clock (DBCK) for DSD mode is required at pin 4 of the DSD1793. The frequency of the bit clock can be N times the sampling frequency. Generally, N is 64 in DSD applications.

The interface timing between the bit clock and DSDL, DSDR is required to meet the setup and hold time specifications shown in Figure 39.

The system clock is necessary for the initialization sequence and the $I^2C$ interface operation.

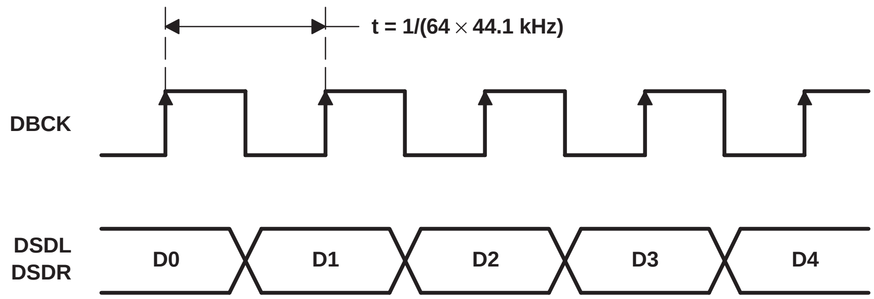
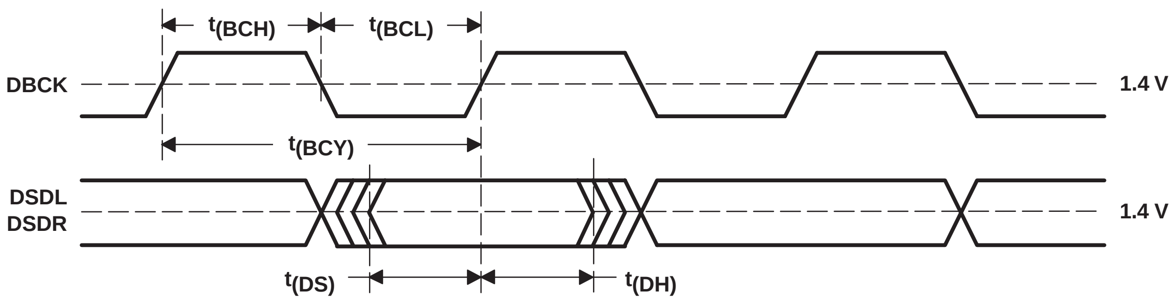



**Figure 38. Normal Data Output Form From DSD Decoder**




| PARAMETER | | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{(BCY)}$ | DBCK pulse cycle time | 85(1) | | ns |
| $t_{(BCH)}$ | DBCK high-level time | 30 | | ns |
| $t_{(BCL)}$ | DBCK low-level time | 30 | | ns |
| $t_{(DS)}$ | DSDL, DSDR setup time | 10 | | ns |
| $t_{(DH)}$ | DSDL, DSDR hold time | 10 | | ns |

(1) 2.8224 MHz × 4. (2.8224 MHz = 64 × 44.1 kHz. This value is specified as a sampling rate of DSD.)

**Figure 39. Timing for DSD Audio Interface**

## ANALOG FIR FILTER PERFORMANCE IN DSD MODE

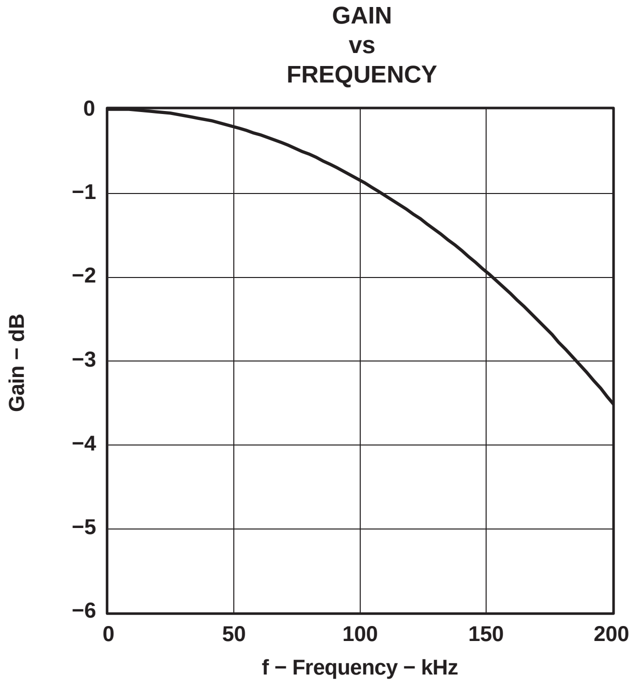



Figure 40. DSD Filter-1, Low BW

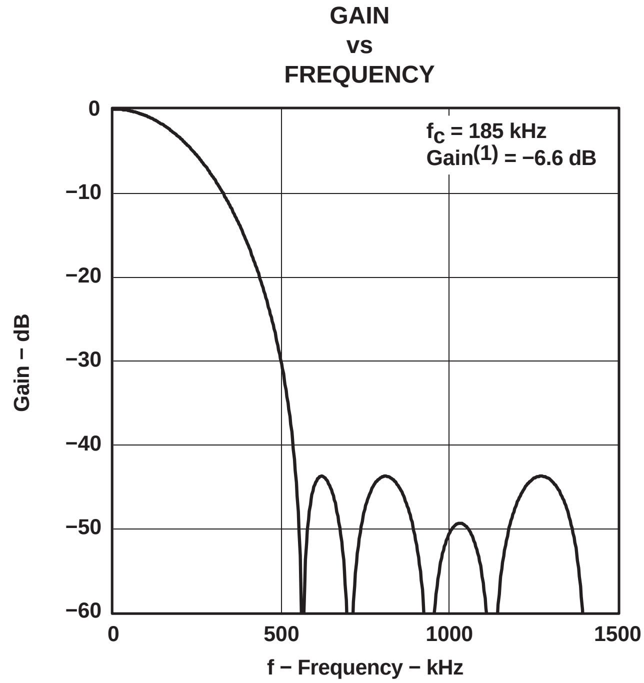



Figure 41. DSD Filter-1, High BW

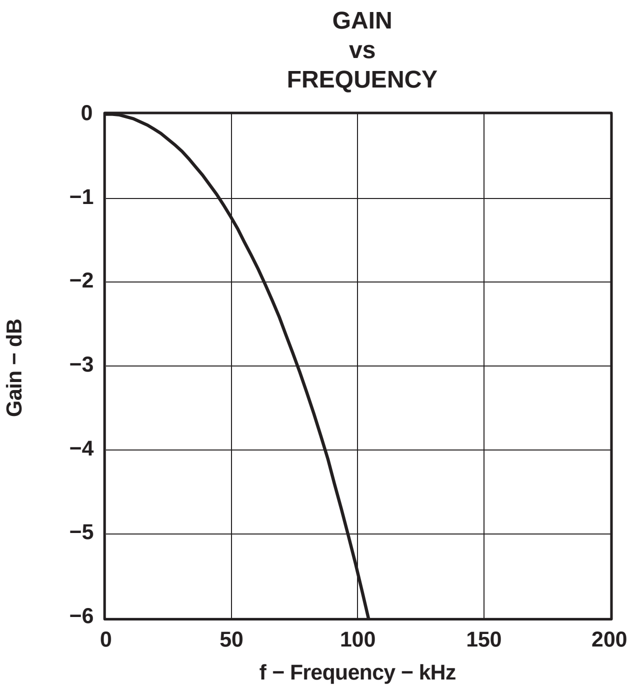



Figure 42. DSD Filter-2, Low BW

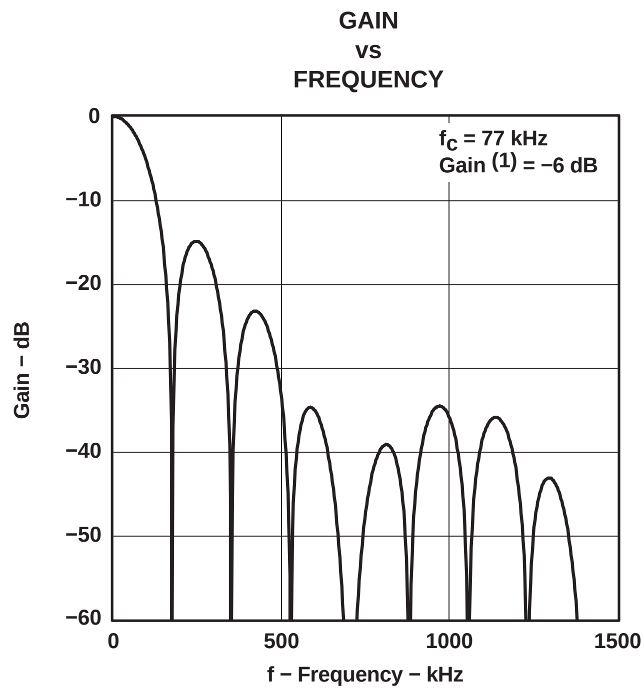



Figure 43. DSD Filter-2, High BW

(1) This gain is in comparison to PCM 0 dB, when the DSD input signal efficiency is 50%.

All specifications at DBCK = 2.8224 MHz (44.1 kHz × 64 $f_S$), and 50% modulation DSD data input, unless otherwise noted.

## ANALOG FIR FILTER PERFORMANCE IN DSD MODE (CONTINUED)

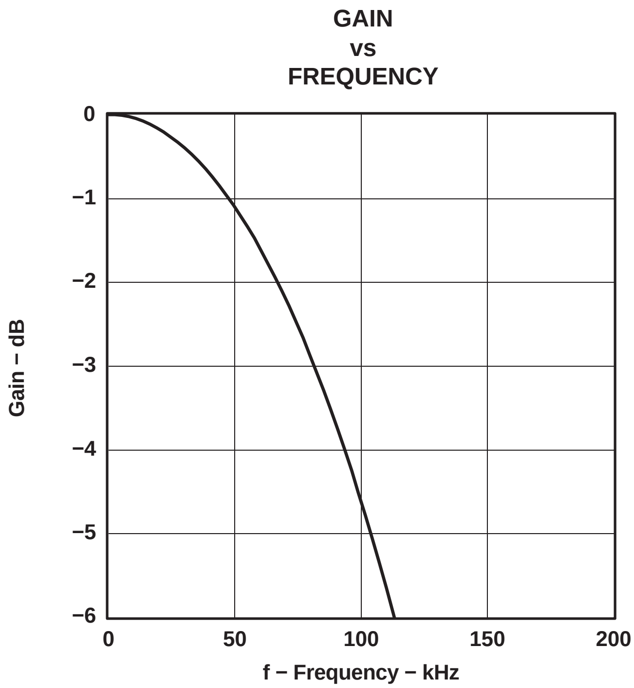



Figure 44. DSD Filter-3, Low BW

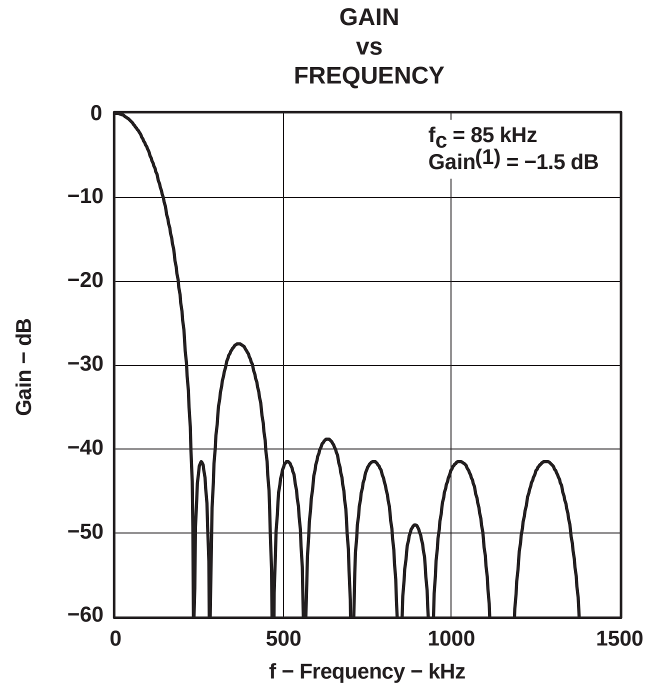



Figure 45. DSD Filter-3, High BW

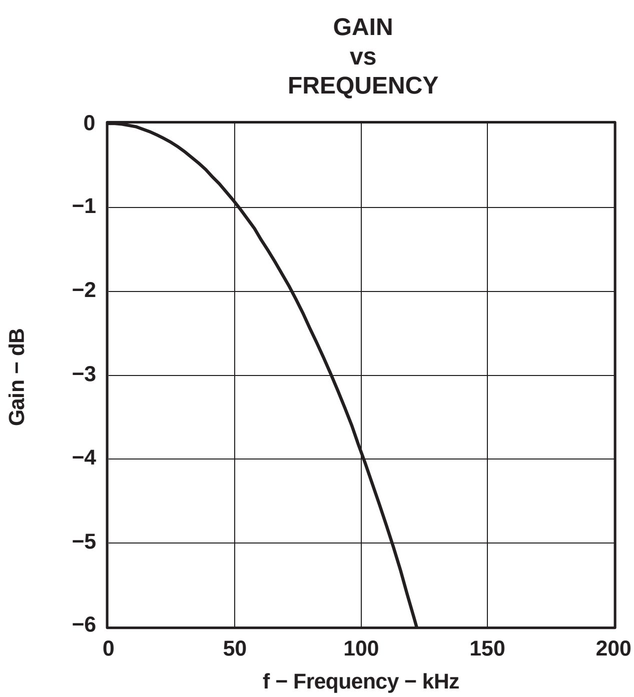



Figure 46. DSD Filter-4, Low BW

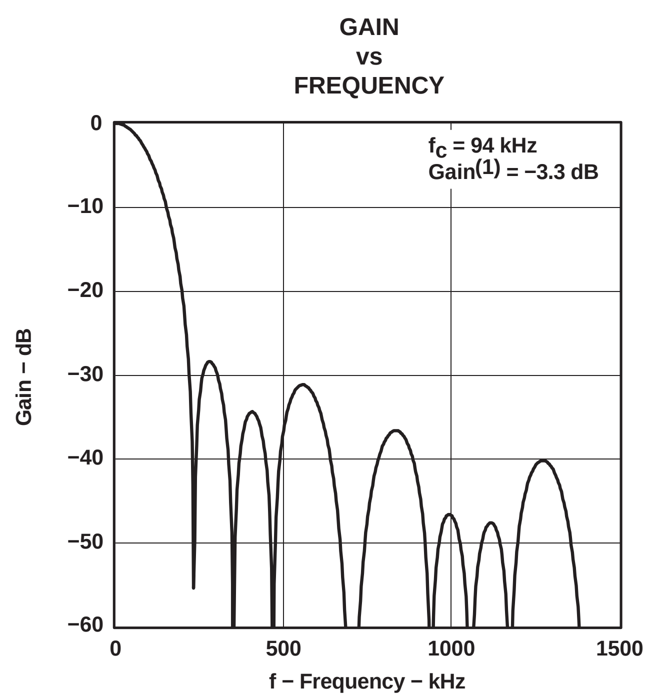



Figure 47. DSD Filter-4, High BW

(1) This gain is in comparison to PCM 0 dB, when the DSD input signal efficiency is 50%.

## DSD MODE CONFIGURATION AND FUNCTION CONTROLS

### Configuration for the DSD Interface Mode

DSD = 1 (Register 20, B5)

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Register 16** | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | − | − | − | − | − | − | − | − |
| **Register 17** | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 0 | 1 | − | − | − | − | − | − | − | − |
| **Register 18** | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 1 | 0 | − | − | − | − | DMF1 | DMF0 | − | − |
| **Register 19** | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 0 | 1 | 1 | REV | − | − | OPE | − | − | − | − |
| **Register 20** | R/$\overline{W}$ | 0 | 0 | 1 | 0 | 1 | 0 | 0 | − | SRST | 1 | − | MONO | CHSL | OS1 | OS0 |
| **Register 21** | R | 0 | 0 | 1 | 0 | 1 | 0 | 1 | − | − | − | − | − | DZ1 | DZ0 | − |
| **Register 22** | R | 0 | 0 | 1 | 0 | 1 | 1 | 0 | − | − | − | − | − | − | ZFGR | ZFGL |

NOTE: −: Function is disabled. No operation even if data bit is set

### DMF[1:0]: Analog FIR Performance Selection

Default value: 00

| DMF[1:0] | Analog FIR Performance Select |
|---|---|
| 00 | FIR-1 (default) |
| 01 | FIR-2 |
| 10 | FIR-3 |
| 11 | FIR-4 |

Plots for the four analog FIR filter responses are shown in the *ANALOG FIR FILTER PERFORMANCE IN DSD MODE* section of this data sheet.

### OS[1:0]: Analog-FIR Operation Speed Selection

Default value: 00

| OS[1:0] | Operation Speed Select |
|---|---|
| 00 | $f_{DBCK}$ (default) |
| 01 | $f_{DBCK}/2$ |
| 10 | Reserved |
| 11 | $f_{DBCK}/4$ |

The OS bits in the DSD mode select the operating rate of the analog FIR. The OS bits must be set before setting the DSD bit to 1.

## THEORY OF OPERATION

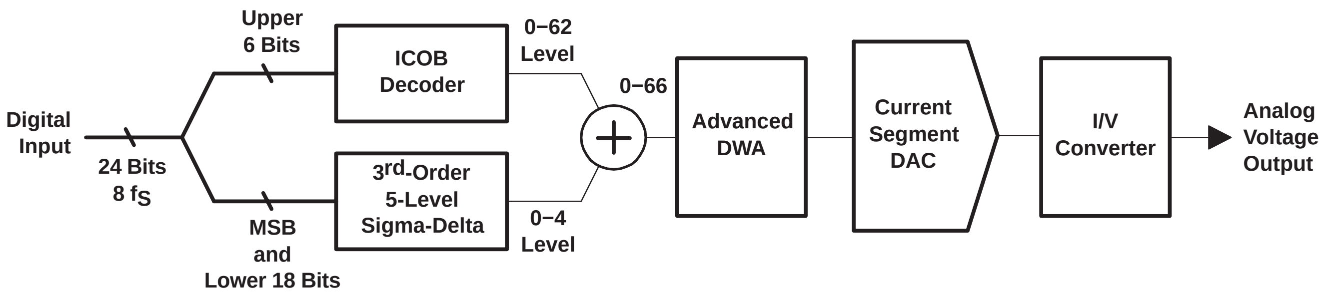



**Figure 48. Advanced Segment DAC With I/V Converter**

The DSD1793 uses TI's advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The DSD1793 provides balanced voltage outputs.

Digital input data via the digital filter is separated into 6 upper bits and 18 lower bits. The 6 upper bits are converted to inverted complementary offset binary (ICOB) code. The lower 18 bits, in association with the MSB, are processed by a five-level third-order delta-sigma modulator operated at 64 $f_S$ by default. The 1 level of the modulator is equivalent to the 1 LSB of the ICOB code converter. The data groups processed in the ICOB converter and third-order delta-sigma modulator are summed together to an up to 66-level digital code, and then processed by data-weighted averaging (DWA) to reduce the noise produced by element mismatch. The data of up to 66 levels from the DWA is converted to an analog output in the differential-current segment section.

This architecture has overcome the various drawbacks of conventional multibit processing and also achieves excellent dynamic performance.

## CONSIDERATIONS FOR APPLICATION CIRCUITS

### PCB Layout Guidelines

A typical PCB floor plan for the DSD1793 is shown in Figure 49. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The DSD1793 must be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board. Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the D/A converters. In cases where a common 5-V supply would be used for the analog and digital sections, an inductance (RF choke, ferrite bead) must be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 50 shows the recommended approach for single-supply applications.

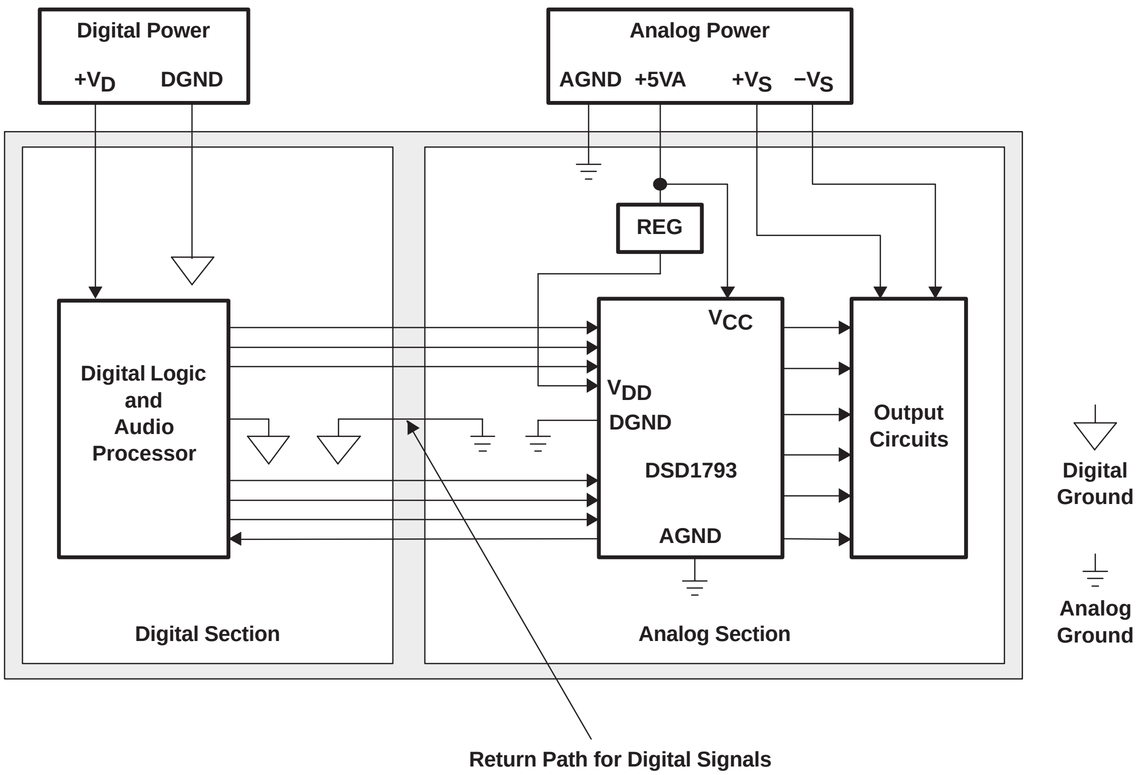



**Figure 49. Recommended PCB Layout**

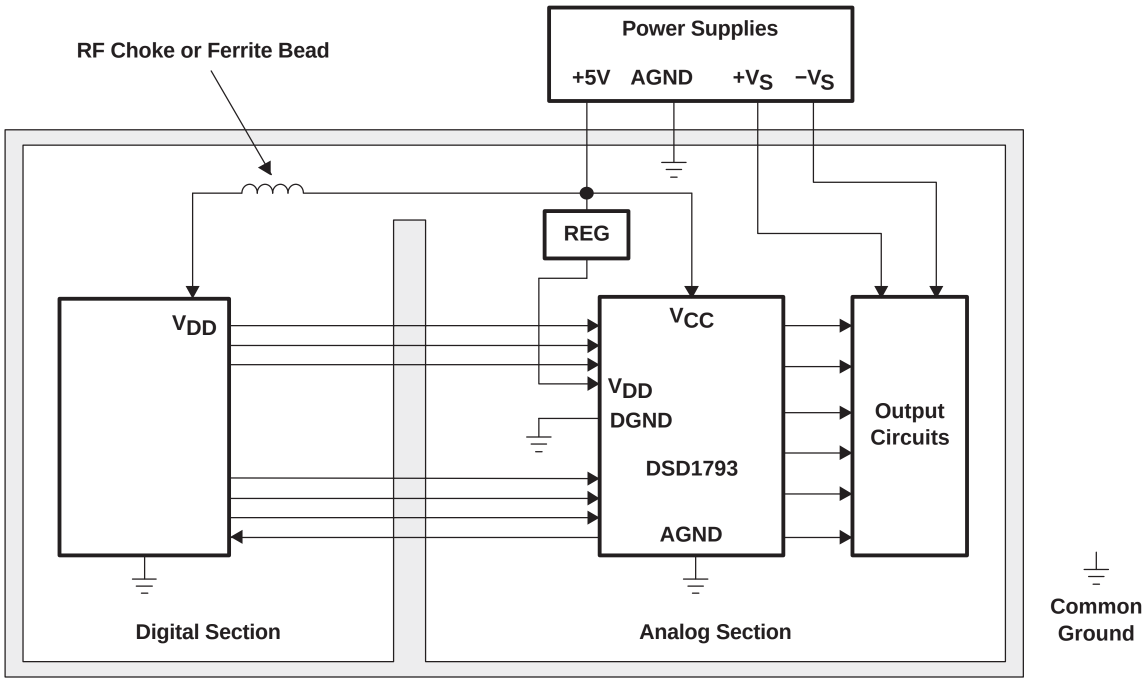



**Figure 50. Single-Supply PCB Layout**

### Bypass and Decoupling Capacitor Requirements

Various sized decoupling capacitors can be used, with no special tolerances being required. All capacitors must be located as close as possible to the appropriate pins of the DSD1793 to reduce noise pickup from surrounding circuitry. Aluminum electrolytic capacitors that are designed for hi-fi audio applications are recommended for larger values, while metal film or monolithic ceramic capacitors are used for smaller values.

### Post-LPF Design

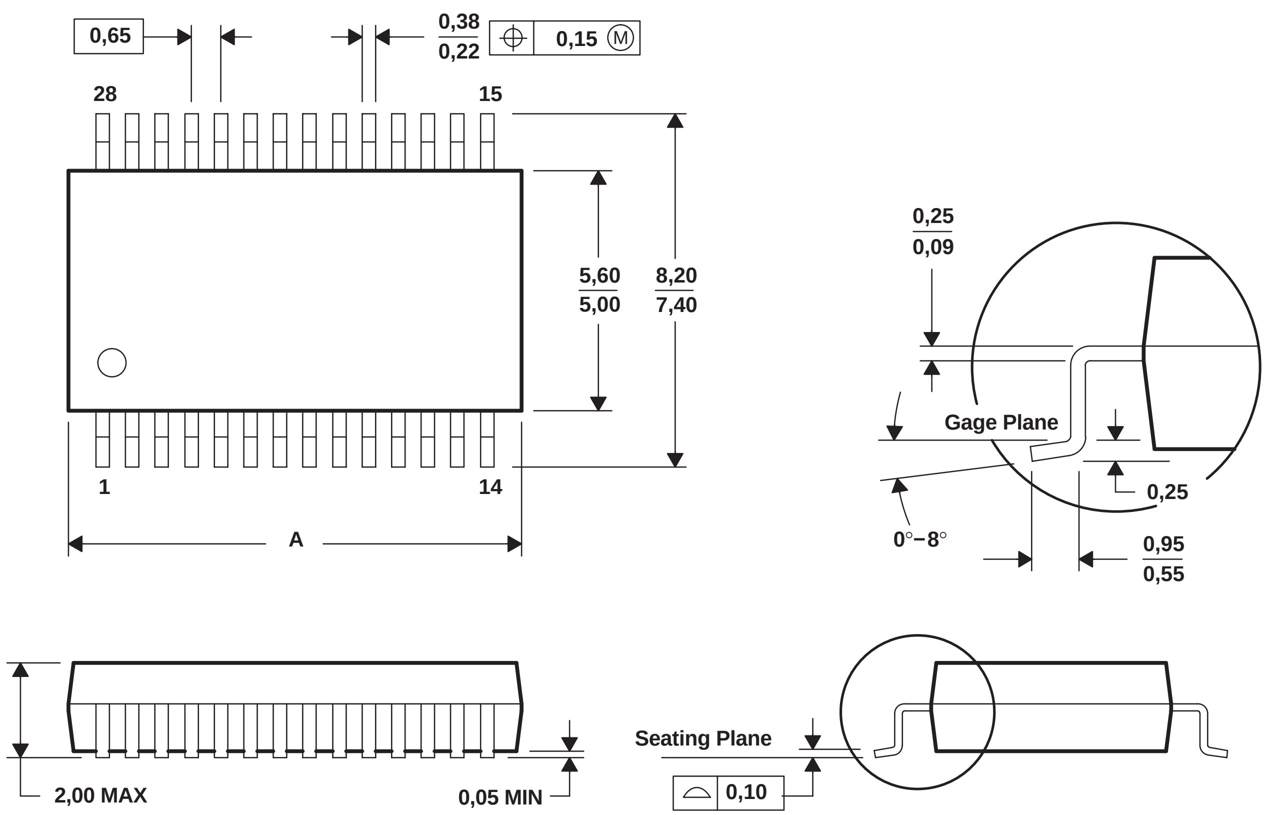
By proper choice of the op amp and resistors used in the post-LPF circuit, excellent performance of the DSD1793 should be achieved. To obtain 0.001% THD+N and 113 dB signal-to-noise-ratio audio performance, the THD+N and input noise performance of the op amp should be considered. This is because the input noise of the op amp contributes directly to the output noise level of the application. The $V_{OUT}$ pin of the DSD1793 and the input resistor of the post-LPF circuit must be connected as closely as possible.

Out-of-band noise level and attenuated sampling spectrum level are much lower than for typical delta-sigma type DACs due to the combination of a high-performance digital filter and advanced segment DAC architecture. The use of a second-order or third-order post-LPF is recommended for the post-LPF of the DSD1793. The cutoff frequency of the post-LPF depends on the application. For example, there are many sampling-rate operations such as $f_S$ = 44.1 kHz on CDDA, $f_S$ = 96 kHz on DVD-M, $f_S$ = 192 kHz on DVD-A, $f_S$ = 64 $f_S$ on DSD (SACD).

## MECHANICAL DATA

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| PINS ** / DIM | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

4040065/E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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