MN3012

BBD With 3 Parallel Signal Delay Lines Incorporating Clock Generator

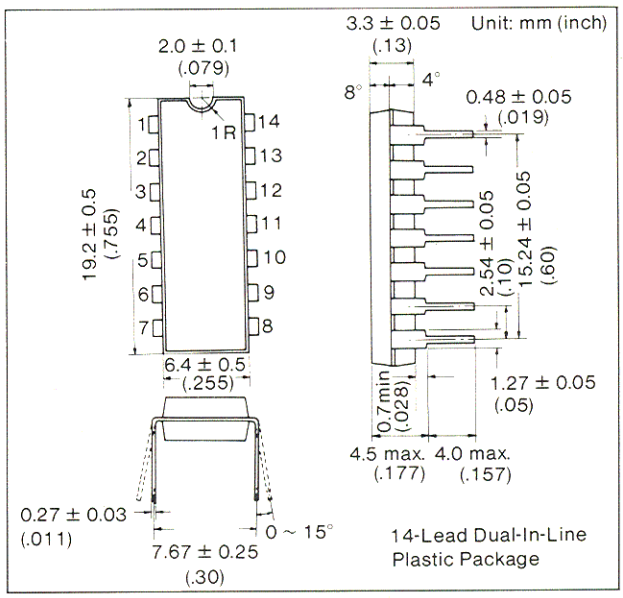
General Description

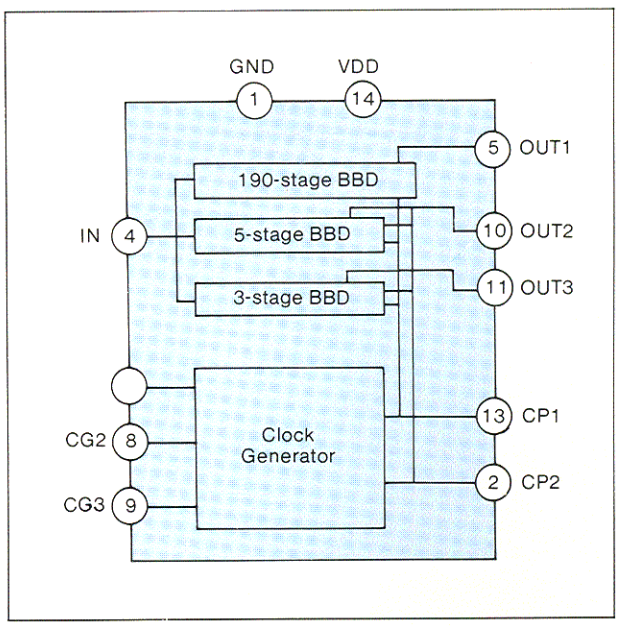
The MN3012 is BBD provided with 3, 5, 190 stages three parallel delay lines and a clock generator. The clock frequency which determines a delay time is controlled by the value of external resistor and capacitor connected to CG1, CG2 and CG3 terminals.

The MN3012 provides three differently delayed signals on OUT1, OUT2 and OUT3 terminals. The device is particularly suitable for producing chorus, vibrato and reverberation effects of audio equipment.

Features:

1. −8.5 −15V single voltage supply (VDD)
2. Delay time 01 : 0.475 − 9.5ms (190-stage)
   02 : 0.0125–0.25 (5-stage)
   03 : 0.0075–0.15 (3-stage)
3. Dynamic range S/N = 98dB typ. (OUT3)
4. Insertion IL = 0 dB typ.
5. Distortion THD = 0.4% typ.
6. Incorporating clock generator
7. Clock frequency 10–200KHz
8. Clock component cancellation
9. P-channel silicon gate process.





Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_I, V_O, V_{cp}	−18~+0.3	V
Operating Temperature	Topr	−20~+70	°C
Storage Temperature	Tstg	−56~+125	°C

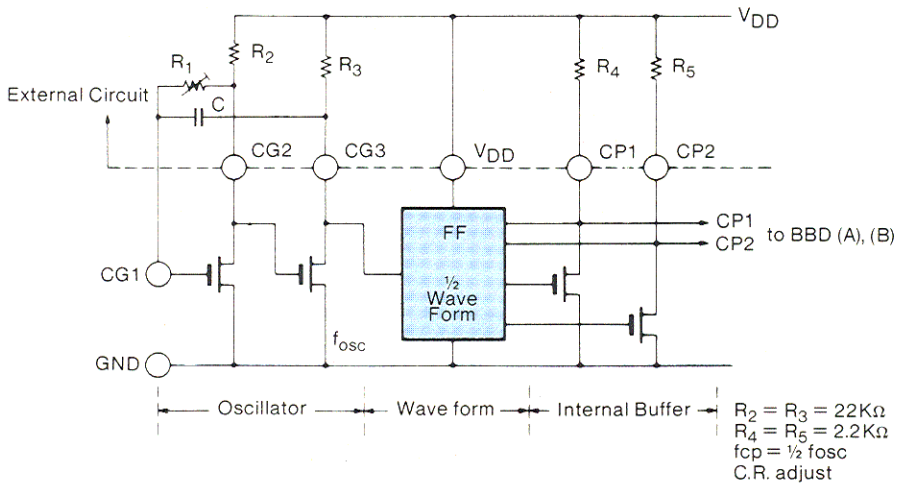
Operating Conditions (Ta = 25C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	−6.5	−15	−16	V
Clock H Level	VcpH	0		−0.4	V
Clock L Level	VcpL		VDD		V
Clock Frequency	fcp	10		200	KHz
Clock Input Capacitance	Ccp			180	pF
Input DC Bias	Vbias				V

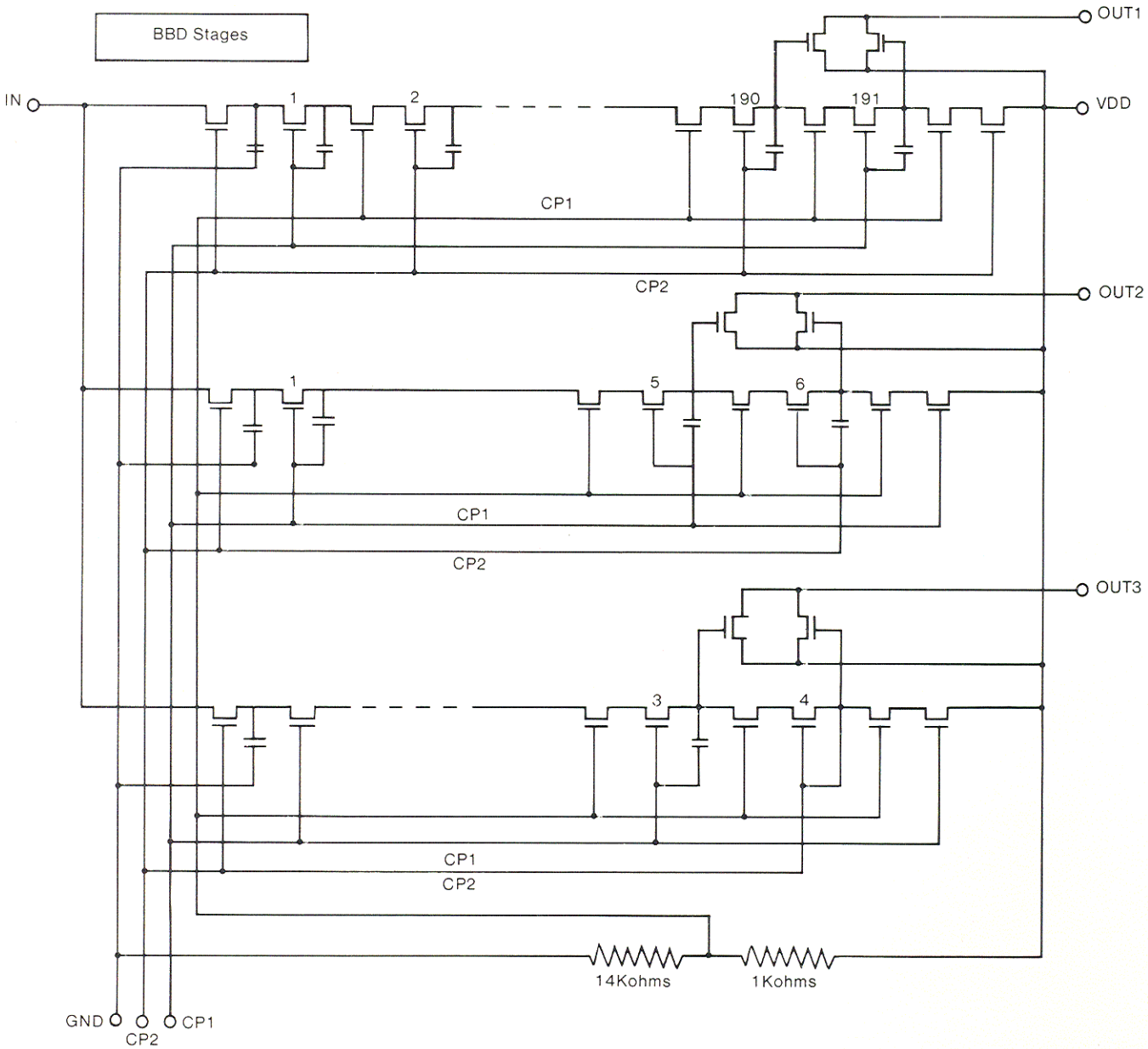
Characteristics (Ta = 25°C, V_{DD} = −15V, V_{cpL} = −15V, V_{cpH} = OV, RL = 56Kohms, C = 100pF R1 = R3 = 22 Mohms, R4 = R5 = 2.2Kohms, fcp = 1/2 fosc (R1 adjust)

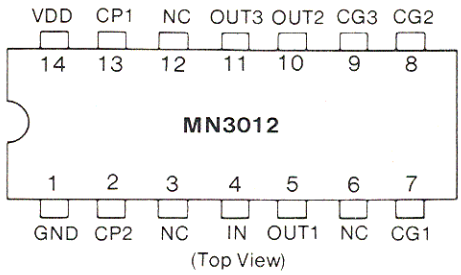
Item	Symbol	Condition	Min.	Typ.	Max.	°Unit
Signal Delay Time OUT1 Terminal OUT2 Terminal OUT3 Terminal	 tD1 tD2 tD3	 fcp = 10KHz 200KHz	 0.475 0.0125 0.0075		 9.5 0.125 0.15	 ms ms ms
Input Signal Frequency OUT Terminal 1 OUT Terminal 2 OUT Terminal 3	 fin1 fin2 fin3	fcp = 40KHz Output −3dB			 12 14 15	 KHz KHz KHz
Input Signal Voltage	vin	THD = 2.5%			1.2	Vrms
Insertion Loss	IL	fcp = 40KHz fin = 1KHz vin = 0.775 Vrms		0		dB
Distortion	THD			0.4		%
Noise Voltage OUT Terminal 1 OUT Terminal 2 OUT Terminal 3	 Vn1 Vn2 Vn3	 fcp = 100KHz Weighted by A curve			 0.14 0.05 0.04	 mVrms mVrms mVrms
S/M Ratio OUT Terminal 1 OUT Terminal 2 OUT Terminal 3	 S/N1 S/N2 S/N3	 Vn/Vin fcp = 100KHz Weighted by A curve		 90 97 98		 dB dB dB

Circuit Diagram
Clock Generator



Note: When external clock is used, remove R1 and C, apply the clock input to CG1.



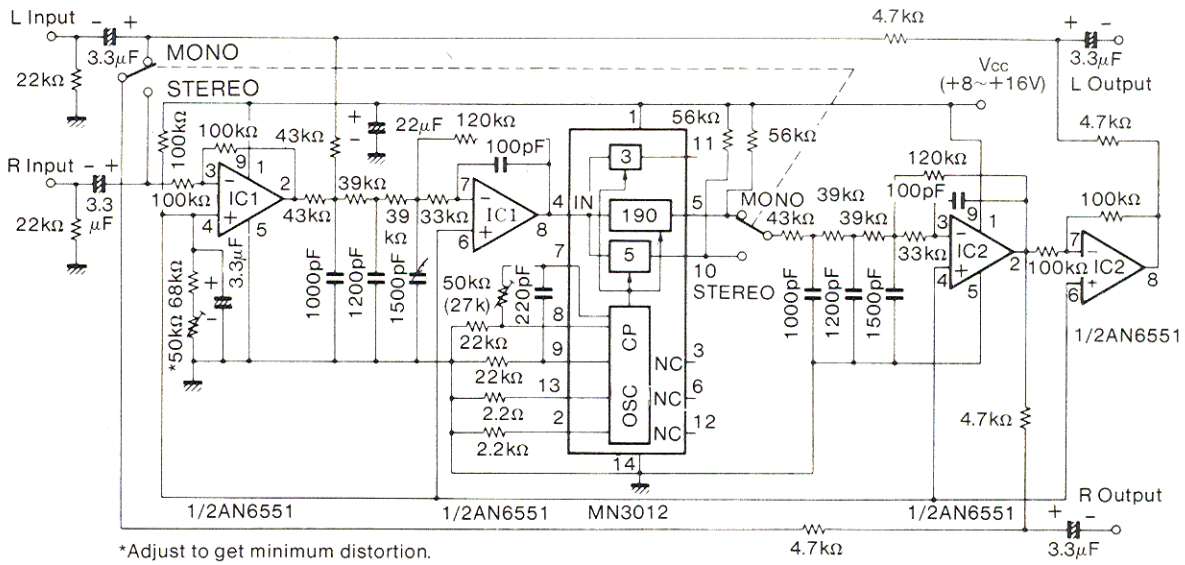


(Top View)

Terminal Assignments

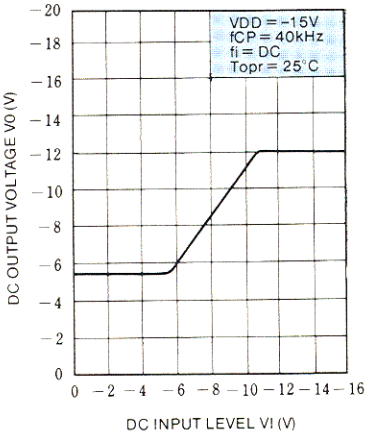
Pin No.	Symbol	Terminal
1	GND	Grounding
2	CP2	Clock pulse input
4	IN	Analog signal input
5	OUT1	Output terminal at 190 and 191-stage
7	CG1	Clock oscillation input
8	CG2	Clock oscillation input
9	CG3	Clock oscillation input
10	OUT2	Output terminal at 5 and 6-stage
11	OUT3	Output terminal at 3 and 4-stage
13	CP1	Clock pulse input
14	VDD	VDD = -15V supply terminal

Note: Terminal No. 3, 6, and 12 are non connection

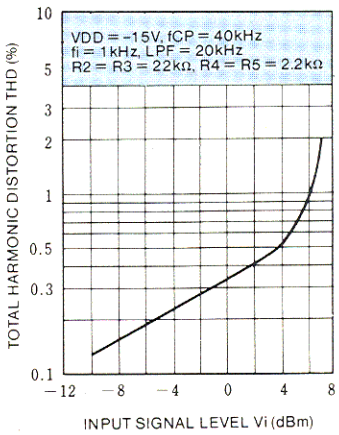


*Adjust to get minimum distortion.

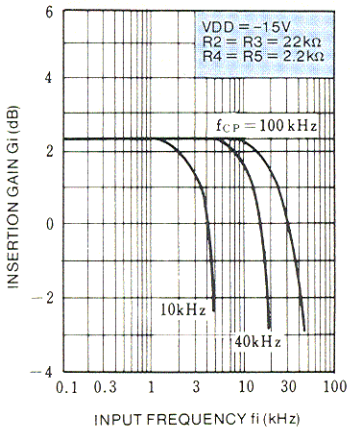
Vo – VI



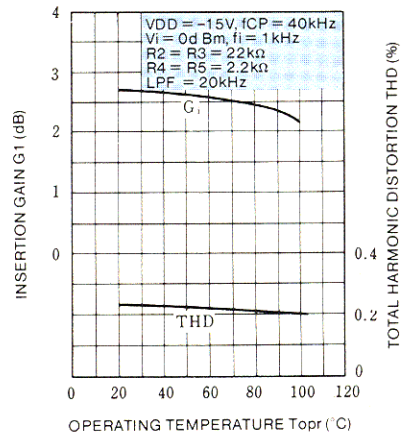
THD – Vi



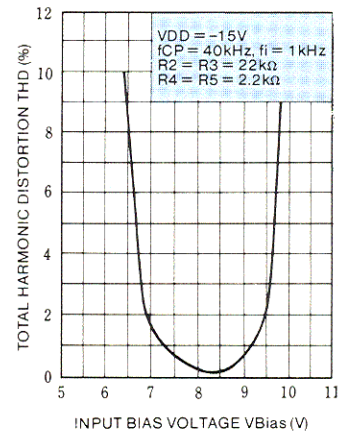
Gi – fi



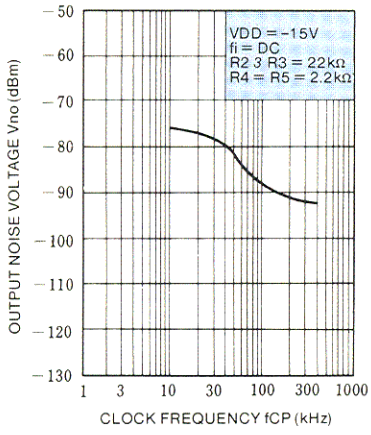
Gi, THD – Topr



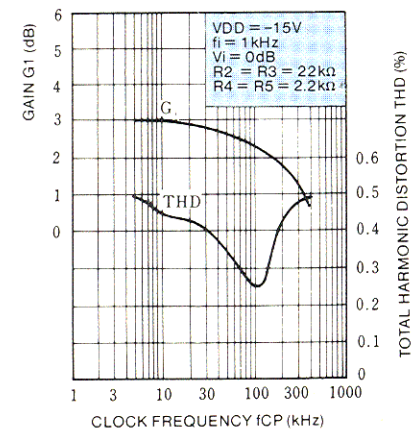
THD – VBias



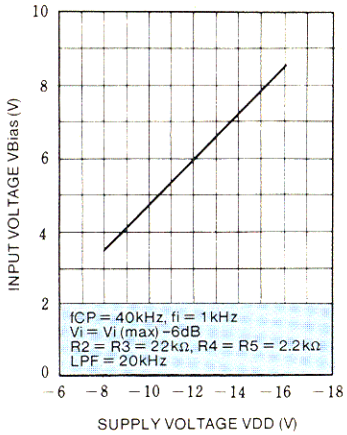
Vno – fCP



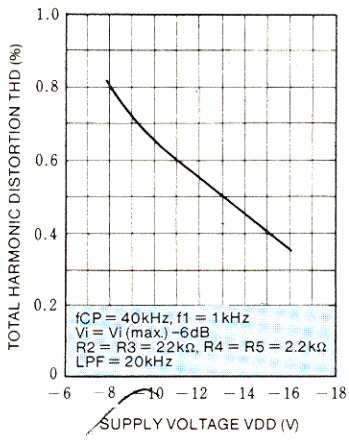
Gi, THD – fCP



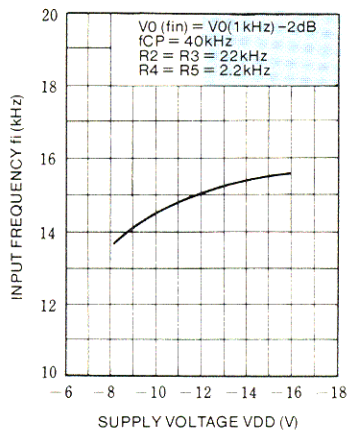
VBias – VDD



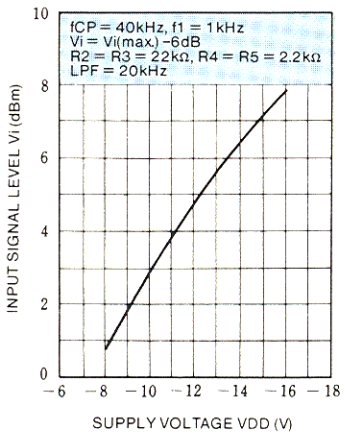
THD – VDD



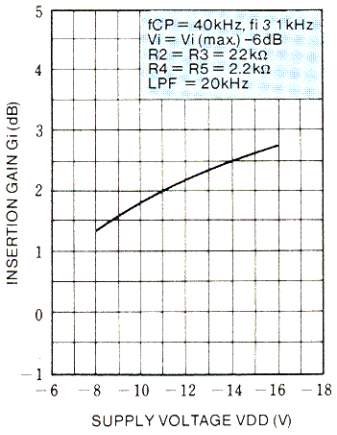
fi – VDD



Vi – VDD



Gi – VDD



S/N, Vno – VDD