VNB35NV04
VNV35NV04

OMNIFET II
fully autoprotected Power MOSFET

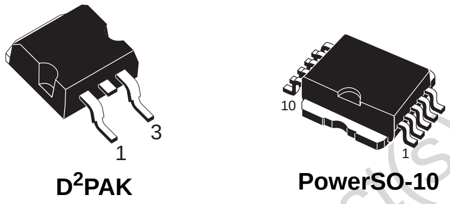
Datasheet − production data

Features

Type	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNB35NV04 VNV35NV04	10 mΩ[1]	30 A	40 V

1. For PowerSO-10 only

- Linear current limitation
- Thermal shut down
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET



Description

The VNB35NV04 and VNV35NV04 are monolithic devices designed in STMicroelectronics® VIPower® M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 25 kHz applications.

Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments. Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
D²PAK	VNB35NV04	VNB35NV0413TR
PowerSO-10	VNV35NV04	VNV35NV0413TR

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1 Block diagram and pin connection

Figure 1. Block diagram

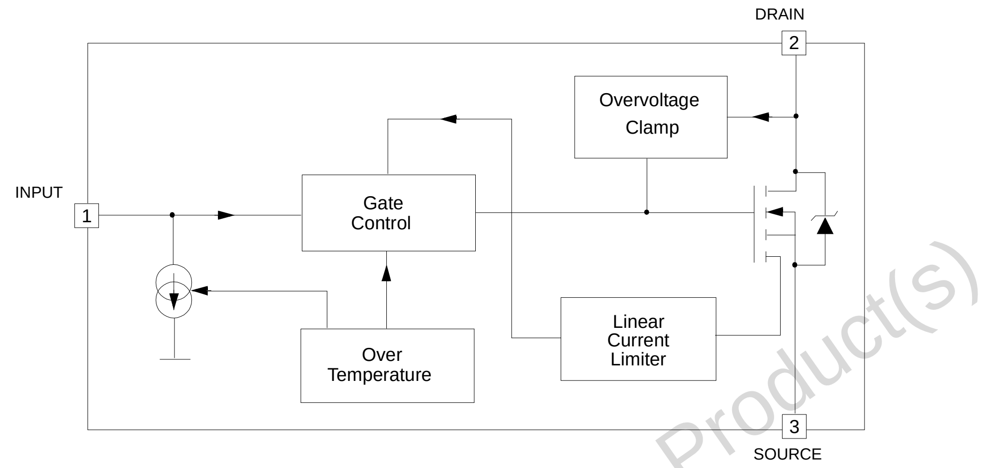
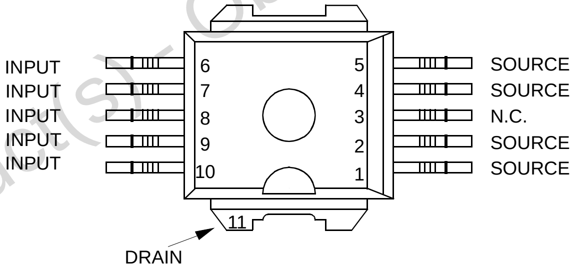


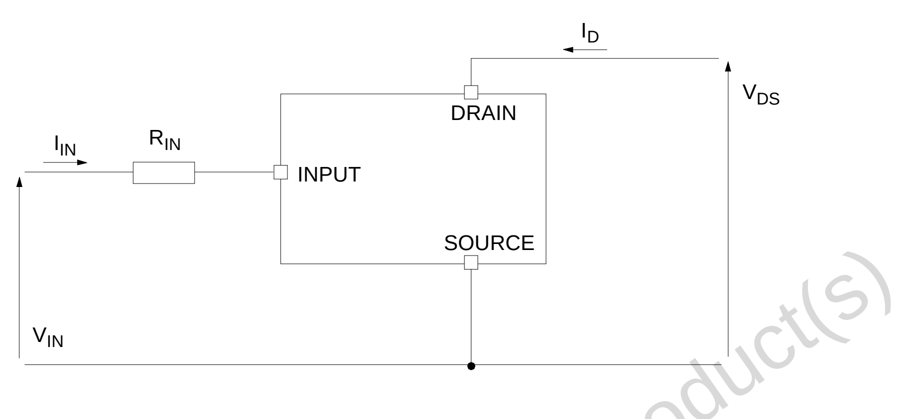
Figure 2. Pin connection



1. For the pins configuration related to D^{2}PAK, see *Figure 1*.

2 Electrical specification

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 2* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		PowerSO-10	D^2PAK	
V_{DS}	Drain-source voltage (V_{IN} = 0 V)	Internally clamped		V
V_{IN}	Input voltage	Internally clamped		V
I_{IN}	Input current	+/-20		mA
$R_{IN\ MIN}$	Minimum input series impedance	4.7		Ω
I_D	Drain current	Internally limited		A
I_R	Reverse DC output current	-30		A
V_{ESD1}	Electrostatic discharge (R = 1.5 KΩ, C = 100 pF)	4000		V
V_{ESD2}	Electrostatic discharge on output pin only (R = 330 Ω, C = 150 pF)	16500		V
P_{tot}	Total dissipation at T_c = 25°C	125	125	W
T_j	Operating junction temperature	Internally limited		°C
T_c	Case operating temperature	Internally limited		°C
T_{stg}	Storage temperature	-55 to 150		°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		PowerSO-10	D^2PAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case (max)	1	1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (max)	50(1)	50(1)	°C/W

1. When mounted on a standard single-sided FR4 board with 50mm^2 of Cu (at least 35 mm thick) connected to all DRAIN pins.

2.3 Electrical characteristics

-40°C < T_j < 150°C, unless otherwise specified.

Table 4. Off

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CLAMP}	Drain-source clamp voltage	V_{IN} = 0 V; I_D = 15 A	40	45	55	V
V_{CLTH}	Drain-source clamp threshold voltage	V_{IN} = 0 V; I_D = 2 mA	36			V
V_{INTH}	Input threshold voltage	V_{DS} = V_{IN}; I_D = 1 mA	0.5		2.5	V
I_{ISS}	Supply current from input pin	V_{DS} = 0 V; V_{IN} = 5 V		100	150	µA
V_{INCL}	Input-source clamp voltage	I_{IN} = 1 mA	6	6.8	8	V
		I_{IN} = -1 mA	-1.0		-0.3	V
I_{DSS}	Zero input voltage drain current (V_{IN} = 0 V)	V_{DS} = 13 V; V_{IN} = 0 V; T_j = 25 °C			30	µA
		V_{DS} = 25 V; V_{IN} = 0 V			75	µA

T_j = 25°C, unless otherwise specified

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
g_{fs}(1)	Forward transconductance	V_{DD} = 13 V; I_D = 15 A	—	35	—	S
C_{OSS}	Output capacitance	V_{DS} = 13 V; f = 1 MHz; V_{IN} = 0 V	—	1300	—	pF

1. Pulsed: Pulse duration = 300 ms, duty cycle 1.5%

Table 6. Switching

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_D = 15 A; V_{gen} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 4.7 Ω (see *Figure 3*)	—	150	500	ns
t_r	Rise time		—	840	2500	ns
$t_{d(off)}$	Turn-off delay time		—	980	3000	ns
t_f	Fall time		—	600	1500	ns
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_D = 15 A; V_{gen} = 5 V; R_{gen} = 2.2 KΩ (see *Figure 3*)	—	4	12	µs
t_r	Rise time		—	27	100	µs
$t_{d(off)}$	Turn-off delay time		—	34	120	µs
t_f	Fall time		—	31	110	µs
$(di/dt)_{on}$	Turn-on current slope	V_{DD} = 15 V; I_D = 15 A;V_{gen} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 4.7 Ω	—	18		A/µs
Q_i	Total input charge	V_{DD} = 12 V; I_D = 15 A; V_{IN} = 5 V; I_{gen} = 2.13 mA (see *Figure 8*)	—	118		nC

Table 7. Source drain diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SD}(1)	Forward on voltage	I_{SD} = 15 A; V_{IN} = 0 V	—	0.8	—	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A; dI/dt = 100 A/µs; V_{DD} = 30 V; L = 200 µH (see *Figure 4*)	—	400	—	ns
Q_{rr}	Reverse recovery charge		—	1.4	—	µC
I_{RRM}	Reverse recovery current		—	7	—	A

1. Pulsed: Pulse duration = 300 ms, duty cycle 1.5%

Table 8. Protections (-40°C < T_j < 150°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	Drain current limit	V_{IN} = 6 V; V_{DS} = 13 V	30	45	60	A
t_{dlim}	Step response current limit	V_{IN} = 6 V; V_{DS} = 13 V		50		µs
T_{jsh}	Overtemperature shutdown		150	175	200	°C
T_{jrs}	Overtemperature reset		135			°C
I_{gf}	Fault Sink Current	V_{IN} = 5 V; V_{DS} = 13 V; T_j = T_{jsh}	10	15	20	mA
E_{as}	Single pulse avalanche energy	Starting T_j = 25°C; V_{DD} = 24 V; V_{IN} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 4.7 Ω; L = 24 mH (see *Figure 6* and *Figure 7*)	1.7			J

2.4 Protection features

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 25 KHz. The only difference from the user's standpoint is that a small DC current I_{ISS} (typ. 100 µA) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection:

  internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit:

  limits the drain current I_D to I_{lim} whatever the INPUT pin voltages is. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh}.
- Overtemperature and short circuit protection:

  these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150°C to 190°C, a typical value being 170°C. The device is automatically restarted when the chip temperature falls of about 15°C below shutdown temperature.
- Status feedback:

  in the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current I_{gf}, the INPUT pin falls to 0 V. This does not however affect the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current I_{ISS}.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

Figure 4. Switching time test circuit for resistive load

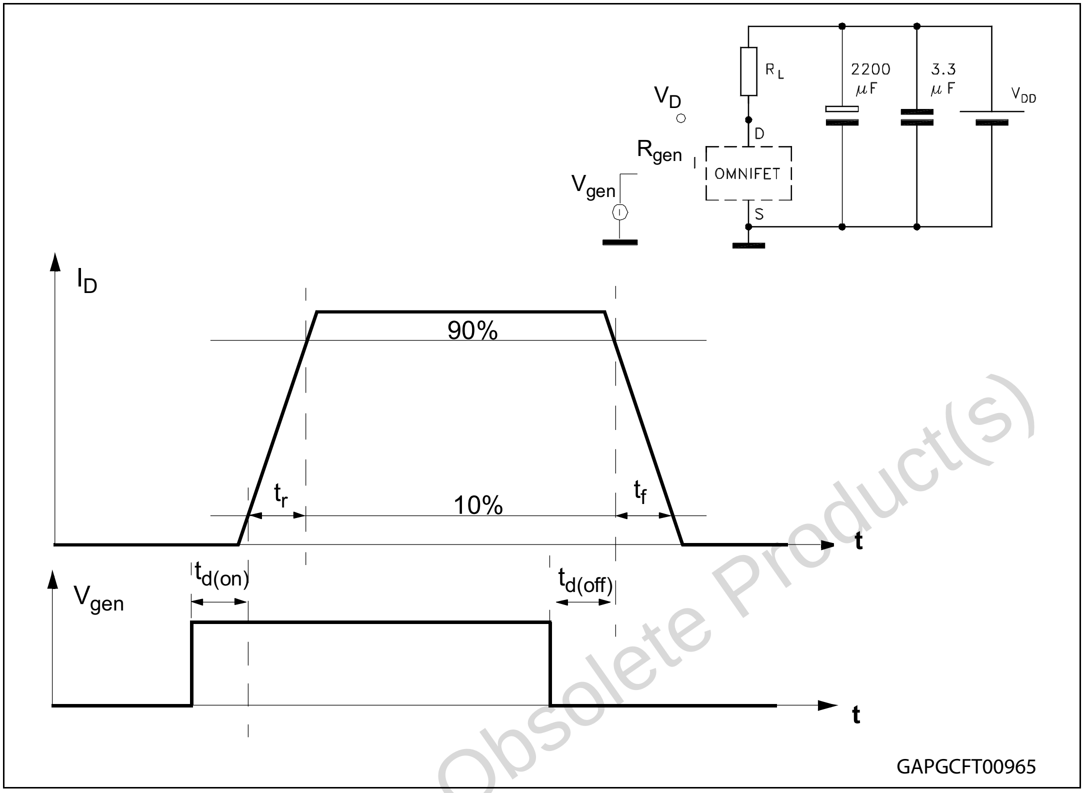


Figure 5. Test circuit for diode recovery times

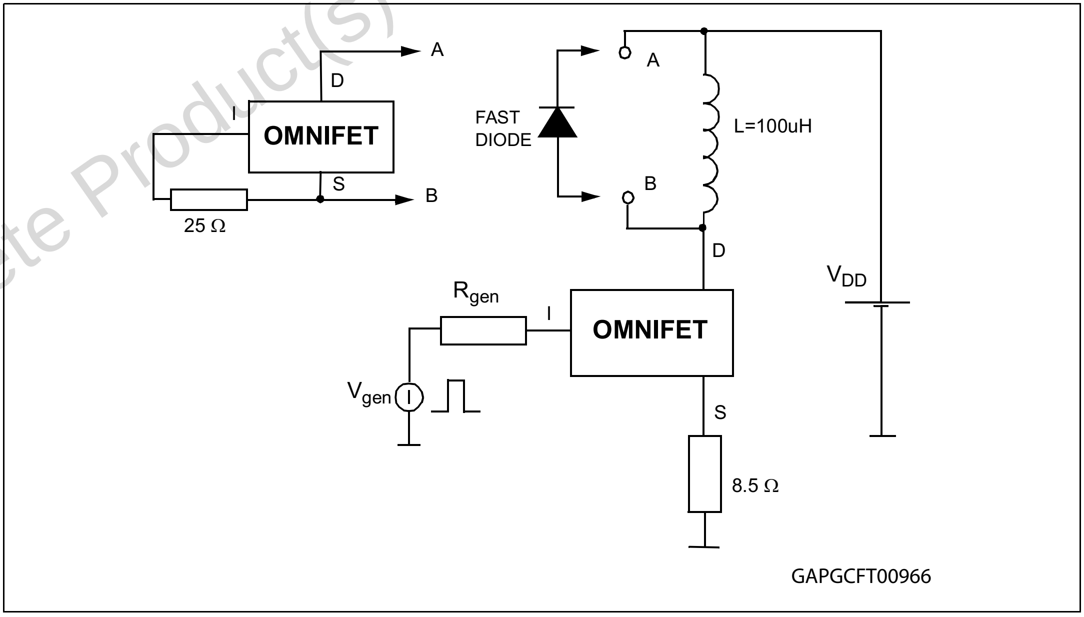


Figure 6. Unclamped inductive load test circuits

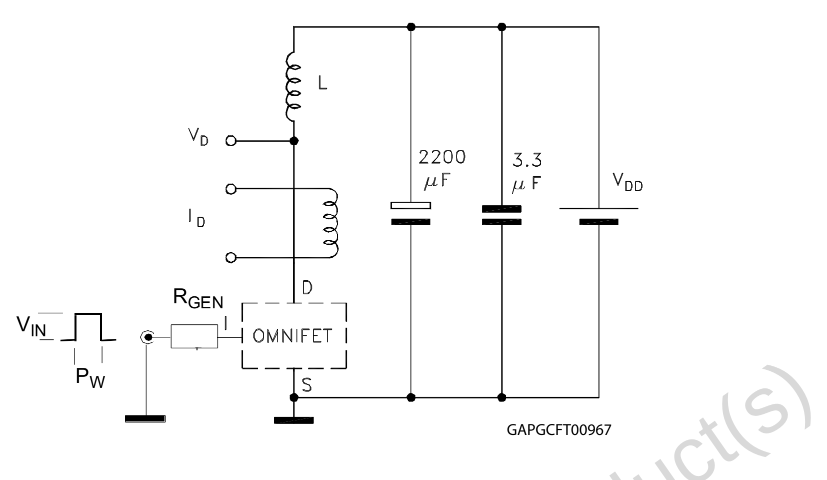


Figure 7. Unclamped inductive waveforms

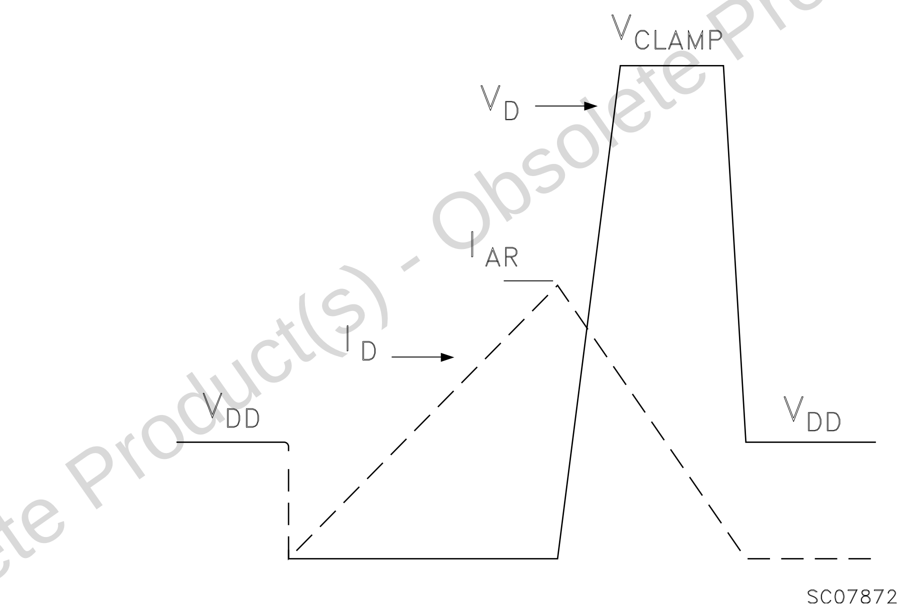
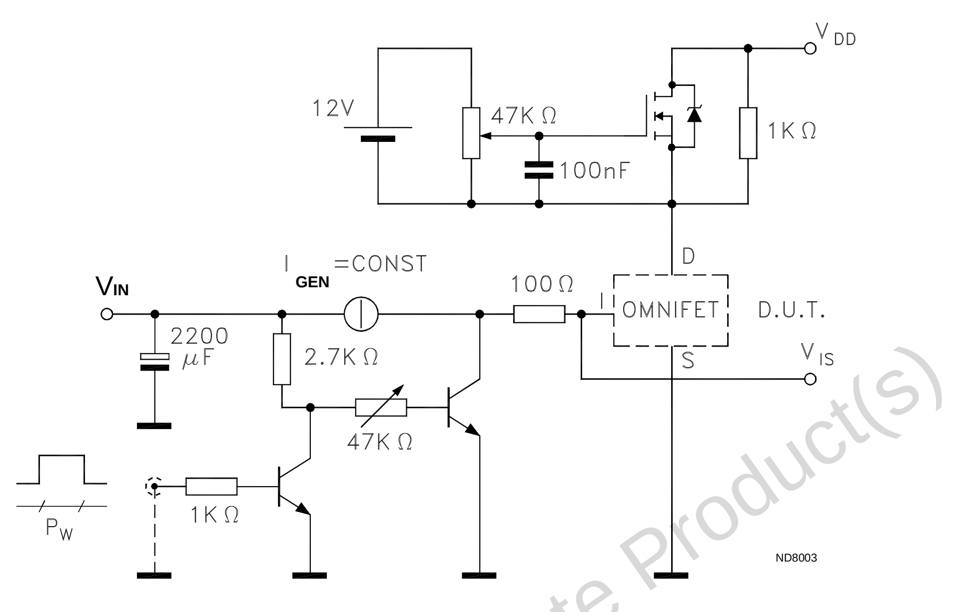


Figure 8. Input charge test circuit



2.5 Electrical characteristics curves

Figure 9. Source-drain diode forward characteristics

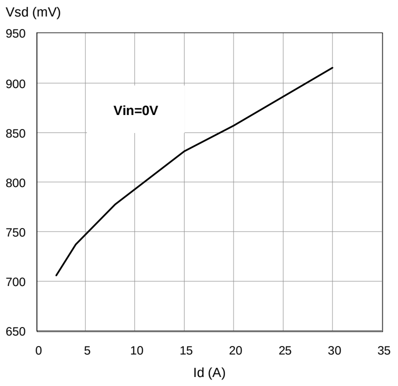


Figure 10. Static drain source on resistance

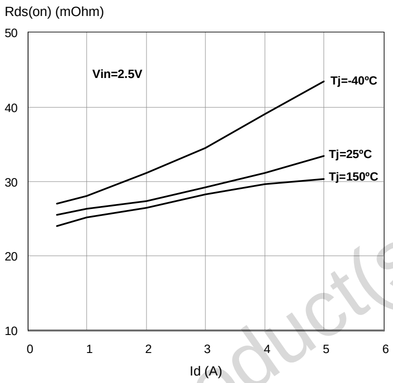


Figure 11. PowerSO-10 static drain-source on resistance vs. input voltage

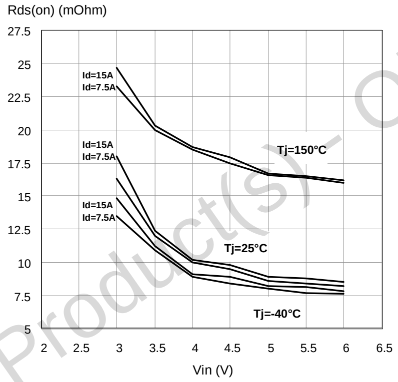


Figure 12. D^{2}PAK static drain-source on resistance vs. input voltage

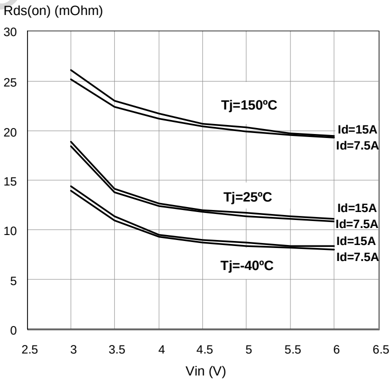


Figure 13. PowerSO-10 static drain-source on resistance vs. id

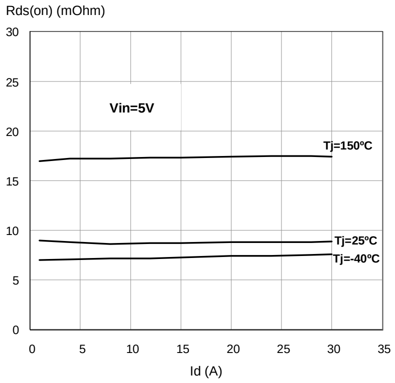


Figure 14. D^{2}PAK static drain-source on resistance vs. id

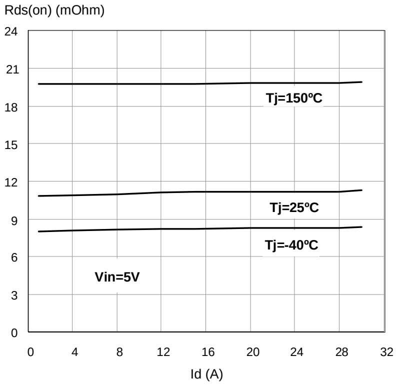


Figure 15. Transconductance

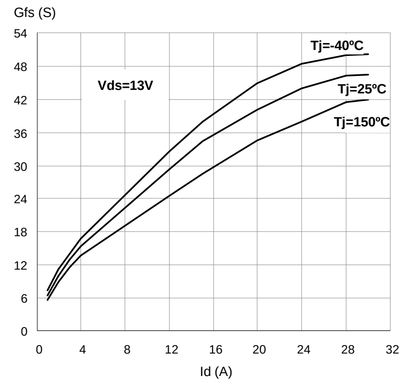


Figure 16. Transfer characteristics

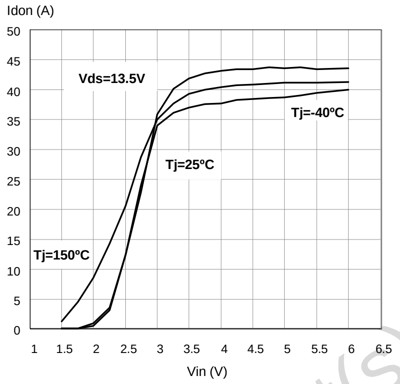


Figure 17. Output characteristics

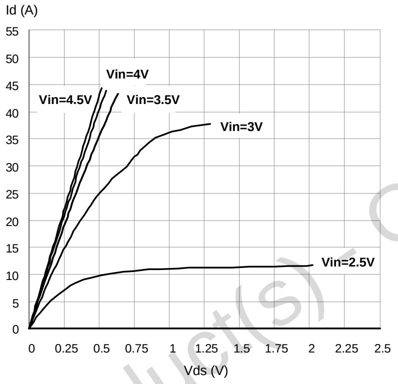


Figure 18. Normalized on resistance vs. temperature

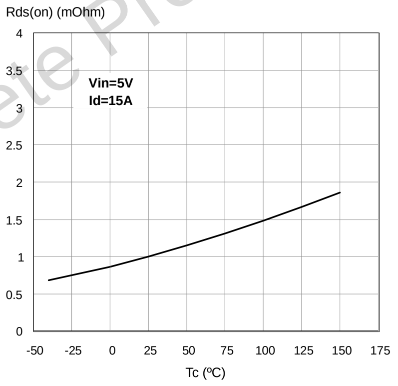


Figure 19. Turn-on current slope, V_{IN} = 5 V

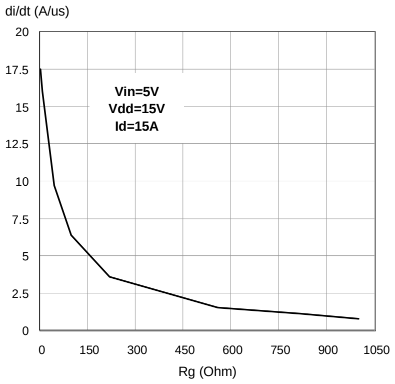


Figure 20. Turn-on current slope, V_{IN} = 3.5 V

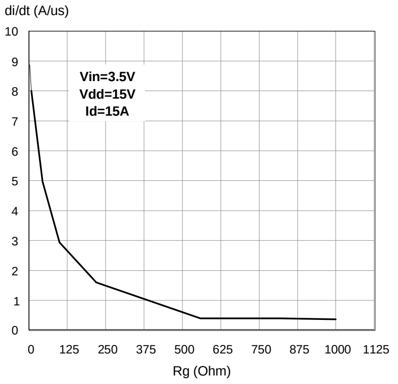


Figure 21. Input voltage vs. input charge

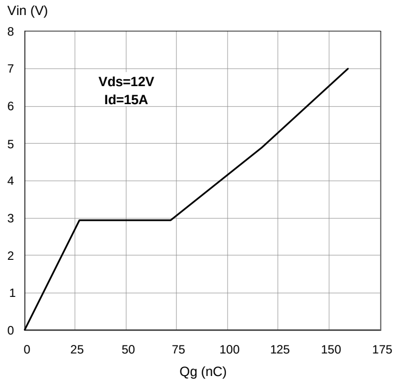


Figure 22. Turn-off drain source voltage slope, V_{IN} = 5 V

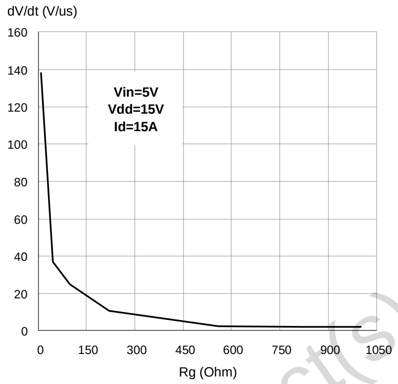


Figure 23. Turn-off drain-source voltage slope, V_{IN} = 3.5 V

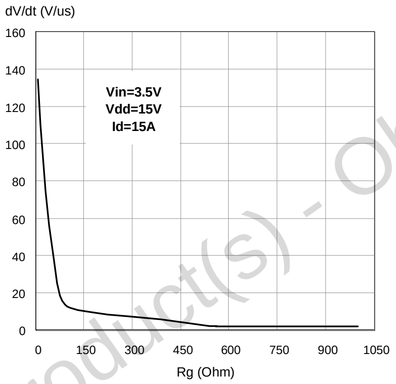


Figure 24. Switching time resistive load (part 1)

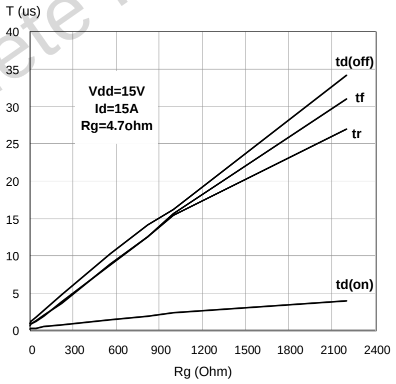


Figure 25. Switching time resistive load (part 2)

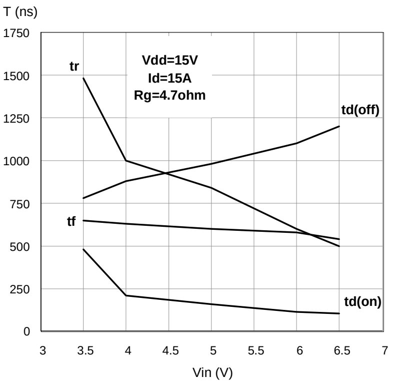


Figure 26. Normalized input threshold voltage vs. temperature

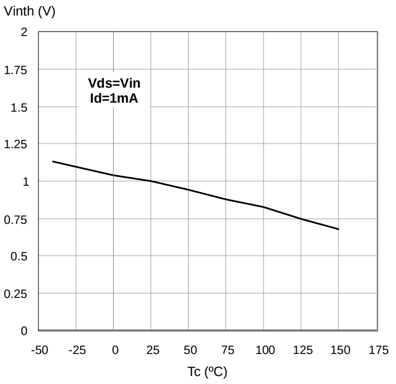


Figure 27. Current limit vs. junction temperature

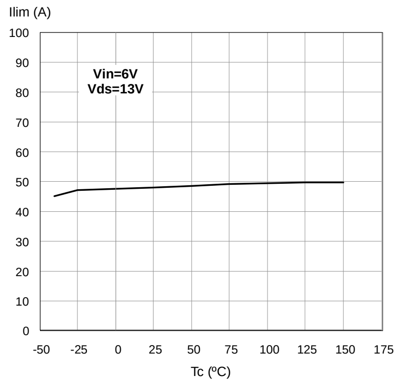


Figure 28. Step response current limit

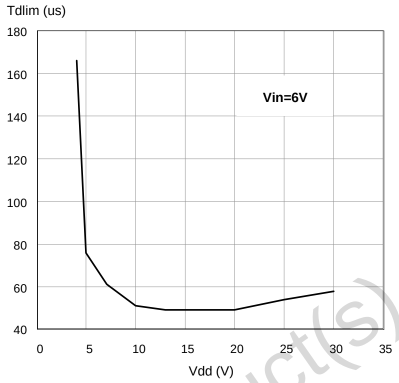
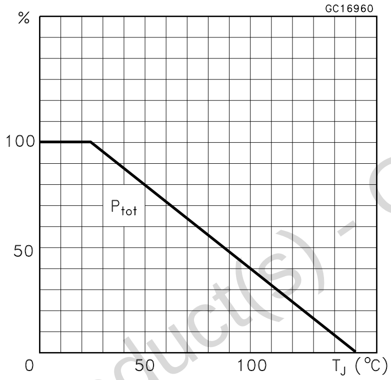


Figure 29. Derating curve



3 Package informantion

3.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

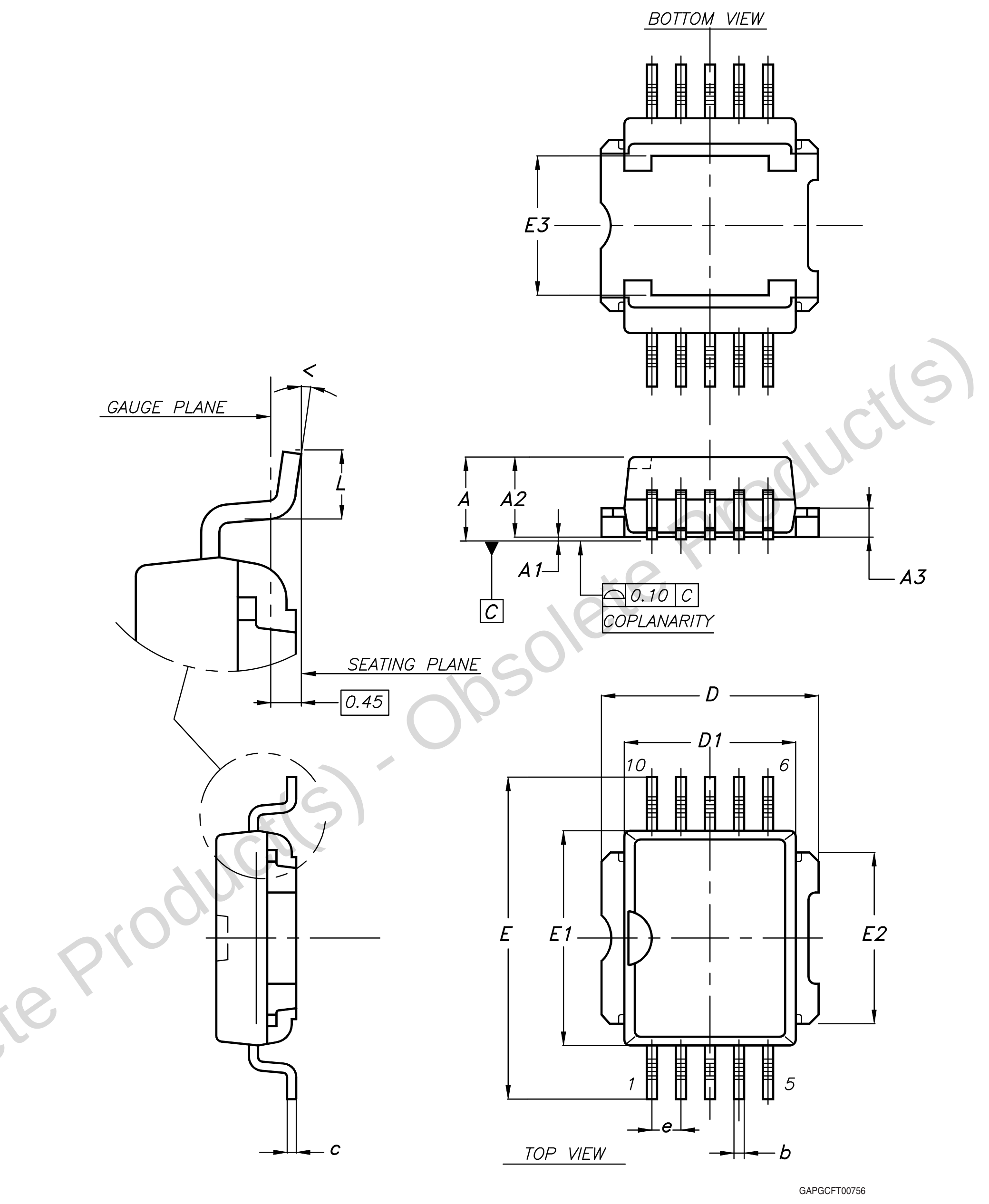
3.2 PowerSO-10 mechanical data

Table 9. PowerSO-10 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			3.70
A1	0.00		0.10
A2	3.40		3.60
A3	1.25		1.35
b	0.40		0.53
c	0.35		0.55
D	9.40		9.60
D1(1)	7.40		7.60
E	13.80		14.40
E1(1)	9.30		9.50
E2	7.20		7.60
E3	5.90		6.10
e		1.27	
L	0.95		1.65
<	0°		8°

1. Resin protrusion not included (max value: 0.20 mm per side)

Figure 30. PowerSO-10 package dimensions

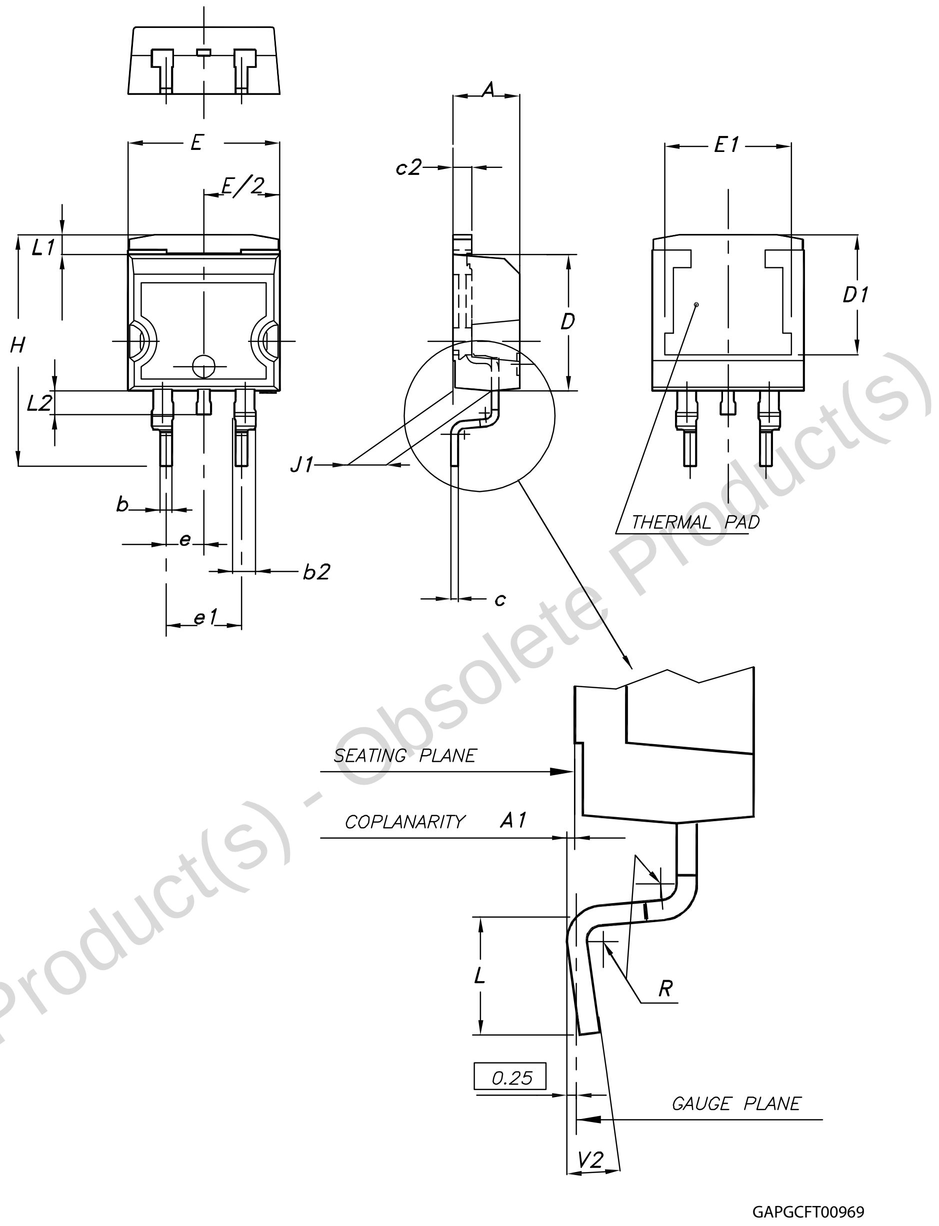


3.3 D²PAK mechanical data

Table 10. D²PAK mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 31. D^{2}PAK package dimensions



3.4 PowerSO-10 packing information

Figure 32. PowerSO-10 suggested pad layout

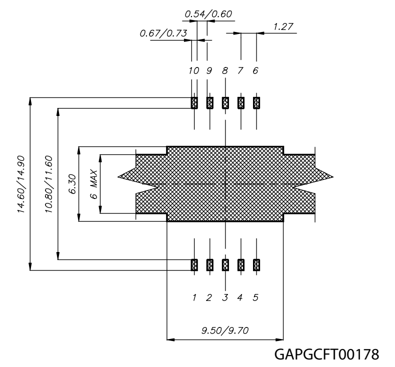
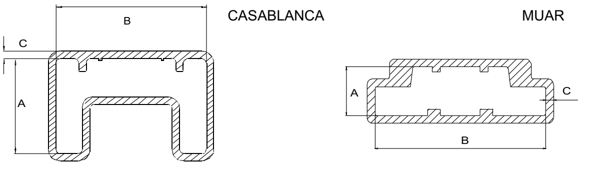


Figure 33. Tube shipment (no suffix)



All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

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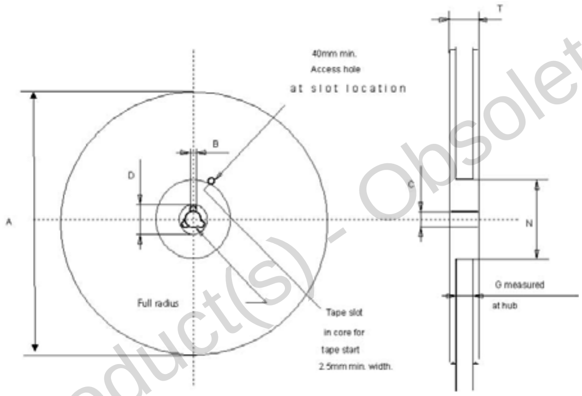
Figure 34. Tape and reel shipment (suffix “13TR”)



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

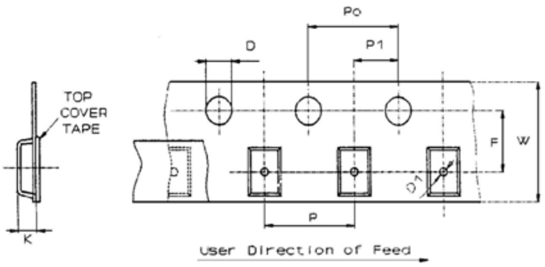
All dimensions are in mm.

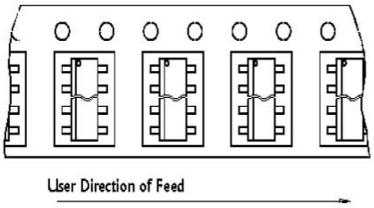
TAPE DIMENSIONS

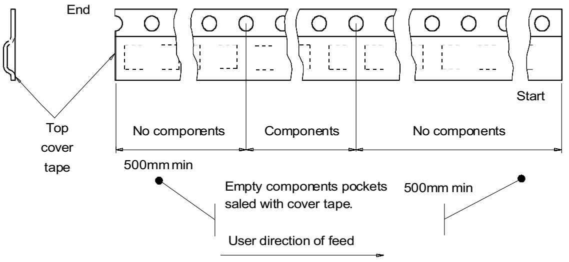
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.







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3.5 D²PAK packing information

Figure 35. D²PAK footprint

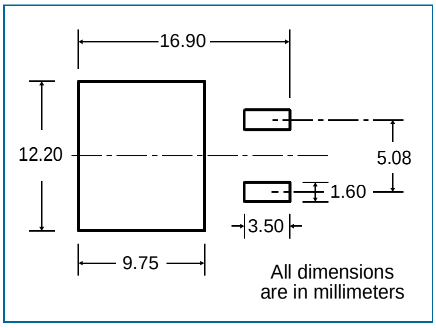
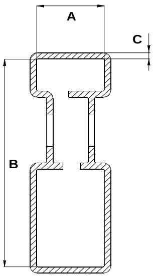


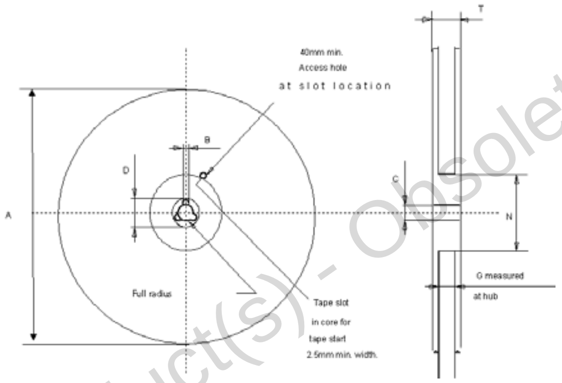
Figure 36. Tube shipment (no suffix)



Base Q.ty	50
Bulk Q.ty	500
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

Figure 37. Tape and reel shipment (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

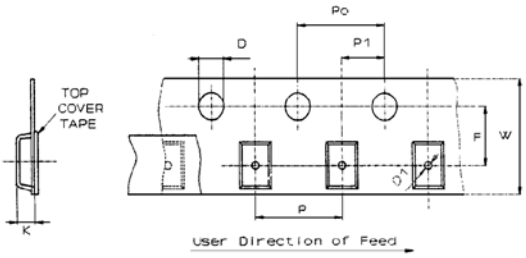
All dimensions are in mm.

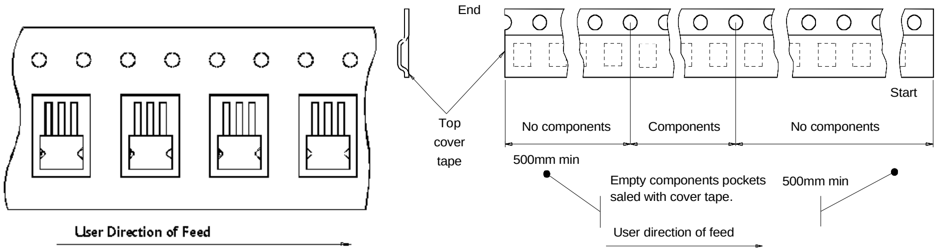
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	16
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.





4 Revision history

Table 11. Document revision history

Date	Revision	Changes
19-Sep-2012	1	Initial release. VNB35NV04 and VNV35NV04 were previously in document CD00002200 (Doc ID 7374) revision 5. Added *Section 3.1: ECOPACK®* Updated *Section 3.2: PowerSO-10 mechanical data* and *Section 3.3: D2PAK mechanical data*
17-Sep-2013	2	Updated disclaimer.

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