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PLESSEY Semiconductors

PRELIMINARY INFORMATION

T-75-33-07

SL9009

ADAPTIVE BALANCE CIRCUIT

The SL9009 is normally used to extract the received signal from the combined transmitted and received signal on a telephone line. It constantly analyses the extracted signal and adjusts to compensate for variations in telephone lines.

The device can be used with a bridge circuit where it acts as an impedance network which adjusts itself to match the telephone line. When the bridge is in balance the difference between its two arms is due to the received signal.

The SL9009 consists of three cells and a correlation detector which is normally used to control the cells via a negative feedback loop. It is built using bipolar technology.

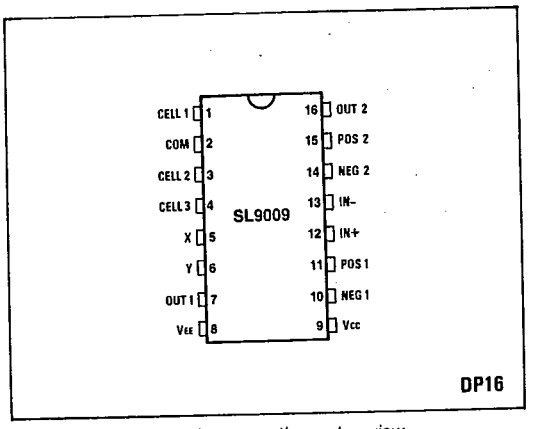

Fig.1 Pin connections - top view

FEATURES

- Extracts the Received Signal
- Adapts Automatically to Line Variations
- No Microprocessor Required
- Simple Application Circuit
- 40dB (Typ.) Rejection of Transmitted Signal

APPLICATIONS

- Modems - Extracting the Received Data
- Feature Phones - Extracting the Received Voice
- PBX/PABX/CO Line Cards - Extracting the Incoming Signal from the Telephone Line

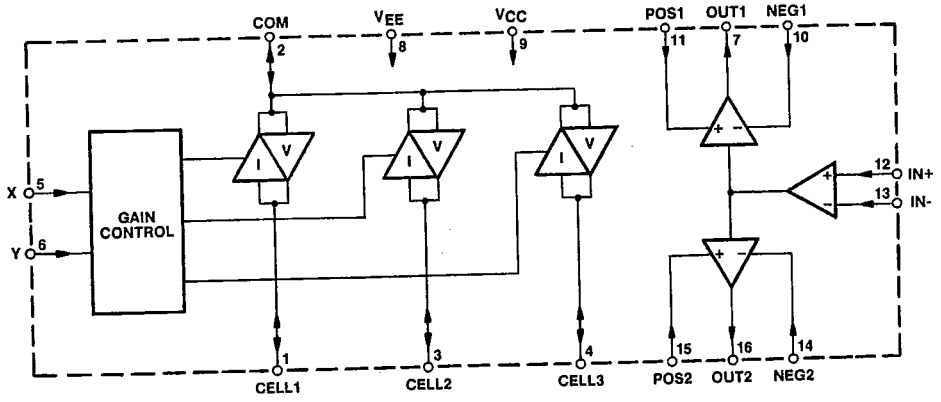

Fig.2 Functional block diagram

FUNCTIONAL DESCRIPTION

The SL9009 adaptive balance circuit is divided into two separate parts as shown in Fig.2. These are the impedance cell section and the phase detector section. The impedance cell section is normally used with a balanced impedance bridge circuit which allows the incoming signal to be extracted from the combined signal on the line.

The phase detector section is used to analyse the extracted signal to determine how much of the residual outgoing signal is present. This allows the circuit to adjust itself to minimise the residual signal automatically.

Impedance Cells

This consists of three cells and the gain controller (see Fig.2). Each cell has a voltage buffer and a variable gain current amplifier. The three cells share the COM pin (pin 2) which is the common input to their voltage buffers and the common output from their current amplifiers.

There is a pin directly associated with each cell. This is the CELL 1, 2 or 3 pin (pin 1, 3 or 4) and it is driven by the cell's voltage buffer. The current which is sunk or sourced at this pin is the input to the cell's current amplifier.

This means that the voltage developed at the COM pin causes a current to flow at each of the three individual cell pins (CELL 1, 2 and 3). These currents are amplified by the gains of the three cells and the sum is the current which flows in or out of the COM pin.

The gain of the cells are controlled by the X and Y gain control pins (pins 5 and 6). Fig.3 indicates how the two controls operate. The precise voltages at the control inputs necessary to give a defined gain vary with the power supplies, but this is compensated for by the feedback loop.

The gain control is characterised by a line of symmetry corresponding to a certain voltage on the Y pin. Above this voltage cell 2 is off and below it cell 3 is off. The line of symmetry also corresponds to the highest gain on cell 1 for a fixed voltage on the X pin.

In addition to the current due to the three impedance cells at the COM pin (pin 2), a DC bias current also flows. The value of this current depends on the power supplies and the voltage at the control inputs, especially the X pin.

If the currents at the cell pins (CELL 1 to 3) are too high then clipping will occur. If these pins are left open circuit then the device still presents a finite impedance at the COM pin, but this is very large.

Phase Detectors

The phase detector section consists of a differential voltage input buffer which drives the two phase analysers (see Fig.2). The input is taken from the IN+ and IN- pins (pins 12 and 13).

Each analyser consists of a transconductance amplifier which can have either a positive or negative gain. The sign of the gain is determined by the analysis pins for the detector. These are POS 1 and NEG 1 (pins 11 and 10) for detector 1 and POS 2 and NEG 2 (pins 15 and 14) for detector 2. The outputs of the transconductance amplifiers are connected to the OUT 1 and OUT 2 pins (pins 7 and 16).

The direction of the current at an output pin is determined by the phase relationship between the signal at the input and the signal at the analysis pins. The magnitude of the current depends on the magnitude of the input alone. If the analysis pins are in phase with the input then the output will source current. If they are 180° out of phase then the output will sink current. If they are 90° out of phase then the output will alternately sink and source current. If the input is small then the current sunk or sourced will be small.

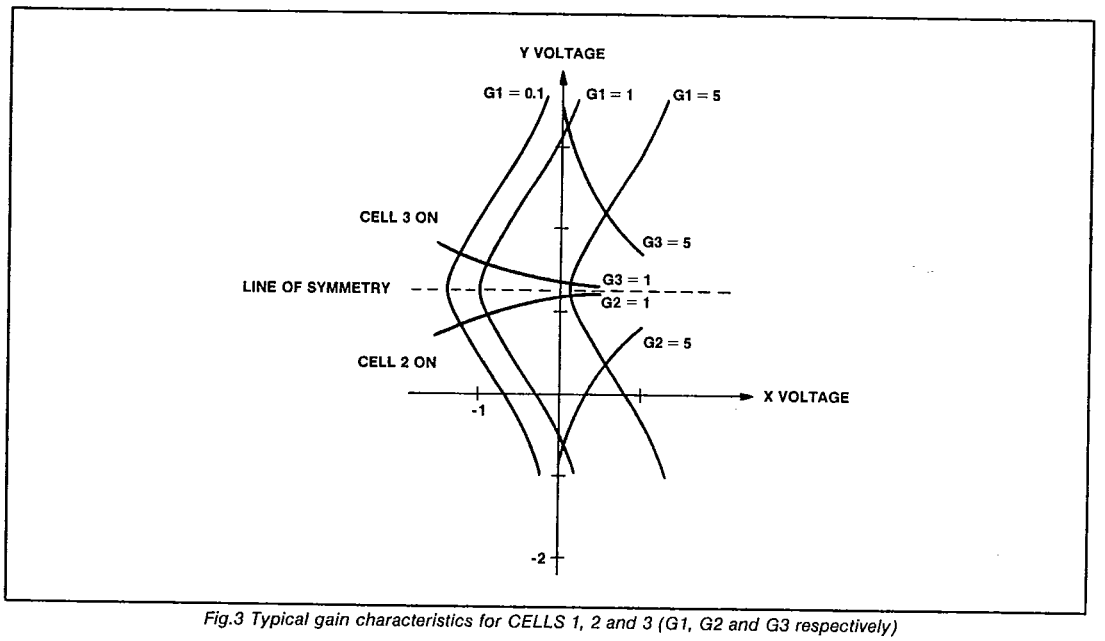

Fig.3 Typical gain characteristics for CELLS 1, 2 and 3 (G1, G2 and G3 respectively)

APPLICATIONS

Fig.4 shows a simple bridge configuration which can adjust the amplitude and phase over a wide range to match an unknown impedance, Z. In this case R1 is used to match R3; R2 is used to match the in-phase component across Z; C1 is used to produce phase lead and C2 is used to produce phase lag. The X and Y gain control inputs give two degrees of freedom which allow both in-phase and out-of-phase components to be balanced.

The feedback arrangement is shown in Fig.5. If the extracted signal is in phase with the transmitted signal then the OUT 1 pin (pin 7) will sink current (since the inverting NEG 1 pin is used) and so cause the voltage at the X pin (pin 5) to fall. This causes the gain of CELL 1 to fall and so produces less attenuation of the signal at the COM pin (pin 2). This means that more of the transmitted signal is subtracted from the combined signal.

If too much of the transmitted signal is subtracted then the extracted signal will become 180° out of phase with the transmitted signal. This produces the opposite effect and so reduces the amount of the transmitted signal which is subtracted.

Any remaining correlation between the transmitted singal and the extracted signal must be due to a lag or lead. If the extracted signal lags the transmitted signal by 90° then the derivative of the extracted signal is in phase with the transmitted signal (see Fig.6).

Applying the derivative of the extracted signal to the inverting NEG 2 pin causes the OUT 2 pin to sink current and so lowers the voltage at the Y pin (pin 6). This causes CELL 2 to switch on and increases its gain until balance occurs. Thus a lag is created (through C2 of Fig.4) in the signal which is subtracted from the combined signal, cancelling the lag in the extracted signal.

If the extracted signal leads the transmitted signal then the circuit causes CELL 3 to switch on and causes a lead (through C1 of Fig.4) in the signal at the COM pin. This cancels the lead in the extracted signal.

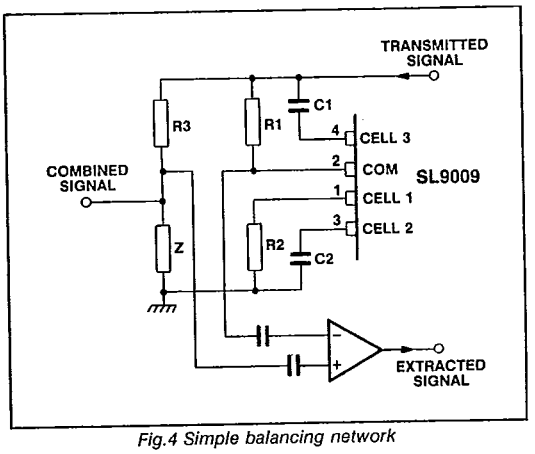

Fig.4 Simple balancing network

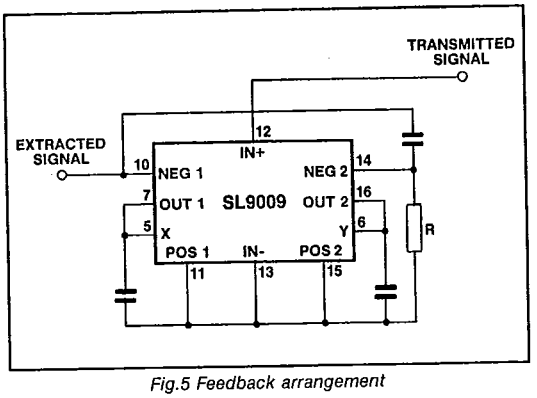

Fig.5 Feedback arrangement

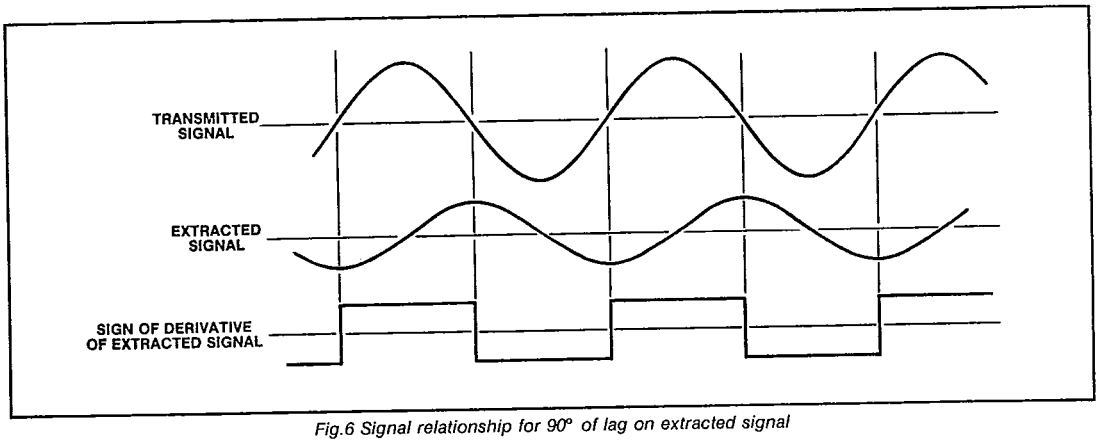

Fig.6 Signal relationship for 90° of lag on extracted signal

Use of a Gyrator Circuit

The transmitted signal may be connected to a telephone line through a transformer, which is often far from an ideal component and can effectively add a resistor and inductor in series to the line. The effect of this can be removed by adding the equivalent of these components, suitably scaled, to the bridge network. The problem of doing this is that although the values of resistance and inductance required may be well known, the scaled inductance may not be practical.

This may be overcome by using a gyrator circuit as shown in Fig.7. This circuit can be used instead of resistor R2 in Fig.4.

If $Z = (j\omega C)$ then the circuit looks like a resistance of R_A in series with an impedance of $L = R_A R_B / Z$. Realistic value for this circuit are $R_A = 5.1k\Omega$, $R_B = 180k\Omega$ and $C = 0.1\mu F$ giving $L = 91.8H$.

Improved Line Modelling

The simple balancing network shown in Fig.4 is capable of amplitude and phase compensation at a single frequency. To balance a telephone line across the voice band we build a model of the line and adjust it using the SL9009. Since the adjustments give good balance at any single frequency, the model ensures that good balance is achieved across the band.

A detailed application circuit making use of this approach is shown in Fig.8. The transmitted signal is output through the termination impedance and on to the line where it forms part of the combined line signal.

The transmitted signal is also passed to the termination balancing impedance and the line balancing impedance to generate the initial expected signal. The line balancing impedance should take account of the resistance and inductance introduced if a line transformer is used, possibly by using a gyrator circuit as previously described.

If the line balancing impedance matches the line impedance then the difference between the combined line signal and the initial expected signal is the received signal. In this special case all components of the transmitted signal wuld be cancelled without using an SL9009.

In most cases, however, the line impedance does not match the line balancing impedance. The SL9009 can then be used to compensate for the mismatch, as shown in Fig.8.

The initial expected signal is fed to the SL9009 which generates the final expected signal. It is the final expected signal which is subtracted from the combined line signal to give the extracted signal. The SL9009 generates the final expected signal by comparing the initial expected signal with the in-phase and the out-of-phase components of the extracted signal as in the case of the simple balancing network.

To be more precise, the SL9009 generates the final expected signal times two thirds. This is multiplied by 1.5 before it is subtracted from the combined line signal. The signal generated by the SL9009 is always less than the initial expected signal so multiplying it by 1.5 enables the final expected signal to be greater than the initial expected signal.

By using the SL9009 to adjust the best estimate of the effect of the line impedance in this way, better balancing can be achieved for broadband voice signals.

A complete circuit which can be used in a modem or in a sophisticated telephone is shown in Fig.9.

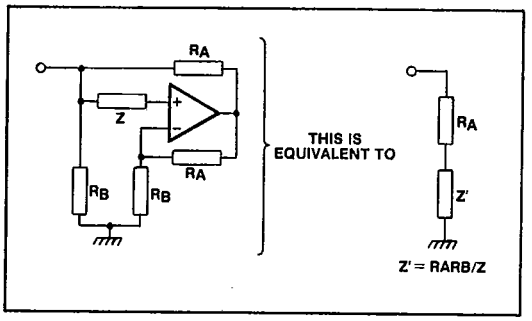

Fig.7 Gyrator circuit

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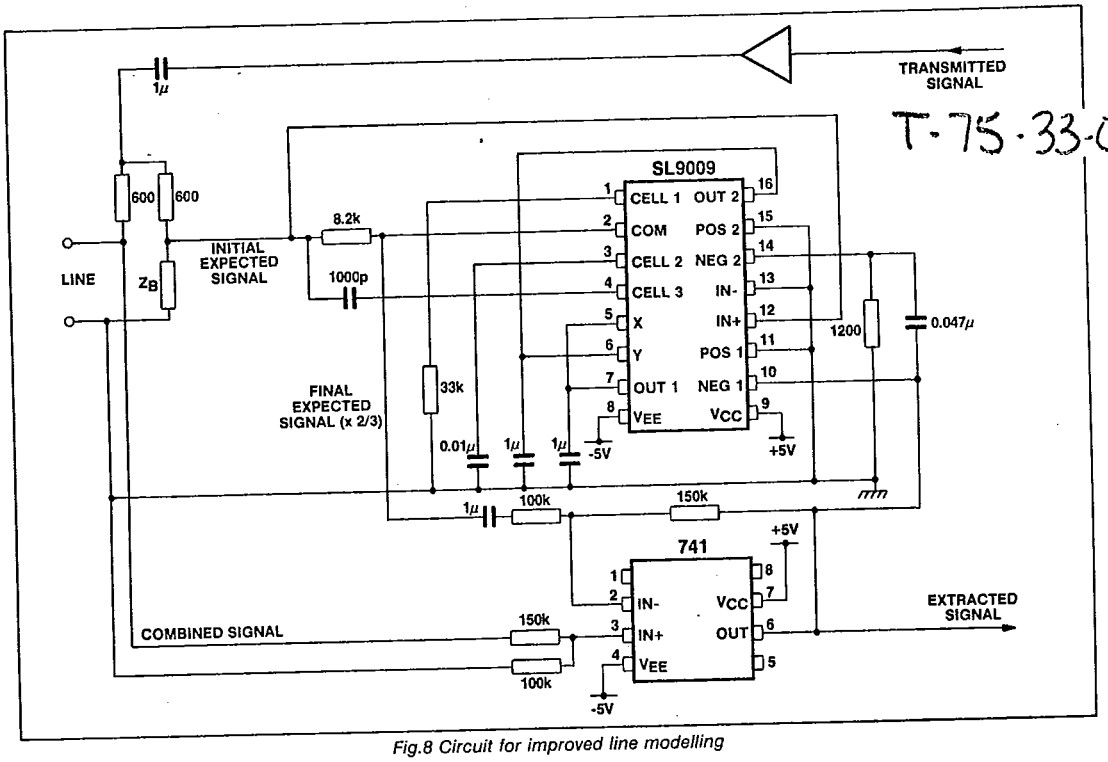
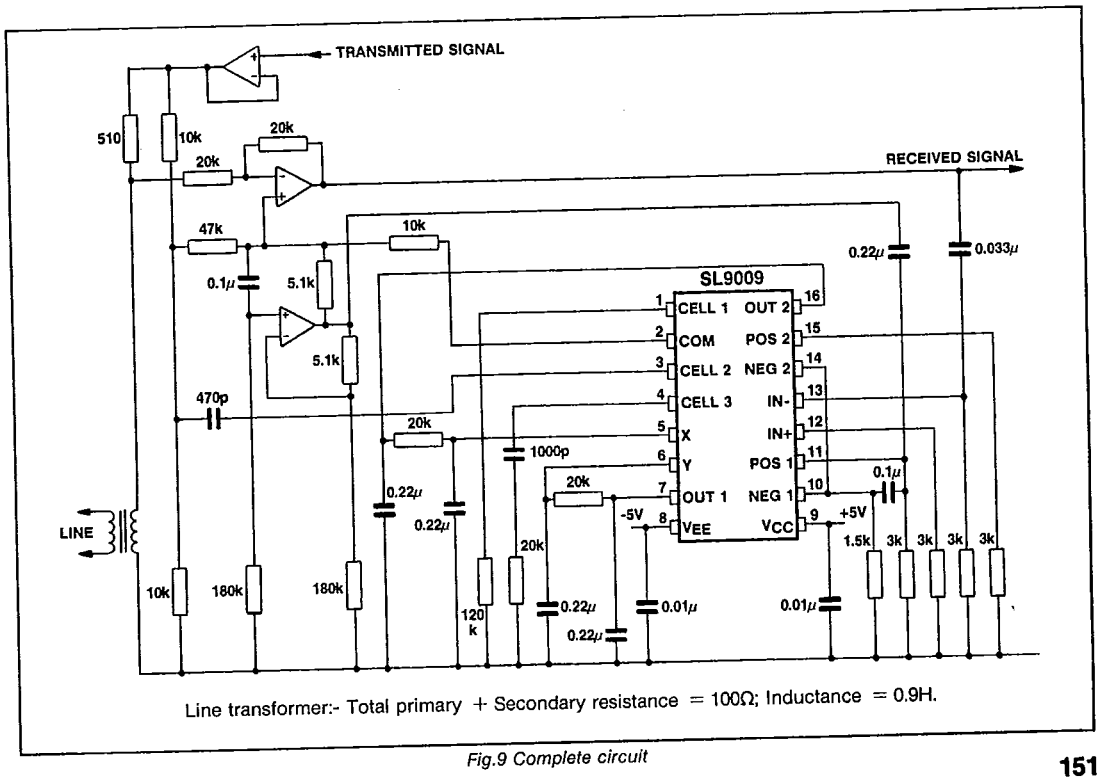


Fig.8 Circuit for improved line modelling



Line transformer:- Total primary + Secondary resistance = 100Ω; Inductance = 0.9H.

Fig.9 Complete circuit

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
CELL 1, CELL 2, CELL 3	1,3,4	**CELL 1, 2 and 3 Pins (Voltage Outputs and Current inputs).** These are the pins which are directly associated with CELLS 1, 2 and 3. The voltage developed at the common cell pin (pin 2) is buffered and output at these pins, causing them to sink or source currents. The currents flowing in or out of these pins act as inputs which are amplified by the gains of the cells and the amplified currents are summed and returned to the common cell pin as its output current. The gains of the cells are determined by the gain control pins (pins 5 and 6).
COM	2	**Common Cell Pin (Voltage Input and Current Output).** The voltage developed at this pin is buffered and output at the separate cell pins (pins 1, 3 and 4). The currents output by the 3 cells are summed and the result is the current which is sunk or sourced at this pin.
X	5	**X Gain Control (Voltage Input).** Increasing the voltage at this pin increases the gain of CELL 1 and also of CELL 2 and CELL 3, but to a lesser extent (see Fig.3).
Y	6	**Y Gain Control (Voltage Input).** Increasing the voltage at this pin from a low value decreases the gain of CELL 2 until it switches off. At this point CELL 3 switches on and increasing the voltage further causes the gain of CELL 3 to increase (see Fig.3). The gain of CELL 1 increases as the voltage at this pin increases from a low value until CELL 2 switches off. Further increasing the voltage causes the gain of CELL 1 to decrease.
OUT 1	7	**Detector 1 Output (Current Output).** This is the output of phase detector 1. The current sunk or sourced at this pin is proportional to the differential voltage between the detector input pins (pins 12 and 13). The sign of the transconductance gain (i.e. of the constant of proportionality) is controlled by the detector 1 analysis pins (pins 11 and 10). The direction of the average current output is determined by the phase relationship between the input and the analysis pins and the magnitude is determined by the input alone.
V_{EE}	8	**Negative Supply (Power Input).** This is the negative power supply for the device.
V_{CC}	9	**Positive Supply (Power Input).** This is the positive power supply for the device.
NEG 1, POS 1	10,11	**Detector 1 Analysis - Negative and Positive (Voltage Inputs).** These pins determine the sign of the transconductance gain from the differential detector input voltage (pins 12 and 13) and the current on the output of detector 1 (pin 7).
IN +, IN-	12,13	**Detector Input Negative and Positive (Voltage Inputs).** These pins form the differential voltage input to the phase detectors.
NEG 2, POS 2	14,15	**Detector 2 Analysis - Positive and Negative (Voltage Inputs).** These pins determine the sign of the transconductance gain from the differential detector input voltage (pins 12 and 13) and the current on the output of detector 2 (pin 16).
OUT 2	16	**Detector 2 Output (Current Output).** This is the output of phase detector 2. The current sunk or sourced at this pin is proportional to the differential voltage between the detector input pins (pins 12 and 13). The sign of the transconductance gain (i.e. of the constant of proportionality) is controlled by the detector 2 analysis pins (pins 14 and 15). The direction of the average current output is determined by the phase relationship between the input and the analysis pins and the magnitude is determined by the input alone.

ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Positive supply voltage (pin 9), V_{CC}	-0.3V to +10V
Negative supply voltage (pin 8), V_{EE}	-10V to +0.3V
Input voltages (pins 2,5,6,10,11, 12,13,14 and 15), V_I	V_{EE} to V_{CC}
Output voltages (pins 1,3,4,7,16), V_O	V_{EE} to V_{CC}
Cell voltage (pins 1,.3,4) minus Common voltage (pin 2), V_C	-5V to +5V
Storage temperature, T_{ST}	-10°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions - Voltages are with respect to digital ground (V_{DGND} [V_{CC} - V_{EE}]/2)

Characteristic	Symbol	Value			Units
		Min.	Typ.(1)	Max.	
Positive supply voltage (pin 9)	V_{CC}	4.5	5	7.0	V
Negative supply voltage (pin 8)	V_{EE}	-7.0	-5	-4.5	V
Ambient temperature	T_{amb}	0		70	°C
Common cell pin voltage (pin 2)	V_{COM}	V_{EE} +2.7		V_{CC} -2	V
Cell input currents (pins 1,3 and 4)	I_{CELL}	-10		10	μA
X control voltage (pin 5)	V_X	V_{EE} +2.7		V_{EE} -6.0	V
Y control voltage (pin 6)	V_Y	-2.0		1.8	V
Detector input voltages (pins 12 and 13)	V_{IN}	V_{EE} +2.7		V_{CC} -2.7	V
Analysis input voltages (pins 10,11,14 and 15)	V_A	V_{EE} +2.7		V_{CC} -2.7	V
Detector output voltages (pins 7 and 16)	V_{OUT}	V_{EE} +2.5		V_{CC} -2	V

Operating Characteristics: General - Voltages are with respect to ground (V_{GND} = [V_{CC} - V_{EE}]/2)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Power dissipation	P_D			30	mW	
Supply current	I_{CC}		1.3	15	mA	
Pin capacitance	C_P		7	15	pF	Pin to supplies

Operating Characteristics: Cells - Voltages are with respect to ground (V_{GND} = [V_{CC} - V_{EE}]/2)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Internal resistance (pins 1, 3 and 4)	R_I	3		14	kΩ	
Control input leakage (pins 5 and 6)	I_C			0.12	μA	
Minimum cell gain	G_{MIN}		0.05			
Maximum cell gain	G_{MAX}		10			
DC bias current (pin 2)	I_{BDC}	-12	0	12	μA	
Residual impedance (pin 2)	Z_R	500			kΩ	Cell pins open circuit

Operating Characteristics: Detectors - Voltages are with respect to ground (V_{GND} = [V_{CC} - V_{EE}]/2)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Differential input offset (pins 10 to 15)	V_{DOFF}			13	mV	
Input offset current (pins 10 to 15)	I_{OFF}	-0.15		0.15	μs	
Input bias current (pins 10 to 15)	I_{IB}		0.1	0.7	μA	
Transconductance gain	G_T	250	500	1000	μΩ	Magnitude
Output offset current (pins 7 and 16)	I_{OFF}	-1.2		1.2	μA	
Maximum output current (pins 7 and 16)	I_{MAX}		50		μA	Sink or Source
Output impedance (pins 7 and 16)	Z_{OUT}		5		MΩ	

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.