

TrenchMOS™ transistor

Standard level FET

PHP87N03T

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in DC-DC converters and general purpose switching applications.

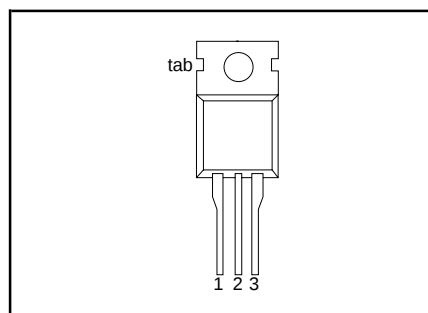
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC) ¹	75	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 10\text{ V}$	10.5	mΩ

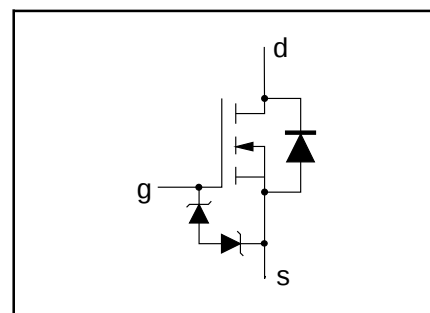
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
I_D	Drain current (DC) ¹	$T_{mb} = 25\text{ °C}$	-	75	A
I_D	Drain current (DC)	$T_{mb} = 100\text{ °C}$	-	61	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\text{ °C}$	-	240	A
P_{tot}	Total power dissipation	$T_{mb} = 25\text{ °C}$	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

¹ Current limited by package to 75A from a theoretical value of 87A.

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ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 k Ω)	-	2	kV

STATIC CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.25\text{ mA}$; $T_j = -55^\circ\text{C}$	30 27	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1\text{ mA}$	2	3.0	4.0	V
		$T_j = 175^\circ\text{C}$	1	-	-	V
		$T_j = -55^\circ\text{C}$	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 30\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175^\circ\text{C}$	-	0.05	10	μA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 175^\circ\text{C}$	-	0.02	1	μA
			-	-	20	μA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = \pm 1\text{ mA}$; $T_j = 175^\circ\text{C}$	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 175^\circ\text{C}$	- -	9 -	10.5 19.5	m Ω m Ω

DYNAMIC CHARACTERISTICS

 $T_{mb} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}$; $I_D = 25\text{ A}$	9	18	-	S
$Q_{g(tot)}$	Total gate charge	$I_D = 75\text{ A}$; $V_{DD} = 24\text{ V}$; $V_{GS} = 10\text{ V}$	-	51	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	29	-	nC
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$	-	2700	3300	pF
C_{oss}	Output capacitance		-	700	800	pF
C_{rss}	Feedback capacitance		-	300	330	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 25\text{ V}$; $I_D = 25\text{ A}$;	-	26	30	ns
t_r	Turn-on rise time	$V_{GS} = 10\text{ V}$; $R_G = 5\ \Omega$	-	35	85	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	50	60	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	$I_F = 25\text{ A}; V_{GS} = 0\text{ V}$	-	0.95	1.2	V
		$I_F = 75\text{ A}; V_{GS} = 0\text{ V}$	-	1.0	-	V
t_{rr}	Reverse recovery time	$I_F = 75\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	95	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = -10\text{ V}; V_R = 25\text{ V}$	-	0.15	-	μC

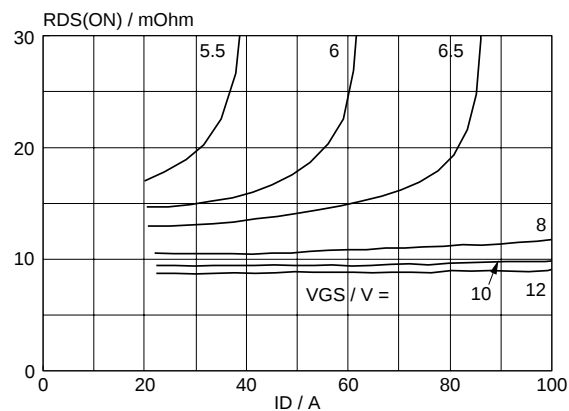
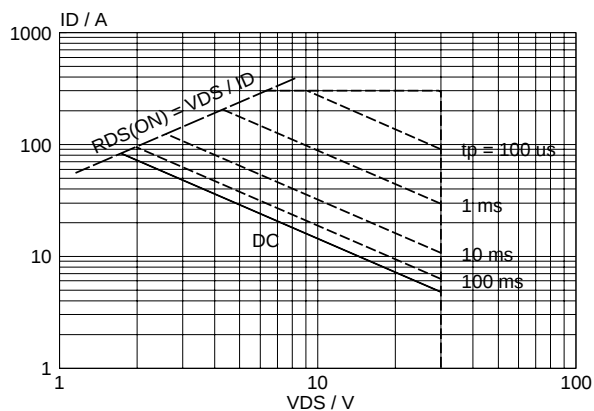
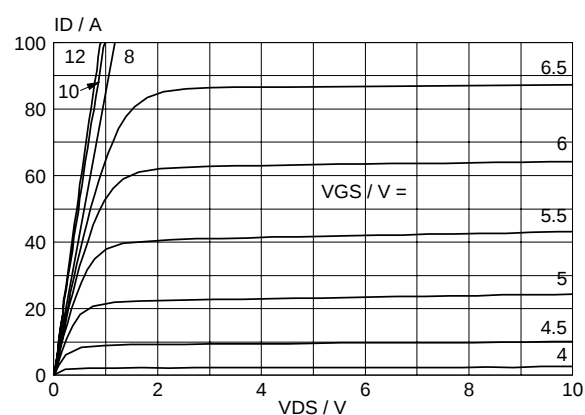
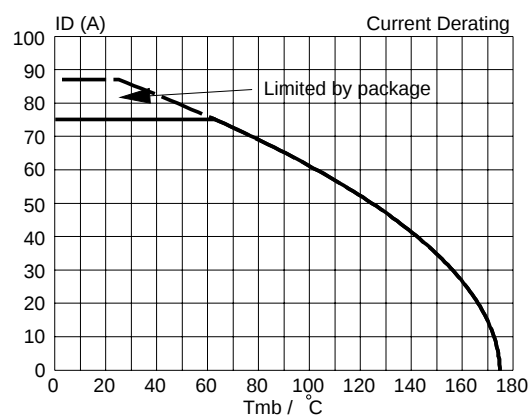
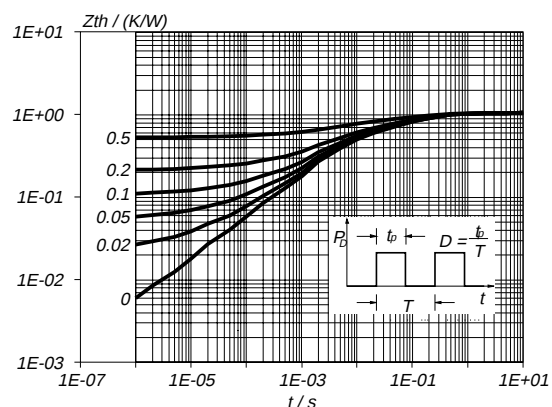
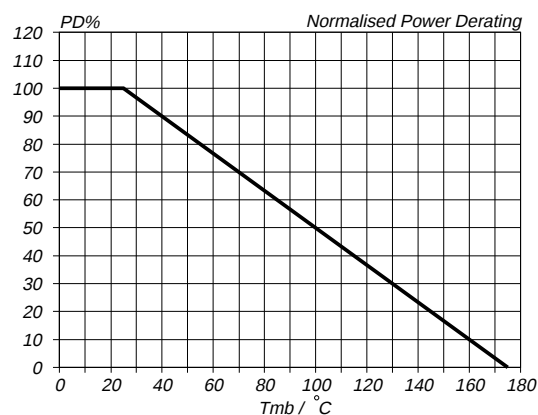
AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 45\text{ A}; V_{DD} \leq 15\text{ V};$ $V_{GS} = 10\text{ V}; R_{GS} = 50\ \Omega; T_{mb} = 25^\circ\text{C}$	-	-	200	mJ

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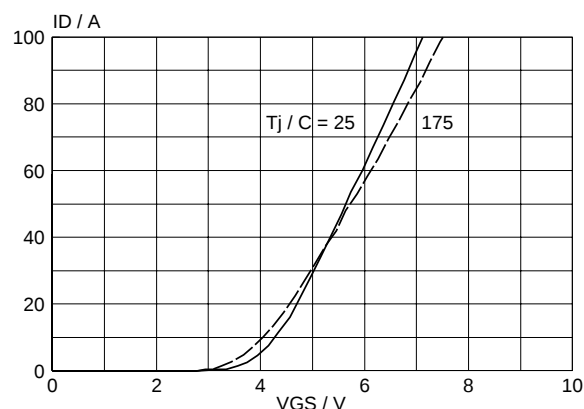


Fig. 7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25 \text{ V}$; parameter T_j

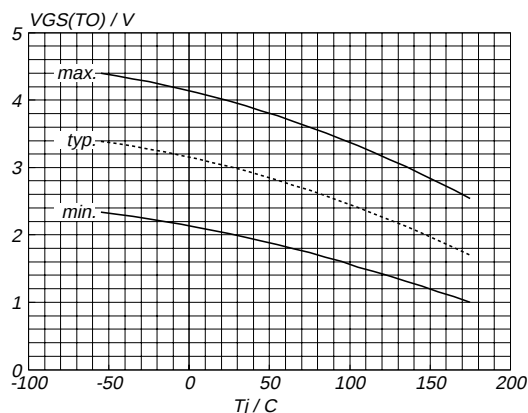


Fig. 10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

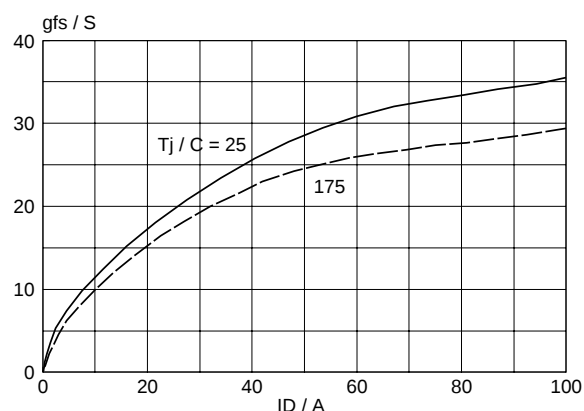


Fig. 8. Typical transconductance, $T_j = 25^\circ \text{C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25 \text{ V}$

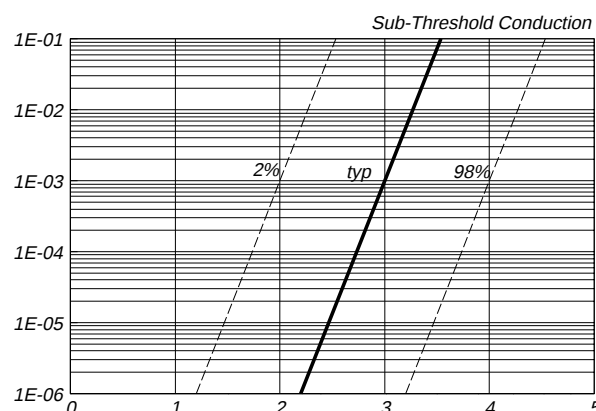


Fig. 11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25^\circ \text{C}$; $V_{DS} = V_{GS}$

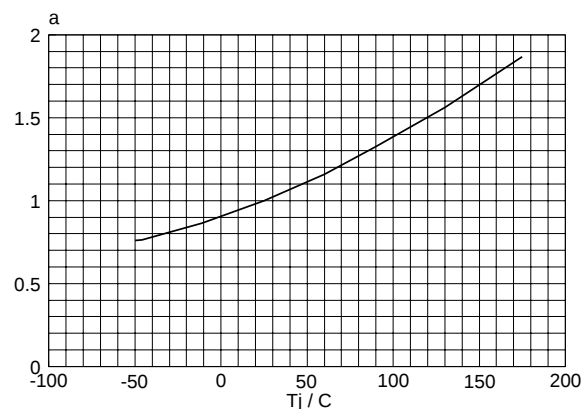


Fig. 9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ \text{C}} = f(T_j)$; $I_D = 25 \text{ A}$; $V_{GS} = 10 \text{ V}$

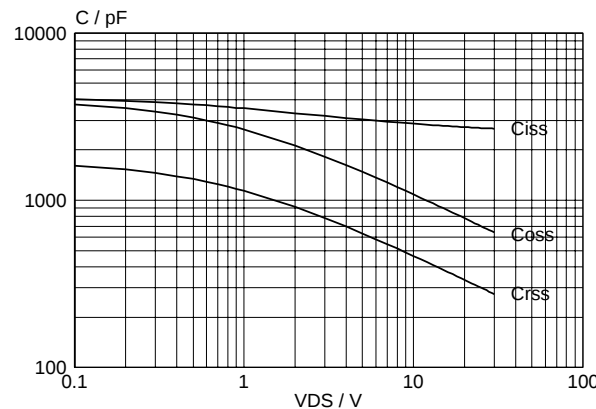


Fig. 12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

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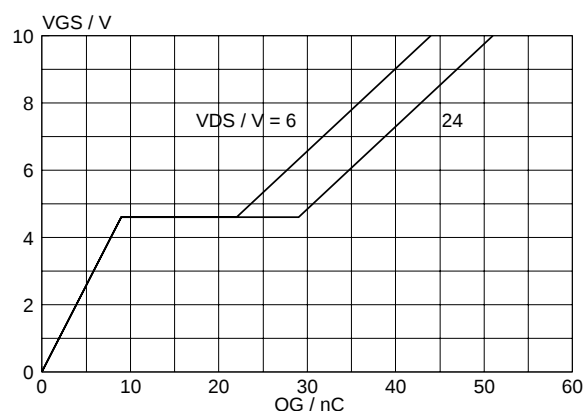


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 75\text{ A}$; parameter V_{DS}

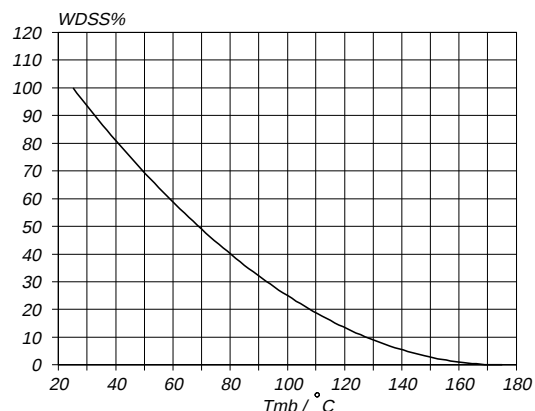


Fig.15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 45\text{ A}$

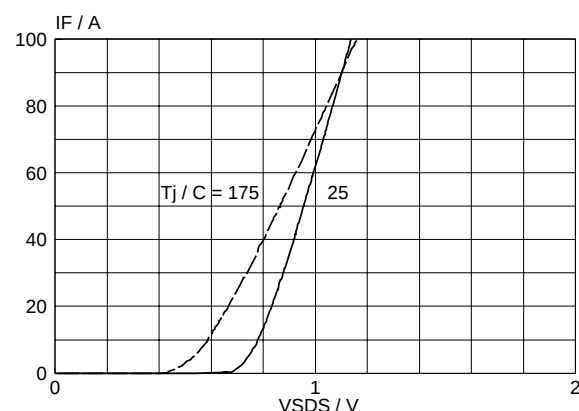


Fig.14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_j

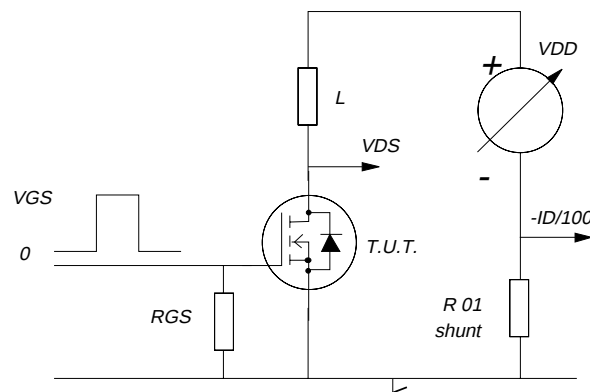


Fig.16. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

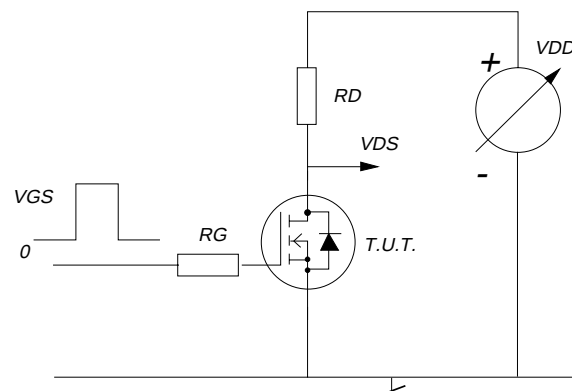


Fig.17. Switching test circuit.

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MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

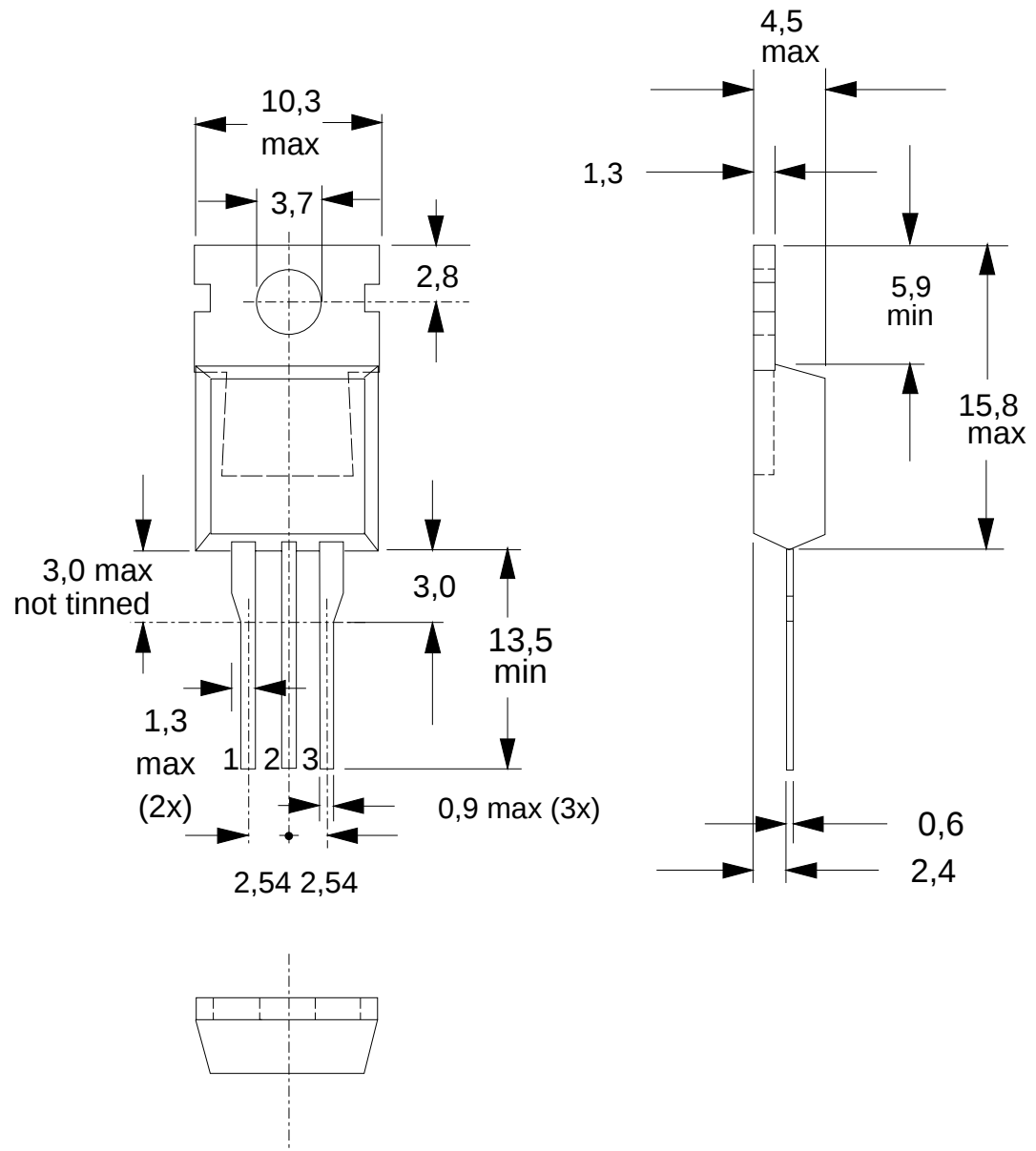


Fig.18. TO220AB; pin 2 connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for TO220 envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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