

I²C BUS Control 5-Input 2-Output AV Switch Monolithic IC MM1313

Outline

This IC is a 5-input 2-output AV switch with I²C control, developed for use in televisions. Two outputs enable it to support two screens or "picture-in-picture".

Features

1. Serial control by I²C bus.
2. 5-inputs, 2-outputs.
3. Video and audio system switches can be controlled independently.
4. 6dB amplifier built in to video system.
5. Built-in Y/C MIX circuit.
6. Slave address can be changed : 90H or 92H.
7. Audio muting possible by external pin.
8. Maintains high impedance even when I²C BUS line (SDA, SCL) power supply is off.
9. Built-in 3 value discrimination function.
10. On-chip power ON reset function.
11. Two types of audio input impedance : 60k Ω and 30k Ω .
 MM1313AD : 60k Ω MM1313BD : 30k Ω
12. Supports 2-screen or P-IN-P TV.

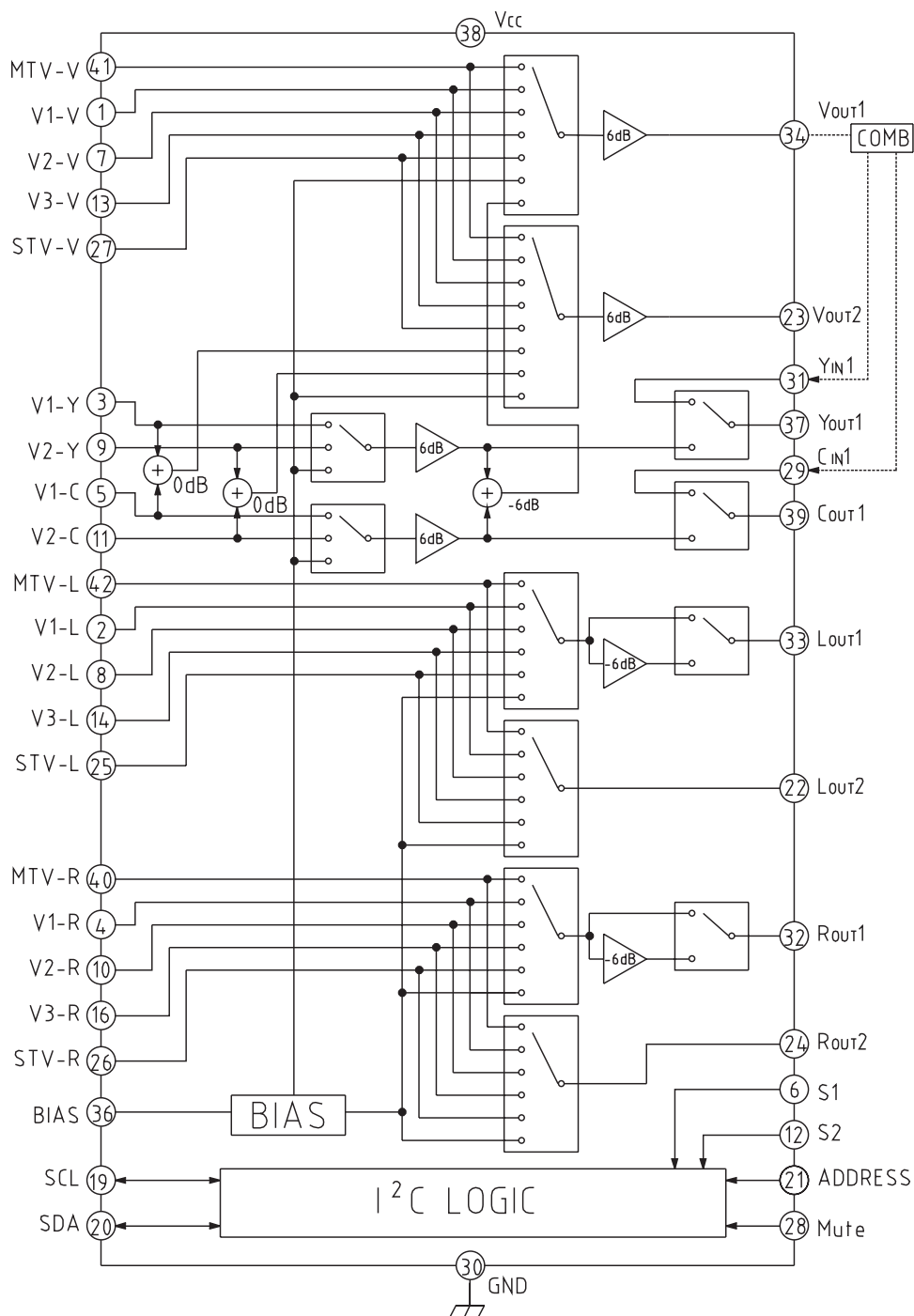
Package

SDIP-42A (MM1313AD, MM1313BD)

Applications

1. Televisions
2. Other video equipment

Equivalent Block Diagram



Pin Function

Pin No.	Name	Internal equivalent circuit diagram	Pin No.	Name	Internal equivalent circuit diagram
41 1 7 13 27 3 9 31	MTV-V V1-V V2-V V3-V STV-V V1-Y V2-Y Y _{IN1}		33 22 32 24	L _{OUT1} L _{OUT2} R _{OUT1} R _{OUT2}	
5 11 29	V1-C V2-C C _{IN1}		36	BIAS	
42 2 8 14 25 40 4 10 16 26	MTV-L V1-L V2-L V3-L STV-L MTV-R V1-R V2-R V3-R STV-R		19	SCL	
34 23	V _{OUT1} V _{OUT2}		20	SDA	
37 39	Y _{OUT1} C _{OUT1}		6 12 21 28	S1 S2 ADR Mute	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Power supply voltage	V _{CC}	12	V
Allowable power dissipation	P _d	850	mW

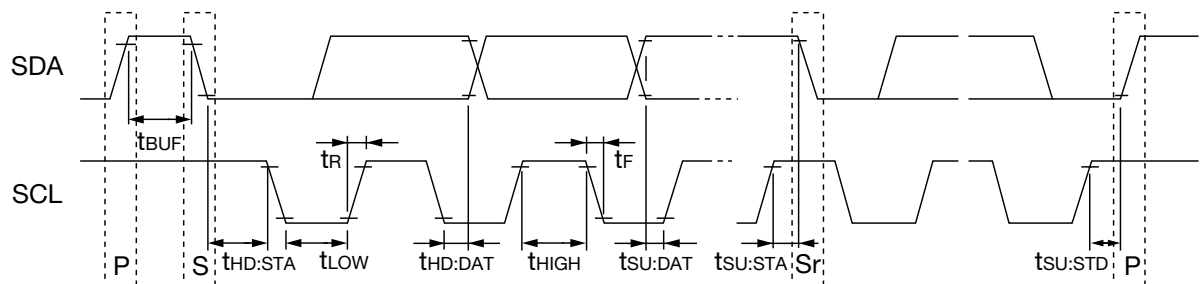
Electrical Characteristics (Ta=25°C, V_{CC}=9V)

Item	Symbol	Measure ment pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Operating power supply voltage	V _{CC}			8	9	10	V
Current consumption	I _{CC}	38	V _{CC} =9V, no signal, no load		40	52	mA
V_{OUT1} output							
Voltage gain	G _{V1}	TP1	Sine wave 1.0V _{P-P} , 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	F _{V1}	TP1	Sine wave 1.0V _{P-P} , 10MHz/100kHz	-1.0	0	1.0	dB
Differential gain	DG _{V1}	TP1	V _n -V : Staircase 1V _{P-P} APL=10~90%	-3	0	3	%
			V _n -Y : Staircase (luminance signal) 1V _{P-P} V _n -C : Chroma signal 0.3V _{P-P} APL=10~90%				
Differential phase	DP _{V1}	TP1	V _n -V : Staircase 1V _{P-P} APL=10~90%	-3	0	3	deg
			V _n -Y : Staircase (luminance signal) 1V _{P-P} V _n -C : Chroma signal 0.3V _{P-P} APL=10~90%				
Input dynamic range	D _{V1}	SG1~3	Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V _{P-P}
V_{OUT2} output							
Voltage gain	G _{V2}	TP6	Sine wave 1.0V _{P-P} , 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	F _{V2}	TP6	Sine wave 1.0V _{P-P} 10MHz/100kHz	-1.0	0	1.0	dB
Differential gain	DG _{V2}	TP6	V _n -V : Staircase 1V _{P-P} APL=10~90%	-3	0	3	%
			V _n -Y : Staircase (luminance signal) 1V _{P-P} V _n -C : Chroma signal 0.3V _{P-P} APL=10~90%				
Differential phase	DP _{V2}	TP6	V _n -V : Staircase 1V _{P-P} APL=10~90%	-3	0	3	deg
			V _n -Y : Staircase (luminance signal) 1V _{P-P} V _n -C : Chroma signal 0.3V _{P-P} APL=10~90%				
Input dynamic range	D _{V2}	SG1~3	Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V _{P-P}
Y_{OUT1} output							
Voltage gain	G _{Y1}	TP2	V _n -Y : Sine wave 1.0V _{P-P} , 100kHz	5.5	6.0	6.5	dB
	G _{Y2}	TP2	Y _{IN1} : Sine wave 2.0V _{P-P} , 100kHz	-0.5	0	0.5	
Frequency characteristics	F _{Y1}	TP2	V _n -Y : Sine wave 1.0V _{P-P} 10MHz/100kHz	-1.0	0	1.0	dB
	F _{Y2}	TP2	Y _{IN1} : Staircase 2.0V _{P-P} 10MHz/100kHz	-1.0	0	1.0	
Differential gain	DG _Y	TP2	V _n -Y : Staircase 1V _{P-P} APL=10~90%	-3	0	3	%
			Y _{IN1} : Staircase 2V _{P-P} APL=10~90%				
Differential phase	DP _Y	TP2	V _n -Y : Staircase 1V _{P-P} APL=10~90%	-3	0	3	deg
			Y _{IN1} : Staircase 2V _{P-P} APL=10~90%				

Item	Symbol	Measure ment pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Input dynamic range	Dy1	SG2	V _{n-Y} : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V _{P-P}
	Dy2	SG4	V _{IN1} : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	3.2	3.8		
Output impedance	Z _{OYC1}				50		Ω
C_{OUT1} output							
Voltage gain	G _{C1}	TP3	V _{n-C} : Sine wave 1.0V _{P-P} , 100kHz	5.5	6.0	6.5	dB
	G _{C2}	TP3	C _{IN1} : Sine wave 2.0V _{P-P} , 100kHz	-0.5	0	0.5	
Frequency characteristics	F _{C1}	TP3	V _{n-C} : Sine wave 1.0V _{P-P} 10MHz/100kHz	-1.0	0	1.0	dB
	F _{C2}	TP3	C _{IN1} : Sine wave 2.0V _{P-P} 10MHz/100kHz	-1.0	0	1.0	
Differential gain	DG _C	TP3	C _{IN1} : Staircase 2V _{P-P} APL=10~90%	-3	0	3	%
Differential phase	DP _C	TP3	C _{IN1} : Staircase 2V _{P-P} APL=10~90%	-3	0	3	deg
Input dynamic range	D _{C1}	SG3	V _{n-C} : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	2.75	3.25		V _{P-P}
	D _{C2}	SG5	C _{IN1} : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	5.5	6.5		
Input impedance	Z _{IC}		V _{n-C} , C _{IN1}	10	15	20	kΩ
Output impedance	Z _{OC1}				50		Ω
L_{OUT1} output							
Voltage gain	G _{L11}	TP4	b7=0, Sine wave 2.5V _{P-P} , 1kHz	-6.5	-6.0	-5.5	dB
	G _{L12}	TP4	b7=1, Sine wave 2.5V _{P-P} , 1kHz	-0.5	0.0	0.5	
Frequency characteristics	F _{L1}	TP4	Sine wave 2.5V _{P-P} , 1MHz/1kHz	-3.0	0	1.0	dB
Total higher harmonic distortion	THD _{L1}	TP4	Sine wave 2.5V _{P-P} , 1kHz		0.03	0.1	%
Input dynamic range	D _{L1}	SG6	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		V _{rms}
Output offset voltage	V _{OFFL1}	33	L _{OUT1} pin DC difference during SW switching		0	±15	mV
Input impedance	Z _{IL1}			42	60	78	kΩ
Output impedance	Z _{OL1}				120		Ω
L_{OUT2} output							
Voltage gain	G _{L2}	TP7	Sine wave 2.5V _{P-P} , 1kHz	-0.5	0.0	0.5	dB
Frequency characteristics	F _{L2}	TP7	Sine wave 2.5V _{P-P} , 1MHz/1kHz	-3.0	0	1.0	dB
Total higher harmonic distortion	THD _{L2}	TP7	Sine wave 2.5V _{P-P} , 1kHz		0.03	0.1	%
Input dynamic range	D _{L2}	SG6	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		V _{rms}
Output offset voltage	V _{OFFL2}	22	L _{OUT2} pin DC difference during SW switching		0	±15	mV
Output impedance	Z _{OL2}				120		Ω
R_{OUT1} output							
Voltage gain	G _{R11}	TP5	b7=0, Sine wave 2.5V _{P-P} , 1kHz	-6.5	-6.0	-5.5	dB
	G _{R12}	TP5	b7=1, Sine wave 2.5V _{P-P} , 1kHz	-0.5	0.0	0.5	
Frequency characteristics	F _{R1}	TP5	Sine wave 2.5V _{P-P} , 1MHz/1kHz	-3.0	0	1.0	dB
Total higher harmonic distortion	THD _{R1}	TP5	Sine wave 2.5V _{P-P} , 1kHz		0.03	0.1	%
Input dynamic range	D _{R1}	SG7	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		V _{rms}
Output offset voltage	V _{OFFR1}	32	R _{OUT1} pin DC difference during SW switching		0	±15	mV
Input impedance	Z _{IR1}			42	60	78	kΩ
Output impedance	Z _{OR1}				120		Ω

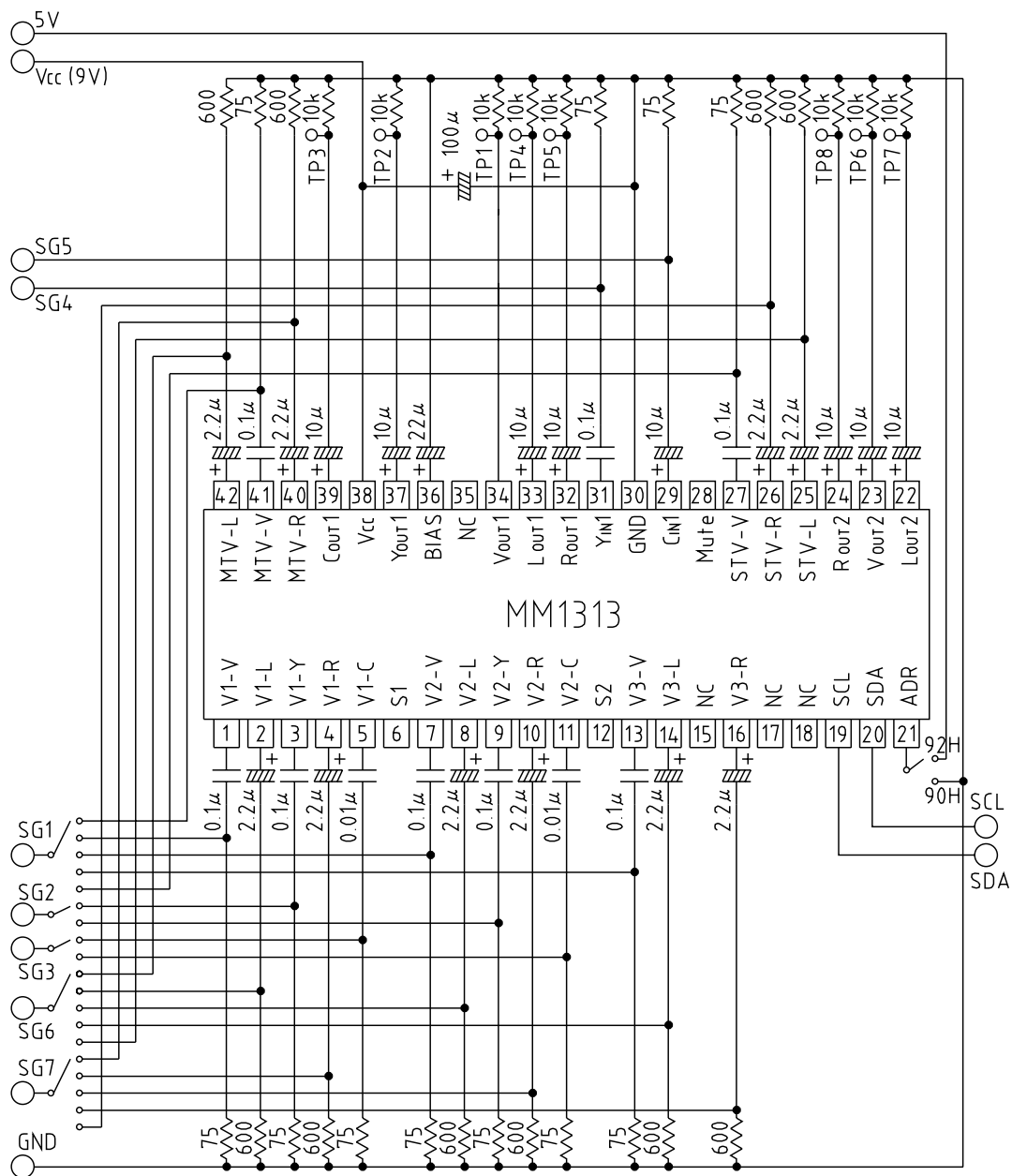
Item	Symbol	Measure ment pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Rout2 output							
Voltage gain	Gr2	TP8	Sine wave 2.5VP-P, 1kHz	-0.5	0.0	0.5	dB
Frequency characteristics	Fr2	TP8	Sine wave 2.5VP-P, 1MHz/1kHz	-3.0	0	1.0	dB
Total higher harmonic distortion	THDR2	TP8	Sine wave 2.5VP-P, 1kHz		0.03	0.1	%
Input dynamic range	Dr2	SG7	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	VOFFR2	24	Rout2 pin DC difference during switching		0	±15	mV
Output impedance	ZOR2				120		Ω
Crosswalk							
VOUT 1	CTV1	TP1	Measurement Circuit Figure 2 for SG1 input : 4.43MHz, 1VP-P for SG2 input : 4.43MHz, 0.5VP-P		-60	-53	dB
VOUT 2	CTV2	TP2			-60	-53	dB
YOUT 1	CTY1	TP3			-60	-53	dB
COUT 1	CTC1	TP6			-60	-53	dB
LOUT 1	CTL1	TP4	Measurement Circuit Figure 2 1kHz, 2.5VP-P		-90	-80	dB
LOUT 2	CTL2	TP5			-90	-80	dB
ROUT 1	CTR1	TP7			-90	-80	dB
ROUT 2	CTR2	TP8			-90	-80	dB
Video I/O Pin Voltage							
Input pin voltage	VVIP		No signal, no load	4.6	4.9	5.2	V
Output pin voltage	VVOP		VOUT1 pin, VOUT2 pin No signal, no load	4.1	4.4	4.7	V
	VSOP		YOUT1 pin, COUT1 pin No signal, no load	3.3	3.6	3.9	V
Audio I/O Pin Voltage							
Input pin voltage	VAIP		No signal, no load	4.0	4.3	4.6	V
Output pin voltage	VAOP		No signal, no load	3.9	4.2	4.5	V
Logic section (Refer to figure below)							
Input voltage L	VIL	I²C logic low level discrimination value		0.0		1.5	V
Input voltage H	VIH	I²Clogic high level discrimination value		3.0		5.0	V
Low level output voltage (SDA)	VOL	SDA for 3mA inflow		0.0		0.4	V
High level input current	IIH	when SDA, SCL=4.5V impressed		-10		+10	µA
Low level input current	IIL	when SDA, SCL=0.4V impressed		-10		+10	µA
Clock frequency	fSCL					100	kHz
Data transmission waiting time	tBUF			4.7			µS
SCL start hold time	tHD;STA			4.0			µS
SCL low level hold time	tLOW			4.7			µS
SCL high level hold time	tHIGH			4.0			µS
SCL start set-up time	tSU;STA			4.7			µS
SDA data hold time	tHD;DAT			200			nS
SDA data set-up time	tSD;DAT			250			nS
SCL rise time	tr					1000	nS
SCL fall time	tf					300	nS
SCL stop set-up time	tSU;STO			4.0			µS

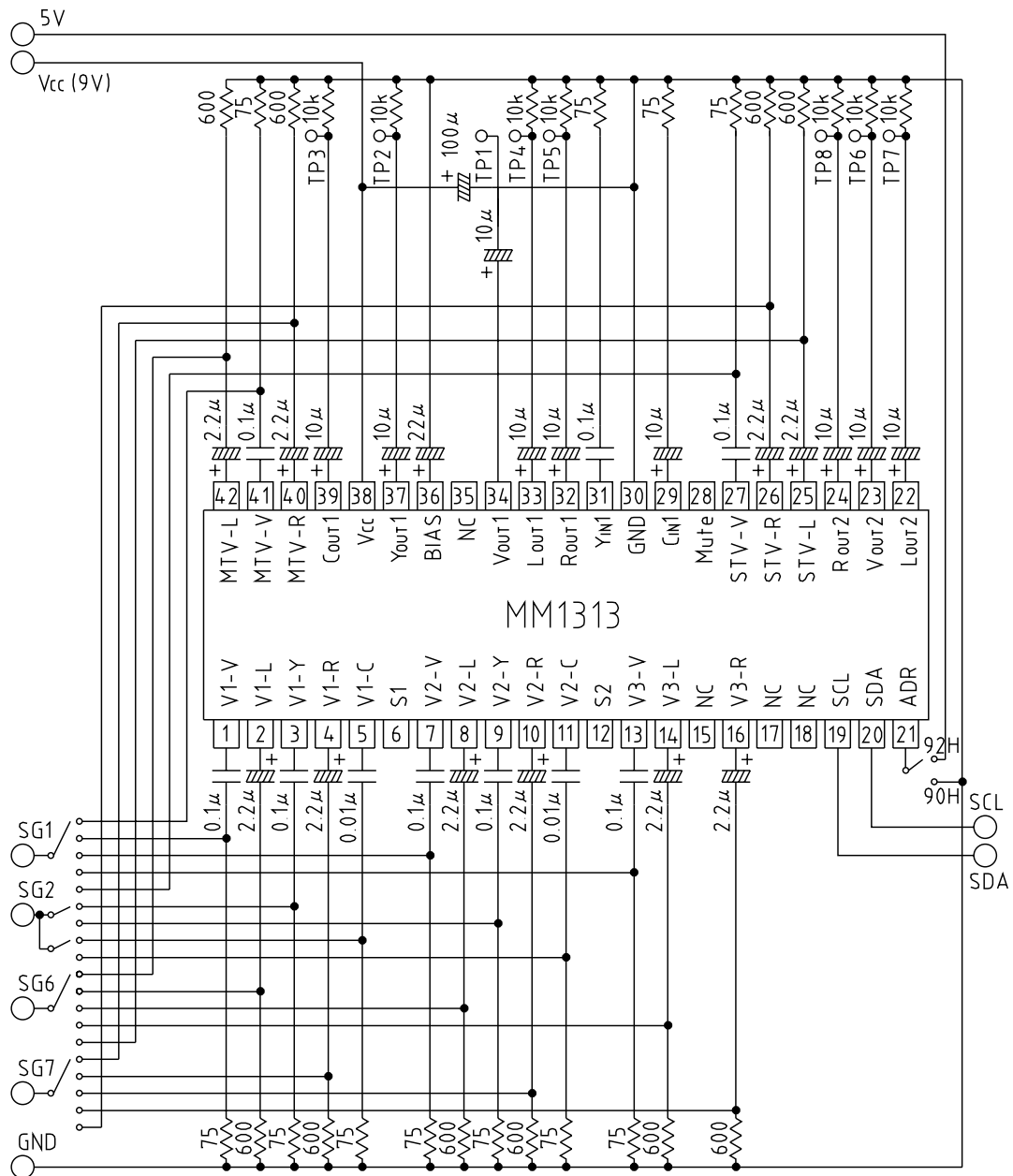
I²C BUS BUS Control Signal



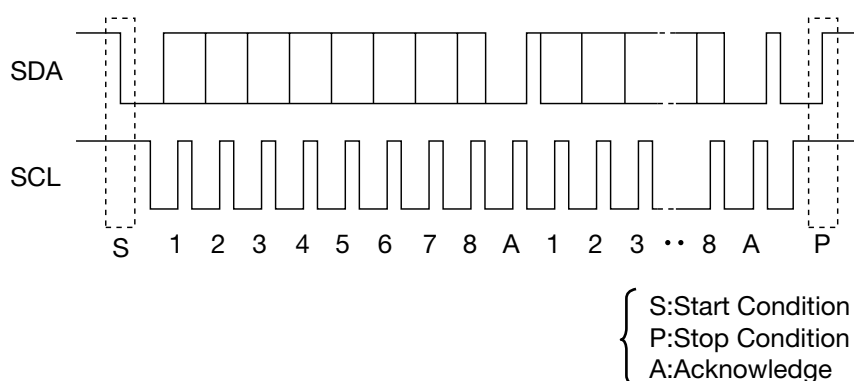
Measurement Circuit

Measurement Circuit 1





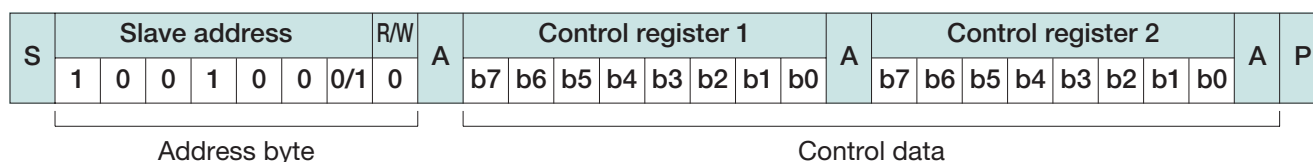
I²C BUS



The I²C BUS is a BUS system developed by Philips for internal use in equipment. Data transmission is carried out by the two SDA and SCL lines, in byte units, with the MSB first from start condition.

[Control Register]

The control register contains data sent from the master in order to determine the status of each switch.



The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 0 when using as a control register.

The MM1313 slave address can be selected as 90H/92H depending on the status of the ADR pin. When ADR pin is low it is 90H.

The relationship between the control register bits and switch control is as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
Audio Gain	S/Comp Select	Video-Select			Audio-Select		

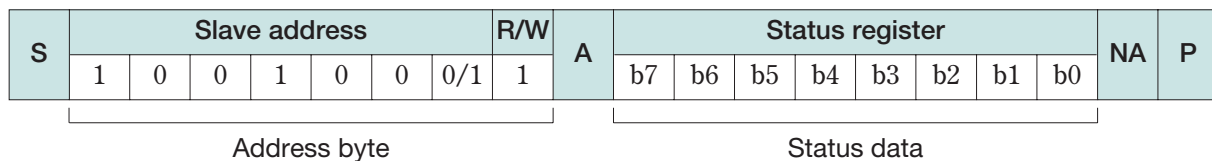
The control register bits are reset to 0 when power is applied.

MM1313 control is carried out by the 3-byte structure of the 1 address byte and 2 control data bytes. The first byte in the control data is control data for output 1, and the remaining 1 byte is control data for output 2.

All of the remaining data (fourth byte and after) are ignored.

Refer to the separate tables for details on switch control.

The status register contains data for sending device status to the master.



The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 1 when using as a status register.

The MM1313 slave address can be selected as 91H/93H depending on the status of the ADR pin. When the ADR pin is low it is 91H. However, the confirmation response after completion of the status register should be non-acknowledge.

The status register output data as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
P-ON RESET	×	S1 OPEN	S1 SEL	S2 OPEN	S2 SEL	×	×

P-ON RESET : Returns 1 for power on reset. However once data read begins, 0 is returned next.

S1/S2 OPEN : Returns 0 when the S1/S2 pin is not open, and returns 1 when the S1/S2 pin is open

S1/S2 SEL : Returns 0 when the S1/S2 pin is not grounded, and returns 1 when the S1/S2 pin is grounded.

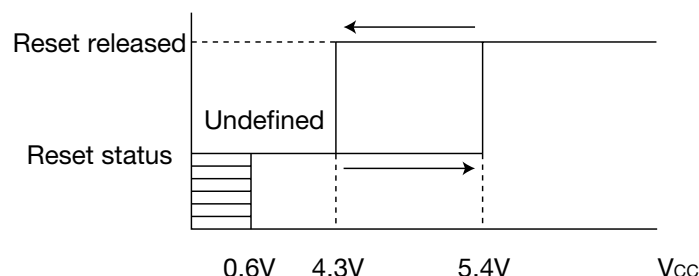
S1/S2 OPEN, SEL have 3-value discrimination, and the combinations are as shown below.

S1/S2 pin DC voltage	S1/S2 OPEN	S1/S2 SEL
0.8V or less	0	1
1.3V or more, 3.5V or less	0	0
4.5V or more	1	0

[Power On Reset]

Power on reset is built in to reset each control register to 0 when power is turned on.

Power on reset threshold has hysteresis as shown in the figure below. The IC power on reset status can be discriminated by reading the status register P-ON RESET.



Switch Control Table

1. Video Output 1

b6	b5	b4	b3	V _{OUT1}	Y _{IN1}	C _{IN1}
0	0	0	0	Mute	Mute	Mute
0	0	0	1	MTV-V	Y _{IN1}	C _{IN1}
0	0	1	0	V1-V	Y _{IN1}	C _{IN1}
0	0	1	1	V2-V	Y _{IN1}	C _{IN1}
0	1	0	0	V3-V	Y _{IN1}	C _{IN1}
0	1	0	1	STV-V	Y _{IN1}	C _{IN1}
0	1	1	0	Mute	Mute	Mute
		1	1			
1	0	0	0	Mute	Mute	Mute
1	0	0	1	MTV-V	Y _{IN1}	C _{IN1}
1	0	1	0	V1-Y+C	V1-Y	V1-C
1	0	1	1	V2-Y+C	V2-Y	V2-C
1	1	0	0	V3-V	Y _{IN1}	C _{IN1}
1	1	0	1	STV-V	Y _{IN1}	C _{IN1}
1	1	1	0	Mute	Mute	Mute
		1	1			

2. Video Output 2

b6	b5	b4	b3	V _{OUT2}
0	0	0	0	Mute
0	0	0	1	MTV-V
0	0	1	0	V1-V
0	0	1	1	V2-V
0	1	0	0	V3-V
0	1	0	1	STV-V
0	1	1	0	Mute
		1	1	
1	0	0	0	Mute
1	0	0	1	MTV-V
1	0	1	0	V1-Y+C
1	0	1	1	V2-Y+C
1	1	0	0	V3-V
1	1	0	1	STV-V
1	1	1	0	Mute
		1	1	

3. Audio Output 1

Mute pin	b2	b1	b0	L _{OUT1}	R _{OUT1}
1.5V or less (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV-L	MTV-R
	0	1	0	V1-L	V1-R
	0	1	1	V2-L	V2-R
	1	0	0	V3-L	V3-R
	1	0	1	STV-L	STV-R
	1	1	0	Mute	Mute
		1	1		
3.0V or more	–	–	–	Mute	Mute

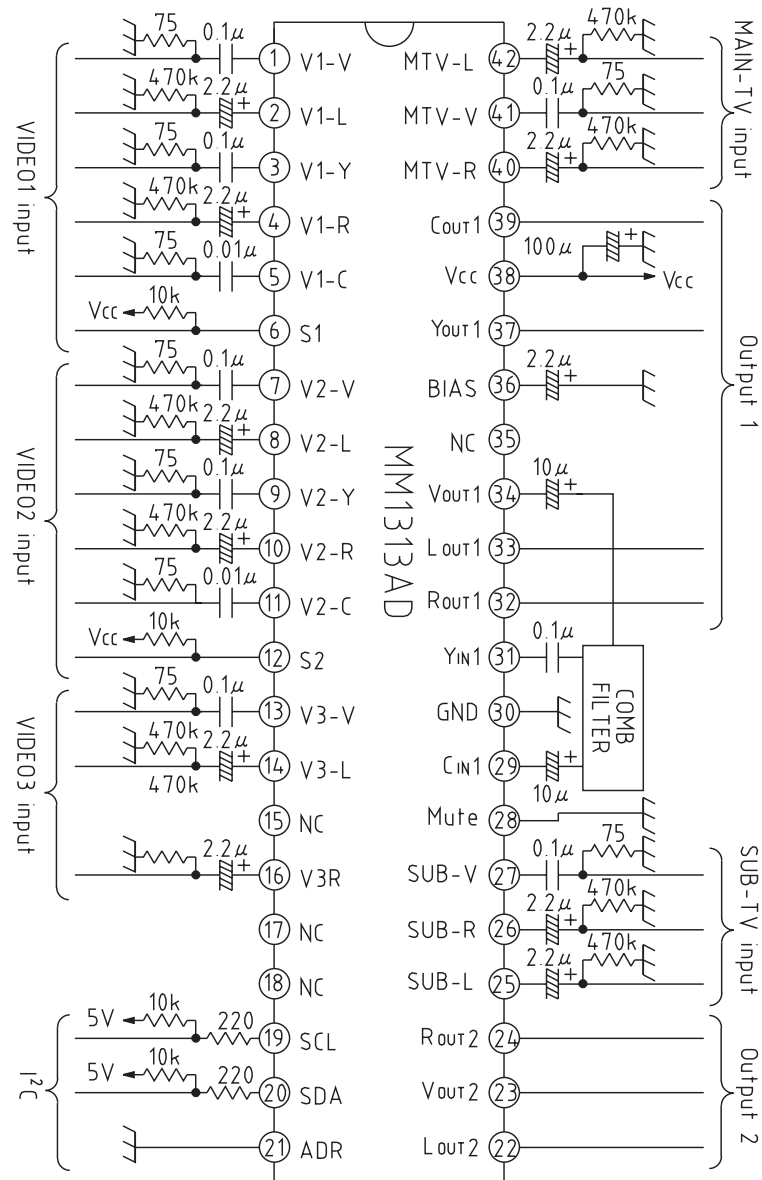
4. Audio Output 1 Gain Switching

b7	Output gain
0	–6dB output
1	0dB output

5. Audio Output 2

Mute pin	b2	b1	b0	L _{OUT2}	R _{OUT2}
1.5V or less (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV-L	MTV-R
	0	1	0	V1-L	V1-R
	0	1	1	V2-L	V2-R
	1	0	0	V3-L	V3-R
	1	0	1	STV-L	STV-R
	1	1	0	Mute	Mute
		1	1		
3.0V or more	–	–	–	Mute	Mute

Application Circuit



Notes

1. V_{OUT} is set at 4.4V and C_{IN} at 4.9V

Please note that capacitance polarity may vary depending on comb filter bias.

2. Each audio output can be muted by making pin 19 high. Mute is off when it is open or low.