

# MM74HCT74

## Dual D-Type Flip-Flop with Preset and Clear

### Features

- Typical propagation delay: 20ns
- Low quiescent current: 40µA maximum (74HCT Series)
- Low input current: 1µA maximum
- Fanout of 10 LS-TTL loads
- Meta-stable hardened

### General Description

The MM74HCT74 utilizes advanced silicon-gate CMOS technology to achieve operation speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and  $\bar{Q}$  outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The 74HCT logic family is functionally and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

### Ordering Information

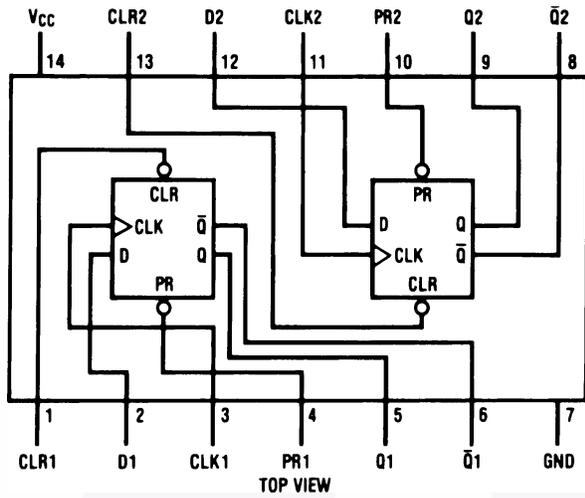
Order Number	Package Number	Package Description
MM74HCT74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HCT74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT74N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

### Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



### Truth Table

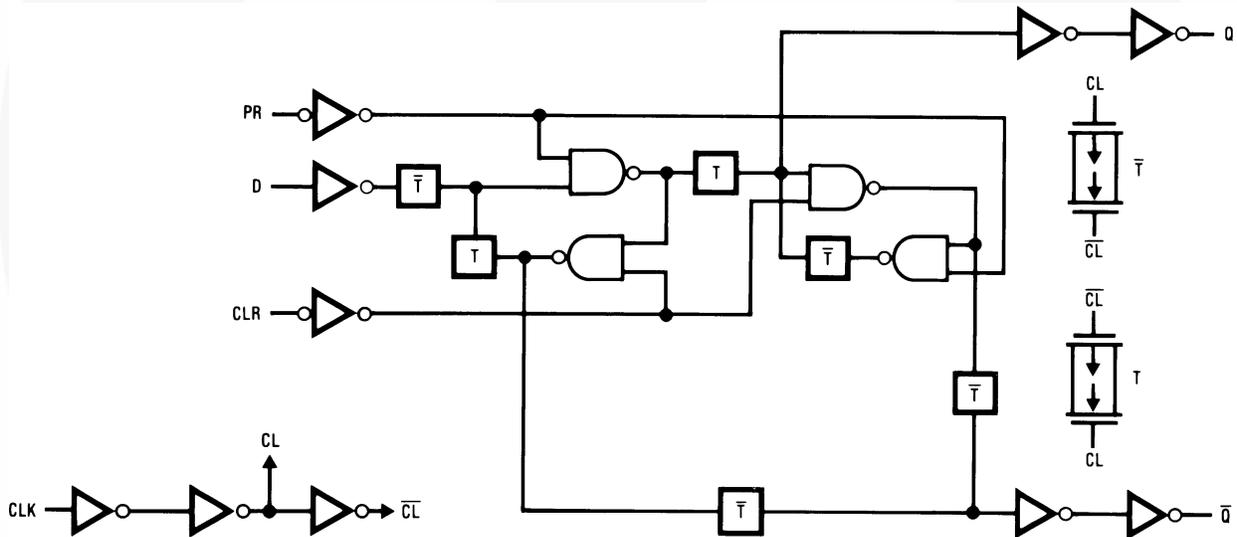
Inputs				Outputs	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>(1)</sup>	H <sup>(1)</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>

Q<sub>0</sub> = the level of Q before the indicated input conditions were established.

**Note:**

1. This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) level.

### Logic Diagram



## Absolute Maximum Ratings<sup>(2)</sup>

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5 to +7.0V
$V_{IN}$	DC Input Voltage	-1.5 to $V_{CC} + 1.5V$
$V_{OUT}$	DC Output Voltage	-0.5 to $V_{CC} + 0.5V$
$I_{IK}, I_{OK}$	Clamp Diode Current	$\pm 20mA$
$I_{OUT}$	DC Output Current, per pin	$\pm 25mA$
$I_{CC}$	DC $V_{CC}$ or GND Current, per pin	$\pm 50mA$
$T_{STG}$	Storage Temperature Range	-65°C to +150°C
$P_D$	Power Dissipation Note 3 S.O. Package only	600mW 500mW
$T_L$	Lead Temperature (Soldering 10 seconds)	260°C

### Notes:

- Unless otherwise specified all voltages are referenced to ground.
- Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
$V_{CC}$	Supply Voltage	4.5	5.5	V
$V_{IN}, V_{OUT}$	DC Input or Output Voltage	0	$V_{CC}$	V
$T_A$	Operating Temperature Range	-40	+85	°C
$t_r, t_f$	Input Rise or Fall Times		500	ns

**DC Electrical Characteristics** $V_{CC} = 5V \pm 10\%$  (unless otherwise specified).

Symbol	Parameter	Conditions	$T_A =$				Units
			25°C		-40°C to 85°C	-55°C to 125°C	
			Typ.	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
$V_{IL}$	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ , $ I_{OUT}  = 20\mu A$	$V_{CC}$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ , $ I_{OUT}  = 4.0mA$ , $V_{CC} = 4.5V$	4.2	3.98	3.84	3.7	
		$V_{IN} = V_{IH}$ or $V_{IL}$ , $ I_{OUT}  = 4.8mA$ , $V_{CC} = 5.5V$	5.2	4.98	4.84	4.7	
$V_{OL}$	Maximum LOW Level Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ , $ I_{OUT}  = 20\mu A$	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ , $ I_{OUT}  = 4.0mA$ , $V_{CC} = 4.5V$	0.2	0.26	0.33	0.4	
		$V_{IN} = V_{IH}$ or $V_{IL}$ , $ I_{OUT}  = 4.8mA$ , $V_{CC} = 5.5V$	0.2	0.26	0.33	0.4	
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, $V_{IH}$ or $V_{IL}$		$\pm 0.5$	$\pm 0.5$	$\pm 1.0$	$\mu A$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$		2.0	20	80	$\mu A$
		$V_{IN} = 2.4V$ or $0.5V^{(4)}$		0.3	0.4	0.5	mA

**Note:**4. This is measured per pin. All other inputs are held at  $V_{CC}$  Ground.**AC Electrical Characteristics** $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15$  pF,  $t_r = t_f = 6$  ns.

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency from Clock to Q or $\bar{Q}$		50	30	MHz
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay Clock to Q or $\bar{Q}$		18	30	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from Preset or Clear to Q or $\bar{Q}$		18	30	ns
$t_{REM}$	Minimum Removal Time, Preset or Clear to Clock			20	ns
$t_S$	Minimum Setup Time Data to Clock			20	ns
$t_H$	Minimum Hold Time Clock to Data		-3	0	ns
$t_W$	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

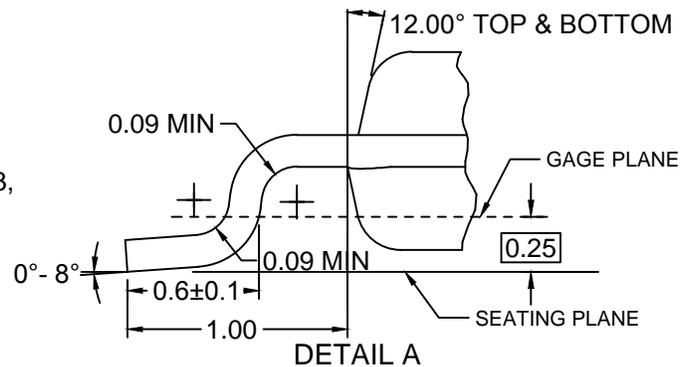
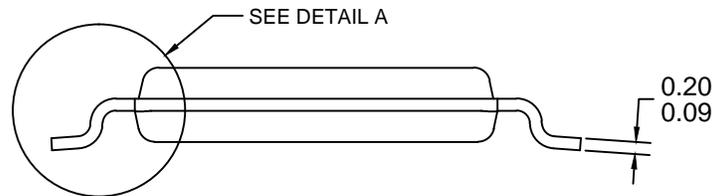
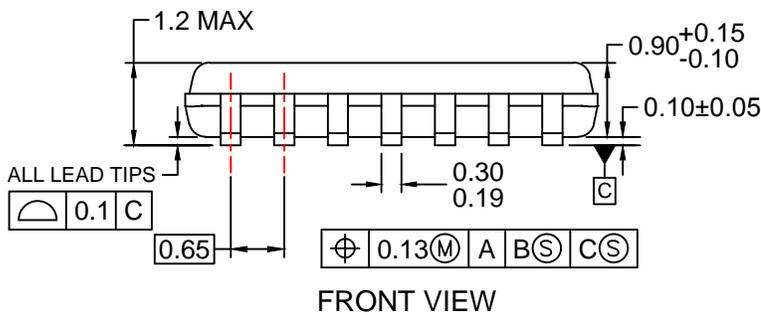
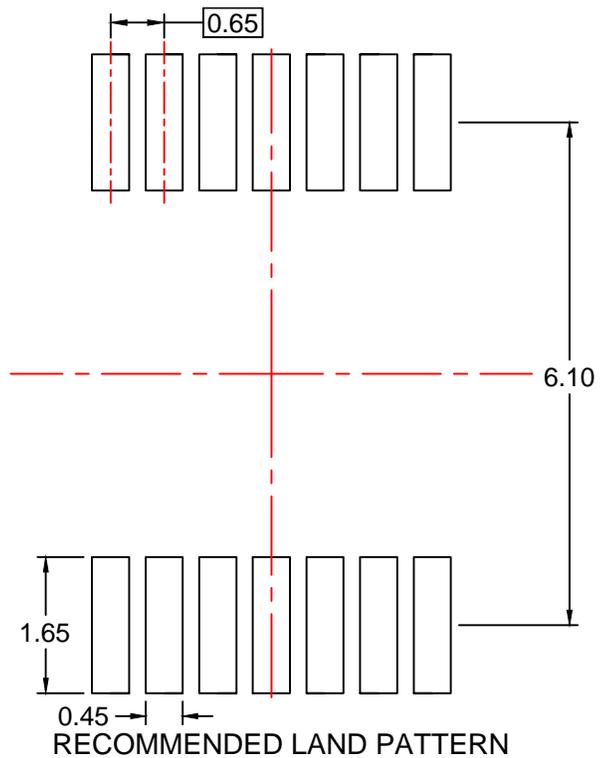
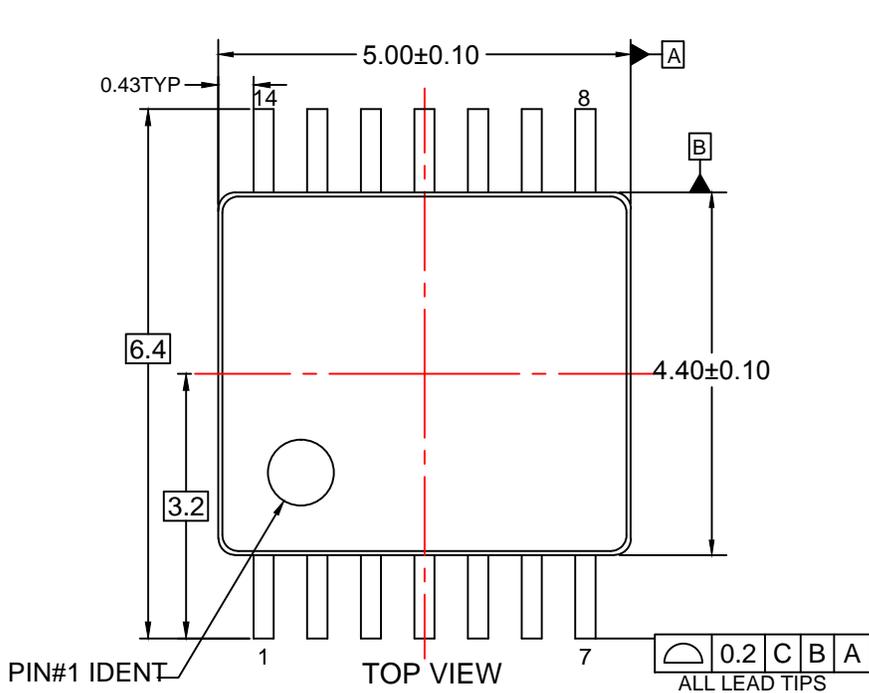
## AC Electrical Characteristics

$V_{CC} = 5.0V \pm 10\%$ ,  $C_L = 50 \text{ pF}$ ,  $t_r = t_f = 6\text{ns}$  unless otherwise specified.

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ \text{ to } +85^\circ\text{C}$		Units
			Typ.	Guaranteed Limits			
$f_{MAX}$	Maximum Operating Frequency			27	21		MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay from Clock to Q or $\bar{Q}$		21	35	44		ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay from Preset or Clear to Q or $\bar{Q}$		21	35	44		ns
$t_{REM}$	Minimum Removal Time Preset or Clear to Clock			20	25		ns
$t_S$	Minimum Setup Time Data to Clock			20	25		ns
$t_H$	Minimum Hold Time Clock to Data		-3	0	0		ns
$t_W$	Minimum Pulse Width Clock, Preset or Clear		9	16	20		ns
$t_r, t_f$	Maximum Clock Input Rise and Fall Time			500	500		ns
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time			15	19		ns
$C_{PD}$	Power Dissipation Capacitance <sup>(5)</sup>	(per flip-flop)	10				pF
$C_{IN}$	Maximum Input Capacitance		5	10	10		pF

### Note:

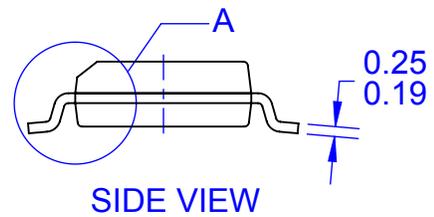
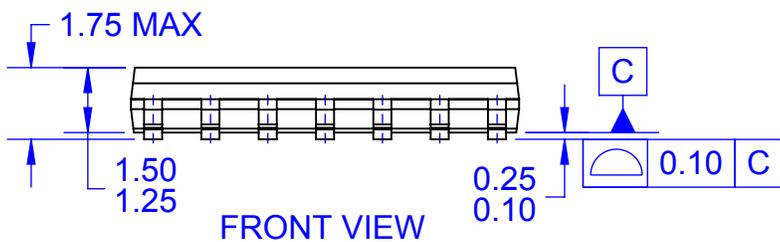
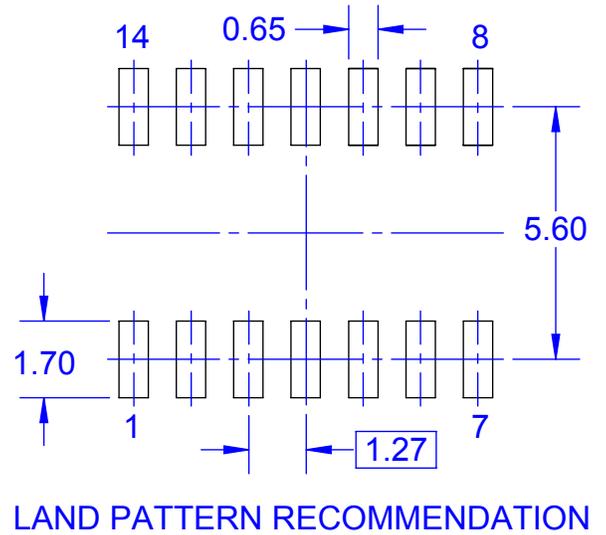
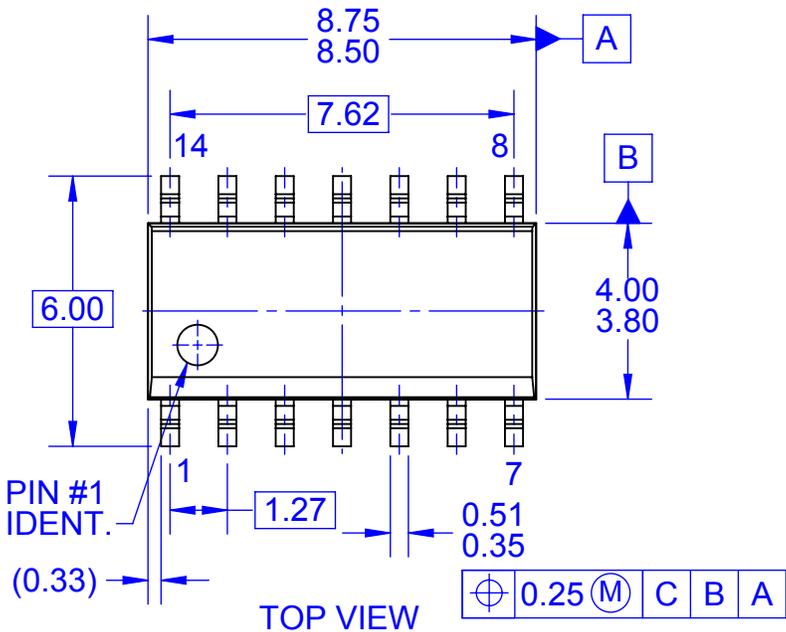
5.  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .



**NOTES:**

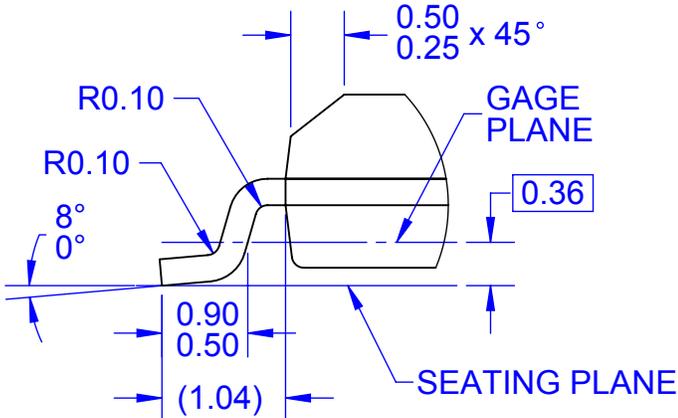
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.
- E. LANDPATTERN STANDARD: SOP65P640X110-14M.
- F. DRAWING FILE NAME: MKT-MTC14rev7.





NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009
- D. DRAWING FILENAME: MKT-M14Arev14



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative