DATA SHEET

SAA4981
Monolithic integrated 16 : 9 compressor

Preliminary specification
Supersedes data of May 1994
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Monolithic integrated 16 : 9 compressor SAA4981

FEATURES

- Fixed horizontal compression by a factor of $^4/_3$ for most video standards
- Three fixed screen positions (left, centre and right)
- 5 MHz bandwidth
- Bypass function
- Inputs for luminance and chrominance of side panels
- Standard video inputs and outputs (Y, (B–Y) and (R–Y))
- Horizontal and vertical sync signals are not processed
- Pre filters and post filters on chip.

GENERAL DESCRIPTION

The integrated 16 : 9 compressor is an IC which compresses the active part of a video line by a factor of $^4/_3$ from, for example, 52 μs to 39 μs. This is necessary to display 4:3 video software on a 16 : 9 tube in the correct proportion. The capacitively coupled video inputs are Y, (B–Y) and (R–Y).

The synchronisation input HREF is a line frequency reference signal. The bandwidth of the IC is up to 5 MHz and the signal delay is realized with SC Line Memories (Switched Capacitors Line Memories). The output of the 16 : 9 compressor also has the format Y, (B–Y) and (R–Y) and provides the following two possibilities:

1. Bypass function (the input signal is not compressed)
2. Compressed video by a factor of $^4/_3$ with three different fixed screen positions (left, centre and right). The luminance and chrominance of the side panels are determined by the external signals YSIDE, BYSIDE and RYSIDE.

The horizontal compression is a time discrete and amplitude continuous signal processing. This provides pre and post filters which are realized on-chip. The internal clock generation is achieved with a 54 MHz horizontal PLL which is synchronized to the positive edge of the HREF signal. The function of the IC is controlled by the three control signals CTRL1, CTRL2 and CTRL3.

QUICK REFERENCE DATA

Voltages for video signals are peak-to-peak values for 75% colour bars. All voltages are referenced to $V_{EEA} = V_{EED} = 0$ V.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.75	5.0	5.5	V
V_{CCD}	digital supply voltage	4.75	5.0	5.5	V
$V_{iY(p-p)}$	Y input voltage (peak-to-peak value)	–	0.32	0.45	V
$V_{iU(p-p)}$	(B–Y) input voltage (peak-to-peak value)	–	1.33	1.9	V
$V_{iV(p-p)}$	(R–Y) input voltage (peak-to-peak value)	–	1.05	1.5	V
V_{iHREF}	input HREF top pulse	3.0	–	6.5	V
$V_{oY(p-p)}$	YOUT output voltage (peak-to-peak value)	–	0.32	0.5	V
$V_{oU(p-p)}$	(B–Y)OUT output voltage (peak-to-peak value)	–	1.33	2.1	V
$V_{oV(p-p)}$	(R–Y)OUT output voltage (peak-to-peak value)	–	1.05	1.7	V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4981	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
SAA4981T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

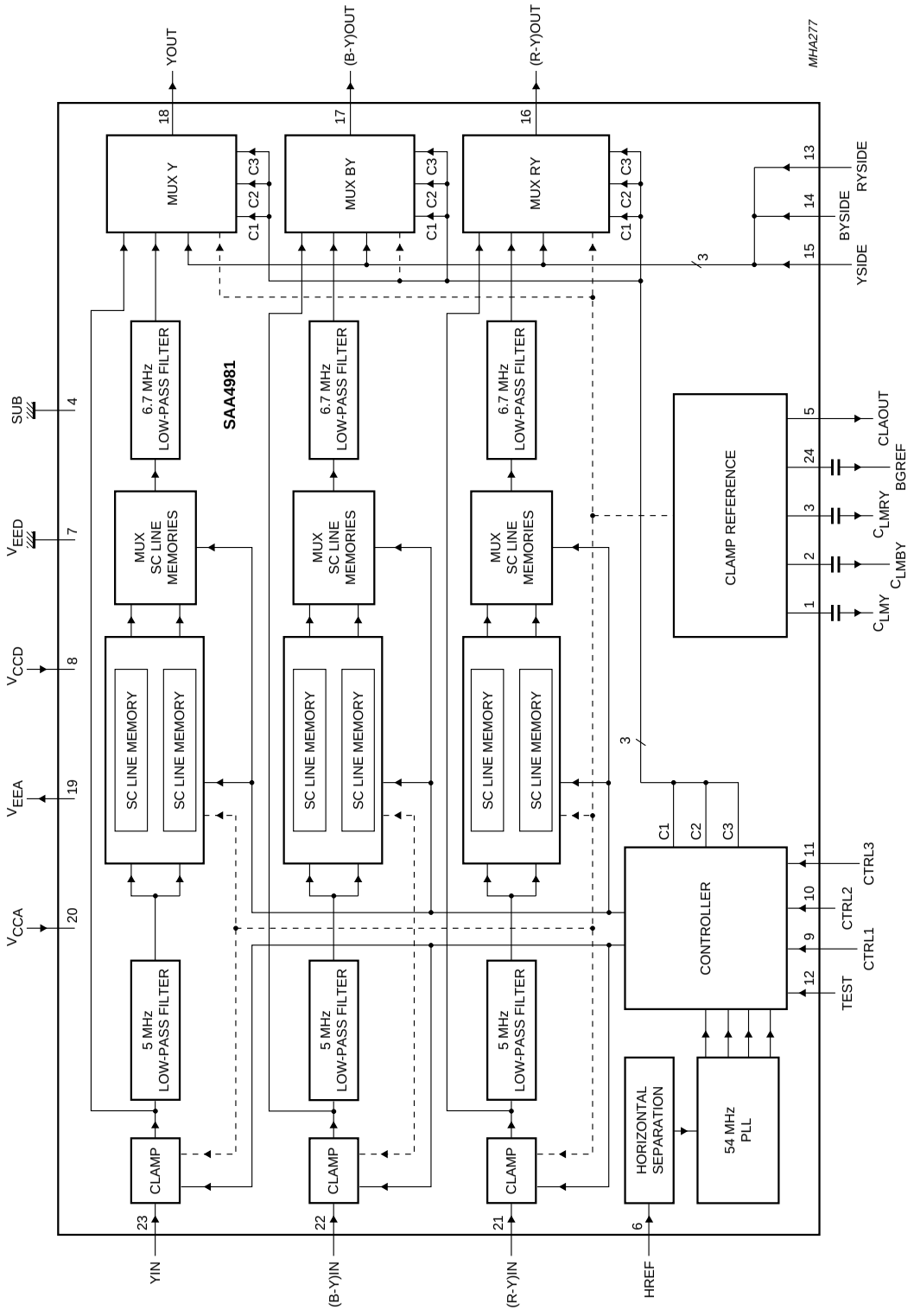


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
C_{LMY}	1	decoupling capacitor for Y reference voltage
C_{LMBY}	2	decoupling capacitor for BY reference voltage
C_{LMRY}	3	decoupling capacitor for RY reference voltage
SUB	4	substrate connection (see Fig.5)
CLAOUT	5	internal clamping reference voltage output
HREF	6	horizontal reference input
V_{EED}	7	ground for digital section
V_{CCD}	8	positive digital supply voltage
CTRL1	9	control input 1
CTRL2	10	control input 2
CTRL3	11	control input 3
TEST	12	test mode activation
RYSIDE	13	side panel input for RY
BYSIDE	14	side panel input for BY
YSIDE	15	side panel input for Y
(R–Y)OUT	16	output signal for (R–Y)
(B–Y)OUT	17	output signal for (B–Y)
YOUT	18	output signal for Y
V_{EEA}	19	ground for analog section
V_{CCA}	20	positive analog supply voltage
(R–Y)IN	21	input signal for (R–Y)
(B–Y)IN	22	input signal for (B–Y)
YIN	23	input signal for Y
BGREF	24	decoupling capacitor for internal reference voltage

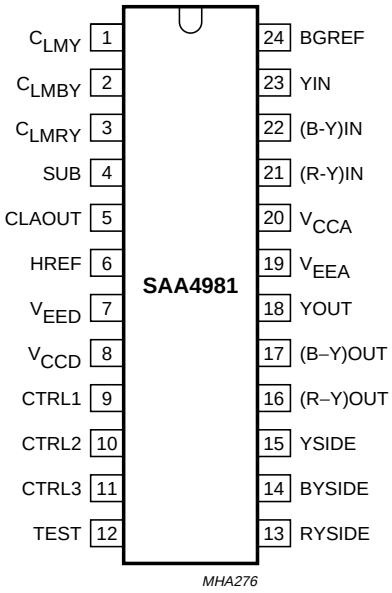


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Applicable video standards

The integrated 16 : 9 compressor can be used for the following video standards; B, C, D, G, H, I, K, K1, L, M and N. standards D, I, K, K1 and L will show a reduced video bandwidth above 5 MHz.

Clamping circuit

The clamping circuits clamp the video input signals Y, (B–Y) and (R–Y) to the DC level of the clamp reference signal fed from the clamp reference circuit. This is necessary to ensure that the input signals are in the correct input voltage range for the 5 MHz low-pass filters and the SC line memories.

Internal pre filters

Before the signals are sampled in the time discrete and amplitude continuous area, low-pass filtering is necessary to avoid any aliasing. Even if the inputs have already been low-pass filtered further filtering is advantageous for the electromagnetic compatibility (EMC). The same transfer function is used for all three low-pass filters because of the same bandwidth for the luminance and chrominance signals (up to 5 MHz).

SC line memories

After the low-pass filters the input signals are fed to the SC line memories. The signals are sampled at a clock frequency of 13.5 MHz. One video line later the signals are read with a clock frequency of 18 MHz in the compression mode. The result of the different clock frequencies is a horizontal compression by a factor of $^4/_3$. The clocks and the horizontal starting pulses for the SC line memories are fed from the controller.

Two line memories are required for each signal path because in the compression mode, in one video line the signals are sampled to the SC line memories with 13.5 MHz and one video line later the signals are read with 18 MHz. In the bypass mode, via the SC line memories, in one video line the signals are sampled with 13.5 MHz and one video line later the signals are read with 13.5 MHz. The SC line memories are suitable for signals with a bandwidth up to 5 MHz. With a multiplexer (MUX) behind the SC line memories, the sampled video signal is connected to the internal post filters.

Output multiplexer MUX Y, MUX (B–Y) and MUX (R–Y)

The output multiplexers are controlled via C1 and C2 fed from the controller. The multiplexers are used to connect one of the four input signals to the output and, also, enable fast switching.

The input signals of the multiplexers for one component [Y, (B–Y) or (R–Y)] are as follows:

- The output signal of the post filter
- The uncompressed signal after the input clamping
- The clamping reference signal
- The signal for the side panel determined by YSIDE, BYSIDE and RYSIDE.

The horizontal separation circuit

The 54 MHz horizontal PLL is locked to the positive edge of the digital HREF signal, which is generated in the horizontal separation circuit. It is also possible to use the positive edge of the burst key of a sandcastle signal.

54 MHz horizontal PLL

The 13.5 MHz clock frequency for the sampling clock and the 18 MHz clock frequency for the reading clock are generated in the 54 MHz horizontal PLL. The 13.5 MHz clock and the 18 MHz clock are line locked.

Clamp reference

Reference voltages are generated In the clamp reference block. These DC signals are used in the clamping circuits as input signals for the output multiplexers and as reference voltages for the SC line memories.

Four external capacitors at the pins C_{LMY}, C_{LMBY}, C_{LMRY} and BGREF respectively are necessary to provide smoothing for the reference voltages. A black level reference signal is available at CLAOUT.

Controller

The controller generates the clocks and the horizontal start signals for the SC line memories and, also, the control signals for the output multiplexers. The timing for the start reading signal for three different screen positions (left, centre and right) and the control signals for the multiplexers (C1 and C2) is fixed. For the uncompressed signals a bypass via the SC line memories and a bypass not via the SC line memories is available. When the signals do not pass the line memories, the frequency response is not affected by the si-function. The compression and bypass mode via the line memories is delayed by one line with respect to the bypass mode not via the line memory.

The 16 : 9 compressor is controlled via the control signals CTRL1, CTRL2 and CTRL3 (see Table 1). The test input must be LOW level.

Table 1 Functions of the control signals

CTRL1	CTRL2	CTRL3	FUNCTION
LOW	LOW	LOW	bypass (through the line memories)
LOW	HIGH	LOW	compression, left position
HIGH	LOW	LOW	compression, centre position
HIGH	HIGH	LOW	compression, right position
LOW	LOW	HIGH	bypass (not through the line memories)

Internal post filters

The output signals of the SC line memories have to be filtered with three 6.7 MHz low-pass filters to eliminate the high frequencies caused by the time discrete signal processing. The cut-off frequency of 6.7 MHz is necessary because, as a result of the $^3/_4$ compression factor, the frequencies are shifted to a higher frequency band with the inverse compression factor (e.g. 5 MHz $\rightarrow$ compression $\rightarrow$ 6.67 MHz). Due to the common bandwidth requirements for all three outputs of the SC line memories the same transfer function for the filters can be used.

Remark: These filters do not provide an si-correction. This means that an input signal with a frequency of 5 MHz will be damped by 2.1 dB at the output if the signal passes an SC line memory.

Signals for the side panels

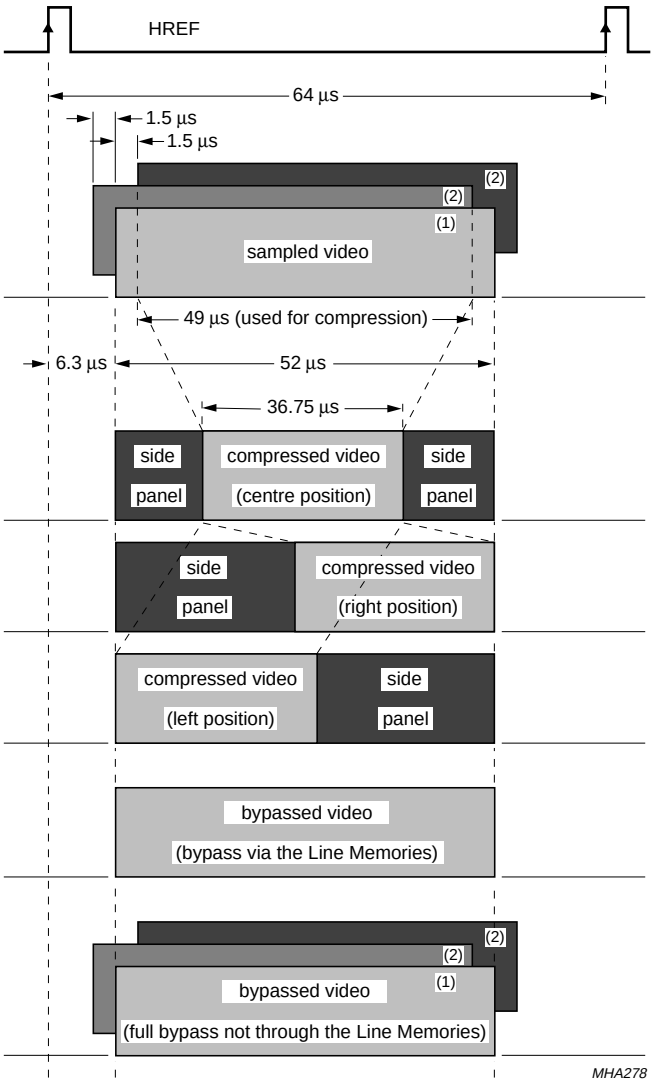
The luminance and chrominance of the side panels is determined by the external signals YSIDE, BYSIDE and RYSIDE. This external generated side panel signal can be referenced to the internal black level reference signal via the output CLAOUT (pin 5).

Horizontal timing (see Fig.3)

The horizontal timing refers to the positive edge of the input HREF signal.

The following timing parameters are valid for a horizontal frequency of 15.625 kHz.

Input clamping typically starts at t_A = 1.55 μs and ends at t_B = 3.78 μs.



(1) Nominal timing for a 52 µs active video signal to generate a centred compressed video signal.

(2) Worst case picture position for a 52 µs active video signal to generate no visible blanking between side panels and compressed video.

Fig.3 Horizontal timing.

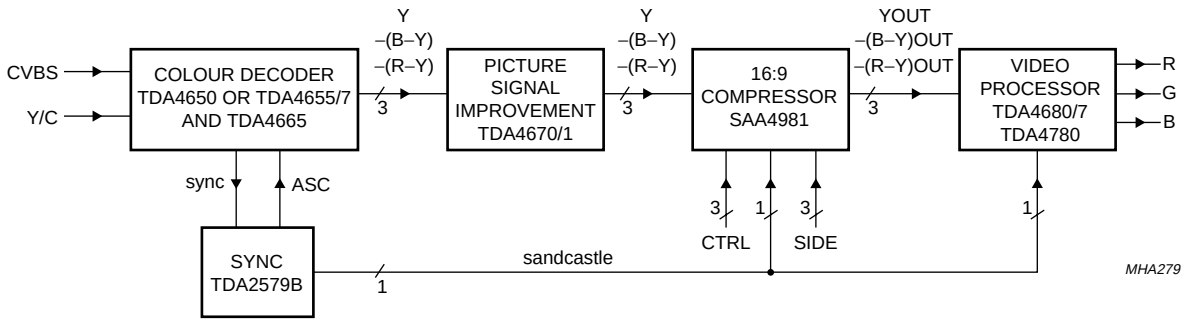


Fig.4 Receiver for 16 : 9, 50 Hz and 15.625 kHz with 16 : 9 compressor.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_n	voltage on any pin (except pin 6 HREF)		V_{EEA} – 0.5	V_{CCA} + 0.5	V
			V_{EED} – 0.5	V_{CCD} + 0.5	V
V_6	input voltage at pin 6		–0.5	+6.5	V
P_{tot}	total power dissipation		–	0.5	W
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C
V_{es}	electrostatic handling for all pins	note 1	–500	+500	V
		note 2	–4000	+4000	V

Notes

1. Equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

QUALITY SPECIFICATION

In accordance with *UZW-B0/FQ-0601*. ESD classification A.

CHARACTERISTICS

$V_{CCA} = V_{CCD} = 5$ V; $T_{amb} = 25$ °C; $f_{HREF} = 15.625$ kHz; substrate connected to V_{EED}; YSIDE, BYSIDE and RYSIDE are connected to CLAOUT; all voltages are referenced to $V_{EEA} = 0$ V; input signal EBU colour bar 100/0/75/0 (CCIR recommended 471-1), Y = 0.32 V (p-p), (B–Y) = 1.33 V (p-p), (R–Y) = 1.05 V (p-p); source impedance $Z_{is} = 300\ \Omega$; coupling capacitor $C_k = 2.2$ nF; output loads connected to ground $R_L = 1\ M\Omega$, $C_L = 20$ pF; measured in Fig.5; test input pin 12 has to be connected to V_{EED}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins 20, 19, 8, 7 and 4); note 1						
V_{CCA}	analog supply voltage		4.75	5.0	5.5	V
I_{CCA}	analog supply current		35	50	65	mA
V_{CCD}	digital supply voltage		4.75	5	5.5	V
I_{CCD}	digital supply current		1	9	14	mA
Video inputs (pins 23, 22 and 21)						
Y						
$V_{iY(p-p)}$	input voltage (peak-to-peak value)	active video	–	0.32	0.45	V
$C_{I(Y)}$	input capacitance		–	–	10	pF
$I_{LI(Y)}$	input leakage current between clamping		–	–	0.1	µA
$R_{iY(cl)}$	input resistance during clamping		–	2	5	kΩ
(B–Y)						
$V_{i(B-Y)(p-p)}$	input voltage (peak-to-peak value)	active video	–	1.33	1.9	V
$C_{I(B-Y)}$	input capacitance		–	–	10	pF
$I_{LI(B-Y)}$	input leakage current between clamping		–	–	0.1	µA
$R_{I(B-Y)(cl)}$	input resistance during clamping		–	2	5	kΩ
(R–Y)						
$V_{i(R-Y)(p-p)}$	input voltage (peak-to-peak value)	active video	–	1.05	1.5	V
$C_{I(R-Y)}$	input capacitance		–	–	10	pF
$I_{LI(R-Y)(cl)}$	input leakage current between clamping		–	–	0.1	µA
$R_{I(R-Y)(cl)}$	input resistance during clamping		–	2	5	kΩ
HREF input (pin 6)						
$V_{i(top)}$	input voltage of the top pulse		3.0	–	6.5	V
$I_{LI(HREF)}$	input leakage current		–	–	10	µA
$C_{I(HREF)}$	input capacitance		–	–	10	pF
V_{slice}	slicing level below top pulse		0.5	0.75	1.0	V
f_i	input frequency		14.0	15.6	17.2	kHz
t_W	pulse width		1	–	–	µs
S_{HREF}	steepness	0.5 V under top	400	–	–	mV/ns
Side panel inputs (pins 15, 14 and 13)						
$V_{i(side)}$	input voltage		0.5	–	2.5	V
$C_{I(side)}$	input capacitance		–	–	10	pF
$I_{LI(side)}$	input leakage current		–	–	0.1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Control inputs/outputs (pins 9, 10 and 11)						
V_{IH}	HIGH level input voltage		3.5	–	–	V
V_{IL}	LOW level input voltage		–	–	1.5	V
C_{Ictr}	input capacitance		–	–	10	pF
I_{LIctr}	input leakage current		–	–	1	μA
Clamping reference output (pin 5)						
V_{o5}	output voltage		1.3	1.45	1.6	V
R_L	load resistor		10	–	–	kΩ
C_L	load capacitor		–	–	30	pF
External capacitors (pins 1, 2 and 3)						
C_{DL}	value for capacitor		–	100	–	nF
V_{oCDL}	output voltage		1.3	1.45	1.6	V
External capacitor (pin 24)						
C_{BGREF}	value for capacitor		–	100	–	nF
V_{oBGREF}	output voltage		1.1	1.25	1.4	V
Video output signals (pins 18, 17 and 16)						
YOUT						
$R_{O(Y)}$	output resistance		–	–	100	Ω
$V_{oY(p-p)}$	output voltage (peak-to-peak value)		–	0.32	0.5	V
S/N	signal-to-noise ratio	0.32 V (p-p)/V_{eff} noise; unweighted; f_i = 200 kHz to 5 MHz	52	–	–	dB
FPN(p-p)	fixed pattern noise peak-to-peak referenced to 0.32 V (p-p) video	f_{clk} < 5 MHz	42	–	–	dB
α_{ctY}	crosstalk between different inputs	f_i = 1 MHz	40	–	–	dB
$\|t_d\|$	delay between different outputs		–	–	30	ns
t_d	jitter in output signal referenced to HREF input signal		–	–	10	ns
Bypass not via the SC line memories						
G_{Y1}	frequency response	f_{ripple} = 0 to 4 MHz	–0.5	–	+0.5	dB
G_{Y2}	frequency response	attenuation at 5 MHz compared to 1 MHz	0	–	–2	dB
Bypass via the SC line memories; note 2						
G_{Y3}	YOUT/YIN at input frequency	f_i = 1 MHz	–1.1	–	+0.9	dB
G_{Y4}	YOUT/YIN at input frequency	f_i = 2 MHz	–1.3	–	+0.7	dB
G_{Y5}	YOUT/YIN at input frequency	f_i = 3 MHz	–1.7	–	+0.3	dB
G_{Y6}	YOUT/YIN at input frequency	f_i = 4 MHz	–2.3	–	–0.3	dB
G_{Y7}	YOUT/YIN at input frequency	f_i = 5 MHz	–3.1	–	–1.1	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Compressed video; note 2						
G_{Y8}	YOUT/YIN at input frequency	f_i = 1 MHz; f_o = 1.3 MHz	–1	–	+1	dB
G_{Y9}	YOUT/YIN at input frequency	f_i = 2 MHz; f_o = 2.7 MHz	–1	–	+1	dB
G_{Y10}	YOUT/YIN at input frequency	f_i = 3 MHz; f_o = 4 MHz	–2	–	0	dB
G_{Y11}	YOUT/YIN at input frequency	f_i = 3.75 MHz; f_o = 5 MHz	–3	–	–1	dB
G_{Y12}	YOUT/YIN at input frequency	f_i = 4 MHz; f_o = 5.3 MHz	–4	–	–1	dB
G_{Y13}	YOUT/YIN at input frequency	f_i = 5 MHz; f_o = 6.67 MHz	–6	–	–1	dB
A_{Ypre}	pre filter stop-band characteristic, damping factor for input signals	f_i > 10 MHz	20	–	–	dB
		f_i > 20 MHz	32	–	–	dB
		f_i > 100 MHz	42	–	–	dB
A_{Ypost}	post filter stop-band characteristic, damping factor for input signals	f_i > 14 MHz	20	–	–	dB
		f_i > 20 MHz	32	–	–	dB
		f_i > 100 MHz	40	–	–	dB
(B–Y)OUT						
$R_{O(U)}$	output resistance		–	–	100	Ω
$V_{oU(p-p)}$	output voltage (peak-to-peak value)		–	1.33	2.1	V
S/N	signal-to-noise ratio	1.33 V (p-p)/V_{eff} noise; unweighted; f_i = 200 kHz to 5 MHz	54	–	–	dB
FPN(p-p)	fixed pattern noise peak-to-peak referenced to 1.33 V (p-p) video	f_{clk} < 5 MHz	42	–	–	dB
α_{ctU}	crosstalk between different inputs	f_i = 1 MHz	40	–	–	dB
$\|t_d\|$	delay between different outputs		–	–	30	ns
t_d	jitter in output signal to input HREF signal		–	–	10	ns
Bypass not via the SC line memories						
G_{U1}	frequency response	f_{ripple} = 0 to 4 MHz	–0.5	–	+0.5	dB
G_{U2}	frequency response	attenuation at 5 MHz compared to 1 MHz	0	–	–2	dB
Bypass via the SC line memories; note 2						
G_{U3}	(B–Y)OUT/(B–Y)IN at input frequency	f_i = 1 MHz	–1.1	–	+0.9	dB
G_{U4}	(B–Y)OUT/(B–Y)IN at input frequency	f_i = 2 MHz	–1.3	–	+0.7	dB
G_{U5}	(B–Y)OUT/(B–Y)IN at input frequency	f_i = 3 MHz	–1.7	–	+0.3	dB
G_{U6}	(B–Y)OUT/(B–Y)IN at input frequency	f_i = 4 MHz	–2.3	–	–0.3	dB
G_{U7}	(B–Y)OUT/(B–Y)IN at input frequency	f_i = 5 MHz	–3.1	–	–1.1	dB

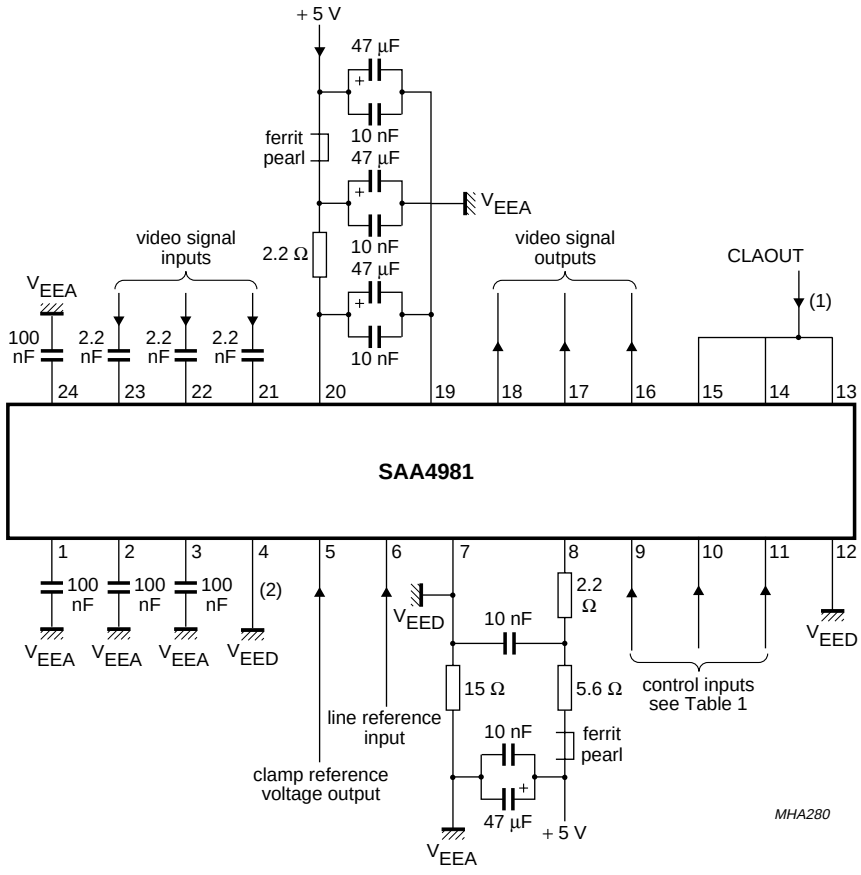
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Compressed video; note 2						
G_{U8}	(B–Y)OUT/(B–Y)IN at input frequency	f_i = 1 MHz; f_o = 1.3 MHz	–1	–	+1	dB
G_{U9}	(B–Y)OUT/(B–Y)IN at input frequency	f_i = 2 MHz; f_o = 2.7 MHz	–1	–	+1	dB
G_{U10}	(B–Y)OUT/(B–Y)IN at input frequency	f_i = 3 MHz; f_o = 4 MHz	–2	–	0	dB
G_{U11}	(B–Y)OUT/(B–Y)IN at input frequency	f_i = 3.75 MHz; f_o = 5 MHz	–3	–	–1	dB
G_{U12}	(B–Y)OUT/(B–Y)IN at input frequency	f_i = 4 MHz; f_o = 5.3 MHz	–4	–	–1	dB
G_{U13}	(B–Y)OUT/(B–Y)IN at input frequency	f_i = 5 MHz; f_o = 6.67 MHz	–6	–	–1	dB
A_{Upre}	pre filter stop-band characteristic, damping factor for input signals	f_i > 10 MHz	20	–	–	dB
		f_i > 20 MHz	32	–	–	dB
		f_i > 100 MHz	42	–	–	dB
A_{Upost}	post filter stop-band characteristic, damping factor for input signals	f_i > 14 MHz	20	–	–	dB
		f_i > 20 MHz	32	–	–	dB
		f_i > 100 MHz	40	–	–	dB
(R–Y)OUT						
$R_{O(V)}$	output resistance		–	–	100	Ω
V_{oV}	output voltage (peak-to-peak value)		–	1.05	1.7	V
S/N	signal-to-noise ratio	1.05 V (p-p)/V_{eff} noise; unweighted; f_i = 200 kHz to 5 MHz	52	–	–	dB
FPN(p-p)	fixed pattern noise peak-to-peak referenced to 1.05 V (p-p) video	f_{clock} < 5 MHz	40	–	–	dB
α_{ctV}	crosstalk between different inputs	f_i = 1 MHz	40	–	–	dB
$\|t_d\|$	delay between different outputs		–	–	30	ns
t_d	jitter in output signal to input HREF signal		–	–	10	ns
Bypass not via the SC line memories						
G_{V1}	frequency response	f_{ripple} = 0 to 4 MHz	–0.5	–	+0.5	dB
G_{V2}	frequency response	attenuation at 5 MHz compared to 1 MHz	0	–	–2	dB
Bypass via the SC line memories; note 2						
G_{V3}	(R–Y)OUT/(R–Y)IN at input frequency	f_i = 1 MHz	–1.1	–	+0.9	dB
G_{V4}	(R–Y)OUT/(R–Y)IN at input frequency	f_i = 2 MHz	–1.3	–	+0.7	dB
G_{V5}	(R–Y)OUT/(R–Y)IN at input frequency	f_i = 3 MHz	–1.7	–	+0.3	dB
G_{V6}	(R–Y)OUT/(R–Y)IN at input frequency	f_i = 4 MHz	–2.3	–	–0.3	dB
G_{V7}	(R–Y)OUT/(R–Y)IN at input frequency	f_i = 5 MHz	–3.1	–	–1.1	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Compressed video; note 2						
G_{V8}	(R–Y)OUT/(R–Y)IN at input frequency	f_i = 1 MHz; f_o = 1.3 MHz	–1	–	+1	dB
G_{V9}	(R–Y)OUT/(R–Y)IN at input frequency	f_i = 2 MHz; f_o = 2.7 MHz	–1	–	+1	dB
G_{V10}	(R–Y)OUT/(R–Y)IN at input frequency	f_i = 3 MHz; f_o = 4 MHz	–2	–	0	dB
G_{V11}	(R–Y)OUT/(R–Y)IN at input frequency	f_i = 3.75 MHz; f_o = 5 MHz	–3	–	–1	dB
G_{V12}	(R–Y)OUT/(R–Y)IN at input frequency	f_i = 4 MHz; f_o = 5.3 MHz	–4	–	–1	dB
G_{V13}	(R–Y)OUT/(R–Y)IN at input frequency	f_i = 5 MHz; f_o = 6.67 MHz	–6	–	–1	dB
A_{Vpre}	pre filter stop-band characteristic, damping factor for input signals	f_i > 10 MHz	20	–	–	dB
		f_i > 20 MHz	32	–	–	dB
		f_i > 100 MHz	42	–	–	dB
A_{Vpost}	post filter stop-band characteristic, damping factor for input signals	f_i > 14 MHz	20	–	–	dB
		f_i > 20 MHz	32	–	–	dB
		f_i > 100 MHz	40	–	–	dB
Video outputs YOUT, (B–Y)OUT and (R–Y)OUT						
RATIO OF OUTPUT AMPLITUDES FOR EQUAL INPUT SIGNALS FOR Y, (B–Y) AND (R–Y)						
V_{oY}/V_{oU}	YOUT/(B–Y)OUT	V_I = 0.32 V (p-p); $f_i \leq$ 1 MHz	–0.4	–	+0.4	dB
V_{oY}/V_{oV}	YOUT/(R–Y)OUT	V_I = 0.32 V (p-p); $f_i \leq$ 1 MHz	–0.4	–	+0.4	dB
V_{oU}/V_{oV}	(B–Y)OUT/(R–Y)OUT	V_I = 1.33 V (p-p)	–0.4	–	+0.4	dB

Notes

1. $\Delta V_1 = |V_{CCA} - V_{CCD}| \leq 300$ mV; $\Delta V_2 = |V_{EED} - V_{EEA}| \leq 300$ mV with V_{EED} = SUB (latch-up prevention).
2. This frequency response includes the si-attenuation as a result of the time discrete signal processing. An si-correction is not performed.

APPLICATION INFORMATION



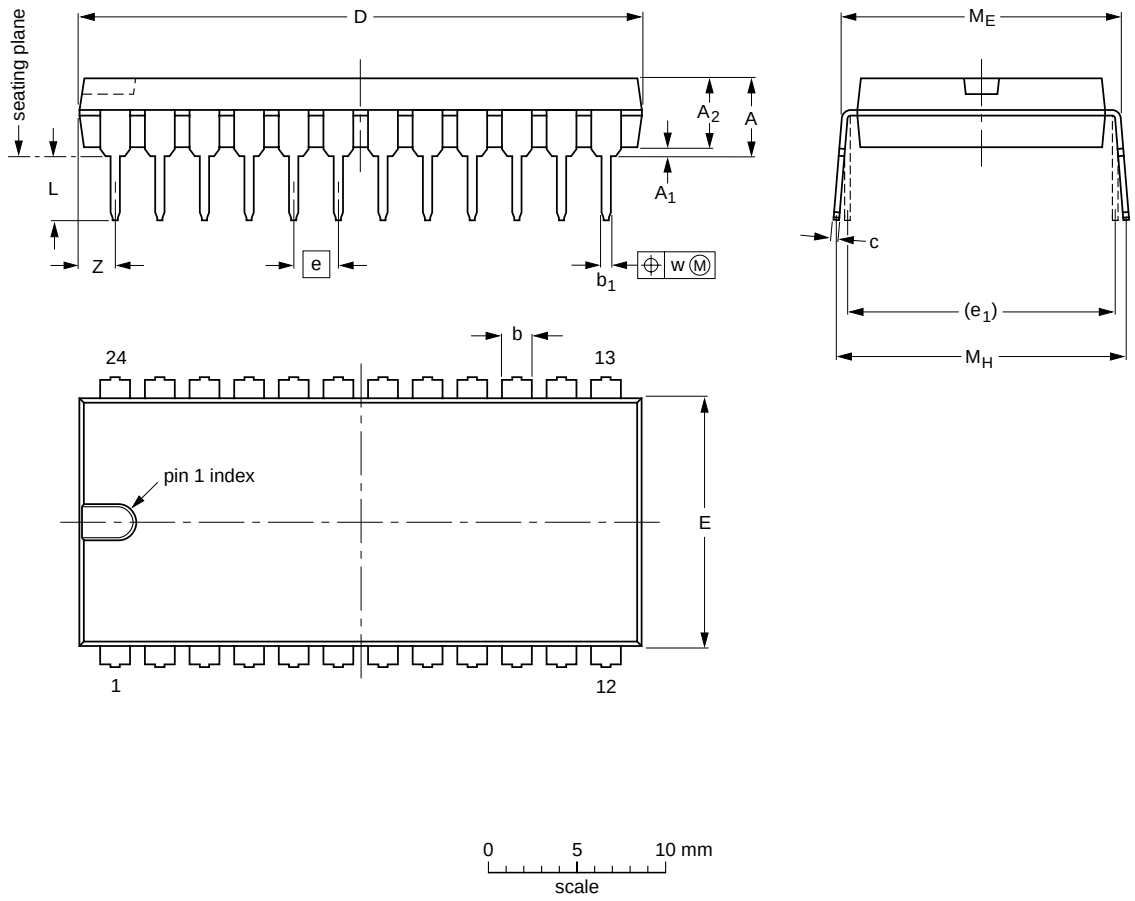
(1) Connected to CLAOUT for black side panels.

(2) Substrate (pin 4) has to be connected to V_{EED}. V_{EEA} and V_{EED}. Substrates have to be separated as much as possible.

Fig.5 Application diagram.

PACKAGE OUTLINES

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

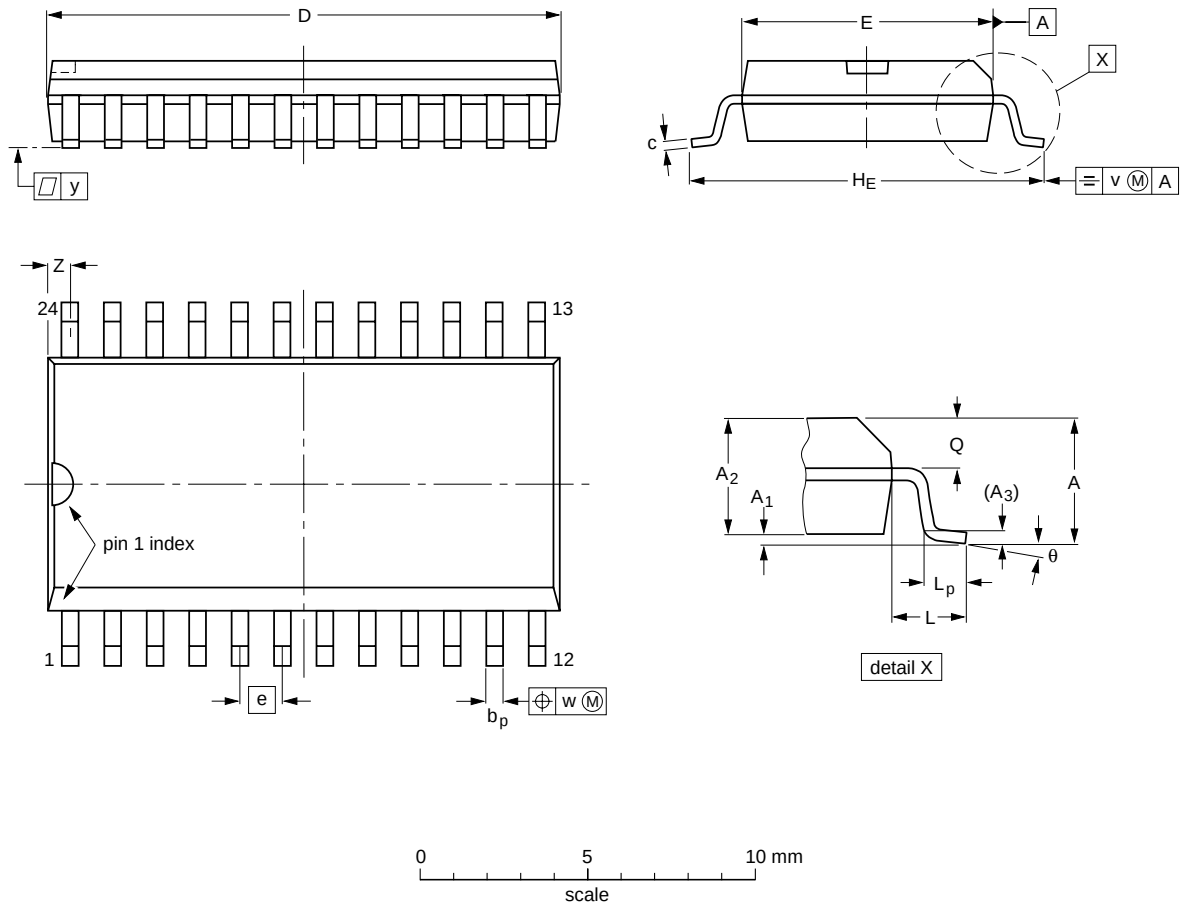
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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