

# DATA SHEET

## **SAA4998H**

Field and line rate converter with  
noise reduction and embedded  
memory

Product specification

2004 Feb 18

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**Field and line rate converter with noise reduction and embedded memory**

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**SAA4998H**

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## Field and line rate converter with noise reduction and embedded memory

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### 1 FEATURES

- Motion compensated frame rate upconversion of all  $1f_H$  film and video standards up to 292 active input lines per field:
  - 50 Hz interlaced to 60 Hz progressive {(60p mode for LCD and Plasma Display (PDP) TV)}
  - 50 Hz interlaced to 75 Hz interlaced {75i mode for jumbo screens, Projection TV (PTV)}
  - 50 Hz interlaced to 100 Hz interlaced (high-end 100 Hz TV)
  - 50 Hz interlaced to 50 Hz progressive (progressive scan TV and LCD and PDP TV)
  - 60 Hz interlaced to 60 Hz progressive (progressive scan TV and LCD and PDP TV)
  - 60 Hz interlaced to 90 Hz interlaced (jumbo screens, PTV)
  - 60 Hz interlaced to 120 Hz interlaced (multistandard high-end 100 Hz TV)
- 480 active lines (NTSC like) or 506 active lines in 50 Hz interlaced to 60 Hz progressive mode
- Motion compensated and Edge Dependent De-Interlacing (EDDI)<sup>(1)</sup>
- Motion estimated film mode detection
- Motion compensated movie judder cancellation:
  - 25 Hz 2 : 2 pull-down (PAL) to 60 Hz progressive or 75 Hz interlaced or 100 Hz interlaced or 50 Hz progressive
  - 30 Hz 2 : 2 pull-down (NTSC) to 60 Hz progressive or 90 Hz interlaced or 120 Hz interlaced
  - 24 Hz 3 : 2 pull-down (NTSC) to 60 Hz progressive or 90 Hz interlaced or 120 Hz interlaced
- Variable vertical sharpness enhancement
- High quality vertical zoom
- Motion compensated temporal noise reduction with after-imaging cancellation
- Split screen demonstration mode
- 2 Mbaud serial interface (SNERT)
- Embedded  $2 \times 2.9$ -Mbit DRAM
- Full 8-bit accuracy
- Memory buffer for Picture-In-Picture (PIP)
- Lead-free package.

### 2 GENERAL DESCRIPTION

The SAA4998H is a high performance video processor featuring Natural Motion™<sup>(2)</sup>, for all global TV standards (PAL, NTSC and SECAM). It is used together with the picture improvement processor SAA4978H and SAA4979H.

The SAA4998H is an advanced version of the SAA4993H. By embedding the field memories it reduces the part count of the realized concept from 4 to 6 parts to only 2 parts and reduces the package size from a QFP160 to a QFP100.

The full FALCONIC mode uses full motion estimation and motion compensation on  $1/4$  pixel accuracy to perform

- Frame rate upconversion
- Film mode detection
- Movie judder cancellation
- Dynamic Noise Reduction (DNR)
- Edge Dependent De-Interlacing (EDDI).

The motion compensated de-interlacer is improved with a new patented Edge Dependent De-Interlacing (EDDI) method. This avoids jagged edges of diagonal lines. The better de-interlacer leads to a significant better performance of progressive as well as interlaced output formats.

A 60 Hz progressive output frame rate can be generated for 50 Hz PAL sources to enable the use of 60 Hz LCD or PDP panels in PAL regions.

50 Hz interlaced to 75 Hz interlaced and 60 Hz interlaced to 90 Hz interlaced can be generated to achieve an increased number of lines and hence a reduction of line visibility for jumbo screens and PTV applications.

The embedded memory can be used to synchronize the main channel and the 2nd channel for PIP and double window applications. This avoids to add additional buffer memory devices to the application.

For demonstration purposes a split screen mode to show the Dynamic Noise Reduction (DNR) function, natural motion, and EDDI is available. The estimated motion vectors can be made visible by colour overlay mode.

The SAA4998H supports a Boundary Scan Test (BST) circuit in accordance with "IEEE Std. 1149.1".

(1) EDDI is protected with two patents of Koninklijke Philips Electronics N.V.

(2) Natural Motion is a trademark of Koninklijke Philips Electronics N.V.

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## 2.1 Patent notice

Notice is herewith given that the subject integrated circuit uses one or more of the following US patents and that each of these patents may have corresponding patents in other jurisdictions.

US 4740842, US 5929919, US 6034734, US 5534946, US 5532750, US 5495300, US 5903680, US 5365280, US 5148269, US 5072293, US 5771074, and US 5302909.

## 2.2 Latch-up test

Latch-up test in accordance with "Latch-up Resistance and Maximum Ratings Test; SNW-FQ-303"; the SAA4998H fulfils the requirements.

## 3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DDD</sub>	core supply voltage (internal rail)	1.65	1.8	1.95	V
V <sub>DDA</sub>	analog supply voltage				
V <sub>DDM</sub>	field memory supply voltage				
V <sub>DDS</sub>	SRAM supply voltage				
V <sub>DDE</sub>	external supply voltage (output pads)	3.0	3.3	3.6	V
V <sub>DDP</sub>	high supply voltage of internal field memories				
I <sub>DD</sub>	sum of supply current				
	at 1.8 V supply voltage pins	–	180	–	mA
	at 3.3 V supply voltage pins	–	6	–	mA
f <sub>CLK</sub>	operating clock frequency	–	32	33.3	MHz
T <sub>amb</sub>	ambient temperature	0	–	70	°C

## 4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4998H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

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### 5 BLOCK DIAGRAMS

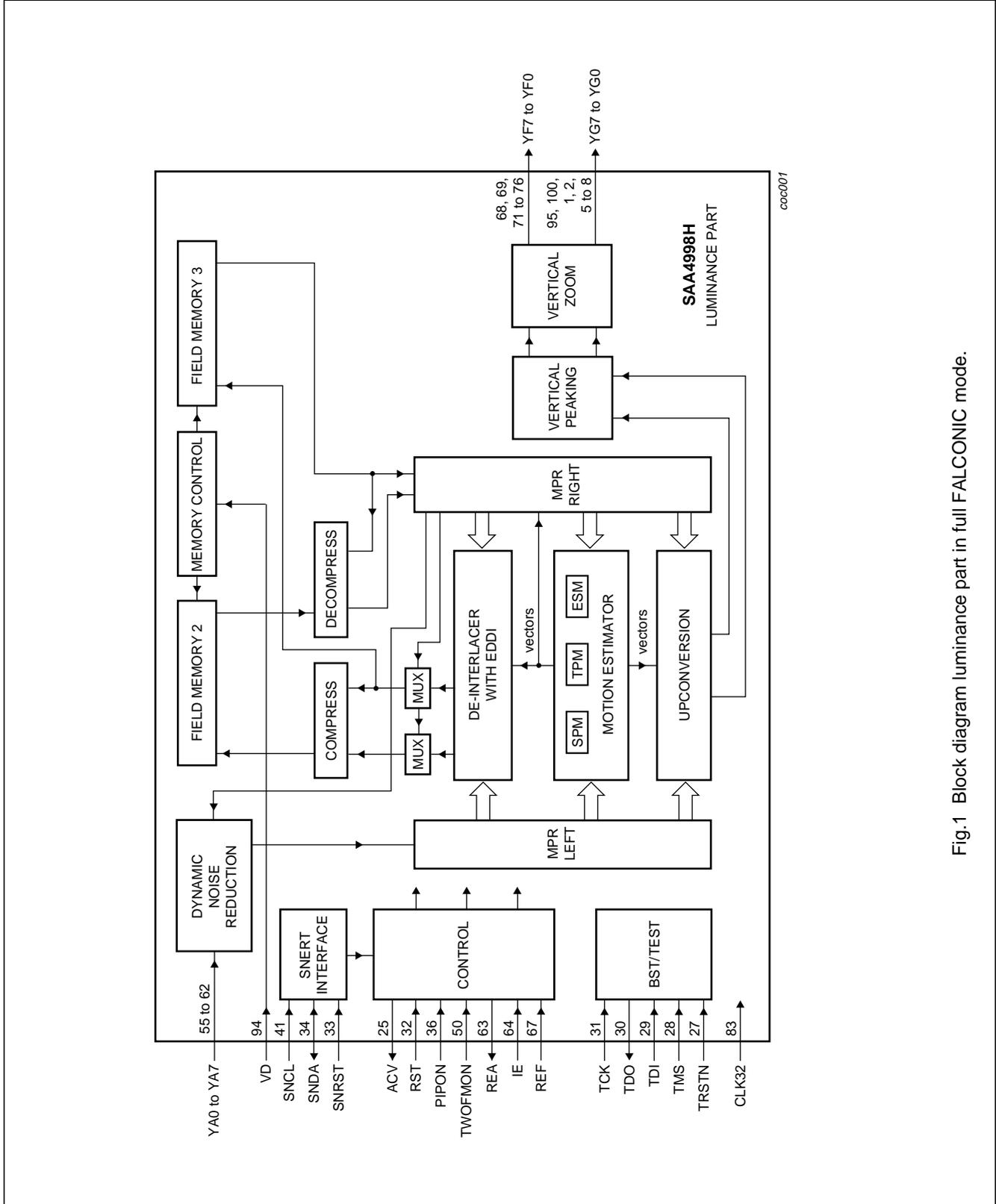


Fig.1 Block diagram luminance part in full FALCONIC mode.

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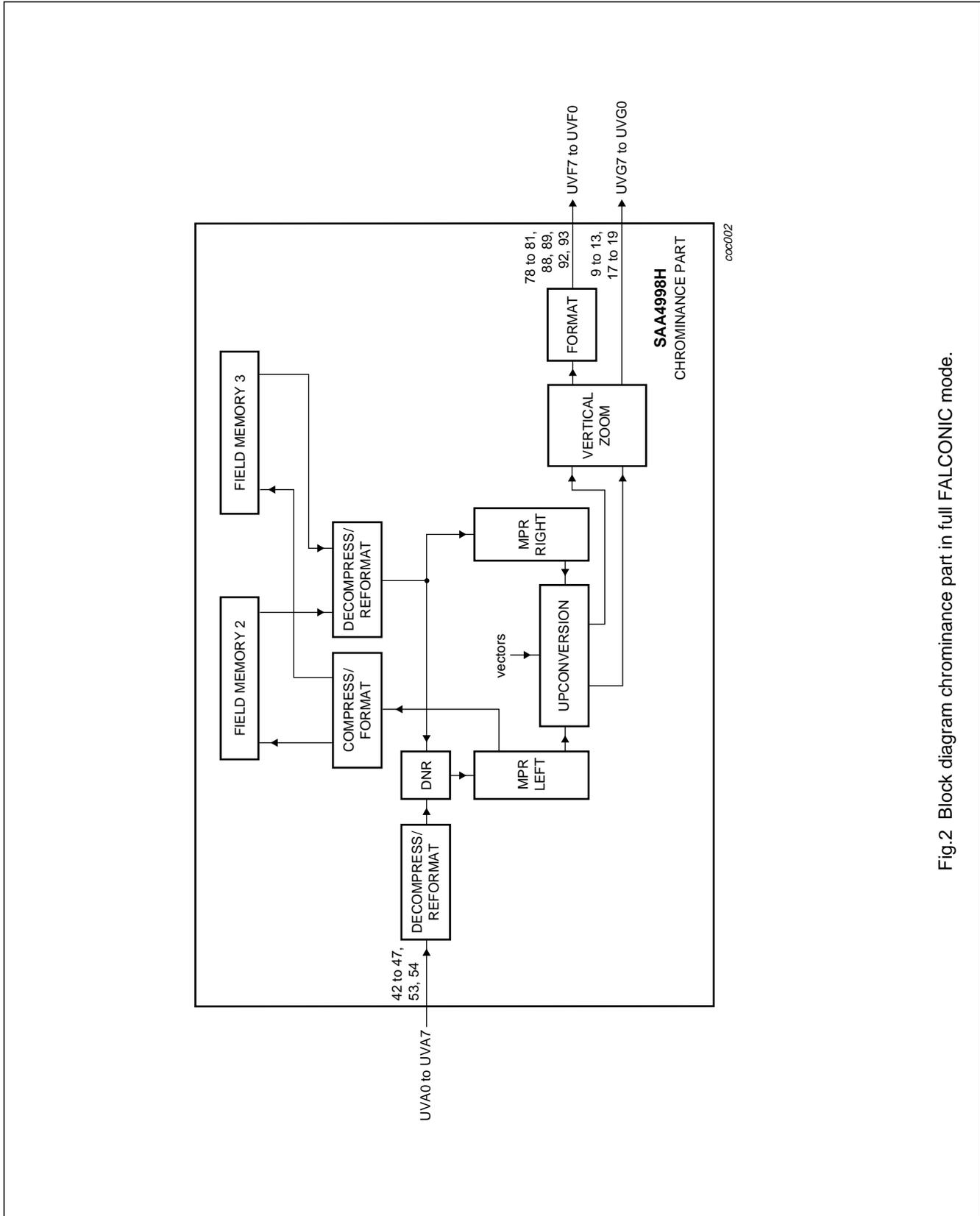


Fig.2 Block diagram chrominance part in full FALCONIC mode.

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### 6 PINNING

SYMBOL	PIN	TYPE	DESCRIPTION <sup>(1)(2)(3)</sup>
YG5/DPIP5	1	output/input	PIP mode disabled: bus G luminance output bit 5; PIP mode enabled: PIP data input bit 5
YG4/DPIP4	2	output/input	PIP mode disabled: bus G luminance output bit 4; PIP mode enabled: PIP data input bit 4
V <sub>DDE</sub>	3	supply	supply voltage of output pads (3.3 V)
V <sub>SSE</sub>	4	ground	ground of output pads
YG3/DPIP3	5	output/input	PIP mode disabled: bus G luminance output bit 3; PIP mode enabled: PIP data input bit 3
YG2/DPIP2	6	output/input	PIP mode disabled: bus G luminance output bit 2; PIP mode enabled: PIP data input bit 2
YG1/DPIP1	7	output/input	PIP mode disabled: bus G luminance output bit 1; PIP mode enabled: PIP data input bit 1
YG0/DPIP0	8	output/input	PIP mode disabled: bus G luminance output bit 0 (LSB); PIP mode enabled: PIP data input bit 0 (LSB)
UVG7/QPIP7	9	output	PIP mode disabled: bus G chrominance output bit 7 (MSB); PIP mode enabled: PIP data output bit 7 (MSB)
UVG6/QPIP6	10	output	PIP mode disabled: bus G chrominance output bit 6; PIP mode enabled: PIP data output bit 6
UVG5/QPIP5	11	output	PIP mode disabled: bus G chrominance output bit 5; PIP mode enabled: PIP data output bit 5
UVG4/QPIP4	12	output	PIP mode disabled: bus G chrominance output bit 4; PIP mode enabled: PIP data output bit 4
UVG3/QPIP3	13	output	PIP mode disabled: bus G chrominance output bit 3; PIP mode enabled: PIP data output bit 3
n.c./LLC	14	input	PIP mode disabled: not connected; PIP mode enabled: line locked clock signal for PIP mode
V <sub>SSE</sub>	15	ground	ground of output pads
n.c./SWCK2	16	input	PIP mode disabled: not connected; PIP mode enabled: serial write clock for PIP memory
UVG2/QPIP2	17	output	PIP mode disabled: bus G chrominance output bit 2; PIP mode enabled: PIP data output bit 2
UVG1/QPIP1	18	output	PIP mode disabled: bus G chrominance output bit 1; PIP mode enabled: PIP data output bit 1
UVG0/QPIP0	19	output	PIP mode disabled: bus G chrominance output bit 0 (LSB); PIP mode enabled: PIP data output bit 0 (LSB)
n.c./RSTW2	20	input	PIP mode disabled: not connected; PIP mode enabled: write reset clock for PIP memory
n.c./OIE2	21	input	PIP mode disabled: not connected; PIP mode enabled: output enable for PIP memory output QPIP <sub>x</sub>
n.c./IE2	22	input	PIP mode disabled: not connected; PIP mode enabled: input enable for PIP memory
V <sub>DDP</sub>	23	supply	high supply voltage of the internal field memories (3.3 V)
n.c./WE2	24	input	PIP mode disabled: not connected; PIP mode enabled: write enable for PIP memory

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SYMBOL	PIN	TYPE	DESCRIPTION <sup>(1)(2)(3)</sup>
ACV/RE2	25	output/input	PIP mode disabled: active video output; PIP mode enabled: read enable for PIP memory
n.c./RSTR2	26	input	PIP mode disabled: not connected; PIP mode enabled: read reset for PIP memory
TRSTN	27	input	boundary scan test reset input (active LOW); with internal pull-up resistor
TMS	28	input	boundary scan test mode select input; with internal pull-up resistor
TDI	29	input	boundary scan test data input; with internal pull-up resistor
TDO	30	3-state	boundary scan test data output
TCK	31	input	boundary scan test clock input; with internal pull-up resistor
RST	32	input	reset input; see Fig.4
SNRST	33	input	SNERT bus reset input; with internal pull-down resistor
SNDA	34	input/output	SNERT bus data input and output; with internal pull-down resistor
V <sub>DDE</sub>	35	supply	supply voltage of output pads (3.3 V)
PIPON	36	input	PIP mode enable input
V <sub>S5M</sub>	37	ground	field memory ground
V <sub>DDM</sub>	38	supply	supply voltage of the internal field memories (1.8 V)
V <sub>S5M</sub>	39	ground	field memory ground
V <sub>DDM</sub>	40	supply	supply voltage of the internal field memories (1.8 V)
SNCL	41	input	SNERT bus clock input; with internal pull-down resistor
UVA0	42	input	bus A chrominance input bit 0 (LSB)
UVA1	43	input	bus A chrominance input bit 1
UVA2	44	input	bus A chrominance input bit 2
UVA3	45	input	bus A chrominance input bit 3
UVA4	46	input	bus A chrominance input bit 4
UVA5	47	input	bus A chrominance input bit 5
V <sub>DDD</sub>	48	supply	core supply voltage (1.8 V)
V <sub>SSD</sub>	49	ground	core ground
TWOFMON	50	input	to be connected to ground
V <sub>DDS</sub>	51	supply	supply voltage of the internal SRAMs (1.8 V)
V <sub>SSS</sub>	52	ground	ground of the internal SRAMs
UVA6	53	input	bus A chrominance input bit 6
UVA7	54	input	bus A chrominance input bit 7 (MSB)
YA0	55	input	bus A luminance input bit 0 (LSB)
YA1	56	input	bus A luminance input bit 1
YA2	57	input	bus A luminance input bit 2
YA3	58	input	bus A luminance input bit 3
YA4	59	input	bus A luminance input bit 4
YA5	60	input	bus A luminance input bit 5
YA6	61	input	bus A luminance input bit 6
YA7	62	input	bus A luminance input bit 7 (MSB)
REA	63	output	read enable output for bus A

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SYMBOL	PIN	TYPE	DESCRIPTION <sup>(1)(2)(3)</sup>
IE	64	input	input enable for PIP mode
V <sub>DDD</sub>	65	supply	core supply voltage (1.8 V)
V <sub>SSD</sub>	66	ground	core ground
REF	67	input	read enable input for bus F and G; note 4
YF7	68	output	bus F luminance output bit 7 (MSB)
YF6	69	output	bus F luminance output bit 6
V <sub>SSE</sub>	70	ground	ground of output pads
YF5	71	output	bus F luminance output bit 5
YF4	72	output	bus F luminance output bit 4
YF3	73	output	bus F luminance output bit 3
YF2	74	output	bus F luminance output bit 2
YF1	75	output	bus F luminance output bit 1
YF0	76	output	bus F luminance output bit 0 (LSB)
V <sub>DDE</sub>	77	supply	supply voltage of output pads (3.3 V)
UVF7	78	output	bus F chrominance output bit 7 (MSB)
UVF6	79	output	bus F chrominance output bit 6
UVF5	80	output	bus F chrominance output bit 5
UVF4	81	output	bus F chrominance output bit 4
V <sub>SSE</sub>	82	ground	ground of output pads
CLK32	83	input	system clock input (32 MHz)
V <sub>DDS</sub>	84	supply	supply voltage of the internal SRAMs (1.8 V)
V <sub>SSS</sub>	85	ground	ground of the internal SRAMs
V <sub>DDD</sub>	86	supply	core supply voltage (1.8 V)
V <sub>SSD</sub>	87	ground	core ground
UVF3	88	output	bus F chrominance output bit 3
UVF2	89	output	bus F chrominance output bit 2
V <sub>SSA</sub>	90	ground	analog ground of the internal PLL
V <sub>DDA</sub>	91	supply	analog supply voltage of the internal PLL (1.8 V)
UVF1	92	output	bus F chrominance output bit 1
UVF0	93	output	bus F chrominance output bit 0 (LSB)
VD	94	input	vertical display synchronization input (reset for field memories)
YG7/DPIP7	95	output/input	PIP mode disabled: bus G luminance output bit 7 (MSB); PIP mode enabled: PIP data input bit 7 (MSB)
V <sub>DDM</sub>	96	supply	supply voltage of the internal field memories (1.8 V)
V <sub>SSM</sub>	97	ground	field memory ground

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SYMBOL	PIN	TYPE	DESCRIPTION <sup>(1)(2)(3)</sup>
V <sub>DDM</sub>	98	supply	supply voltage of the internal field memories (1.8 V)
V <sub>SSM</sub>	99	ground	field memory ground
YG6/DPIP6	100	output/input	PIP mode disabled: bus G luminance output bit 6; PIP mode enabled: PIP data input bit 6

### Notes

1. **Not used input pins should be connected to ground.**
2. Because of the noisy characteristic of the supply voltage of output pads (V<sub>DDE</sub>), it is recommended not to connect V<sub>DDE</sub> directly at the high supply voltage of the intern field memories (V<sub>DDP</sub>). All pins V<sub>DDE</sub> should be buffered as close as possible to the device. V<sub>DDP</sub> needs a low noise supply voltage, therefore, it is recommended that V<sub>DDP</sub> has to be separated from V<sub>DDE</sub> by an external filter structure. Because of the high working frequency of the device, it is also recommended to filter the core supply voltage (V<sub>DD</sub>). All pins V<sub>DD</sub> should be buffered as close as possible to the device.
3. V<sub>SSD</sub>, V<sub>SSM</sub> and V<sub>SSS</sub> are connected internally.
4. REF rising edge must be after rising edge of SNRST in order to be detected.



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7 CONTROL REGISTER DESCRIPTION

NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7	6	5	4	3	2	1	0	DESCRIPTION <sup>(2)</sup>
<b>DNR/peaking/colour</b>											
<b>Kstep10</b>	010	write; S					X	X	X	X	set LUT value: $k = \frac{1}{16}$ if difference below (0 to 15)
Kstep0											set LUT value: $k = \frac{1}{8}$ if difference below (0 to 15)
Kstep1			X	X	X						
<b>Kstep32</b>	011	write; S									
Kstep2							X	X	X	X	set LUT value: $k = \frac{2}{8}$ if difference below (0 to 30 in multiples of 2)
Kstep3			X	X	X						set LUT value: $k = \frac{3}{8}$ if difference below (0 to 30 in multiples of 2)
<b>Kstep54</b>	012	write; S									
Kstep4							X	X	X	X	set LUT value: $k = \frac{4}{8}$ if difference below (0 to 60 in multiples of 4)
Kstep5			X	X	X						set LUT value: $k = \frac{5}{8}$ if difference below (0 to 60 in multiples of 4)
<b>Kstep76</b>	013	write; S									
Kstep6							X	X	X	X	set LUT value: $k = \frac{6}{8}$ if difference below (0, 8, 16, 24, 32, 40, 48, 56, 64, 72, 80, 88, 96, 104, 112 or 120)
Kstep7			X	X	X						set LUT value: $k = \frac{7}{8}$ if difference below (0, 8, 16, 24, 32, 40, 48, 56, 64, 72, 80, 88, 96, 104, 112 or 120)
<b>Gain_fix_y</b>	014	write; S									
FixvalY							X	X	X	X	set fixed Y value; used when FixY = 1 or in left part of split screen (0, $\frac{1}{16}$ to $\frac{14}{16}$ or $\frac{15}{16}$ )
GainY			X	X	X						set gain in difference signal for adaptive DNR Y ( $\frac{1}{8}$ , $\frac{1}{4}$ , $\frac{1}{2}$ , 1, 2 or 4)
FixY			X								select fixed Y (adaptive or fixed) (full screen)
<b>Gain_fix_uv</b>	015	write; S									
FixvalUV							X	X	X	X	set fixed UV value; used when FixUV = 1 or in left part of split screen (0, $\frac{1}{16}$ to $\frac{14}{16}$ or $\frac{15}{16}$ )
GainUV			X	X	X						set gain in difference signal for adaptive DNR UV ( $\frac{1}{8}$ , $\frac{1}{4}$ , $\frac{1}{2}$ , 1, 2 or 4)
FixUV			X								select fixed UV (adaptive or fixed) (full screen)



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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7	6	5	4	3	2	1	0	DESCRIPTION <sup>(2)</sup>
<b>Zoom4</b>	01B	write; F									
ZoomEnVal						X	X	X	X	X	zoom run in value = number of lines without zoom active <b>(0 to 15 lines)</b>
ZoomDiVal			X	X	X						zoom run out value = number of lines without zoom active <b>(-8 to +7 lines)</b>
<b>De-interlacer</b>											
<b>Proscan1</b>	01C	write; S									
KifLim						X	X	X	X	X	limitation of recursion factor in calculation of original line positions: <b>(1 to 16)</b> ; 1 limits to almost full recursion, 16 limits to no recursion
KifOfs			X	X	X						The transfer curve of the de-interlacing filter coefficient is determined by the difference (Diff) between a line in the input field and the counterpart in the previous field shifted over the estimated motion vector. KifOfs determines the bias of the transfer curve for the original input line, such that coefficient = KifOfs + F(Diff), where the function F is calculated in the SAA4998H. The bias can take a value in the range <b>(0 to 15)</b> , representing decreasing filter strength.
<b>Proscan2</b>	01D	write; S									
PifLim						X	X	X	X	X	limitation of recursion factor in calculation of interpolated line positions: <b>(1 to 16)</b> ; 1 limits to almost full recursion, 16 limits to no recursion
PifOfs			X	X	X						see KifOfs; this offset applies to interpolated lines
<b>Proscan3</b>	01E	write; S									
PeakLim						X	X	X	X	X	Maximum that the peaked pixel is allowed to deviate from original pixel value: deviation <b>(0 to 30 in steps of 2)</b> . Above this deviation, the peaked pixel is clipped to (original pixel + or - PeakLim).
DeiOfs			X	X	X						offset to bias between average and median in the initial de-interlacing, if the KplFad = MIX option is chosen

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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7	6	5	4	3	2	1	0	DESCRIPTION <sup>(2)</sup>
<b>Proscan4</b> PflThr	01F	write, F					X	X	X	X	Multiplier threshold at which to switch the lower limit of the filter coefficient for interpolated lines. Above this threshold, the differences corresponding to the two neighbouring lines are used as clipping parameters, below this threshold, the interpolated line difference is used as clipping level. This parameter can be used to optimize the de-interlacing quality in slowly moving edges; it is not likely to have effect if PflLim is high.
AdRecOut						X					select adaptive recursive or order statistic output ( <b>order statistic or adaptive</b> )
ProDiv				X							Scaling factor to control the strength of the filtering for the interpolated lines. A value 0 means no scaling (normal filtering), while 3 means scaling by factor 8 (very strong filtering). This parameter can be used to adjust the de-interlacing to varying level of noise in the input picture; use higher scaling for higher noise.
KplOff			X								disable all recursion in calculating pixels for frame memory ( <b>recursive or non recursive</b> )
<b>Proscan5</b> VecRbf	0CB	write, S					X	X	X	X	Roll back factor on vectors used for motion-compensated de-interlacing. Values <b>0 to 14</b> (on a scale of 16) indicate attenuation. A value of <b>15</b> indicates no attenuation.
FadDiv				X	X						sensitivity scaling factor in transition from average to median in initial de-interlacing
KplFad			X								chooses between majority selection and median/average mix for initial de-interlacing ( <b>majority or mix</b> ); when KplFad = 0, FadDiv and DeiOfs are don't cares
<b>Proscan6</b> EddiOut EddiDemo EddiCmp	0F0	write, S								X	turns EDDI on and off ( <b>off or on</b> ) activates split screen demonstration mode for EDDI ( <b>off or on</b> ) Factor to specify the size of the additional compensation area left and right of the 'real' edge. A high factor (e.g. 1) can increase the compensation in regions far away from the true edge ( <b>1, 1/2, 1/4 or 1/8</b> ).

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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7	6	5	4	3	2	1	0	DESCRIPTION <sup>(2)</sup>
<b>Proscan7</b>	0F1	write; S							X	X	Factor for the comparison of the monotonous regions belonging to two edge points to verify an edge (1, 1/2, 1/4 or 1/8). Factor for the comparison of the monotonous regions belonging to two edge points and the edge point distance to verify an edge (1, 1/2, 1/4 or 1/8). minimal required Y difference at edge point position to be a reliable edge point; higher values result in higher reliability of EDDI, but less edges will be detected (0 to 60 in multiples of 4)
EddiMR								X			
EddiED						X					
EddiDif			X	X	X						
<b>Proscan8</b>	0F2	write; S					X	X	X	X	minimal required edge filter value at start and end of the monotonous region to be a reliable edge point; should be set higher in pictures with noise (0 to 60 in multiples of 4) minimal required length of monotonous region to be reliable; higher values result in higher reliability of EDDI, but less steep edges will be detected (2, 3, 4 or 5)
EddiFil								X			
EddiLng				X							
<b>Proscan9</b>	0F3	write; S									offset to increase or decrease the amount of EDDI compensation; lower values increase the amount of compensation (1 to 16) limitation of the compensation factor of EDDI; 1 limits to full EDDI compensation, 16 limits to almost no EDDI compensation (1 to 16)
EddiOfs						X	X	X	X	X	
EddiLim			X	X	X						
<b>General</b>											
<b>NrBlks</b>	020	write; S									number of blocks in active video (6 to 53, corresponds to 96 to 848 pixels), to be set as 1/16 (number of active pixels per line + 15); take remarks on TotalPxDiv8 into consideration total number of output lines (bits 9 and 8) total number of output lines (bits 7 to 0)
NrBlks				X	X	X	X	X	X	X	
TotalLnsAct98			X								
<b>TotalLnsAct70</b>	021	write; S	X	X	X	X	X	X	X	X	

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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	DESCRIPTION <sup>(2)</sup>								
			0	1	2	3	4	5	6	7	
<b>TotalPxDiv8</b>	022	write, S	X	X	X	X	X	X	X	X	Total number of pixels per line divided-by-8 (80 to 128, corresponds to 640 to 1024 pixels). The horizontal blanking interval is calculated as $\text{TotalPxDiv8} - 2 \times \text{NrBlks}$ and has to be in the range from 12 to 124 (corresponds to 96 to 992 pixels). Conclusion: TotalPxDiv8 has to be set to $12 + 2 \times \text{NrBlks} < \text{TotalPxDiv8} < 124 + 2 \times \text{NrBlks}$ and NrBlks has to be set to $\frac{\text{TotalPxDiv8} - 124}{2} < \text{NrBlks} < \frac{\text{TotalPxDiv8} - 12}{2}$
<b>REaShift</b>	023	write, S	X	X	X	X	X	X	X	X	shift of REA signal in number of pixels (0, +1, +2, +3, -4, -3, -2 or -1)
<b>WEbdReceShift</b>	024	write, S									reserved
<b>REceShift</b>									X	X	reserved
<b>POR</b>	025	write, S									power-on reset command, to be set high temporarily during start-up (normal or reset); note 3
<b>ScalingFactor</b>	0D6	write, S	X	X	X	X	X	X	X	X	8-bit scaling factor for EggSliceMix, EggSliceRgt and global activity (the same factor for all registers). output value (n+1) = $\frac{\text{ScalingFactor}}{128} \times \text{output value (n)}$
<b>FieldMemoryControl</b>	000	write, F									
<b>PIPON</b>										X	Picture-In-Picture (PIP) field memory mode enable
<b>TWOFMON</b>				0							has to be set to logic 0
<b>PIPDataDelay</b>					X						input data will be delayed by one clock cycle with respect to WE2 (write enable)
<b>PIPStillPicture</b>							X				no new data will be written into the field memory

Field and line rate converter with noise reduction and embedded memory

SAA4998H

NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7 6 5 4 3 2 1 0							DESCRIPTION <sup>(2)</sup>	
			7	6	5	4	3	2	1		0
<b>Mode control</b>											
<b>Control1</b>	026	write, F								X	Set estimator mode; <b>0</b> = line alternating use of left and right estimator: use in progressive scan except with vertical compress. <b>1</b> = field alternating use of left and right estimator: use in field doubling and progressive scan with vertical compress.
FilmMode									X		set film mode; <b>0</b> = video camera mode; <b>1</b> = film mode
UpcMode					X						select upconversion quality; <b>00</b> = full, <b>01</b> = economy (DPCM), <b>10</b> = single memory with motion compensation, <b>11</b> = single memory without motion compensation
MatrixOn				X							set matrix output mode; <b>1</b> = double output, disabling vertical peaking; <b>0</b> = normal single output mode; this bit setting is the AND function of BusGControl bits
EmbraceOn						X					Master enable for embrace mode ( <b>off or on</b> ); SwapMpr in control2 should be at 'swap' position to really cross-switch FM1 and FM3 field outputs. Should be set to logic 0 except in film mode and FM3 is present.
MemComp									X		set memory compression (luminance DPCM) ( <b>off or on</b> )
MemDecom									X		set memory decompression (luminance DPCM) ( <b>off or on</b> )

Field and line rate converter with noise reduction and embedded memory

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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7	6	5	4	3	2	1	0	DESCRIPTION <sup>(2)</sup>
<b>Control2</b>	027	write, F								X	Quincunx phase of current field (in TPM) ( <b>phase0 or phase1</b> ); this needs to toggle each time a new field comes from FM1. In phase0 the estimator operates on a checker-board pattern that starts with the left upper block; in phase1 the other blocks are estimated.
QQcurr										X	Quincunx phase of previous field (in TPM) ( <b>phase0 or phase1</b> ); this is the value of QQcurr during the last estimate written into the temporal prediction memory
QQprev									X		Field status ( <b>same input field or new input field</b> ); reflects whether the output of FM1 is a new or a repeated field. This bit will toggle field by field in field doubling mode and is continuously HIGH in progressive output mode.
FldStat							X				enable writing FM2 and FM3 for both luminance and chrominance (recirculation of data for luminance alone can be controlled with OrigFmEnY and IntpFmEnY in Control3) ( <b>off or on</b> )
FieldWeYUV						X					odd input field ( <b>even or odd</b> ), this is to be set equal to the detected field interlace for the field that comes out of FM1
OddFM1					X						Swap multi port RAMs ( <b>normal or swap</b> ); this bit needs to be set to get real frame data at the temporal position from FM1. If swapped, the current field (FM1) will be stored in the right line memory tree, while the original lines from the stored frame (FM2/3) are stored in the left memory tree. Should be set only in film mode if FM3 is present; EmbraceOn must be set as well.
SwapMpr				X							Set vertical vector offset ( <b>0, +1, - or -1</b> ) frame lines; vertical offset of the right line memory tree with respect to the left line memory tree. A higher offset value means: on the right memory tree access to less delayed video lines is taken; in interlaced video operation, the vertical offset will be -1 with an odd field on the left side and +1 with an even field on the left. With non-interlaced input, vertical offset should be constantly 0. In film mode, vertical offset is dynamically switched between +1, 0 and -1.
VecOffs			X	X							



Field and line rate converter with noise reduction and embedded memory

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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	DESCRIPTION <sup>(2)</sup>									
			7	6	5	4	3	2	1	0		
Upconv2 YVecClip	02A	write S	X	X		X						
RollBack		F	X	X	X							
Upconv3	02B	write; S										
MeizLfbm											X	
Meizmemc										X		
MeiDeint									X			
MixCtrl			X	X	X	X	X					
UpcColShiFac	0C4	write; F			X	X	X	X	X	X	X	X
Upconv4	0C5	write; S										
Lfindex									X	X	X	X
MCDemo												
EggSlice1	0C6	write; S	X									
EggStartLine												

Field and line rate converter with noise reduction and embedded memory

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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7	6	5	4	3	2	1	0	DESCRIPTION <sup>(2)</sup>
<b>EggSlice2</b>	0C7	write; S		X		X	X	X	X	X	Minimum line egg slice right value to activate reliability measurement. The parameter is multiplied internally by 4.
EggSlicThr					X						
EggRelInd			X								The egg slice reliability is computed internally as EggSliceRgt (ESR) > RelFactor × EggSliceMix (ESM). RelFactor is determined by EggRelInd (2/8, 3/8, 4/8 or 5/8).
<b>SafeShiFac</b>	0C8	write; F		X		X	X	X	X	X	upconverter shift factor to be used in protection mode; <b>0</b> (for current field position) <b>to 32</b> (for previous field position)
<b>Motion estimator</b>											
<b>Motest1</b>	02C	write; S					X	X	X	X	additional penalty on vector candidates with odd vertical component ( <b>0, 8, 16, 32, 64, 128, 256 or 511</b> )
PenOdd											
SpcThr				X		X					Active when EstMode = 0: replace the spatial prediction of one estimator (left or right) by that of the other if the match error of the former exceeds that of the latter by more than ( <b>0, 8, 16, 32, 64, 128, 256 or 511</b> ). A higher threshold means the two estimators are very independent.
BmsThr			X								Active when EstMode = 0; select as estimated vector the output of the right estimator unless its match error exceeds that of the left estimator by more than ( <b>0, 8, 16 or 32</b> ). This parameter should normally be set to logic 0.
<b>Motest2</b>	02D	write; S									
TavLow										X	If the difference between the current vector and the previous one in the same spatial location is within a small window, then the two vectors are averaged to improve temporal consistency. TavLow is the lower threshold of this window ( <b>1 or 2</b> ).
TavUpp							X				see above; TavUpp is the upper threshold ( <b>0, 4, 8 or 16</b> )
MedEns					X						scaling factor to reduce all sizes of update vectors in the ensemble with medium sized vector templates ( <b>1, 1/2, 1/4 or 1/8</b> )
LarEns			X								scaling factor to reduce all sizes of update vectors in the ensemble with large sized vector templates ( <b>1, 1/2, 1/4 or 1/8</b> )



Field and line rate converter with noise reduction and embedded memory

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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7	6	5	4	3	2	1	0	DESCRIPTION <sup>(2)</sup>
<b>LeftBorder</b>	0CF	write; S									
LeftBorder			X						X		estimator left border (in 8-pixel blocks)
WinNullWrite			X								enable writing of null vectors outside estimators' active window (off or on)
<b>RightBorder</b>	0D0	write; S									
RightBorder			X						X		estimator right border (in 8-pixel blocks)
<b>TopBorder</b>	0D1	write; S									
TopBorder			X						X		estimator top border (in 4-line blocks)
<b>BottomBorder</b>	0D2	write; S									
BottomBorder			X						X		estimator bottom border (in 4-line blocks)
<b>Candidate1</b>	090	write; S									
Candidate1								X	X		selection Candidate1 (SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max)
Update1				X							update for Candidate1 (zero update, medium update, large update or zero update)
Penalty1			X	X							penalty for Candidate1 (0, 8, 16, 32, 64, 128, 256 or 511)
<b>Candidate2</b>	091	write; S									
Candidate2								X	X		selection Candidate2 (SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max)
Update2				X							update for Candidate2 (zero update, medium update, large update or zero update)
Penalty2			X	X							penalty for Candidate2 (0, 8, 16, 32, 64, 128, 256 or 511)
<b>Candidate3</b>	092	write; S									
Candidate3								X	X		selection Candidate3 (SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max)
Update3				X							update for Candidate3 (zero update, medium update, large update or zero update)
Penalty3			X	X							penalty for Candidate3 (0, 8, 16, 32, 64, 128, 256 or 511)
<b>Candidate4</b>	093	write; S									
Candidate4								X	X		selection Candidate4 (SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max)
Update4				X							update for Candidate4 (zero update, medium update, large update or zero update)
Penalty4			X	X							penalty for Candidate4 (0, 8, 16, 32, 64, 128, 256 or 511)

Field and line rate converter with noise reduction and embedded memory

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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7	6	5	4	3	2	1	0	DESCRIPTION <sup>(2)</sup>
<b>Candidate5</b>	094	write; S									
Candidat5						X			X	X	selection Candidate5 (SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max)
Update5					X						update for Candidate5 (zero update, medium update, large update or zero update)
Penalty5				X	X						penalty for Candidate5 (0, 8, 16, 32, 64, 128, 256 or 511)
<b>Candidate6</b>	095	write; S									
Candidat6						X			X	X	selection Candidate6 (SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max)
Update6					X			X			update for Candidate6 (zero update, medium update, large update or zero update)
Penalty6				X	X						penalty for Candidate6 (0, 8, 16, 32, 64, 128, 256 or 511)
<b>Candidate7</b>	096	write; S									
Candidat7							X		X	X	selection Candidate7 (SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max)
Update7					X			X			update for Candidate7 (zero update, medium update, large update or zero update)
Penalty7				X	X						penalty for Candidate7 (0, 8, 16, 32, 64, 128, 256 or 511)
<b>Candidate8</b>	097	write; S									
Candidat8							X		X	X	selection Candidate8 (SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max)
Update8					X			X			update for Candidate8 (zero update, medium update, large update or zero update)
Penalty8				X	X						penalty for Candidate8 (0, 8, 16, 32, 64, 128, 256 or 511)
<b>PZpositionLeftUppX</b>	098	write; S				X	X	X	X	X	X position of LeftUpp measurement point for pan-zoom calculations (resolution: 16 pixels)
<b>PZpositionLeftUppY</b>	099	write; S				X	X	X	X	X	Y position of LeftUpp measurement point for pan-zoom calculations (resolution: 4 lines)
<b>PZpositionRightLowX</b>	09A	write; S				X	X	X	X	X	X position of RightLow measurement point for pan-zoom calculations (resolution: 16 pixels)
<b>PZpositionRightLowY</b>	09B	write; S				X	X	X	X	X	Y position of RightLow measurement point for pan-zoom calculations (resolution: 4 lines)
<b>PZvectorStartX</b>	09C	write; F	X	X	X	X	X	X	X	X	X start value of pan-zoom vectors

Field and line rate converter with noise reduction and embedded memory

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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7	6	5	4	3	2	1	0	DESCRIPTION <sup>(2)</sup>
PZvectorDeltaX	09D	write; F	X	X	X	X	X	X	X	X	X delta value of pan-zoom vectors
PZvectorStartY	09E	write; F	X	X	X	X	X	X	X	X	Y start value of pan-zoom vectors
PZvectorDeltaY	09F	write; F	X	X	X	X	X	X	X	X	Y delta value of pan-zoom vectors
Read data; note 3											
GlobalMSEmsb	0A0	read; F	X	X	X	X	X	X	X	X	Global Mean Square Error (MSE) = summation within a field period of squared differences in comparing vector shifted video from frame memory (FM2/3) with new field input (FM1) in those lines coinciding with new field lines. The window for the measurement is kept at 40 pixels horizontal and 20 field lines vertical from the border of the video. Measurements is only done in fields where the de-interlacer is active, otherwise reading is zero. In field doubling mode, MSE is zero at the end of every new input field.
GlobalMSElsb	0A1	read; F	X	X	X	X	X	X	X	X	
GlobalMTImsb	0A2	read; F	X	X	X	X	X	X	X	X	Global Motion Trajectory Inconsistency (MTI) = summation within a field period of squared differences comparing shifted video from frame memory (FM2/3 output) with filtered data that is rewritten to the frame memory (FM2/3 input) in those lines coinciding with new field lines. The window for the measurement is kept at 40 pixels horizontal and 20 field lines vertical from the border of the video. Measurement is done only in fields where de-interlacer is active, otherwise reading is zero; in field doubling mode, MTI is zero at the end of every new input field.
GlobalMTIlsb	0A3	read; F	X	X	X	X	X	X	X	X	
GlobalACTmsb	0A4	read; F	X	X	X	X	X	X	X	X	global activity (ACT) = summation over a field period of the horizontal plus the vertical components of the vectors of all blocks
GlobalACTlsb	0A5	read; F	X	X	X	X	X	X	X	X	
VectTempCons	0A6	read; F	X	X	X	X	X	X	X	X	Vector temporal consistency = summation over a field period of absolute differences of horizontal plus vertical components of vectors newly estimated for each block compared with those vectors estimated in the previous run at the same spatial block position. It should be noted that a lower figure implies better consistency.
VectSpatCons	0A7	read; F	X	X	X	X	X	X	X	X	Vector spatial consistency = summation over a field period of absolute differences of horizontal and vertical components of vectors compared with those of the neighbour blocks (L, R, U and D); in the comparison, all vector data is used from the previous estimator run. It should be noted that a lower figure implies better consistency.
BlockErrCnt	0A8	read; F	X	X	X	X	X	X	X	X	burst error count (number of burst errors)

Field and line rate converter with noise reduction and embedded memory

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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7	6	5	4	3	2	1	0	DESCRIPTION <sup>(2)</sup>
LeastErrSum	0A9	read; F	X	X	X	X	X	X	X	X	least error sum (summation over a field period of the smallest match error that the estimator has found for each block; indicates reliability of the estimation process)
YvecRangeErrCntmsb	0AA	read; F	X	X	X	X	X	X	X	X	Y vector range error count (number of vectors that have a vertical component that is out of range for upconversion at the chosen temporal position) (15 to 8)
YvecRangeErrCntlsb	0AB	read; F	X	X	X	X	X	X	X	X	Y vector range error count (7 to 0)
RefLineCountPrev	0AC	read; F	X	X	X	X	X	X	X	X	read out of [number of input (run-) lines – 40] used in previous field
RefLineCountNew	0AD	write; F	X	X	X	X	X	X	X	X	Write of [number of input (run-) lines – 40] to be used in new field (actual maximum number of input lines in normal operation: 292; register value 252). Nominally this is to be set as an exact copy of the value read from RefLineCountPrev before a new field starts. In case the effective number of input (run-) lines has increased, RefLineCountNew should, for one field, be set to 255. This will occur e.g. with decreasing vertical zoom magnification or changing from 525 lines video standard to 625 lines standard. If this is not done, a deadlock will occur with too few lines processed correctly by the motion estimator.
PanZoomVec0-X	0B0	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 0 (8-bit X value)
PanZoomVec0-Y	0B1	read									
FalconIdent		S	0								SAA4998H identification: fixed bit, reading this bit as zero means SAA4998H is present
PanZoomVec0-Y		F		X	X	X	X	X	X	X	pan-zoom vector 0 (7-bit Y value)
PanZoomVec1-X	0B2	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 1 (8-bit X value)
PanZoomVec1-Y	0B3	read									
StatusJump0		S	X								1: both field memories are in use by the motion estimation and motion compensation function; see Fig.1 0: field memory 2 is in use by the motion estimation and motion compensation function; field memory 3 for PIP application; see Fig.1
PanZoomVec1-Y		F		X	X	X	X	X	X	X	pan-zoom vector 1 (7-bit Y value)
PanZoomVec2-X	0B4	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 2 (8-bit X value)
PanZoomVec2-Y	0B5	read									
StatusJump1		S	1								logic 1
PanZoomVec2-Y		F		X	X	X	X	X	X	X	pan-zoom vector 2 (7-bit Y value)

## Field and line rate converter with noise reduction and embedded memory

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NAME	SNERT ADDRESS (HEX)	READ/ WRITE <sup>(1)</sup>	7	6	5	4	3	2	1	0	DESCRIPTION <sup>(2)</sup>
PanZoomVec3-X	0B6	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 2 (8-bit X value)
PanZoomVec3-Y	0B7	read; F		X	X	X	X	X	X	X	pan-zoom vector 3 (7-bit Y value)
PanZoomVec4-X	0B8	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 4 (8-bit X value)
PanZoomVec4-Y	0B9	read; F		X	X	X	X	X	X	X	pan-zoom vector 4 (7-bit Y value)
PanZoomVec5-X	0BA	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 5 (8-bit X value)
PanZoomVec5-Y	0BB	read; F		X	X	X	X	X	X	X	pan-zoom vector 5 (7-bit Y value)
PanZoomVec6-X	0BC	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 6 (8-bit X value)
PanZoomVec6-Y	0BD	read; F		X	X	X	X	X	X	X	pan-zoom vector 6 (7-bit Y value)
PanZoomVec7-X	0BE	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 7 (8-bit X value)
PanZoomVec7-Y	0BF	read; F		X	X	X	X	X	X	X	pan-zoom vector 7 (7-bit Y value)
PanZoomVec8-X	0AE	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 8 (8-bit X value)
PanZoomVec8-Y	0AF	read; F		X	X	X	X	X	X	X	pan-zoom vector 8 (7-bit Y value)
EggSliceRgtMSB	0C0	read; F	X	X	X	X	X	X	X	X	result of right pixels egg-slice detector (15 to 8)
EggSliceRgtLSB	0C1	read; F	X	X	X	X	X	X	X	X	result of right pixels egg-slice detector (7 to 0)
EggSliceMixMSB	0C2	read; F	X	X	X	X	X	X	X	X	result of mixed pixels egg-slice detector (15 to 8)
EggSliceMixLSB	0C3	read; F	X	X	X	X	X	X	X	X	result of mixed pixels egg-slice detector (7 to 0)
SafeFbLine	0C9	read; F	X	X	X	X	X	X	X	X	reference line number (divided by two) at which the upconverter goes into protection mode
EggBinGoodness	0CA	read; F	X	X	X	X	X	X	X	X	Goodness of the four egg-slice sections, from top to bottom, 2 bits per section. Each section is represented with 2 bits in this register, where bits 0 and 1 represent the top section and bits 6 and 7 represent the lowest of the 4 sections. Each pair of bits indicate <b>00</b> = ( $ESR > \frac{3}{4}ESM$ ), <b>01</b> = ( $\frac{1}{2}ESM < ESR \leq \frac{3}{4}ESM$ ), <b>10</b> = ( $\frac{1}{4}ESM < ESR \leq \frac{1}{2}ESM$ ), <b>11</b> = ( $ESR \leq \frac{1}{4}ESM$ ).
LoActCnt	0D3	read; F	X	X	X	X	X	X	X	X	number of blocks having low activity
HiActCnt	0D4	read; F	X	X	X	X	X	X	X	X	number of blocks having high activity
NullErrSum	0D5	read; F	X	X	X	X	X	X	X	X	sum of errors for the null candidate over the complete field; when no null candidate is selected a value of FFH will be read

# Field and line rate converter with noise reduction and embedded memory

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## Notes

1. S means semi static, used at initialization or mode changes; F means field frequent, in general updated in each display field.
2. Selectable items are marked bold.
3. Almost all of the R(ead) and W(rite) registers of SAA4998H are double buffered. The write registers are latched by a signal called New\_field. New\_field gets set, when REF rises after SNRST (New\_field is effectively at the start of active video). The read registers are latched by a signal called Reg\_upd. Reg\_upd gets set, when half the number of active pixels of the fourth line of vertical blanking have entered the SAA4998H (Reg\_upd will effectively be active 3½ lines after the REA has ended). The only exception are the registers which are not double buffered, these are as follows:
  - a) Write register 025H: power\_on\_reset
  - b) Write register 02FH, bit 1: CndSet
  - c) Read register 0B0H to 0BFH, 0AEH and 0AFH: pan\_zoom\_vectors, including FalconIdent (= 0), StatusJump0 and StatusJump1.

## 8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DDD</sub>	core supply voltage (internal rail)		-0.5	+2.5	V
V <sub>DDA</sub>	analog supply voltage				
V <sub>DDM</sub>	field memory supply voltage				
V <sub>DDS</sub>	SRAM supply voltage				
V <sub>DDE</sub>	external supply voltage (output pads)		-0.5	+4.6	V
V <sub>DDP</sub>	high supply voltage of internal field memories				
V <sub>i</sub>	input voltage of all I/O pins		-0.5	+6 <sup>(1)</sup>	V
I <sub>o</sub>	output current		-	4	mA
T <sub>stg</sub>	storage temperature		-40	+125	°C
T <sub>j</sub>	junction temperature		0	125	°C
V <sub>esd</sub>	electrostatic discharge voltage on all pins	MM; note 2	-400	+400	V
		HBM; note 3	-3000	+3000	V

## Notes

1. Only valid, if V<sub>DDE</sub> is present.
2. In accordance with "Transient energy (ESD machine model); SNW-FQ-302B" class C, discharging a 200 pF capacitor via a 0.75 µH series inductance.
3. In accordance with "Transient energy (ESD human body model); SNW-FQ-302A" class 2, discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

## 9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	45	K/W
R <sub>th(j-c)</sub>	thermal resistance from junction to case		10	K/W

# Field and line rate converter with noise reduction and embedded memory

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## 10 CHARACTERISTICS

$V_{DDE} = 3.0$  to  $3.6$  V;  $T_{amb} = 0$  to  $70$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{DDD}$	core supply voltage (internal rail)		1.65	1.8	1.95	V
$V_{DDA}$	analog supply voltage					
$V_{DDM}$	field memory supply voltage					
$V_{DDS}$	SRAM supply voltage					
$V_{DDE}$	external supply voltage (output pads)		3.0	3.3	3.6	V
$V_{DDP}$	high supply voltage of internal field memories					
$I_{DD}$	sum of supply current					
	at 1.8 V supply voltage pins		–	180	–	mA
	at 3.3 V supply voltage pins		–	6	–	mA
<b>General</b>						
$V_{OH}$	HIGH-level output voltage		$V_{DDE} - 0.4$	–	–	V
$V_{OL}$	LOW-level output voltage		–	–	0.4	V
$V_{IH}$	HIGH-level input voltage		2	–	–	V
$V_{IL}$	LOW-level input voltage		–	–	0.8	V
$I_{OH}$	HIGH-level output current	10 ns slew rate output; $V_{OH} = V_{DDE} - 0.4$ V	–4	–	–	mA
$I_{OL}$	LOW-level output current	10 ns slew rate output; $V_{OL} = 0.4$ V	–	–	4	mA
$C_i$	input capacitance		–	–	8	pF
$I_{LI}$	input leakage current	note 1	–	–	1	μA
<b>Outputs; see Fig.5; note 2</b>						
$I_{OZ}$	output current in 3-state mode	$-0.5 < V_o < 3.6$	–	–	1	μA
$t_{d(o)}$	output delay time		–	–	23	ns
$t_{h(o)}$	output hold time		4	–	–	ns
<b>Inputs</b>						
$t_r$	rise time		–	–	30	ns
$t_f$	fall time		–	–	30	ns
$t_{su(i)}$	input set-up time	see Fig.5; note 3	6	–	–	ns
$t_{h(i)}$	input hold time	see Fig.5; note 3	2	–	–	ns
<b>Input CLK32; see Fig.5</b>						
$t_r$	rise time		–	–	4	ns
$t_f$	fall time		–	–	4	ns
$\delta$	duty factor		40	–	60	%
$T_{cy}$	cycle time		30	–	39	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>BST interface; see Fig.6</b>						
$T_{cy(BST)}$	BST cycle time		–	1	–	$\mu$ s
$t_{su(i)(BST)}$	input set-up time		3	–	–	ns
$t_{h(i)(BST)}$	input hold time		6	–	–	ns
$t_{h(o)(BST)}$	output hold time		4	–	–	ns
$t_{d(o)(BST)}$	output delay		–	–	30	ns
<b>SNERT interface; see Fig.7</b>						
$t_{SNRST(H)}$	SNRST pulse HIGH time		500	–	–	ns
$t_{d(SNRST-SNCL)}$	delay SNRST pulse to SNCL LOW time		200	–	–	ns
$T_{cy(SNCL)}$	SNCL cycle time		0.5	–	1	$\mu$ s
$t_{su(i)(SNCL)}$	input set-up time to SNCL		53	–	–	ns
$t_{h(i)(SNCL)}$	input hold time to SNCL		10	–	–	ns
$t_{h(o)}$	output hold time		30	–	–	ns
$t_{d(o)}$	output delay		–	–	330	ns
$t_{o(en)}$	output enable time		210	–	–	ns

Notes

1. All inputs except inputs with internal pull-up or pull-down resistor. These inputs have an absolute leakage current of maximum 50  $\mu$ A.
2. Timing characteristics are measured with  $C_L = 15$  pF.
3. All inputs except SNERT interface inputs, CLK32 input and BST/TEST inputs.

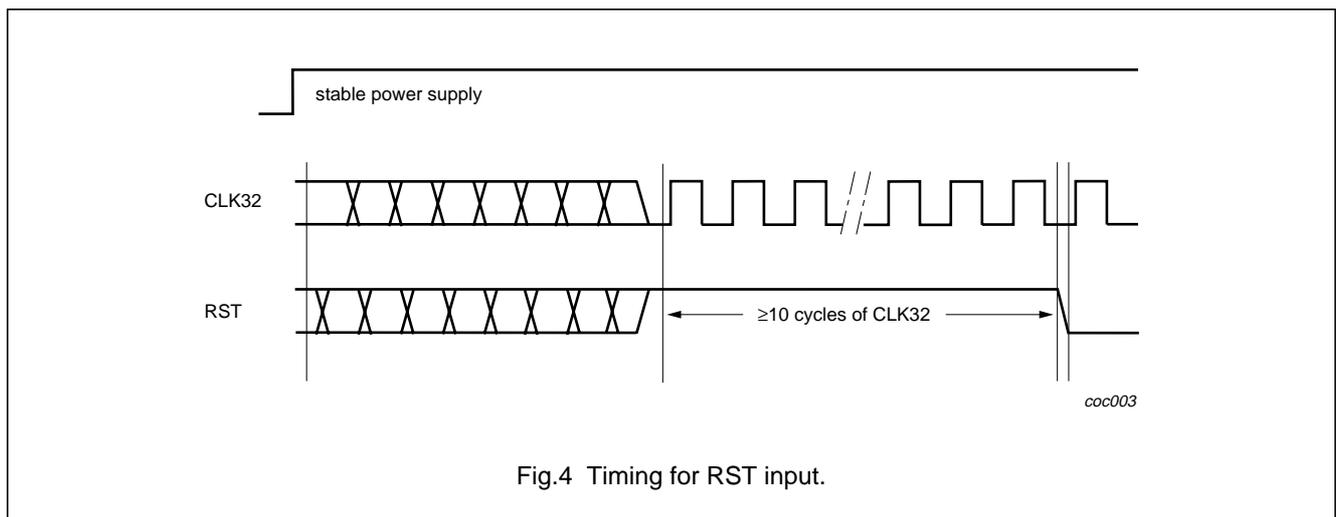


Fig.4 Timing for RST input.

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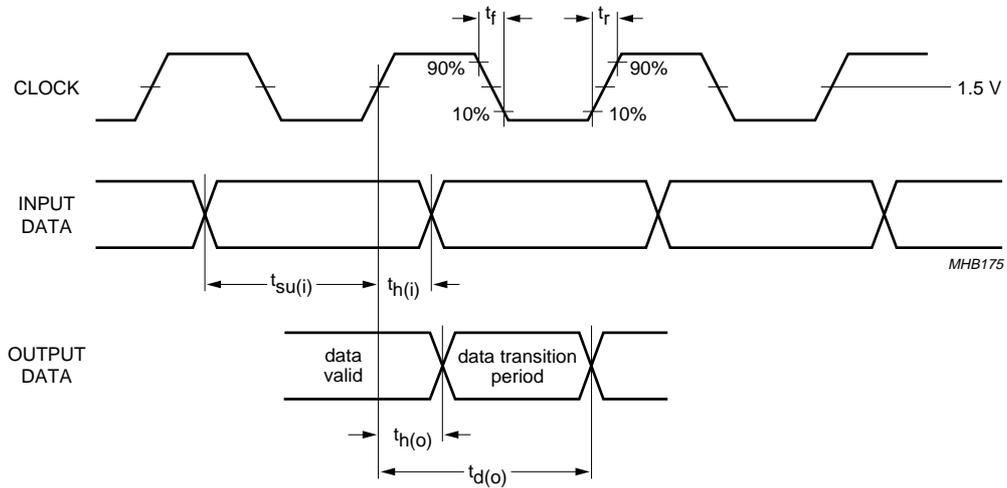


Fig.5 Data input/output timing diagram.

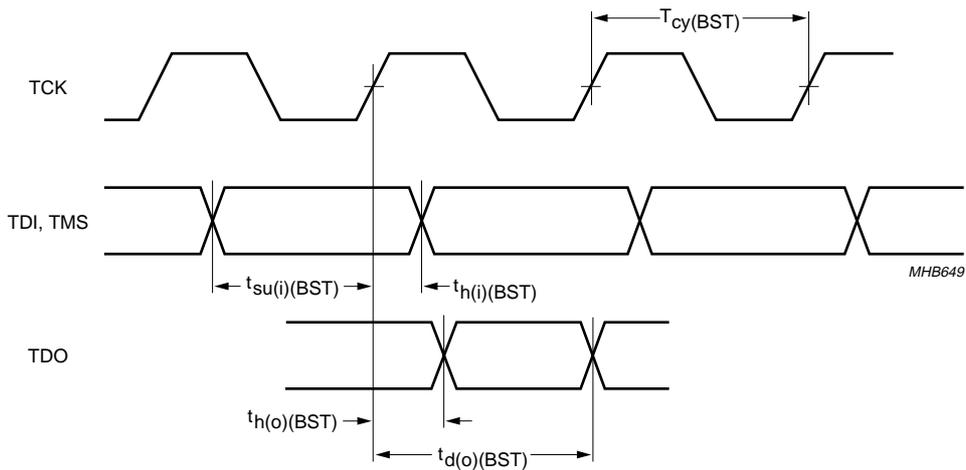


Fig.6 Boundary scan test interface timing diagram.

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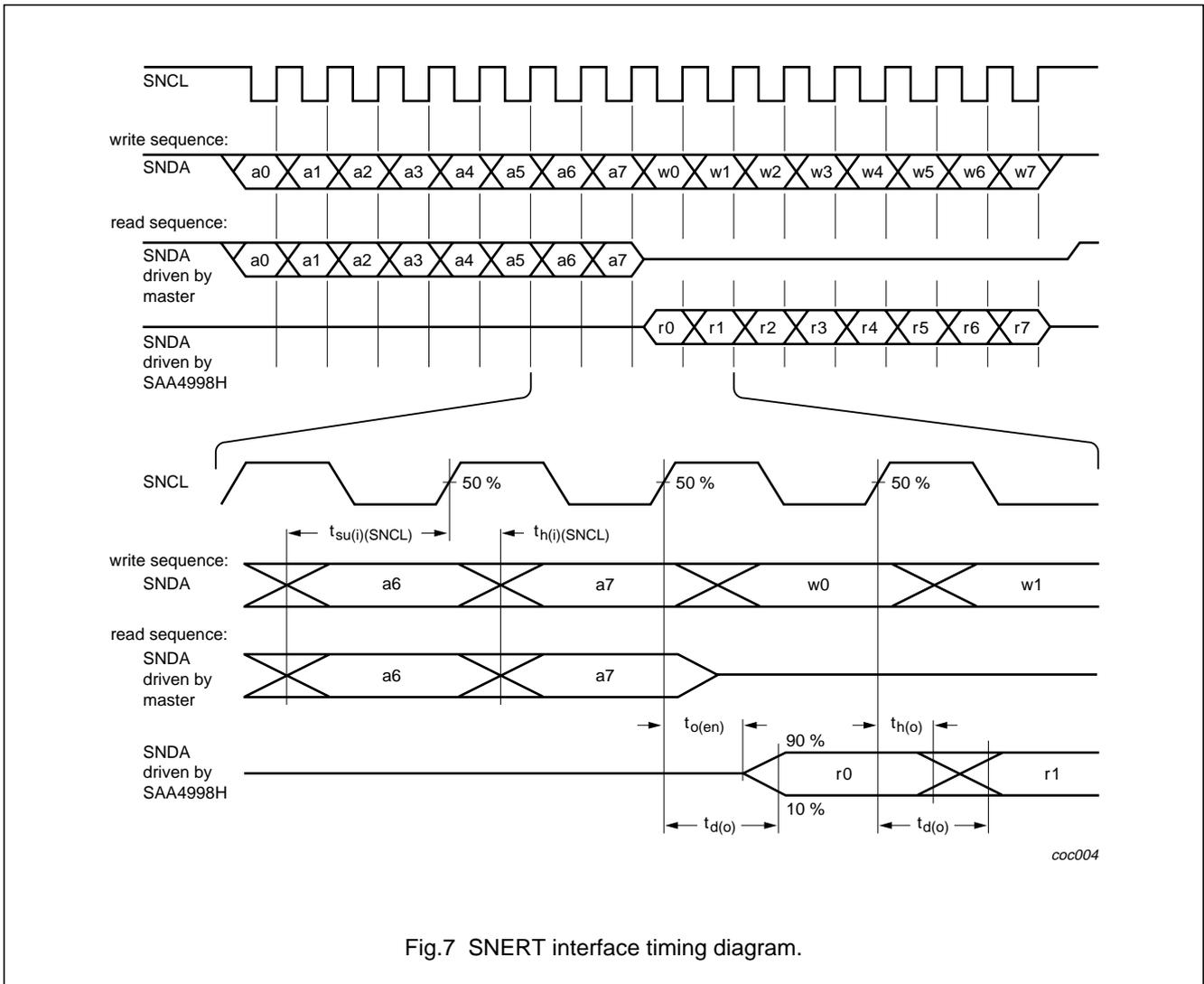


Fig.7 SNERT interface timing diagram.

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**Table 1** YUV formats

I/O PIN <sup>(1)</sup>	FORMAT <sup>(2)(3)</sup>							
	4 : 1 : 1				4 : 2 : 2		4 : 2 : 2 DPCM	
Yx7	Y07	Y17	Y27	Y37	Y07	Y17	Y07	Y17
Yx6	Y06	Y16	Y26	Y36	Y06	Y16	Y06	Y16
Yx5	Y05	Y15	Y25	Y35	Y05	Y15	Y05	Y15
Yx4	Y04	Y14	Y24	Y34	Y04	Y14	Y04	Y14
Yx3	Y03	Y13	Y23	Y33	Y03	Y13	Y03	Y13
Yx2	Y02	Y12	Y22	Y32	Y02	Y12	Y02	Y12
Yx1	Y01	Y11	Y21	Y31	Y01	Y11	Y01	Y11
Yx0	Y00	Y10	Y20	Y30	Y00	Y10	Y00	Y10
UVx7	U07	U05	U03	U01	U07	V07	UC03	VC03
UVx6	U06	U04	U02	U00	U06	V06	UC02	VC02
UVx5	V07	V05	V03	V01	U05	V05	UC01	VC01
UVx4	V06	V04	V02	V00	U04	V04	UC00	VC00
UVx3	X	X	X	X	U03	V03	X	X
UVx2	X	X	X	X	U02	V02	X	X
UVx1	X	X	X	X	U01	V01	X	X
UVx0	X	X	X	X	U00	V00	X	X

**Notes**

- Digit x refers to different I/O buses:
  - A = input from 1st field memory
  - F = main output
  - G = 2nd output for matrix purposes.
- The first index digit defines the sample number and the second defines the bit number.
- X = don't care or not available.

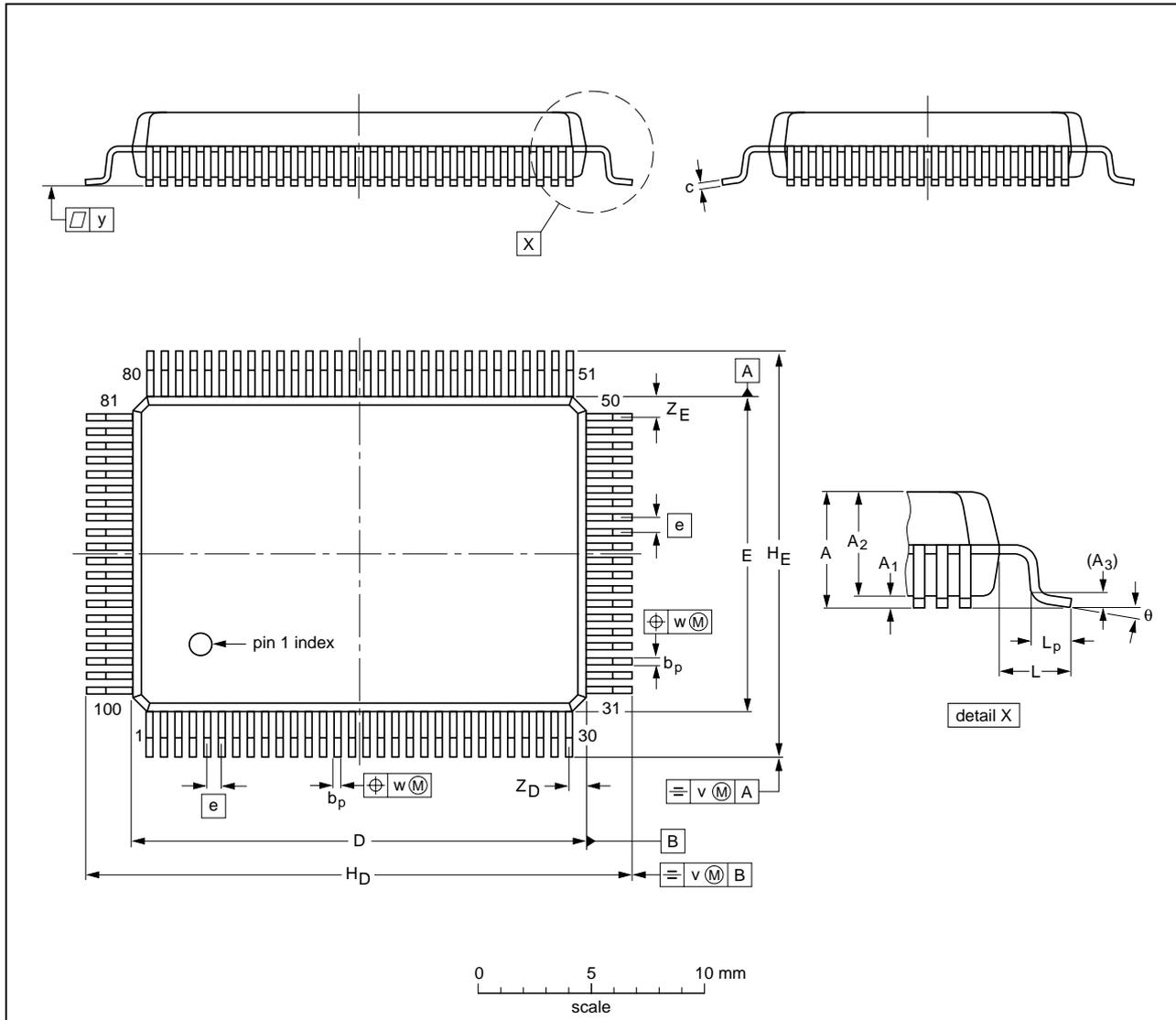
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11 PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm

SOT317-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT317-2		MO-112				99-12-27 03-02-25

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### 12 SOLDERING

#### 12.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### 12.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

#### 12.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### 12.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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### 12.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE <sup>(1)</sup>	SOLDERING METHOD	
	WAVE	REFLOW <sup>(2)</sup>
BGA, HTSSON..T <sup>(3)</sup> , LBGA, LFBGA, SQFP, SSOP..T <sup>(3)</sup> , TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>(4)</sup>	suitable
PLCC <sup>(5)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(5)(6)</sup>	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>(7)</sup>	suitable
CWQCCN..L <sup>(8)</sup> , PMFP <sup>(9)</sup> , WQCCN..L <sup>(8)</sup>	not suitable	not suitable

#### Notes

- For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
- These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding  $217\text{ °C} \pm 10\text{ °C}$  measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a  $45^\circ$  angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- Hot bar or manual soldering is suitable for PMFP packages.

### 12.6 Additional soldering information

The package QFP100 (lead-free; SOT317GC11, subpackage of the SOT317-2) is granted the Moisture Sensitivity Level (MSL) 3.

Soldering temperature of  $> 215\text{ °C}$  is recommended or RMA flux.

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### 13 DATA SHEET STATUS

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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