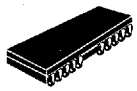
T-46-23-15

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

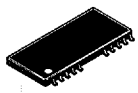
# MCM54402A

*Advance Information*

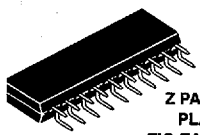
## 4M x 1 CMOS Dynamic RAM
### Static Column



N PACKAGE
300 MIL SOJ
CASE 822-03



T PACKAGE
300 MIL TSOP
CASE 892-01



Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

3

The MCM54402A is a 0.7µ CMOS high-speed dynamic random access memory. It is organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The static column mode feature allows column data to be accessed upon the column address transition when $\overline{RAS}$ and $\overline{CS}$ are held low, similar to static RAM operation.

The MCM54402A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil J-lead small outline package, a 300 mil thin-small-outline package (TSOP), and a 100 mil zig-zag in-line package (ZIP).

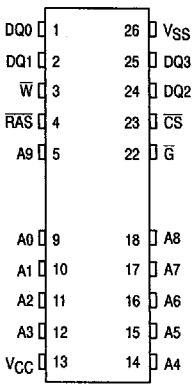
- Three-State Data Output
- Static Column Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM54402A = 16 ms
- Fast Access Time ($t_{RAC}$):
  MCM54402A-60 = 60 ns (Max)
  MCM54402A-70 = 70 ns (Max)
  MCM54402A-80 = 80 ns (Max)
- Low Active Power:
  MCM54402A-60 = 660 mW (Max)
  MCM54402A-70 = 550 mW (Max)
  MCM54402A-80 = 468 mW (Max)
- Low Standby Power Dissipation:
  MCM54402A = 11 mW (Max, TTL Levels)
  = 5.5 mW (Max, CMOS Levels)

**PIN NAMES**

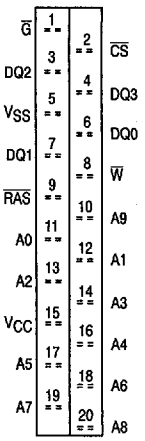
| | |
|---|---|
| A0 – A9 | Address Input |
| DQ0 – DQ3 | Data Input |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | Read/Write Input |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CS}$ | Chip Select |
| $V_{CC}$ | Power Supply (+ 5 V) |
| $V_{SS}$ | Ground |

**PIN ASSIGNMENTS**

**300 MIL SOJ/TSOP**

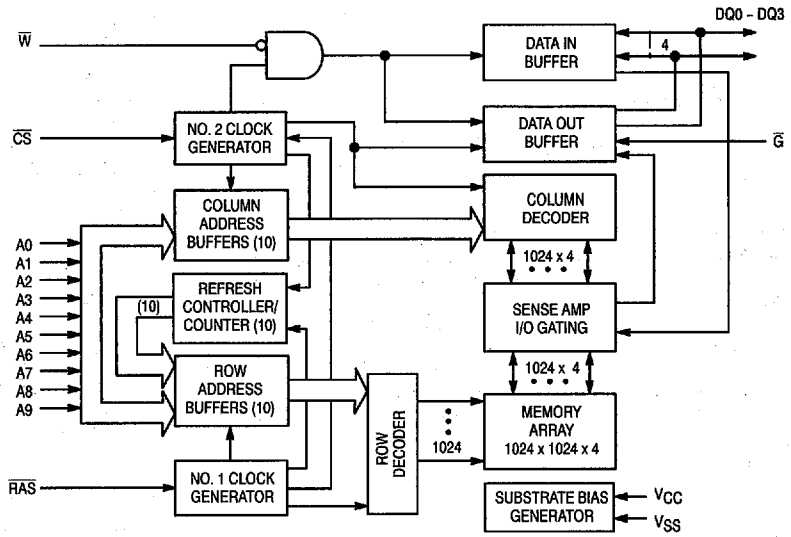



**100 MIL ZIP**




This document contains information on a new product. Specifications and information herein are subject to change without notice.

## BLOCK DIAGRAM




**ABSOLUTE MAXIMUM RATINGS** (See Note)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | – 1 to + 7 | V |
| Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$ | $V_{in}$, $V_{out}$ | – 1 to + 7 | V |
| Data Out Current | $I_{out}$ | 50 | mA |
| Power Dissipation | $P_D$ | 700 | mW |
| Operating Temperature Range | $T_A$ | 0 to + 70 | °C |
| Storage Temperature Range | $T_{stg}$ | – 55 to + 150 | °C |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 10%, $T_A$ = 0 to + 70°C, Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS** (All voltages referenced to $V_{SS}$)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage (Operating Voltage Range) | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$ | 0 | 0 | 0 | |
| Logic High Voltage, All Inputs | $V_{IH}$ | 2.4 | — | 6.5 | V |
| Logic Low Voltage, All Inputs | $V_{IL}$ | – 1.0 | — | 0.8 | V |

**DC CHARACTERISTICS AND SUPPLY CURRENTS**

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $V_{CC}$ Power Supply Current<br>MCM54402A-60, $t_{RC}$ = 110 ns<br>MCM54402A-70, $t_{RC}$ = 130 ns<br>MCM54402A-80, $t_{RC}$ = 150 ns | $I_{CC1}$ | —<br>—<br>— | 120<br>100<br>85 | mA | 1, 2 |
| $V_{CC}$ Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = $V_{IH}$) | $I_{CC2}$ | — | 2.0 | mA | |
| $V_{CC}$ Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CS}$ = $V_{IH}$)<br>MCM54402A-60, $t_{RC}$ = 110 ns<br>MCM54402A-70, $t_{RC}$ = 130 ns<br>MCM54402A-80, $t_{RC}$ = 150 ns | $I_{CC3}$ | <br>—<br>—<br>— | <br>120<br>100<br>85 | mA | 1, 2 |
| $V_{CC}$ Power Supply Current During Static Column Mode Cycle ($\overline{RAS}$ = $\overline{CS}$ = $V_{IL}$)<br>MCM54402A-60, $t_{SC}$ = 35 ns<br>MCM54402A-70, $t_{SC}$ = 40 ns<br>MCM54402A-80, $t_{SC}$ = 45 ns | $I_{CC4}$ | <br>—<br>—<br>— | <br>95<br>85<br>75 | mA | 1, 2 |
| $V_{CC}$ Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = $V_{CC}$ – 0.2 V) | $I_{CC5}$ | — | 1.0 | mA | |
| $V_{CC}$ Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle<br>MCM54402A-60, $t_{RC}$ = 110 ns<br>MCM54402A-70, $t_{RC}$ = 130 ns<br>MCM54402A-80, $t_{RC}$ = 150 ns | $I_{CC6}$ | <br>—<br>—<br>— | <br>120<br>100<br>85 | mA | 1 |
| Input Leakage Current (0 V ≤ $V_{in}$ ≤ 6.5 V) | $I_{lkg(I)}$ | – 10 | 10 | µA | |
| Output Leakage Current ($\overline{CS}$ = $V_{IH}$, 0 V ≤ $V_{out}$ ≤ 5.5 V) | $I_{lkg(O)}$ | – 10 | 10 | µA | |
| Output High Voltage ($I_{OH}$ = – 5 mA) | $V_{OH}$ | 2.4 | — | V | |
| Output Low Voltage ($I_{OL}$ = 4.2 mA) | $V_{OL}$ | — | 0.4 | V | |

NOTES:
1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = $V_{IL}$ and $\overline{CS}$ = $V_{IH}$.

**CAPACITANCE** (f = 1.0 MHz, $T_A$ = 25°C, $V_{CC}$ = 5 V, Periodically Sampled Rather Than 100% Tested)

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Input Capacitance A0 – A9 | $C_{in}$ | 5 | pF |
| Input Capacitance $\overline{G}$, $\overline{RAS}$, $\overline{CS}$, $\overline{W}$ | | 7 | |
| I/O Capacitance ($\overline{CS}$ = $V_{IH}$ to Disable Output) DQ0 – DQ3 | $C_{out}$ | 7 | pF |

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

## AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 10%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

**READ, WRITE, AND READ-WRITE CYCLES** (See Notes 1, 2, 3, and 4)

| Parameter | Symbol | | MCM54402A-60 | | MCM54402A-70 | | MCM54402A-80 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | Min | Max | | |
| Random Read or Write Cycle Time | $t_{RELREL}$ | $t_{RC}$ | 110 | — | 130 | — | 150 | — | ns | 5 |
| Read-Write Cycle Time | $t_{RELREL}$ | $t_{RWC}$ | 165 | — | 185 | — | 205 | — | ns | 5 |
| Static Column Mode Cycle Time | $t_{AVAV}$ | $t_{SC}$ | 35 | — | 40 | — | 45 | — | ns | |
| Static Column Mode Read-Write Cycle Time | $t_{AVAV}$ | $t_{SRWC}$ | 90 | — | 100 | — | 110 | — | ns | |
| Access Time from $\overline{RAS}$ | $t_{RELQV}$ | $t_{RAC}$ | — | 60 | — | 70 | — | 80 | ns | 6, 7 |
| Access Time from $\overline{CS}$ | $t_{CELQV}$ | $t_{CAC}$ | — | 20 | — | 20 | — | 20 | ns | 6, 8 |
| Access Time from Column Address | $t_{AVQV}$ | $t_{AA}$ | — | 30 | — | 35 | — | 40 | ns | 6, 9 |
| Access Time from Last Write | $t_{WLQV}$ | $t_{ALW}$ | — | 55 | — | 65 | — | 75 | ns | 6, 10 |
| $\overline{CS}$ to Output in Low-Z | $t_{CELQX}$ | $t_{CLZ}$ | 0 | — | 0 | — | 0 | — | ns | 6 |
| Output Buffer and Turn-Off Delay | $t_{CEHQZ}$ | $t_{OFF}$ | 0 | 20 | 0 | 20 | 0 | 20 | ns | 11 |
| Data Out Hold from Address Change | $t_{AXQX}$ | $t_{AOH}$ | 5 | — | 5 | — | 5 | — | ns | |
| Data Out Enable from Write | $t_{WHQV}$ | $t_{OW}$ | — | 20 | — | 20 | — | 20 | ns | |
| Transition Time (Rise and Fall) | $t_T$ | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | |
| $\overline{RAS}$ Precharge Time | $t_{REHREL}$ | $t_{RP}$ | 40 | — | 50 | — | 60 | — | ns | |
| $\overline{RAS}$ Pulse Width | $t_{RELREH}$ | $t_{RAS}$ | 60 | 10 k | 70 | 10 k | 80 | 10 k | ns | |
| $\overline{RAS}$ Pulse Width (Static Column Mode) | $t_{RELREH}$ | $t_{RASC}$ | 60 | 200 k | 70 | 200 k | 80 | 200 k | ns | |
| $\overline{RAS}$ Hold Time | $t_{CELREH}$ | $t_{RSH}$ | 20 | — | 20 | — | 20 | — | ns | |
| $\overline{CS}$ Hold Time | $t_{RELCEH}$ | $t_{CSH}$ | 60 | — | 70 | — | 80 | — | ns | |
| $\overline{CS}$ Pulse Width | $t_{CELCEH}$ | $t_{CS}$ | 20 | 10 k | 20 | 10 k | 20 | 10 k | ns | |
| $\overline{CS}$ Pulse Width (Static Column Mode) | $t_{CELCEH}$ | $t_{CSC}$ | 20 | 200 k | 20 | 200 k | 20 | 200 k | ns | |
| $\overline{RAS}$ to $\overline{CS}$ Delay Time | $t_{RELCEL}$ | $t_{RCD}$ | 20 | 40 | 20 | 50 | 20 | 60 | ns | 12 |
| $\overline{RAS}$ to Column Address Delay Time | $t_{RELAV}$ | $t_{RAD}$ | 15 | 30 | 15 | 35 | 15 | 40 | ns | 13 |
| $\overline{CS}$ to $\overline{RAS}$ Precharge Time | $t_{CEHREL}$ | $t_{CRP}$ | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{CS}$ Precharge Time | $t_{CEHCEL}$ | $t_{CP}$ | 10 | — | 10 | — | 10 | — | ns | |
| Row Address Setup Time | $t_{AVREL}$ | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | ns | |
| Row Address Hold Time | $t_{RELAX}$ | $t_{RAH}$ | 10 | — | 10 | — | 10 | — | ns | |

NOTES: (continued)

1. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
4. AC measurements $t_T$ = 5.0 ns.
5. The specifications for $t_{RC}$ (min) and $t_{RWC}$ (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ $T_A$ ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at $V_{OH}$ = 2.0 V and $V_{OL}$ = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. Assumes that $t_{LWAD} \geq t_{LWAD}$ (max).
11. $t_{OFF}$ (max) and/or $t_{GZ}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the $t_{RCD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
13. Operation within the $t_{RAD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RAD}$ (max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max), then access time is controlled exclusively by $t_{AA}$.

**READ, WRITE, AND READ-WRITE CYCLES** (Continued)

| Parameter | Symbol | | MCM54402A-60 | | MCM54402A-70 | | MCM54402A-80 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | Min | Max | | |
| Column Address Setup Time | $t_{AVCEL}$ | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | ns | |
| Column Address Hold Time | $t_{CELAX}$ | $t_{CAH}$ | 15 | — | 15 | — | 15 | — | ns | |
| Column Address Hold Time Referenced to $\overline{RAS}$ (Read Cycle) | $t_{RELAX}$ | $t_{AR}$ | 70 | — | 80 | — | 90 | — | ns | |
| Column Address to $\overline{RAS}$ Lead Time | $t_{AVREH}$ | $t_{RAL}$ | 30 | — | 35 | — | 40 | — | ns | |
| Column Address Hold Time Reference to $\overline{RAS}$ High | $t_{REHAX}$ | $t_{AH}$ | 5 | — | 5 | — | 5 | — | ns | 14 |
| Last Write to Column Address Delay Time | $t_{WLAV}$ | $t_{LWAD}$ | 20 | 25 | 20 | 30 | 20 | 35 | ns | 15 |
| Last Write to Column Address Hold Time | $t_{WLAX}$ | $t_{AHLW}$ | 55 | — | 65 | — | 75 | — | ns | |
| Read Command Setup Time | $t_{WHCEL}$ | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time Referenced to $\overline{CS}$ | $t_{CEHWX}$ | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | ns | 16 |
| Read Command Hold Time Referenced to $\overline{RAS}$ | $t_{REHWX}$ | $t_{RRH}$ | 0 | — | 0 | — | 0 | — | ns | 16 |
| Write Command Hold Time Referenced to $\overline{CS}$ | $t_{CELWH}$ | $t_{WCH}$ | 10 | — | 15 | — | 15 | — | ns | |
| Write Command Pulse Width | $t_{WLWH}$ | $t_{WP}$ | 10 | — | 15 | — | 15 | — | ns | |
| Write Command Inactive Time | $t_{WHWL}$ | $t_{WI}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write Command to $\overline{RAS}$ Lead Time | $t_{WLREH}$ | $t_{RWL}$ | 20 | — | 20 | — | 20 | — | ns | |
| Write Command to $\overline{CS}$ Lead Time | $t_{WLCEH}$ | $t_{CWL}$ | 20 | — | 20 | — | 20 | — | ns | |
| Data in Setup Time | $t_{DVCEL}$ | $t_{DS}$ | 0 | — | 0 | — | 0 | — | ns | 17 |
| Data in Hold Time | $t_{CELDX}$ | $t_{DH}$ | 15 | — | 15 | — | 15 | — | ns | 17 |
| Refresh Period | $t_{RVRV}$ | $t_{RFSH}$ | — | 16 | — | 16 | — | 16 | ms | |
| Write Command Setup Time | $t_{WLCEL}$ | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | ns | 18 |
| $\overline{CS}$ to Write Delay | $t_{CELWL}$ | $t_{CWD}$ | 50 | — | 50 | — | 50 | — | ns | 18 |
| $\overline{RAS}$ to Write Delay | $t_{RELWL}$ | $t_{RWD}$ | 90 | — | 100 | — | 110 | — | ns | 18 |
| Column Address to Write Delay Time | $t_{AVWL}$ | $t_{AWD}$ | 60 | — | 65 | — | 70 | — | ns | 18 |
| $\overline{CS}$ Setup Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh | $t_{RELCEL}$ | $t_{CSR}$ | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{CS}$ Hold Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh | $t_{RELCEH}$ | $t_{CHR}$ | 15 | — | 15 | — | 15 | — | ns | |
| $\overline{RAS}$ Precharge to $\overline{CS}$ Active Time | $t_{REHCEL}$ | $t_{RPC}$ | 0 | — | 0 | — | 0 | — | ns | |
| $\overline{CS}$ Precharge Time for $\overline{CS}$ Before $\overline{RAS}$ Counter Test | $t_{CEHCEL}$ | $t_{CPT}$ | 30 | — | 40 | — | 40 | — | ns | |
| $\overline{RAS}$ Hold Time Referenced to $\overline{G}$ | $t_{GLREH}$ | $t_{ROH}$ | 10 | — | 10 | — | 10 | — | ns | |

NOTES: (continued)

14. $t_{AH}$ must be met for a read cycle.
15. Operation within the $t_{LWAD}$ (max) limit ensures that $t_{ALW}$ can be met. $t_{LWAD}$ (max) is specified as a reference point only; if $t_{LWAD}$ is greater than the specified $t_{LWAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.
16. Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a read cycle.
17. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in read-write cycles.
18. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$, and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

**READ, WRITE, AND READ-WRITE CYCLES** (Continued)

| Parameter | Symbol | | MCM54402A-60 | | MCM54402A-70 | | MCM54402A-80 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | Min | Max | | |
| $\overline{G}$ Access Time | $t_{GLQV}$ | $t_{GA}$ | — | 20 | — | 20 | — | 20 | ns | |
| $\overline{G}$ to Data Delay | $t_{GLHDX}$ | $t_{GD}$ | 20 | — | 20 | — | 20 | — | ns | |
| Output Buffer Turn-Off Delay Time from $\overline{G}$ | $t_{GHQZ}$ | $t_{GZ}$ | 0 | 20 | 0 | 20 | 0 | 20 | ns | 11 |
| $\overline{G}$ Command Hold Time | $t_{WLGL}$ | $t_{GH}$ | 20 | — | 20 | — | 20 | — | ns | |
| Write Command Setup Time (Test Mode) | $t_{WLREL}$ | $t_{WTS}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write Command Hold Time (Test Mode) | $t_{RELWH}$ | $t_{WTH}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write to $\overline{RAS}$ Precharge Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh) | $t_{WHREL}$ | $t_{WRP}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write to $\overline{RAS}$ Hold Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh) | $t_{RELWL}$ | $t_{WRH}$ | 10 | — | 10 | — | 10 | — | ns | |

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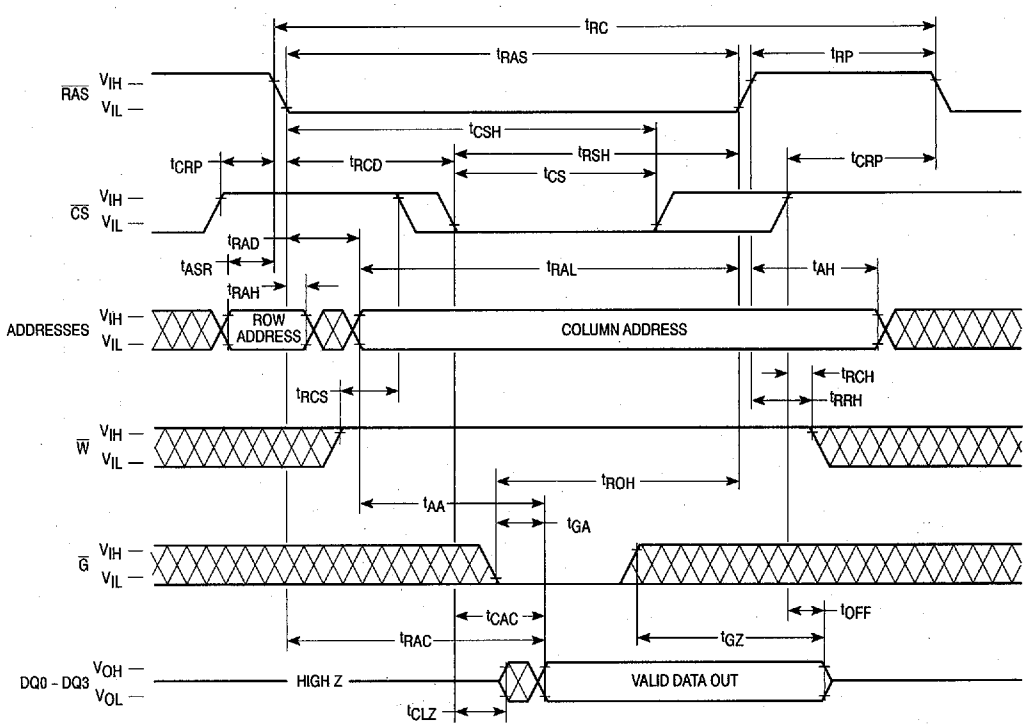
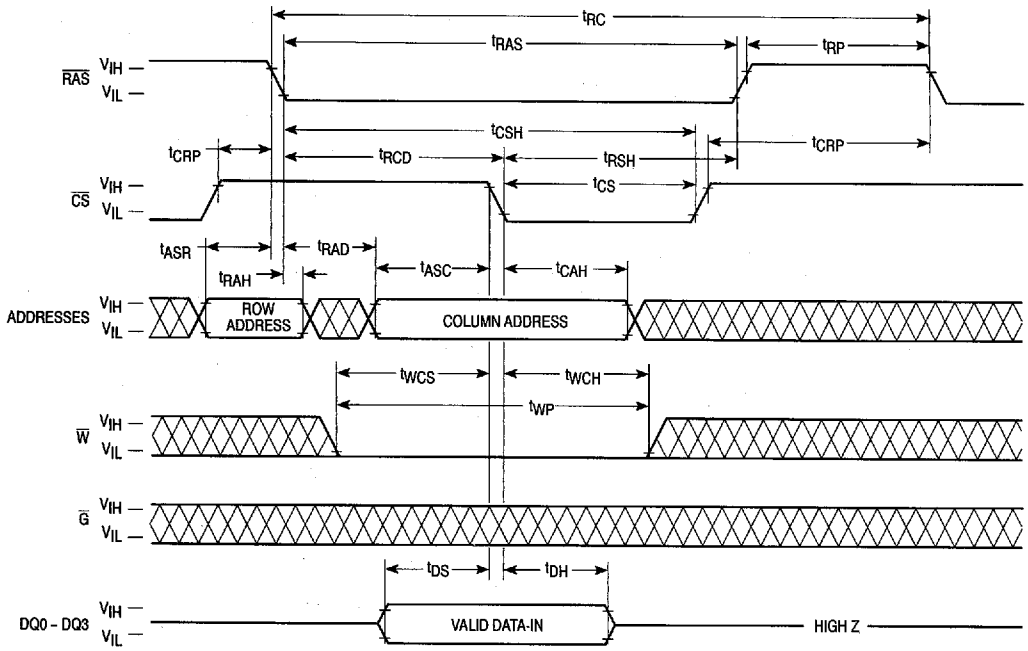
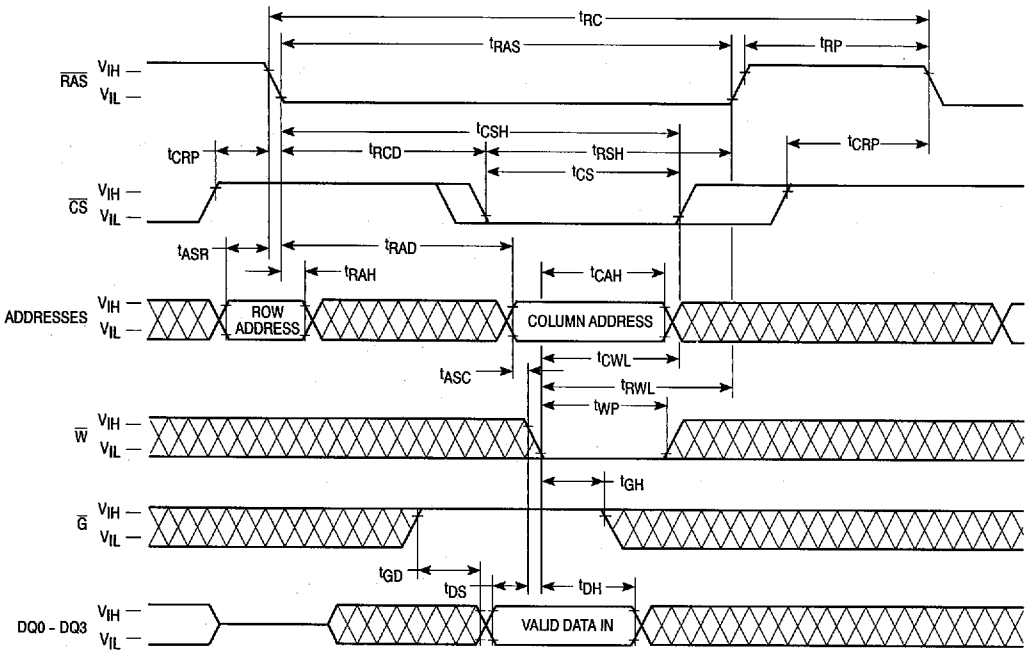
**READ CYCLE**



## EARLY WRITE CYCLE




## G CONTROLLED LATE WRITE CYCLE



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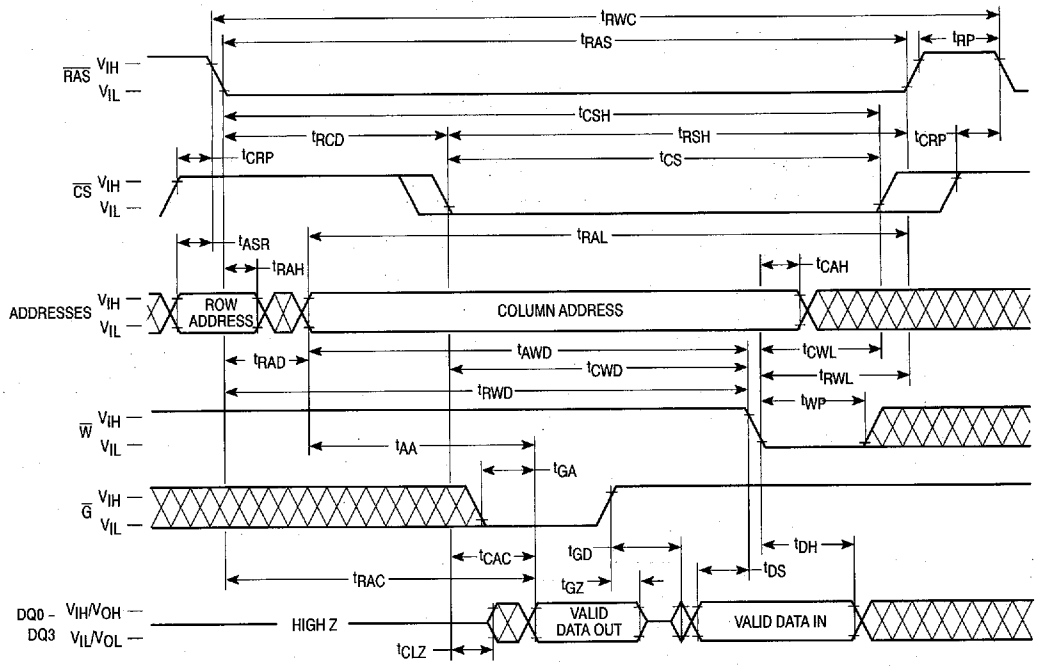
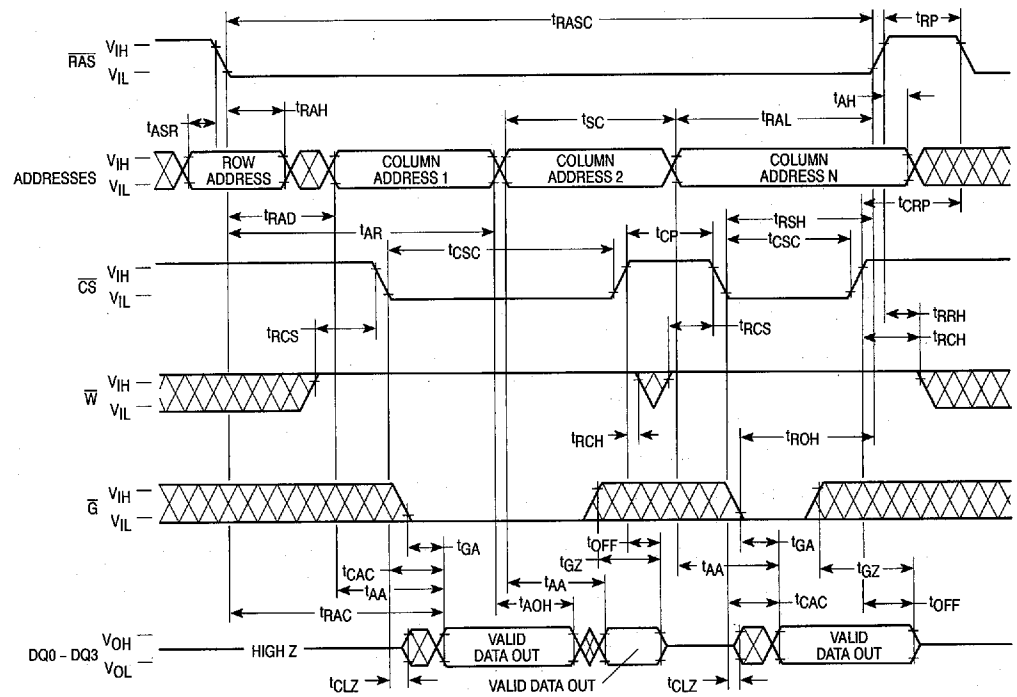
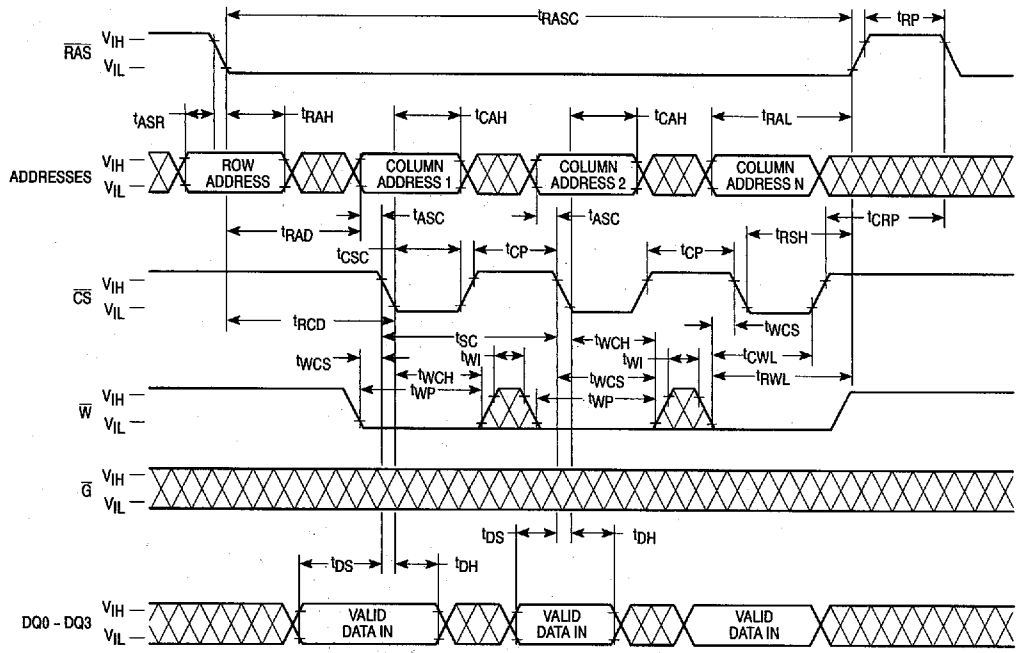
## READ-WRITE CYCLE



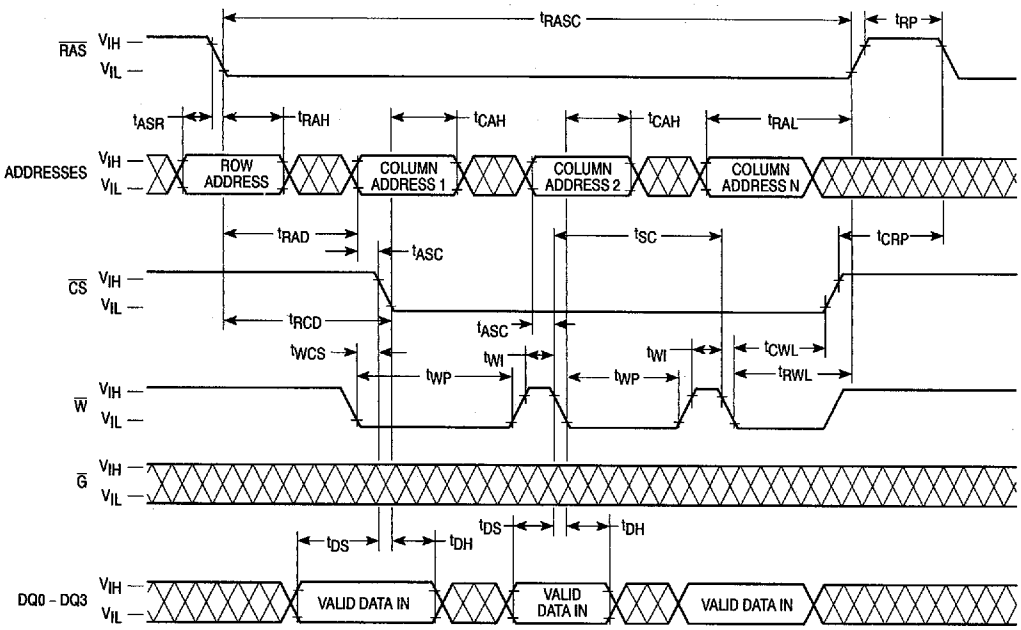

## STATIC COLUMN MODE READ CYCLE



## STATIC COLUMN MODE EARLY WRITE CYCLE (A)




## STATIC COLUMN MODE EARLY WRITE CYCLE (B)



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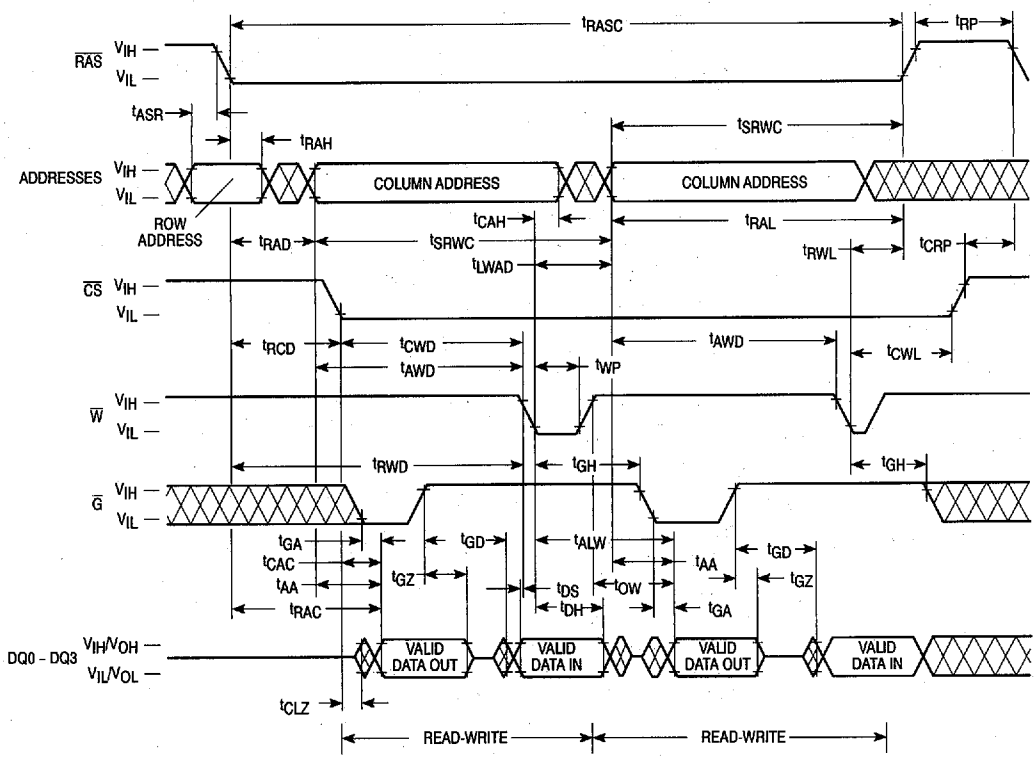
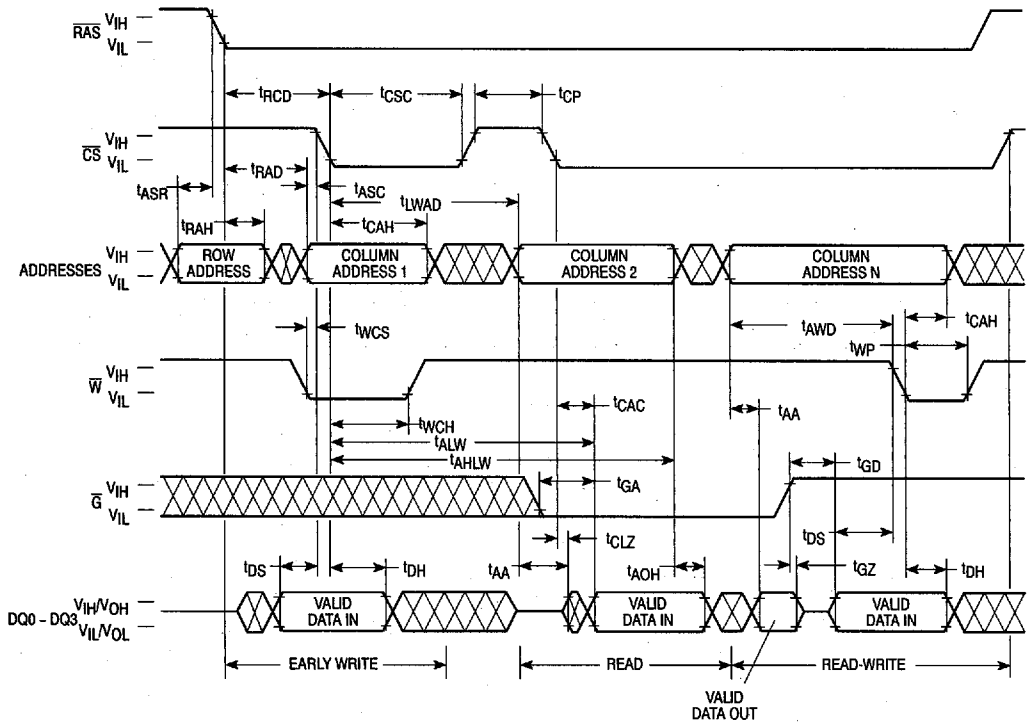
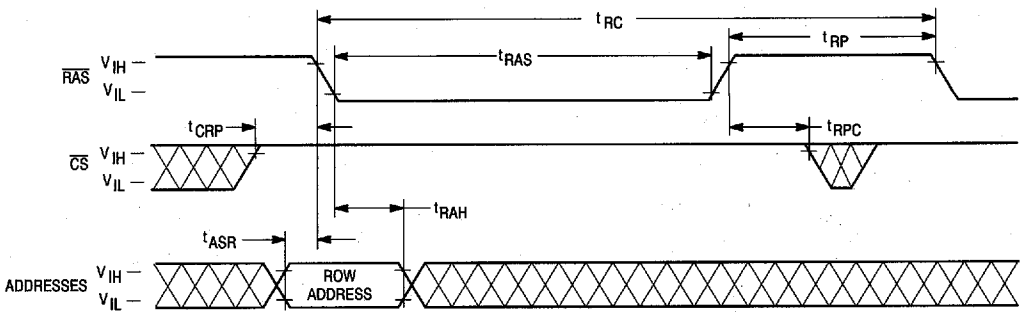
## STATIC COLUMN MODE READ-WRITE CYCLE



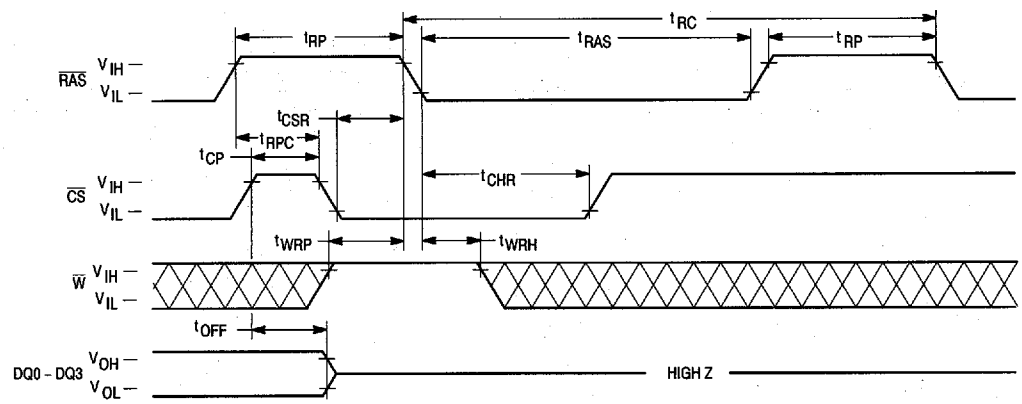
## STATIC COLUMN MODE READ/WRITE MIXED CYCLE



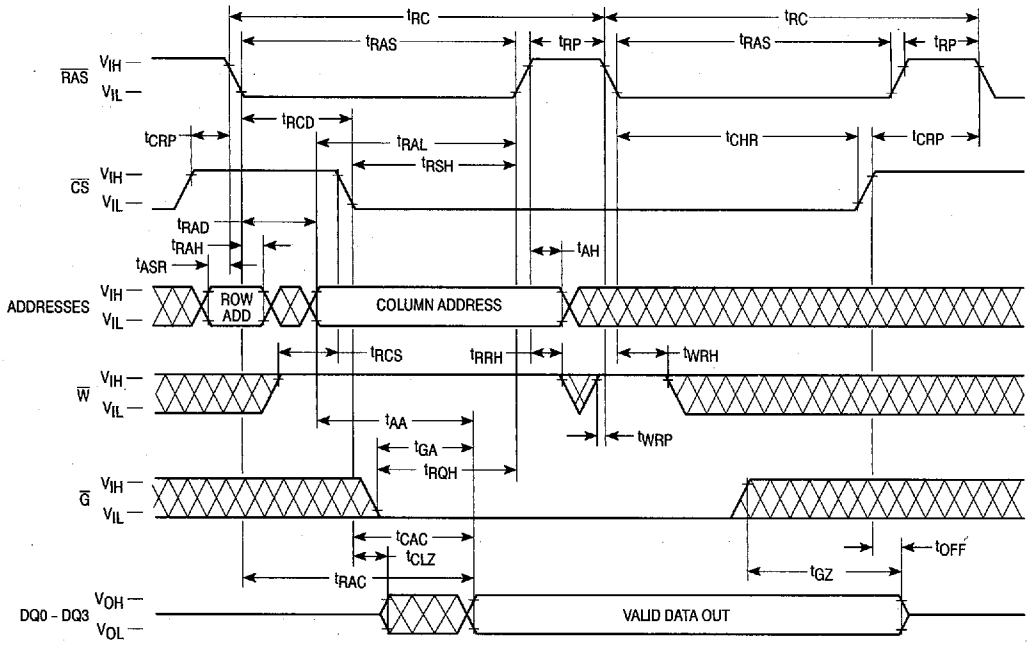
## $\overline{RAS}$-ONLY REFRESH CYCLE
($\overline{W}$ and $\overline{G}$ are Don't Care)



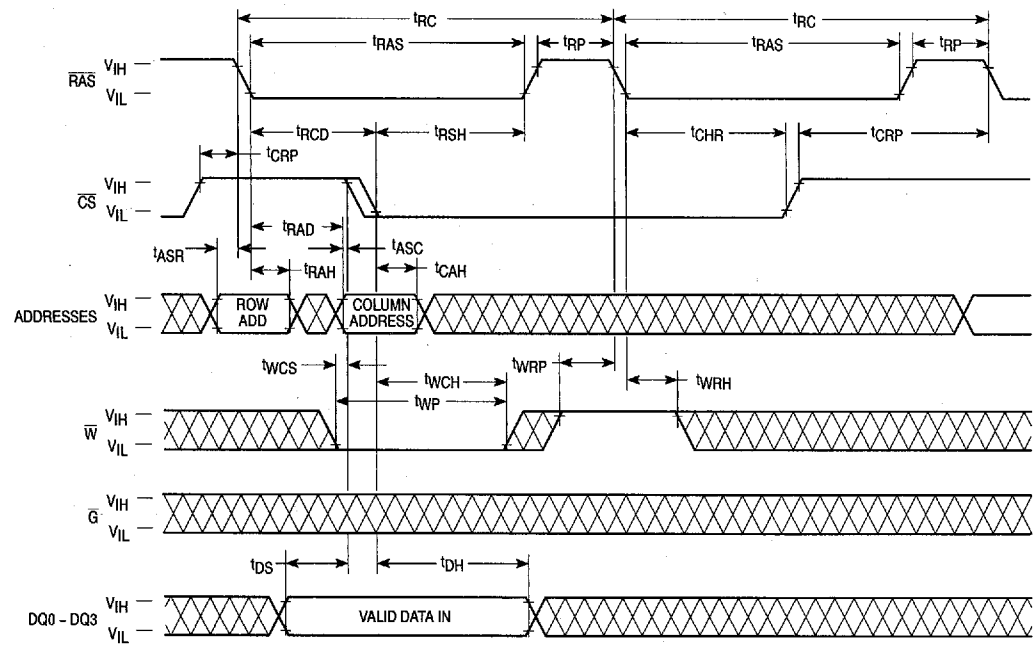

## $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{G}$ and A0 – A9 are Don't Care)



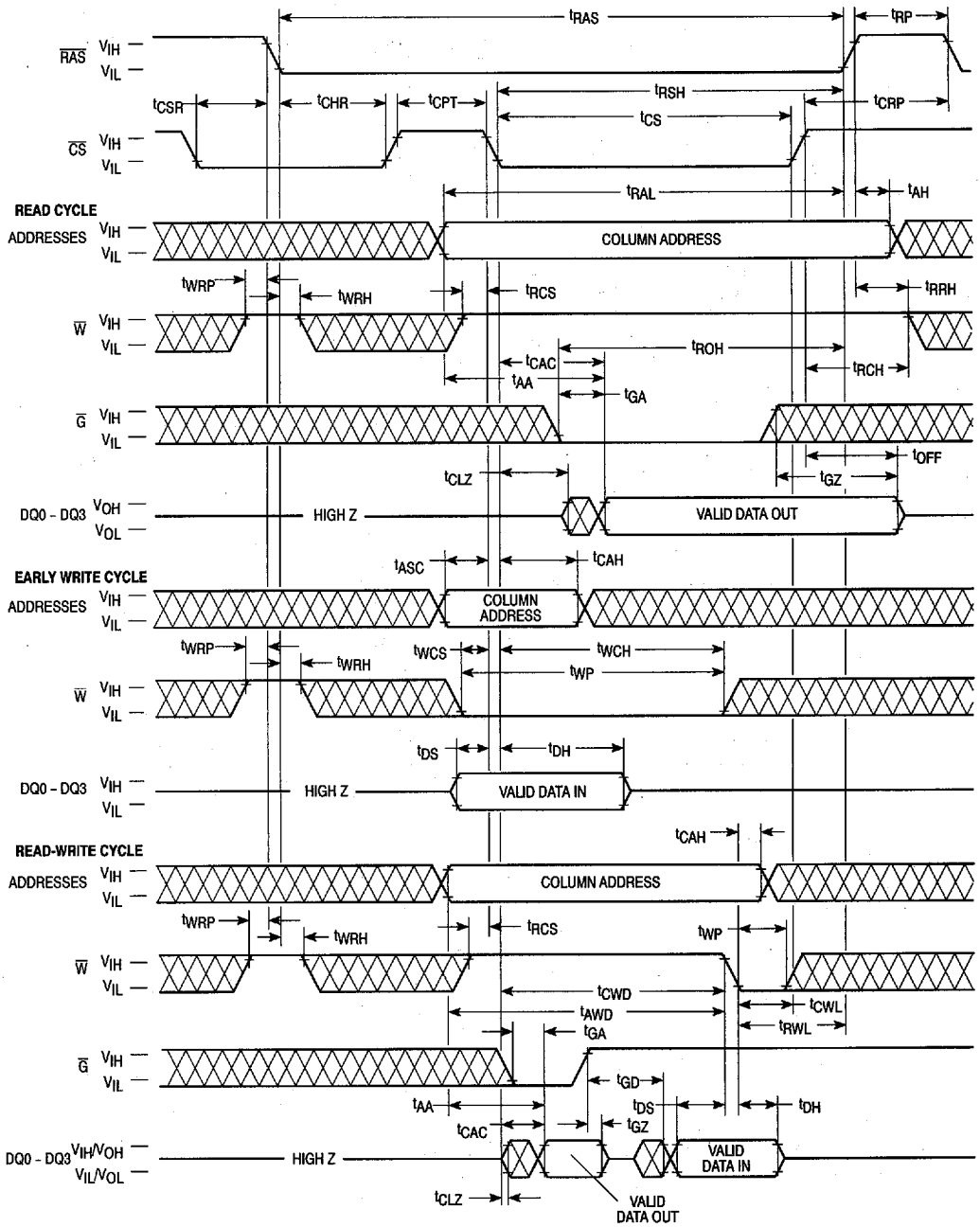
## HIDDEN REFRESH CYCLE (READ)




## HIDDEN REFRESH CYCLE (EARLY WRITE)



## $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



### DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

### ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by the row address strobe ($\overline{RAS}$) clock, into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{RAS}$ active transition latches the row address field. Column addresses are not latched, hence the "static column" designation of this device. Chip select ($\overline{CS}$) active transition (active = $V_{IL}$, $t_{RCD}$ minimum) follows $\overline{RAS}$ on all read, write, or read-write cycles and is independent of column address. The static column feature allows greater flexibility in setting up the external column addresses into the RAM.

There are three other variations in addressing the 1M x 4 RAM: **$\overline{RAS}$-only refresh cycle, $\overline{CS}$ before $\overline{RAS}$ refresh cycle,** and **Static Column mode**. All three are discussed in separate sections that follow.

### READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, static column mode read cycle, read-write cycle, and static column mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ active transition latching the desired row. The write ($\overline{W}$) input level must be high ($V_{IH}$), $t_{RCS}$ (minimum) before the $\overline{CS}$ active transition, to enable read mode. A valid column address can be provided at any time ($t_{RAD}$ minimum), independent of the $\overline{CS}$ active transition.

Both the $\overline{RAS}$ and $\overline{CS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{CS}$ and output enable ($\overline{G}$) control read access time; $\overline{CS}$ and $\overline{G}$ must be active (and column address must be valid) by $t_{RCD}$ maximum, and $t_{RAC} - t_{GA}$ minimum, respectively, to guarantee valid data out (Q) at $t_{RAC}$ (access time from $\overline{RAS}$ active transition). If the $t_{RCD}$ maximum is exceeded and/or $\overline{G}$ active transition does not occur in time, read access time is determined by either the $\overline{CS}$ or $\overline{G}$ clock active transition ($t_{CAC}$ or $t_{GA}$).

The $\overline{RAS}$ and $\overline{CS}$ clocks must remain active for minimum times of $t_{RAS}$ and $t_{CS}$, respectively, to complete the read cycle. The column address must remain valid for $t_{AH}$ after $\overline{RAS}$ inactive transition to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time $t_{RRH}$ or $t_{RCH}$ after $\overline{RAS}$ or $\overline{CS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of $t_{RP}$ to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CS}$ and $\overline{G}$ clocks are active. When either the $\overline{CS}$ or $\overline{G}$ clock transitions to inactive, the output will switch to High Z (three-state) $t_{OFF}$ or $t_{GZ}$ after the inactive transition.

### WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, static column mode early write, and static column mode read-write. Early and late write modes are discussed here, while static column mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM.** Write mode is enabled by the transition of $\overline{W}$ to active ($V_{IL}$). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CS}$ leading edge. Minimum active time $t_{RAS}$ and $t_{CS}$, and precharge time $t_{RP}$ apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time $t_{WCS}$ before $\overline{CS}$ active transition. Column address set up and hold times ($t_{ASC}$, $t_{CAH}$), and data in (D) set up and hold times ($t_{DS}$, $t_{DH}$) are referenced to $\overline{CS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CS}$ clocks must stay active for $t_{RWL}$ and $t_{CWL}$, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CS}$ active transition, keeping data-out buffers and $\overline{G}$ disabled.

A late write cycle (referred to as $\overline{G}$-controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T$) $\leq t_{RAS}$, if other timing minimums ($t_{RCD}$, $t_{RWL}$, and $t_T$) are maintained. Column address and D timing parameters are referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CS}$ active transition but Q may be indeterminate — see note 18 of AC Operating Conditions table. Parameters $t_{RWL}$ and $t_{CWL}$ also apply to late write cycles.

### READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for $t_{CWD}$ and/or $t_{AWD}$ minimum, to guarantee valid Q before writing the bit.

### STATIC COLUMN MODE CYCLES

Static column mode refers to multiple successive data operations performed at any or all 1024 column locations on the selected row of the 1M x 4 dynamic RAM during one $\overline{RAS}$ cycle. Read access time of multiple operations ($t_{AA}$ or $t_{CAC}$) is considerably faster than the regular $\overline{RAS}$ clock access time $t_{RAC}$. Multiple operations can be performed simply by keeping $\overline{RAS}$ active. $\overline{CS}$ may be toggled between active and inactive states at any time within the $\overline{RAS}$ cycle.

Once the timing requirements for the initial read, write, or read-write cycle are met and $\overline{RAS}$ remains low, the device is ready for the next operation. Operations can be intermixed in any order, at any column address, subject to normal operating conditions previously described. Every write operation must be clocked with either $\overline{CS}$ or $\overline{W}$, as indicated in **static column mode early write cycle** timing diagrams **A** and **B**.

Column address and D timing parameters are referenced to the signal clocking the write operation. $\overline{CS}$ must be toggled inactive ($t_{CP}$) to perform a read operation after an early write operation (to turn output on), as indicated in **static column mode read/write mixed cycle** timing diagram. The maximum number of consecutive operations is limited to $t_{RASC}$. The cycle ends when $\overline{RAS}$ transitions to inactive.

### REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54402A require refresh every 16 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54402A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54402A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh, $\overline{CS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

### $\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CS}$ remains high ($V_{IH}$) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

### $\overline{CS}$ Before $\overline{RAS}$ Refresh

$\overline{CS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle.

The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{W}$ must be inactive for time $t_{WRP}$ before and time $t_{WRH}$ after $\overline{RAS}$ active transition to prevent switching the device into **test mode**.

### Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CS}$ active the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for $t_{RP}$ and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1). $\overline{W}$ is subject to the same conditions with respect to $\overline{RAS}$ active transition (to prevent test mode) as in $\overline{CS}$ before $\overline{RAS}$ refresh.

### $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{CS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of 8 **$\overline{CS}$ before $\overline{RAS}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 1024 times.
5. Read "0" which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

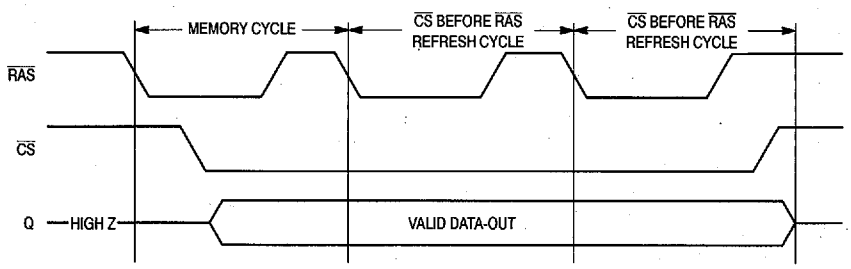



**Figure 1. Hidden Refresh Cycle**

## TEST MODE

The internal organization of this device (512 x 8) allows it to be tested as if it were a 512K x 4 DRAM. Nineteen of the twenty addresses are used when operating the device in test mode. Column address A0 is ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of the device. See the following truth table and test mode block diagram.

$\overline{W}$, $\overline{CS}$ before $\overline{RAS}$ timing puts the device in **Test Mode**, as shown in the test mode timing diagram. A **$\overline{CS}$ before $\overline{RAS}$ refresh cycle** or a **$\overline{RAS}$-only refresh cycle** puts the device back in normal mode. Refresh is performed in test mode by using a **$\overline{W}$, $\overline{CS}$ before $\overline{RAS}$ refresh cycle** which uses the internal refresh address counter.

**TEST MODE TRUTH TABLE**

| D | B0, B1 | B2, B3 | B4, B5 | B6, B7 | Q |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |
| — | Any Other | | | | 0 |

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## TEST MODE
## AC OPERATING CONDITIONS AND CHARACTERISTICS

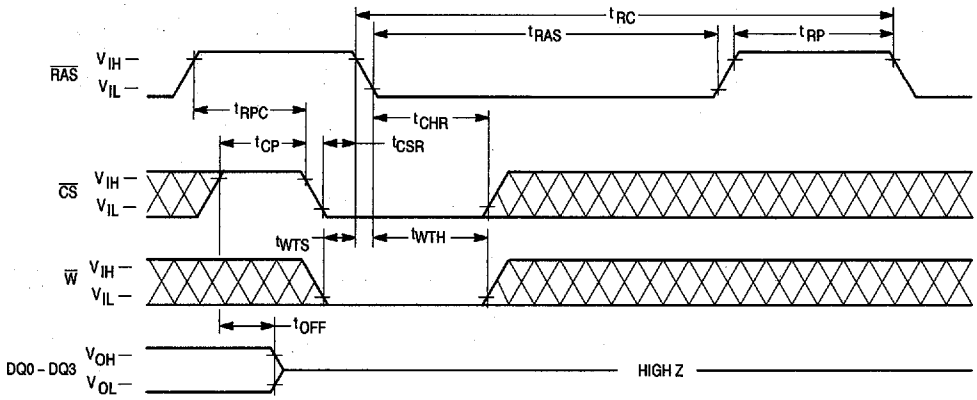
($V_{CC}$ = 5.0 V ± 10%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

**READ, WRITE, AND READ-WRITE CYCLES** (See Notes 1, 2, 3, and 4)

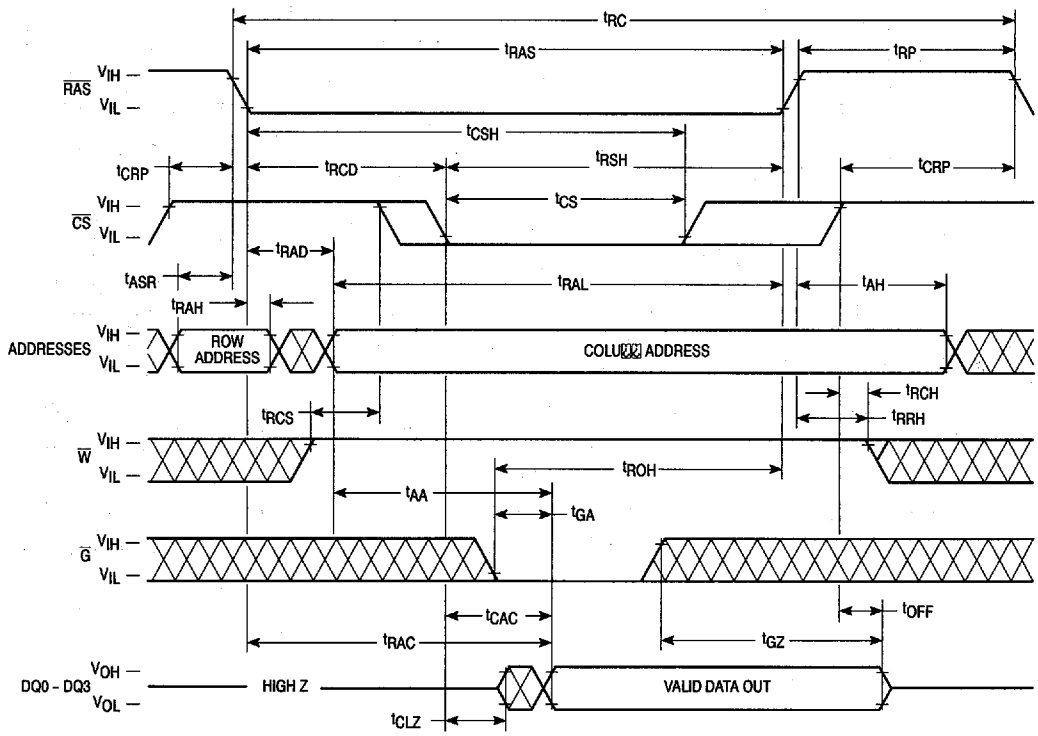
| Parameter | Symbol | | MCM54402A-60 | | MCM54402A-70 | | MCM54402A-80 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | Min | Max | | |
| Random Read or Write Cycle Time | $t_{RELREL}$ | $t_{RC}$ | 115 | — | 135 | — | 155 | — | ns | 5 |
| Static Column Mode Cycle Time | $t_{AVAV}$ | $t_{SC}$ | 40 | — | 45 | — | 50 | — | ns | |
| Access Time from $\overline{RAS}$ | $t_{RELQV}$ | $t_{RAC}$ | — | 65 | — | 75 | — | 85 | ns | 6, 7 |
| Access Time from $\overline{CS}$ | $t_{CELQV}$ | $t_{CAC}$ | — | 25 | — | 25 | — | 25 | ns | 6, 8 |
| Access Time from Column Address | $t_{AVQV}$ | $t_{AA}$ | — | 35 | — | 40 | — | 45 | ns | 6, 9 |
| $\overline{RAS}$ Pulse Width | $t_{RELREH}$ | $t_{RAS}$ | 65 | 10 k | 75 | 10 k | 85 | 10 k | ns | |
| $\overline{RAS}$ Pulse Width (Static Column Mode) | $t_{RELREH}$ | $t_{RASC}$ | 65 | 200 k | 75 | 200 k | 85 | 200 k | ns | |
| $\overline{RAS}$ Hold Time | $t_{CELREH}$ | $t_{RSH}$ | 25 | — | 25 | — | 25 | — | ns | |
| $\overline{CS}$ Hold Time | $t_{RELCEH}$ | $t_{CSH}$ | 65 | — | 75 | — | 85 | — | ns | |
| $\overline{CS}$ Pulse Width | $t_{CELCEH}$ | $t_{CS}$ | 25 | 10 k | 25 | 10 k | 25 | 10 k | ns | |
| $\overline{CS}$ Pulse Width (Static Column Mode) | $t_{CELCEH}$ | $t_{CSC}$ | 25 | 200 k | 25 | 200 k | 25 | 200 k | ns | |
| Column Address to $\overline{RAS}$ Lead Time | $t_{AVREH}$ | $t_{RAL}$ | 35 | — | 40 | — | 45 | — | ns | |

NOTES:
1. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
4. AC measurements $t_T$ = 5.0 ns.
5. The specification for $t_{RC}$ (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ $T_A$ ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at $V_{OH}$ = 2.0 V and $V_{OL}$ = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).

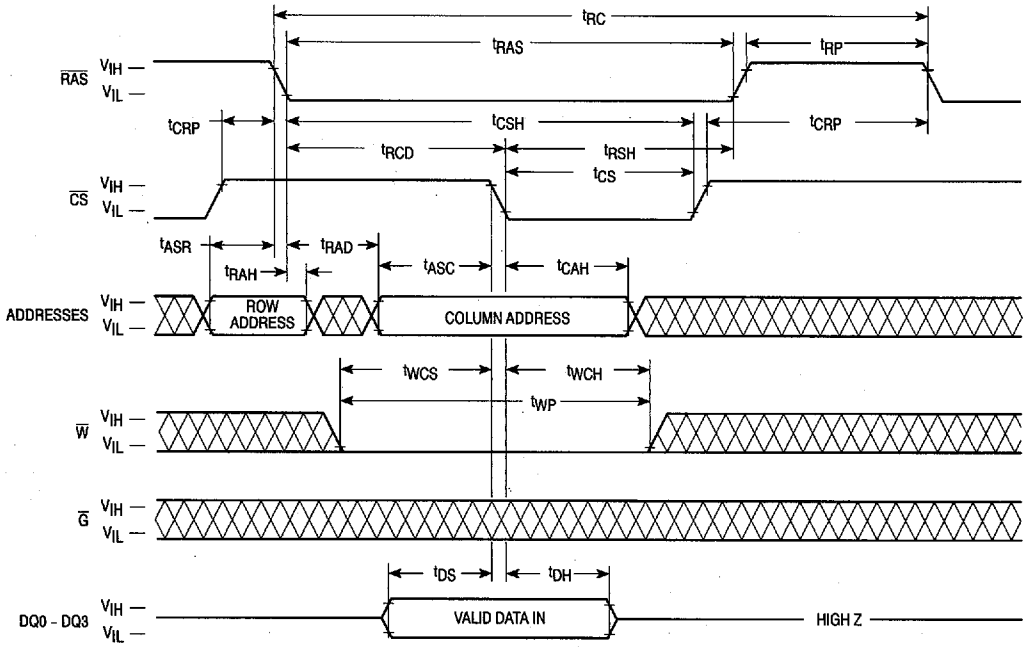
**W, CS BEFORE RAS REFRESH CYCLE (TEST MODE ENTRY)**
**(G and A0 – A9 are Don't Care)**



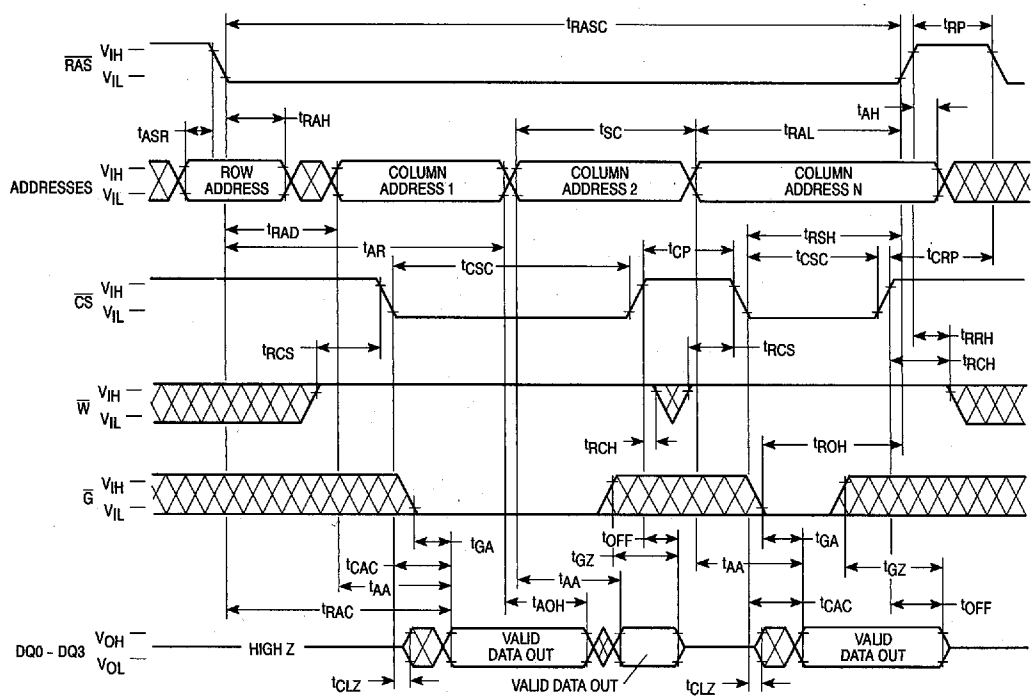

**TEST MODE — READ CYCLE**



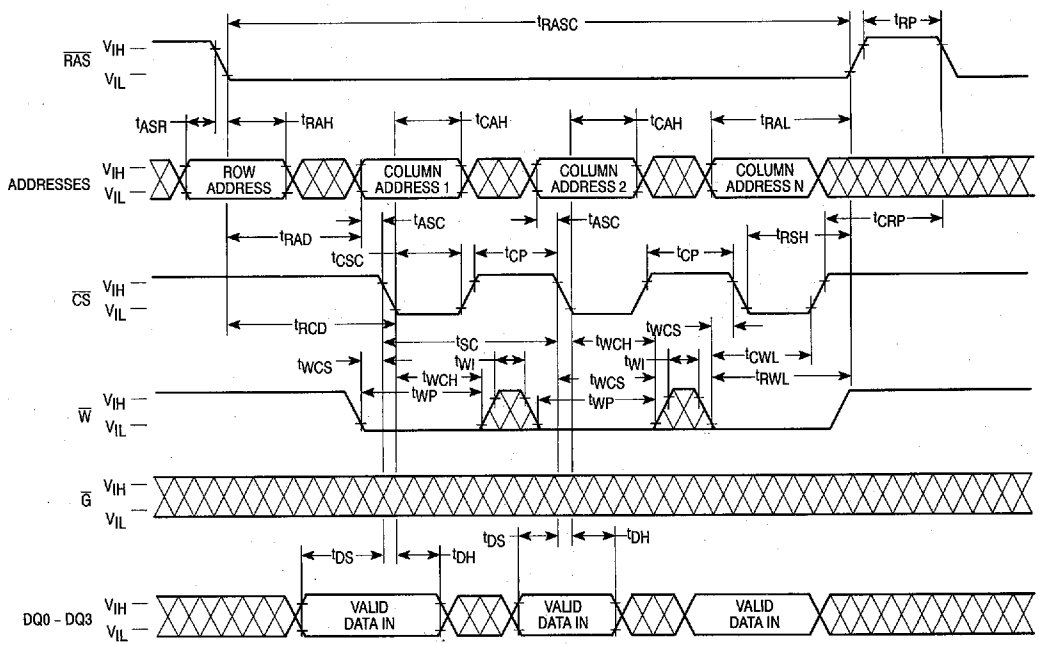
## TEST MODE — EARLY WRITE CYCLE



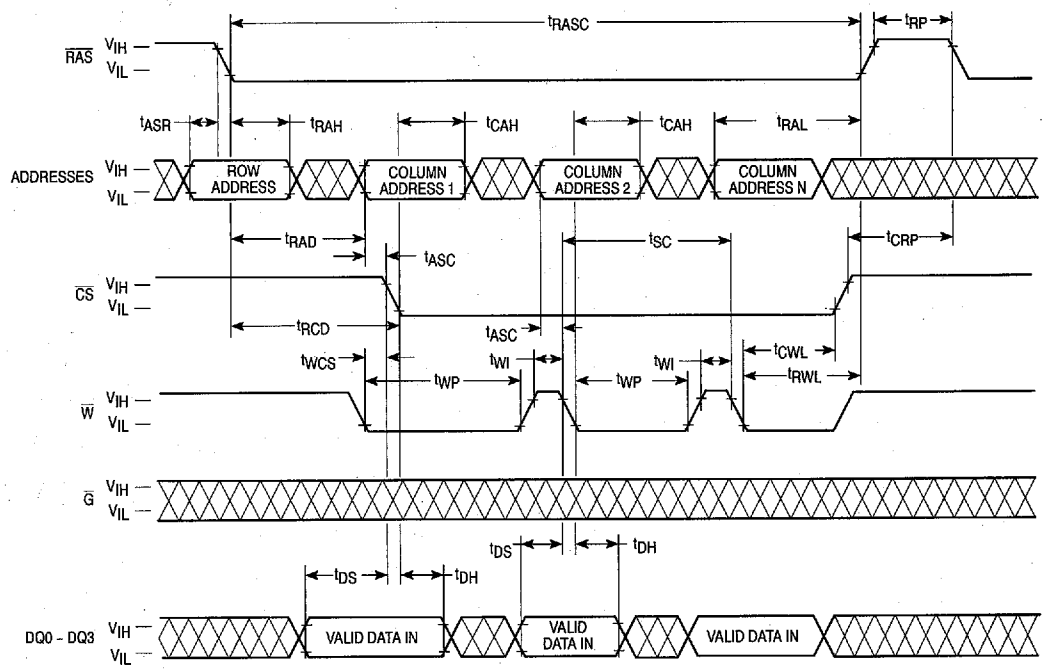

## TEST MODE — STATIC COLUMN MODE READ CYCLE



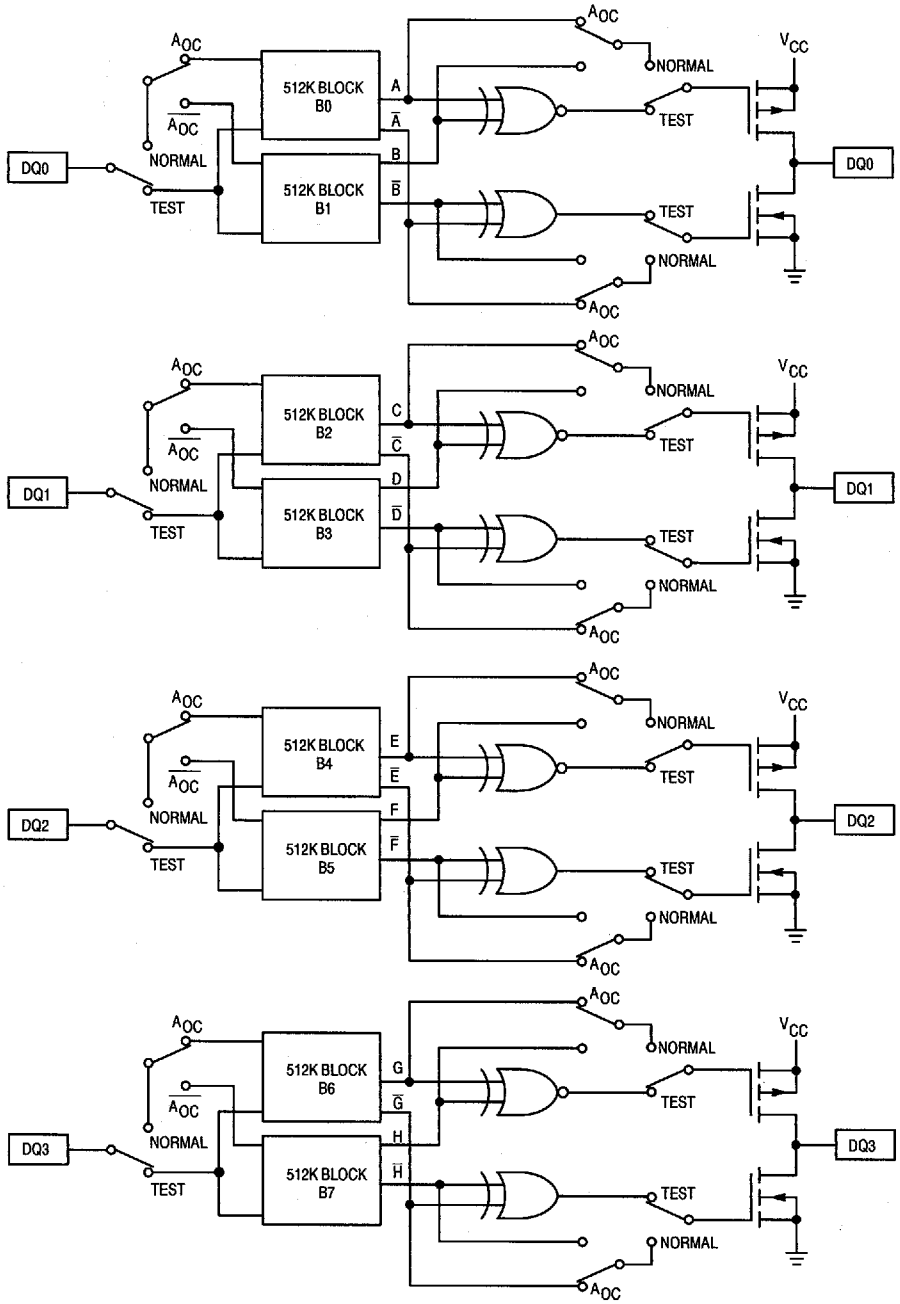
## TEST MODE – STATIC COLUMN MODE EARLY WRITE CYCLE (A)



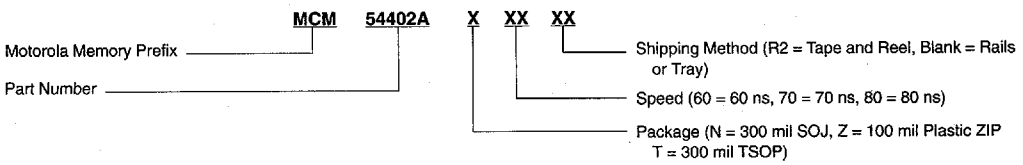

## TEST MODE – STATIC COLUMN MODE EARLY WRITE CYCLE (B)



**TEST MODE BLOCK DIAGRAM**



## ORDERING INFORMATION
**(Order by Full Part Number)**




| Full Part Numbers — | | | | |
|---|---|---|---|---|
| | MCM54402AN60 | MCM54402AN60R2 | MCM54402AZ60 | MCM54402AT60 |
| | MCM54402AN70 | MCM54402AN70R2 | MCM54402AZ70 | MCM54402AT70 |
| | MCM54402AN80 | MCM54402AN80R2 | MCM54402AZ80 | MCM54402AT80 |

NOTE: For mechanical data, please see Chapter 10.

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