

BB304C

Build in Biasing Circuit MOS FET IC UHF/VHF RF Amplifier

HITACHI

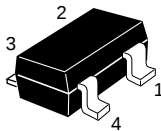
ADE-208-606C (Z)
4th. Edition
August 1998

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- High gain;
(PG = 29 dB typ. at $f = 200$ MHz)
- Low noise characteristics;
(NF = 1.2 dB typ. at $f = 200$ MHz)
- Wide supply voltage range;
Applicable with 5V to 9V supply voltage.
- Withstanding to ESD;
Build in ESD absorbing diode. Withstand up to 200V at $C=200\text{pF}$, $R_s=0$ conditions.
- Provide mini mold packages; CMPAK-4(SOT-343mod)

Outline

CMPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

Notes: 1 Marking is "DW-".

2. BB304C is individual type number of HITACHI BBFET.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DS}	12	V
Gate1 to source voltage	V _{G1S}	+10 -0	V
Gate2 to source voltage	V _{G2S}	±10	V
Drain current	I _D	25	mA
Channel power dissipation	P _{ch}	100	mW
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	12	—	—	V	I _D = 200μA, V _{G1S} = V _{G2S} = 0
Gate1 to source breakdown voltage	V _{(BR)G1SS}	+10	—	—	V	I _{G1} = +10μA, V _{G2S} = V _{DS} = 0
Gate2 to source breakdown voltage	V _{(BR)G2SS}	±10	—	—	V	I _{G2} = +10μA, V _{G1S} = V _{DS} = 0
Gate1 to source cutoff current	I _{G1SS}	—	—	+100	nA	V _{G1S} = +9V, V _{G2S} = V _{DS} = 0
Gate2 to source cutoff current	I _{G2SS}	—	—	±100	nA	V _{G2S} = +9V, V _{G1S} = V _{DS} = 0
Gate1 to source cutoff voltage	V _{G1S(off)}	0.4	—	1.0	V	V _{DS} = 5V, V _{G2S} = 4V I _D = 100μA
Gate2 to source cutoff voltage	V _{G2S(off)}	0.5	—	1.0	V	V _{DS} = 5V, V _{G1S} = 5V I _D = 100μA

Electrical Characteristics (Ta = 25°C)

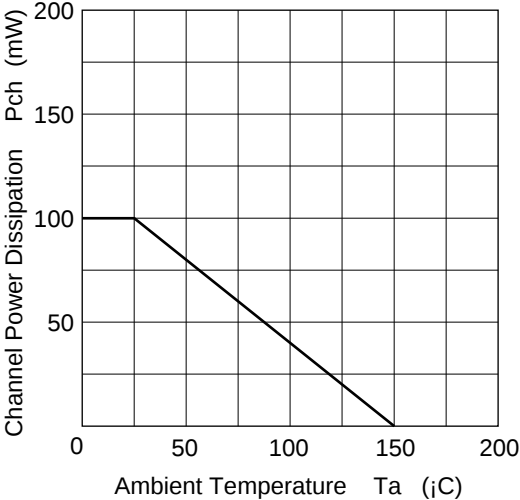
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{iss}	2.3	2.8	3.6	pF	$V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V$
Output capacitance	C_{oss}	0.9	1.3	2.0	pF	$R_G = 180k\Omega, f = 1MHz$
Reverse transfer capacitance	C_{rss}	0.003	0.02	0.05	pF	
Drain current	$I_{D(op)1}$	9	14	19	mA	$V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V$ $R_G = 180k\Omega$
	$I_{D(op)2}$	—	13	—	mA	$V_{DS} = 9V, V_{G1} = 9V, V_{G2S} = 6V$ $R_G = 470k\Omega$
Forward transfer admittance	$ y_{fs} 1$	22	27	34	mS	$V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V$ $R_G = 180k\Omega, f = 1kHz$
	$ y_{fs} 2$	—	27	—	mS	$V_{DS} = 9V, V_{G1} = 9V, V_{G2S} = 6V$ $R_G = 470k\Omega, f = 1kHz$
Power gain	PG1	24	29	32	dB	$V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V$ $R_G = 180k\Omega, f = 200MHz$
	PG2	—	29	—	dB	$V_{DS} = 9V, V_{G1} = 9V, V_{G2S} = 6V$ $R_G = 470k\Omega, f = 200MHz$
Noise figure	NF1	—	1.2	1.9	dB	$V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V$ $R_G = 180k\Omega, f = 200MHz$
	NF2	—	1.2	—	dB	$V_{DS} = 9V, V_{G1} = 9V, V_{G2S} = 6V$ $R_G = 470k\Omega, f = 200MHz$

The diagram shows a two-terminal device with two gates, Gate 1 and Gate 2. Gate 1 is connected to a voltage source V_{G1} through a resistor R_G . Gate 2 is connected to a voltage source V_{G2} . The drain and source terminals are connected to a current source I_D and ground, respectively. The device is represented by a central rectangle with four terminals: Gate 1, Gate 2, Drain, and Source.

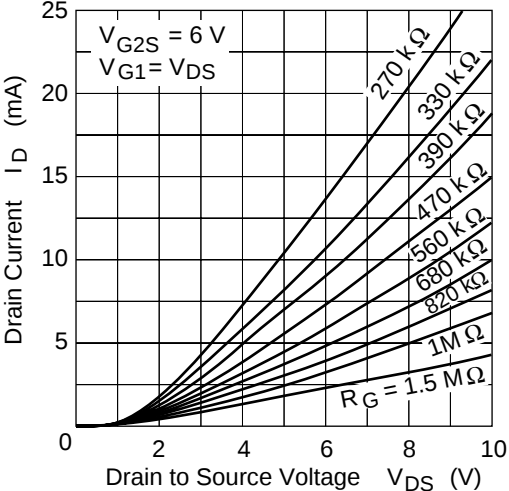
Unit Resistance (Ω)
Capacitance (F)

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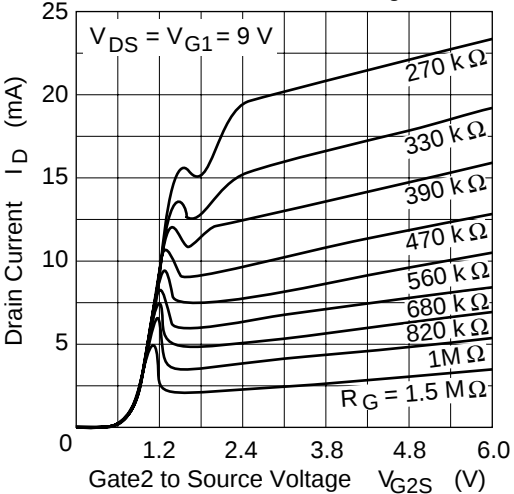
Maximum Channel Power
Dissipation Curve



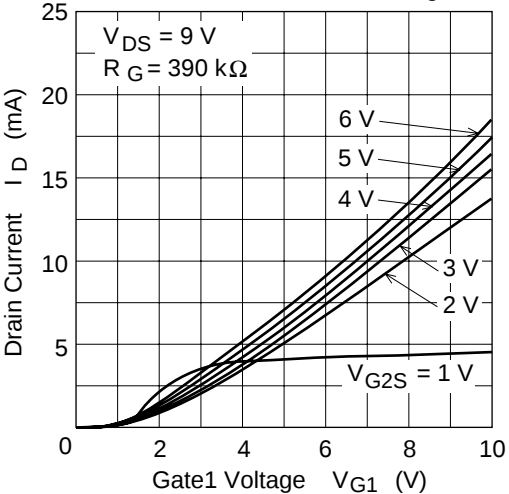
Typical Output Characteristics

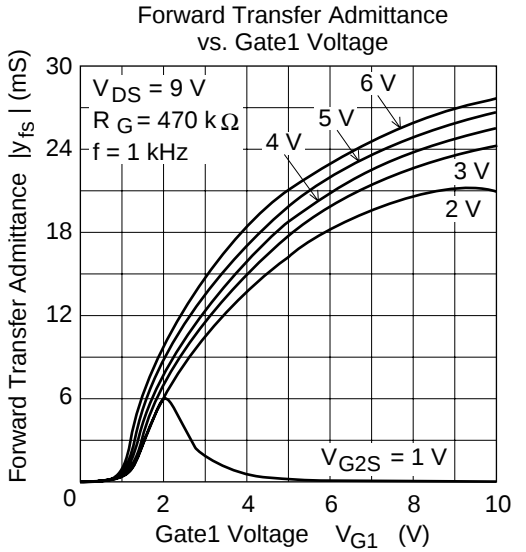
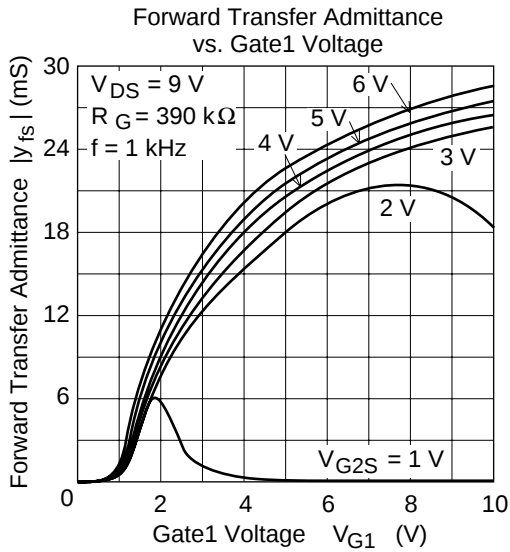
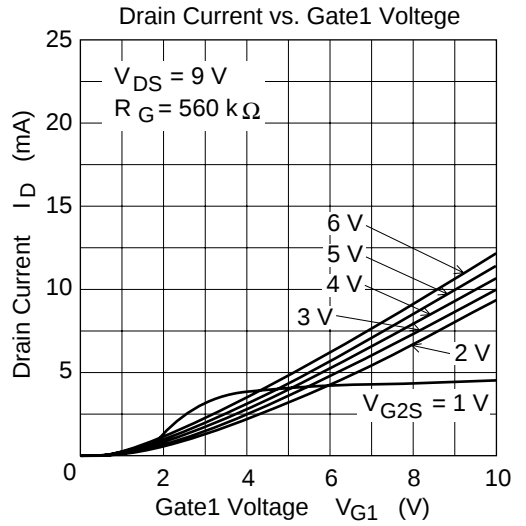
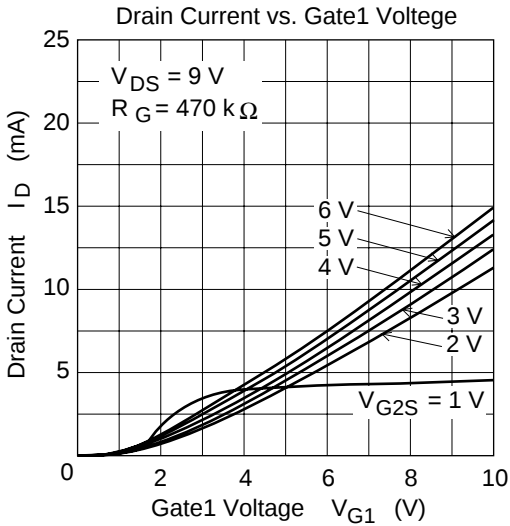


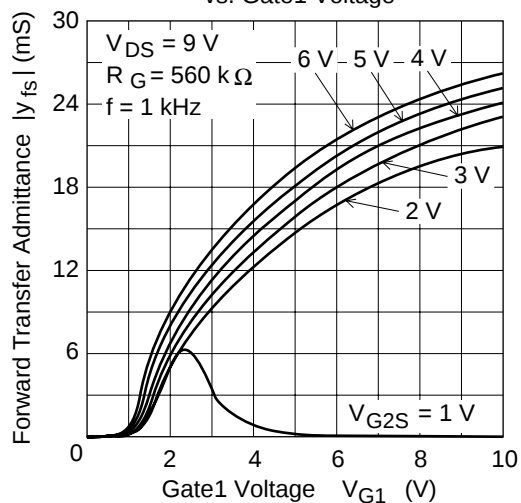
Drain Current vs.
Gate2 to Source Voltage



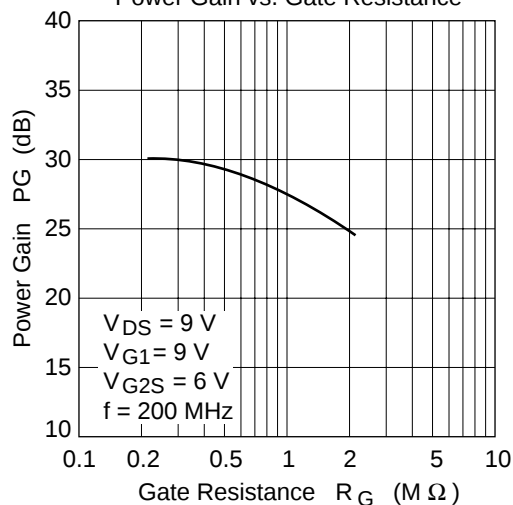
Drain Current vs. Gate1 Voltage



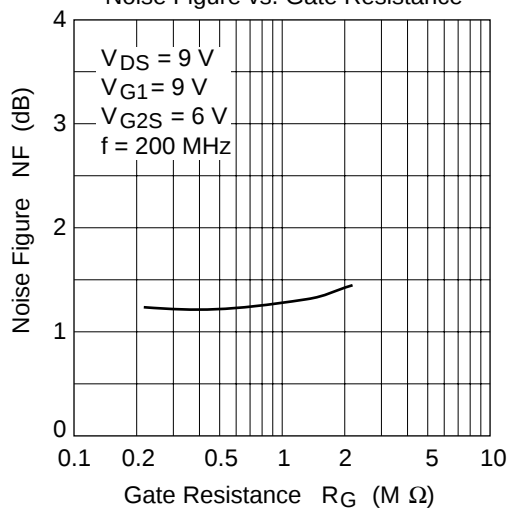


Forward Transfer Admittance
vs. Gate1 Voltage

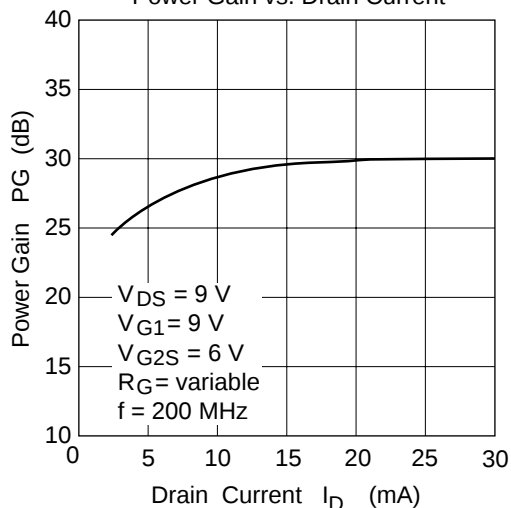
Power Gain vs. Gate Resistance

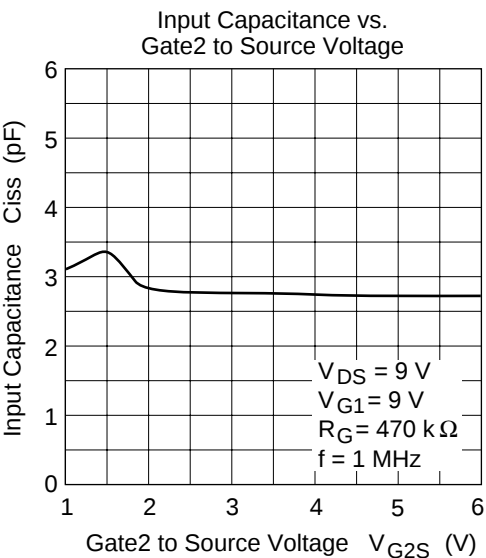
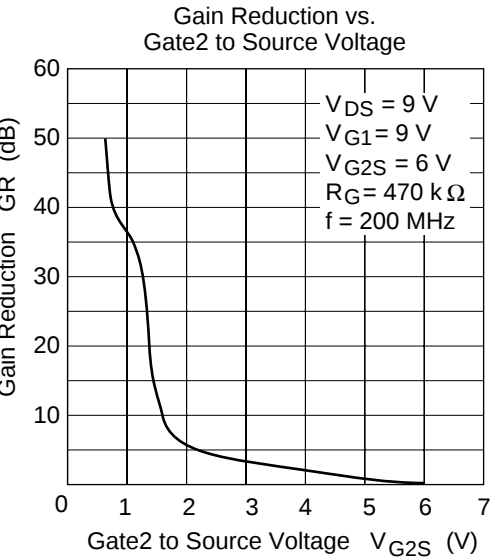
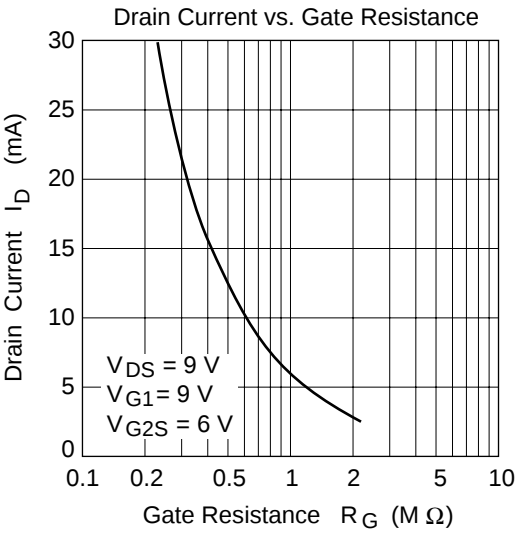
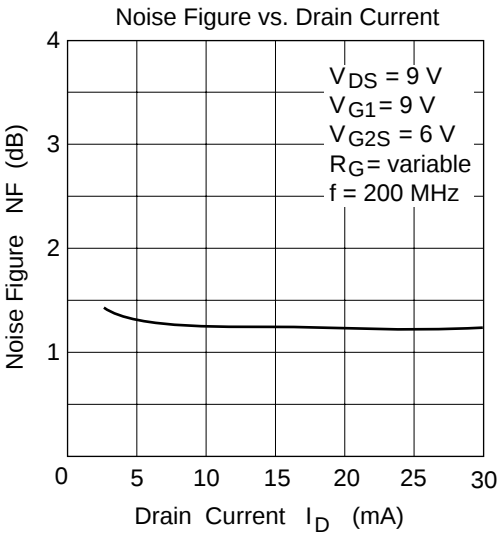


Noise Figure vs. Gate Resistance

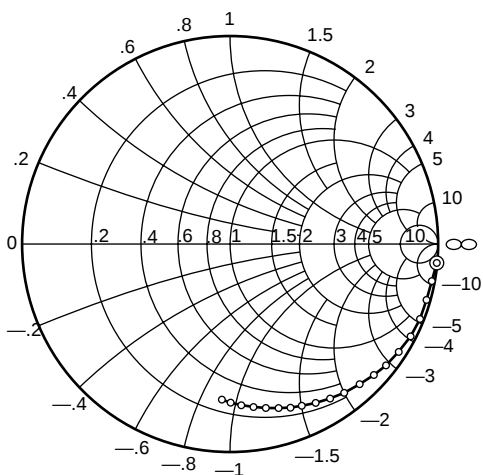


Power Gain vs. Drain Current





S11 Parameter vs. Frequency

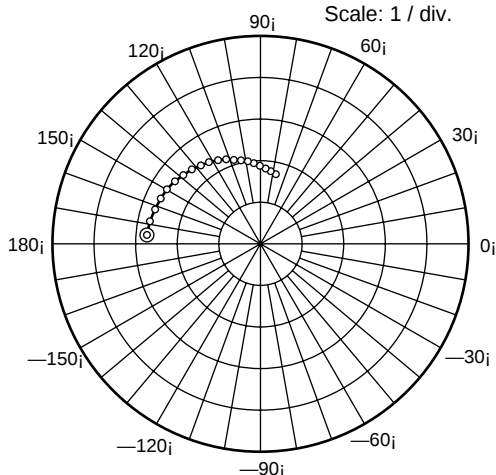


Test Condition : $V_{DS} = 9\text{ V}$, $V_{G1} = 9\text{ V}$
 $V_{G2S} = 6\text{ V}$, $R_G = 470\text{ k}\Omega$
 50 1000 MHz (50 MHz step)

⊙—○

S21 Parameter vs. Frequency

Scale: 1 / div.

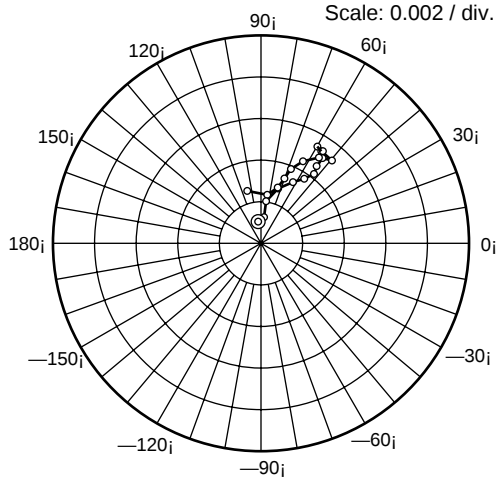


Test Condition : $V_{DS} = 9\text{ V}$, $V_{G1} = 9\text{ V}$
 $V_{G2S} = 6\text{ V}$, $R_G = 470\text{ k}\Omega$
 50 1000 MHz (50 MHz step)

⊙—○

S12 Parameter vs. Frequency

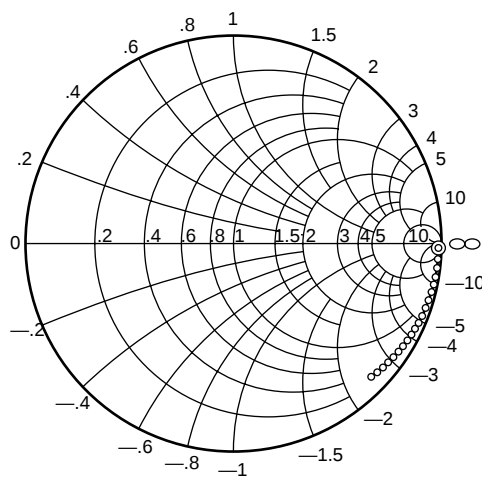
Scale: 0.002 / div.



Test Condition : $V_{DS} = 9\text{ V}$, $V_{G1} = 9\text{ V}$
 $V_{G2S} = 6\text{ V}$, $R_G = 470\text{ k}\Omega$
 50 1000 MHz (50 MHz step)

⊙—○

S22 Parameter vs. Frequency



Test Condition : $V_{DS} = 9\text{ V}$, $V_{G1} = 9\text{ V}$
 $V_{G2S} = 6\text{ V}$, $R_G = 470\text{ k}\Omega$
 50 1000 MHz (50 MHz step)

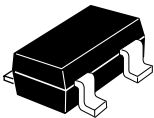
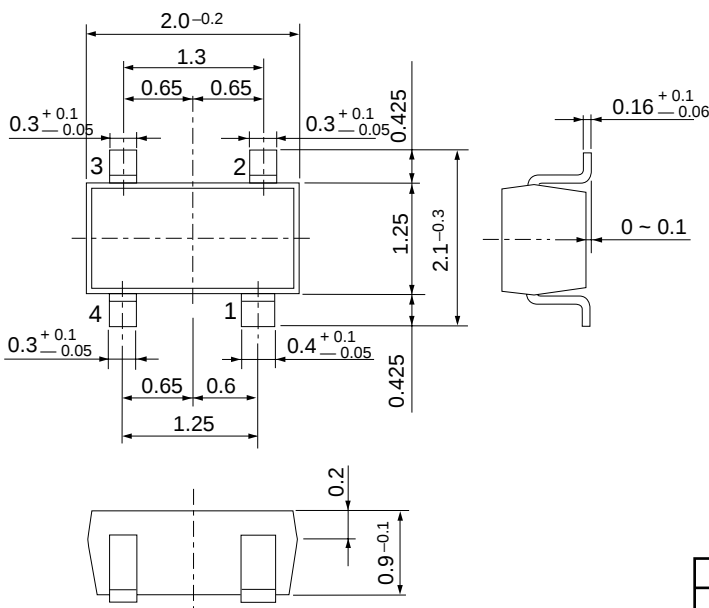
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Sparameter ($V_{DS} = V_{G1} = 9V$, $V_{G2S} = 6V$, $R_G = 470k\Omega$, $Z_o = 50\Omega$)

f (MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.996	−5.3	2.74	174.0	0.00096	98.6	0.985	−1.9
100	0.993	−10.9	2.73	168.0	0.00130	84.4	0.991	−4.5
150	0.987	−16.6	2.68	162.3	0.00203	83.6	0.990	−6.5
200	0.978	−21.9	2.66	156.3	0.00285	72.3	0.988	−9.4
250	0.972	−27.4	2.63	150.4	0.00335	69.7	0.985	−11.6
300	0.954	−33.2	2.57	144.3	0.00385	68.3	0.982	−14.0
350	0.943	−38.2	2.50	138.7	0.00455	63.2	0.979	−16.2
400	0.925	−43.2	2.43	133.3	0.00488	55.4	0.975	−18.4
450	0.910	−48.0	2.37	128.0	0.00526	59.8	0.971	−21.0
500	0.893	−52.5	2.30	122.6	0.00522	56.1	0.967	−23.0
550	0.880	−57.4	2.24	117.5	0.00498	53.2	0.962	−25.2
600	0.861	−62.1	2.17	112.7	0.00512	49.1	0.957	−27.3
650	0.847	−66.1	2.10	108.1	0.00497	53.4	0.952	−29.4
700	0.829	−69.9	2.02	103.6	0.00455	53.6	0.947	−31.6
750	0.816	−74.1	1.96	99.1	0.00418	51.6	0.943	−33.7
800	0.804	−78.2	1.91	94.8	0.00372	55.7	0.937	−35.8
850	0.791	−82.4	1.85	80.4	0.00329	62.4	0.933	−38.0
900	0.779	−86.1	1.79	86.3	0.00275	73.0	0.928	−40.0
950	0.764	−89.5	1.73	82.2	0.00233	82.4	0.921	−42.1
1000	0.753	−92.4	1.68	78.3	0.00258	105.1	0.918	−44.2

Package Dimensions

Unit: mm



Hitachi Code	CMPAK-4
EIAJ	SC-82AB
JEDEC	

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