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# SP8602 500MHz ÷ 2

# SP8604 300MHz ÷ 2

The SP8602 and SP8604 are emitter coupled logic dividers which feature ECL10K compatible outputs when used with external pulldown resistors. The inputs are AC coupled.

### FEATURES

- ECL Compatible Outputs
- AC-Coupled Inputs (Internal Bias)

### QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 85mW
- Temperature Range:
  - 55°C to +125°C (A Grade)
  - 30°C to +70°C (B Grade)

### ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{EE}$	-8V
Output current	10mA
Storage temperature range	-65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2.5V p-p

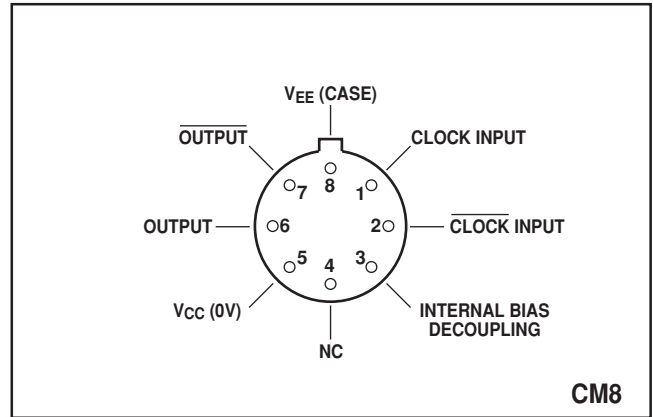


Fig. 1 Pin connections - bottom view

### ORDERING INFORMATION

- SP8602 A CM
- SP8602 B CM
- SP8604 A CM
- SP8604 B CM
- 5962-92059 (SMD) (SP8602)

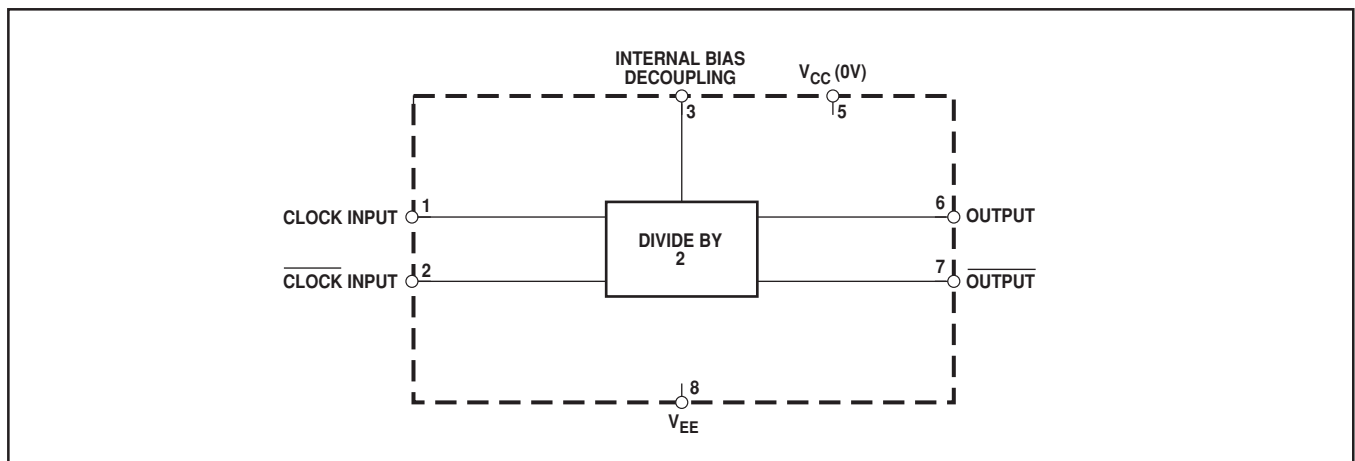


Fig. 2 Functional diagram

**ELECTRICAL CHARACTERISTICS**

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

Supply voltage,  $V_{CC} = 0V$ ,  $V_{EE} = -5.2V \pm 0.25V$

Temperature,  $T_{AMB} = -55^{\circ}C$  to  $+125^{\circ}C$  (A Grade),  $-30^{\circ}C$  to  $+70^{\circ}C$  (B Grade)

Characteristic	Symbol	Value		Units	Type	Conditions	Notes
		Min.	Max.				
Maximum frequency (sinewave input)	$f_{MAX}$	500		MHz	SP8602	Input = 400-800mV p-p	
		300		MHz	SP8604	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	$f_{MIN}$		40	MHz	Both	Input = 400-800mV p-p	
Power supply current	$I_{EE}$		18	mA	Both	$V_{EE} = -5.2V$ , outputs unloaded	
Output low voltage	$V_{OL}$	-1.8	-1.4	V	Both	$V_{EE} = -5.2V$	3
Output high voltage	$V_{OH}$	-0.85	-0.7	V	Both	$V_{EE} = -5.2V$	3
Minimum output swing	$V_{OUT}$	400		mV	Both	$V_{EE} = -5.2V$	

NOTES

1. The temperature coefficients of  $V_{OH} = +1.63mV/^{\circ}C$ , and  $V_{OL} = +0.34mV/^{\circ}C$  but these are not tested.
2. The test configuration for dynamic testing is shown in Fig.5.
3. Tested at  $25^{\circ}C$  only.

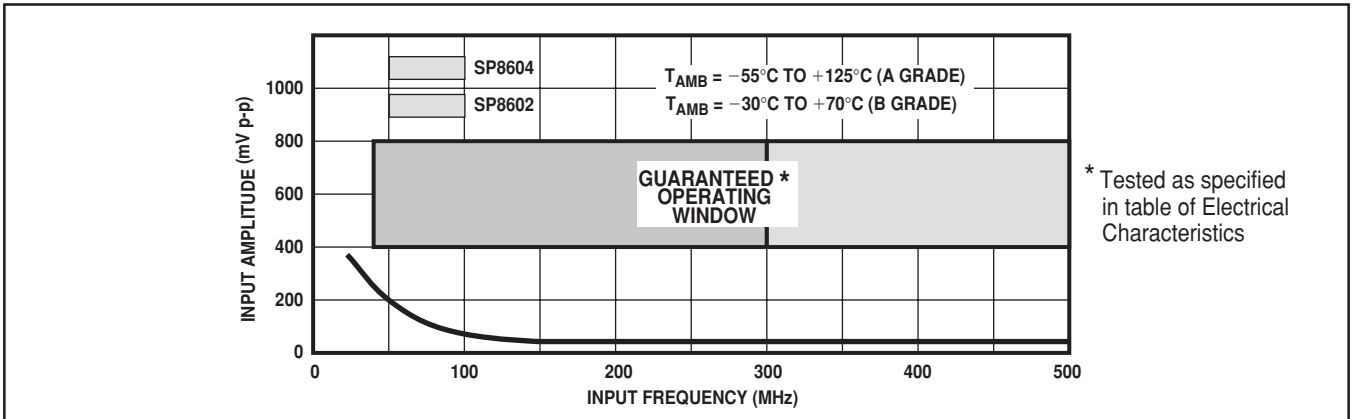


Fig. 3 Typical input characteristics of SP8602 and SP8604

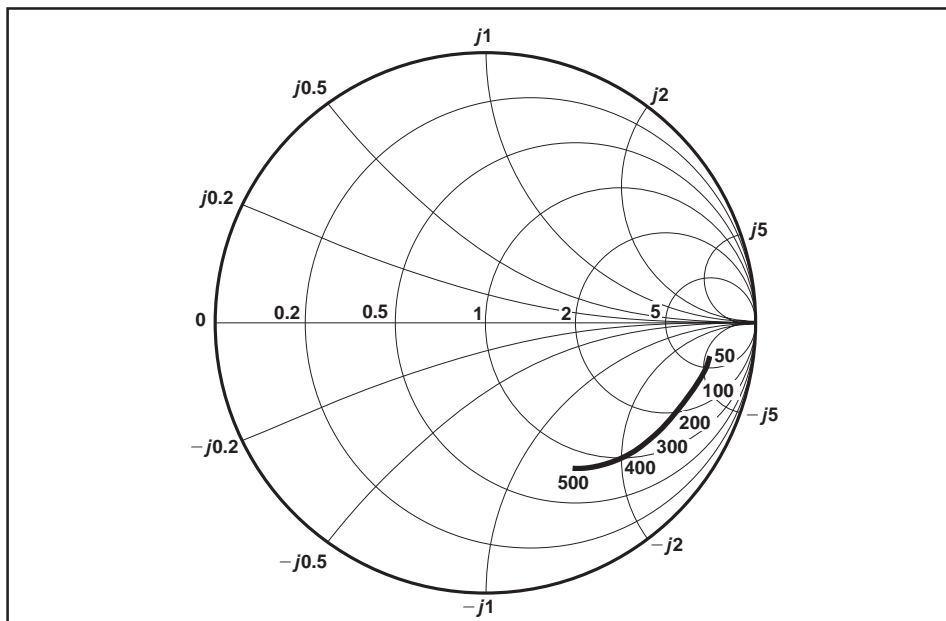


Fig. 4 Typical input impedance. Test conditions: supply voltage =  $-5.2V$ , ambient temperature =  $25^{\circ}C$ , frequencies in MHz, Impedances normalised to  $50\Omega$

**OPERATING NOTES**

1. The clock inputs (pins 1 and 2) can be driven single ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 3, to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 15kΩ resistor from the unused input to V<sub>EE</sub>. This will reduce the input sensitivity by approximately 100mV.

3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The outputs are compatible with ECLII. There is an internal load of 4kΩ on each output. The outputs can be interfaced to ECL10K by the addition of 1.5kΩ pull-down resistors from the outputs to V<sub>EE</sub> to increase output voltage swing.
5. Input impedance is a function of frequency, See Fig. 4.
6. All components should be suitable for the frequency in use.

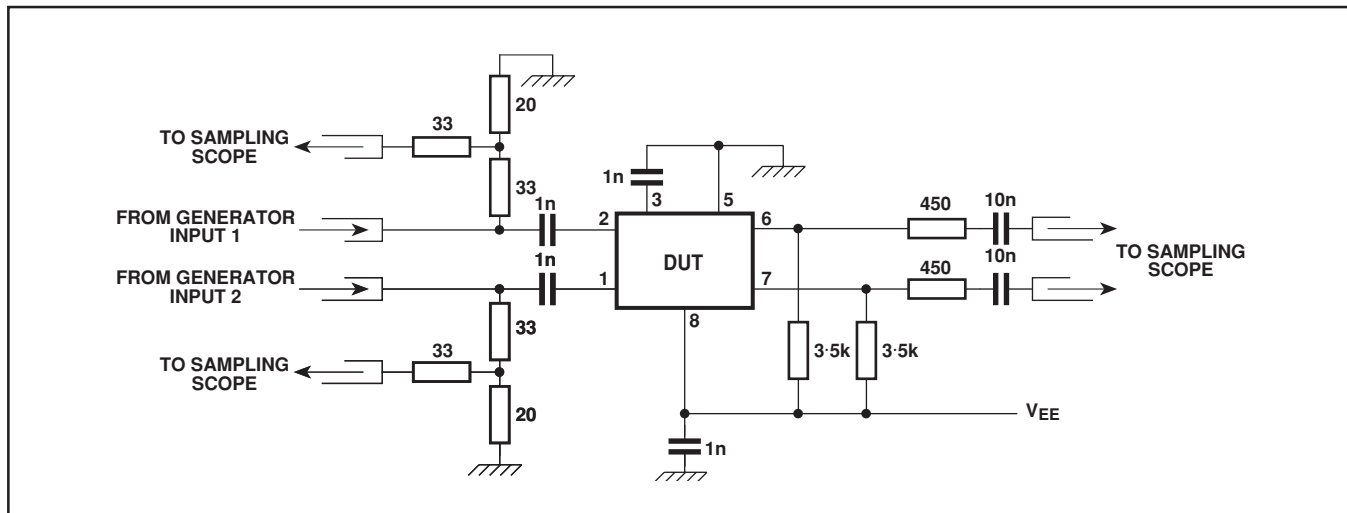


Fig. 5 Test circuit

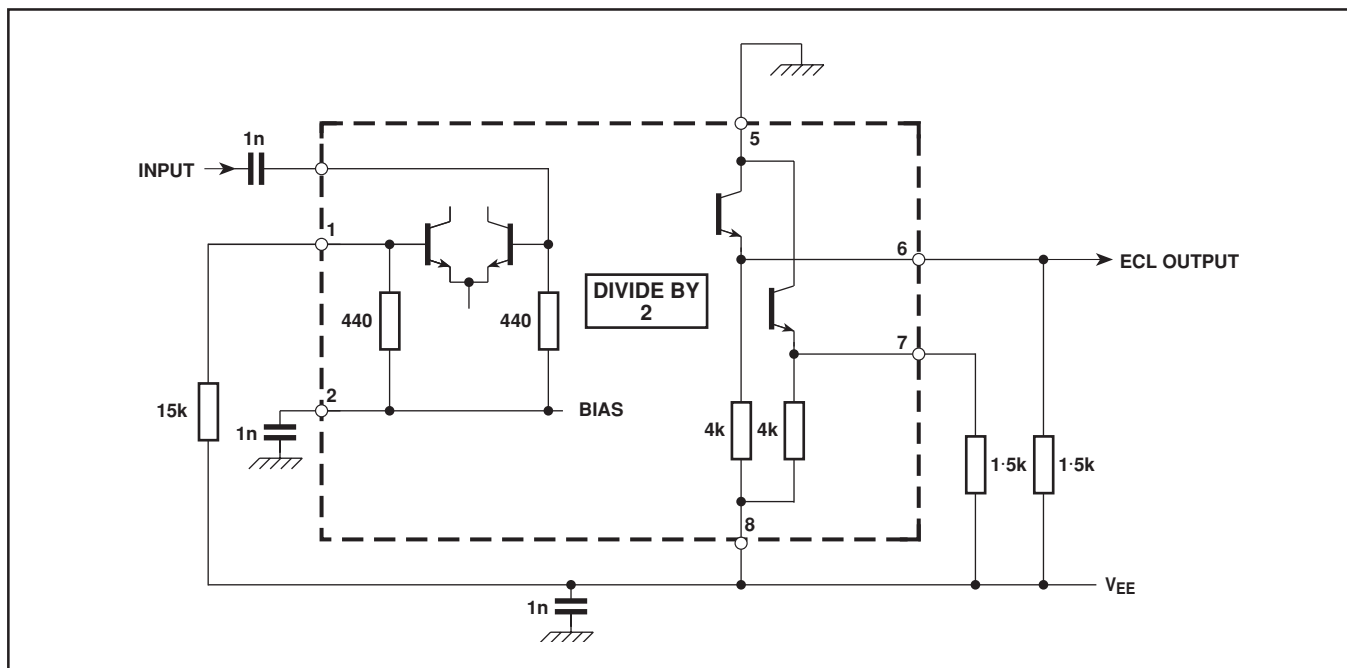
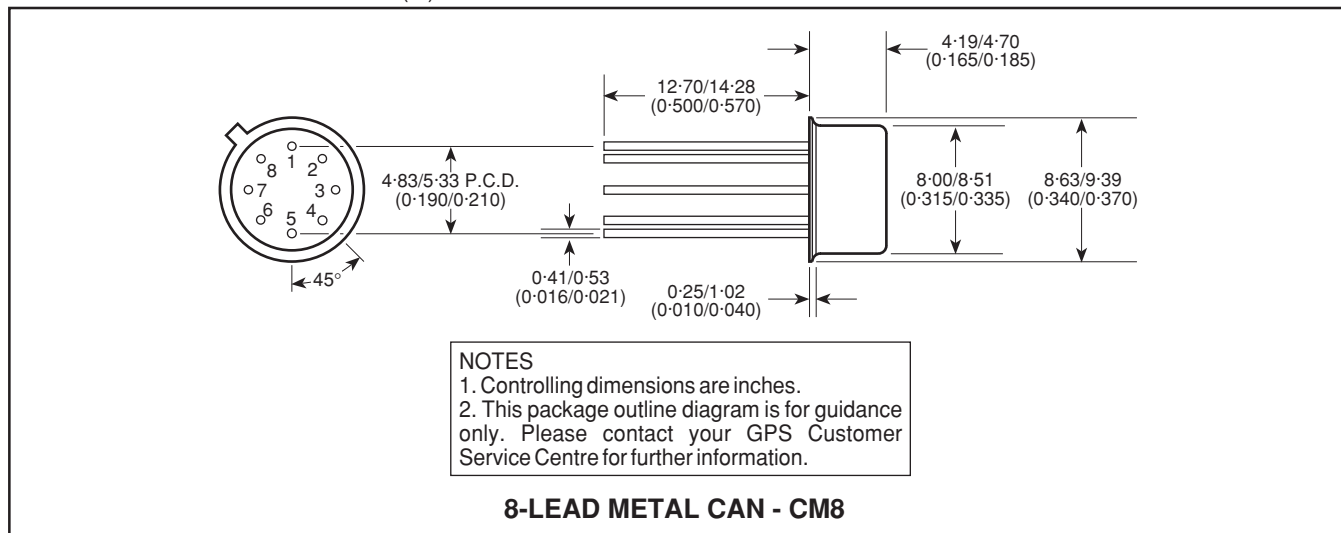


Fig. 6 Typical application showing interfacing

**PACKAGE DETAILS**

Dimensions are shown thus: mm (in).



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